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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	01/03/2017	9535490	141062/1173-141	3463

115309 7590 12/14/2016

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 119 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Vinod Harimohan Kaushik, San Diego, CA;
QUALCOMM Incorporated, San Diego, CA;
Uppinder Singh Babbar, San Diego, CA;
Andrei Danaila, San Diego, CA;
Neven Klacar, San Diego, CA;
Muralidhar Coimbatore Krishnamoorthy, San Diego, CA;
Arunn Coimbatore Krishnamurthy, San Diego, CA;
Vaibhav Kumar, Encinitas, CA;
Vanitha Aravamudhan Kumar, San Diego, CA;
Shailesh Maheshwari, San Diego, CA;
Alok Mitra, San Diego, CA;
Roshan Thomas Pius, San Jose, CA;
Hariharan Sukumar, San Diego, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

INTEL 1403

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

115309 7598 11/01/2016
W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141	3463

TITLE OF INVENTION: POWER SAVING TECHNIQUES IN COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/01/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHURY, ZAHID	2116	713-320000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Withrow + Terranova, PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: QUALCOMM Incorporated

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Diego, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 501732 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Taylor M. Davenport/ Date November 23, 2016
Typed or printed name Taylor M. Davenport Registration No. 42,466

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 23696

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	14/568,694

Completed by (check one):

☐ Applicant/Inventor — /Taylor M. Davenport/ (Signature)

☑ Attorney or Agent of record 42,466 (Reg. No.) — Taylor M. Davenport (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — 919-238-2300 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame _____ — November 23, 2016 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 m inutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alex andria, VA 22313- 1450. DO NOT SEND COMPLETE D FORMS TO THIS A DDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	14568694
Filing Date:	12-Dec-2014
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Filer:	Taylor M. Davenport/David Smith
Attorney Docket Number:	141062/1173-141

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	27607674
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/David Smith
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	23-NOV-2016
Filing Date:	12-DEC-2014
Time Stamp:	16:44:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	112516INTEFSW16453100
Deposit Account	501732
Authorized User	David Smith

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	141062_IssueFeeTransmittal_11-23-16_AsFiled.PDF	110340 ec2411a2eedd663c7a59ad6a19511931 6d4 6f5f	no	1
Warnings:					
Information:					
2	Maintenance Fee Address Change	141062_FeeAddressIndication_11-23-16_AsFiled.pdf	203941 cdd99a5ec4c2667e2551d09d7c0345e7 7d6 2a9	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31025 3d8faaa1a82f4886 2dc7bbd3cad61e75bfb8e 7652	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	345306		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

115309 7590 11/01/2016

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

EXAMINER
CHOUDHURY, ZAHID

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/01/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141	3463

TITLE OF INVENTION: POWER SAVING TECHNIQUES IN COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/01/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

115309 7590 11/01/2016
W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141	3463

TITLE OF INVENTION: POWER SAVING TECHNIQUES IN COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/01/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHURY, ZAHID	2116	713-320000

1. Change of correspondence address or Indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141	3463

115309 7590 11/01/2016

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

EXAMINER
CHOUDHURY, ZAHID

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/01/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/568,694	Applicant(s) KAUSHIK ET AL.	
	Examiner ZAHID CHOUDHURY	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/24/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-31*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 07/01/2016
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ZAHID CHOUDHURY/
Primary Examiner, Art Unit 2116

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Reason for Allowance

The following is an examiner's statement of reasons for allowance:

Interpreting the claims in light of the specification and based on applicant's argument filed on 08/24/2016 examiner finds the claimed invention is patentably distinct from the prior art of record. The prior art does not expressly teach or render obvious the invention as recited in the independent claims 1,15,20,24,25,26,27,28 and 29.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ZAHID CHOUDHURY whose telephone number is (571)270-5153. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huynh Kim can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ZAHID CHOUDHURY/
Primary Examiner, Art Unit 2116

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	459112	(hold$3 delay$3) near5 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:53
S2	602163	(rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S3	459112	S1 with S1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S4	1324	S1 with S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S5	292	S4 same (CPU proceossr controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:55
S6	1	S5 same (cell mobile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:55
S7	4	"2013198538"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:19
S8	26	"2009039034"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:23
S9	2018	(hold$3 delay$3 wait$3) near5 until near5 data near5 (send$3 sent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:29
S10	123	S9 with (CPU proceossr controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:30

S11	1	S10 same (rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:30
S12	10	S10 and (rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:39
S13	31	"5727233"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:05
S14	91956	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem) near5 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:08
S15	92000	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem) near5 data$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:08
S16	1871	S15 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:09
S17	0	S6 and 713/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:10
S18	38	S16 and 713/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:10
S19	97	S16 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:18
S20	93263	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem uplink downlink) near5 data$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:19
S21	1890	S20 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:20
S22	97	S21 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:20

S23	27	"7137018"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:33
S24	959	(hold$3 delay$3 wait$3) near5 data near6 modem	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:44
S25	58	S24 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:44
S26	3	"20130198538"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:58
S27	86	(hold$3 delay$3 wait$3) near5 data near6 modem near8 until	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:03
S28	47	(hold$3 delay$3 wait$3) near5 data near6 router near8 until	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:15
S29	25541	data near6 collision	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:17
S30	349	S29 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:17
S31	88	(hold$3 delay$3 wait$3) same S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:17
S32	44285	(hold$3 delay$3 wait$3) same (modem router)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:18
S33	88	S31 same (modem router)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:18
S34	4246	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till) near6 (receipt received)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:21

S35	59	S34 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:22
S36	33273	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:24
S37	1074	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till) near5 (bus PCI PCIE serial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:24
S38	59	S35 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:25
S39	9	S37 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:25
S40	42	S37 with (clear free idle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:26
S41	5731	(avoid$3 prevent$3) near5 data near6 collision	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:17
S42	4	S41 near6 ((network adj card) modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:17
S43	31	S41 same ((network adj card) modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:19
S44	473	S41 near6 (PCI PCIE bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:22
S45	49	(hold$3 delay$3 wait$3) same S44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:22
S46	2	"9158628"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 09:01

S47	50181	(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:13
S48	2018	(hold$3 delay$3 wait$3) near5 until near5 data near5 (send$3 sent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:14
S49	10	S48 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:14

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10907	(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10)	US-PGPUB; USPAT	OR	OFF	2016/10/26 16:50
L2	2	responsive near5 recipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:28
L3	0	processor near6 hold near6 aplicaion near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:29
L4	0	aplicaion near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:29
L5	0	applicaion near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:29
L6	25964	application near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:29
L7	1	processor near6 hold near6 application near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:30
L8	27	hold near6 application near10 receipt	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:30
L9	4	8.clm.	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:30
L10	0	9 and 1	US-PGPUB; USPAT	OR	OFF	2016/10/26 17:30

10/26/2016 5:30:57 PM
C:\Users\zchoudhury\Documents\EAST\Workspaces\14568694.wsp

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BIB DATA SHEET

CONFIRMATION NO. 3463

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/568,694	12/12/2014	713	2116	141062/1173-141

APPLICANTS

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**** CONTINUING DATA ***************************

This appln claims benefit of 61/916,498 12/16/2013
and claims benefit of 62/019,073 06/30/2014

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/24/2014

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ZAHID CHOUDHURY/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	13	29	9

ADDRESS

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511
UNITED STATES

TITLE

POWER SAVING TECHNIQUES IN COMPUTING DEVICES

FILING FEE RECEIVED		
5140	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

| CPC | | |

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		G	0	6	F	1/32 (2006.01.01)						

CROSS REFERENCE(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	31	
/ZAHID CHOUDHURY/ Primary Examiner.Art Unit 2116	10/26/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	18	17												
2	2	19	18												
3	3	20	19												
4	4	22	20												
6	5	23	21												
7	6	24	22												
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11	11	29	27												
12	12	30	28												
13	13	31	29												
14	14	15	30												
16	15	21	31												
17	16														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	31	
/ZAHID CHOUDHURY/ Primary Examiner.Art Unit 2116	10/26/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

CPC- SEARCHED		
Symbol	Date	Examiner
(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10)	6/6/2016	ZC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
NPL Search: Google. Google Patent	6/6/2016	ZC
East Search History is attached	6/6/2016	ZC
Updated East Search History	10/26/2016	ZC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/ZAHID CHOUDHURY/ Primary Examiner.Art Unit 2116

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10)		10/26/2016	ZC

	/ZAHID CHOUDHURY/ Primary Examiner.Art Unit 2116

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14568694
Filing Date	2014-12-12
First Named Inventor	Vinod Harimohan Kaushik
Art Unit	2116
Examiner Name	Zahid Choudhury
Attorney Docket Number	141062/1173-141

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Receipt date: 07/01/2016 14568694 - GAU: 2116

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Art Unit	2116
Examiner Name	Zahid Choudhury
Attorney Docket Number	141062/1173-141

	1	International Preliminary Report on Patentability for PCT/US2014/070368, mailed April 1, 2016, 33 pages	

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EXAMINER SIGNATURE

Examiner Signature	/ZAHID CHOUDHURY/	Date Considered	10/26/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	14568694
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First Named Inventor	Vinod Harimohan Kaushik
Art Unit	2116
Examiner Name	Zahid Choudhury
Attorney Docket Number	141062/1173-141

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

X That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2016-07-01
Name/Print	Taylor M. Davenport	Registration Number	42466

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	14/568,694	Confirmation No.: 3463
Applicant:	QUALCOMM Incorporated	
First Named Inventor:	Vinod Harimohan Kaushik et al.	
Filed:	12/12/2014	
Art Unit:	2116	
Examiner:	Zahid Choudhury	
Title:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	
Docket No.:	141062/1173-141	
Customer No.:	115309	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY PURSUANT TO
37 CFR § 1.111

Sir:

In response to the Office Action mailed June 10, 2016, please find enclosed Applicant's reply:

Amendments to the Claims are reflected in the listing of claims beginning on page **2**.

Remarks begin on page **10** of this paper.

In the Claims:

1. (Currently Amended) A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

2. (Original) The mobile terminal of claim 1, wherein the interconnectivity bus comprises a peripheral component interconnect (PCI) compliant bus.

3. (Original) The mobile terminal of claim 2, wherein the PCI compliant bus comprises a PCI express (PCIe) bus.

4. (Original) The mobile terminal of claim 1, wherein the application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer.

5. (Original) The mobile terminal of claim 1, wherein the modem timer is implemented in software.

6. (Original) The mobile terminal of claim 1, wherein the modem timer has a period of approximately six (6) milliseconds.

7. (Original) The mobile terminal of claim 4, wherein the application processor is configured to hold the application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first.

8. (Original) The mobile terminal of claim 1, wherein the modem processor comprises the modem timer.

9. (Original) The mobile terminal of claim 1, wherein the application processor comprises the modem timer.

10. (Original) The mobile terminal of claim 1, further comprising an application timer, and wherein the modem processor is configured to instruct the application processor to send an interrupt if no data is received within one time slot of the application timer.

11. (Original) The mobile terminal of claim 1, further comprising a byte accumulation limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the byte accumulation limit counter is exceeded.

12. (Original) The mobile terminal of claim 1, further comprising a packet number limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the packet number limit counter is exceeded.

13. (Original) The mobile terminal of claim 1, wherein the modem processor is configured to determine if held data comprises a control packet and send such control packet before expiration of the modem timer.

14. (Original) The mobile terminal of claim 3, wherein the modem processor further comprises an application timer, and the modem processor is configured to pull data from the application processor on receipt of the modem processor to application processor data or expiration of the application timer.

15. (Currently Amended) A method of controlling power consumption in a computing device, comprising:

holding data received by a modem processor from a remote network until expiration of a downlink timer;

passing the data received by the modem processor to an application processor over an interconnectivity bus; and

holding application data generated by an application associated with the application processor until receipt of the data from the modem processor or expiration of an uplink timer, whichever occurs first,

wherein receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state.

16. (Original) The method of claim 15, wherein passing the data comprises passing the data over a peripheral component interface (PCI) compliant bus.

17. (Original) The method of claim 15, wherein a period of the downlink timer comprises six (6) milliseconds.

18. (Original) The method of claim 15, wherein a period of the uplink timer comprises seven (7) milliseconds.

19. (Original) The method of claim 15, further comprising providing an override capability based on one of accumulated packet size, accumulated packet count, accumulated byte count, quality of service requirement, and control message status.

20. (Currently Amended) A mobile terminal comprising:

a modem processor;

an application timer;

an application processor, the application processor configured to hold application processor to modem processor data until expiration of the application timer;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the application processor to modem processor data from the application processor through the interconnectivity bus.

21. (Original) The mobile terminal of claim 20, wherein the application processor comprises the application timer.

22. (Original) The mobile terminal of claim 20, wherein the modem processor comprises the application timer.

23. (Original) The mobile terminal of claim 20, further comprising a byte counter counting bytes at the modem processor.

24. (Currently Amended) A mobile terminal comprising:

a modem byte accumulation limit counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

25. (Currently Amended) A mobile terminal comprising:

a modem packet counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of packets has been reached by the modem packet counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem

processor to application processor data from the modem processor through the interconnectivity bus.

26. (Currently Amended) A mobile terminal comprising:

a modem processor;

an application byte counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of bytes has been reached by the application byte counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the application processor to modem processor data from the application processor through the interconnectivity bus.

27. (Currently Amended) A mobile terminal comprising:

a modem processor;

an application packet counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of packets has been reached by the application packet counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the

modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

28. (Currently Amended) A method comprising:

starting an application timer at an application processor;

accumulating data at the application processor until expiration of the application timer;

sending the accumulated data from the application processor to a modem processor across an interconnectivity bus; and

holding modem processor data at the modem processor until triggered by receipt of the accumulated data from the application processor,

wherein receipt of the accumulated data from the application processor triggers passing the modem processor data to the application processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state.

29. (Currently Amended) A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data,

wherein the modem processor is further configured pull data from the application processor after transmission of the modem processor to application processor data

and before the interconnectivity bus transitions from an active power state to a low power state.

30. (Previously Presented) The mobile terminal of claim 1, further comprising a second modem processor, the second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor.

31. (Previously Presented) The method of claim 15, further comprising holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor.

REMARKS

This paper is responsive to the Office Action mailed June 10, 2016 (hereinafter "Office Action"). Applicant would like to thank the Examiner for a timely and thorough review of the above-referenced patent application. It is respectfully submitted that in light of the amendments above and remarks below, all of the claims are now in condition for allowance.

Status of Claims

Claims 1-31 are pending. Claims 1, 15, 20, and 24-29 have been amended herein. Support for these amendments may be found, *inter alia*, at paragraphs 0051-0055 of the Application as originally filed. No claims have been canceled or added herein. No new matter is added.

Objection to Drawings

The drawings stand objected to in the Office Action as not "show[ing] every feature of the invention specified in the claims." In particular, the Office Action states that "the second modem processor as cited in claim 30 and 31 must be shown or the feature(s) canceled from the claim(s)."

37 C.F.R. § 1.83(a) states that "[t]he drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, **conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).**" Emphasis added. Here, claim 30 recites a "second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor." Claim 31 recites "holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor." Applicant respectfully submits that a drawing specifically illustrating a "second modem processor" is not essential for a proper understanding of claims 30 or 31.

Paragraph 0083 of Applicant's specification states that "[a] **processor may also be implemented as a combination of computing devices, e.g.,** a combination of a DSP and a

microprocessor, **a plurality of microprocessors**, one or more microprocessors in conjunction with a DSP core, or any other such configuration." Emphasis added. The "modem processor," which "may be implemented as a combination of computing devices, e.g., ... a plurality of microprocessors" (Specification, ¶ 0083) is illustrated in Figure 2 et al. Support for the features of claims 30 and 31 are also described in detail in paragraph 0053 of the Application as originally filed. Paragraph 0053 states:

> As noted above, the uplink timer (i.e., the application timer) is, in an exemplary aspect, designed to be longer than the downlink timer (i.e., the modem timer) to increase the uplink/downlink synchronization whenever the downlink timer expires. While holding data for an extra time slot adds some latency, the brief amount added is readily absorbed by the application processor 34. Likewise, this latency is considered acceptable for the power savings. For example, by making the period of the modem timer twice the period of the time slot 58, the number of low power to active power transitions is potentially halved. Likewise, by making the period of the application timer six times the period of the time slot 58, the chance of being able to "piggyback" onto the active power state of the interconnectivity bus 36 caused by the modem data is increased, but still frequent enough that any uplink data 56 will still be sent in a timely fashion even if there is no downlink data 54 to trigger releasing the uplink data 56. **Similar logic can be extended to synchronize traffic from multiple processors over the data link.** In an exemplary aspect, the other processors may each have timer values higher (i.e., longer) than that of the downlink timer, and **the processors can exchange their data availability information** so that traffic on one processor can trigger the data transfer on other processors if there is data available to transfer. Emphasis added.

Thus, because a "modem processor" that may contain multiple processors is illustrated in Figure 2, and because the features of claims 30 and 31 are fully supported by Applicant's specification, Applicant respectfully declines to amend the drawings at this time. In the event that the objection is maintained and the Application is found to be in condition for allowance but for this objection, Applicant reserves the right to revisit this objection at that time.

Rejection of Claims 30 and 31 under 35 U.S.C. § 112(a)

Claims 30 and 31 stand rejected under 35 U.S.C. § 112(a) as failing to comply with the written description requirement. Applicant respectfully traverses.

Page 3 of the Office Action states that "[n]o mention of [a] second modem processor can be found in [the] application as filed." However, as noted in Applicant's Preliminary Amendment filed April 27, 2015, and as discussed above with respect to the Office Action's Drawing Objections, support for the features of claims 30 and 31 may be found, *inter alia*, in paragraph 0053 of the Application as originally filed. Paragraph 0083 also discloses that "[a] **processor may also be implemented as a combination of computing devices, e.g.,** a combination of a DSP and a microprocessor, **a plurality of microprocessors**, one or more microprocessors in conjunction with a DSP core, or any other such configuration." Emphasis added. Thus, it is apparent that the features of claim 30, including a "second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor," is fully supported by the Application as originally filed. It is also apparent that the features of claim 31, including "holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor," are also fully supported by the Application as originally filed.

Accordingly, for at least these reasons, Applicant respectfully requests that the rejection be withdrawn.

Rejection of Claim 6 under 35 U.S.C. § 112(b)

Claim 6 stands rejected under 35 U.S.C. § 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor regards as the invention. In particular, the Office Action objects to the use of the word "approximately" as "a relative term which renders the claim indefinite."

MPEP § 2173.05(b) states that "[t]he use of relative terminology in claim language, including terms of degree, does not automatically render the claim indefinite under 35 U.S.C. 112(b) or pre-AIA 35 U.S.C. 112, second paragraph. Seattle Box Co., Inc. v. Industrial Crating & Packing, Inc., 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification."

Here, the phrase "the modem timer has a period of approximately six (6) milliseconds" in claim 6 does not automatically render the claim indefinite. The Office Action states that "the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention." The Office Action does not provide any evidence for this conclusory statement, however. Applicant respectfully submits that the examples provided by MPEP § 2173.05(b)(III) (entitled "Approximations") support Applicant's contention that the term "approximately" is clear and unambiguous in the context of claim 6. For example, in W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), "the court held that a limitation defining the stretch rate of a plastic as 'exceeding about 10% per second' is definite because infringement could clearly be assessed through the use of a stopwatch." MPEP § 2173.05(b)(III)(A). Here, infringement of the features of claim 6 can also be clearly assessed through the use of timing measurements readily available to those of ordinary skill in the art. Thus, for at least this reason, Applicant respectfully submits that the features of claim 6 are clear an unambiguous. Accordingly, Applicant respectfully requests that the rejection be withdrawn and the claim allowed.

Rejection of Claims 1-31 under 35 U.S.C. § 103 – Intel and Morita

Claims 1-31 stand rejected under 35 U.S.C. § 103 over International Patent Application Publication No. WO 2009/039034 A1 to Intel Corporation (hereinafter "Intel") in view of U.S. Patent No. 6,021,265 to Morita (hereinafter "Morita"). To establish *prima facie* obviousness, "[a]ll words in a claim must be considered" and all limitations must be disclosed by or derived from the prior art. MPEP § 2143.03, In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Additionally, "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" to establish obviousness. KSR Int'l v. Teleflex, Inc., 550 U.S. 398, 418, 82 USPQ.2d 1385, 1396 (2007). Applicant respectfully traverses.

Claim 1, as amended, recites a "mobile terminal" comprising a "modem processor configured to hold modem processor to application processor data until expiration of [a] modem timer" and an "application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data

from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Amendment noted. Intel and Morita do not disclose these features, particularly "hold[ing] application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor" or sending "application processor to modem processor data ... to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Amendment noted.

Page 4 of the Office Action admits that "[Intel] does not teach the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus." Pages 4 and 5 rely on the Abstract and Column 1, lines 15-20 of Morita as allegedly disclosing these features, but Morita still fails to disclose "hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data," as recited by amended claim 1. Amendment noted. The cited passages of Morita disclose, at most, "delay[ing] an output start timing of write data by a **predetermined time length**." Morita, Abstract, emphasis added. This "predetermined time length" is, by definition, determined in advance, and there is no disclosure or suggestion that the "predetermined time length" is even capable of being "triggered by" or otherwise "responsive to the receipt of the modem processor to application processor data," as required by claim 1. Thus, Intel and Morita fail, alone or in combination, to disclose all the features of claim 1.

Accordingly, for at least this reason, Applicant respectfully requests withdrawal of the rejection of independent claim 1. Independent claims 15, 20, and 24-29 have been amended to recite similar features and are therefore allowable for at least the same reasons as claim 1, as well as for the additional features recited therein. Claims 2-14, 16-19, 21-23, 30, and 31 depend, directly or indirectly, from claims 1, 15, and 20 and are thus allowable over Intel and Morita for at least the same reasons. Because of these dependencies, it is not necessary to address the

additional features presented in claims 2-14, 16-19, 21-23, 30, and 31. However, Applicant reserves the right to do so in the future, and does so below with respect to claims 4 and 7.

In this regard, claim 4 further recites that the "application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer." Page 5 of the Office Action relies on paragraph 0009 of Intel for this feature, but this passage is relied on only for the general disclosure of "implementing buffering techniques and/or logic that allows the communications sub-system and/or the computing sub-system to enter and remain within a lower power state, while maintaining Quality of Service (QoS) and other performance requirements for the communications sub-system and/or the computing sub-system." Intel, ¶ 0009. The specific feature of an "uplink timer [having] a period longer than a period of the modem timer" is not disclosed anywhere in this passage. Instead, page 5 of the Office Action concludes, without evidence, that "it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency," and that "[t]herefore, it would have been obvious that a skilled person will select a duration for the buffer that fits the circumstances, without making use of inventive skills." Even if this conclusory argument were accurate, a point Applicant does not concede, Applicant respectfully submits that the Office Action's conclusion still fails to arrive at the specific features of claim 4, i.e., that the "application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer." Thus, for at least this additional reason, claim 4 is independently allowable.

Claim 7 further recites "the application processor is configured to hold the application processor to modem processor data **until receipt of the modem processor to application processor data** from the modem processor **or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first**." Emphasis added. Page 6 of the Office Action relies on the Abstract, column 1, lines 15-20, and column 8, lines 50-62 of Morita as allegedly disclosing these features, but as noted above, Morita is directed, at most, to "delay[ing] an output start timing of write data by a **predetermined time length**." Morita, Abstract, emphasis added. Even if this feature could be interpreted as meeting the feature of claim 7 of "expiration of the uplink timer," a point Applicant does not concede, Morita would still continue to fail to disclose "hold[ing] the application processor to modem processor data **until receipt of the modem processor to application processor data** from the modem

processor," let alone "hold[ing] the application processor to modem processor data **until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first**," as recited by claim 7. Emphasis added. Thus, for at least this additional reason, claim 7 is independently allowable.

Conclusion

In view of the foregoing remarks and amendments, Applicant respectfully submits that claims 1-31 of the present Application are in condition for allowance. It is respectfully requested that a Notice of Allowance be issued in due course. Examiner Choudhury is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present Application.

No fee is believed due in connection with this Reply. However, the Office is authorized to charge any additional fees that may be necessitated by this Reply to Deposit Account No. 50-1732.

Respectfully submitted,

/Taylor M. Davenport Reg#42466/

Taylor M. Davenport
Registration No. 42,466
Withrow & Terranova, PLLC
106 Pinedale Springs Way
Cary, NC 27511
919-238-2300

Date: August 24, 2016
Attorney Docket No.: 141062/1173-141

Electronic Acknowledgement Receipt

EFS ID:	26734619
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/David Smith
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	24-AUG-2016
Filing Date:	12-DEC-2014
Time Stamp:	14:15:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		141062_OAR_08-24-16_AsFiled.pdf	88696 4b16ca6d3c26e3f023086751d6208bbb25a80877e3	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	16

Warnings:	
Information:	
Total Files Size (in bytes):	88696

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/568,694	Filing Date 12/12/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/24/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 31	Minus	** 31	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 9	Minus	*** 9	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
VINCENT BUTLER

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14568694
Filing Date	2014-12-12
First Named Inventor	Vinod Harimohan Kaushik
Art Unit	2116
Examiner Name	Zahid Choudhury
Attorney Docket Number	141062/1173-141

U.S.PATENTS

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1							

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NON-PATENT LITERATURE DOCUMENTS

Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14568694
	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	2116
	Examiner Name	Zahid Choudhury
	Attorney Docket Number	141062/1173-141

	1	International Preliminary Report on Patentability for PCT/US2014/070368, mailed April 1, 2016, 33 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14568694
	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	2116
	Examiner Name	Zahid Choudhury
	Attorney Docket Number	141062/1173-141

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

X That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2016-07-01
Name/Print	Taylor M. Davenport	Registration Number	42466

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

DAVENPORT, Taylor, M.
WITHROW & TERRANOVA, PLLC
2530 Meridian Parkway, Suite 300
Durham, NC 27713
ETATS-UNIS D'AMERIQUE

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	01.04.2016

Applicant's or agent's file reference	IMPORTANT NOTIFICATION
141062WO	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2014/070368	15.12.2014	16.12.2013

Applicant
QUALCOMM INCORPORATED

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary report on patentability and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary report on patentability. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

The applicant's attention is drawn to Article 33(5), which provides that the criteria of novelty, inventive step and industrial applicability described in Article 33(2) to (4) merely serve the purposes of international preliminary examination and that "any Contracting State may apply additional or different criteria for the purposes of deciding whether, in that State, the claimed inventions is patentable or not" (see also Article 27(5)). Such additional criteria may relate, for example, to exemptions from patentability, requirements for enabling disclosure, clarity and support for the claims.

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	de Haas, Bart Tel. +31 70 340-4736

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Form PCT/IPEA/416
141062WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2014/070368	15.12.2014	16.12.2013

International Patent Classification (IPC) or national classification and IPC

INV. G06F1/32

Applicant

QUALCOMM INCORPORATED

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 9 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *(sent to the applicant and to the International Bureau)* a total of 22 sheets, as follows:
      - ☒ sheets of the description, claims and/or drawings which have been amended and/or sheets containing rectifications authorized by this Authority, unless those sheets were superseded or cancelled, and any accompanying letters (see Rules 46.5, 66.8, 70.16, 91.2, and Section 607 of the Administrative Instructions).
      - ☐ sheets containing rectifications, where the decision was made by this Authority not to take them into account because they were not authorized by or notified to this Authority at the time when this Authority began to draw up this report, and any accompanying letters (Rules 66.4bis, 70.2(e), 70.16 and 91.2).
      - ☐ superseded sheets and any accompanying letters, where this Authority either considers that the superseding sheets contain an amendment that goes beyond the disclosure in the international application as filed, or the superseding sheets were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in item 4 of Box No. I and the Supplemental Box (see Rule 70.16(b)).

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing, in the form of an Annex C/ST.25 text file, as indicated in the Supplemental Box Relating to Sequence Listing (see paragraph 3*ter* of Annex C of the Administrative Instructions).

4. This report contains indications relating to the following items:
   - ☒ Box No. I Basis of the report
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☐ Box No. VII Certain defects in the international application
   - ☒ Box No. VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
23.06.2015	01.04.2016

Name and mailing address of the international preliminary examining authority:	Authorized officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	De Meyer, Arnaud Telephone No. +31 70 340-4302

Box No. I Basis of the report

1. With regard to the **language**, this report is based on

☒ the international application in the language in which it was filed

☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:

- ☐ international search (under Rules 12.3(a) and 23.1(b))
- ☐ publication of the international application (under Rule 12.4(a))
- ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a) and (b))

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1-16	as originally filed

Claims, Numbers

1, 15, 20, 24-29	as originally filed	
2-14, 16-19, 21-23	filed with the letter of	23-06-2015

Drawings, Sheets

1/13-13/13	as originally filed

☐ a sequence listing - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

- ☐ the description, pages
- ☐ the claims, Nos.
- ☐ the drawings, sheets/figs
- ☐ the sequence listing *(specify)*:

4. ☒ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since either they are considered to go beyond the disclosure as filed, or they were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in the Supplemental Box (Rules 70.2(c) and (c-*bis*)):

- ☐ the description, pages
- ☒ the claims, Nos. 1, 15, 20, 24-31
- ☐ the drawings, sheets/figs
- ☐ the sequence listing *(specify)*:

5. ☐ This report has been established:

- ☐ taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rules 66.1(d-*bis*) and 70.2(e)).
- ☐ without taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91(Rules 66.4*bis* and 70.2(e)).

6. ☒ With regard to top-up searches (Rules 66.1*ter* and 70.2(f)):
   ☒ A top-up search was carried out by this Authority on 03.11.2015 (all discovered documents are listed in the Supplemental Box Relating to Top-up Search).
   ☐ Additional relevant documents have been discovered during the top-up search.
   ☐ No top-up search was carried out by this Authority because it would serve no useful purpose.

7. ☐ Supplementary international search report(s) from Authority(ies) hashave been received and taken into account in establishing this report (Rule 45bis.8(b) and (c)).

* *If item 4 applies, some or all of those sheets may be marked "superseded".*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-29
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-29
Industrial applicability (IA)	Yes:	Claims	1-29
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item I

Basis of the opinion

1 In his letter dated 06-01-2016 (from now on, this reply will be referred to as R2), the applicant maintained the claims as submitted with the previous letter dated 23-06-2015 (R1) and answered to the objections of the examiner as set out in the official communication dated 09-11-2015 (C1).

1.1 Claims 1, 20 and 24-27: The objection raised in §1.1 of C1 is upheld. This amendment is allegedly based on [0054]-[0056] of the description, which support fig.5. The wording of [0054]-[0056] is vague. In the light of fig.5, it appears that what is meant in [0054]-[0056] is that data from the application manager are transmitted *after* reception of the data from the modem processor; and not at the time of the receipt, as specified by the amended claims.

The arguments of the applicant have been duly considered. However, "triggered by" (claims) is different in scope from "responsive to" ([0054]-[0056]). There is no basis in the application as filed for introducing "triggered by".

1.2 Claims 15, 28 and 29: The objection raised in §1.2 of C1 is upheld. The subject-matter of this amendment, allegedly based on [0053] of the description, is extracted from the technical context wherein it is disclosed, resulting in an intermediate generalisation. Specifically, the application as filed does not comprise any embodiment comprising the transition from the active power state to the low power state, without also specifying the transition from the low power state to the active power state. Furthermore, it is pointed out that this amendment also introduces obscurity into the claims, because it is not clear from the amended claims what differentiates the active power state and the low power state.

The opinion of the applicant expressed in R2 has been duly considered. Since an intermediate generalisation means that the skilled person is faced with a combination of features which is new over the content of the application as originally filed, this concept is not only relevant under the EPC but also under Article 34(2)(b) PCT, contrary to the opinion of the applicant.

1.3 Claims 30-31: The objection raised in §1.3 of C1 is upheld. No mention of a second modem processor can be found in the application as filed.

In R2, the applicant provided a basis for claims 30-31, namely [0054]-[0060]. It appears that the only relevant passage therein is the end of [0054], wherein reference is made to the possibility of having multiple processors. However, consistently with §1.3 of C1, there is still no basis for more than one *modem* (emphasis added) processor.

2 Under Rule 70.2 (c) PCT, this report shall be established as if the amendments objected upon in above §1.1-1.3 had not been made.

In R2, the applicant requested the amendments to be considered when establishing the report. It is deemed inappropriate to spend energy in discussing new features which are anyway non-allowable, especially when the the claims already contains severe clarity issues, see below §5. Therefore the request of the applicant is not granted.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-29 does not involve an inventive step in the sense of **Article 33(3) PCT**.

The objections raised in §2-4 of the WO-ISA are upheld. Said objections are reproduced in the following for convenience.

3.1 Claim 1: Document D1 (by default, references in parentheses apply to this document) discloses a mobile terminal ([0013]: "a smartphone") comprising:
a modem timer ([0037]: "when a buffer unload timeout value expires");
a modem processor (fig.2: "communications sub-system 210"; Implicitly, "communication sub-system 210" is/comprises a *modem*, otherwise the smartphone of D1 could not process voice data and thus perform the functions of a phone), the modem processor configured to hold modem processor to application processor data until expiration of the modem timer ([0037]: "when a buffer unload timeout value expires");
an application processor (fig.2: "computing sub-system 230");
an interconnectivity bus communicatively coupling the application processor to the modem processor (fig.2: "bus 220");~~and~~

~~the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus~~.

The subject-matter of claim 1 differs from document D1 in that:

(1) the application processor is configured to buffer the data to be sent to the modem processor; and

(2) the data from the application processor are sent after reception of the data from the modem processor.

These differences relate to different technical problems: power saving (1) and data transmission on a serial bus (2) and do not have a synergetic effect. These differences will therefore be considered independently for the assessment of a possible inventive step.

3.1.1 The technical effect of difference (1) is a reduction of power consumption, see [0007] of the application. Document D1 also relates to "buffering techniques for power management" (`title and [0001]`).

Starting from D1, the technical problem is formulated as how to further reduce power consumption.

In D1, the data are buffered by the modem processor so that downstream components can be put in a power saving mode (`[0008]`). Starting from D1, the most obvious solution to further reduce power consumption would be to increase the buffer size or the duration of the buffering. However, since there is a commonly known compromise between buffering and performance (`[0009]: "...while maintaining Quality of Service (QoS) and other performance requirements"`), it may not be possible to increase the buffering of the data to be transferred to the application processor. In such case, an obvious solution to further reduce power consumption consists of also buffering the data to be transferred to the modem processor, in the exact same way as for the data to be transferred to the application processor. This modification corresponds merely to the duplication of the buffing means disclosed by D1. This is the solution recited by claim 1.

3.1.2 The technical effect of difference (2) is to avoid data collisions on the serial bus, i.e the PCI express bus introduced by claims 2 and 3. Document D1 also uses a PCI express bus (`[0028]`).

Starting from D1, the technical problem is formulated as how to avoid data collision on a serial bus.

It is not possible to transmit data on PCI express bus at the same time and in both directions. Therefore, there are only two possible solutions: it is only possible to send the data from application processor after having receiving, or before sending, the data from the modem processor; the first solution being the one recited by the claim 1. Document D1 is silent about which one of these solutions to use. Consequently, the skilled person willing to implement D1 would have to choose one of these two solutions. Sending the data from the application processor before or after the data from the modem processor are obviously equivalent solutions, and the skilled person would select one or the other, depending on the circumstances, without making use of inventive skills.

3.2 Claims 15, 20 and 24-29: Substantially, claims 1, 15, 20 and 24-29 correspond to different alternatives combinations of using a timer/ a counter/ an amount of data being buffered, and of sending the data from the application processor before or after the data from the modem processor. The different alternatives combinations of using a timer/ a counter/ an amount of data being buffered are disclosed by D1 ([0037]). Therefore the reasoning in above §2.1 for the subject-matter of claim 1 also applies, mutatis mutandis, to the subject-matter of claims 15, 20 and 24-29.

3.3 Claims 2, 3 and 16: Disclosed by D1 ([0028]: "PCI Express (PCIe)").

3.4 Claims 4, 6, 7, 17 and 18: As illustrated by D1 ([0009]: "...while maintaining Quality of Service (QoS) and other performance requirements"), it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, the skilled person will select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.

3.5 Claim 5: Disclosed by D1 ([0010]: "software").

3.6 Claim 8: Disclosed by D1 (fig.2).

3.7 Claims 9, 21 and 22: Considering the clarity issues raised in below Re Item VIII, claims 9, 21 and 22 are seen as mere design choices.

3.8 Claims 10-14, 19 and 23: Considering the clarity issues raised in below Re Item VIII, claims 10-14, 19 and 23 are interpreted broadly and disclosed by D1 ([0037]).

3.9 For the sake of completeness, it is pointed out that the claimed invention seems to correspond to the mere implementation of the PCI Express (PCIe) standard, in particular of the full-duplex mode of the L1/L0s power states of the Active State Power Management (ASPM), as illustrated for example by document D3 (slides 23-28). The person skilled in the art knows the PCIe standard which forms part of the common general knowledge in the art. Therefore, starting from any document that hints to use the PCIe ASPM, the person skilled in the art would think of the different power saving states (L1, L0 and L0s) and implement the most appropriate once, without making use of inventive skills.

Document D2, for example, discloses an apparatus comprising a network controller and a CPU linked by a PCIe bus (fig.1). Also, D2 leads to the use of the PCIe ASPM ([0007]). The subject-matter of claims 1-29 lacks an inventive step in the light of D2 combined with the common general knowledge, i.e. the PCIe standard, see references in the associated search report.

Re Item VIII

Certain observations on the international application

4 The objections raised in §4 of C1 are upheld.

The applicant seems to consider that the terms objected upon are clear to the skilled person in the light of the description. The claims should be clear by themselves. The claims should therefore have been clarified based on the description.

Said objections are reproduced in the following for convenience.

5 Although claims 1, 20, 24, 25, 26, 27, and 29 (terminals) and claims 15 and 28 (methods) have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and/or in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of **Article 6 PCT**.

6 The application does not meet the requirements of **Article 6 PCT**, because the claims are not clear.

6.1 The claims relate to different timers and counters that are designated in a vague and inconsistent manner, and leave the reader in doubt as to the meaning of the technical features to which they refer.

First example: The skilled person would normally understand that the "modem timer" is the timer of a modem. However, in claim 9 for example, the "modem timer" is not part of the modem. Therefore it is not clear what is the "*modem* timer" and what it times.

Second example: The terminology is inconsistent. From the claims, the skilled person would understand that the "uplink timer" and the "application timer" are distinct features. This is consistent with part of the description. However, in other parts of the description, the "uplink timer" and the "application timer" are the same, e.g. [0054]: "the uplink timer (i.e. the application timer)". The same applies for the "downlink timer" and the "modem timer" In other words, it is not clear what are these different timers and what they time.

Third example: Even in the the help of the description, it is not clear what is performed by the "modem byte accumulation limit counter".

It is pointed out that this list of examples is not exhaustive.

Altogether, it is not clear what differentiates the claimed timers and counters from those known in the art. The claims should be clarified. When assessing novelty an inventive step, the different timers and counters recited by the claims are therefore interpreted broadly as "a timer" and "a counter".

6.2 Independent claims: It could be understood, for example from claim 1, that the transmission of each data is simply delayed for a duration defined by the "modem timer". However, it appears in the light of fig.10 that the data to be transferred are buffered. The claims should be clarified. When assessing novelty an inventive step, it is considered that the data are buffered.

IN THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

In Re International Application No.:	PCT/US2014/070368
International Filing Date:	15 December 2014
Applicant:	Qualcomm Incorporated
Applicant Docket No.:	141062WO/1173-141-WO

RESPONSE TO WRITTEN OPINION MAILED 5 MARCH 2015 UNDER ARTICLE 34

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Attention: Arnaud De Meyer

Dear Sirs:

This communication is in response to the Written Opinion, dated 5 March 2015, for the International Patent Application identified above.

REMARKS

Remarks Regarding Item V

Paragraph 2 of the Written Opinion indicates that claims 1, 15, 20, and 24-29 do not involve an inventive step. Paragraph 2.1 elaborates that claim 1 is not inventive over International Patent Application Publication WO 2009/039034 A1 to Tsai (hereinafter "D1").

Claim 1 has been amended to recite "the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Amendment noted. Paragraph 2.1.2 opines that "[i]t is not possible to

transmit data on PCI express bus at the same time and in both directions. Therefore, there are only two possible solutions: it is only possible to send the data from application processor after having receiving, or before sending, the data from the modem processor...." Assuming, without admitting, that this assertion is true, D1 still does not teach that the "application processor [is] configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor" or "the application processor to modem processor data is sent to the modem processor...responsive to the receipt of the modem processor to application processor data..." as recited in amended claim 1.

Thus, D1 does not teach or suggest the elements of claim 1, and claim 1 defines an inventive step over D1.

Paragraph 2.2 groups claims 15, 20, and 24-29, indicating that these claims are likewise not inventive over D1 for essentially the same reasons.

Claim 15 has been amended to recite "wherein receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state." Amendment noted. Applicant respectfully maintains that D1 does not teach or suggest this element. Thus, claim 15 defines an inventive step over D1.

Claims 20 and 24-27 have been amended in a fashion similar to claim 1 and define an inventive step for at least the same reasons.

Claims 28 and 29 have been amended in a fashion similar to claim 15 and define an inventive step for at least the same reasons.

Paragraph 3 indicates that dependent claims 2-14, 16-19, and 21-23 are likewise not inventive over D1. Claims 2-14, 16-19, and 21-23 depend directly or indirectly from claims 1, 15, and 20. Thus, claims 2-14, 16-19, and 21-23 are allowable over D1 for at least the same reasons as claims 1, 15, and 20.

Paragraph 4 asserts that claims 1-29 are not inventive over U.S. Patent Application Publication No. 2013/0198538 A1 to Diab et al. (hereinafter "D2") and "PCI Express™ Architecture Advanced Protocols & Features PCI Express™ Architecture Advanced Protocols and Features," PCI-SIG Developers Conference (hereinafter "D3").

Applicant respectfully disagrees. The implementation of PCIe Active State Power Management as set forth in D2 or D3 does not teach or suggest "the application processor

configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus" as recited in amended claims 1, 20, and 24-27. Thus, independent claims 1, 20, and 24-27 define an inventive step over D2 or D3.

Likewise, the implementation of PCIe Active State Power Management as set forth in D2 or D3 does not teach or suggest "wherein receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state" as recited in amended claims 15, 28, and 29. Thus, independent claims 15, 28, and 29 define an inventive step over D2 or D3.

Claims 2-14, 16-19, and 21-23 depend directly or indirectly from claims 1, 15, and 20. Thus, claims 2-14, 16-19, and 21-23 are allowable over D2 or D3 for at least the same reasons as claims 1, 15, and 20.

Remarks Regarding Item VIII

Paragraph 5 of the Written Opinion alleges that "[a]lthough claims 1, 20, 24, 25, 26, 27, and 29 (terminals) and claims 15 and 28 (methods) have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and/or in respect to the terminology used for the features of that subject-matter." The Written Opinion opines that the "aforementioned claims therefore lack conciseness."

Applicant acknowledges the objection to the claims, but notes that some jurisdictions allow for multiple independent claims with varying scope directed to different aspects of the Application. Accordingly, Applicant declines to consolidate the claims at this time.

Paragraph 6 of the Written Opinion alleges that the claims are not clear. Paragraph 6.1 alleges that there is "a vague and inconsistent" use of "timers and counters" in the claims.

Applicant respectfully disagrees. Applicant respectfully submits that the meaning of each term is clear from its plain meaning as well as from its context in light of Applicant's specification.

The first example of paragraph 6.1 of the Written Opinion alleges that "it is not clear what is the 'modem timer' and what it times." Applicant respectfully submits that the "modem timer" is a "timer" that is associated with, but is not necessarily part of, a "modem." See, for example, paragraphs 0051-0055 of the Application as filed.

The second example of paragraph 6.1 of the Written Opinion alleges that "the terms 'uplink timer' and 'application timer' are the same." Applicant respectfully submits that, while the terms "uplink timer" and "application timer" may have overlapping scope, they are not always equivalent terms. For example, an "application timer" may not necessarily relate to "uplink" data, and an "uplink timer" may not necessarily relate to "application" data in every claimed embodiment. Applicant respectfully submits that the terms are used for features of differing scope, and that the claims are adequately clear.

The third example of paragraph 6.1 of the Written Opinion alleges that "it is not clear what is performed by the 'modem byte accumulation limit counter.'" Applicant respectfully submits that the term "modem byte accumulation limit counter" is fully disclosed and supported by paragraph 0063 of the Application as filed. For example, "a byte accumulation limit counter may also be used by the modem processor 44 for downlink traffic and the application processor 34 for uplink traffic." Id.

Thus, for at least these reasons, Applicant respectfully submits that the meaning of each term is clear from its plain meaning as well as from its context in light of Applicant's specification.

Paragraph 6.2 of the Written Opinion asserts per "claim 1, that the transmission of each data is simply delayed for a duration defined by the 'modem timer'. However, it appears in light of fig. 10 that the data to be transferred are buffered." Applicant notes that buffering is one technique through which the delay of claim 1 is achieved. Accordingly, the claims are not limited to buffering. Applicant requests withdrawal of the objection at this time.

Claim Amendments Remarks

Statement under Article 34(2)(b)

Upon entry of the amendment, claims 1-31 are presented for reconsideration, with 1, 15, 20, and 24-29 being the independent claims.

Claims 1, 15, 20, and 24-29 are amended. Support for these amendments can be found in at least paragraphs 0054-0056 of the International Application as originally filed. No new matter is added.

Claims 30 and 31 are added. Support for these claims can be found in at least paragraph 0053 of the International Application as originally filed. No new matter is added.

Applicant reserves the right to prosecute similar or broader claims, with respect to the amended claims, in the future. The Applicant does not dedicate to the public any aspect of the inventions disclosed by the current application.

Conclusion

The invention, as defined in the amended claims submitted herewith, is novel, inventive, and has industrial applicability, at least for the reasons stated above. However, should the Examiner reach a different conclusion, we request issue of a further written communication, and to be provided an opportunity to file a further response and/or an interview before the Preliminary Examination Report is issued.

We look forward to receiving the International Preliminary Report on Patentability.

Respectfully submitted,

Dated: 23 June 2015

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REPLACEMENT PAGE

What is claimed is:

1. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

2. The mobile terminal of claim 1, wherein the interconnectivity bus comprises a peripheral component interconnect (PCI) compliant bus.

3. The mobile terminal of claim 2, wherein the PCI compliant bus comprises a PCI express (PCIe) bus.

4. The mobile terminal of claim 1, wherein the application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer.

5. The mobile terminal of claim 1, wherein the modem timer is implemented in software.

6. The mobile terminal of claim 1, wherein the modem timer has a period of approximately six (6) milliseconds.

REPLACEMENT PAGE

7. The mobile terminal of claim 4, wherein the application processor is configured to hold the application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first.

8. The mobile terminal of claim 1, wherein the modem processor comprises the modem timer.

9. The mobile terminal of claim 1, wherein the application processor comprises the modem timer.

10. The mobile terminal of claim 1, further comprising an application timer, and wherein the modem processor is configured to instruct the application processor to send an interrupt if no data is received within one time slot of the application timer.

11. The mobile terminal of claim 1, further comprising a byte accumulation limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the byte accumulation limit counter is exceeded.

12. The mobile terminal of claim 1, further comprising a packet number limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the packet number limit counter is exceeded.

13. The mobile terminal of claim 1, wherein the modem processor is configured to determine if held data comprises a control packet and send such control packet before expiration of the modem timer.

REPLACEMENT PAGE

14. The mobile terminal of claim 3, wherein the modem processor further comprises an application timer, and the modem processor is configured to pull data from the application processor on receipt of the modem processor to application processor data or expiration of the application timer.

15. A method of controlling power consumption in a computing device, comprising:

holding data received by a modem processor from a remote network until expiration of a downlink timer;

passing the data received by the modem processor to an application processor over an interconnectivity bus; and

holding application data generated by an application associated with the application processor until receipt of the data from the modem processor or expiration of an uplink timer, whichever occurs first,

wherein receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state.

16. The method of claim 15, wherein passing the data comprises passing the data over a peripheral component interface (PCI) compliant bus.

17. The method of claim 15, wherein a period of the downlink timer comprises six (6) milliseconds.

18. The method of claim 15, wherein a period of the uplink timer comprises seven (7) milliseconds.

19. The method of claim 15, further comprising providing an override capability based on one of accumulated packet size, accumulated packet count, accumulated byte count, quality of service requirement, and control message status.

REPLACEMENT PAGE

20. A mobile terminal comprising:

a modem processor;

an application timer;

an application processor, the application processor configured to hold application processor to modem processor data until expiration of the application timer;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the application processor to modem processor data from the application processor through the interconnectivity bus.

21. The mobile terminal of claim 20, wherein the application processor comprises the application timer.

22. The mobile terminal of claim 20, wherein the modem processor comprises the application timer.

23. The mobile terminal of claim 20, further comprising a byte counter counting bytes at the modem processor.

24. A mobile terminal comprising:

a modem byte accumulation limit counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter;

an application processor;

REPLACEMENT PAGE

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

25. A mobile terminal comprising:

a modem packet counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of packets has been reached by the modem packet counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

26. A mobile terminal comprising:

a modem processor;

an application byte counter;

REPLACEMENT PAGE

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of bytes has been reached by the application byte counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the application processor to modem processor data from the application processor through the interconnectivity bus.

27. A mobile terminal comprising:

a modem processor;

an application packet counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of packets has been reached by the application packet counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until triggered by receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

REPLACEMENT PAGE

28. A method comprising:

starting an application timer at an application processor;

accumulating data at the application processor until expiration of the application timer;

sending the accumulated data from the application processor to a modem processor across an interconnectivity bus; and

holding modem processor data at the modem processor until triggered by receipt of the accumulated data from the application processor,

wherein receipt of the accumulated data from the application processor triggers passing the modem processor data to the application processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state.

29. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data,

wherein the modem processor is further configured pull data from the application processor after transmission of the modem processor to application processor data and before the interconnectivity bus transitions from an active power state to a low power state.

30. The mobile terminal of claim 1, further comprising a second modem processor, the second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor.

International application number: US2014070368
Letter accompanying amendments under Article 34 submitted with Demand for IPEA dated 23 Jun 2015

REPLACEMENT PAGE

31. The method of claim 15, further comprising holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor.

IN THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

In Re International Application No.:	PCT/US2014/070368
International Filing Date:	15 December 2014
Applicant:	Qualcomm Incorporated
Applicant Docket No.:	141062WO/1173-141-WO

RESPONSE TO SECOND WRITTEN OPINION MAILED 09 NOVEMBER 2015 UNDER ARTICLE 34

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Dear Sirs:

This communication is in response to the Second Written Opinion, dated 09 November 2015, for the International Patent Application identified above.

REMARKS

Remarks Regarding Item I

Paragraph 1 of the Second Written Opinion objects to the amendments filed 23 June 2015 under Article 34(2)(b) because these amendments allegedly "introduce subject-matter which extends beyond the content of the application as filed." Applicant respectfully traverses and addresses the particulars in order below.

Paragraph 1.1 of the Second Written Opinion states that the amendments to claims 1, 20, and 24-27 extend beyond the content of the Application as filed because "it appears that what is meant in [0054]-[0056]," which Applicant identified as providing support for these amendments, "is that data from the application manager are transmitted *after* reception of the data from the modem processor; and not at the same time of the receipt, as specified by the amended claims." Emphasis in original. Applicant respectfully submits that this

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characterization of claim 1 as amended is not accurate, and that paragraphs 0054-0056, by the Examiner's own interpretation, provide support for Applicant's amendments.

Claim 1 recites "the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus **responsive** to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Emphasis added. These features do not refer, as the Examiner suggests, to transmitting data "at the time of the receipt," but instead explicitly recite that "the application processor to modem processor data is sent to the modem processor" after the "application processor" is "triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Thus, Applicant's amendments are consistent with the Examiner's own characterization of Applicant's paragraphs 0054-0056. This interpretation is also consistent with the feature of claim 1 that the sending of the "modem processor data" is "responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus." Thus, there is no feature of claim 1 that requires the "data from the modem processor" to be transmitted "at the time of the receipt," as suggested by the Examiner. For at least this reason, Applicant respectfully submits that the amendments to claim 1 are proper under Article 34(2)(b).

Paragraph 1.2 of the Second Written Opinion states that the amendments to claims 15, 28, and 29 extend beyond the content of the Application as filed because "the application as filed does not comprise any embodiment comprising the transition from the active power state to the low power state, without also specifying the transition from the low power state to the active power state." Paragraph 1.2 of the Second Written Opinion also states that "it is not clear from the amended claims themselves what differentiates the active power state and the low power state." Applicant respectfully disagrees.

Claim 15 recites that "receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus **before the interconnectivity bus transitions from an active power state to a low power state.**" Emphasis added. Applicant respectfully points out that these features are fully supported by paragraphs 0054-0056, *inter alia*, of the International Application as originally filed. For the benefit of the Examiner, Applicant further points out

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that a "transition[] from an active power state to a low power state" is also shown, without limitation, by Figure 5, reproduced below. It is readily apparent from Figure 5 and paragraphs 0054-0056, *inter alia*, that the amended features of claim 15 are fully supported by the International Application as originally filed, and that the differences between a "low power state" and an "active power state" are readily apparent to a person of ordinary skill.

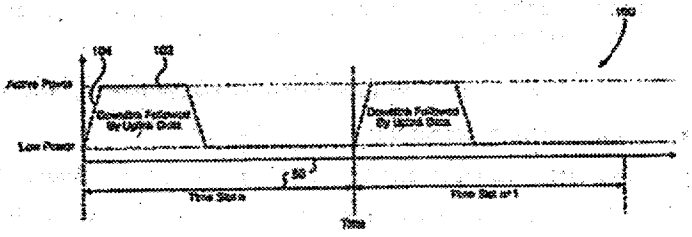


FIG. 5

Paragraph 1.2 of the Second Written Opinion does not appear to dispute that these features are supported, but instead suggests that Applicant's claimed feature, e.g., "passing the data ... before the interconnectivity bus transitions from an active power state to a low power state," is an "intermediate generalisation" because it is not accompanied by a "transition from the low power state to the active power state." Even accepting the Examiner's characterization, a point Applicant does not concede, Applicant is unaware of any requirement under Article 34 of the PCT that proscribes this practice. While so-called "intermediate generalisations" may be disfavored in some jurisdictions, such as in European practice, Applicant respectfully submits that many other jurisdictions, including the PCT, have no such requirement. Thus, Applicant respectfully submits that there is no basis for objecting to claims 15, 28, and 29 under Article 34(2)(b).

Paragraph 1.3 of the Second Written Opinion states that new claims 30 and 31 extend beyond the content of the Application as filed because "[n]o mention of a second modem processor can be found in the application as filed." Applicant respectfully disagrees.

Claim 30 recites, *inter alia*, a "second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor." Claim 31 recites, *inter alia*, "holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor." As noted in Applicant's previous response, support for these features may be found at paragraph 0053 of the International Application as

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originally filed. For the benefit of the Examiner, Applicant respectfully points out that additional support for these features may be found, *inter alia*, at paragraphs 0054 and 0060 of the International Application as originally filed. For example, paragraph 0054 states that:

> Similar logic can be extended to synchronize traffic from multiple processors over the data link. In an exemplary aspect, the other processors may each have timer values higher (i.e., longer) than that of the downlink timer, and the processors can exchange their data availability information so that traffic on one processor can trigger the data transfer on other processors if there is data available to transfer.

Emphasis added. Thus, claims 30 and 31 are fully supported by the International Application as originally filed, and are therefore proper under Article 34(2)(b).

Paragraph 2 indicates "this report shall be established as if the amendments objected upon in above § 1.1-1.3 had not been made…Therefore this report shall be established on the claims as originally filed." In view of the explanations provided above, Applicant requests reconsideration of this position and a report established on the claims as amended.

Remarks Regarding Item V

Paragraph 3 of the Second Written Opinion asserts that claims 1-29 do not involve an inventive step and upholds the objections of the Written Opinion of the International Searching Authority dated 05 March 2015 (hereinafter "First Written Opinion"). The First Written Opinion asserts that claims 1-29 are not inventive over International Patent Application Publication WO 2009/039034 A1 to Tsai (hereinafter "D1"), U.S. Patent Application Publication No. 2013/0198538 A1 to Diab et al. (hereinafter "D2"), and "PCI Express™ Architecture Advanced Protocols & Features PCI Express™ Architecture Advanced Protocols and Features," PCI-SIG Developers Conference (hereinafter "D3"). Applicant respectfully disagrees.

Applicant respectfully submits that the Second Written Opinion has been improperly established on the claims as originally filed. Applicant respectfully resubmits and incorporates by reference all arguments pertaining to the claims as amended from Applicant's previous response filed 23 June 2015.

For example, as discussed in detail in Applicant's previous response, D1 does not teach that the "application processor [is] configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor" or "the application processor to modem processor data is sent to

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the modem processor…responsive to the receipt of the modem processor to application processor data..." as recited in amended claim 1. D1 also does not disclose that "receipt of the data from the modem processor triggers passing the data received by the application processor to the modem processor over the interconnectivity bus before the interconnectivity bus transitions from an active power state to a low power state," as recited by amended claim 15. Similarly, implementations of PCIe Active State Power Management as set forth in D2 or D3 also do not disclose these amended features.

The Second Written Opinion has not responded to these or any other previously presented arguments regarding the Written Opinion's Item V objections. Thus, Applicant respectfully requests that the objections be withdrawn.

Remarks Regarding Item VIII

Paragraph 4 of the Second Written Opinion upholds the objections of the First Written Opinion. Paragraph 5 of the Second Written Opinion responds to a portion of Applicant's previously presented arguments.

Paragraph 5.1 states that the term "modem timer" is not clear, and states that "[t]he claims should be clear by themselves." Applicant respectfully submits that the term "modem timer" is clear and unambiguous to a person of ordinary skill from the wording of the claim alone, i.e., that the "modem timer" is a "timer" that is associated with, but is not necessarily part of, a "modem." To the extent the scope and meaning of the term "modem timer" is unclear to the Examiner, Applicant respectfully refers to paragraphs 0051-0055 of the International Application as filed, *inter alia*.

Paragraph 5.2 states that, with respect to the use of the terms "uplink timer" and "application timer" in different claims, "the skilled person would understand from the use of two different names that only embodiments wherein 'uplink timer' and 'application timer' are different features are covered by the scope of the claims." Applicant respectfully submits that the Examiner's statement supports Applicant's position. In this regard, Applicant again respectfully submits that, while the terms "uplink timer" and "application timer" may have overlapping scope, they do not have identical scopes. For example, an "application timer" may not necessarily always relate to "uplink" data, and an "uplink timer" may not necessarily always relate to "application" data in every claimed embodiment. The mere fact that a single element could potentially infringe both features does not make these features equivalent.

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Thus, Applicant respectfully submits that the terms are used for features of differing scope, and that the scope and meaning of the claims are adequately clear.

Paragraph 5.3 states, regarding the term "modem byte accumulation limit counter," that "[t]he claims should be clear by themselves." Applicant respectfully submits that the term "modem byte accumulation limit counter" is clear and unambiguous to a person of ordinary skill from the wording of the claim alone. To the extent the scope and meaning of the term "modem byte accumulation limit counter" is unclear to the Examiner, Applicant again respectfully refers to paragraph 0063 of the International Application as filed, *inter alia*.

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Claim Amendments Remarks

Statement under Article 34(2)(b)

Upon entry of the amendment, claims 1-31 are presented for reconsideration, with 1, 15, 20, and 24-29 being the independent claims.

The claims are unchanged from the amendment filed 23 June 2015. Applicant reserves the right to prosecute similar or broader claims, with respect to the amended claims, in the future. The Applicant does not dedicate to the public any aspect of the inventions disclosed by the current application.

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Conclusion

The invention, as defined in the amended claims previously submitted, is novel and inventive, at least for the reasons stated above. However, should the Examiner reach a different conclusion, we request issue of a further written communication, and to be provided an opportunity to file a further response and/or an interview before the Preliminary Examination Report is issued.

We look forward to receiving the International Preliminary Report on Patentability.

Respectfully submitted,

Dated: 06 January 2016

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Electronic Acknowledgement Receipt

EFS ID:	26237399
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/Rebecca Meier
Filer Authorized By:	Taylor M. Davenport
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Receipt Date:	01-JUL-2016
Filing Date:	12-DEC-2014
Time Stamp:	11:13:09
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	141062_IDS_5-20-16.pdf	611999 b8d7ccc56652e25d080a8fdb7e1eac5f62dcaec	no	4
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141	3463

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W&T/Qualcomm
106 Pinedale Springs Way
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EXAMINER
CHOUDHURY, ZAHID

ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
06/10/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@wt-ip.com
us-docketing@qualcomm.com
ocpat_uspto@qualcomm.com

Office Action Summary	Application No. 14/568,694	Applicant(s) KAUSHIK ET AL.	
	Examiner ZAHID CHOUDHURY	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/27/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-31* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-31* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *12/12/2014* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *02/09/2016, 06/05/2015 and 12/12/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second modem processor as cited in claim 30 and 31 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms

> as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 30 and 31 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention. No mention of second modem processor can be found in application as filed.

> The following is a quotation of 35 U.S.C. 112(b):
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

The term "approximately" in claims 6 is a relative term which renders the claim indefinite. The term "approximately" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. In particular, it is unclear as to the range with which " approximately" refers. Therefore, one of ordinary skill would not be able to determine what qualifies as "approximately"

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims1-31 are rejected under 35 U.S.C. 103 as being unpatentable over John et al. (John) (WO 2009/039034) in view of Morita (Patent No.: 6,021,264)

Regarding Claim 1 John teaches A mobile terminal ***[0013]*** comprising: a modem timer; ***[[0037]: "when a buffer unload timeout value expires"]*** a modem processor, ***[fig. 2: "communications sub-system 210, I.e. A mart phone having processor to process voice data and other functions]*** the modem processor configured to hold modem processor to application processor data until expiration of the modem timer; ***[[0037], when a buffer unload timeout value expires]*** an application processor; ***[Fig.2, Compute sub-system 230]*** an interconnectivity bus communicatively coupling the application processor to the modem processor; ***[Fig.2, item 220, BUS]***

John does not teach the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

However, Morita teaches: the application processor configured to hold application processor to modem processor data ***[write mode register stores delay information and write data output signal***

generation unit delays an output start timing of write data] until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus. ***[Abstract, Col.1 lines 15-20; processing system read/write data from input output system, col.8 lines 50-62]***

It would have been obvious to one of ordinary skill in the art **before the effective filing date of the claimed invention** to combine John and Morita delay the writing of data for a predetermined period of time in John's system using Morita's teaching in order to avoid possible data collision between read and write data.

Regarding Claim 2 John teaches the interconnectivity bus comprises a peripheral component interconnect (PCI) compliant bus. **[[0028], PCI Express]**

Regarding Claim 3 John teaches the PCI compliant bus comprises a PCI express (PCIe) bus. ***[[0028], PCI Express]***

Regarding Claim 4 John teaches the application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer. ***[[0009] maintaining Quality of Service (QoS) and other performance requirements. it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, it would have been obvious that a skilled person will select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.]***

Regarding Claim 5 John teaches the modem timer is implemented in software. ***[[0010] software]***

Regarding Claim 6 John teaches the modem timer has a period of approximately six (6) milliseconds. ***[[0009] maintaining Quality of Service (QoS) and other performance requirements. it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, it would have been obvious that a skilled person will***

select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.]

Regarding Claim 7 Morita teaches the application processor is configured to hold the application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first. ***[Abstract, Col.1 lines 15-20; col.8 lines 50-62]***

Regarding Claim 8 John teaches the modem processor comprises the modem timer. ***[Fig.2]***

Regarding claim 9, the combination of John and Morita discloses the claimed invention except the application processor comprises the modem timer. It would have been an obvious matter of design choice to have a modem timer in the application processor, since applicant has not disclosed that having a modem timer in the application processor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the system describes by the combination of John and Morita. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975).

Regarding Claim 10 John teaches an application timer, and wherein the modem processor is configured to instruct the application processor to send an interrupt if no data is received within one time slot of the application timer. ***[0037]***

Regarding Claim 11 John teaches a byte accumulation limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the byte accumulation limit counter is exceeded. ***[0037]***

Regarding Claim 12 John teaches a packet number limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the packet number limit counter is exceeded. ***[0037]***

Regarding Claim 13 John teaches the modem processor is configured to determine if held data comprises a control packet and send such control packet before expiration of the modem timer. ***[0037]***

Regarding Claim 14 John teaches the modem processor further comprises an application timer, and the modem processor is configured to pull data from the application processor on receipt of the modem processor to application processor data or expiration of the application timer. ***[0037]***

Claim 15 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 15 is rejected under a similar rational as that of claim 1 above.

Regarding Claim 16 John teaches passing the data comprises passing the data over a peripheral component interface (PCI) compliant bus. ***[[0028], PCI Express]***

Regarding Claim 17 John teaches a period of the downlink timer comprises six (6) milliseconds. ***[[0009] maintaining Quality of Service (QoS) and other performance requirements. it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, it would have been obvious that a skilled person will select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.]***

Regarding Claim 18 John teaches a period of the uplink timer comprises seven (7) milliseconds. ***[[0009] maintaining Quality of Service (QoS) and other performance requirements. it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, it would have been obvious that a skilled person will select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.]***

Regarding Claim 19 John teaches comprising providing an override capability based on one of accumulated packet size, accumulated packet count, accumulated byte count, quality of service requirement, and control message status. ***[0037]***

Claim 20 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 20 is rejected under a similar rational as that of claim 1 above.

Regarding claim 21, the combination of John and Morita discloses the claimed invention except the application processor comprises the application timer. . It would have been an obvious matter of design choice to have an application timer in the application processor, since applicant has not disclosed that having an application timer in the application processor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the system describes by the combination of John and Morita. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975).

Regarding claim 22, the combination of John and Morita discloses the claimed invention except the modem processor comprises the application timer. It would have been an obvious matter of design choice to have an application timer in the modem processor, since applicant has not disclosed that having a application timer in the modem processor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the system describes by the combination of John and Morita. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975).

Regarding Claim 23 John teaches comprising a byte counter counting bytes at the modem processor. ***[0037]***

Claim 24 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 24 is rejected under a similar rational as that of claim 1 above.

Claim 25 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 25 is rejected under a similar rational as that of claim 1 above.

Claim 26 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 26 is rejected under a similar rational as that of claim 1 above.

Claim 27 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 27 is rejected under a similar rational as that of claim 1 above.

Claim 28 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 28 is rejected under a similar rational as that of claim 1 above.

Claim 29 is having similar limitations to that of the apparatus of claim 1. Accordingly, claim 29 is rejected under a similar rational as that of claim 1 above.

Regarding Claim 30 Morita teaches a second modem processor, the second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor. ***[col.7, lines 22-co.8, lines 65]***

Regarding Claim 31 Morita teaches holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor. ***[col.7, lines 22-co.6, lines 65]***

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ZAHID CHOUDHURY whose telephone number is (571)270-5153. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huynh Kim can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ZAHID CHOUDHURY/
Primary Examiner, Art Unit 2116

Notice of References Cited	Application/Control No. 14/568,694	Applicant(s)/Patent Under Reexamination KAUSHIK ET AL.	
	Examiner ZAHID CHOUDHURY	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,619,681 A	04-1997	Benhamida; Boubekeur	G06F13/385	703/23
*	B	US-6,021,264 A	02-2000	Morita; Hiroshi	G06F13/4213	710/117
*	C	US-6,151,355 A	11-2000	Vallee; Richard	G06F13/385	375/220
*	D	US-6,272,452 B1	08-2001	Wu; Yung-Jung Wayne	G06F13/385	703/24
*	E	US-6,472,770 B1	10-2002	Pohjola; Jorma	B60R16/0315	307/10.1
*	F	US-2003/0114186 A1	06-2003	GOETZ, IAN	H04M1/725	455/552.1
*	G	US-6,765,901 B1	07-2004	Johnson; Michael Ward	H04L12/2856	370/352
*	H	US-6,996,214 B1	02-2006	Beck; Laurence A.	H04M3/4281	379/215.01
*	I	US-RE39,427 E	12-2006	O'Sullivan; Harry M.		455/126
	J	US-				
	K	US-				
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FOREIGN PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/06/2016								
	1	✓								
	2	✓								
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	31	✓								

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2014-12-12
First Named Inventor	Vinod Harimohan Kaushik
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	141062/1173-141

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7137018	B2	2006-11-14	GUTMAN; Michael et al.	
	2	7647517	B2	2010-01-12	TSENG; Wen-Yu et al.	
	3	8615671	B2	2013-12-24	ROBLES; Raymond C. et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080034106	A1	2008-02-07	BAKSHI; Sanjay et al.	
	2	20090185487	A1	2009-07-23	ADAR; Etai et al.	
	3	20140207991	A1	2014-07-24	KAUSHIK; Vinod H. et al.	

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Receipt date: 12/12/2014	Application Number	14568694 - GAU: 2116
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	141062/1173-141

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Signature	/Zahid Choudhury/	Date Considered	06/06/2016

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Receipt date: 12/12/2014	Application Number	14568694 - GAU: 2116
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	141062/1173-141

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2014-12-12
Name/Print	Taylor M. Davenport	Registration Number	42466

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	50181	(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:13
L16	2018	(hold$3 delay$3 wait$3) near5 until near5 data near5 (send$3 sent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:14
L17	10	L16 and 15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 15:14
S1	459112	(hold$3 delay$3) near5 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:53
S2	602163	(rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S3	459112	S1 with S1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S4	1324	S1 with S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:54
S5	292	S4 same (CPU proceossr controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:55
S6	1	S5 same (cell mobile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 10:55
S7	4	"2013198538"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/06/02 11:19

			IBM_TDB			
S8	26	"2009039034"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:23
S9	2018	(hold$3 delay$3 wait$3) near5 until near5 data near5 (send$3 sent)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:29
S10	123	S9 with (CPU proceossr controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:30
S11	1	S10 same (rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:30
S12	10	S10 and (rounter$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 11:39
S13	31	"5727233"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:05
S14	91956	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem) near5 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:08
S15	92000	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem) near5 data$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:08
S16	1871	S15 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:09
S17	0	S6 and 713/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:10
S18	38	S16 and 713/$3.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:10
S19	97	S16 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/06/02 12:18

			IBM_TDB			
S20	93263	(hold$3 delay$3 wait$3) near5 (transmit$4 receiv$3 send$3 upstream downstrem uplink downlink) near5 data$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:19
S21	1890	S20 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:20
S22	97	S21 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:20
S23	27	"7137018"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:33
S24	959	(hold$3 delay$3 wait$3) near5 data near6 modem	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:44
S25	58	S24 same (serial bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:44
S26	3	"20130198538"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 12:58
S27	86	(hold$3 delay$3 wait$3) near5 data near6 modem near8 until	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:03
S28	47	(hold$3 delay$3 wait$3) near5 data near6 router near8 until	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:15
S29	25541	data near6 collision	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:17
S30	349	S29 same (router modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:17
S31	88	(hold$3 delay$3 wait$3) same S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/06/02 13:17

			IBM_TDB			
S32	44285	(hold$3 delay$3 wait$3) same (modem router)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:18
S33	88	S31 same (modem router)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:18
S34	4246	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till) near6 (receipt received)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:21
S35	59	S34 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:22
S36	33273	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:24
S37	1074	(hold$3 delay$3 wait$3) near5 data$1 near6 (until till) near5 (bus PCI PCIE serial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:24
S38	59	S35 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:25
S39	9	S37 same (router$1 modem$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:25
S40	42	S37 with (clear free idle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 13:26
S41	5731	(avoid$3 prevent$3) near5 data near6 collision	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:17
S42	4	S41 near6 ((network adj card) modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:17
S43	31	S41 same ((network adj card) modem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/06/02 14:19

			IBM_TDB			
S44	473	S41 near6 (PCI PCIE bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:22
S45	49	(hold$3 delay$3 wait$3) same S44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/02 14:22
S46	2	"9158628"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/06 09:01

EAST Search History (Interference)

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C:\Users\zchoudhury\Documents\EAST\Workspaces\14568694.wsp

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CONFIRMATION NO. 3463

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/568,694	12/12/2014 RULE	713	2116	141062/1173-141

APPLICANTS

QUALCOMM Incorporated, San Diego, CA;

INVENTORS

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Shailesh Maheshwari, San Diego, CA;
Alok Mitra, San Diego, CA;
Roshan Thomas Pius, San Jose, CA;
Hariharan Sukumar, San Diego, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 61/916,498 12/16/2013
and claims benefit of 62/019,073 06/30/2014

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/24/2014

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ZAHID CHOUDHURY/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	13	29	9

ADDRESS

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511
UNITED STATES

TITLE

POWER SAVING TECHNIQUES IN COMPUTING DEVICES

FILING FEE RECEIVED	FEES: Authority has been given in Paper	☐ All Fees
5140	No._____ to charge/credit DEPOSIT ACCOUNT	☐ 1.16 Fees (Filing)
	No._____ for following:	☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	14568694
Filing Date	2014-12-12
First Named Inventor	KAUSHIK; Vinod Harimohan
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	141062/1173-141

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Receipt date: 02/09/2016	Application Number	14568694	14568694 - GAU: 2116
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2014-12-12	
(Not for submission under 37 CFR 1.99)	First Named Inventor	KAUSHIK; Vinod Harimohan	
	Art Unit	2115	
	Examiner Name	LEE, THOMAS C	
	Attorney Docket Number	141062/1173-141	

	1	Second Written Opinion for PCT/US2014/070368, mailed November 9, 2015, 5 pages	

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	Art Unit	2115	
	Examiner Name	LEE, THOMAS C	
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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

X A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2016-02-09
Name/Print	Taylor M. Davenport	Registration Number	42466

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(Not for submission under 37 CFR 1.99)

Application Number	14568694
Filing Date	12-12-2014
First Named Inventor	KAUSHIK; Vinod Harimohan
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	141062/1173-141

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	1	20130198538	A1	2013-08-01	DIAB; Wael William et al.	

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	1	2009039034	WO	A1	2009-03-26	INTEL CORPORATION [US]		☐
	2	2010125429	WO	A1	2010-11-04	FREESCALE SEMICONDUCTOR, INC. [US]		☐

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Receipt date: 06/05/2015	Application Number	14568694	14568694 - GAU: 2116
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	12-12-2014	
(Not for submission under 37 CFR 1.99)	First Named Inventor	KAUSHIK; Vinod Harimohan	
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	Attorney Docket Number	141062/1173-141	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	AJANOVIC, J., "PCI Express™ Architecture Advanced Protocols & Features," December 31, 2003, PCI-SIG Developers Conference, retrieved February 25, 2015 from https://www.pcisig.com/developers/main/training_materials/get_document?doc_id=f275ada7d622d20947d69cbb34b6e0a0622249c3, 49 pages	☐
	2	International Search Report and Written Opinion for PCT/US2014/070368, mailed March 5, 2015, 14 pages	☐

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14568694	KAUSHIK ET AL.
	Examiner	Art Unit
	ZAHID CHOUDHURY	2116

CPC- SEARCHED		
Symbol	Date	Examiner
(G06F1/3202, G06F1/3231, G06F1/26, G06F1/206, G06F1/3228, G06F1/08, H04L12/12, G06F1/3289, G06F1/266, G06F1/206, H04L12/10)	6/6/2016	ZC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
NPL Search: Google. Google Patent	6/6/2016	ZC
East Search History is attached	6/6/2016	ZC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/ZAHID CHOUDHURY/ Primary Examiner.Art Unit 2116

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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X A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2016-02-09
Name/Print	Taylor M. Davenport	Registration Number	42466

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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WITHROW & TERRANOVA, P.L.L.C.
DOCKETED
NOV 23 2015
E.W.

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

WITHROW & TERRANOVA, PLLC
2530 Meridian Parkway, Suite 300
Durham, NC 27713
ETATS-UNIS D'AMERIQUE

PCT

WRITTEN OPINION OF THE INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

(PCT Rule 66)

Date of mailing *(day/month/year)*	09.11.2015
Applicant's or agent's file reference: 141062WO	**REPLY DUE** within 2 month(s) from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2014/070368	15.12.2014	16.12.2013

International Patent Classification (IPC) or both national classification and IPC
INV. G06F1/32

Applicant
QUALCOMM INCORPORATED

1. ☒ The written opinion established by the International Searching Authority:
   ☒ is ☐ is not
   considered to be a written opinion of the International Preliminary Examining Authority.

2. This second opinion contains indications relating to the following items:
   - ☒ Box No. I Basis of the opinion
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☒ Box No. V Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☐ Box No. VII Certain defects in the international application
   - ☒ Box No. VIII Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.
   When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(e).
   How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 55.3 and 66.8.
   Also: For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4*bis*. For an informal communication with the examiner, see Rule 66.6. For an additional opportunity to submit amendments, see Rule 66.4.

   If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary report on patentability (Chapter II of the PCT) must be established according to Rule 69.2 is: 16.04.2016

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	De Meyer, Arnaud Telephone No. +31 70 340-4302

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3(a) and 23.1(b)).
   - ☐ publication of the international application (under Rule 12.4(a))
   - ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a) and (b))

2. With regard to the elements of the international application, this opinion has been established on the basis of *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed")*:

Description, Pages

1-16 as originally filed

Claims, Numbers

1-29 as originally filed

Drawings, Sheets

1/13-13/13 as originally filed

   ☐ a sequence listing - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:

4. ☒ This opinion has been established as if (some of) the amendments listed below had not been made, since either they are considered to go beyond the disclosure as filed, or they were not accompanied by a letter indicating the basis for the amendments in the application as filed, as indicated in the Supplemental Box (Rules 70.2(c) and (c-*bis*)):
   - ☐ the description, pages
   - ☒ the claims, Nos. 1, 15, 20, 24-31
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:

5. ☐ This opinion has been established:
   - ☐ taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 66.1(d-*bis*)).
   - ☐ without taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 66.4*bis*).

6. ☐ Supplementary international search report(s) from Authority(ies) have been received and taken into account in drawing up this opinion (Rule 45*bis*.8(b) and (c)).

Box No. V Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	No:	Claims
Inventive step (IS)	No:	Claims 1-29
Industrial applicability (IA)	No:	Claims

2. Citations and explanations:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item I

Basis of the opinion

1 The amendments filed with the letter dated 23-06-2015 introduce subject-matter which extends beyond the content of the application as filed, contrary to **Article 34(2)(b) PCT.**

1.1 Claims 1, 20 and 24-27: This amendment is allegedly based on [0054]-[0056] of the description, which support fig.5. The wording of [0054]-[0056] is vague. In the light of fig.5, it appears that what is meant in [0054]-[0056] is that data from the application manager are transmitted *after* reception of the data from the modem processor; and not at the time of the receipt, as specified by the amended claims.

1.2 Claims 15, 28 and 29: The subject-matter of this amendment, allegedly based on [0053] of the description, is extracted from the technical context wherein it is disclosed, resulting in an intermediate generalisation. Specifically, the application as filed does not comprise any embodiment comprising the transition from the active power state to the low power state, without also specifying the transition from the low power state to the active power state. Furthermore, it is pointed out that this amendment also introduces obscurity into the claims, because it is not clear from the amended claims themselves what differentiates the active power state and the low power state.

1.3 Newly added claims 30-31: No mention of a second modem processor can be found in the application as filed. Therefore claims 30-31 introduce added subject-matter.

2 Under Rule 70.2 (c) PCT, this report shall be established as if the amendments objected upon in above §1.1-1.3 had not been made. These are all the amendments submitted by the applicant. Therefore this report shall be established on the claims as originally filed.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-29 does not involve an inventive step in the sense of **Article 33(3) PCT.**

3.1 Claims 1-29: The objections raised in §2-4 of the WO-ISA are upheld.

Re Item VIII

Certain observations on the international application

4 The objections raised in §5-6 of the WO-ISA are upheld.

5 Reply to the arguments of the applicant.

5.1 It is argued by the applicant that the terms "modem timer" are clear in the light of [0051]-[0055] of the application as filed. The claims should be clear by themselves. Therefore the argument of the applicant is not followed.

5.2 It is argued by the applicant that in some embodiments "uplink timer" and "application timer" refer to the same feature, and in other embodiments "uplink timer" and "application timer" are different features. The applicant states that the claims should be construed to encompass both alternatives. From the claims, however, the skilled person would understand from the use of two different names that only embodiments wherein "uplink timer" and "application timer" are different features are covered by the scope of the claims. The scope of the claims should be clarified.

5.3 It is argued by the applicant that the terms "modem byte accumulation limit counter" are clear in the light of [0063] of the application as filed. The claims should be clear by themselves. Therefore the argument of the applicant is not followed.

Electronic Acknowledgement Receipt

EFS ID:	24861606
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/Rebecca Meier
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	09-FEB-2016
Filing Date:	12-DEC-2014
Time Stamp:	11:24:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	141062_IDS_01-04-16.pdf	611972	no	4

Warnings:	
Information:	

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	Other Reference-Patent/App/Search documents	PCTUS2014070368_Second_WO_11-9-15.pdf	1001476 c3010599a7a3d69c4a0ad6c7cbd3446f97e9d1bfe	no	5

Warnings:

Information:

Total Files Size (in bytes):	1613448

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141

CONFIRMATION NO. 3463

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
Cary, NC 27518

PUBLICATION NOTICE

OC00000075811189

Title:POWER SAVING TECHNIQUES IN COMPUTING DEVICES

Publication No.US-2015-0169037-A1
Publication Date:06/18/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14568694
Filing Date	12-12-2014
First Named Inventor	KAUSHIK; Vinod Harimohan
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	141062/1173-141

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20130198538	A1	2013-08-01	DIAB; Wael William et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] j	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2009039034	WO	A1	2009-03-26	INTEL CORPORATION [US]		☐
	2	2010125429	WO	A1	2010-11-04	FREESCALE SEMICONDUCTOR, INC. [US]		☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	KAUSHIK; Vinod Harimohan
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	141062/1173-141

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	AJANOVIC, J., "PCI Express™ Architecture Advanced Protocols & Features," December 31, 2003, PCI-SIG Developers Conference, retrieved February 25, 2015 from https://www.pcisig.com/developers/main/training_materials/get_document?doc_id=f275ada7d622d20947d69cbb34b6e0a0622249c3, 49 pages	☐
	2	International Search Report and Written Opinion for PCT/US2014/070368, mailed March 5, 2015, 14 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14568694
	Filing Date	12-12-2014
	First Named Inventor	KAUSHIK, Vinod Harimohan
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	141062/1173-141

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2015-06-05
Name/Print	Taylor M. Davenport	Registration Number	42466

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 March 2009 (26.03.2009)

PCT

(10) International Publication Number
WO 2009/039034 A1

(51) International Patent Classification:
G06F 1/32 (2006.01) *G06G 7/10* (2006.01)
H04B 3/54 (2006.01)

(21) International Application Number:
PCT/US2008/076135

(22) International Filing Date:
12 September 2008 (12.09.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/973,031	17 September 2007 (17.09.2007)	US
60/973,035	17 September 2007 (17.09.2007)	US
60/973,038	17 September 2007 (17.09.2007)	US
60/973,044	17 September 2007 (17.09.2007)	US
12/208,654	11 September 2008 (11.09.2008)	US

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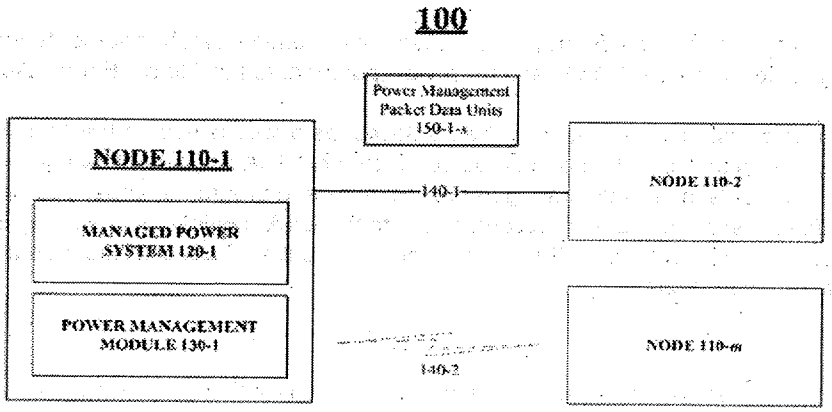


FIG. 1

(57) Abstract: Buffering techniques for power management are described. A method may comprise modifying a power state for a communications sub-system and a computing sub-system from a higher power state to a lower power state, storing packets of information in a buffer for the communications sub-system during a communications idle duration period, generating a variable receive threshold value for the buffer, and transferring the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value. Other embodiments are described and claimed.

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BUFFERING TECHNIQUES FOR POWER MANAGEMENT

BACKGROUND

[0001] Power management for electronic devices such as computer systems play an important part in conserving energy, managing heat dissipation, and improving overall system performance. Modern computers systems are increasingly designed to be used in settings where a reliable external power supply is not available making power management to conserve energy important. Power management techniques allow certain components of a computer system to be powered down or put in a sleep mode that requires less power than while in active operation, thereby reducing the total amount of energy consumed by a device over some period of time. Energy conservation is especially important for mobile devices to conserve battery power. Even when reliable external power supplies are available careful power management within the computing system can reduce heat produced by the system enabling improved performance of the system. Computing systems generally have better performance at lower ambient temperatures because key components can run at higher speeds without damaging their circuitry. Consequently, there are many advantages to enhancing power management for electronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] **FIG. 1** illustrates one embodiment of a communications system.

[0003] **FIG. 2** illustrates one embodiment of an apparatus.

[0004] **FIG. 3** illustrates one embodiment of a first logic diagram.

[0005] **FIG. 4** illustrates one embodiment of a second logic diagram.

[0006] **FIG. 5** illustrates one embodiment of a third logic diagram.

DETAILED DESCRIPTION

[0007] Various embodiments may be generally directed to buffering techniques to provide enhanced power management. Some embodiments may be particularly directed to power management techniques for conserving energy in a node operating from an energy storage device such as a battery. In one embodiment, for example, an apparatus such as a network device may include a power management module having a power management controller, and a managed power system to couple to the power management module. The managed power system may comprise a communications sub-system and a computing sub-system. The power management controller may be arranged to switch the communications sub-system and the computing sub-system to a lower power state to conserve energy.

[0008] In various embodiments, a communications sub-system for a first node may be arranged to process and store information received from other nodes within a communications system in a manner that increases energy conservation for a computing sub-system of the first node. In some embodiments, the communications sub-system may extend a time period for when the computing sub-system may remain in a lower power state by buffering packets and event information until ready for processing by the computing sub-system. This may reduce the number of interrupts sent to the computing sub-system when in a lower power state, with each interrupt forcing the computing sub-system to resume a higher power state to service the interrupt. This technique may sometimes be referred to as "interrupt coalescing."

[0009] In one embodiment, for example, the communications sub-system may further include a transceiver, buffer, watermark generator, and a buffer manager. The transceiver may be arranged to communicate information over a network. The buffer may be coupled to the transceiver, and arranged to store packets of information for the transceiver during a communications idle duration period to create a computing idle duration period. The communications idle duration period, for example, may refer to a time interval when the communications sub-system does not receive (or expect to receive) information from a network. The computing idle duration period, for example, may refer to a time interval when the computing sub-system does not receive (or expect to receive) information from the communications sub-system. The watermark generator may be coupled to the buffer, and arranged to generate a variable receive threshold value. The buffer manager may be coupled to the buffer and the watermark generator, and arranged to transfer the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value, among other factors. The variable receive threshold value may be algorithmically derived based on changing communications power state information, as described in more detail below. In this manner, the power management module may perform enhanced energy conservation for the managed power system by implementing buffering techniques and/or logic that allows the communications sub-system and/or the computing sub-system to enter and remain within a lower power state, while maintaining Quality of Service (QoS) and other performance requirements for the communications sub-system and/or the computing sub-system. Other embodiments are described and claimed.

[0010] Various embodiments may comprise one or more elements. An element may comprise any structure arranged to perform certain operations. Each element may be implemented as hardware, software, or any combination thereof, as desired for a given set of

design parameters or performance constraints. Although an embodiment may be described with a limited number of elements in a certain topology by way of example, the embodiment may include more or less elements in alternate topologies as desired for a given implementation. It is worthy to note that any reference to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0011] **FIG. 1** illustrates a block diagram of a communications system 100. In various embodiments, the communications system 100 may comprise multiple nodes. A node generally may comprise any physical or logical entity for communicating information in the communications system 100 and may be implemented as hardware, software, or any combination thereof, as desired for a given set of design parameters or performance constraints. Although FIG. 1 may show a limited number of nodes in a certain topology by way of example, it can be appreciated that more or less nodes may be employed in different topologies for a given implementation.

[0012] In various embodiments, the communications system 100 may comprise, or form part of, a wired communications system, a wireless communications system, or a combination of both. For example, the communications system 100 may include one or more nodes 110-1-*m* arranged to communicate information over one or more types of wired communications links, such as a wired communications link 140-1. Examples of the wired communications link 140-1 may include without limitation a wire, cable, bus, printed circuit board (PCB), Ethernet connection, peer-to-peer (P2P) connection, backplane, switch fabric, semiconductor material, twisted-pair wire, co-axial cable, fiber optic connection, and so forth. The communications system 100 also may include one or more nodes 110-1-*m* arranged to communicate information over one or more types of wireless communications links, such as wireless shared media 140-2. Examples of the wireless shared media 140-2 may include without limitation a radio channel, infrared channel, radio-frequency (RF) channel, Wireless Fidelity (WiFi) channel, a portion of the RF spectrum, and/or one or more licensed or license-free frequency bands. In the latter case, the wireless nodes may include one more wireless interfaces and/or components for wireless communications, such as one or more radios, transmitters, receivers, transceivers, chipsets, amplifiers, filters, control logic, network interface cards (NICs), antennas, antenna arrays, and so forth. Examples of an antenna may include, without limitation, an internal antenna, an omni-directional antenna, a monopole

antenna, a dipole antenna, an end fed antenna, a circularly polarized antenna, a micro-strip antenna, a diversity antenna, a dual antenna, an antenna array, and so forth. In one embodiment, certain devices may include antenna arrays of multiple antennas to implement various adaptive antenna techniques and spatial diversity techniques.

[0013] As shown in the illustrated embodiment of FIG. 1, the communications system 100 comprises multiple nodes 110-1-*m*. The nodes 110-1-*m* may comprise or be implemented as any type of fixed or mobile electronic device or resource, including a network device, network endpoint equipment, network infrastructure equipment, cellular radiotelephone network equipment, a processing system, a computer system, a computer sub-system, a computer, a workstation, a terminal, a server, a personal computer (PC), a laptop computer, an ultra-laptop computer, a portable computer, a handheld computer, a personal digital assistant (PDA),a cellular telephone, a smart phone, a router, a switch, a bridge, a gateway, a network appliance, a microprocessor, an integrated circuit, a programmable logic device (PLD), a digital signal processor (DSP), a processor, a circuit, a logic gate, a register, a microprocessor, an integrated circuit, a semiconductor device, a chip, a transistor, and so forth. In some embodiments, some of the nodes 110-1-*m* may represent heterogeneous network devices. In one embodiment, for example, the nodes 110-1-*m* may comprise various mobile computer systems (e.g., laptop computers, handheld computers, smart phones, cellular telephones, and so forth) utilizing a mobile power source, such as one or more batteries.

[0014] Although some of the nodes 110-1-*m* may comprise different network devices, each of the nodes 110-1-*m* may include a common number of elements as shown by the node 110-1. For example, the nodes 110-1-*m* may each include various power management elements to implement a power management scheme operative to perform power management operations for the nodes 110-1-*m*. In the illustrated embodiment shown in FIG. 1, for example, a first node 110-1 may include a managed power system 120-1 coupled to a power management module 130-1. The power management module 130-1 may be operative to communicate power state information with a second node (e.g., one of the nodes 110-2-*m*) over a communications connection established via the communications links 140-1, 140-2. In general operation, the power management module 130-1 may manage various power states for the managed power system 120-1 of the first node 110-1. The power state information may include past, present or future power states for one or more portions of a managed power system 120-1 of the first node 110-1. In this manner, the portions of a managed power system 120-1 may exchange power state information to improve or enhance power state management for the first node 110-1. For example, the power management module 130-1

may synchronize power management operations between the sub-systems 210-1, 230-1 of the managed power system 120-1, such as placing computing components of the computing sub-system 230-1 in lower power states based on operations or anticipated operations for the communications components of the communications sub-system 210-1 for a given power state duration period, and vice-versa.

[0015] Although the node 110-1 is the only node shown in FIG. 1 to include the managed power system 120-1 and the power management module 130-1, it may be appreciated that each of the nodes 110-1-*m* may include an identical or similar managed power system 120-1-*n* and power management module 130-1-*p*. For example, the node 110-2 may include a managed power system 120-2 coupled to a power management module 130-2, the node 110-3 may include the elements 120-3, 130-3, and so forth. Furthermore, the descriptions and examples of the structures and operations provided with reference to the managed power system 120-1 and the power management module 130-1 may also apply to the corresponding elements in the other nodes 110-2-*m*. Exemplary embodiments for the managed power system 120-1-*n* and the power management module 130-1-*p* may be described in more detail with reference to FIG. 2.

[0016] **FIG. 2** illustrates a more detailed block diagram for a managed power system 120 and a power management module 130. In the illustrated embodiment shown in FIG. 2, the managed power system 120 may include a communications sub-system 210 and a computing sub-system 230. Although FIG. 2 may show a limited number of power management elements in a certain arrangement by way of example, it can be appreciated that more or less power management elements may be employed in different arrangements for a given implementation.

[0017] In various embodiments, the managed power system 120 may include any electrical or electronic elements of the nodes 110-1-*m* consuming power from the power source 232 and suitable for power management operations. Power management techniques allow certain components of an electronic device or system (e.g., a computer system) to be powered down or put in a sleep mode that requires less power than while in active operation, thereby reducing the total amount of energy consumed by a device over some period of time. The power management techniques may be implemented by power gating and/or clock gating various hardware elements of the managed power system 120, thereby conserving battery power.

[0018] More particularly, the managed power system 120 may include various electrical or electronic elements of the nodes 110-1-*m* that can operate in various power states drawing

multiple levels of power from the power source 232 as controlled by the power management controller 234 of the power management module 130. The various power states may be defined by any number of power management schemes. In some cases, for example, the power states may be defined in accordance with the Advanced Configuration and Power Interface (ACPI) series of specifications, including their progeny, revisions and variants. In one embodiment, for example, the power states may be defined by the ACPI Revision 3.0a, December 30, 2005 (the "ACPI Revision 3.0a Specification"). The ACPI series of specifications define multiple power states for electronic devices, such as global system states (G*x* states), device power states (D*x* states), sleeping states (S*x* states), processor power states (C*x* states), device and processor performance states (P*x* states), and so forth. It may be appreciated that other power states of varying power levels may be implemented as desired for a given set of design parameters and performance constraints. The embodiments are not limited in this context.

[0019] In some embodiments, the various electrical or electronic elements of the nodes 110-1-*m* suitable for power management operations may be generally grouped or organized into the communications sub-system 210 and the computing sub-system 230. It may be appreciated, however, that the sub-systems 210, 230 are provided by way of example for purposes of clarity and not limitation, and the managed power system 120 may include other electrical or electronic elements of the nodes 110-1-*m* suitable for power management operations by the power management module 130. For example, the nodes 110-1-*m* may typically include a computer monitor or display, such as a digital electronic display or an analog electronic display. Examples of digital electronic displays may include electronic paper, nixie tube displays, vacuum fluorescent displays, light-emitting diode displays, electroluminescent displays, plasma display panels, liquid crystal displays, thin-film transistor displays, organic light-emitting diode displays, surface-conduction electron-emitter displays, laser television displays, carbon nanotubes, nanocrystal displays, and so forth. An example for analog electronic displays may include cathode ray tube displays. Computer monitors are often placed in a sleep mode when an operating system detects that the computer system has not received any input from a user for a defined period of time. Other system components may include digital cameras, touch screens, video recorders, audio recorders, storage devices, vibrating elements, oscillators, system clocks, controllers, and other platform or system architecture equipment. These other system components can also be placed in a sleep or powered down state in order to conserve energy when the components are

not in use. The computer system monitors input devices and wakes devices as needed. The embodiments are not limited in this context.

[0020] In various embodiments, the managed power system 120 may include the communications sub-system 210. The communications sub-system 210 may comprise various communications elements arranged to communicate information and perform communications operations between the nodes 110-1-*m*. Examples of suitable communications elements may include any electrical or electronic element designed to communicate information over the communications links 140-1, 140-2, including without limitation radios, transmitters, receivers, transceivers, chipsets, amplifiers, filters, control logic, interfaces, network interfaces, network interface cards (NICs), antennas, antenna arrays, digital signal processors, baseband processors, media access controllers, memory units, and so forth.

[0021] In various embodiments, the communications sub-system 210-1 may include one or more transceivers 204-1-*r* capable of operating at different communications rates. The transceivers 204-1-*r* may comprise any communications elements capable of transmitting and receiving information over the various wired media types (e.g., copper, single-mode fiber, multi-mode fiber, etc.) and wireless media types (e.g., RF spectrum) for communications link 140-1, 140-2. Examples of the transceivers 204-1-*r* may include various Ethernet-based PHY devices, such as a Fast Ethernet PHY device (e.g., 100Base-T, 100Base-TX, 100Base-T4, 100Base-T2, 100Base-FX, 100Base-SX, 100BaseBX, and so forth), a Gigabit Ethernet (GbE) PHY device (e.g., 1000Base-T, 1000Base-SX, 1000Base-LX, 1000Base-BX10, 1000Base-CX, 1000Base-ZX, and so forth), a 10 GbE PHY device (e.g., 10GBase-SR, 10GBase-LRM, 10GBase-LR, 10GBase-ER, 10GBase-ZR, 10GBase-LX4, 10GBase-CX4, 10GBase-Kx, 10GBase-T, and so forth), a 100 GbE PHY device, and so forth. The transceivers 204-1-*r* may also comprise various radios or wireless PHY devices, such as for mobile broadband communications systems. Examples of mobile broadband communications systems include without limitation systems compliant with various Institute of Electrical and Electronics Engineers (IEEE) standards, such as the IEEE 802.11 standards for Wireless Local Area Networks (WLANs) and variants, the IEEE 802.16 standards for Wireless Metropolitan Area Networks (WMANs) and variants, and the IEEE 802.20 or Mobile Broadband Wireless Access (MBWA) standards and variants, among others. The transceivers 204-1-*r* may also be implemented as various other types of mobile broadband communications systems and standards, such as a Universal Mobile Telecommunications System (UMTS) system series of standards and variants, a Code Division Multiple Access (CDMA) 2000 system series of

standards and variants (e.g., CDMA2000 1xRTT, CDMA2000 EV-DO, CDMA EV-DV, and so forth), a High Performance Radio Metropolitan Area Network (HIPERMAN) system series of standards as created by the European Telecommunications Standards Institute (ETSI) Broadband Radio Access Networks (BRAN) and variants, a Wireless Broadband (WiBro) system series of standards and variants, a Global System for Mobile communications (GSM) with General Packet Radio Service (GPRS) system (GSM/GPRS) series of standards and variants, an Enhanced Data Rates for Global Evolution (EDGE) system series of standards and variants, a High Speed Downlink Packet Access (HSDPA) system series of standards and variants, a High Speed Orthogonal Frequency-Division Multiplexing (OFDM) Packet Access (HSOPA) system series of standards and variants, a High-Speed Uplink Packet Access (HSUPA) system series of standards and variants, and so forth. The embodiments are not limited in this context.

[0022] In various embodiments, a controller 208 may be operative to switch communications rates using a single transceiver (e.g., 204-1) or multiple transceivers 204-1-*r*. The controller 208 may be implemented as any computing elements or logic device capable of executing logical operations, such as processors, microprocessors, chipsets, controllers, microcontrollers, embedded controllers, media access controller, baseband controller, and so forth. The transceivers 204-1-*r* may individually or collectively operate at different communications rates or link rates. In one embodiment, for example, a single transceiver 204-1 may be capable of operating at various communications rates. In another embodiment, for example, a first transceiver 204-1 may be capable of operating at a first communications rate, a second transceiver 204-2 may be capable of operating at a second communications rate, and so forth. The controller 208 may switch the first transceiver 204-1 from a first communications rate to a second communications rate, or switch operations from the first transceiver 204-1 to a second transceiver 204-2, to achieve the desired communications rate. The controller 208 may switch communications rates in accordance with a control policy, such as one or more Energy Efficient Ethernet (EEE) control policies, for example. The controller 208 may also switch communications rates in accordance with instructions from a buffer manager 216.

[0023] In various embodiments, the communications sub-system 210-1 may include one or more buffers 206-1-*t* managed by a buffer manager 216. The buffers 206-1-*t* may be operative to store network packets received by the transceivers 204-1-*r*, or ready for transmission by the transceivers 204-1-*r*. For example, the buffers 206-1-*t* may be used to buffer packets when the communications sub-system 210-1 or the computing sub-system

230-1 enters a lower power state and is therefore unable to communicate or process the packets. In another example, the buffers 206-1-*t* may be used to buffer packets until the communications rate for the transceiver has been completely switched or modified since switching communications rates for the transceivers 204-1-*r* is typically not instantaneous. The buffers 206-1-*t* may be implemented, for example, as standard First-In-First-Out (FIFO) queues. The buffer manager 216 may implement various types of buffer logic to manage operations for the buffers 201-1-*t*.

[0024] In various embodiments, the managed power system 120 may include the computing sub-system 230. The computing sub-system 230 may comprise various computing elements arranged to process information and perform computing operations for the nodes 110-1-*m*. Examples of suitable computing elements may include any electrical or electronic element designed to process information, including without limitation processors, microprocessors, chipsets, controllers, microcontrollers, embedded controllers, clocks, oscillators, audio cards, video cards, multimedia cards, peripherals, memory units, memory controllers, video controllers, audio controllers, multimedia controllers, and so forth.

[0025] In various embodiments, the power management module 130 may comprise a power source 232. The power source 232 may be arranged to provide power to the elements of a node 110-1-*m* in general, and the managed power system 120 in particular. In one embodiment, for example, the power source 232 may be operative to provide varying levels of power to the communications sub-system 210 and the computing sub-system 230. In various embodiments, the power source 232 may be implemented by a rechargeable battery, such as a removable and rechargeable lithium ion battery to provide direct current (DC) power, and/or an alternating current (AC) adapter to draw power from a standard AC main power supply.

[0026] In various embodiments, the power management module 130 may include a power management controller 234. The power management controller 234 may generally control power consumption by the managed power system 120. In one embodiment, the power management controller 234 may be operative to control varying levels of power provided to the communications sub-system 210 and the computing sub-system 230 in accordance with certain defined power states. For example, the power management controller 234 may modify, switch or transition the power levels provided by the power source 232 to the sub-systems 210, 230 to a higher or lower power level, thereby effectively modifying a power state for the sub-systems 210, 230.

[0027] In various embodiments, the power management module 130 may include one or more power control timers 236. The power control timer 236 may be used by the power management controller 234 to maintain a certain power state for a given power state duration period. The power state duration period may represent a defined time interval a node or portion of a node is in a given power state. For example, the power management controller 234 may switch the computing sub-system 230 from a higher power state to a lower power state for a defined time interval, and when the time interval has expired, switch the computing sub-system 230 back to the higher power state.

[0028] In order to coordinate power management operations for a node 110-1-*m*, the communications sub-system 210, the computing sub-system 230, and the power management module 130 may communicate various power management messages 240-1-*q* via a communications bus 220 and the respective power management interfaces 214-1, 214-2, and 214-3. To manage power for all the devices in a system, an operating system typically utilizes standard techniques for communicating control information over a particular Input/Output (I/O) interconnect. Examples of various I/O interconnects suitable for implementation as the communications bus 220 and associated interfaces 214 may include without limitation Peripheral Component Interconnect (PCI), PCI Express (PCIe), CardBus, Universal Serial Bus (USB), IEEE 1394 FireWire, and so forth.

[0029] Referring again to FIG. 2, the communications sub-system 210 may include a network state module 212. The network state module 212 may be arranged to monitor certain states or characteristics of the communications sub-system 210, such as the traffic activity of the communications connections 250-1-*v*, capabilities information, and other operations for the various communications elements of the communications sub-system 210. The network state module 212 may send communications power management messages 240-1-*q* to the power management module 130 with the measured characteristics. The power management module 130 may generate power state information 260 for the managed power system 120 based in part on the communications power management messages 240-1-*q*.

[0030] Similarly, the computing sub-system 230 may include a computing state module 232. The computing state module 232 may be arranged to monitor certain states or characteristics of the computing sub-system 230, such as the level of system activity, capabilities information, and other operations for the various computing elements of the computing sub-system 230. The computing state module 232 may send computing power management messages 240-1-*q* to the power management module 130 with the measured

characteristics. The power management module 130 may generate power state information 260 for the managed power system 120 based in part on the computing power management messages 240-1-*q*.

[0031] In general operation, the power management module 130-1 may perform power management operations for portions of the managed power system 120-1 of the node 110-1 based on power state information received from other portions of the first node 110-1. In some cases, for example, the power management module 130-1 for the node 110-1 may be operative to receive communications power state information from the network state module 212 of the communications sub-system 210-1 for the managed power system 120-1 over the communications bus 220. The power management module 130-1 may manage various power states for the computing sub-system 230-1 of the managed power system 120-1 for the node 110-1 based on the communications power state information for the communications sub-system 210-1. The power management module 130-1 and the sub-systems 210-1, 230-1 may communicate the communications power state information over the communications bus 220 in accordance with various communications bus protocols.

[0032] The communications power state information may represent information explicitly or implicitly related to power states for the communications sub-system 210. The communications power state information may also represent various characteristics or attributes for the power states of the communications sub-system 210, such as such as power state duration periods, idle durations, resume latencies, and so forth. In one embodiment, for example, the communications power state information may include without limitation a communications power state parameter, a communications idle duration parameter, a communications resume latency parameter, or a power state duration period. The communications idle duration parameter represents an amount of time, or defined time interval, the network link or communications sub-system 210-1 will remain in a given power state. The communications idle duration parameter allows the sub-systems 210-1, 230-1 to enter and exit the lower power states with a deterministic manner. The communications resume latency parameter represents an amount of time, or defined time interval, the network link or communications sub-system 210-1 needs to exit a given power state and enter a higher power state. The communications resume latency parameter allows the sub-systems 210-1, 230-1 to determine how soon it can expect the communications sub-system 210-1 to wake up and be ready for providing services such as out-going transmission. The communications idle duration parameter and the communications resume latency parameter may be

communicated by the power management messages 240-1-*q* over the communications bus 220.

[0033] In various embodiments, the network state module 212 may be arranged to generate the communications idle duration parameter and the communications resume latency parameter based on the capabilities of the communications sub-system 210-1. For example, the communications sub-system 210-1 may implement various buffers to store information received from the communications connections 250-1-*v*, such as network packets, and forward the information for servicing and processing by the computing sub-system 230-1. In another example, the communications sub-system 210-1 may also implement various buffers to store information received from the communications bus 220, such as network packets, and forward the information for communications by the communications sub-system 210-1 to other nodes 110-2-*m* over the communications connections 250-1-*v* via the communications links 140-1, 140-2. In yet another example, the communications sub-system 210-1 may include various wired or wireless transceiver operating at different communications speeds, such as the IEEE 802.3-2005 standard 10 Gigabit Ethernet (10GbE or 10GigE), the IEEE 802.3ba proposed standard 100 Gigabit Ethernet (100GbE or 100GigE), and so forth. In still another example, the communications sub-system 210-1 may include various processors operating at different speeds, such as baseband or communications processor. In still another example, the network state module 212 may monitor the rate of information being received over the communications connections 250-1-*v* via the communications links 140-1, 140-2. In this example, the network state module 212 of the communications sub-system 210-1 may monitor the communications links 140-1, 140-2 to measure packet inter-arrival times. Other examples of communications capabilities may include other network traffic load measurements on the communications links 140-1, 140-2 (e.g., synchronous traffic, asynchronous traffic, burst traffic, and so forth), a signal-to-noise ratio (SNR), a received signal strength indicator (RSSI), throughput of the communications bus 220, physical layer (PHY) speed, power state information 260 for other nodes 110-2-*m* received via one or more PMPDU 150-1-*s*, and so forth. The network state module 212 may evaluate these and other network or communications capabilities of the communications sub-system 210-1, and generate the appropriate communications idle duration parameter and the communications resume latency parameter based on the evaluated capabilities of the communications sub-system 210-1.

[0034] In various embodiments, the nodes 110-1-*m* may use the communications power state information to enhance power management operations for a given node 110-1-*m* to

improve energy conservation (e.g., increase battery life or decrease battery size), heat dissipation or overall system performance. In one embodiment, for example, the network state module 212 of the communications sub-system 210-1 may monitor the communications links 140-1, 140-2 and various communications elements (e.g., radio, baseband processor, chipset, memory units, etc.) to determine communications power state information for the communications sub-system 210-1. The network state module 212 may send a power management message 240-1-*q* with the communications power state information over the communications bus 220 and interfaces 214-1, 214-3 to the power management module 130-1. The power management module 130-1 may receive the power management message 240-1-*q*, and retrieve the communications power state information from the power management message 240-1-*q*. The power management module 130-1 may manage power states for the computing sub-system 230-1 based on the communications power state information for the communications sub-system 210-1. For example, the power management module 130-1 may modify a power level for a computing sub-system 230-1 of the managed power system 120-1 from a first power level to a second power level using the communications power state information for the communications sub-system 210-1. Furthermore, the power management module 130-1 may modify the power level for the computing sub-system 230-1 from a first power level to a second power level for a defined time interval, referred to as a power state duration period, as determined using the communications power state information for the communications sub-system 210-1.

[0035] Whenever the communications sub-system 210-1 has been placed in a lower power state, however, the communications sub-system 210-1 may still continue to receive packets of information from other nodes 110-2-*m* over the communications links 140-1, 140-2, as well as packets of information from the computing sub-system 230-1 ready for transmit by the communications sub-system 210-1 to other nodes 110-2-*m* over the communications links 140-1, 140-2. If every packet received by the communications sub-system 210-1 were sent directly to the computing sub-system 230-1 for processing, the computing sub-system 230-1 would continually need to exit a lower power state and enter and higher power state to process each packet. This may consume significant amounts of energy from the power source 232.

[0036] To solve these and other problems, the communications sub-system 210-1 may implement interrupt coalescing techniques. For example, the communications sub-system 210-1 may be arranged to store or buffer incoming packets using one or more of the buffers 206-1-*t*, and the buffer manager 216 may determine when to release or transfer the stored

packets to the computing sub-system 230-1 for processing. The buffer manager 216 may determine when to transfer the packets from the buffers 206-1-*t* to the computing sub-system 230-1 in accordance with a buffer management policy designed to increase energy conservation for the computing sub-system 230-1, and therefore the overall node 110-1.

[0037] In various embodiments, the buffer manager 216 may implement a buffer management policy designed to allow the communications sub-system 210-1 and/or the computing sub-system 230-1 to enter and stay in a lower power state for a longer period of time, while maintaining QoS, throughput and other performance requirements for the communications sub-system 210-1 and/or the computing sub-system 230-1. In some embodiments, the buffer management policy may include various buffer management rules to determine when to transfer the packets from the buffers 206-1-*t* to the computing sub-system 230-1. In one embodiment, for example, the buffer manager 216 may implement a buffer management rule to store packets in the buffers 206-1-*t* during a communications idle duration period, and transfer the stored packets from the buffers 206-1-*t* to the computing sub-system 230-1 when any combination of four buffer management conditions are satisfied, including: (1) when a number of packets stored by one or more buffers 206-1-*t* exceeds a variable receive threshold value; (2) when a buffer unload timeout value expires; (3) when a buffer unload event signal is received; and/or (4) when a communications idle duration parameter is less than a communications idle duration threshold value. It may be appreciated that these 4 buffer management conditions are provided by way of example and not limitation. The embodiments are not limited in this context.

[0038] The buffer manager 216 may utilize one or more of the buffer management conditions, in various combinations, to trigger a release or transfer of any packets stored within the buffers 206-1-*t* to the computing sub-system 230-1 for processing. In one embodiment, for example, the buffer manager 216 may transfer the packets stored within the buffers 206-1-*t* to the computing sub-system 230-1 utilizing a direct memory access (DMA) technique to accelerate movement of the packets from the buffers 206-1-*t* to the memory units 234 used by the computing sub-system 230-1. The buffer manager 216 may then issue an interrupt to the computing sub-system 230-1 (e.g., a processor) to indicate packets are in the memory units 234 and ready for processing by the computing sub-system 230-1.

[0039] In one embodiment, the buffer manager 216 transfer the stored packets from the buffers 206-1-*t* to the computing sub-system 230-1 when a number of packets stored by one or more buffers 206-1-*t* exceeds a variable receive threshold value. For example, the communications sub-system 210-1 may include a watermark generator 217 coupled to the

buffer manager 216 and the buffers 206-1-*t*. The watermark generator 217 may be operative to generate a variable receive threshold value. The variable receive threshold value may comprise a defined threshold value or watermark for the buffers 206-1-*t*. The variable receive threshold value may be calculated, derived or otherwise determined as a function with at least three inputs, including: (1) a receive data rate parameter; (2) a buffer size parameter; and (3) a communications resume latency parameter. The receive data rate parameter may represent a communications rate for one or more transceivers 204-1-*r*. The buffer size parameter may represent a size for one or more buffers 206-1-*t*. The communications resume latency parameter may represent an amount of time, or defined time interval (e.g., 1 ms), the network link or communications sub-system 210-1 needs to exit a given power state and enter a higher power state. Utilizing these or other communications parameters, the watermark generator 217 may periodically, continuously or on-demand generate the variable receive threshold value, thereby ensuring the variable receive threshold accurately reflects changing communications rates, latencies and other network traffic considerations. The buffer manager 216 may receive the variable receive threshold value from the watermark generator 217 and a current buffer utilization parameter from the buffers 206-1-*t*, compare the current buffer utilization parameter with the variable receive threshold value, and initiate a DMA transfer based on the comparison results. For example, the buffer manager 216 may initiate the DMA transfer when a number of packets of information stored by the buffer exceeds a variable receive threshold value.

[0040] In one embodiment, the buffer manager 216 may transfer the stored packets from the buffers 206-1-*t* to the computing sub-system 230-1 when a buffer unload timeout value expires. For example, the communications sub-system 210-1 may include a buffer timer 218 to couple to the buffer manager 216. The buffer timer 218 may be a hardware or software timer used to time or measure a defined time interval. For example, the buffer timer 218 may be set or loaded with a buffer unload timeout value. The buffer timer 218 may monitor or perform a count down until the buffer unload timeout value expires. The buffer manager 216 may be arranged to transfer the stored packets of information from the buffers 206-1-*t* to the computing sub-system 230-1 when the buffer unload timeout value expires. When used in combination with another buffer management condition, such as the variable receive threshold value, the buffer manager 216 may transfer the stored packets when the buffer unload timeout value expires before a number of packets stored by the buffers 206-1-*t* exceeds the variable receive threshold value.

[0041] In one embodiment, the buffer manager 216 may transfer the stored packets from the buffers 206-1-*t* to the computing sub-system 230-1 when a buffer unload event signal is received by the buffer manager 216. For example, the communications sub-system 210-1 may randomly receive event signals from various portions of the node 110-1 that merits the buffer manager 216 to transfer the packets from the buffers 206-1-*t* to the computing sub-system 230-1. For example, assume the computing sub-system 230-1 implements a chipset computer architecture that includes a memory controller hub (MCH) and an input/output (I/O) controller hub (ICH), such as the "northbridge" and "southbridge" controller hubs made by Intel® Corporation, Santa Clara, California. Further assume the MCH and ICH communicate information using a direct media interface (DMI) and associated link. As with other portions of the computing sub-system 230-1, the DMI link may be placed in various power states, such as a higher power state L0 and a lower power state L1. When the DMI link exits from the lower power state L1 to the higher power state L0 due to activities by other devices, the computing sub-system 230-1 may send a buffer unload event signal to the buffer manager 216. The buffer unload event signal may indicate to the buffer manager 216 that the computing sub-system 230-1 is already in a higher power state and active, and therefore the buffer manager 216 may opportunistically use the higher power state of the computing sub-system 230-1 to transfer the packets from the buffers 206-1-*t* to the memory 234. When used in combination with another buffer management condition, such as the variable receive threshold value, the buffer manager 216 may transfer the stored packets when it receives a buffer unload event signal before a number of packets stored by the buffer 206-1-*t* exceeds the variable threshold value.

[0042] In one embodiment, the buffer manager 216 may implement a buffer management rule to transfer the stored packets from the buffers 206-1-*t* to the computing sub-system 230-1 when a communications idle duration parameter is less than a communications idle duration threshold value. The communications idle duration threshold value may comprise a defined threshold value for the communications idle duration parameter. Typically, the higher the communications idle duration parameter, the lower the communications rates for data coming over the communications links 140-1, 140-2, and vice-versa. The communications idle duration threshold value is configurable, and may be set to determine when the communications idle duration parameter is low enough to indicate a high enough communications rate that will not necessarily tolerate any additional latencies introduced by the buffers 206-1-*t*. The buffer manager 216 may be arranged to disable one or more of the buffers 206-1-*t* to prevent the buffers 206-1-*t* from storing the packets of information when

the communications idle duration parameter is lower than a communications idle duration threshold value.

[0043] In some embodiments, the buffer manager 216 may be arranged to issue signals to the controller 208 to modify communications rates for the transceivers 204-1-*r*. For example, the buffer manager 216 may instruct the controller 208 to modify communications rates based on its FIFO size and/or energy left. In one embodiment, for example, the buffer manager 216 may receive or maintain a buffer size parameter, an energy measurement parameter, or both parameters. The buffer size parameter may represent a FIFO size or FIFO remaining capacity. The energy measurement parameter may represent an amount of energy remaining for a power source, such as the power source 232. The buffer manager 216 may be arranged to send a request to the controller 208 to adjust a communications rate for the transceivers 204-1-*r* based on the buffer size parameter. Similarly, the buffer manager 216 may be arranged to receive a power management message with an energy measurement parameter from the power management controller 234, and send a request to adjust a communications rate for the transceivers 204-1-*r* based on the energy measurement parameter.

[0044] **FIG. 3** illustrates a logic flow 300 in accordance with one or more embodiments. The logic flow 300 may be performed by various systems and/or devices and may be implemented as hardware, software, and/or any combination thereof, as desired for a given set of design parameters or performance constraints. For example, the logic flow 300 may be implemented by a logic device (e.g., processor) and/or logic (e.g., instructions, data, and/or code) to be executed by a logic device. For purposes of illustration, and not limitation, the logic flow 300 is described with reference to FIGS. 1-2.

[0045] The logic flow 300 may illustrate various operations for the nodes 110-1-*m* in general, and the managed power system 120 and the power management module 130 in particular. As shown in FIG. 3, the logic flow 300 may modify a power state for a communications sub-system and a computing sub-system from a higher power state to a lower power state at block 302. The logic flow 300 may store packets of information in a buffer for the communications sub-system during a communications idle duration period to create a computing idle duration period at block 304. The logic flow 300 may generate a variable receive threshold value for the buffer at block 306. The logic flow 300 may transfer the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value at block 308. The embodiments are not limited in this context.

[0046] In one embodiment, the logic flow 300 may modify a power state for a communications sub-system and a computing sub-system from a higher power state to a lower power state at block 302. For example, the power management controller 234 may receive power management messages 240-1-*q* with computing power state information generated by the computing state module 232 and communications power state information generated by the network state module 212. The power management controller 234 may receive the power management messages 240-1-*q* from the communications bus 220 via the interfaces 214-1, 214-2 and 214-3. The power management controller 234 may process the power management messages 240-1-*q*, and determine an appropriate communications power state (e.g., NL0, NL1, NL2, etc.) and an appropriate computing power state (e.g., S0, S0i1, S0i2, S0i3, S4, etc.). The power management controller 234 may send the communications power state and the computing power state to the respective sub-systems 210-1, 210-2 via power management messages 240-1-*q* over the communications bus 220 and interfaces 214-1, 214-2 and 214-3, and the sub-systems 210-1, 210-2 may modify their respective power states accordingly.

[0047] In one embodiment, the logic flow 300 may store packets of information in a buffer for the communications sub-system during a communications idle duration period to create a computing idle duration period at block 304. The communications idle duration period, for example, may refer to a time interval when the communications sub-system 210-1 does not receive (or expect to receive) information from a network over the communications links 140-1, 140-2. The computing idle duration period, for example, may refer to a time interval when the computing sub-system 230-1 does not receive (or expect to receive) information from the communications sub-system 210-1. By way of example, the communications sub-system 210-1 may receive the communications idle duration parameter from the power management messages 240-1-*q* for the communications sub-system 210-1 sent by the power management controller 234. In this case, the communications idle duration parameter may be calculated by the power management controller 234 using the power state information received from the sub-systems 210-1, 230-1. In another example, the communications sub-system 210-1 may receive the communications idle duration parameter from the network state module 212. In either case, the communications sub-system 210-1 may enter a lower power state indicated by the communications power state for a time interval defined by the communications idle period parameter. The lower power state may be entered directly by reducing power to all communications elements for the communications sub-system 210-1, or indirectly by modifying a communications rate for the transceivers 204-

1-*r*. Once the communications sub-system 210-1 enters the lower power state, the buffer manager 216 may store packets of information in one or more receive buffers 206-1-*t* for the communications sub-system 210-1- during a communications idle duration period defined by the communications idle duration parameter, thereby creating a computing idle duration period for the computing sub-system 230-1. In some cases, the communications sub-system 210-1 may communicate the computing idle duration period to the computing sub-system 230-1 so that the computing sub-system 230-1 may operate accordingly, such as switching to a lower power state for a time interval corresponding to the expected computing idle duration period.

[0048] In one embodiment, the logic flow 300 may generate a variable receive threshold value for the buffer at block 306. For example, the watermark generator 217 may receive a receive data rate parameter, a buffer size parameter, and/or a communications resume latency parameter, and generates a variable receive threshold value (e.g., buffer watermark) for the receive buffers 206-1-*t* based on these parameters. The watermark generator 217 may output the variable receive threshold value to the buffer manager 216.

[0049] In one embodiment, the logic flow 300 may transfer the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value at block 308. For example, the buffer manager 216 may receive the variable receive threshold value from the watermark generator 217, set the buffers 206-1-*t* with the variable receive threshold value, and may periodically or aperiodically compare a number of packets of information stored by the receive buffers 206-1-*t* with the variable receive threshold value. When a number of packets of information stored by the receive buffers 206-1-*t* meets or exceeds the variable receive threshold value, the buffer manager may transfer the contents of the receive buffers 206-1-*t* to the memory units 234 of the computing sub-system 230 via a DMA transfer for further processing.

[0050] **FIG. 4** illustrates a logic flow 400 in accordance with one or more embodiments. The logic flow 400 may be performed by various systems and/or devices and may be implemented as hardware, software, and/or any combination thereof, as desired for a given set of design parameters or performance constraints. For example, the logic flow 400 may be implemented by a logic device (e.g., processor) and/or logic (e.g., instructions, data, and/or code) to be executed by a logic device. For purposes of illustration, and not limitation, the logic flow 400 is described with reference to FIGS. 1-2.

[0051] The logic flow 400 may illustrate various operations for the nodes 110-1-*m* in general, and the managed power system 120 and the power management module 130 in

particular. As shown in FIG. 4, the logic flow 400 begins at block 402 by having the watermark generator 217 calculating or re-calculating a variable receive threshold value (e.g., buffer watermark) with a receive data rate parameter, a buffer size parameter, and/or a communications resume latency parameter, and then configures the buffer watermark trigger. This allows the buffer manager 216 to react to various link speeds and delays. The buffer manager 216 may utilize a communications idle duration parameter to determine how long the communications sub-system 210-1 and/or the computing sub-system 230-1 may remain in a lower power state. Since there is no incoming traffic expected during the communications idle duration parameter, the sub-systems 210-1, 230-1 can be power-gated provided there is sufficient time that discrete elements for the sub-system 210-1, 230-1 can do so economically. For example, communications elements such as transceivers 204-1-*r* implemented as wireless transceivers typically require a communications idle duration parameter of at least 8 ms to move to a lower power state. When the communications idle duration parameter is below 8ms, this scenario implies a higher data rate for incoming traffic. Based on this assumption, when the communications idle duration parameter is determined to be less than 8 ms at diamond 404, then the buffers 206-1-*t* are disabled at block 406 to eliminate the additional delay (latency) that the buffers 206-1-*t* might introduce. When the communications idle duration parameter is determined to be greater than 8 ms at diamond 404, however, then the buffer manager 216 may set the variable receive threshold value for the buffers 206-1-*t* and buffer unload timeout value for the buffer timer 218 at block 408.

[0052] The buffer manager 216 may begin receiving packets from one or more of the transceivers 204-1-*r* at block 410, and buffering the received packets in one or more of the buffers 206-1-t at block 412, until one or more of the buffer management conditions become TRUE at diamond 414. In one embodiment, for example, the diamond 414 may evaluate at least 4 conditions, including whether: (1) a first condition (Condition 1) is TRUE based on exceeding a variable receive threshold value; (2) a second condition (Condition 2) is TRUE based on expiration of a buffer unload timeout value; (3) a third condition (Condition 3) is TRUE based on receiving a buffer unload event signal; and (4) a fourth condition (Condition 4) is TRUE based on exceeding an event counter. In the third condition (Condition 3), for example, the buffer manager 216 can utilize various system events (e.g., a transmit interrupt) from the driver, or a DMI link state between the ICH and MCH, as an input to trigger the un-buffering of the packets from a receive buffer 206-1-*t*. For example, when the DMI exits from L1 to L0 due to activities from other devices, it signals to the communications sub-system 210-1 that the host system is already active, and therefore the buffer manager 216

should take advantage of the opportunity to un-buffer the buffered packets from the buffers 206-1-*t* if possible. The fourth condition (Condition 4) may be described in more detail with reference to FIG. 5 as indicated by off page reference 414a.

[0053] When one of the four conditions tested at diamond 414 is TRUE, the buffer manager 216 invalidates the buffer timer 218 (e.g., when armed) at block 416, and triggers the DMI link to exit the lower power state L1 and enter the higher power state L0 at block 418. The buffer manager 216 unbuffers the packets by transferring the packets from the buffers 206-1-*t* to the memory units 234 of the computing sub-system 230-1 using a DMA transfer, and issues an interrupt for the computing sub-system 230-1, at block 420. The buffer manager 216 may optionally modify a communications rate for the transceivers 204-1-*r* to either increase or decrease the rate of incoming packets based on its FIFO size and/or amount of energy remaining at block 422.

[0054] The buffer manager 216 may determine whether more packets have arrived within a stay-awake timer at diamond 424. The buffer manager 216 may keep a timestamp of the last packet. When the timestamp minus the current time is less than a stay-awake timer, then the network is presumed busy. In this case, the buffer manager 216 will continue operations at block 402. When the timestamp minus the current time is more than the stay-awake timer, then the network is presumed idle. In this case, the buffer manager 216 triggers the DMI link to exit the higher power state L0 and enter the lower power state L1 at block 426, and continues operations at block 402.

[0055] Referring again to diamond 414, one of the conditions the buffer manager 216 evaluates may include the fourth condition (Condition 4) sometimes referred to as a "Fail-Safe" trigger. The Fail-Safe trigger is designed to avoid a recurring condition where a small number of packets (or a single packet) remain in a buffer 206-1-*t* until the buffer timer 218 expires. The buffer manager 216 may detect this condition by monitoring how many times a single packet is inside a buffer 206-1-*t* when the buffer timer 218 expires. For example, if this condition happens more than a certain number of times (e.g., 3), then the buffer manager 216 may temporarily disable the buffers 206-1-*t* until a configurable number of resume conditions occur thereby indicating the buffers 206-1-*t* should be enabled or re-enabled. Examples for resume conditions may include: (1) timer-based such as enable buffers 206-1-*t* after a defined time interval (e.g., 10 seconds); and (2) packet-count-based such as enable buffers 206-1-*t* after a defined number of packets have been received (e.g., 4000 packets). An example logic flow to evaluate the fourth condition may be described in more detail with reference to FIG. 5.

[0056] FIG. 5 illustrates a logic flow 500 in accordance with one or more embodiments. The logic flow 500 may be performed by various systems and/or devices and may be implemented as hardware, software, and/or any combination thereof, as desired for a given set of design parameters or performance constraints. For example, the logic flow 500 may be implemented by a logic device (e.g., processor) and/or logic (e.g., instructions, data, and/or code) to be executed by a logic device. For purposes of illustration, and not limitation, the logic flow 500 is described with reference to FIGS. 1-2.

[0057] The logic flow 500 may illustrate various operations for the nodes 110-1-*m* in general, and the managed power system 120 and the power management module 130 in particular. The logic flow 500 may provide an example of a logic flow to evaluate the fourth condition (Condition 4) at block 414 described with reference to FIG. 4 as indicated by the off page reference 414a. To implement the fourth condition (Condition 4), the buffer manager 216 may implement an event counter that counts a number of times a certain event occurs (X). The event may comprise a case where there is only a limited number of packets (e.g. 1) in a buffer 206-1-*t* when the buffer unload timeout value expires. When the event counter counts the occurrence of the event (X) more than an event threshold value (N) (e.g., N = 3), the buffer manager 216 may temporarily disable the buffers 206-1-*t* until the resume conditions are met.

[0058] In one embodiment, for example, the buffer manager 216 may implement a packet counter to count a number of packets in a buffer 506-1-*t* (M), and set the buffer timer 218 with a buffer disable timeout value (B). As shown in FIG. 5, when M is not equal to a packet threshold value (e.g., M > 1) at diamond 502, then the buffer manager 216 resets an event counter (e.g., X = 0) at block 514 and passes control to block 416 of the logic flow 400. When M is equal to a packet threshold value (e.g., M = 1) at diamond 502, however, then the buffer manager 216 increments the event counter by one (e.g., X = X + 1) at block 504. The buffer manager 216 may determine whether the event counter (X) is greater than or equal to the event threshold value (e.g., N = 3) at diamond 506. When FALSE at diamond 506, the buffer manager 216 restarts at block 502. When TRUE at diamond 506, the buffer manager 216 disables the buffers 206-1-*t* at block 508. The buffer manager 216 then determines if a resume condition occurs, such as the buffer timer 218 is greater than the buffer disable timeout value (e.g., timer > L seconds) or the number of packets received since the buffers 206-1-*t* were disabled is greater than packet threshold value (e.g., P > 4000 packets). When both of the resume conditions are FALSE, then control is passed back to block 508. When either of the resume conditions is TRUE, however, then the buffer manager 216 enables the

buffers 206-1-*t* at block 510, and passes control to block 416 of the logic flow 400. It is worthy to note that the values for M, N, L and P are configurable values.

[0059] The various embodiments may provide several advantages for multiple use scenarios and applications. In one embodiment, for example, the buffer manager 216 and the buffers 206-1-*t* may be used to allow the computing sub-system 230-1 to remain in a lower power state, thereby increasing energy conservation. In one embodiment, for example, approximately 500 milliwatts (mW) to 2 Watts (W) of power savings may be achieved for active communications scenarios.

[0060] In some cases, various embodiments may be implemented as an article of manufacture. The article of manufacture may include a computer-readable medium or storage medium arranged to store logic and/or data for performing various operations of one or more embodiments. Examples of computer-readable media or storage media may include, without limitation, those examples as previously described. In various embodiments, for example, the article of manufacture may comprise a magnetic disk, optical disk, flash memory or firmware containing computer program instructions suitable for execution by a general purpose processor or application specific processor. The embodiments, however, are not limited in this context.

[0061] Various embodiments may be implemented using hardware elements, software elements, or a combination of both. Examples of hardware elements may include any of the examples as previously provided for a logic device, and further including microprocessors, circuits, circuit elements (e.g., transistors, resistors, capacitors, inductors, and so forth), integrated circuits, logic gates, registers, semiconductor device, chips, microchips, chip sets, and so forth. Examples of software elements may include software components, programs, applications, computer programs, application programs, system programs, machine programs, operating system software, middleware, firmware, software modules, routines, subroutines, functions, methods, procedures, software interfaces, application program interfaces (API), instruction sets, computing code, computer code, code segments, computer code segments, words, values, symbols, or any combination thereof. Determining whether an embodiment is implemented using hardware elements and/or software elements may vary in accordance with any number of factors, such as desired computational rate, power levels, heat tolerances, processing cycle budget, input data rates, output data rates, memory resources, data bus speeds and other design or performance constraints, as desired for a given implementation.

[0062] Some embodiments may be described using the expression "coupled" and "connected" along with their derivatives. These terms are not necessarily intended as

synonyms for each other. For example, some embodiments may be described using the terms "connected" and/or "coupled" to indicate that two or more elements are in direct physical or electrical contact with each other. The term "coupled," however, may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

[0063] It is emphasized that the Abstract of the Disclosure is provided to comply with 37 C.F.R. Section 1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment. In the appended claims, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein," respectively. Moreover, the terms "first," "second," "third," and so forth, are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0064] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims. Examples of what could be claimed include the following:

CLAIMS

1. An apparatus, comprising:

a power management module having a power management controller;

a managed power system to couple to the power management module, the managed power system comprising a communications sub-system and a computing sub-system, the power management controller to switch the communications sub-system and the computing sub-system to a lower power state to conserve energy, the communications sub-system having:

a transceiver;

a buffer to couple to the transceiver, the buffer to store packets of information for the transceiver during a communications idle duration period to create a computing idle duration period;

a watermark generator to couple to the buffer, the watermark generator operative to generate a variable receive threshold value; and

a buffer manager to couple to the buffer and the watermark generator, the buffer manager operative to transfer the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value.

2. The apparatus of claim 1, the buffer manager operative to transfer the stored packets of information from the buffer to the computing sub-system when a number of packets of information stored by the buffer exceeds a variable receive threshold value.

3. The apparatus of claim 1, the watermark generator operative to generate the variable receive threshold value based on a receive data rate parameter, a buffer size parameter and a communications resume latency parameter.

4. The apparatus of claim 1, the buffer manager operative to disable the buffer to prevent the buffer from storing the packets of information when a communications idle duration parameter is lower than a communications idle duration threshold value.

5. The apparatus of claim 1, comprising a buffer timer to couple to the buffer manager, the buffer timer set with a buffer unload timeout value, the buffer manager operative to transfer the stored packets of information from the buffer to the computing sub-system when the buffer unload timeout value expires before a number of packets stored by the buffer exceeds the variable receive threshold value.

6. The apparatus of claim 1, the buffer manager operative to receive a buffer unload event signal before a number of packets stored by the buffer exceeds the variable threshold

value, and transfer the stored packets of information from the buffer to the computing sub-system in response to the buffer unload event signal.

7. The apparatus of claim 1, comprising a controller to couple to the transceiver, the buffer manager operative to send a request to adjust a communications rate for the transceiver based on a buffer size parameter.

8. The apparatus of claim 1, comprising controller to couple to the transceiver, the buffer manager operative to receive a power management message with an energy measurement parameter from the power management controller, and send a request to adjust a communications rate for the transceiver based on the energy measurement parameter.

9. A method, comprising:

modifying a power state for a communications sub-system and a computing sub-system from a higher power state to a lower power state;

storing packets of information in a buffer for the communications sub-system during a communications idle duration period to create a computing idle duration period;

generating a variable receive threshold value for the buffer; and

transferring the stored packets of information from the buffer to the computing sub-system based on a variable receive threshold value.

10. The method of claim 9, comprising transferring the stored packets of information from the buffer to the computing sub-system when a number of packets of information stored by the buffer is greater than a variable receive threshold value.

11. The method of claim 9, comprising generating the variable receive threshold value based on a receive data rate parameter, a buffer size parameter and a communications resume latency parameter.

12. The method of claim 9, comprising disabling the buffer to prevent the buffer from storing the packets of information when the communications idle duration parameter is lower than a communications idle duration threshold value.

13. The method of claim 9, comprising transferring the stored packets of information from the buffer to the computing sub-system when a buffer unload timeout value expires before a number of packets stored by the buffer exceeds the variable receive threshold value.

14. The method of claim 9, comprising transferring the stored packets of information from the buffer to the computing sub-system when a buffer unload event signal is received before a number of packets stored by the buffer exceeds the variable threshold value.

15. The method of claim 9, comprising a set of computer-readable program elements operative to configure a system to implement the method of claim 9.

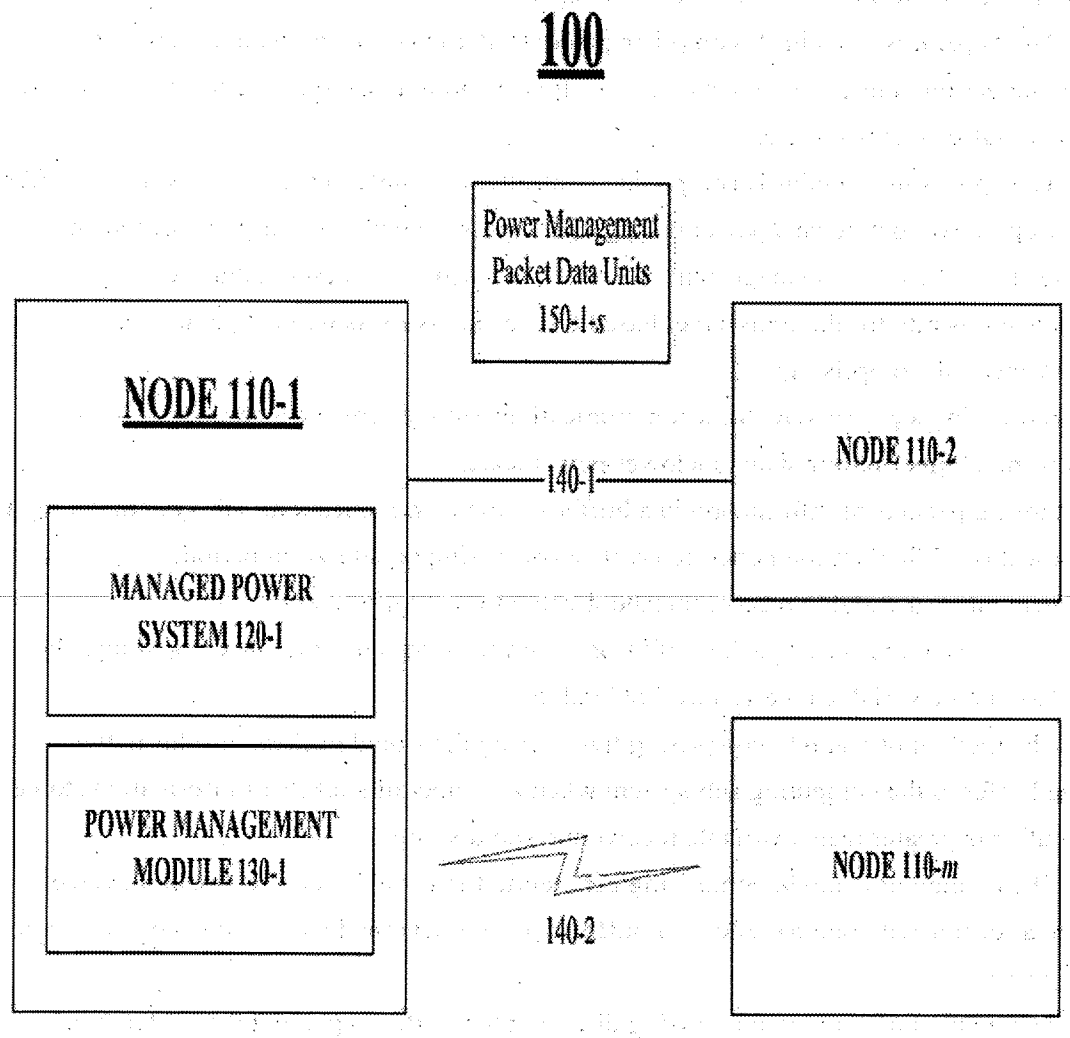

100
Power Management Packet Data Units 150-1-s
NODE 110-1
MANAGED POWER SYSTEM 120-1
POWER MANAGEMENT MODULE 130-1
140-1
NODE 110-2
140-2
NODE 110-m

FIG. 1

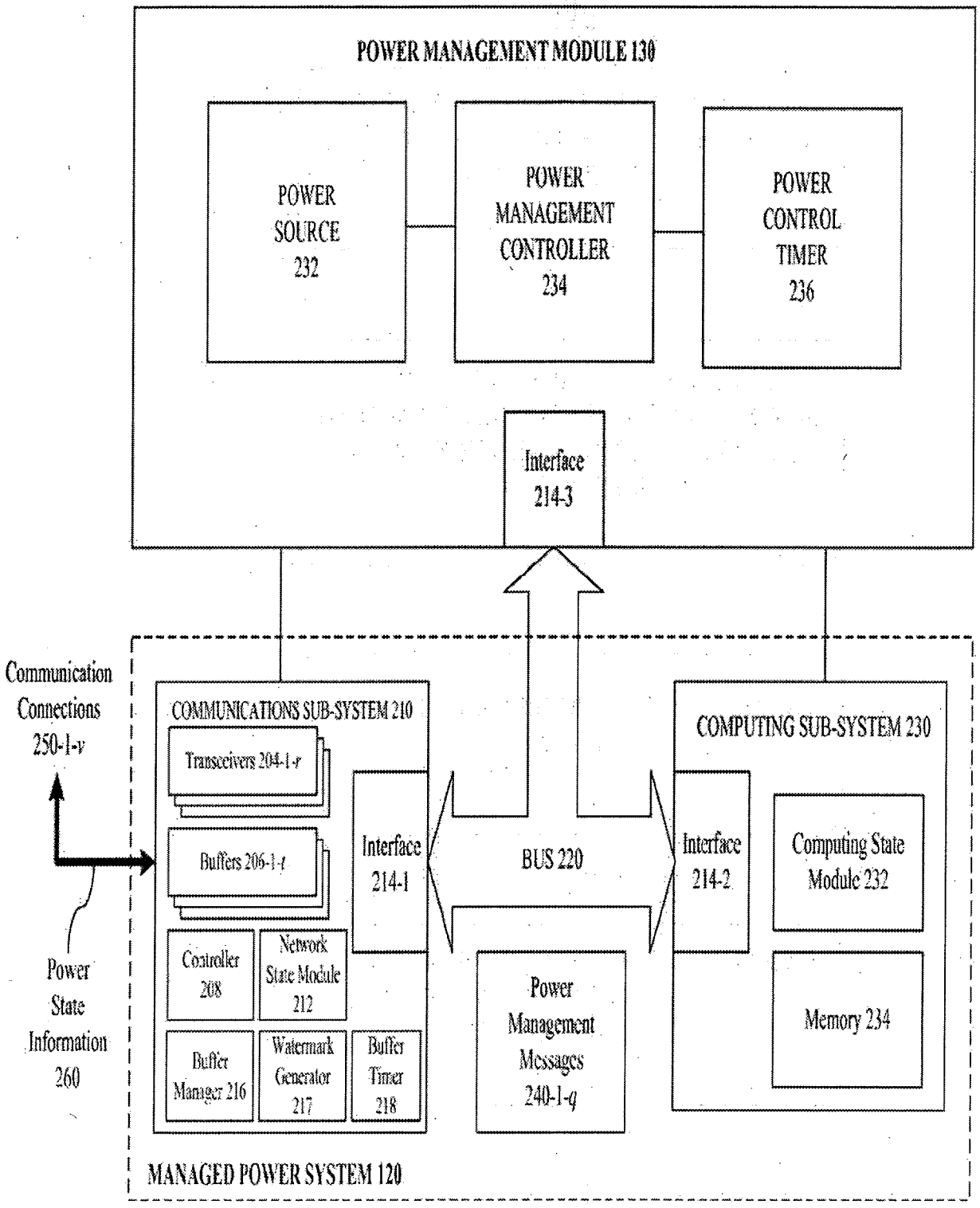

POWER MANAGEMENT MODULE 130
POWER SOURCE 232
POWER MANAGEMENT CONTROLLER 234
POWER CONTROL TIMER 236
Interface 214-3
Communication Connections 250-1-v
Power State Information 260
COMMUNICATIONS SUB-SYSTEM 210
Transceivers 204-1-r
Buffers 206-1-t
Controller 208
Network State Module 212
Buffer Manager 216
Watermark Generator 217
Buffer Timer 218
Interface 214-1
BUS 220
Power Management Messages 240-1-q
COMPUTING SUB-SYSTEM 230
Interface 214-2
Computing State Module 232
Memory 234
MANAGED POWER SYSTEM 120

FIG. 2

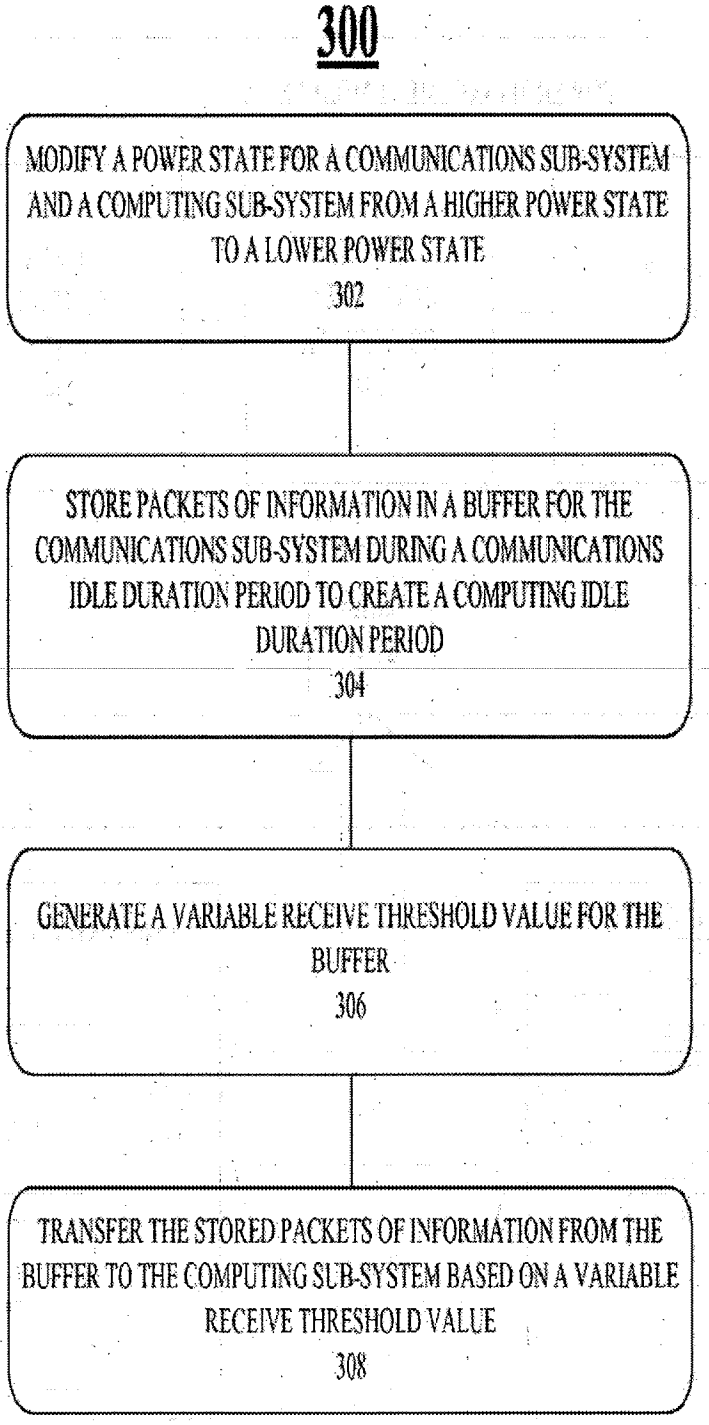

300
MODIFY A POWER STATE FOR A COMMUNICATIONS SUB-SYSTEM AND A COMPUTING SUB-SYSTEM FROM A HIGHER POWER STATE TO A LOWER POWER STATE
302
STORE PACKETS OF INFORMATION IN A BUFFER FOR THE COMMUNICATIONS SUB-SYSTEM DURING A COMMUNICATIONS IDLE DURATION PERIOD TO CREATE A COMPUTING IDLE DURATION PERIOD
304
GENERATE A VARIABLE RECEIVE THRESHOLD VALUE FOR THE BUFFER
306
TRANSFER THE STORED PACKETS OF INFORMATION FROM THE BUFFER TO THE COMPUTING SUB-SYSTEM BASED ON A VARIABLE RECEIVE THRESHOLD VALUE
308

FIG. 3

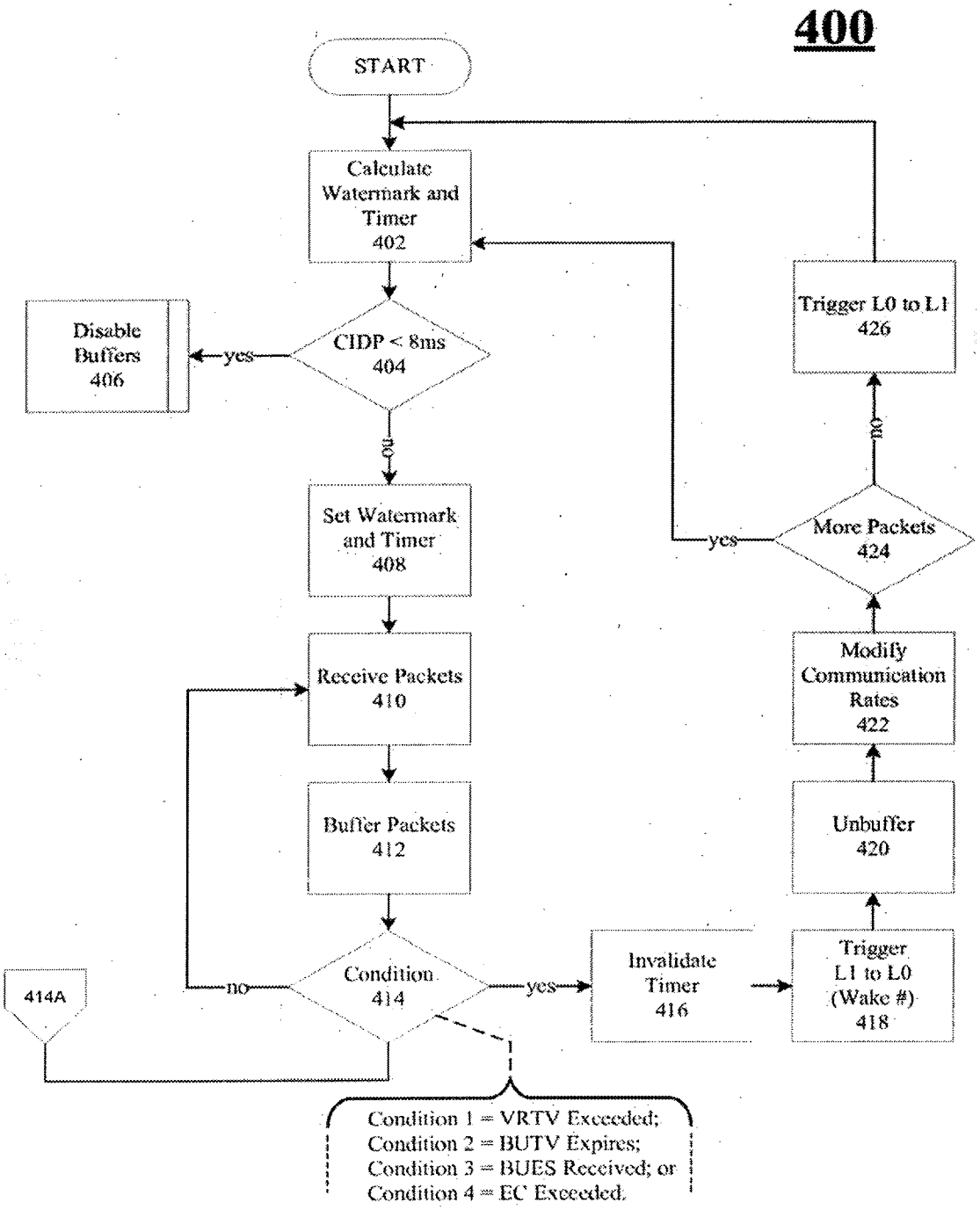

400
START
Calculate Watermark and Timer 402
Disable Buffers 406
yes
CIDP < 8ms 404
no
Set Watermark and Timer 408
Receive Packets 410
Buffer Packets 412
414A
no
Condition 414
yes
Invalidate Timer 416
Trigger L1 to L0 (Wake #) 418
Unbuffer 420
Modify Communication Rates 422
More Packets 424
yes
no
Trigger L0 to L1 426
Condition 1 = VRTV Exceeded;
Condition 2 = BUTV Expires;
Condition 3 = BUES Received; or
Condition 4 = EC Exceeded.

FIG. 4

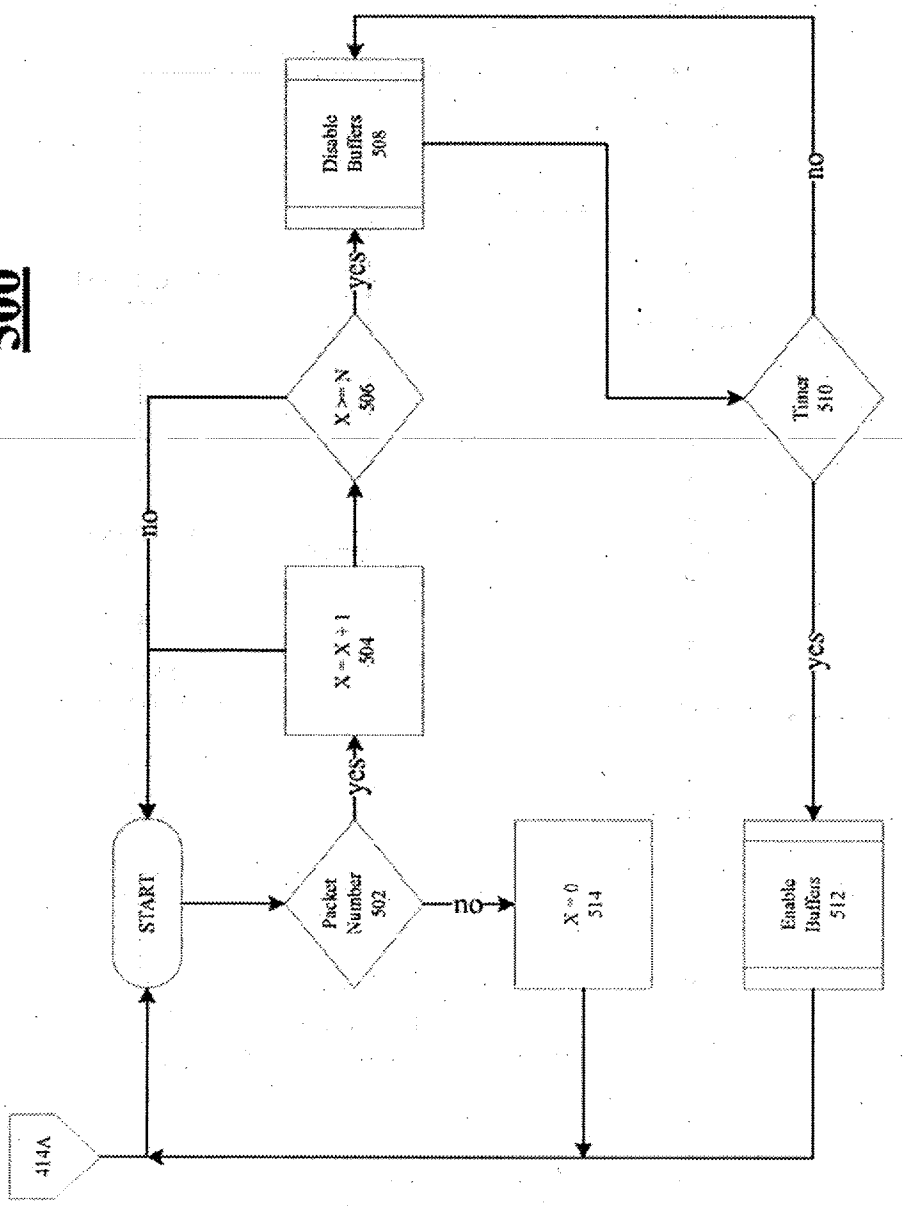

500
START
Packet Number 502
yes
no
X = X + 1 504
X >= N 506
yes
no
Disable Buffers 508
Timer 510
yes
no
Enable Buffers 512
X = 0 514
414A

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/076135

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/32(2006.01)i, H04B 3/54(2006.01)i, G06G 7/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC G06F, G08C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO internal), IEEExplore : "power", "state","change, transit", "computing", "packet"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/0264396 A (BORIS GINZBURG et al.) 30 December 2004 See the abstract, paragraphs [0007] - [0025], and figures 1-3.	1-15
A	US 6865653 B2 (ANDRE ZACCARIN et al.) 8 March 2005 See the abstract, column 3, line 9 - line 23, and figure 2.	1-15
A	US 2003-0131273 A1 (LA VAUGHN F. WATTS JR et al.) 10 July 2003 See the abstract, figure 2, and related explanations.	1-15
A	US 6311081 B1 (JOHN NORTHCUTT et al.) 30 October 2001 See the abstract, figure 7 and related explanations.	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/KR
Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
HWANG, Yun Koo
Telephone No. 82-42-481-5788

Form PCT/ISA/210 (second sheet) (July 2008)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2008/076135

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 6311081 B1	30.10.2001	AU 2000-67969 A1	17.04.2001
		WO 01-20790 A1	22.03.2001

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(72) Inventors; and

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: APPARATUS, COMMUNICATIONS SYSTEM AND METHOD FOR OPTIMIZING DATA PACKET FLOW

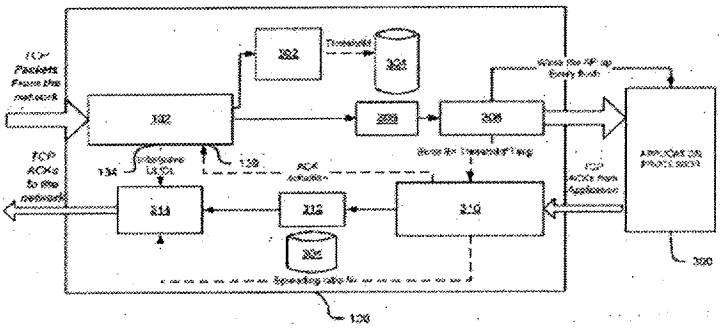


Fig. 3

(57) Abstract: A datagram flow optimizer apparatus (100) comprises a buffer resource (306, 312) capable of receiving and temporarily storing a plurality of datagrams in respect of a forward path. The apparatus (100) also comprises and a buffer controller (102, 308) arranged to implement, when in use, buffering of received datagrams by the buffer resource (306) until a predetermined threshold number of datagrams has been stored by the buffer resource (306). The apparatus (100) further comprises an acknowledgement regulator (124, 310, 312, 314) arranged to use the buffer resource (312) to manipulate temporal spacing between acknowledgements of datagrams on a reverse path. The buffer controller (102, 308) is arranged to permit forwarding on the forward path of datagrams stored by the buffer resource (306) in response to the predetermined threshold number of stored datagrams being reached.

WO 2010/125429 A1

APPARATUS, COMMUNICATIONS SYSTEM AND METHOD FOR OPTIMIZING DATA PACKET FLOW

Description

Field of the invention

This invention relates to a datagram flow optimizer apparatus of the type that, for example, is located between a source of datagrams and a destination for the datagrams and modifies a flow of the datagrams between the source and the destination. The present invention also relates to a communications system of the type that, for example, communicates datagrams between a source of datagrams and a destination for the datagrams. The present invention further relates to a method of optimizing datagram flow, the method being of the type that, for example, communicates datagrams from a source of the datagrams to a destination for the datagrams.

Background of the invention

In the field of communications, particularly but not exclusively wireless communications, it is known to communicate data in datagrams, the datagrams traversing a communications network from a source node to a destination node or a communications fabric between the source node and the destination node. In order to ensure reliable communication of the datagrams between the source node and the destination node, a so-called flow control protocol is employed. The flow control protocol is usually one of a number of protocols employed in a communications system between the source and destination nodes. In this respect, an Open Systems Interconnection model is a common reference model for a so-called protocol stack employed at the source and destination nodes. In relation to flow control, a common protocol employed is a Transmission Control Protocol (TCP), which is one of the core protocols of an Internet Protocol suite. The TCP is defined over a number of Requests for Comments (RFCs) available from the Internet Engineering Task Force (IETF). One aspect of the TCP is congestion avoidance as defined in RFC 2581.

Electronic devices, for example portable communications devices, comprise so-called "application processors" that receive the datagrams, for example TCP segments, and confirm receipt of the TCP segments by sending acknowledgement messages (ACKs) respectively in reply to the receipt of the TCP segments in order to confirm receipt thereof. Furthermore, the electronic devices are usually powered by portable power sources, for example rechargeable cells, the capacity or remaining charge of which needs to be conserved as much as possible to enable the electronic device to operate for as long a period of time as possible. The application processor therefore usually implements a number of power conservation measures in the form of modes of operation that consume varying amounts of electrical power, for example: a Wait or Doze mode, a Stop mode and/or a Sleep Mode. In some circumstances, the provision of the sleep mode in respect of the application processor enables the electronic device to enter a so-called "Deep Sleep Mode", whereby the electronic device can conserve energy.

In one known scenario, a processing resource within a communications network, for example a in a Node B of a Universal Mobile Telecommunications System (UMTS) Terrestrial Radio Access Network (UTRAN), receives TCP segments from a source node attached or coupled to the Internet at a rate of receipt. The TCP segments are addressed to a destination node associated with the application processor of the electronic device. In this example, the electronic device is a User Equipment (UE) unit of a UMTS communications network. The Node B is therefore used to transmit the TCP segments to the UE over a Radio Frequency (RF) interface of the TCP segments by the UTRAN. At the UE unit, a modem processor of the UE unit receives the TCP segments at a rate corresponding to the rate of receipt. The modem processor communicates the received TCP segments to the application processor of the UE at a corresponding rate of receipt.

Referring back to the power saving features of the application processor, in order to be able to enter the Sleep Mode and therefore conserve maximum electrical power, a sufficient amount of time has to elapse during which data is not received by the application processor before the Sleep Mode can be entered by the application processor. If TCP segments are being received at a sufficiently fast rate that the application processor does not remain idle for the necessary amount of time required for the Sleep Mode to be entered, the application processor simply transitions between the lesser power conserving Wait and Stop modes. Consequently, the application processor does not get an opportunity to enter the sleep mode and less power is conserved by the UE and hence battery life is reduced.

Additionally, repeated interruption of the application processor in order to process TCP segments and transmit ACKs back to the source node via the modem processor consumes Millions of Cycles Per Second (MCPS) of the application processor. As the application processor is only capable of supporting a finite number of MCPS, consumption of the MCPS in relation to generation of ACKs and processing of received TCP segments results in a corresponding reduction in the available MCPS for other applications, for example: video telephony, Internet browsing and/or voice switched telephony. Consequently, if insufficient MCPS are available, data throughput in respect of receipt of TCP segments is reduced. Additionally, the quality of one or more of the applications being supported by the application processor will have to be downgraded in order for sufficient MCPS to be available to support all applications running.

In order to reduce transmission of ACKs and hence attempt to improve performance efficiency, it is known to employ various ACK filtering techniques, for example as described in US 6,078,564 and US 6,458,108. However, such techniques sacrifice the Quality of Service (QoS) associated with communication of the TCP segments when multiple streams of data are employed. Furthermore, filtering of the ACKs consumes MCPS, because the application processor has to "read into" the TCP ACKs. As filtering of ACKs can only be supported correctly using "byte counting", implementation of ACK counting in TCP stacks reduce data throughput in the communications network. Also, ACK filtering creates bursts of ACKs that reduces throughput. Consequently, RFC specifications do not recommend use of ACK filtering except in cases of asynchronous communications links. Additionally, ACK filtering does not work with the IPSEC

suite of protocols for securing Internet Protocol (IP), and when the so-called "SACK" option is employed, as in 2.5G, 3G, 3.5G and Wireless Local Area Network standards.

Summary of the invention

The present invention provides a datagram flow optimizer apparatus as described in the accompanying claims.

The present invention provides an integrated circuit as described in the accompanying claims.

The present invention provides a communications system as described in the accompanying claims.

The present invention provides a method of optimizing datagram flow as described in the accompanying claims.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

Figure 1 is a schematic diagram of a datagram flow optimizer apparatus in overview constituting an embodiment of the invention;

Figure 2 is a schematic diagram of a flow control mode detector for the apparatus of Figure 1;

Figure 3 is a schematic diagram of the apparatus of Figure 1 in greater detail;

Figure 4 is a schematic diagram of an alternative implementation to the apparatus of Figure 3 and constituting another embodiment of the invention;

Figure 5 is a schematic diagram of data being communicated by a system comprising any of the apparatus of Figures 1, 3 or 4;

Figures 6 to 9 are flow diagrams of respective parts of a method of optimizing datagram flow in respect of the apparatus of any of Figures 1, 3 or 4;

Figures 10A and 10B are schematic diagrams of another system configuration comprising the apparatus of any of Figures 1, 3 or 4;

Figure 11 is a schematic diagram of a further communications system comprising the apparatus of any of Figures 1, 3 or 4 and that can be implemented in respect of different communications networks; and

Figure 12 is a schematic diagram of an embedded communications system comprising the apparatus of any of Figures 1, 3 or 4.

Detailed description of the preferred embodiments

Throughout the following description, identical reference numerals will be used to identify like parts.

Referring to Figure 1, a datagram flow optimizer apparatus 100 may comprise a flow control mode detector 102 having a first input 104 coupled to a first input path of communications circuitry (not shown) for receiving data from a source node 106. A first output 108 of the flow control mode detector 102 may be coupled to a first output path of the communications circuitry for sending data to a destination node 110. A second output 112 of the flow control mode detector 102 is coupled to an input 114 of a datagram scheduler 116, a first output 118 of the datagram scheduler 116 also being coupled to the first output path of the communications circuitry. A second output 120 of the datagram scheduler 116 is coupled to a first input 122 of an acknowledgement regulator 124. A second input 126 of the acknowledgement regulator 124 is coupled to a second input path of the communications circuitry for receiving data from the destination node 110. A first output 128 of the acknowledgement regulator 124 is coupled to a second input 130 of the flow control mode detector 102. An interleaving port 132 of the acknowledgement regulator 124 is coupled to a corresponding interleaving port 134 of the flow control mode detector 102. A second output 136 of the acknowledgement regulator 124 is coupled to a second output path of the communications circuitry for communication of data to the source node 106.

From references herein to the first and second input paths and the first and second output paths, the skilled person should readily appreciate that the datagram flow optimizer apparatus 100 can be disposed in or integrally formed with any suitable communications circuitry as will be described in greater detail later herein. In this respect, the datagram flow optimizer apparatus 100 can be implemented in a network protocol stack associated with, for example, over-the-air communications, such as comprising protocols relating to Layers 1, 2 and 3 of the OSI model.

Referring to Fig. 2, the flow control mode detector 102 may comprise a data size measurement module 200 coupled to a combinatorial logic module 202, an inter-arrival time measurement module 204 coupled to the combinatorial logic module 202, and an acknowledgement detector module 206 also coupled to the combinatorial logic module 202. The combinatorial logic module 202 also has a mode detect output 208.

Referring to Fig. 3, in one example implementation where datagrams are communicated from a modem processor, comprising the datagram flow optimizer apparatus 100 to an application processor 300 of the destination node, for example a User Equipment (UE) unit of a UMTS communications network (not shown), the flow control mode detector 102 may also be coupled to a threshold control module 302 that is capable of accessing a data store 304 where a variable can be stored relating to a buffer threshold. In this example, the datagram scheduler 116 of Fig. 1 comprises a forward queue 306, constituting a buffer resource, coupled to a queue flushing module 308. Together, the flow control mode detector 102 and the queue flushing module 308 serve to control the forward queue 306. The acknowledgement regulator 124 of Fig. 1 may comprise, in this example, a spread measurement module 310, the spread measurement module 310 being coupled to the first output 128 of the acknowledgement regulator 124 and hence the second input 130 of the flow mode control detector 102. The spread measurement module 310 is capable of accessing

the data store 304 in order to store another variable, relating to a spreading ratio, N, and is also coupled to the second input path of the communications circuitry and a reverse queue 312, which can be part of the buffer resource, the reverse queue 312 being coupled to an acknowledgement release module 314. The acknowledgement release module 314 is coupled to the interleaving port 132 of the acknowledgement regulator 124 and hence the corresponding interleaving port 134 of the flow control mode detector 102. The acknowledgement release module 314 is coupled to the second output path of the communications circuitry, and also has access to the data store 304 where the another variable relating to the spreading ratio, N, is stored. Hence, it can be seen that the acknowledgement regulator 124 may comprise the spread measurement module 310, the reverse queue 312 and the acknowledgement release module 314.

Turning to Fig. 4, in an alternative example, the queue flushing module 308 is coupled to a reverse path frequency measurement module 400 in place of the spread measurement module 310, the reverse path frequency measurement module 400 being coupled to the reverse queue 312. Whilst the reverse queue 312 is still coupled to the acknowledgement release module 314, the coupling is via a bit rate extraction module 402. Hence, in this example, the acknowledgement regulator 124 may comprise the reverse path frequency measurement module 400, the reverse queue 312, the bit rate extraction module 402 and the acknowledgement release module 314.

Operation of the datagram flow optimizer apparatus 100 will now be described in the context of the source node 106 being coupled to the Internet via an Internet Service Provider (ISP) and capable of communicating with the application processor 300 of the UE unit mentioned above.

In operation (Figure 5), the datagram flow optimizer apparatus 100 is supported by a modem processor 500 of the UE unit. The datagram flow optimizer apparatus 100 may receive TCP segments from the source node 106 on a forward path and at a forward path rate, f_{dlink}. Referring to Figure 6, at the datagram flow optimizer apparatus 100, the flow control mode detector 102 via the threshold control module 302, may set (Step 600) an initial buffer size threshold value, for example to a value that corresponds to at least about 5 TCP segments, which is incrementally increased with time, as will be described later herein. The buffer size may be increased to more than about 10 TCP segments, for example a value less than about 50 TCP segments, such as about 20 TCP segments. In this respect, the threshold control module 302 can be configured to receive an advertised window size obtained from an ACK message or pre-stored in relation to operation of an operating system, and to incrementally increase the buffer size threshold up to a proportion of the advertised window size. In this example, the proportion of the advertised window size is about half the advertised window size. The advertised window size can be a value that is less than or equal to a maximum window size. The flow control mode detector 102 receives the TCP segments sent on the forward path from the source node 106.

Using the data size measurement module 200, the flow control mode detector 102 measures the size of TCP segments received during a predetermined period of time from a Node B of a UTRAN of the UMTS network and via the RF interface thereof. Also, using the inter-arrival time measurement module 204, the flow control mode detector 102 also measures the inter-arrival time between TCP segments received over the predetermined period of time. In response to receipt of

a substantially constant TCP segment size being detected, the data size measurement module 200 generates a logic HIGH signal. Similarly, in response to receipt of a substantially constant inter-arrival time between TCP segments, the inter-arrival time measurement module 204 also generates a logic HIGH signal. Additionally, the acknowledgement detector module 206 determines if acknowledgement messages (ACKs) are being received from the application processor 300 in response to the TCP segments sent by the source node 106. In the event that ACKs are being received, the acknowledgement detector mode 206 also generates a logic HIGH signal. Receipt of ACKs is communicated by the acknowledgement regulator 124, for example by the spread measurement module 310 (Fig. 3) or the reverse path frequency measurement module 400 (Fig. 4).

When logic HIGH signals are received from the data size measurement module 200, the inter-arrival time measurement module 204 and the acknowledgement detector module 206, the combinatorial logic module 202, in this example an AND logic gate having three inputs, generates a logic HIGH output signal.

The detection of TCP segments of constant size and having a constant inter-arrival time, and the detection of the presence of ACKs on the reverse path sent by the application processor 300 are, together, indicative that the TCP implemented in the respective protocol stacks of the source node 106 and the applications processor 300, is in a steady state, for example a congestion avoidance phase. Hence, the flow control mode detector 102 determines (Step 602) whether the communication of TCP segments between the source node 106 and the application processor 300 is in the congestion avoidance phase. The congestion avoidance phase is an example of a delay tolerant flow control mode.

If the congestion avoidance phase is not detected, for example if the TCP is currently in the so-called "slow start" phase, a QoS conversational situation exists, for example to support Voice over IP (VoIP) communications, a streaming situation exists requiring a constant packet inter-arrival time, or any other latency intolerant phase or situation, the flow control mode detector 102 is set (Step 604) to a passthrough mode and TCP segments received from the source node 106 are simply communicated to the application processor 300 without buffering. However, in the event that the flow control mode detector 102 determines that the TCP is in the congestion avoidance phase, then the TCP segments received are passed (Step 606) to the forward queue 306 for buffering. Thereafter, using the buffer size threshold value stored by the data store, the queue flushing module 308 monitors (Step 608) the size of the forward queue 306 in order to determine whether the forward queue size has exceeded the buffer size threshold value. In the event that the buffer size threshold value has not been exceeded, the forward queue 306 continues to fill with TCP segments directed thereto by the flow control mode detector 102.

Once the buffer size threshold value has been reached, the queue flushing module 308 empties (Step 610) the forward queue 306 by "releasing" the TCP segments stored by the forward queue for communication on the forward path to the application processor 300 by the UTRAN as a "burst" of TCP segments 502 (Fig. 5). Thereafter, the threshold control module 302 determines (Step 612) whether the buffer size threshold value should be incrementally increased, for example

if the proportion of the advertised window size has not been reached, and if the buffer size threshold value can be increased, the threshold control module 302 increases (Step 614) the buffer size threshold value, by a predetermined increment size, for example 1 segment, 2 segments, 5 segments, or more. The incremental increase of the buffer size threshold value prevents unnecessary triggering of the retransmission timeout in respect of the source node 106. In another embodiment, it can be desirable to reduce the buffer size threshold value, for example where the buffer size threshold value is interfering with the congestion avoidance mode.

Once the forward queue 306 has been flushed and the buffer size threshold value considered and/or set, the above-described process (Steps 602 to 614) are repeated.

At the application processor 300, the application processor 300 is in a sleep mode prior to receipt of the burst of TCP segments via the UTRAN. However, upon receipt of the burst of TCP segments, the application processor 300 receives an interrupt and awakens from the sleep mode and processes the TCP segments received and, in accordance with the TCP, the application processor 300 generates ACKs for communication using the RF circuitry of the UE unit to the Node B (not shown). Consequently, a burst of ACKs 504 is received by the datagram flow optimizer apparatus 100 from the application processor 300.

In order to avoid bursty reverse path traffic between the datagram flow optimizer apparatus 100 and the source node 106, and hence a reduction in throughput of network traffic traversing the UMTS, the acknowledgement regulator 124 serves to "even out" spacings between ACKs received by the datagram flow optimizer apparatus 100 as bursts of ACKs by manipulating temporal spacing between ACKs on the reverse path. Hence, by maintaining a constant uplink data rate, the network maintains an optimal downlink data rate, thereby avoiding so-called network "under-run" that can lead to asynchronism between forward and reverse paths and hence a reduction in bandwidth on the downlink.

Two different arrangements for the acknowledgement regulator 124 are set out above. Operation of each of the arrangements of Figs. 3 and 4 will therefore now be described separately.

Turning to Figs. 3 and 7, the spread measurement module 310, using data generated by the flow control mode detector 102, measures (Step 620) an average forward path TCP segment arrival rate, f_{ave_dlink}, over a predetermined period of time exceeding the time required to receive the TCP segments that fill the forward queue 306. In this respect, the sample size for calculation of the average forward path arrival rate, f_{ave_dlink}, can exceed the buffer size threshold value. The duration of the predetermined period of time can depend upon the radio access technology employed, for example about 200ms for High-Speed Downlink Packet Access (HSDPA). Similarly, the spread measurement module 310 monitors ACKs received from the application processor 300 and measures (Step 622) an average reverse path ACK arrival rate, f_{ave_ulink} in respect of a period of time exceeding the time required to transmit the contents of the reverse queue 312. In this respect, the sample size for calculation of the average reverse path arrival rate, f_{ave_ulink}, can exceed the buffer size threshold value. Thereafter, the spread measurement module 310 calculates (Step 624) a ratio of the measured average forward path arrival rate, f_{ave_dlink}, to the measured average reverse path arrival rate, f_{ave_ulink}, the ratio constituting a so-called spreading ratio, N. The

spreading ratio, N, is then stored (Step 626) in the data store 304. In this respect, the skilled person should appreciate that a given TCP policy employed by a receiver of TCP segments does not usually require generation and sending of an ACK for each TCP segment received, but rather one ACK in respect of a number of received TCP segments.

Referring to Fig. 8, the spread measurement module 310 also awaits (Step 640) receipt of bursts of ACKs sent by the application processor 300. Upon detection of receipt of one or more ACKs, the spread measurement module 310 stores (Step 642) the received ACK(s) in the reverse queue 312.

The acknowledgement release module 314 (Figure 9) accesses (Step 660) the spreading ratio, N, from the data store 304. The flow control mode detector 102 provides a clock signal via the interleaving port 134 thereof to indicate when a TCP segment has been received. Using the clocking signal generated by the flow control mode detector 102, the acknowledgement release module 314 determines (Step 662) whether a sufficient number of TCP segments have been received in order to merit sending an ACK from the reverse queue 312 in order to comply with the spreading ratio, for example 1 ACK for every 3 TCP segments.

Once a sufficient number of TCP segments have been received, the acknowledgement release module 314 sends (Step 664) an ACK using the RF circuitry of the UE unit to the node B for onward transit to the source node 106. Consequently, ACKs received from the application processor 300 in bursts, as a result of the TCP segments being sent by the datagram flow optimizer apparatus 100 to the application processor 300 in bursts in order to provide further opportunities for the application processor 300 to enter a deep sleep mode, are spread out 506 on the reverse path according to the spreading ratio, N, so as to be interleaved with the TCP segments transmitted on the forward path between the source node 106 and the datagram flow optimizer apparatus 100.

In the embodiment of Fig. 4, instead of calculation and use of the spreading ratio, N, mentioned above, the reverse path frequency measurement module 400 measures a frequency of ACKs sent as a burst by the application processor 300 over a predetermined period of time, for example exceeding the time required to transmit the contents of the reverse queue 312. The duration of the predetermined period of time again can depend upon the radio access technology employed, for example about 200ms for High-Speed Downlink Packet Access (HSDPA),and stores the calculated frequency of ACKs, f_{ACK}, in the data store 304. Thereafter (Fig. 10), the bit rate extraction module 402 accesses the ACK frequency, f_{ACK}, and empties the reverse queue 312 at the frequency / bit rate retrieved, f_{ACK}. The bit rate extraction module 402 also received a system clock signal that, in combination with the ACK frequency, f_{ACK}, enables the ACKs to be passed to the acknowledgement release module 314 for sending the ACK. Again, the ACKs received in bursts from the application processor 300 are spread out 506 on the reverse path.

In another embodiment, the datagram flow optimizer apparatus 100 can be located in a network protocol stack of an intermediate node, for example a Node B of a UTRAN of the UMTS network. The datagram flow optimizer apparatus 100 can alternatively be supported in a network protocol stack of the UTRAN. In any event, the datagram flow optimizer apparatus 100 behaves in

a like manner to that described above in the context of the modem processor 500. However, the data is exchanged between the application processor 300 of the UE unit and the datagram flow optimizer apparatus 100 via an RF interface.

Referring to Figures 10A and 10B, the UTRAN described above can be optimised in order to ensure optimum use is made of bandwidth that is unused by an application processor whilst in the deep sleep mode. In this respect, a first UE unit 700, a second UE unit 702 and a third UE unit 704 may each be capable of communicating with a UTRAN 706 via an RF interface. In this example, the first UE unit 700 constitutes the destination node mentioned above, and the second and third UE units 702, 704 constitute other destination nodes. As the UTRAN 706 is part of a UMTS network, the UTRAN is coupled to a gateway 708 to a core IP network (not shown). In this example, the datagram flow optimizer apparatus 100 of the UTRAN may employ a separate queue for each of the UEs. When the datagram flow optimizer apparatus 100 is buffering incoming TCP segments destined for the first UE unit 700, the first UE unit 700 is in a FACH or RACH mode and hence in a deep sleep mode, and the 2 Mbps bandwidth allocated to the first UE unit 700 is reallocated to the second and third UE units 702, 704 so that the second and third UE units 702, 704 each enjoy 3 Mbps of bandwidth each as opposed to 2Mbps.

Subsequently, the datagram flow optimizer apparatus 100 starts forwarding the buffered TCP segments to the first UE unit 700, but starts buffering TCP segments received and destined for the second UE unit 702. Consequently, in accordance with the above-described policy, the bandwidth allocated for the second UE unit 702 is reallocated to the first and third UE units 700, 704. Hence, UE units that are not receiving TCP segments can enter into a Deep Sleep Mode (DSM).

This pattern of behaviour can be continued in respect of buffering of TCP segments received and destined for the third UE unit 704. Although substantially all the bandwidth used by a dormant UE unit/application processor is reallocated to other active UE units/application processors, the skilled person should appreciate that in other examples at least part of the bandwidth can be reallocated instead of substantially all of the bandwidth used by the dormant device when active.

In order to achieve the increased data rates, the TCP segments received, and forwarded by the datagram flow optimizer apparatus 100 to the UE units not in a deep sleep mode, are transmitted at a higher data rate.

Although the above examples describe deployment of the datagram flow optimizer apparatus 100 in the context of a network protocol stack in a UTRAN of a Third Generation (3G) communications network, the skilled person should appreciate that the above architecture can be applied in respect of communication of flow control datagrams between an application processor and a processor of any other suitable communications system (Fig. 11). In such an embodiment, a modem stack 720 of an eUTRAN, of a Fourth Generation (4G) communications system, associated with Long Term Evolution (LTE) of the UMTS, or a Wireless Local Area Network (WLAN) 722 may comprise the datagram flow optimizer apparatus 100.

Similarly, the datagram flow optimizer apparatus 100 can be deployed in wired applications, for example a communications card, such as an Ethernet communications card or an

Asynchronous Digital Subscriber Line (ADSL) modem, which communicate flow control datagrams, for example TCP segments, to an application processor, the communications card or circuit being coupled to a wired communications network, for example a Local Area Network (LAN) 722.

In a further embodiment (Fig. 12), the datagram flow optimizer apparatus 100 can be deployed in an embedded system as a first thread 730, supporting, for example, a Radio Link Control (RLC) protocol. The first thread 730 is capable of communicating with a second thread 732 supporting, for example a Packet Data Convergence Protocol (PDCP) or an Inter-Processor Communication (IPC) thread, for example an enhanced Universal Asynchronous Receiver/Transmitter (UART) driver, an enhanced USB driver or a shared memory, the first and second threads 730, 732 having access to a memory resource 734. Hence, the second thread 732 is woken in accordance with the manner of operation of the datagram flow optimizer apparatus 100.

As should be appreciated by the skilled person, the above-described threads relate to a protocol architecture for LTE.

It is thus possible to provide an apparatus, system and method that facilitates reduced power consumption by processing devices, for example an application processor, operating in a system comprising the datagram flow optimization apparatus. Additionally, MCPS consumed by the processing device is reduced. Both the power saving and the MCPS consumption reduction are achieved without being at the expense of data throughput in the system. Hence, QoS is not compromised as a result of the power consumption and MCPS savings achieved. Furthermore, the computational overhead required to implement the datagram flow optimization apparatus is minimal. Also, the apparatus, system and method support operation of the IPSEC suite of protocols and permit implementation of the SACK option of the TCP.

Of course, the above advantages are exemplary, and these or other advantages may be achieved by the invention. Further, the skilled person will appreciate that not all advantages stated above are necessarily achieved by embodiments described herein.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, the connections may be an type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

The examples described herein can be implemented, if desired, as respective integrated circuits using any suitable substrate. In this respect, the semiconductor substrate described herein can be any semiconductor material or combinations of materials, such as gallium arsenide, silicon germanium, silicon-on-insulator (SOI), silicon, monocrystalline silicon, the like, and combinations of the above.

As used herein, if the logically true state is a logic level one, the logically false state is a logic level zero. And if the logically true state is a logic level zero, the logically false state is a logic level one.

Each signal described herein may be designed as positive or negative logic, where negative logic can be indicated by a bar over the signal name or an asterisk (*) following the name. In the case of a negative logic signal, the signal is active low where the logically true state corresponds to a logic level zero. In the case of a positive logic signal, the signal is active high where the logically true state corresponds to a logic level one. Note that any of the signals described herein can be designed as either negative or positive logic signals. Therefore, in alternate embodiments, those signals described as positive logic signals may be implemented as negative logic signals, and those signals described as negative logic signals may be implemented as positive logic signals.

The conductors as discussed herein may be illustrated or described in reference to being a single conductor, a plurality of conductors, unidirectional conductors, or bidirectional conductors. However, different embodiments may vary the implementation of the conductors and so many options exist for transferring signals.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

Moreover, the terms "front," "back," "top," "bottom," "over," "under" and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

Some of the above embodiments, as applicable, may be implemented using a variety of different information processing systems. For example, although Figure 1 and the discussion thereof describe an exemplary information processing architecture, this exemplary architecture is presented merely to provide a useful reference in discussing various aspects of the invention. Of course, the description of the architecture has been simplified for purposes of discussion, and it is just one of many different types of appropriate architectures that may be used in accordance with the invention. Those skilled in the art will recognize that the boundaries between logic blocks are merely illustrative and that alternative embodiments may merge logic blocks or circuit elements or impose an alternate decomposition of functionality upon various logic blocks or circuit elements.

Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In

an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

Also for example, in one embodiment, the illustrated elements of the datagram flow optimizer apparatus 100 can be circuitry located on a single integrated circuit or within a same device. Alternatively, the datagram flow optimizer apparatus 100 may include any number of separate integrated circuits or separate devices interconnected with each other. For example, the flow control mode detector 102 may be located on a same integrated circuit as the datagram scheduler 106 or on a separate integrated circuit or located within another peripheral discretely separate from other elements of the datagram flow optimizer apparatus 100. Also for example, the datagram flow optimizer apparatus 100 or portions thereof may be soft or code representations of physical circuitry or of logical representations convertible into physical circuitry. As such, the datagram flow optimizer apparatus 100 may be embodied in a hardware description language of any appropriate type.

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operation may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

Also, the invention is not limited to physical devices or units implemented in non-programmable hardware but can also be applied in programmable devices or units able to perform the desired device functions by operating in accordance with suitable program code. Furthermore, the devices may be physically distributed over a number of apparatuses, while functionally operating as a single device.

Also, devices functionally forming separate devices may be integrated in a single physical device.

However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps then those listed in a claim. Furthermore, Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced

claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A datagram flow optimizer apparatus comprising:

a buffer resource capable of receiving and temporarily storing a plurality of datagrams in respect of a forward path;

a buffer controller arranged to implement, when in use, buffering of received datagrams by the buffer resource until a predetermined threshold number of datagrams has been stored by the buffer resource; and

an acknowledgement regulator arranged to use the buffer resource to manipulate temporal spacing between acknowledgements of datagrams on a reverse path; wherein

the buffer controller is arranged to permit forwarding on the forward path of datagrams stored by the buffer resource in response to the predetermined threshold number of stored datagrams being reached.

2. An apparatus as claimed in Claim 1, wherein

the buffer controller is arranged to detect a flow control mode being employed in respect of the forward path and implement the buffering of received datagrams in response to the flow control mode being a delay tolerant flow control mode.

3. An apparatus as claimed in Claim 2, wherein the flow control mode is a congestion avoidance phase.

4. An apparatus as claimed in Claim 1 or Claim 2 or Claim 3, wherein the buffer controller comprises a flow control mode detector, the flow control mode detector being capable of measuring datagram size, measuring datagram inter-arrival time and detecting an acknowledgement of a datagram on the reverse path.

5. An apparatus as claimed in Claim 4, wherein the flow control mode detector is arranged to identify substantially constant size of received datagrams over a period of time and to identify substantially constant inter-arrival times over the period of time in respect of the received plurality of datagrams.

6. An apparatus as claimed in any one of the preceding claims, wherein the predetermined threshold number of datagrams is set to an initial value and incrementally increased with time.

7. An apparatus as claimed in Claim 6, wherein the buffer controller is arranged to receive an advertised window size, the predetermined threshold number of datagrams being incrementally increased up to a proportion of the advertised window size.

8. An apparatus as claimed in any one of the preceding claims, wherein the communication of the datagrams from the buffer resource on the forward path is controlled by the buffer controller so as to ensure a reverse path data rate that corresponds to maintenance of a forward path data rate.

9. An apparatus as claimed in any one of the preceding claims, wherein the temporal spacing between the acknowledgements of datagrams is defined by a ratio, N, of transmission of datagrams to acknowledgements, the ratio, N, being:

$$N = f_{avg_downlink}/f_{avg_uplink},$$

where: $f_{avg_downlink}$ is an average forward path datagram arrival rate, and f_{avg_uplink} is an average reverse path acknowledgement arrival rate.

10. An apparatus as claimed in any one of Claims 1 to 8, wherein the temporal spacing between acknowledgements is defined by a bit rate corresponding to receipt of a plurality of acknowledgements over a predetermined period of time.

11. An integrated circuit comprising the datagram flow optimizer apparatus as claimed in any one of the preceding claims.

12. A communications system comprising:

a source node arranged to send the plurality of datagrams to a destination node on a forward path via an intermediate node; wherein

the intermediate node comprises the datagram flow optimizer apparatus.

13. A system as claimed in Claim 12, wherein the intermediate node is capable of communicating with the destination node via a wireless interface.

14. A system as claimed in Claim 12 or Claim 13, wherein an application processor constitutes the destination node.

15. A system as claimed in Claim 12 or Claim 13, wherein a Universal Mobile Telecommunications System (UMTS) Terrestrial Radio Access Network (UTRAN) comprises the intermediate node.

16. A system as claimed in Claim 14 or Claim 15, wherein a User Equipment (UE) comprises the application processor.

17. A system as claimed in Claim 12, wherein the intermediate node is electrically coupled to the destination node.

18. A system as claimed in Claim 12, further comprising:

another destination node capable of communicating with the intermediate node; wherein

the intermediate node is arranged to assign to the another destination node at least part of bandwidth unused by the destination node during buffering of the plurality of datagrams by the datagram flow optimizer apparatus, thereby temporarily increasing bandwidth available for communications on the forward path with the another destination node.

19. A system as claimed in Claim 12, wherein the intermediate node is supported by a first thread and the destination node is supported by a second thread.

20. A method of optimizing datagram flow, the method comprising:

receiving a plurality of datagrams in respect of a forward path;

buffering the plurality of datagrams until a predetermined threshold number of datagrams has been stored;

permitting forwarding on the forward path of the buffered datagrams in response to the predetermined threshold number of stored datagrams being reached;

receiving acknowledgements of datagrams on a reverse path in respect of the forwarded datagrams; and

manipulating temporal spacing between the acknowledgements of datagrams on the reverse path.

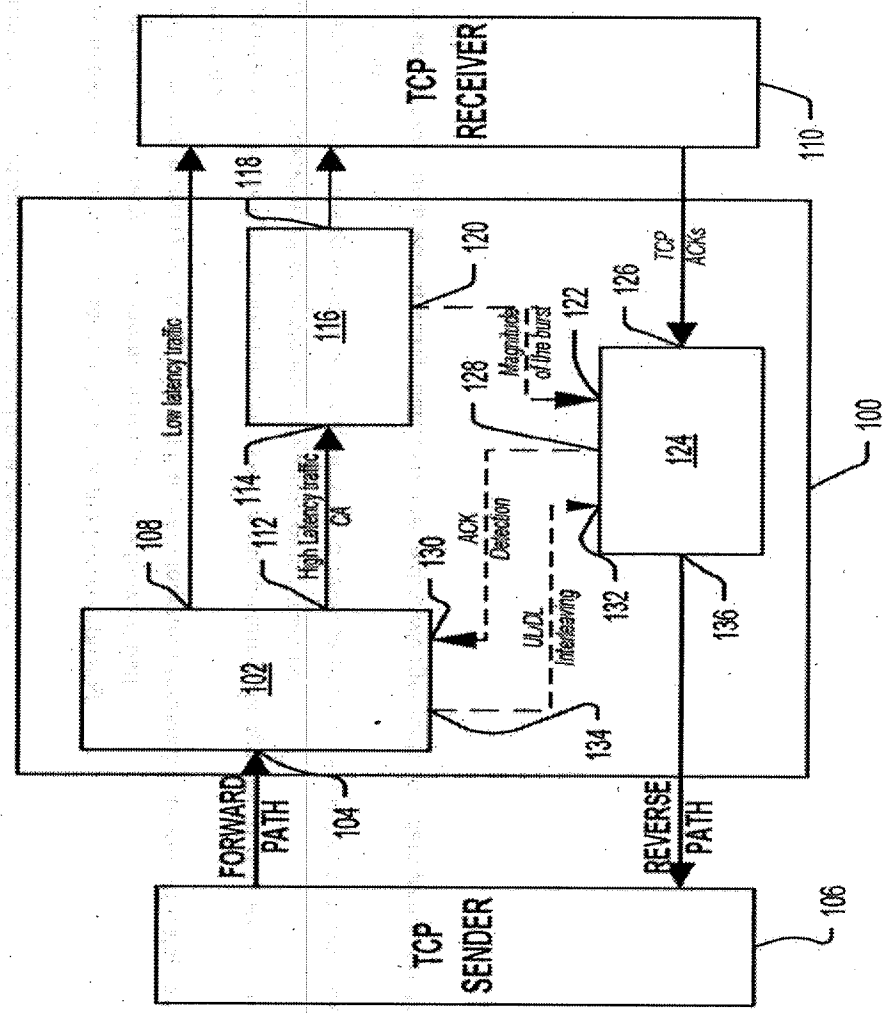

TCP RECEIVER
110
116
118
120
Low latency traffic
High Latency traffic
114
112
108
102
104
FORWARD PATH
TCP SENDER
106
ACK Detection
130
ULDL Interleaving
134
124
126
TCP ACKs
122
Magnitude of the burst
128
132
136
100
REVERSE PATH

Fig. 1

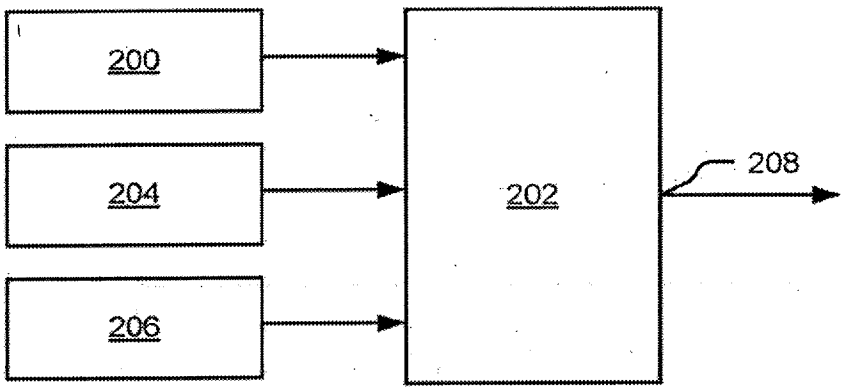
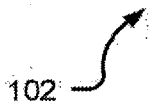


Fig. 2



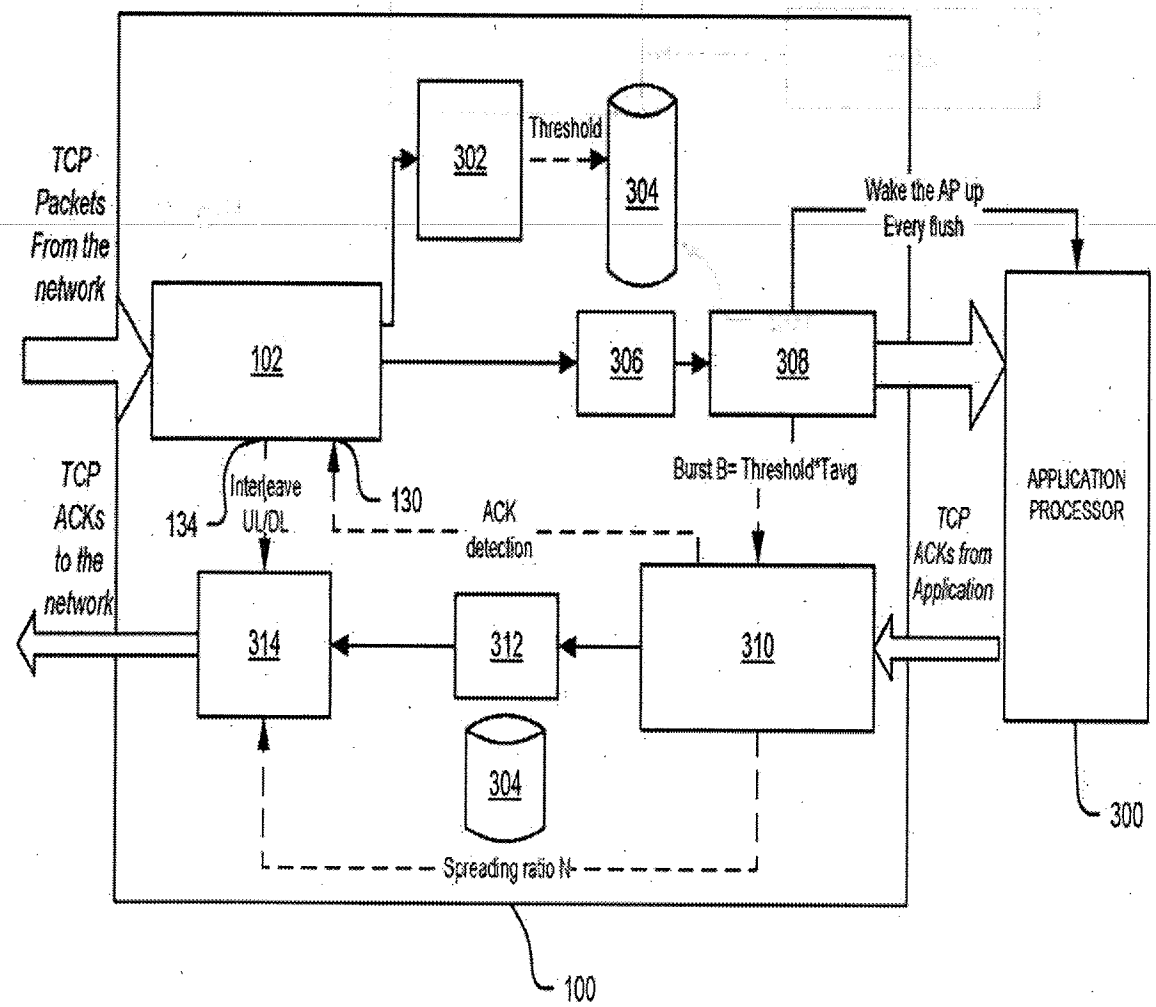

TCP Packets From the network
102
302
Threshold
304
306
308
Wake the AP up Every flush
APPLICATION PROCESSOR
300
TCP ACKs to the network
134
Interleave UL/DL
130
ACK detection
Burst B= Threshold*Tavg
TCP ACKs from Application
314
312
310
304
Spreading ratio N
100

Fig. 3

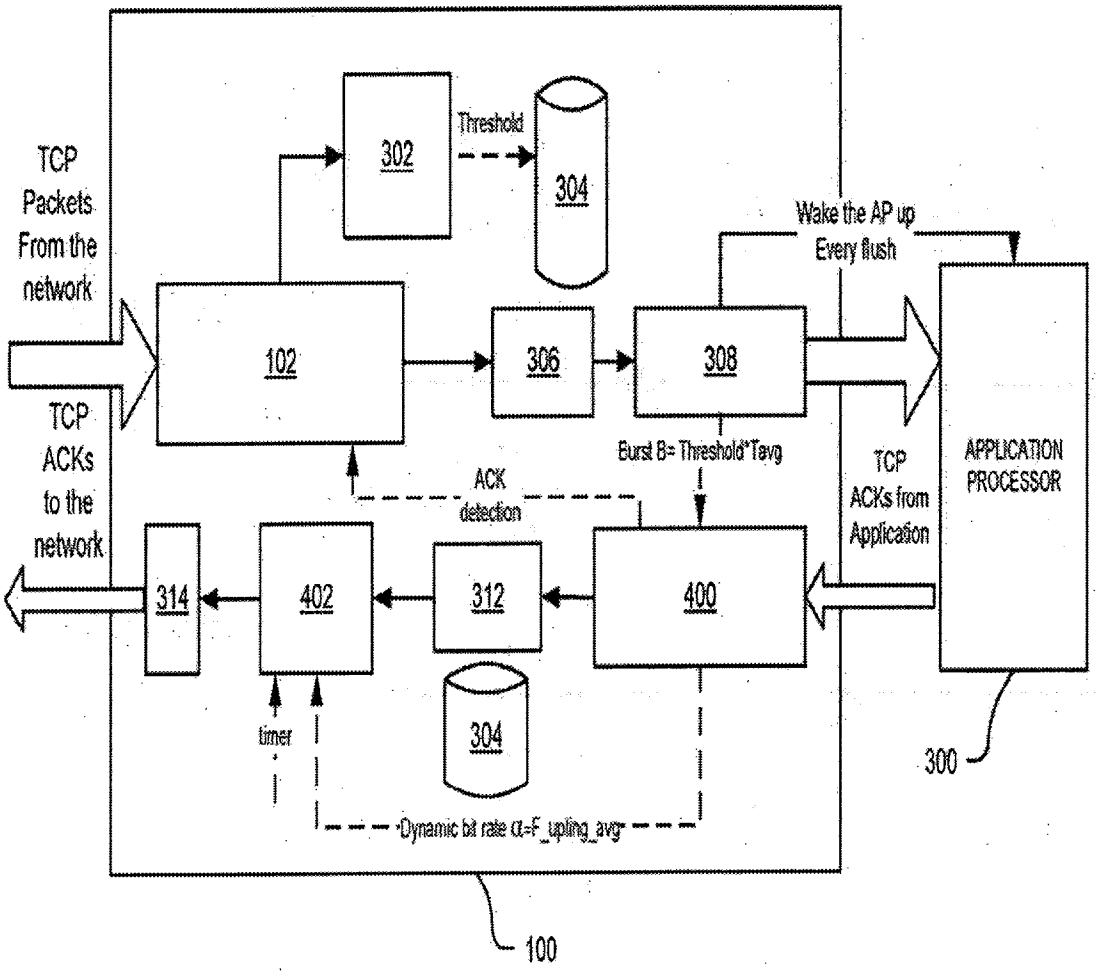

TCP Packets From the network
TCP ACKs to the network
302
Threshold
304
102
306
308
Wake the AP up Every flush
Burst B= Threshold*Tavg
ACK detection
TCP ACKs from Application
APPLICATION PROCESSOR
314
402
312
400
304
timer
Dynamic bit rate α=F_upling_avg
300
100

Fig. 4

502
System2
(eg
Application
Processor)
TCP
Packets
BURSTS
System1
(eg Modem
Processor)
TCP Packets
Frequency
F_downlink
Internet
Network
FORWARD PATH
TCP stack
Receiver
504
506
TCP
stack
Sender
REVERSE PATH
TCP ACKs
BURSTS
1 ACK out of n
packets
TCP ACKs
Frequency
F_uplink
=F_downlink/n
300
500
106

Fig. 5

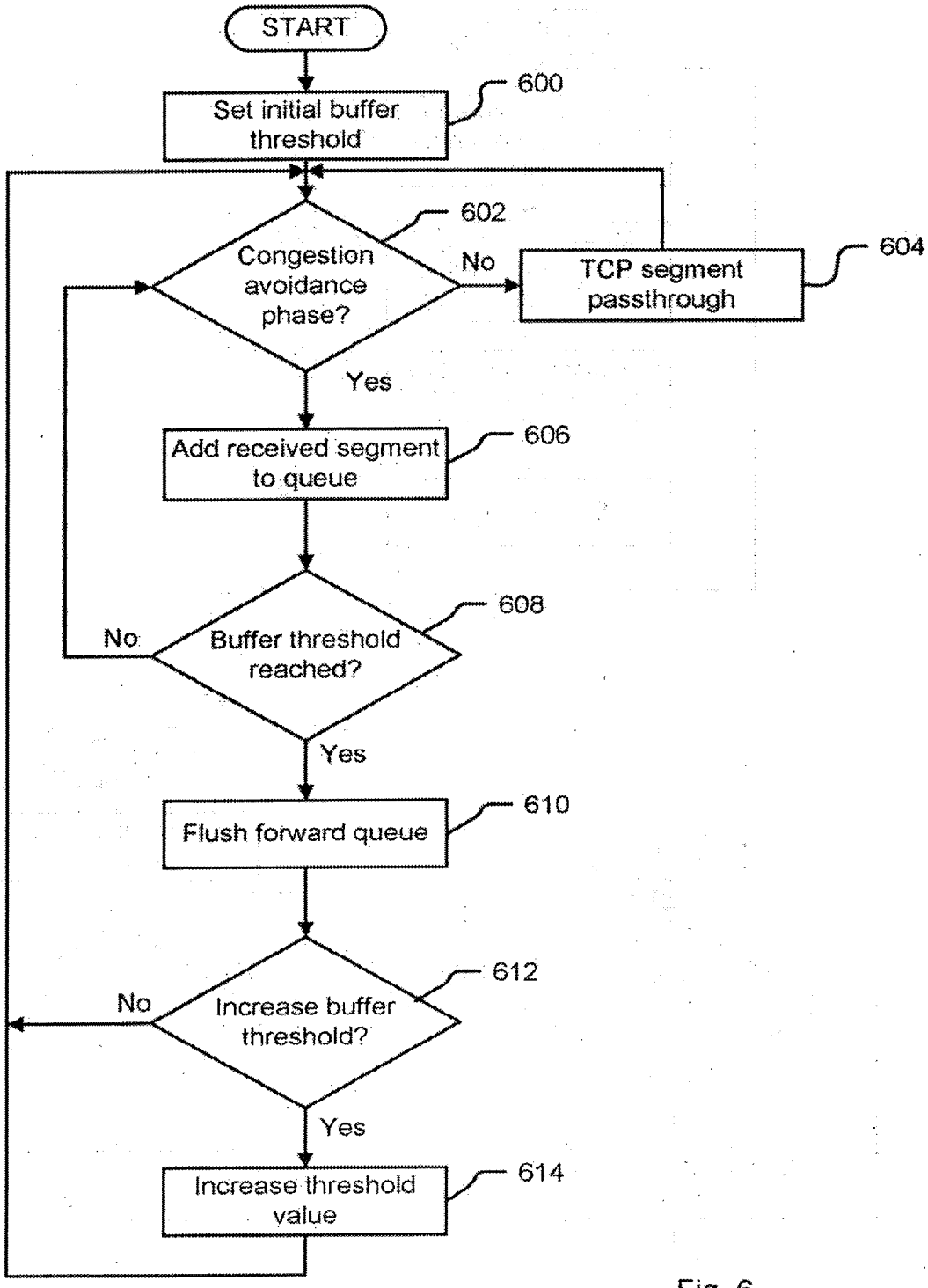

START
Set initial buffer threshold
600
Congestion avoidance phase?
602
No
TCP segment passthrough
604
Yes
Add received segment to queue
606
Buffer threshold reached?
608
No
Yes
Flush forward queue
610
Increase buffer threshold?
612
No
Yes
Increase threshold value
614

Fig. 6

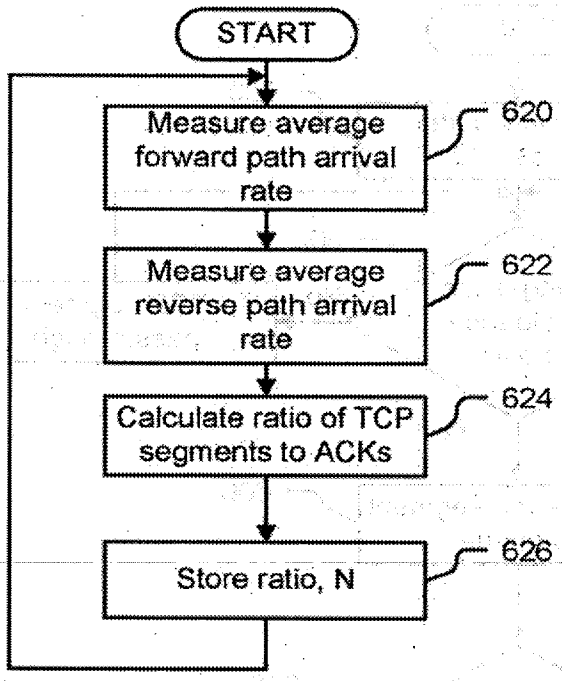


Fig. 7

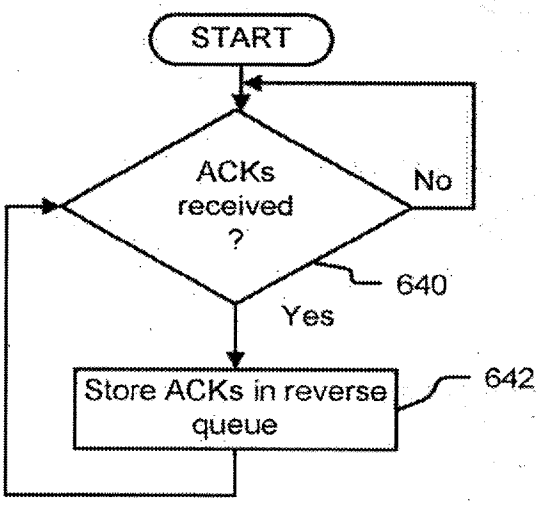


Fig. 8

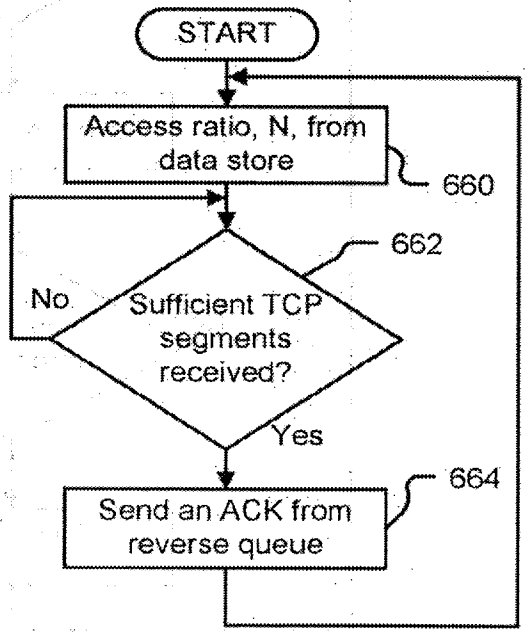


Fig. 9

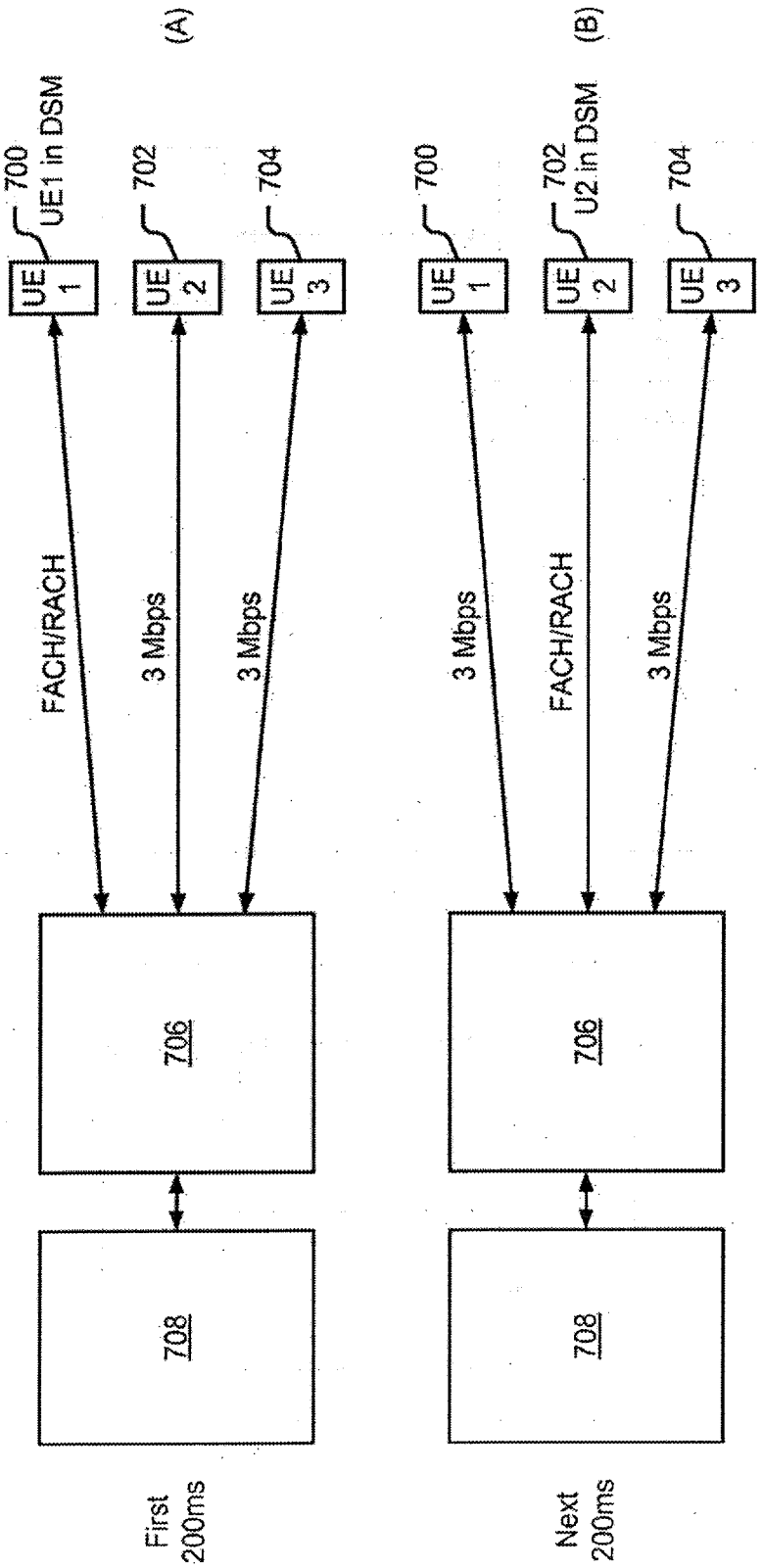

(A)
(B)
700
UE1 in DSM
702
704
UE 1
UE 2
UE 3
FACH/RACH
3 Mbps
3 Mbps
706
708
First 200ms
Next 200ms

Fig. 10

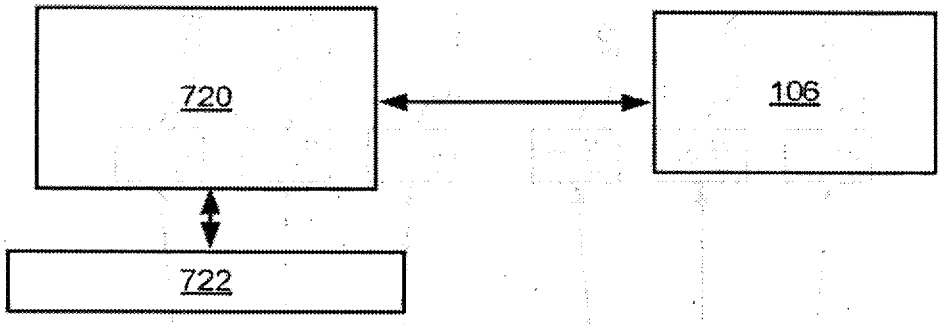


Fig. 11

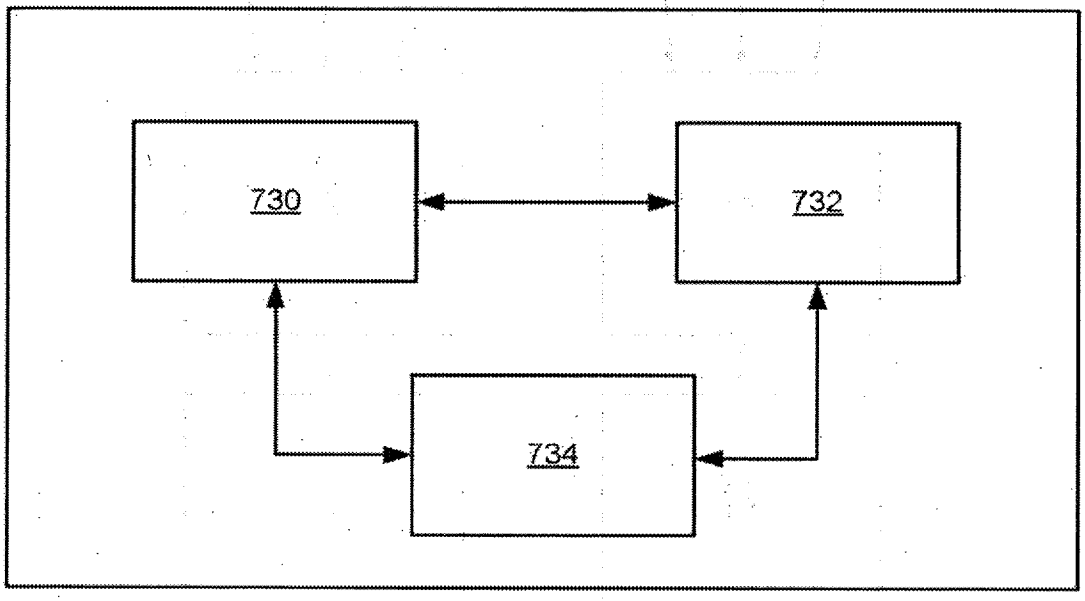


Fig. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/052801

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04W52/02 H04L12/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/215753 A1 (CHAN MUN-CHOON [US] ET AL) 28 October 2004 (2004-10-28) abstract page 1, paragraph 1 - page 2, paragraph 22 page 3, paragraph 29 - page 5, paragraph 53; claims 1-20; figures 1-14	1-17,19, 20
A	US 2007/218938 A1 (CARTER TRENT R [US]) 20 September 2007 (2007-09-20) abstract claims 1-7; figures 4,5	1,20
X	WO 02/33909 A (NOKIA CORP [FI]; CUNY RENAUD [ES]) 25 April 2002 (2002-04-25) abstract	1,20

-/--

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 December 2009	16/12/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jimenez Hernandez, P

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/052801

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/21233 A (NOKIA INTERNET COMMUNICATIONS [US]; DIXIT SUDHIR [US]; GHANI NASIR [US]) 13 April 2000 (2000-04-13) abstract	1,20
X	US 6 252 851 B1 (SIU KAI-YEUNG S [US] ET AL) 26 June 2001 (2001-06-26) abstract	1,20
A	WO 02/052800 A (NOKIA CORP [FI]; GROENBERG PETRI [FI]) 4 July 2002 (2002-07-04) the whole document	1-20

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/052801

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004215753 A1	28-10-2004	NONE	
US 2007218938 A1	20-09-2007	NONE	
WO 0233909 A	25-04-2002	AU 8997701 A	29-04-2002
		CA 2425230 A1	25-04-2002
		EP 1327337 A1	16-07-2003
		FI 20002320 A	21-04-2002
		US 2003179720 A1	25-09-2003
WO 0021233 A	13-04-2000	AU 6289099 A	26-04-2000
		CN 1344456 A	10-04-2002
		EP 1169826 A2	09-01-2002
		JP 2002527936 T	27-08-2002
		US 6215769 B1	10-04-2001
US 6252851 B1	26-06-2001	NONE	
WO 02052800 A	04-07-2002	CN 1478345 A	25-02-2004
		EP 1344352 A1	17-09-2003
		FI 20002848 A	23-06-2002
		US 2004057378 A1	25-03-2004

WITHROW & TERRANOVA, P.L.L.C.
DOCKETED
MAR 26 2015
K.B.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

To:
Davenport, Taylor M.
WITHROW & TERRANOVA, PLLC
100 Regency Forest Drive, Suite 160
Cary NC 27518
ETATS-UNIS D'AMERIQUE

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)*: 5 March 2015 (05-03-2015)
Applicant's or agent's file reference: 141062WO	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US2014/070368	International filing date *(day/month/year)*: 15 December 2014 (15-12-2014)
Applicant: QUALCOMM INCORPORATED	

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   How? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with any applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **19 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	SOGNO-PABIS, Elzbieta Tel: +31 (0)70 340-2414

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
141062WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2014/070368	15 December 2014 (15-12-2014)	16 December 2013 (16-12-2013)
Applicant		
QUALCOMM INCORPORATED		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title**,
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,
   a. the figure of the drawings to be published with the abstract is Figure No. 10
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/070368

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F1/32 G06F13/38 H04W52/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2009/039034 A1 (INTEL CORP [US]; TSAI JR-SHIAN [US]) 26 March 2009 (2009-03-26) the whole document	1-29
X	US 2013/198538 A1 (DIAB WAEL WILLIAM [US] ET AL) 1 August 2013 (2013-08-01) figures 2-5 paragraph [0007] paragraph [0017] - paragraph [0018] paragraph [0020] - paragraph [0028] paragraph [0031] - paragraph [0032] paragraph [0036]	1-29

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 February 2015	05/03/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	De Meyer, Arnaud

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/070368

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Jasmin Ajanovic: "PCI Express(TM) Architecture Advanced Protocols & Features PCI Express(TM) Architecture Advanced Protocols & Features", , 31 December 2003 (2003-12-31), XP055172048, PCI-SIG Developers Conference Retrieved from the Internet: URL:https://www.pcisig.com/developers/main/training_materials/get_document?doc_id=f275ada7d622d20947d69cbb34b6e0a0622249c3 [retrieved on 2015-02-25] slides 23-28	1-29
A	WO 2010/125429 A1 (FREESCALE SEMICONDUCTOR INC [US]; ROBIN JEAN-LUC [FR]; MENDES-CARVALHO) 4 November 2010 (2010-11-04) figure 5	1-29

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/070368

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2009039034 A1	26-03-2009	CN 101802753 A	11-08-2010
		EP 2191345 A1	02-06-2010
		JP 5047360 B2	10-10-2012
		JP 2010539753 A	16-12-2010
		KR 20100044268 A	29-04-2010
		US 2009077394 A1	19-03-2009
		US 2009077395 A1	19-03-2009
		US 2009077396 A1	19-03-2009
		US 2009077401 A1	19-03-2009
		US 2012178491 A1	12-07-2012
		WO 2009039034 A1	26-03-2009
US 2013198538 A1	01-08-2013	NONE	
WO 2010125429 A1	04-11-2010	US 2012039174 A1	16-02-2012
		WO 2010125429 A1	04-11-2010

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2014/070368	15.12.2014	16.12.2013

International Patent Classification (IPC) or both national classification and IPC
INV. G06F1/32 G06F13/38 H04W52/02

Applicant
QUALCOMM INCORPORATED

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	see form PCT/ISA/210	Telephone No. +31 70 340-0

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-29
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-29
Industrial applicability (IA)	Yes:	Claims	1-29
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:

D1 WO 2009/039034 A1 (INTEL CORP [US]; TSAI JR-SHIAN [US]) 26 March 2009 (2009-03-26)

D2 US 2013/198538 A1 (DIAB WAEL WILLIAM [US] ET AL) 1 August 2013 (2013-08-01)

D3 Jasmin Ajanovic: "PCI Express(TM) Architecture Advanced Protocols & Features PCI Express(TM) Architecture Advanced Protocols & Features",
, 31 December 2003 (2003-12-31), XP055172048,
PCI-SIG Developers Conference
Retrieved from the Internet:
URL:https://www.pcisig.com/developers/main/training_materials/get_document?doc_id=f275ada7d622d20947d69cbb34b6e0a0622249c3
[retrieved on 2015-02-25]

D4 WO 2010/125429 A1 (FREESCALE SEMICONDUCTOR INC [US]; ROBIN JEAN-LUC [FR]; MENDES-CARVALHO) 4 November 2010 (2010-11-04)

2 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of independent claims 1, 15, 20 and 24-29, when understood as specified in below Re Item VIII (clarity), does not involve an inventive step in the sense of **Article 33(3) PCT**.

2.1 Claim 1: Document D1 (by default, references in parentheses apply to this document) discloses a mobile terminal ([0013]: "a smartphone") comprising:
a modem timer ([0037]: "when a buffer unload timeout value expires");
a modem processor (fig.2: "communications sub-system 210"; Implicitly, "communication sub-system 210" is/comprises a *modem*, otherwise the smartphone of D1 could not process voice data and thus perform the functions of a phone), the

modem processor configured to hold modem processor to application processor data until expiration of the modem timer ([0037]: "when a buffer unload timeout value expires");
an application processor (fig.2: "computing sub-system 230");
an interconnectivity bus communicatively coupling the application processor to the modem processor (fig.2: "bus 220");~~and~~
~~the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus~~.

The subject-matter of claim 1 differs from document D1 in that:

(1) the application processor is configured to buffer the data to be sent to the modem processor; and

(2) the data from the application processor are sent after reception of the data from the modem processor.

These differences relate to different technical problems: power saving (1) and data transmission on a serial bus (2) and do not have a synergetic effect. These differences will therefore be considered independently for the assessment of a possible inventive step.

2.1.1 The technical effect of difference (1) is a reduction of power consumption, see [0007] of the application. Document D1 also relates to "buffering techniques for power management" (title and [0001]).

Starting from D1, the technical problem is formulated as how to further reduce power consumption.

In D1, the data are buffered by the modem processor so that downstream components can be put in a power saving mode ([0008]). Starting from D1, the most obvious solution to further reduce power consumption would be to increase the buffer size or the duration of the buffering. However, since there is a commonly known compromise between buffering and performance ([0009]: "...while maintaining Quality of Service (QoS) and other performance requirements"), it may not be possible to increase the buffering of the data to be transferred to the application processor. In such case, an obvious solution to further reduce power consumption consists of also buffering the data to be transferred to the modem processor, in the exact same way as for the data to be transferred to

the application processor. This modification corresponds merely to the duplication of the buffing means disclosed by D1. This is the solution recited by claim 1.

2.1.2 The technical effect of difference (2) is to avoid data collisions on the serial bus, i.e the PCI express bus introduced by claims 2 and 3. Document D1 also uses a PCI express bus ([0028]).

Starting from D1, the technical problem is formulated as how to avoid data collision on a serial bus.

It is not possible to transmit data on PCI express bus at the same time and in both directions. Therefore, there are only two possible solutions: it is only possible to send the data from application processor after having receiving, or before sending, the data from the modem processor; the first solution being the one recited by the claim 1. Document D1 is silent about which one of these solutions to use. Consequently, the skilled person willing to implement D1 would have to choose one of these two solutions. Sending the data from the application processor before or after the data from the modem processor are obviously equivalent solutions, and the skilled person would select one or the other, depending on the circumstances, without making use of inventive skills.

2.2 Claims 15, 20 and 24-29: Substantially, claims 1, 15, 20 and 24-29 correspond to different alternatives combinations of using a timer/ a counter/ an amount of data being buffered, and of sending the data from the application processor before or after the data from the modem processor. The different alternatives combinations of using a timer/ a counter/ an amount of data being buffered are disclosed by D1 ([0037]). Therefore the reasoning in above §2.1 for the subject-matter of claim 1 also applies, mutatis mutandis, to the subject-matter of claims 15, 20 and 24-29.

3 The subject-matter of dependent claims 2-14, 16-19, 21-23, when understood as specified in below Re Item VIII (clarity), does not involve an inventive step in the sense of **Article 33(3) PCT**.

3.1 Claims 2, 3 and 16: Disclosed by D1 ([0028]: "PCI Express (PCIe)").

3.2 Claims 4, 6, 7, 17 and 18: As illustrated by D1 ([0009]: "...while maintaining Quality of Service (QoS) and other performance requirements"), it is commonly known that there is a trade-off between buffering and performances, e.g. more buffering implies more latency. Therefore, the skilled person will select a duration for the buffer timer that fits the circumstances, without making use of inventive skills.

3.3 Claim 5: Disclosed by D1 ([0010]: "software").

3.4 Claim 8: Disclosed by D1 (fig.2).

3.5 Claims 9, 21 and 22: Considering the clarity issues raised in below Re Item VIII, claims 9, 21 and 22 are seen as mere design choices.

3.6 Claims 10-14, 19 and 23: Considering the clarity issues raised in below Re Item VIII, claims 10-14, 19 and 23 are interpreted broadly and disclosed by D1 ([0037]).

4 For the sake of completeness, it is pointed out that the claimed invention seems to correspond to the mere implementation of the PCI Express (PCIe) standard, in particular of the full-duplex mode of the L1/L0s power states of the Active State Power Management (ASPM), as illustrated for example by document D3 (slides 23-28). The person skilled in the art knows the PCIe standard which forms part of the common general knowledge in the art. Therefore, starting from any document that hints to use the PCIe ASPM, the person skilled in the art would think of the different power saving states (L1, L0 and L0s) and implement the most appropriate once, without making use of inventive skills.

Document D2, for example, discloses an apparatus comprising a network controller and a CPU linked by a PCIe bus (fig.1). Also, D2 leads to the use of the PCIe ASPM ([0007]). The subject-matter of claims 1-29 lacks an inventive step in the light of D2 combined with the common general knowledge, i.e. the PCIe standard, see references in the associated search report.

Re Item VIII

Certain observations on the international application

5 Although claims 1, 20, 24, 25, 26, 27, and 29 (terminals) and claims 15 and 28 (methods) have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and/or in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of **Article 6 PCT**.

6 The application does not meet the requirements of **Article 6 PCT**, because the claims are not clear.

6.1 The claims relate to different timers and counters that are designated in a vague and inconsistent manner, and leave the reader in doubt as to the meaning of the technical features to which they refer.

First example: The skilled person would normally understand that the "modem timer" is the timer of a modem. However, in claim 9 for example, the "modem timer" is not part of the modem. Therefore it is not clear what is the "*modem* timer" and what it times.

Second example: The terminology is inconsistent. From the claims, the skilled person would understand that the "uplink timer" and the "application timer" are distinct features. This is consistent with part of the description. However, in other parts of the description, the "uplink timer" and the "application timer" are the same, e.g. [0054]: "the uplink timer (i.e. the application timer)". The same applies for the "downlink timer" and the "modem timer" In other words, it is not clear what are these different timers and what they time.

Third example: Even in the the help of the description, it is not clear what is performed by the "modem byte accumulation limit counter".

It is pointed out that this list of examples is not exhaustive.

Altogether, it is not clear what differentiates the claimed timers and counters from those known in the art. The claims should be clarified. When assessing novelty an inventive step, the different timers and counters recited by the claims are therefore interpreted broadly as "a timer" and "a counter".

6.2 Independent claims: It could be understood, for example from claim 1, that the transmission of each data is simply delayed for a duration defined by the "modem timer". However, it appears in the light of fig.10 that the data to be transferred are buffered. The claims should be clarified. When assessing novelty an inventive step, it is considered that the data are buffered.

Bitte beachten Sie, dass angeführte Nichtpatentliteratur (wie z. B. wissenschaftliche oder technische Dokumente) je nach geltendem Recht dem Urheberrechtsschutz und/oder anderen Schutzarten für schriftliche Werke unterliegen könnte. Die Vervielfältigung urheberrechtlich geschützter Texte, ihre Verwendung in anderen elektronischen oder gedruckten Publikationen und ihre Weitergabe an Dritte ist ohne ausdrückliche Zustimmung des Rechtsinhabers nicht gestattet.

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XS CPRTENFRDE

BNSDOCID: <XS_____20061001103CF_1_>

Electronic Acknowledgement Receipt

EFS ID:	22545969
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/Ross Trevor
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	05-JUN-2015
Filing Date:	12-DEC-2014
Time Stamp:	10:29:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	141062_IDS_5-15-15.pdf	707052 6549218dc859a8998e58d54b8ec59c7dc5b8 46f	no	4

Warnings:	
Information:	

2	Non Patent Literature	Ajanovic_PCI-Express-Architecture.pdf	15740236	no	49
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
3	Foreign Reference	WO2009039034A1.pdf	1909770	no	35
Warnings:					
Information:					
4	Foreign Reference	WO2010125429A1.pdf	1137450	no	29
Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	PCTUS2014070368_ISR_3-5-15.pdf	1194336	no	14
Warnings:					
Information:					
Total Files Size (in bytes):			20688844		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/568,694	12/12/2014	2115	5140	141062/1173-141	29	9

CONFIRMATION NO. 3463

CORRECTED FILING RECEIPT

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
Cary, NC 27518



Date Mailed: 05/22/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Vinod Harimohan Kaushik, San Diego, CA;
Uppinder Singh Babbar, San Diego, CA;
Andrei Danaila, San Diego, CA;
Neven Klacar, San Diego, CA;
Muralidhar Coimbatore Krishnamoorthy, San Diego, CA;
Arunn Coimbatore Krishnamurthy, San Diego, CA;
Vaibhav Kumar, Encinitas, CA;
Vanitha Aravamudhan Kumar, San Diego, CA;
Shailesh Maheshwari, San Diego, CA;
Alok Mitra, San Diego, CA;
Roshan Thomas Pius, San Jose, CA;
Hariharan Sukumar, San Diego, CA;

Applicant(s)

QUALCOMM Incorporated, San Diego, CA;

Power of Attorney: The patent practitioners associated with Customer Number 115309

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/916,498 12/16/2013
and claims benefit of 62/019,073 06/30/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 12/24/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/568,694**

Projected Publication Date: 06/18/2015

Non-Publication Request: No

Early Publication Request: No

Title

POWER SAVING TECHNIQUES IN COMPUTING DEVICES

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	14/568,694	Confirmation No.: 3463
Applicant(s):	Vinod Harimohan Kaushik et al.	
Filed:	12/12/2014	
Art Unit:	2642	
Examiner:		
Title:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Docket No.: 141062/1173-141
Customer No.: 115309

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTED FILING RECEIPT

This is a Request for Corrected Filing Receipt for the above-identified application. Please correct the information of the eleventh inventor to read:

Roshan Thomas Pius, San Jose, CA

An updated Application Data Sheet with changes marked thereon is submitted concurrently herewith to supply the requested changes above, along with a marked up copy of the filing receipt showing the changes. In addition, Applicant herewith submits the processing fee under 37 CFR 1.17(i)(1) of one hundred forty dollars ($140.00). If any issues remain, please contact the undersigned attorney.

Respectfully submitted,

/Taylor M. Davenport Reg#42466/

Taylor M. Davenport
Registration No. 42,466
Withrow & Terranova, PLLC
100 Regency Forest Drive, Suite 160
Cary, NC 27518
919-238-2300

Date: May 19, 2015
Attorney Docket No.: 141062/1173-141

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vinod	Harimohan	Kaushik	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Uppinder	Singh	Babbar	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Andrei		Danaila	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Remove

Inventor 4

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Neven		Klacar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Remove

Inventor 5

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Muralidhar	Coimbatore	Krishnamoorthy	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Remove

Inventor 6

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Arunn	Coimbatore	Krishnamurthy	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country**	US

Inventor 7 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vaibhav		Kumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Encinitas	**State/Province**	CA	**Country of Residence**	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country**	US

Inventor 8 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vanitha	Aravamudhan	Kumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	**State/Province**	CA	**Country of Residence**	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country**	US

Inventor 9 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shailesh		Maheshwari	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	**State/Province**	CA	**Country of Residence**	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Deigo	**State/Province**	CA
Postal Code	92121	**Country**	US

Remove

Inventor 10

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Alok		Mitra	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country**	US

Remove

Inventor 11

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Roshan	Thomas	Pius	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	~~San Diego~~ San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	~~5775 Morehouse Drive~~ 65 Rio Robles East		
Address 2	Unit #2115		
City	~~San Diego~~ San Jose	**State/Province**	CA
Postal Code	~~92121~~ 95134	**Country**	US

Remove

Inventor 12

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hariharan		Sukumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence information of this application.**

Customer Number	115309		
Email Address	patents@wt-ip.com	Add Email	Remove Email
Email Address	us-docketing@qualcomm.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES		
Attorney Docket Number	141062/1173-141	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	10

Filing By Reference :

Only compete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	(●) Customer Number	( ) US Patent Practitioner	( ) Limited Recognition (37 CFR 11.9)
Customer Number	115309		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	61916498	2013-12-16
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62019073	2014-06-30

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

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Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	QUALCOMM Incorporated		
Mailing Address Information For Applicant:			
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Address 2			
City	San Diego	**State/Province**	CA
Country	US	Postal Code	92121
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Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Taylor M. Davenport/			Date (YYYY-MM-DD)	2014-12-12
First Name	Taylor	Last Name	Davenport	Registration Number	42466

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/568,694	12/12/2014	2642	4980	141062/1173-141	29	9

CONFIRMATION NO. 3463

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
Cary, NC 27518

WITHROW & TERRANOVA P.L.L.C.
DOCKETED
DEC 31 2014
K.B.

FILING RECEIPT

OC00000072563130

Date Mailed: 12/30/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

QUALCOMM Incorporated, San Diego, CA

Power of Attorney: The patent practitioners associated with Customer Number 115309

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/916,498 12/16/2013
and claims benefit of 62/019,073 06/30/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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If Required, Foreign Filing License Granted: 12/24/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/568,694**

Projected Publication Date: 06/18/2015

Non-Publication Request: No

Early Publication Request: No

Title

POWER SAVING TECHNIQUES IN COMPUTING DEVICES

Preliminary Class

455

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141

CONFIRMATION NO. 3463

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
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NOTICE

OC000000072563131

Date Mailed: 12/30/2014

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  - Vinod Harimohan Kaushik
  - Uppinder Singh Babbar
  - Andrei Danaila
  - Neven Klacar
  - Muralidhar Coimbatore Krishnamoorthy
  - Arunn Coimbatore Krishnamurthy
  - Vaibhav Kumar
  - Vanitha Aravamudhan Kumar
  - Shailesh Maheshwari
  - Alok Mitra
  - Roshan Pius
  - Hariharan Sukumar

Electronic Patent Application Fee Transmittal

Application Number:	14568694
Filing Date:	12-Dec-2014
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Filer:	Taylor M. Davenport/David Smith
Attorney Docket Number:	141062/1173-141

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**140**

Electronic Acknowledgement Receipt

EFS ID:	22388343
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/David Smith
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	19-MAY-2015
Filing Date:	12-DEC-2014
Time Stamp:	14:44:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$140
RAM confirmation Number	1086
Deposit Account	501732
Authorized User	DAVENPORT, TAYLOR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	1173-141_RequestforCorrectedFilingReceipt.pdf	18613 25a1ac675282d5acd435e6dac7e945472aa2267	no	2
Warnings:					
Information:					
2	Application Data Sheet	141062_Supplemental_ADS.pdf	146073 6f7e6cbdae674bea07116728e9ea8b4d9d6e243	no	10
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Request for Corrected Filing Receipt	141062_FilingReceipt_markup.pdf	1728110 2561299433824565162164a78e29d36f54e4aee	no	5
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30929 a1cea0443894fb5b138f6ec5e02d8e6ca378e45a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1923725		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	14/568,694	Confirmation No.: 3463
Applicant(s):	Vinod Harimohan Kaushik et al.	
Filed:	12/12/2014	
Art Unit:	2115	
Examiner:	Thomas C. Lee	
Title:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Docket No.: 141062/1173-141
Customer No.: 115309

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

The following is a Preliminary Amendment for the above-referenced application. Applicant submits payment of $160.00 for two additional claims in excess of 20. If any additional fees are required in association with this Preliminary Amendment, the Director is hereby authorized to charge them to Deposit Account 50-1732, and consider this a petition therefor.

Amendments to the Claims are reflected in the listing of claims beginning on page **2**.

Remarks begin on page **9** of this paper.

In the Claims:

1. (Original) A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

2. (Original) The mobile terminal of claim 1, wherein the interconnectivity bus comprises a peripheral component interconnect (PCI) compliant bus.

3. (Original) The mobile terminal of claim 2, wherein the PCI compliant bus comprises a PCI express (PCIe) bus.

4. (Original) The mobile terminal of claim 1, wherein the application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer.

5. (Original) The mobile terminal of claim 1, wherein the modem timer is implemented in software.

6. (Original) The mobile terminal of claim 1, wherein the modem timer has a period of approximately six (6) milliseconds.

7. (Original) The mobile terminal of claim 4, wherein the application processor is configured to hold the application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first.

8. (Original) The mobile terminal of claim 1, wherein the modem processor comprises the modem timer.

9. (Original) The mobile terminal of claim 1, wherein the application processor comprises the modem timer.

10. (Original) The mobile terminal of claim 1, further comprising an application timer, and wherein the modem processor is configured to instruct the application processor to send an interrupt if no data is received within one time slot of the application timer.

11. (Original) The mobile terminal of claim 1, further comprising a byte accumulation limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the byte accumulation limit counter is exceeded.

12. (Original) The mobile terminal of claim 1, further comprising a packet number limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the packet number limit counter is exceeded.

13. (Original) The mobile terminal of claim 1, wherein the modem processor is configured to determine if held data comprises a control packet and send such control packet before expiration of the modem timer.

14. (Original) The mobile terminal of claim 3, wherein the modem processor further comprises an application timer, and the modem processor is configured to pull data from the application processor on receipt of the modem processor to application processor data or expiration of the application timer.

15. (Original) A method of controlling power consumption in a computing device, comprising:

holding data received by a modem processor from a remote network until expiration of a downlink timer;

passing the data received by the modem processor to an application processor over an interconnectivity bus; and

holding application data generated by an application associated with the application processor until receipt of the data from the modem processor or expiration of an uplink timer, whichever occurs first.

16. (Original) The method of claim 15, wherein passing the data comprises passing the data over a peripheral component interface (PCI) compliant bus.

17. (Original) The method of claim 15, wherein a period of the downlink timer comprises six (6) milliseconds.

18. (Original) The method of claim 15, wherein a period of the uplink timer comprises seven (7) milliseconds.

19. (Original) The method of claim 15, further comprising providing an override capability based on one of accumulated packet size, accumulated packet count, accumulated byte count, quality of service requirement, and control message status.

20. (Original) A mobile terminal comprising:

a modem processor;

an application timer;

an application processor, the application processor configured to hold application processor to modem processor data until expiration of the application timer;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

21. (Original) The mobile terminal of claim 20, wherein the application processor comprises the application timer.

22. (Original) The mobile terminal of claim 20, wherein the modem processor comprises the application timer.

23. (Original) The mobile terminal of claim 20, further comprising a byte counter counting bytes at the modem processor.

24. (Original) A mobile terminal comprising:

a modem byte accumulation limit counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

25. (Original) A mobile terminal comprising:

a modem packet counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of packets has been reached by the modem packet counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

26. (Original) A mobile terminal comprising:

a modem processor;

an application byte counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of bytes has been reached by the application byte counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the

application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

27. (Original) A mobile terminal comprising:

a modem processor;

an application packet counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of packets has been reached by the application packet counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

28. (Original) A method comprising:

starting an application timer at an application processor;

accumulating data at the application processor until expiration of the application timer;

sending the accumulated data from the application processor to a modem processor across an interconnectivity bus; and

holding modem processor data at the modem processor until receipt of the accumulated data from the application processor.

29. (Original) A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data.

30. (New) The mobile terminal of claim 1, further comprising a second modem processor, the second modem processor configured to exchange data availability information with the modem processor such that traffic on the modem processor can trigger data transfer for the second modem processor.

31. (New) The method of claim 15, further comprising holding data at a second modem processor until traffic on the modem processor triggers data transfer for the second modem processor.

REMARKS

Applicant files the Preliminary Amendment to herein to provide new claims 30 and 31. Support for these claims can be found in at least paragraph 0053 of the application as originally filed. No new matter is added. Applicant respectfully requests these amendments be entered before examination.

Applicant herein pays $160.00 for the two additional dependent claims.

Respectfully submitted,

/Taylor M. Davenport Reg#42466/

Taylor M. Davenport
Registration No. 42,466
Withrow & Terranova, PLLC
100 Regency Forest Drive, Suite 160
Cary, NC 27518
919-238-2300

Date: April 27, 2015
Attorney Docket No.: 141062/1173-141

Electronic Patent Application Fee Transmittal

Application Number:	14568694
Filing Date:	12-Dec-2014
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Filer:	Taylor M. Davenport/David Smith
Attorney Docket Number:	141062/1173-141

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	2	80	160
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Electronic Acknowledgement Receipt

EFS ID:	22170443
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/David Smith
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	27-APR-2015
Filing Date:	12-DEC-2014
Time Stamp:	09:48:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$160
RAM confirmation Number	11134
Deposit Account	501732
Authorized User	DAVENPORT, TAYLOR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

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Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		141062_PreliminaryAmendment_04-27-15_AsFiled.pdf	42800	yes	9

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	8
Applicant Arguments/Remarks Made in an Amendment	9	9

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30991	no	2

Warnings:

Information:

Total Files Size (in bytes):	73791

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/568,694	Filing Date 12/12/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT 04/27/2015

	(Column 1)		(Column 2)	(Column 3)		
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 31	Minus	** 29	= 2	x $80 =	160
Independent (37 CFR 1.16(h))	* 9	Minus	***9	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	160

AMENDMENT

	(Column 1)		(Column 2)	(Column 3)		
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/KAREN VESTAL/

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number 14/568,694 filed on 2014-12-12

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Vinod Harimohan Kaushik Date (Optional): 01/23/15

Signature: Vinod Kaushik

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: Uppinder Singh Babbar Date (Optional): Jan 22, 2015

Signature: [signature]

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Andrei Danaila Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Neven Klacar Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Muralidhar Coimbatore Krishnamoorthy Date (Optional): 12/12/14

Signature: C.K. Muralidhar

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Arunn Coimbatore Krishnamurthy Date (Optional): 01/12/15

Signature: [signature]

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number 14/568,694 filed on 2014-12-12.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Vaibhav Kumar Date (Optional):

Signature: Vaibhav Kumar

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Vanitha Aravamudhan Kumar Date (Optional): 02/10/15

Signature: Vanitha

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Shailesh Maheshwari Date (Optional): _____

Signature: _____

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LEGAL NAME OF INVENTOR

Inventor: Alok Mitra Date (Optional): 01/20/2015

Signature: _____

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LEGAL NAME OF INVENTOR

Inventor: Roshan Pius Date (Optional): 01/14/2015

Signature: Roshan

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LEGAL NAME OF INVENTOR

Inventor: Hariharan Sukumar Date (Optional): 01/20/2015

Signature: Hariharan

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	21496183
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/Allyson Van Gorder
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	13-FEB-2015
Filing Date:	12-DEC-2014
Time Stamp:	13:47:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	141062_Decs_02-13-15_AsFiled.PDF	11597394 b326de36af7aa26d7c7e343868686f340ca8360	no	13

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vinod	Harimohan	Kaushik	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Inventor 2 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Uppinder	Singh	Babbar	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Inventor 3 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Andrei		Danaila	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Neven		Klacar	

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Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Muralidhar	Coimbatore	Krishnamoorthy	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country	US

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Arunn	Coimbatore	Krishnamurthy	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country i**	US

Remove

Inventor 7

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vaibhav		Kumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Encinitas	**State/Province**	CA	**Country of Residence**	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country i**	US

Remove

Inventor 8

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vanitha	Aravamudhan	Kumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	**State/Province**	CA	**Country of Residence**	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country i**	US

Remove

Inventor 9

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shailesh		Maheshwari	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	**State/Province**	CA	**Country of Residence**	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Deigo	State/Province	CA
Postal Code	92121	Country i	US

Inventor 10 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Alok		Mitra	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	State/Province	CA
Postal Code	92121	Country i	US

Inventor 11 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Roshan	Thomas	Pius	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	~~San Diego~~ San Jose	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	~~5775 Morehouse Drive~~ 65 Rio Robles East		
Address 2	Unit #2115		
City	~~San Diego~~ San Jose	State/Province	CA
Postal Code	~~92121~~ 95134	Country i	US

Inventor 12 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hariharan		Sukumar	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Diego	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	115309		
Email Address	patents@wt-ip.com	Add Email	Remove Email
Email Address	us-docketing@qualcomm.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES		
Attorney Docket Number	141062/1173-141	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	10

Filing By Reference :

Only compete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	(●) Customer Number	( ) US Patent Practitioner	( ) Limited Recognition (37 CFR 11.9)
Customer Number	115309		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	61916498	2013-12-16
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62019073	2014-06-30

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	QUALCOMM Incorporated		
Mailing Address Information For Applicant:			
Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Country	US	Postal Code	92121
Phone Number	(858) 658-4351	Fax Number	(919) 297-3298
Email Address	us-docketing@qualcomm.com		

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country[i]		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Taylor M. Davenport/			Date (YYYY-MM-DD)	2014-12-12
First Name	Taylor	Last Name	Davenport	Registration Number	42466

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	21321472
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Steven Terranova/Allyson Van Gorder
Filer Authorized By:	Steven Terranova
Attorney Docket Number:	141062/1173-141
Receipt Date:	27-JAN-2015
Filing Date:	12-DEC-2014
Time Stamp:	15:26:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	141062_UpdatedADS_01-27-15.pdf	155231 [illegible]	no	10

Warnings:	
Information:	

This is not an USPTO supplied ADS fillable form	
Total Files Size (in bytes):	155231

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/568,694

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	29 minus 20 =	* 9			OR	x 80 =	720
INDEPENDENT CLAIMS (37 CFR 1.16(h))	9 minus 3 =	* 6				x 420 =	2520
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	4840

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/568,694	12/12/2014	2642	4980	141062/1173-141	29	9

CONFIRMATION NO. 3463

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
Cary, NC 27518

FILING RECEIPT



Date Mailed: 12/30/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Vinod Harimohan Kaushik, San Diego, CA;
Uppinder Singh Babbar, San Diego, CA;
Andrei Danaila, San Diego, CA;
Neven Klacar, San Diego, CA;
Muralidhar Coimbatore Krishnamoorthy, San Diego, CA;
Arunn Coimbatore Krishnamurthy, San Diego, CA;
Vaibhav Kumar, Encinitas, CA;
Vanitha Aravamudhan Kumar, San Diego, CA;
Shailesh Maheshwari, San Diego, CA;
Alok Mitra, San Diego, CA;
Roshan Pius, San Diego, CA;
Hariharan Sukumar, San Diego, CA;

Applicant(s)

QUALCOMM Incorporated, San Diego, CA

Power of Attorney: The patent practitioners associated with Customer Number 115309

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/916,498 12/16/2013
and claims benefit of 62/019,073 06/30/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/568,694**

Projected Publication Date: 06/18/2015

Non-Publication Request: No

Early Publication Request: No

Title

POWER SAVING TECHNIQUES IN COMPUTING DEVICES

Preliminary Class

455

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/568,694	12/12/2014	Vinod Harimohan Kaushik	141062/1173-141

CONFIRMATION NO. 3463

115309
W&T/Qualcomm
100 Regency Forest Drive
Suite 160
Cary, NC 27518

NOTICE



Date Mailed: 12/30/2014

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Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  - Vinod Harimohan Kaushik
  - Uppinder Singh Babbar
  - Andrei Danaila
  - Neven Klacar
  - Muralidhar Coimbatore Krishnamoorthy
  - Arunn Coimbatore Krishnamurthy
  - Vaibhav Kumar
  - Vanitha Aravamudhan Kumar
  - Shailesh Maheshwari
  - Alok Mitra
  - Roshan Pius
  - Hariharan Sukumar

Doc Code: PA..
Document Description: Power of Attorney

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Application Number	
Filing Date	2014-12-12
First Named Inventor	Vinod Harimohan Kaushik
Title	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	141062/1173-141

SIGNATURE of Applicant or Patent Practitioner

Signature	/Taylor M. Davenport/	Date (Optional)	December 12, 2014
Name	Taylor M. Davenport	Registration Number	42466
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

115309

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☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

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I am the Applicant:

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☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient *Proprietary* Interest (*e.g.*, a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature	/RHorn/	Date	15 May 2013
Name	Raymond S. Horn	Telephone	858-651-3679
Title and Company	VP, Patent Counsel and Qualcomm Incorporated		

NOTE: Signature - This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

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(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2014-12-12
First Named Inventor	Vinod Harimohan Kaushik
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	141062/1173-141

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	2	7647517	B2	2010-01-12	TSENG; Wen-Yu et al.	
	3	8615671	B2	2013-12-24	ROBLES; Raymond C. et al.	

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	2	20090185487	A1	2009-07-23	ADAR; Etai et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	141062/1173-141

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2014-12-12
	First Named Inventor	Vinod Harimohan Kaushik
	Art Unit	TBD
	Examiner Name	TBD
	Attorney Docket Number	141062/1173-141

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Signature	/Taylor M. Davenport/	Date (YYYY-MM-DD)	2014-12-12
Name/Print	Taylor M. Davenport	Registration Number	42466

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POWER SAVING TECHNIQUES IN COMPUTING DEVICES

PRIORITY CLAIMS

[0001] The present application claims priority to U.S. Provisional Patent Application Serial No. 61/916,498 filed on December 16, 2013 and entitled "POWER SAVING TECHNIQUES IN COMPUTING DEVICES," which is incorporated herein by reference in its entirety.

[0002] The present application also claims priority to U.S. Provisional Patent Application Serial No. 62/019,073 filed on June 30, 2014 and entitled "POWER SAVING TECHNIQUES IN COMPUTING DEVICES," which is incorporated herein by reference in its entirety.

BACKGROUND

I. Field of the Disclosure

[0003] The technology of the disclosure relates generally to power saving techniques in computing devices.

II. Background

[0004] Computing devices are common within modern society. Ranging from small, mobile computing devices, such as a smart phone or tablet, to large server farms with numerous blades and memory banks, these devices are expected to communicate across myriad networks while providing various other base functions. While desktop devices and servers are generally immune to concerns about power consumption, mobile devices constantly struggle to find a proper balance between available functions and battery life. That is, as more functions are provided, power consumption increases, and battery life is shortened. Servers may likewise have power consumption concerns when assembled in large server farms.

[0005] Concurrent with power consumption concerns, improvements in network communications have increased data rates. For example, copper wires have been replaced with higher bandwidth fiber optic cables, and cellular networks have evolved from early Advanced Mobile Phone System (AMPS) and Global System for Mobile Communications (GSM) protocols to 4G and Long Term Evolution (LTE) protocols

capable of supporting much higher data rates. As the data rates have increased, the need to be able to process these increased data rates within computing devices has also increased. Thus, earlier mobile computing devices may have had internal buses formed according to a High Speed Inter-Chip (HSIC) standard, universal serial bus (USB) standard (and particularly USB 2.0), or universal asynchronous receiver/transmitter (UART) standard. However, these buses do not support current data rates.

[0006] In response to the need for faster internal buses, the peripheral component interconnect express (PCIe) standard, as well as, later generations of USB (e.g., USB 3.0 and subsequent versions) have been adopted for some mobile computing devices. However, while PCIe and USB 3.0 can handle the high data rates currently being used, usage of such buses results in excessive power consumption and negatively impacts battery life by shortening the time between recharging events.

SUMMARY OF THE DISCLOSURE

[0007] Aspects disclosed in the detailed description include power saving techniques in computing devices. In particular, as data is received by a modem processor in a computing device, the data is held until the expiration of a modem timer. The data is then passed to an application processor in the computing device over a peripheral component interconnect express (PCIe) interconnectivity bus. On receipt of the data from the modem processor, the application processor sends data held by the application processor to the modem processor over the PCIe interconnectivity bus. The application processor also has an uplink timer. If no data is received from the modem processor before expiration of the uplink timer, the application processor sends any collected data to the modem processor at expiration of the uplink timer. However, if data is received from the modem processor, the uplink timer is reset. By holding or accumulating the data at a source processor in this fashion, unnecessary transitions between low power states and active states on the PCIe bus are reduced and power is conserved.

[0008] In an alternate aspect, instead of initiating data transfer based on the expiration of the downlink timer (with or without expiration of the uplink timer), accumulated data transfer may be initiated based on expiration of just an uplink

accumulation timer. The uplink accumulation timer may be within a host or a device associated with the interconnectivity bus.

[0009] In another alternate aspect, initiation of the data transfer may be based on reaching a predefined threshold for a byte accumulation limit counter. The byte accumulation limit counter is not mutually exclusive relative to the other counters and may operate as an override mechanism for one of the other accumulation timers. Use of such an override may be useful in situations where a sudden burst of data arrives that would exceed buffer space and/or bus bandwidth. Likewise, instead of a byte counter, a packet size counter or a "total number of packets" counter may be used to cover situations where numerous packets or a particularly large packet is delivered by the network.

[0010] In further aspects of the present disclosure, the timers may be overridden by other factors or parameters. Such an override is alluded to above with the byte accumulation limit counters and the total number of packets counter, which causes data transfers independently of the timers. Other parameters may also override the timers, such as the presence of low latency traffic (e.g., control messages), synchronizing the uplink and downlink data transfers, or low latency quality of service requirements. When such traffic is present, an interrupt or other command may be used to initiate data transfers before expiration of a timer. Still other factors may override the timers, such as an indication that a device or host is not in an automatic polling mode.

[0011] In this regard in one aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem timer. The mobile terminal also comprises a modem processor. The modem processor is configured to hold modem processor to application processor data until expiration of the modem timer. The mobile terminal also comprises an application processor. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The application processor is configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

[0012] In another aspect, a method of controlling power consumption in a computing device is disclosed. The method comprises holding data received by a

modem processor from a remote network until expiration of a downlink timer. The method also comprises passing the data received by the modem processor to an application processor over an interconnectivity bus. The method also comprises holding application data generated by an application associated with the application processor for until receipt of the data from the modem processor or expiration of an uplink timer, whichever occurs first.

[0013] In another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem processor. The mobile terminal also comprises an application timer. The mobile terminal also comprises an application processor. The application processor is configured to hold application processor to modem processor data until expiration of the application timer. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The modem processor is configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

[0014] In another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem byte accumulation limit counter. The mobile terminal also comprises a modem processor. The modem processor is configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter. The mobile terminal also comprises an application processor. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The application processor is configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

[0015] With regards to another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem packet counter. The mobile terminal also comprises a modem processor. The modem processor is configured to hold modem processor to

application processor data until a predefined threshold of packets has been reached by the modem packet counter. The mobile terminal also comprises an application processor. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The application processor is configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

[0016] In another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem processor. The mobile terminal also comprises an application byte counter. The mobile terminal also comprises an application processor. The application processor is configured to hold application processor to modem processor data until a predefined threshold of bytes has been reached by the application byte counter. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The modem processor is configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

[0017] In another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem processor and an application packet counter. The mobile terminal also comprises an application processor. The application processor is configured to hold application processor to modem processor data until a predefined threshold of packets has been reached by the application packet counter. The mobile terminal comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The modem processor is configured to hold the modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

[0018] With regards to another aspect, a method is disclosed. The method comprises starting an application timer at an application processor. The method also

comprises accumulating data at the application processor until expiration of the application timer. The method comprises sending the accumulated data from the application processor to a modem processor across an interconnectivity bus. The method further comprises holding modem processor data at the modem processor until receipt of the accumulated data from the application processor.

[0019] In another aspect, a mobile terminal is disclosed. The mobile terminal comprises a modem timer. The mobile terminal also comprises a modem processor. The modem processor is configured to hold modem processor to application processor data until expiration of the modem timer. The mobile terminal also comprises an application processor. The mobile terminal also comprises an interconnectivity bus communicatively coupling the application processor to the modem processor. The application processor is configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data.

BRIEF DESCRIPTION OF THE FIGURES

[0020] Figure 1A is a simplified view of a mobile computing device operating with remote networks;

[0021] Figure 1B is a simplified view of a mobile terminal operating with remote networks;

[0022] Figure 1C is an expanded block diagram view of the mobile terminal of Figure 1B with an interconnectivity bus illustrated;

[0023] Figure 2 is a block diagram of the mobile terminal of Figure 1B;

[0024] Figure 3 is an exemplary time versus link power graph in a conventional computing device;

[0025] Figure 4 is a flowchart of an exemplary process for achieving power savings in the mobile terminal of Figure 1B;

[0026] Figure 5 is an exemplary time versus link power graph in a mobile computing device using the process of Figure 4;

[0027] Figure 6 is a flowchart of another exemplary process for achieving power savings in the mobile computing device;

[0028] Figure 7 is an exemplary time versus link power graph in the mobile computing device using the process of Figure 6;

[0029] Figure 8 is a flowchart of an exemplary process that uses a byte counter to control data accumulation;

[0030] Figure 9 is a flowchart of an exemplary process that uses a packet counter to control data accumulation;

[0031] Figure 10 is a flowchart of a consolidated accumulation process with overrides illustrated from a downlink priority perspective;

[0032] Figure 11 is a continuation of the flowchart of Figure 10; and

[0033] Figure 12 is a simplified flowchart of a consolidated accumulation process with overrides illustrated from an uplink priority perspective.

DETAILED DESCRIPTION

[0034] With reference now to the drawing figures, several exemplary aspects of the present disclosure are described. The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects.

[0035] Aspects disclosed in the detailed description include power saving techniques in computing devices. In particular, as data is received by a modem processor in a computing device, the data is held until the expiration of a modem timer. The data is then passed to an application processor in the computing device over a peripheral component interconnect express (PCIe) interconnectivity bus. On receipt of the data from the modem processor, the application processor sends data held by the application processor to the modem processor over the PCIe interconnectivity bus. The application processor also has an uplink timer. If no data is received from the modem processor before expiration of the uplink timer, the application processor sends any collected data to the modem processor at expiration of the uplink timer. However, if data is received from the modem processor, the uplink timer is reset. By holding or accumulating the data at a source processor in this fashion, unnecessary transitions between low power states and active states on the PCIe bus are reduced and power is conserved.

[0036] In an alternate aspect, instead of initiating data transfer based on the expiration of the downlink timer (with or without expiration of the uplink timer), accumulated data transfer may be initiated based on expiration of just an uplink accumulation timer. The uplink accumulation timer may be within a host or a device associated with the interconnectivity bus.

[0037] In another alternate aspect, initiation of the data transfer may be based on reaching a predefined threshold for a byte accumulation limit counter. The byte accumulation limit counter is not mutually exclusive relative to the other counters and may operate as an override mechanism for one of the other accumulation timers. Use of such an override may be useful in situations where a sudden burst of data arrives that would exceed buffer space and/or bus bandwidth. Likewise, instead of a byte counter, a packet size counter or a "total number of packets" counter may be used to cover situations where numerous packets or a particularly a large packet is delivered by the network.

[0038] In further aspects of the present disclosure, the timers may be overridden by other factors or parameters. Such an override is alluded to above with the byte accumulation limit counters and the total number of packets counter, which causes data transfers independently of the timers. Other parameters may also override the timers, such as the presence of low latency traffic (e.g., control messages), synchronizing the uplink and downlink data transfers, or low latency quality of service requirements. When such traffic is present, an interrupt or other command may be used to initiate data transfers before expiration of a timer. Still other factors may override the timers, such as an indication that a device or host is not in an automatic polling mode.

[0039] While it is contemplated that the power saving techniques of the present disclosure are used in mobile terminals, such as smart phones or tablets, the present disclosure is not so limited. Accordingly, Figures 1A and 1B illustrate computing devices coupled to remote networks via modems that may implement exemplary aspects of the power saving techniques of the present disclosure. In this regard, Figure 1A illustrates a computing device 10 coupled to a network 12, which, in an exemplary aspect, is the internet. The computing device 10 may include a housing 14 with a central processing unit (CPU) (not illustrated), therein. A user may interact with the computing device 10 through a user interface formed from input/output elements such

as a monitor 16 (sometimes referred to as a display), a keyboard 18, and/or a mouse 20. In some aspects, the monitor 16 may be incorporated into the housing 14. While a keyboard 18 and mouse 20 are illustrated input devices, the monitor 16 may be a touchscreen display, which may supplement or replace the keyboard 18 and mouse 20 as an input device. Other input/output devices may also be present as is well understood in conjunction with desktop or laptop style computing devices. While not illustrated in Figure 1A, the housing 14 may also include a modem, therein. The modem may be positioned on a network interface card (NIC), as is well understood. Likewise, a router and/or an additional modem may be external to the housing 14. For example, the computing device 10 may couple to the network 12 through a router and a cable modem, as is well understood. However, even where such external routers and modems are present, the computing device 10 is likely to have an internal modem to effectuate communication with such external routers and modems.

[0040] In addition to the computing device 10, exemplary aspects of the present disclosure may also be implemented on a mobile terminal, which is a form of computing device as that term is used herein. In this regard, an exemplary aspect of a mobile terminal 22 is illustrated in Figure 1B. The mobile terminal 22 may be a smart phone, such as a SAMSUNG GALAXY™ or APPLE iPHONE®. Instead of a smart phone, the mobile terminal 22 may be a cellular telephone, a tablet, a laptop, or other mobile computing device. The mobile terminal 22 may communicate with a remote antenna 24 associated with a base station (BS) 26. The BS 26 may communicate with the public land mobile network (PLMN) 28, the public switched telephone network (PSTN, not shown), or a network 12 (e.g., the internet), similar to the network 12 in Figure 1A. It is also possible that the PLMN 28 communicates with the internet (e.g., the network 12) either directly or through an intervening network (e.g., the PSTN). It should be appreciated that most contemporary mobile terminals 22 allow for various types of communication with elements of the network 12. For example, streaming audio, streaming video, and/or web browsing are all common functions on most contemporary mobile terminals 22. Such functions are enabled through applications stored in the memory of the mobile terminal 22 and using the wireless transceiver of the mobile terminal 22.

[0041] To effectuate functions, such as streaming video, data arrives from the remote antenna 24 at an antenna 30 of the mobile terminal 22, as illustrated in Figure 1C. The data is initially processed at a mobile device modem (MDM) 32 of the mobile terminal 22 and passed to an application processor 34 by an interconnectivity bus 36. In this context, the application processor 34 may be a host, and the MDM 32 may be a device as those terms are used in the PCIe standard. While exemplary aspects contemplate operating over a PCIe-compliant interconnectivity bus 36, it is possible that the interconnectivity bus 36 may comply with High Speed Interconnect (HSIC), Universal Asynchronous Receiver/Transmitter (UART), universal serial bus (USB), or the like.

[0042] A more detailed depiction of the components of the mobile terminal 22 is provided with reference to Figure 2. In this regard, a block diagram of some of the elements of the mobile terminal 22 of Figure 1B is illustrated. The mobile terminal 22 may include a receiver path 38, a transmitter path 40, the antenna 30 (mentioned above with reference to Figure 1C), a switch 42, a modem processor 44, and the application processor 34 (also introduced above in reference to Figure 1C). Optionally, a separate control system (not shown) may also be present with a CPU as is well understood. The application processor 34 and the modem processor 44 are connected by the interconnectivity bus 36. The application processor 34 and/or the control system (if present) may interoperate with a user interface 46 and memory 48 with software 50 stored therein.

[0043] The receiver path 38 receives information bearing radio frequency (RF) signals from one or more remote transmitters provided by a base station (e.g., the BS 26 of Figure 1B). A low noise amplifier (not shown) amplifies the signal. A filter (not shown) minimizes broadband interference in the received signal. Down conversion and digitization circuitry (not shown) down converts the filtered, received signal to an intermediate or baseband frequency signal. The baseband frequency signal is then digitized into one or more digital streams. The receiver path 38 typically uses one or more mixing frequencies generated by the frequency synthesizer. The modem processor 44 may include a base band processor (BBP) (not shown) that processes the digitized received signal to extract the information or data bits conveyed in the signal. As such, the BBP is typically implemented in one or more digital signal processors

(DSPs) within the modem processor 44 or as a separate integrated circuit (IC) as needed or desired.

[0044] With continued reference to Figure 2, on the transmit side, the modem processor 44 receives digitized data, which may represent voice, data, or control information, from the application processor 34, which it encodes for transmission. The encoded data is output to the transmitter path 40, where it is used by a modulator (not shown) to modulate a carrier signal at a desired transmit frequency. An RF power amplifier (not shown) amplifies the modulated carrier signal to a level appropriate for transmission, and delivers the amplified and modulated carrier signal to the antenna 30 through the switch 42. Collectively, the modem processor 44, the receiver path 38, and the transmitter path 40 form the MDM 32 of Figure 1C (sometimes also referred to as a wireless modem). While the MDM 32 is specifically described with relation to the RF signals associated with a cellular signal, the present disclosure is not so limited. For example, a wireless modem using other wireless protocols may also benefit from inclusion of aspects of the present disclosure. Thus, modems operating according to standards such as BLUETOOTH®, the various IEEE 802.11 standards, Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Long Term Evolution (LTE), and other wireless protocols may all use aspects of the present disclosure.

[0045] With continued reference to Figure 2, a user may interact with the mobile terminal 22 via the user interface 46, such as a microphone, a speaker, a keypad, and a display. Audio information encoded in the received signal is recovered by the BBP, and converted into an analog signal suitable for driving the speaker. The keypad and display enable the user to interact with the mobile terminal 22. For example, the keypad and display may enable the user to input numbers to be dialed, access address book information, or the like, as well as monitor call progress information. The memory 48 may have the software 50 therein as noted above, which may effectuate exemplary aspects of the present disclosure.

[0046] In conventional mobile terminals that have a PCIe interconnectivity bus (i.e., the interconnectivity bus 36), the PCIe standard allows the interconnectivity bus 36 to be placed into a sleep mode. While placing the interconnectivity bus 36 in a sleep mode generally saves power, such sleep modes do have a drawback in that they consume

relatively large amounts of power as they transition out of the sleep mode. This power consumption is exacerbated because of the asynchronous nature of the PCIe interconnectivity bus 36. That is, first data may arrive at the modem processor 44 for transmission to the application processor 34 at a time different than when the second data is ready to pass from the application processor 34 to the modem processor 44. This problem is not unique to the PCIe interconnectivity bus 36.

[0047] Figure 3 illustrates a time versus link power graph 52 that highlights how downlink data 54 may have a different transmission time than uplink data 56 within a given time slot 58. In particular, the interconnectivity bus 36 (Figure 2) begins in a sleep or low power mode and transitions up to an active power mode by transition 60 so that the downlink data 54 may be transmitted to the application processor 34. However, the downlink data 54 may not occupy the entirety of the time slot 58, and the interconnectivity bus 36 may return to a low power state. However, subsequently, but still within the same time slot 58, the uplink data 56 from the application processor 34 is sent to the modem processor 44. Accordingly, the interconnectivity bus 36 is again transitioned from the low power state to the active power state by a second transition 62. In an exemplary aspect, the time slot 58 is approximately one millisecond long. Thus, if two transitions (i.e., 60, 62) from low power to active power occur every time slot 58, then thousands of transitions 60, 62 occur every second. Thousands of transitions 60, 62 consume substantial amounts of power and reduce the battery life of the mobile terminal 22.

[0048] Exemplary aspects of the present disclosure reduce the number of transitions (i.e., 60, 62) from low power to active power by synchronizing packet transmission from the modem processor 44 and the application processor 34, which in turn allows the link to be maintained in a low power mode more efficiently since the communication on the link is consolidated to eliminate the second power state transition. In an exemplary aspect, the data (i.e., the modem data) from the modem processor 44 transmits first, and the data (i.e., the application data) from the application processor 34 is sent after arrival of the modem data and before the interconnectivity bus 36 can return to the low power state. The synchronization is done through the use of timers at the modem processor 44 and the application processor 34. The timers may be longer than a time slot 58 of the interconnectivity bus 36.

[0049] In a first exemplary aspect, the timer on the application processor 34 is longer than the timer on the modem processor 44. The accumulation may be done on a per logical channel basis. The timer may be configurable by the application processor 34 using a mechanism suitable to the interconnectivity bus 36. For example, on a fusion device using a modem host interface (MHI) over PCIe, the timer is maintained for every inbound MHI channel and the time value used by the timers shall be configured via a MHI command message or a PCIe memory mapped input/output (MMIO) device configuration register exposed via a base address register (BAR). The BAR is a PCIe standard defined mechanism by which a host maps the registers of a device into its virtual address map. For more information about MHI, the interested reader is referred to U.S. Patent Application Serial Number 14/163,846, filed January 24, 2013, which is herein incorporated by reference in its entirety. In other exemplary aspects, the timer on the modem processor 44 is longer than the timer on the application processor 34. In still other exemplary aspects, counters may be used in place of timers. The counters may be bit counters, packet counters, packet size counters, or the like. In other exemplary aspects, use of such alternate counters may be combined with the timers. In still other exemplary aspects, other override criteria may allow for data to be sent before timer or counter expiration so as to reduce latency and/or satisfy the quality of service requirements. The present disclosure steps through each of these aspects in turn, beginning with the situation where there are two timers, and the application processor 34 has a timer that is longer than the timer of the modem processor 44.

[0050] In this regard, Figure 4 illustrates an exemplary power saving process 70. The process 70 begins with the interconnectivity bus 36 in a low power state (block 72). The modem timer and the application timer are started (block 74). The timers may be software stores in the modem processor 44 and the application processor 34 or may be physical elements, as desired. Data is generated by the application processor 34 and data is received from the network 12 by the modem processor 44. The application data is held at the application processor 34 (block 76), and the modem data is held at the modem processor 44 (block 78) while the timers are running. As noted above, in an exemplary aspect, the time slot 58 of the interconnectivity bus 36 is one millisecond. In such an aspect, the modem timer may be approximately two to six milliseconds, and the application timer is three to seven milliseconds, or at least longer than the modem timer.

The modem timer expires (block 80). If modem data is present, the modem data is released by the modem processor 44 through the interconnectivity bus 36 to the application processor 34 (block 82).

[0051] The mechanism for data transfer may be initiated and controlled by the modem processor 44 (i.e., the device). For example, on a fusion device using MHI over PCIe, the modem processor 44 may poll (read) the MHI channel Context Write Pointer to determine data buffers where downlink packets can be transferred. The application processor 34 updates the channel context data structure's Context Write Pointer field to point to the data transfer descriptors without ringing an Inbound channel doorbell. The modem processor 44 may poll for updates on the Context Write Pointer field as necessitated by downlink traffic. When the modem processor 44 runs out of buffers, i.e., a transfer ring is empty, and no buffers are present to transfer downlink data, the modem processor 44 may generate an event (e.g., an "out-of-buffer") notification to the application processor 34, followed by an interrupt. Upon receiving the event notification from the modem processor 44, the application processor 34 shall provide data buffers by updating the channel Context Write Pointer and shall ring the Inbound channel doorbell.

[0052] After arrival of the modem data at the application processor 34, the application processor 34 releases any application data that has been held at the application processor 34 and resets the application timer (block 84). Note that the application timer can run on the modem processor 44 or the application processor 34. As an alternative, the modem processor 44 may continue to pull the uplink data 56 from the application processor 34 until it detects no further downlink data 54 activity. That is, the modem processor 44 may intersperse pulling the uplink data 56 while receiving the downlink data 54. If, however, no modem data is present at the modem processor 44 when the modem timer expires, the application timer continues (i.e., another millisecond) (block 86). At the expiration of the application timer, the application processor 34 sends any held data to the modem processor 44 through the interconnectivity bus 36 (block 88). The process then repeats by starting over (block 90).

[0053] As noted above, the uplink timer (i.e., the application timer) is, in an exemplary aspect, designed to be longer than the downlink timer (i.e., the modem timer)

to increase the uplink/downlink synchronization whenever the downlink timer expires. While holding data for an extra time slot adds some latency, the brief amount added is readily absorbed by the application processor 34. Likewise, this latency is considered acceptable for the power savings. For example, by making the period of the modem timer twice the period of the time slot 58, the number of low power to active power transitions is potentially halved. Likewise, by making the period of the application timer six times the period of the time slot 58, the chance of being able to "piggyback" onto the active power state of the interconnectivity bus 36 caused by the modem data is increased, but still frequent enough that any uplink data 56 will still be sent in a timely fashion even if there is no downlink data 54 to trigger releasing the uplink data 56. Similar logic can be extended to synchronize traffic from multiple processors over the data link. In an exemplary aspect, the other processors may each have timer values higher (i.e., longer) than that of the downlink timer, and the processors can exchange their data availability information so that traffic on one processor can trigger the data transfer on other processors if there is data available to transfer.

[0054] Figure 5 illustrates a graph 100 where the uplink data 56 follows the downlink data 54 during an active period 102 of the interconnectivity bus 36 (Figure 2). As illustrated, there is only one transition 104 from low power to active power per time slot 58. Thus, by consolidating the data into a single active period 102, the overall time that is spent in low power may be increased, thus resulting in power savings. Additionally, power spent transitioning from a low power to active power state is reduced by the elimination of the second transition 62.

[0055] While it is conceivable that the uplink data 56 could be sent before the downlink data 54 (i.e., the application timer is shorter than the modem timer), such is generally not considered optimal because there are usually far more downlink packets than uplink packets. If this aspect is used, the application processor 34 may buffer uplink data packets into local memory prior to initiating transfer to the modem processor 44. These accumulated packets are controlled via an uplink accumulation timer. If there are plural channels, then a timer may be applied to each channel independently. When the application processor 34 is unable to use or does not have an uplink timer, the modem processor 44 may be able to instantiate an uplink timer, and

upon expiry of the uplink timer, will poll data from the application processor 34. This exemplary aspect is explained in greater detail below with reference to Figures 6 and 7.

[0056] In this regard, Figure 6 illustrates an exemplary power saving process 110. The process 110 begins with the interconnectivity bus 36 in a low power state (block 112). The modem timer and the application timer are started (block 114). The timers may be software stored in the modem processor 44 and the application processor 34 or may be physical elements as desired. Data is generated by the application processor 34 and data is received from the network 12 by the modem processor 44. The application data is held at the application processor 34 (block 116), and the modem data is held at the modem processor 44 (block 118) while the timers are running. As noted above, in an exemplary aspect, the time slot 58 of the interconnectivity bus 36 is one millisecond. In such an aspect, the application timer may be approximately two milliseconds, and the modem timer is three milliseconds, or at least longer than the application timer. The application timer expires (block 120). If application data is present, the application data is released by the application processor 34 through the interconnectivity bus 36 to the modem processor 44 (block 122).

[0057] After arrival of the application data at the modem processor 44, the modem processor 44 releases any modem data that has been held at the modem processor 44 and resets the modem timer (block 124). Note that the application timer can run on the modem processor 44 or the application processor 34. Likewise, the modem timer can run on the modem processor 44 or the application processor 34.

[0058] With continued reference to Figure 6, if no application data is present at the application processor 34 when the application timer expires, the modem timer continues (i.e., another millisecond) (block 126). At the expiration of the modem timer, the modem processor 44 sends any held data to the application processor 34 through the interconnectivity bus 36 (block 128). The process then repeats by starting over (block 130).

[0059] As noted above, in this exemplary aspect, the uplink timer (i.e., the application timer) is, in an exemplary aspect, designed to be shorter than the downlink timer (i.e., the modem timer). While holding data for an extra time slot 58 adds some latency, the brief amount added is readily absorbed by the application processor 34. Likewise, this latency is considered acceptable for the power savings. For example, by

making the period of the application timer twice the period of the time slot 58, the number of low power to active power transitions is lowered. Likewise, by making the period of the modem timer six times the period of the time slot 58, the chance of being able to "piggyback" onto the active power state of the interconnectivity bus 36 caused by the application data is increased, but still frequent enough that any downlink data 54 will still be sent in a timely fashion even if there is no uplink data 56 to trigger releasing the downlink data 54. Similar logic can be extended to synchronize traffic from multiple processors over the data link. In an exemplary aspect, the other processors may each have timer values higher (i.e., longer) than that of the uplink timer and the processors can exchange their data availability information so that traffic on one processor can trigger the data transfer on other processors if there is data available to transfer.

[0060] Figure 7 illustrates a graph 140 where the uplink data 56 precedes the downlink data 54 during an active period 142 of the interconnectivity bus 36. As illustrated, there is only one transition 144 from low power to active power per time slot 58. Thus, by consolidating the data into a single active period 142, the overall time that is spent in low power may be increased, thus resulting in power savings. Additionally, power spent transitioning from a low power to active power state is reduced by the elimination of the second transition 62.

[0061] In an exemplary aspect, the modem processor 44 may override and choose the minima from all configured values of each of the configurable parameters (like downlink or uplink accumulation timers, byte threshold, number of packets threshold, size of packet threshold, or the like) or downlink accumulation expiry timer values (e.g., from among the various channels) as the effective downlink accumulation timer expiry value. Intelligent modem processors 44 may also dynamically override or alter the downlink accumulation timer value depending on the downlink traffic pattern, and/or may adjust the downlink accumulation timer to achieve a desired quality of service (QoS) for data and/or to control traffic. A change of configuration can be triggered/controlled by the application processor 44 or any other processor in the system as well, via MHI control or QMI signaling (such as, for inter process signaling).

[0062] In addition to, or in place of, downlink and uplink timers, a byte accumulation limit counter may also be used by the modem processor 44 for downlink

traffic and the application processor 34 for uplink traffic. This aspect may be advantageous in situations where there is a sudden burst of data pushed by the network or application. Note that this aspect is not mutually exclusive and may be implemented as an override mechanism for either downlink or uplink timers. For example, if the downlink accumulation timer is set relatively high to conserve power, a sudden burst of data may exceed the buffer capacity of the modem processor 44, or if allowed to accumulate in memory of the modem processor 44, this burst of data may exceed bus bandwidth allocations on the application processor 34. The application processor 34 can determine and configure the maximum byte accumulation limit based on its bus bandwidth budget, and/or buffer size reserved for downlink data transfer. The modem processor 44 can also choose an internal byte accumulation limit based on the size of downlink buffer, and/or interconnect link data throughput. With the byte accumulation limit counters, the modem processor 44 can initiate downlink data transfer to the application processor 34 prior to downlink accumulation timer expiry, if and when the buffered data size exceeds the byte accumulation limit counter. Since both the modem processor 44 and the application processor 34 may have independent recommendations for byte accumulation limit counter, the modem processor 44 may select the minima of these two values to be the effective byte accumulation limit. Similar parameters may be maintained in the application processor 34 to trigger the uplink data 56 transfer immediately (i.e., overriding the uplink accumulation timer).

[0063] Instead of, or in addition to the byte accumulation limit counter, a number of packets limit counter may be used. In an exemplary aspect, the packet number limit counter may be of similar design, and can be employed to add number of packet counter limits instead of byte limits to cover cases where a large number of packets are delivered by the network or an application. Again, such a packet limit counter may also be present or associated with the application processor 34 or the modem processor 44. Note, that the accumulation timers (uplink and/or downlink) and other configuration parameters like the number of accumulated packets threshold, accumulated bytes threshold, and the like, may be a function of LTE, HSPA, GERAN, or the like.

[0064] In still another exemplary aspect, the modem processor 44 or the application processor 34 may disable downlink or uplink accumulation in cases where there is a necessity to expedite message transfer, for example control messages (like flow control)

or high QoS data traffic or low latency traffic, as determined by the modem processor 44 or the application processor 34. Latency introduced by accumulation may not be tolerable for these traffic classes.

[0065] Returning to the data accumulation based on amounts of data instead of a strict process, Figures 8 and 9 illustrate two exemplary aspects. In this regard, Figure 8 illustrates a process 150 illustrating a byte counter process. In particular, the process 150 begins with the interconnectivity bus 36 in a low power state (block 152). The process 150 starts a modem byte counter and an application byte counter (block 154). Data is held at the application processor 34 (block 156) and the modem processor 44 (block 158). A control system determines if the modem byte counter has exceeded a predefined threshold (block 160) based on the amount of data that has been held or accumulated at the modem processor 44.

[0066] With continued reference to Figure 8, if the answer to block 160 is yes, then data is sent from the modem processor 44 to the application processor 34 (block 162). After receipt of the data from the modem processor 44, the application processor 34 sends data (if any) that has accumulated at the application processor 34 to the modem processor 44 (block 164). Having cleared the accumulated data at both the modem processor 44 and the application processor 34, the process starts over (block 166).

[0067] With continued reference to Figure 8, if the answer to block 160 is no, the control system determines if the data at the application byte counter has exceeded a predefined threshold (block 168). If the answer to block 168 is no, the process 150 returns to block 156 and data continues to be held until a byte counter threshold is exceeded. If, however, the answer to block 168 is yes, then the data is sent from the application processor 34 to the modem processor 44 (block 170). After receipt of the data from the application processor 34, the modem processor 44 sends data (if any) to the application processor 34 (block 172). Having cleared the accumulated data at both the modem processor 44 and the application processor 34, the process 150 starts over (block 166).

[0068] While a byte counter may be effective in managing latency, another exemplary aspect uses a packet counter. In this regard, Figure 9 illustrates a process 180 illustrating a byte counter process. In particular, the process 180 begins with the interconnectivity bus 36 in a low power state (block 182). The process 180 starts a

modem packet counter and an application packet counter (block 184). Data is held at the application processor 34 (block 186) and the modem processor 44 (block 188). A control system determines if the modem packet counter has exceeded a predefined threshold (block 190) based on the number of packets held or accumulated at the modem processor 44.

[0069] With continued reference to Figure 9, if the answer to block 190 is yes, then data is sent from the modem processor 44 to the application processor 34 (block 192). After receipt of the packets from the modem processor 44, the application processor 34 sends data (if any) that has accumulated at the application processor 34 to the modem processor 44 (block 194). Having cleared the accumulated packets at both the modem processor 44 and the application processor 34, the process 180 starts over (block 196).

[0070] With continued reference to Figure 9, if the answer to block 190 is no, the control system determines if the number of packets at the application packet counter has exceeded a predefined threshold (block 198). If the answer to block 198 is no, the process 180 returns to block 186 and data continues to be held until a packet counter threshold is exceeded. If, however, the answer to block 198 is yes, then the data is sent from the application processor 34 to the modem processor 44 (block 200). After receipt of the packets from the application processor 34, the modem processor 44 sends data (if any) to the application processor 34 (block 202). Having cleared the accumulated packets at both the modem processor 44 and the application processor 34, the process 180 starts over (block 196).

[0071] A similar process may be used, where instead of determining if a particular number of bytes or packets have been accumulated, the control system evaluates a size of packets or whether the system is running low in memory. Likewise, it should be appreciated that certain priority data (e.g., a control signal or other data requiring low latency) may be associated with a flag or other indicator that overrides the timers and/or counters of the present disclosure.

[0072] As noted above, it should be appreciated that the aspects of the present disclosure are not mutually exclusive and can be combined. The combinations are myriad in that a timer may be used at the application processor 34 with a byte counter at the modem processor 44 (or vice versa), the modem processor 44 works with a timer and a byte counter, while the application processor 34 just has a timer, and so on. In

this regard, Figures 10-12 are provided that illustrate how the timers and data accumulation counters may interoperate. That is, Figures 10 and 11 illustrate how the downlink timer (whether in the modem processor 44 or the application processor 34) is used as the basis for data transmission (e.g., as illustrated in Figures 4 and 5), may be combined with the data accumulation counters, and is further modified by a high priority data override. Figure 12 illustrates a simplified process in which the uplink timer combined with the data accumulation counters is used as the basis for data transmission (e.g., as illustrated in Figures 6 and 7), modified by the data overrides.

[0073] In this regard, Figures 10 and 11 illustrate a combined process 210 that begins at start (block 212). The process 210 continues with the arrival of downlink (DL) data (e.g., a packet) (block 214). The control system evaluates if there is any priority data, control messages, and/or other data that requires low latency (block 216). If the answer to block 216 is no, then the control system determines if a byte threshold has been crossed (i.e., are there more than the threshold worth of bytes in the accumulator) (block 218). If the answer to block 218 is no, then the control system determines if a number of packets threshold has been crossed (i.e., there are more than the threshold worth of packets in the accumulator) (block 220). If the answer to block 220 is no, then the control system determines if the system is running low in memory (block 222). If the answer to block 222 is no, then the control system ascertains if the downlink accumulation timer is running (block 224). If the answer to block 224 is yes, then the downlink data continues to accumulate and no data transfer is initiated over the link (block 226).

[0074] With continued reference to Figure 10, if, however, the answer to block 224 is no, the downlink timer has expired, or if any of the overrides from block 216, 218, 220, or 222 has been answered affirmatively, then the process 210 starts transfer of the accumulated data (including the current packet) over the link from the modem processor 44 (also sometimes referred to as modem (44) in the Figures) to the application processor 34 (also sometimes referred to as AP (34) in the Figures) (block 230). The control system starts or restarts the downlink accumulation timer and sets the downlink accumulation timer to running (block 232). The control system determines if the modem processor 44 is in an uplink (UL) polling mode (block 234). If the answer to block 234 is no, then there is no uplink transfer (block 236). If, however, the modem

processor 44 is polling the uplink device, then, based on that polling, the control system determines if there is pending uplink data from the application processor 34 (block 238). If there is pending data (i.e., the answer to block 238 is yes), then the application processor 34 starts data transfer to the modem processor 44 (block 240). Once the data transfer is finished, or if there was no data at block 238, the control system restarts the uplink accumulation timer (block 242) and the process 210 returns to start 212.

[0075] With continued reference to Figure 10, after block 226, the control system determines if the downlink timer has expired (block 244). If the answer to block 244 is no, the control system determines if a new packet has arrived (block 246). If the answer to block 246 is no, then the process 210 returns to block 244. If a new packet has arrived, the process 210 returns to the start 212. If the answer to block 244 is yes, the downlink timer has expired, the control system knows the downlink accumulation timer has expired (block 248). At expiration of the downlink timer, the control system determines if there is any pending accumulated downlink data (block 250). If there is data at block 250, then the data is transferred at block 230. If there is no data, then the downlink accumulation timer is set to "not running" (block 252) and the process 210 goes to Figure 11, element C. It should be appreciated that blocks 216, 218, 220, and 222 are optional.

[0076] With reference to Figure 11, the process 210 may continue from block 252. At this point, the uplink accumulation timer has expired (block 254). The uplink accumulation timer will expire if there is no downlink data since the uplink timer was restarted. The control system determines if there is any pending uplink data from the application processor 34 (block 256). If the answer to block 256 is yes, then the application processor 34 starts the data transfer over the link from the application processor 34 to the modem processor 44 (block 258). The control system then restarts the uplink accumulation timer (block 260). If, however, the answer to block 256 is no, there is no data, the control system sends an event to the application processor 34 indicating the modem processor 44 is expecting a doorbell/interrupt for any pending or next packet submission (block 262). That is, since there has been no data from the application processor 34 to the modem processor 44 since the previous poll time, then the modem processor 44 may go into an interrupt mode for uplink data and the modem processor 44 would expect the application processor 34 to send an interrupt whenever

there was data pending at the application processor 34. The control system then changes the state internally to reflect the same (block 264).

[0077] With continued reference to Figure 11, the modem processor 44 receives an interrupt or other indication from the application processor 34 indicating pending data in the transfer ring (block 266). The control system then restarts the uplink accumulation timer and changes the state to indicate the uplink polling mode (block 268). All the uplink data is processed (block 270) and the process 210 starts over.

[0078] In another alternate aspect, there may be situations where the buffers of the application processor 34 may be full and there is no room for data from the modem processor 44. In such an event, the application processor 34 may so inform the modem processor 44, and the modem processor 44 may send an event to the application processor 34 to provide an interrupt signal to the modem processor 44 when there are free buffers.

[0079] Figure 12 is similar to Figures 10 and 11, in that it illustrates how overrides and data counters may be used in conjunction with an accumulation timer, but a process 280 of Figure 12 assumes that the uplink timer is shorter than the downlink timer (e.g., analogous to the aspect illustrated in Figures 6 and 7). The process 280 begins at start (block 282). The process 280 continues with the arrival of uplink (UL) data (e.g., a packet) (block 284). The control system evaluates if there is any priority data, control messages, and/or other data that requires low latency (block 286). If the answer to block 286 is no, then the control system determines if a byte threshold has been crossed (i.e., are there more than the threshold worth of bytes in the accumulator) (block 288). If the answer to block 288 is no, then the control system determines if a number of packets threshold has been crossed (i.e., there are more than the threshold worth of packets in the accumulator) (block 290). If the answer to block 290 is no, then the control system determines if the system is running low in memory (block 292). If the answer to block 292 is no, then the control system ascertains if the device is in an uplink polling mode (block 294). If the answer to block 294 is yes, the device is in the polling mode, then the application processor 34 updates the internal data structure/context array with uplink data packet information that the device can pull and update write pointers accordingly (block 296).

[0080] With continued reference to Figure 12, if, however, the answer to block 294 is no, the device is not in an uplink polling mode, or if any of the overrides from blocks 286, 288, 290, or 292 has been answered affirmatively, then the application processor 34 updates the internal data structure/context array with uplink data packet information that the device can pull and update write pointers accordingly (block 298). The application processor 34 then rings the doorbell or otherwise interrupts the device to indicate the availability of uplink data (block 300). The application processor 34 then sets the device state to the polling state (not the doorbell/event/interrupt mode) (block 302), and the process repeats.

[0081] It should be appreciated that similar processes may be performed where both timers are in the application processor 34 or the modem processor 44 or are split between the respective processors 34, 44. Likewise, once a timer has expired, data can be pulled or pushed across the interconnectivity bus 36 based on polling, setting doorbell registers, or other technique.

[0082] Those of skill in the art will further appreciate that the various illustrative logical blocks, modules, circuits, and algorithms described in connection with the aspects disclosed herein may be implemented as electronic hardware, instructions stored in memory or in another computer-readable medium and executed by a processor or other processing device, or combinations of both. The devices described herein may be employed in any circuit, hardware component, IC, or IC chip, as examples. Memory disclosed herein may be any type and size of memory and may be configured to store any type of information desired. To clearly illustrate this interchangeability, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. How such functionality is implemented depends upon the particular application, design choices, and/or design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0083] The various illustrative logical blocks, modules, and circuits described in connection with the aspects disclosed herein may be implemented or performed with a processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit

(ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0084] The aspects disclosed herein may be embodied in hardware and in instructions that are stored in hardware, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a remote station. In the alternative, the processor and the storage medium may reside as discrete components in a remote station, base station, or server.

[0085] It is also noted that the operational steps described in any of the exemplary aspects herein are described to provide examples and discussion. The operations described may be performed in numerous different sequences other than the illustrated sequences. Furthermore, operations described in a single operational step may actually be performed in a number of different steps. Additionally, one or more operational steps discussed in the exemplary aspects may be combined. It is to be understood that the operational steps illustrated in the flow chart diagrams may be subject to numerous different modifications as will be readily apparent to one of skill in the art. Those of skill in the art will also understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents,

electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0086] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and designs described herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

2. The mobile terminal of claim 1, wherein the interconnectivity bus comprises a peripheral component interconnect (PCI) compliant bus.

3. The mobile terminal of claim 2, wherein the PCI compliant bus comprises a PCI express (PCIe) bus.

4. The mobile terminal of claim 1, wherein the application processor includes an uplink timer and the uplink timer has a period longer than a period of the modem timer.

5. The mobile terminal of claim 1, wherein the modem timer is implemented in software.

6. The mobile terminal of claim 1, wherein the modem timer has a period of approximately six (6) milliseconds.

7. The mobile terminal of claim 4, wherein the application processor is configured to hold the application processor to modem processor data until receipt of the modem

processor to application processor data from the modem processor or expiration of the uplink timer having a period longer than a period of the modem timer, whichever occurs first.

8. The mobile terminal of claim 1, wherein the modem processor comprises the modem timer.

9. The mobile terminal of claim 1, wherein the application processor comprises the modem timer.

10. The mobile terminal of claim 1, further comprising an application timer, and wherein the modem processor is configured to instruct the application processor to send an interrupt if no data is received within one time slot of the application timer.

11. The mobile terminal of claim 1, further comprising a byte accumulation limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the byte accumulation limit counter is exceeded.

12. The mobile terminal of claim 1, further comprising a packet number limit counter associated with the modem processor, the modem processor configured to send data to the application processor if a threshold associated with the packet number limit counter is exceeded.

13. The mobile terminal of claim 1, wherein the modem processor is configured to determine if held data comprises a control packet and send such control packet before expiration of the modem timer.

14. The mobile terminal of claim 3, wherein the modem processor further comprises an application timer, and the modem processor is configured to pull data from the application processor on receipt of the modem processor to application processor data or expiration of the application timer.

15. A method of controlling power consumption in a computing device, comprising:

holding data received by a modem processor from a remote network until expiration of a downlink timer;

passing the data received by the modem processor to an application processor over an interconnectivity bus; and

holding application data generated by an application associated with the application processor until receipt of the data from the modem processor or expiration of an uplink timer, whichever occurs first.

16. The method of claim 15, wherein passing the data comprises passing the data over a peripheral component interface (PCI) compliant bus.

17. The method of claim 15, wherein a period of the downlink timer comprises six (6) milliseconds.

18. The method of claim 15, wherein a period of the uplink timer comprises seven (7) milliseconds.

19. The method of claim 15, further comprising providing an override capability based on one of accumulated packet size, accumulated packet count, accumulated byte count, quality of service requirement, and control message status.

20. A mobile terminal comprising:

a modem processor;

an application timer;

an application processor, the application processor configured to hold application processor to modem processor data until expiration of the application timer;

an intereonnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem

processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

21. The mobile terminal of claim 20, wherein the application processor comprises the application timer.

22. The mobile terminal of claim 20, wherein the modem processor comprises the application timer.

23. The mobile terminal of claim 20, further comprising a byte counter counting bytes at the modem processor.

24. A mobile terminal comprising:

a modem byte accumulation limit counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

25. A mobile terminal comprising:

a modem packet counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of packets has been reached by the modem packet counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus.

26. A mobile terminal comprising:

a modem processor;

an application byte counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of bytes has been reached by the application byte counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

27. A mobile terminal comprising:

a modem processor;

an application packet counter;

an application processor, the application processor configured to hold application processor to modem processor data until a predefined threshold of packets has been reached by the application packet counter;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the modem processor configured to hold modem processor to application processor data until receipt of the application processor to modem processor data from the application processor through the interconnectivity bus after which the modem processor to application processor data is sent to the application processor through the interconnectivity bus.

28. A method comprising:

starting an application timer at an application processor;

accumulating data at the application processor until expiration of the application timer;

sending the accumulated data from the application processor to a modem processor across an interconnectivity bus; and

holding modem processor data at the modem processor until receipt of the accumulated data from the application processor.

29. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data.

ABSTRACT

Aspects disclosed in the detailed description include power saving techniques in computing devices. In particular, as data is received by a modem processor in a computing device, the data is held until the expiration of a modem timer. The data is then passed to an application processor in the computing device over a peripheral component interconnect express (PCIe) interconnectivity bus. On receipt of the data from the modem processor, the application processor sends data held by the application processor to the modem processor over the PCIe interconnectivity bus. The application processor also has an uplink timer. If no data is received from the modem processor before expiration of the uplink timer, the application processor sends any collected data to the modem processor at expiration of the uplink timer. However, if data is received from the modem processor, the uplink timer is reset.

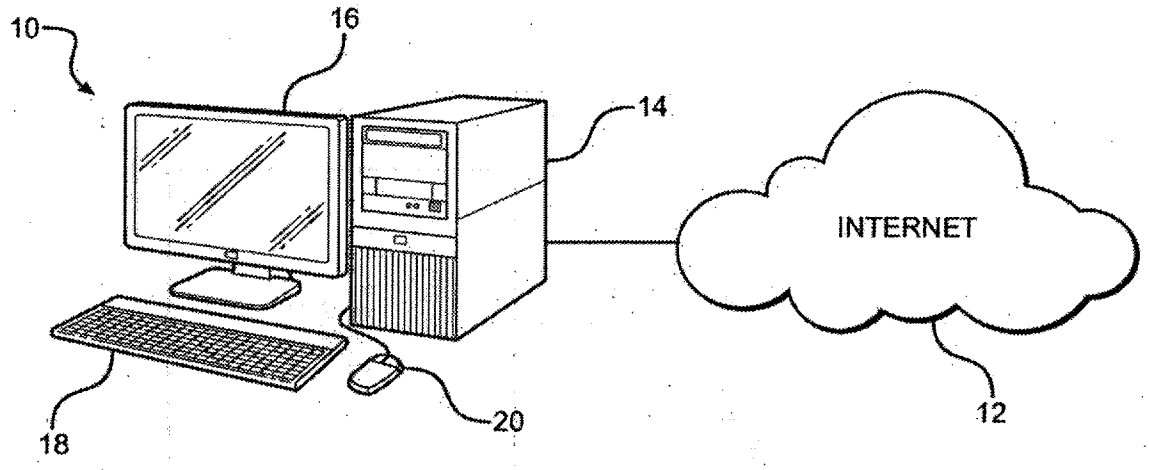


FIG. 1A

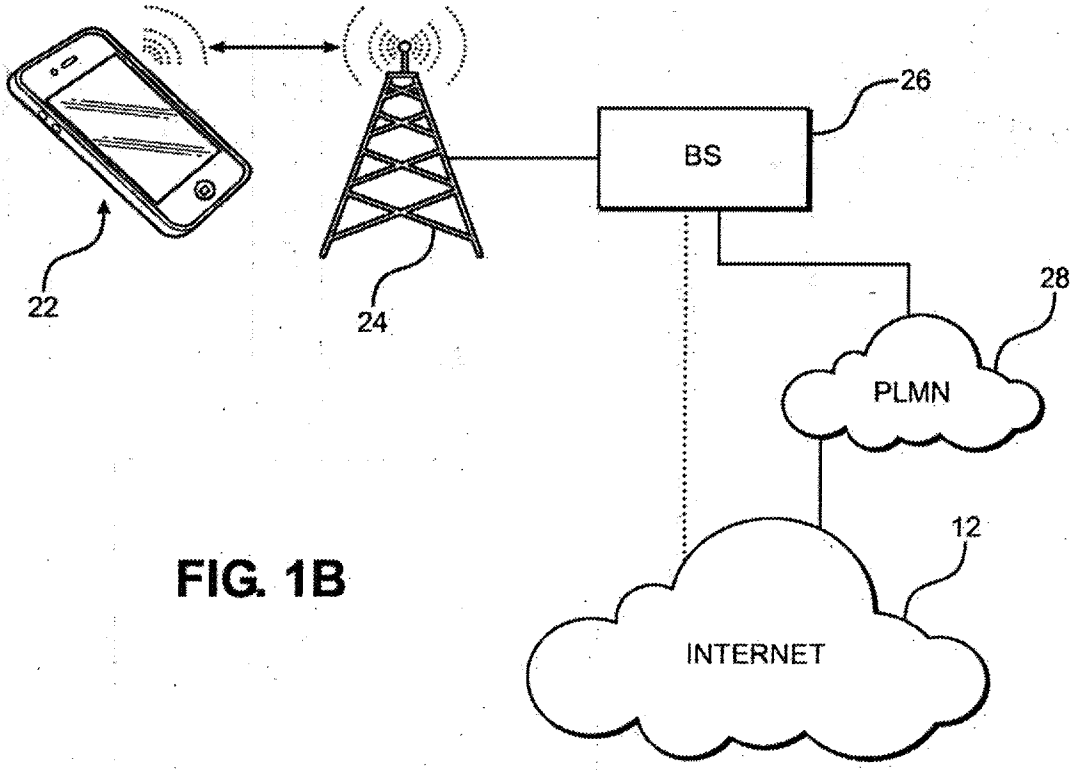


FIG. 1B

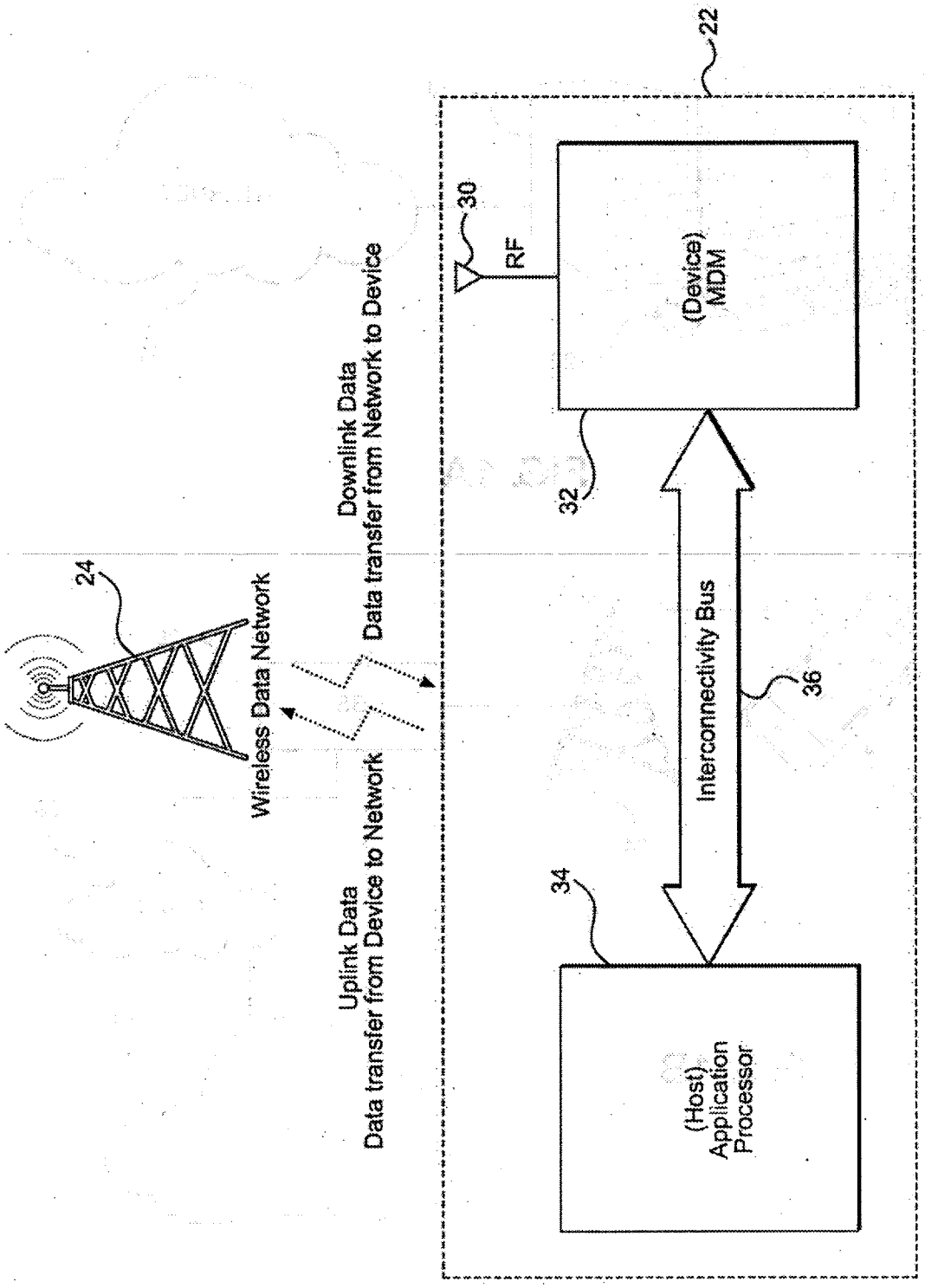

22
30
RF
(Device)
MDM
32
Interconnectivity Bus
36
34
(Host)
Application
Processor
24
Wireless Data Network
Downlink Data
Data transfer from Network to Device
Uplink Data
Data transfer from Device to Network

FIG. 1C

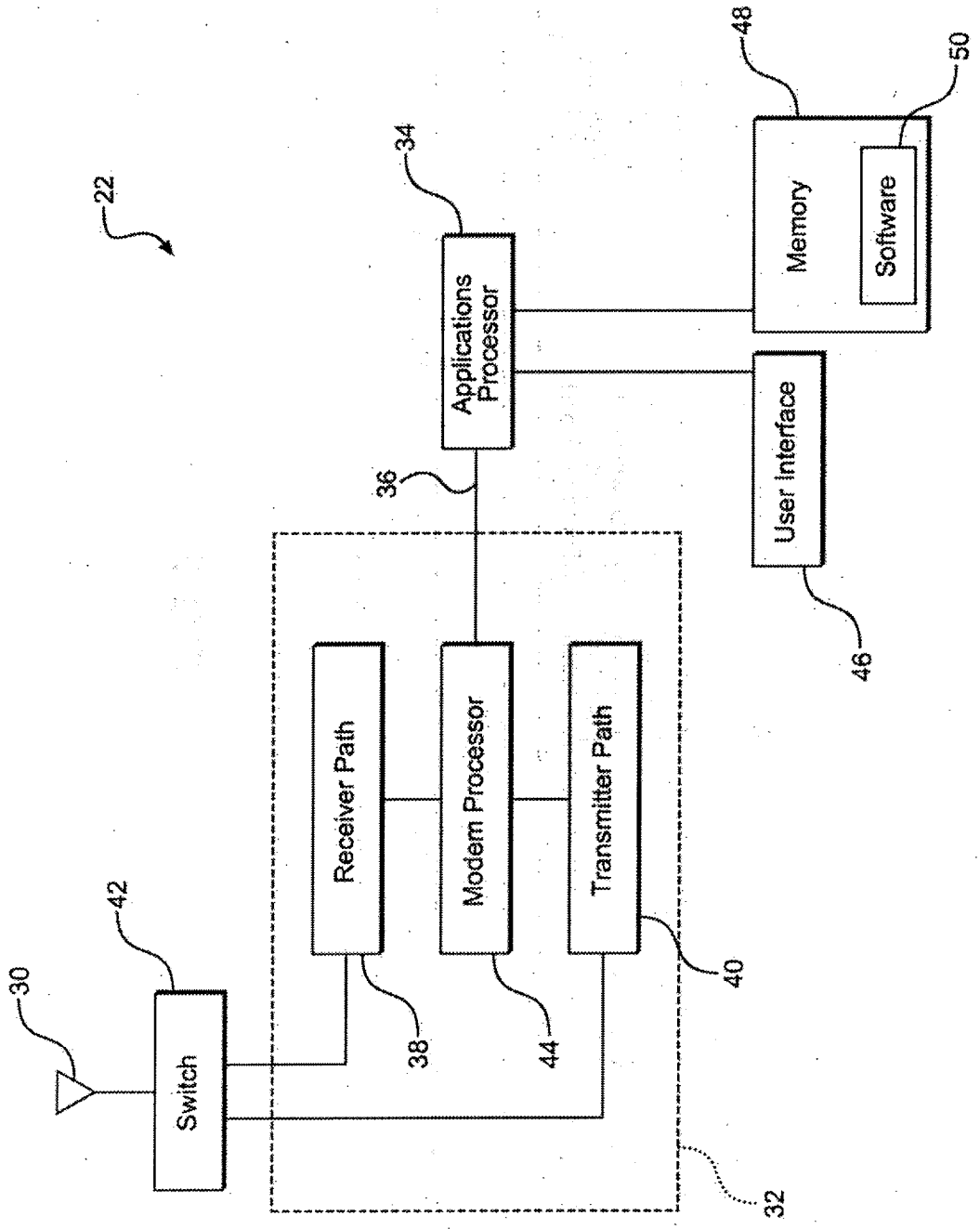

22
34
Applications Processor
48
Memory
50
Software
User interface
46
36
Receiver Path
Modem Processor
Transmitter Path
38
44
40
30
42
Switch
32

FIG. 2

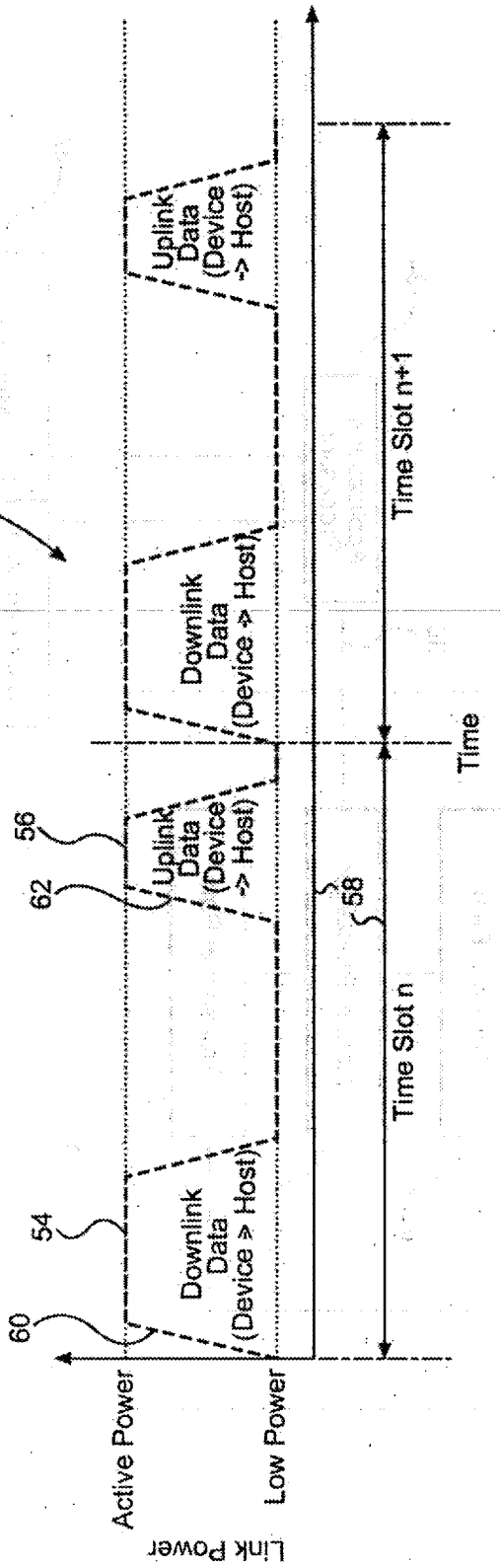

52
54
56
58
60
62
Downlink Data (Device -> Host)
Uplink Data (Device -> Host)
Downlink Data (Device -> Host)
Uplink Data (Device -> Host)
Time Slot n
Time Slot n+1
Time
Active Power
Low Power
Link Power

FIG. 3

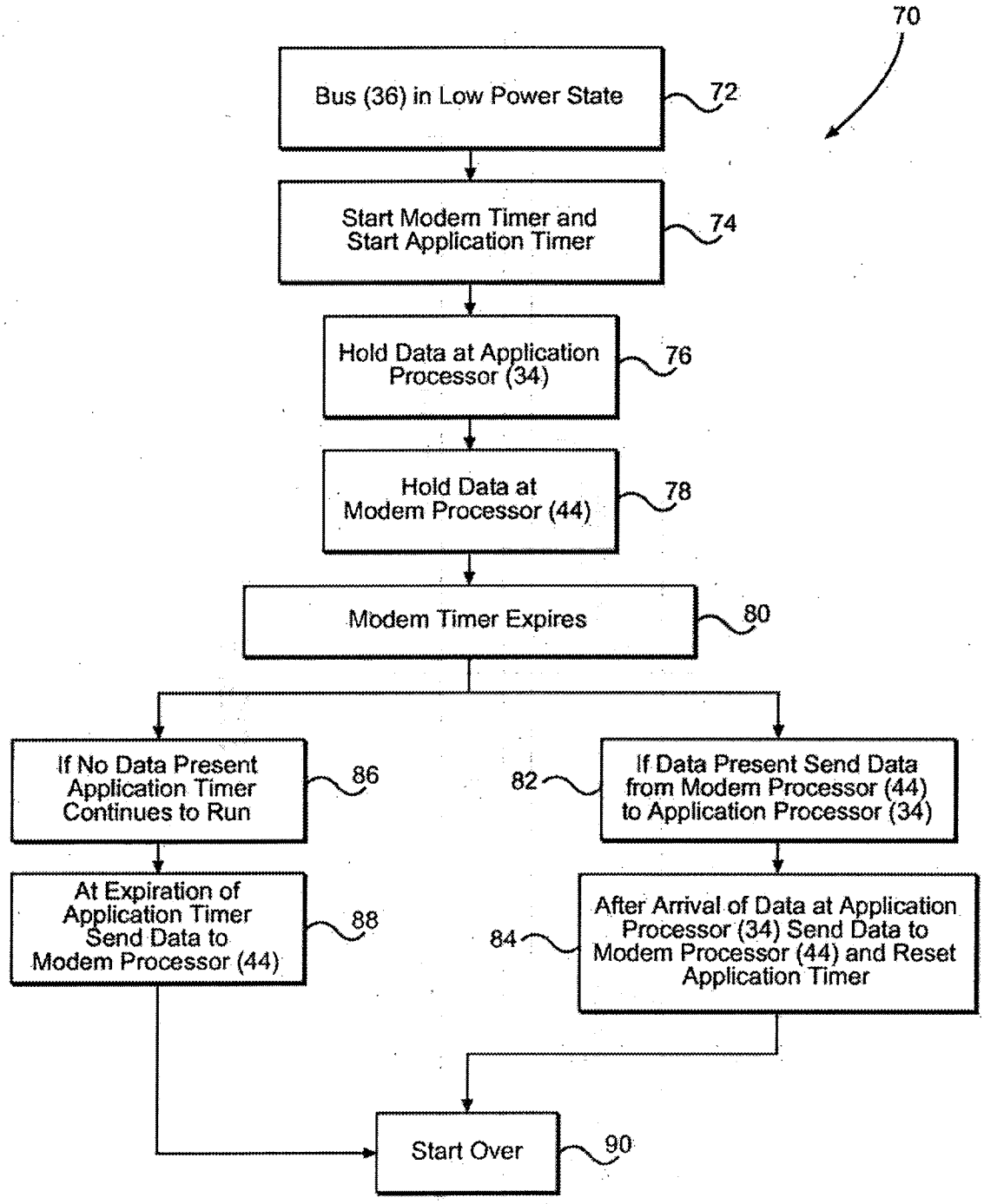

70
Bus (36) in Low Power State
72
Start Modem Timer and Start Application Timer
74
Hold Data at Application Processor (34)
76
Hold Data at Modem Processor (44)
78
Modem Timer Expires
80
If No Data Present Application Timer Continues to Run
86
82
If Data Present Send Data from Modem Processor (44) to Application Processor (34)
At Expiration of Application Timer Send Data to Modem Processor (44)
88
84
After Arrival of Data at Application Processor (34) Send Data to Modem Processor (44) and Reset Application Timer
Start Over
90

FIG. 4

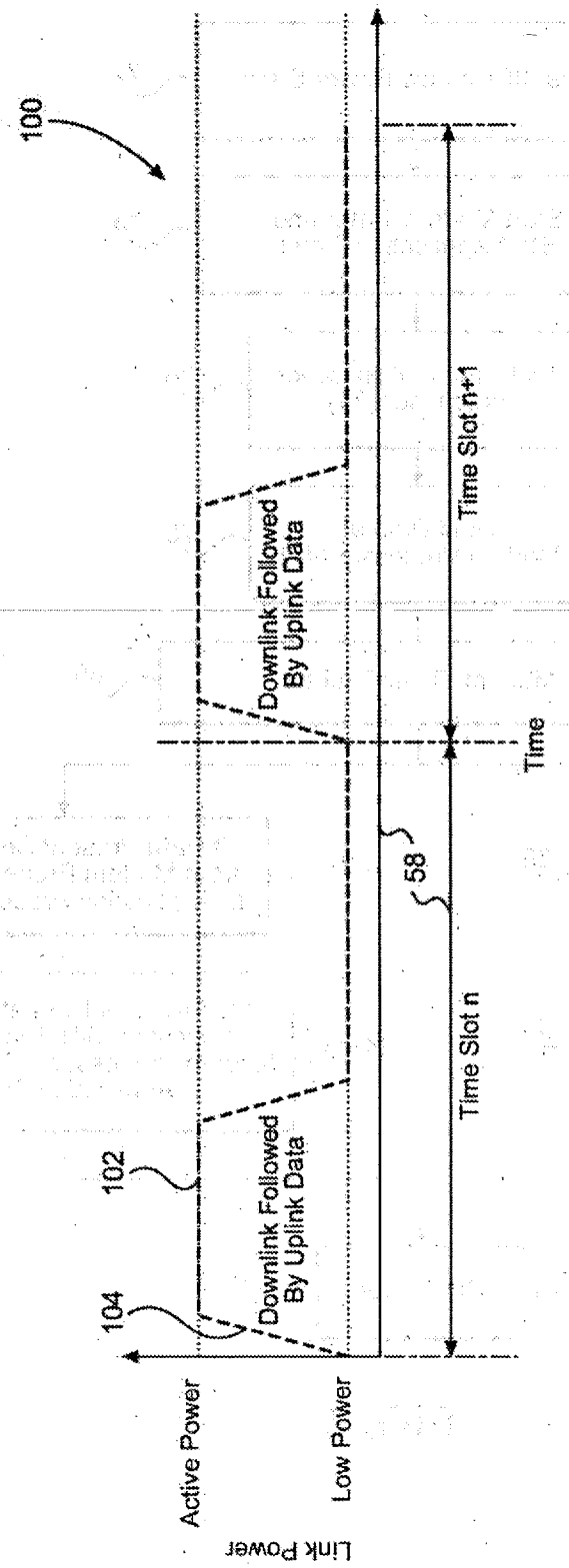

100
Link Power
Active Power
Low Power
104
102
Downlink Followed By Uplink Data
Downlink Followed By Uplink Data
58
Time Slot n
Time Slot n+1
Time

FIG. 5

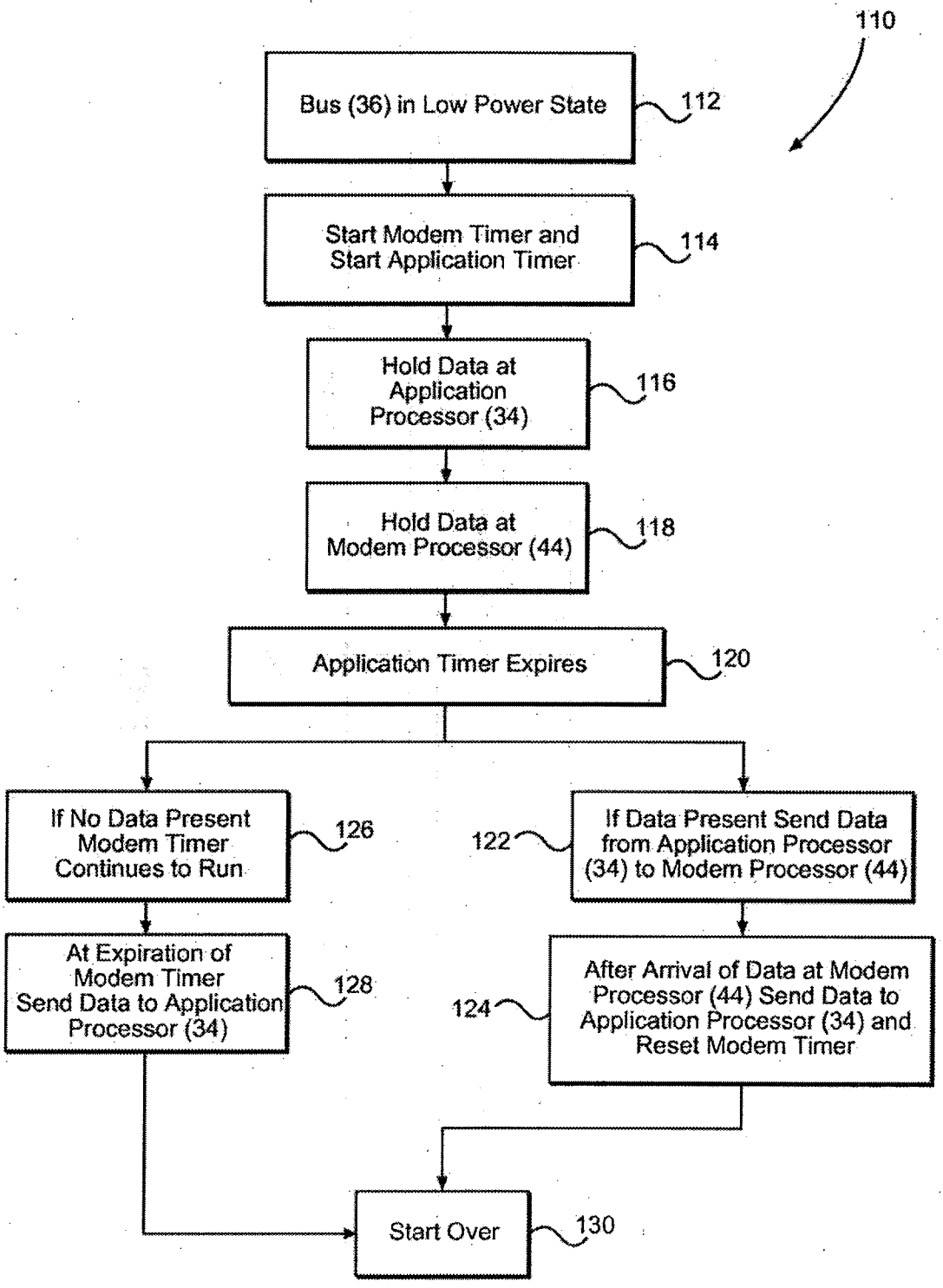

110
Bus (36) in Low Power State
112
Start Modem Timer and Start Application Timer
114
Hold Data at Application Processor (34)
116
Hold Data at Modem Processor (44)
118
Application Timer Expires
120
If No Data Present Modem Timer Continues to Run
126
122
If Data Present Send Data from Application Processor (34) to Modem Processor (44)
At Expiration of Modem Timer Send Data to Application Processor (34)
128
124
After Arrival of Data at Modem Processor (44) Send Data to Application Processor (34) and Reset Modem Timer
Start Over
130

FIG. 6

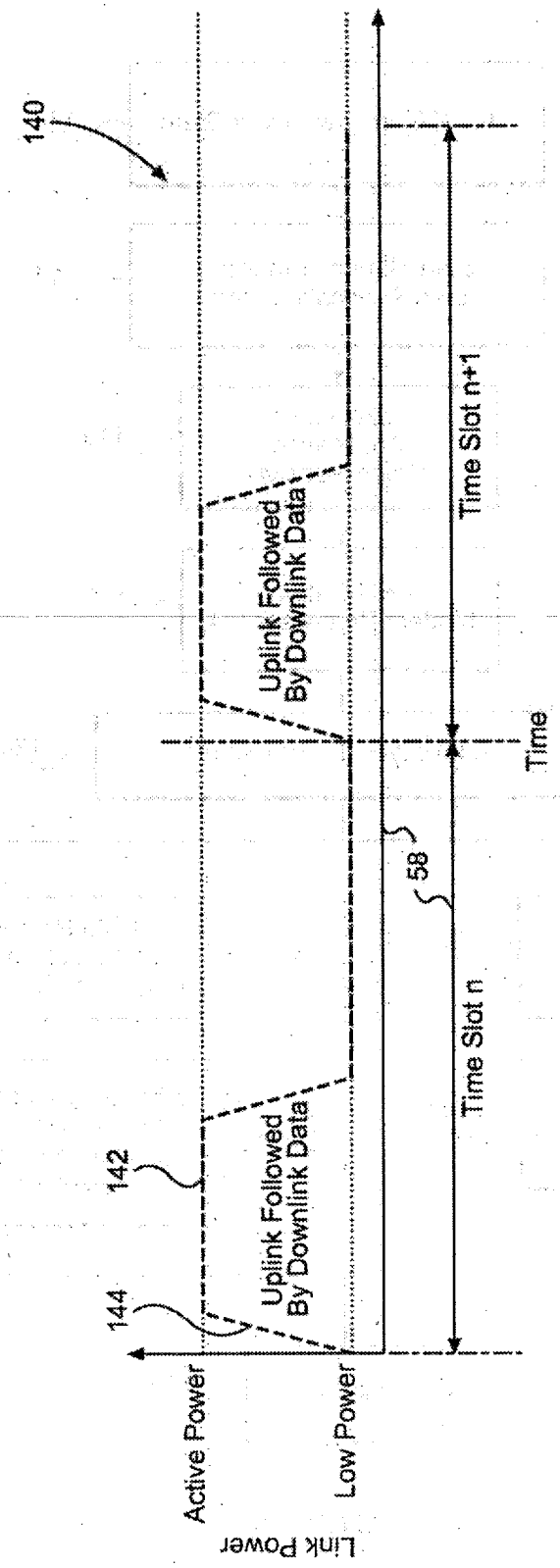

140
142
144
58
Link Power
Active Power
Low Power
Uplink Followed By Downlink Data
Uplink Followed By Downlink Data
Time Slot n
Time Slot n+1
Time

FIG. 7

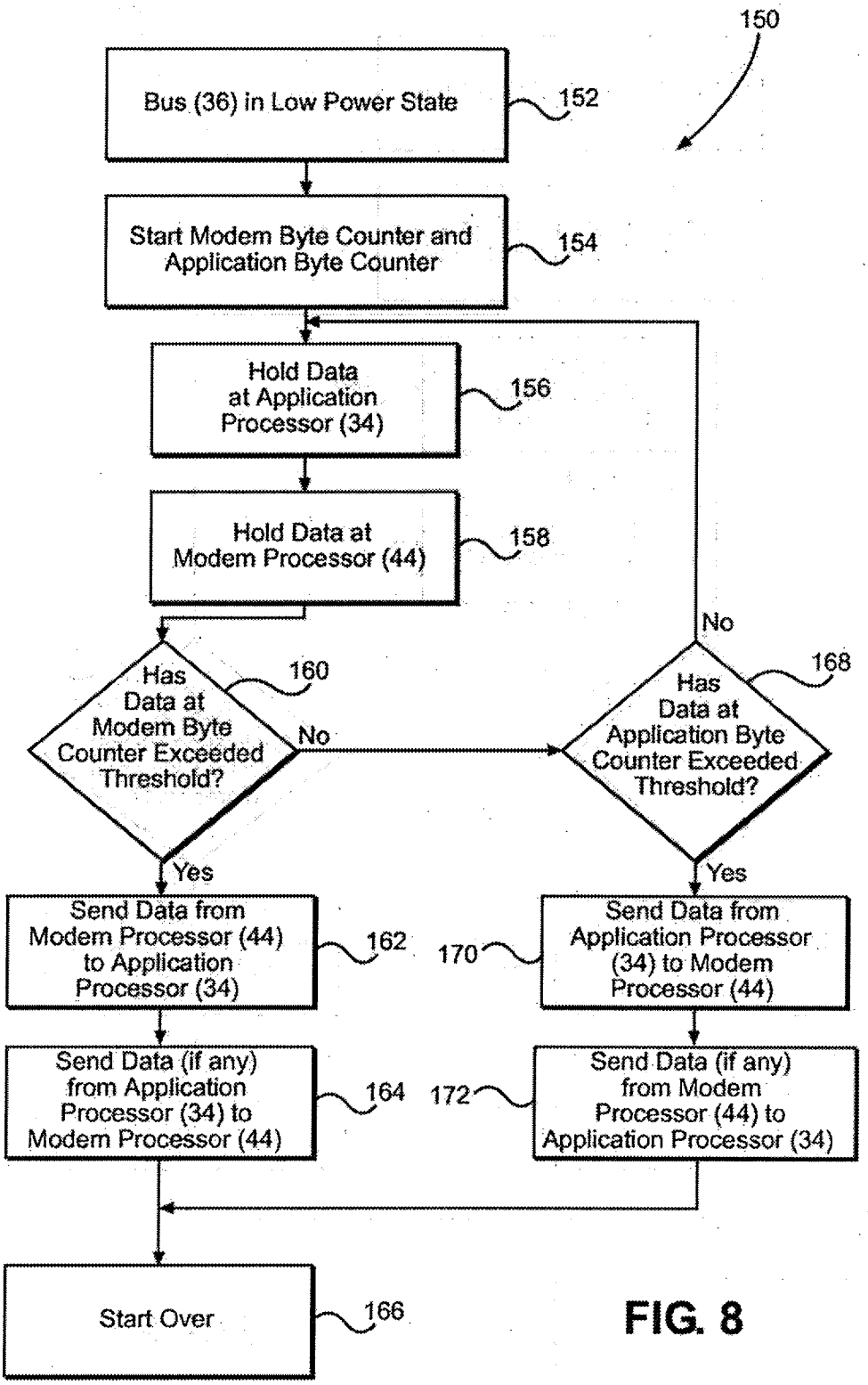

150
Bus (36) in Low Power State
152
Start Modem Byte Counter and Application Byte Counter
154
Hold Data at Application Processor (34)
156
Hold Data at Modem Processor (44)
158
Has Data at Modem Byte Counter Exceeded Threshold?
160
No
Yes
Has Data at Application Byte Counter Exceeded Threshold?
168
No
Yes
Send Data from Modem Processor (44) to Application Processor (34)
162
Send Data (if any) from Application Processor (34) to Modem Processor (44)
164
Send Data from Application Processor (34) to Modem Processor (44)
170
Send Data (if any) from Modem Processor (44) to Application Processor (34)
172
Start Over
166

FIG. 8

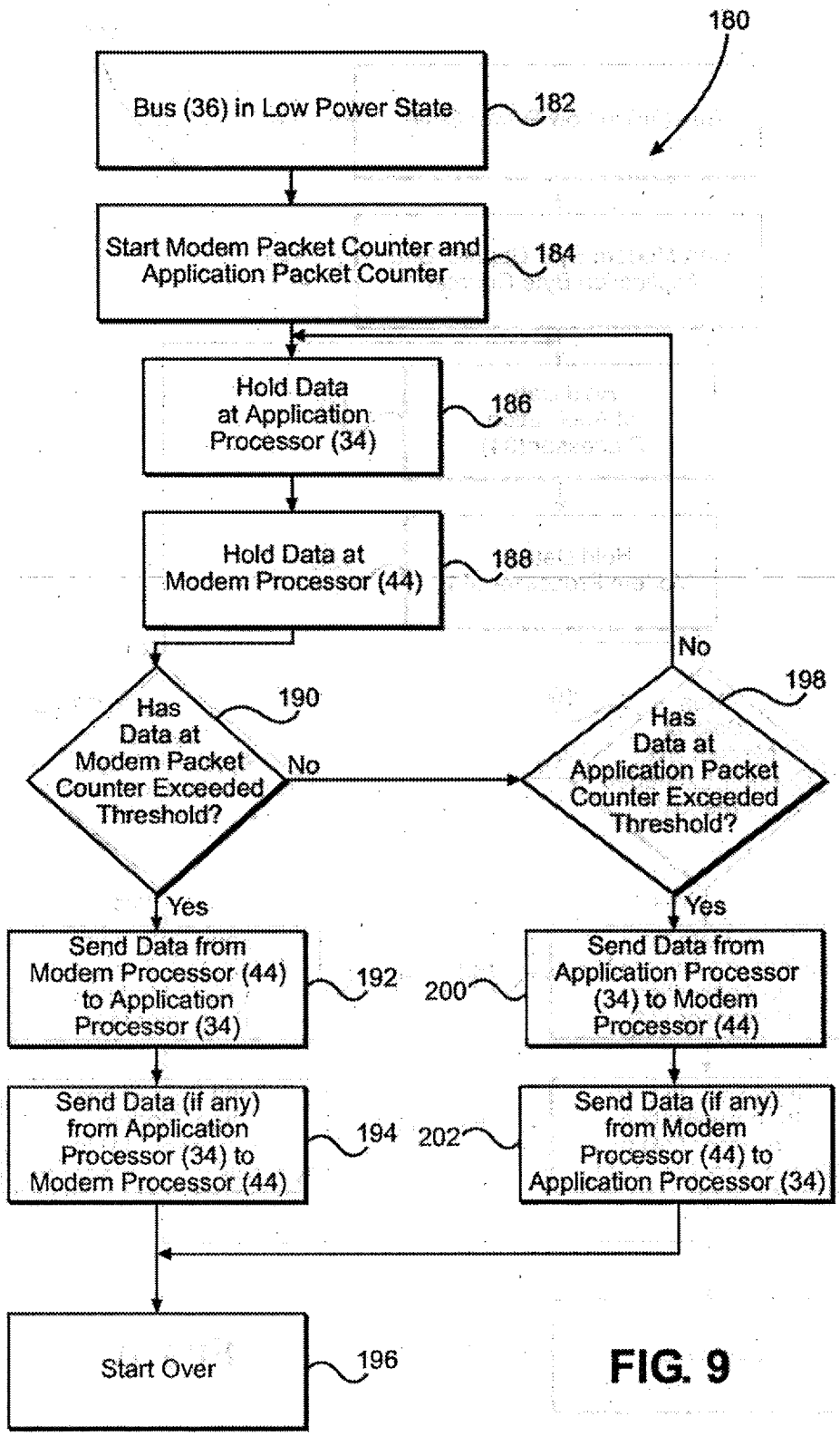

180
Bus (36) in Low Power State
182
Start Modem Packet Counter and Application Packet Counter
184
Hold Data at Application Processor (34)
186
Hold Data at Modem Processor (44)
188
Has Data at Modem Packet Counter Exceeded Threshold?
190
No
Yes
Has Data at Application Packet Counter Exceeded Threshold?
198
No
Yes
Send Data from Modem Processor (44) to Application Processor (34)
192
Send Data (if any) from Application Processor (34) to Modem Processor (44)
194
Send Data from Application Processor (34) to Modem Processor (44)
200
Send Data (if any) from Modem Processor (44) to Application Processor (34)
202
Start Over
196

FIG. 9

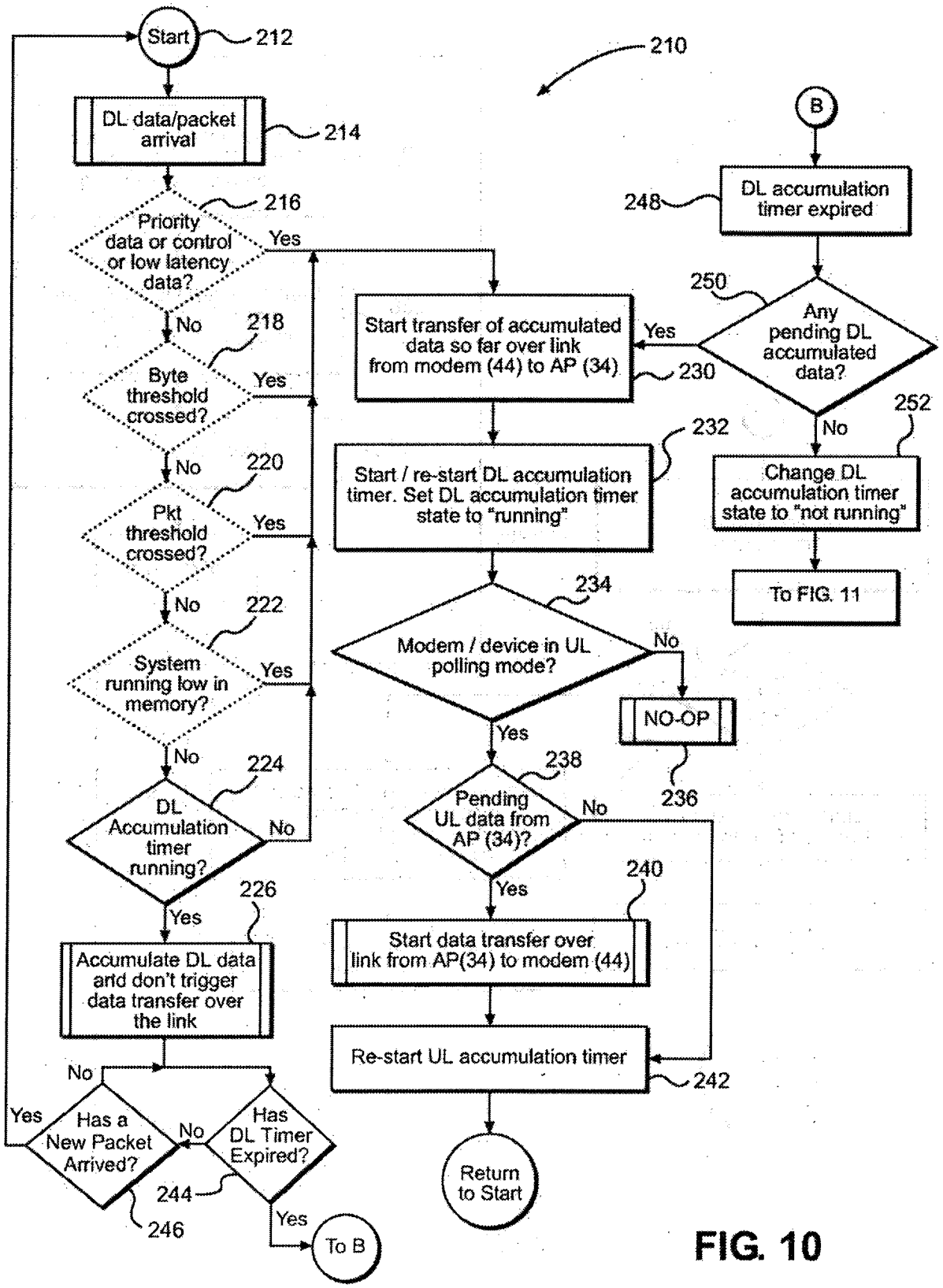

Start
212
210
DL data/packet arrival
214
Priority data or control or low latency data?
216
Yes
No
Byte threshold crossed?
218
Yes
No
Pkt threshold crossed?
220
Yes
No
System running low in memory?
222
Yes
No
DL Accumulation timer running?
224
No
Yes
Accumulate DL data and don't trigger data transfer over the link
226
No
Has a New Packet Arrived?
Yes
No
Has DL Timer Expired?
244
246
Yes
To B
Start transfer of accumulated data so far over link from modem (44) to AP (34)
230
Start / re-start DL accumulation timer. Set DL accumulation timer state to "running"
232
Modem / device in UL polling mode?
234
No
Yes
NO-OP
236
Pending UL data from AP (34)?
238
No
Yes
Start data transfer over link from AP(34) to modem (44)
240
Re-start UL accumulation timer
242
Return to Start
B
DL accumulation timer expired
248
Any pending DL accumulated data?
250
Yes
No
Change DL accumulation timer state to "not running"
252
To FIG. 11

FIG. 10

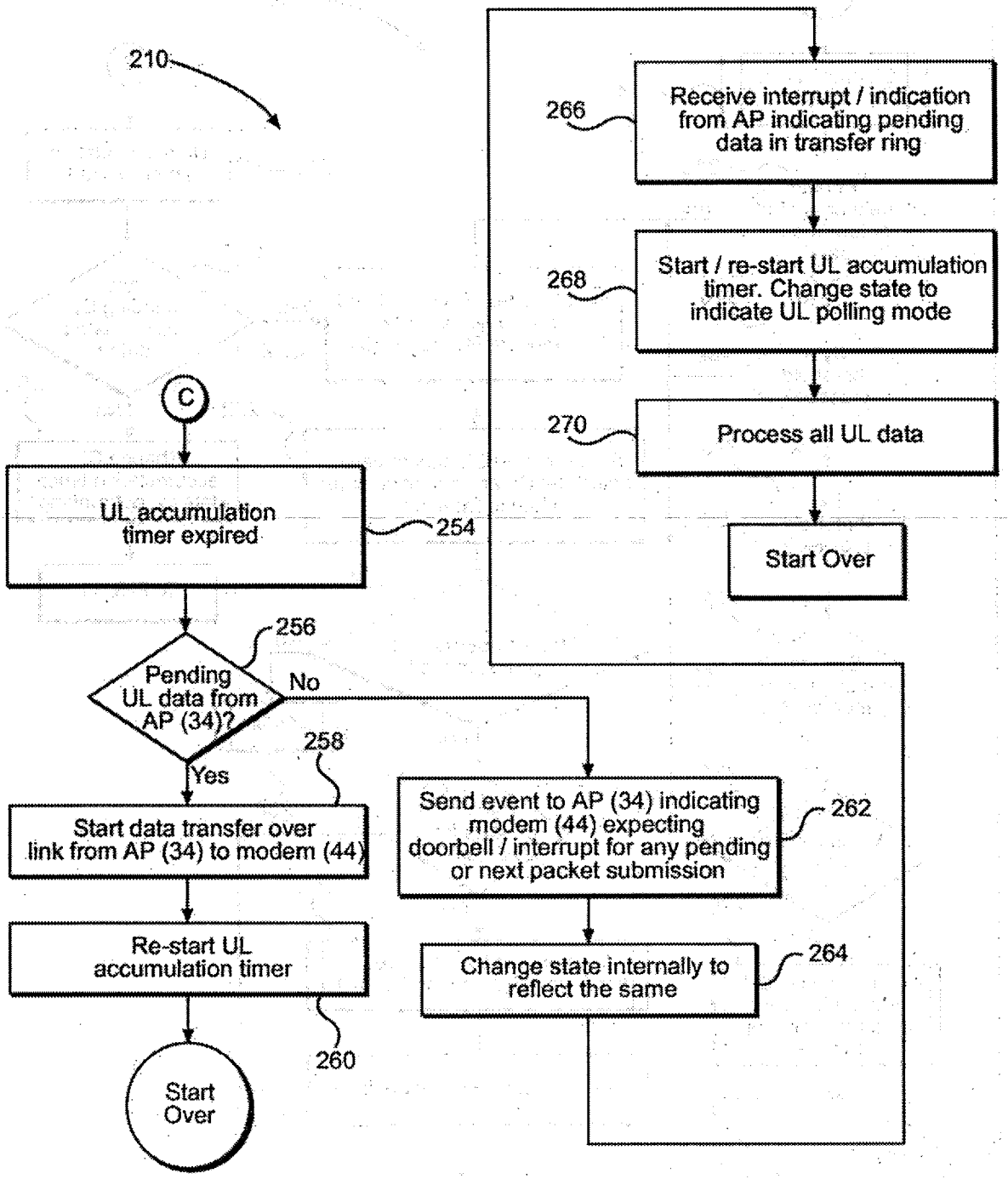

210
Receive interrupt / indication from AP indicating pending data in transfer ring
266
Start / re-start UL accumulation timer. Change state to indicate UL polling mode
268
Process all UL data
270
Start Over
C
UL accumulation timer expired
254
256
Pending UL data from AP (34)?
No
Yes
258
Start data transfer over link from AP (34) to modem (44)
Re-start UL accumulation timer
260
Start Over
Send event to AP (34) indicating modem (44) expecting doorbell / interrupt for any pending or next packet submission
262
Change state internally to reflect the same
264

FIG. 11

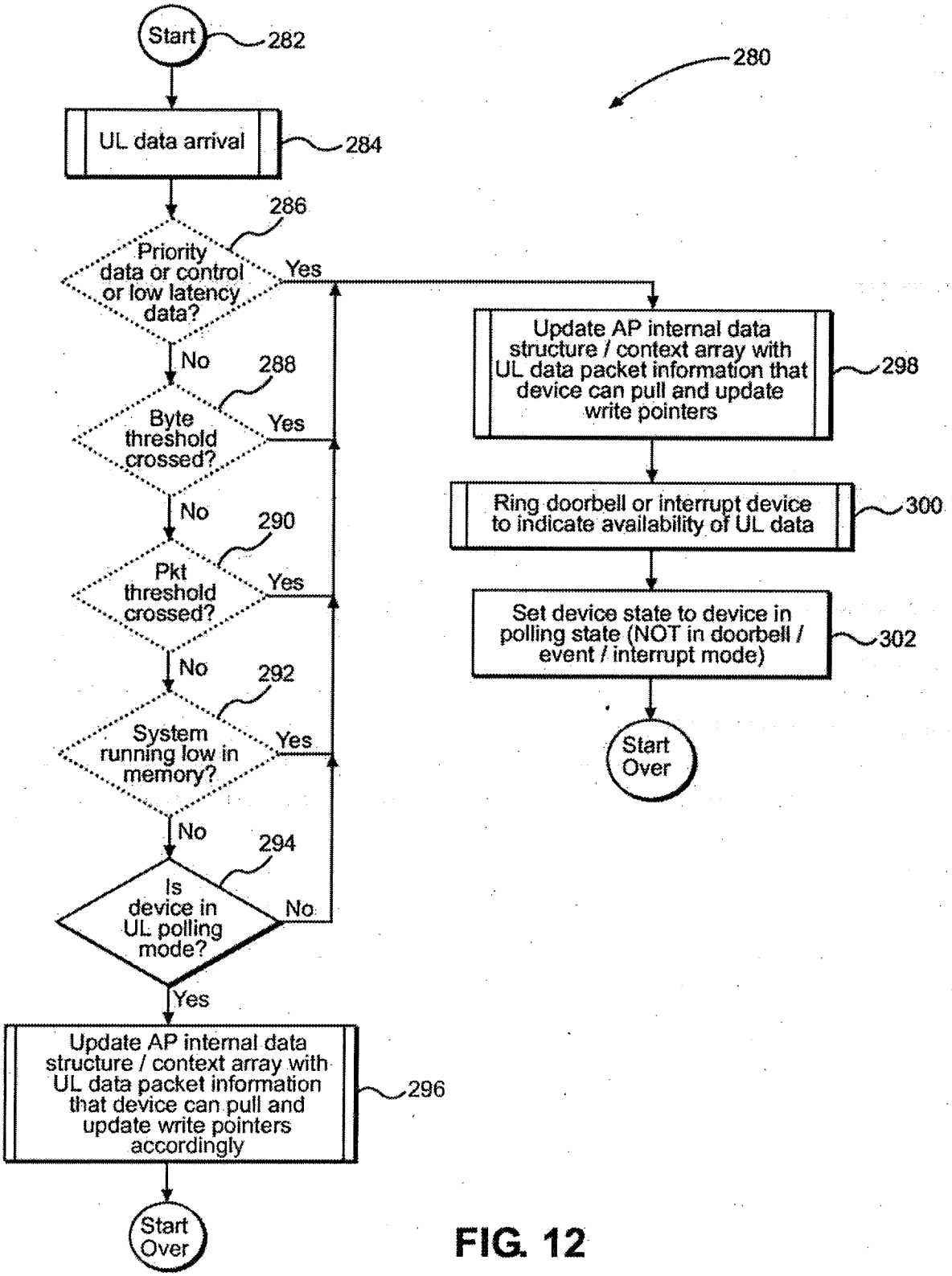

Start
282
280
UL data arrival
284
286
Priority data or control or low latency data?
Yes
No
288
Byte threshold crossed?
Yes
No
290
Pkt threshold crossed?
Yes
No
292
System running low in memory?
Yes
No
294
Is device in UL polling mode?
No
Yes
Update AP internal data structure / context array with UL data packet information that device can pull and update write pointers accordingly
296
Start Over
Update AP internal data structure / context array with UL data packet information that device can pull and update write pointers
298
Ring doorbell or interrupt device to indicate availability of UL data
300
Set device state to device in polling state (NOT in doorbell / event / interrupt mode)
302
Start Over

FIG. 12

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Filer:	Taylor M. Davenport/Allyson Van Gorder
Attorney Docket Number:	141062/1173-141

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	9	80	720
Independent claims in excess of 3	1201	6	420	2520
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**4980**

Electronic Acknowledgement Receipt

EFS ID:	20947912
Application Number:	14568694
International Application Number:	
Confirmation Number:	3463
Title of Invention:	POWER SAVING TECHNIQUES IN COMPUTING DEVICES
First Named Inventor/Applicant Name:	Vinod Harimohan Kaushik
Customer Number:	115309
Filer:	Taylor M. Davenport/Allyson Van Gorder
Filer Authorized By:	Taylor M. Davenport
Attorney Docket Number:	141062/1173-141
Receipt Date:	12-DEC-2014
Filing Date:	
Time Stamp:	14:43:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$4980
RAM confirmation Number	826
Deposit Account	501732
Authorized User	DAVENPORT, TAYLOR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	141062_ADS.pdf	1561672	no	10
Warnings:					
Information:					
2	Power of Attorney	141062_POA.PDF	454476	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	141062_IDS_12-12-14_AsFiled.PDF	706830	no	4
Warnings:					
Information:					
4		141062_APP_12-12-14_AsFiled.pdf	185620	yes	34

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	26
Claims	27	33
Abstract	34	34

Warnings:					
Information:					
5	Drawings-only black and white line drawings	141062_FDWG_12-12-14_AsFiled.pdf	131024	no	13
Warnings:					
Information:					

6	Fee Worksheet (SB06)	fee-info.pdf	40514 a8421a80a3688fd4c2140f2f2adc6133a3e09b2f5	no	2

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Total Files Size (in bytes):	3080136

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Vinod	Harimohan	Kaushik	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Diego	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
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Postal Code	92121	Country i	US

Inventor 2 Remove

Legal Name

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	Uppinder	Singh	Babbar	

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Inventor 3 Remove

Legal Name

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	Andrei		Danaila	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

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Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
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Inventor 4 Remove

Legal Name

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	Neven		Klacar	

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	Muralidhar	Coimbatore	Krishnamoorthy	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

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City	San Diego	**State/Province**	CA
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Inventor 7 Remove

Legal Name

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	Vaibhav		Kumar	

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City	Encinitas	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

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City	San Diego	**State/Province**	CA
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Inventor 8 Remove

Legal Name

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	Vanitha	Aravamudhan	Kumar	

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	Shailesh		Maheshwari	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Mailing Address of Inventor:

Address 1	5775 Morehouse Drive		
Address 2			
City	San Deigo	**State/Province**	CA
Postal Code	92121	**Country** i	US

Inventor 10 Remove

Legal Name

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	Alok		Mitra	

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Inventor 11 Remove

Legal Name

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	Roshan		Pius	

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Inventor 12 Remove

Legal Name

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	Hariharan		Sukumar	

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City	San Diego	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Postal Code	92121	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	115309		
Email Address	patents@wt-ip.com	Add Email	Remove Email
Email Address	us-docketing@qualcomm.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES		
Attorney Docket Number	141062/1173-141	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	10

Filing By Reference :

Only compete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	115309		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	61916498	2013-12-16
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62019073	2014-06-30

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	QUALCOMM Incorporated		
Mailing Address Information:			
Address 1	5775 Morehouse Drive		
Address 2			
City	San Diego	**State/Province**	CA
Country i	US	Postal Code	92121
Phone Number	(858) 658-4351	Fax Number	(919) 297-3298
Email Address	us-docketing@qualcomm.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	141062/1173-141
	Application Number	
Title of Invention	POWER SAVING TECHNIQUES IN COMPUTING DEVICES	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
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Phone Number		Fax Number	
Email Address			

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Signature	/Taylor M. Davenport/			Date (YYYY-MM-DD)	2014-12-12
First Name	Taylor	Last Name	Davenport	Registration Number	42466

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.