

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation,
Petitioner,

v.

Qualcomm Incorporated,
Patent Owner

Case IPR2018-01346
U.S. Patent No. 9,535,490

PATENT OWNER PRELIMINARY RESPONSE

TABLE OF CONTENTS

I. INTRODUCTION.....	1
II. BACKGROUND.....	3
A. The '490 Patent	5
B. Prosecution History	13
III. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”).....	14
IV. CLAIM CONSTRUCTION	14
V. THE BOARD SHOULD EXERCISE ITS DISCRETION UNDER 35 U.S.C. § 314(A) TO DENY INSTITUTION	15
A. The Petition Should Be Denied In View Of The Advanced Stage Of The Parallel ITC Investigation And District Court Litigation.....	15
B. Filing Five Separate Petitions Against the Same Patent Is An Unnecessary and Abusive Duplication of Proceedings	20
VI. THE PETITION SHOULD ALSO BE DENIED ON THE MERITS	23
A. The Asserted References	24
1. Heinrich.....	24
2. Balasubramanian	28
B. The Petition Fails To Establish A Motivation To Combine Heinrich With Balasubramanian	31
C. The Cited References, Alone Or In Combination, Fail To Teach Or Disclose The Claim 1, 26, And 27 Limitation “the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus”	36
VII. CONCLUSION	40

TABLE OF AUTHORITIES

Page

CASES

<i>Adidas AG v. Nike, Inc.</i> , 894 F.3d 1256 (Fed. Cir. 2018)	2, 21
<i>Alere Inc. v. Rembrandt Diagnostics, LP</i> , IPR2017-01130, Paper 10 (PTAB Sept. 28, 2017).....	23
<i>American Honda Motor Co., Inc. v. Intellectual Ventures II LLC</i> , IPR2018-00349, Paper 9 (PTAB, June 27, 2018)	3, 21, 22
<i>Nautilus Hyosung, Inc. v. Diebold, Inc.</i> , IPR2017-00426, Paper 17 (PTAB June 22, 2017)	15, 18, 19
<i>NetApp, Inc. v. Realtime Data LLC</i> , IPR2017-01195, Paper 9 (PTAB Oct. 12, 2017).....	15, 20
<i>NHK Spring Co. v. Intrix-Plex Tech., Inc.</i> , IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018).....	15, 16, 18, 20
<i>PGS Geophysical AS v. Iancu</i> , 891 F.3d 1354 (Fed. Cir. 2018)	21
<i>Qualcomm Incorporated v. Apple Inc.</i> , Case No. 3:17-CV-01375 (S.D. Cal).....	18
<i>SAS Institute v. Iancu</i> , 138 S. Ct. 1348 (2018).....	passim
<i>Tittex International, Ltd. v. Precision Fabrics Group, Inc.</i> , IPR2015-01671, Paper 7 (PTAB Feb. 11, 2016).....	22

STATUTES

35 U.S.C. § 103(a)	13
--------------------------	----

35 U.S.C. § 314(a)	passim
35 USC § 316(b)	2, 15, 21, 22
37 C.F.R. § 42.100(b)	14
37 C.F.R. § 42.108(c).....	24

OTHER AUTHORITIES

Trial Practice Guide (Aug. 2018).....	15
“Guidance on the Impact of SAS on AIA Trial Proceedings,” April 26, 2018 (https://www.uspto.gov/sites/default/files/documents/guidance_on_the_impact_of_sas_on_aia_trial_proceedings_%20(april_26,_2018).pdf)	20
“Chief Judge Guidance: SAS Impact, Motions to Amend, and Claim Construction,” PTAB Litigation Blog, June 5, 2018, available at: http://www.ptablitigationblog.com/chief-judge-guidance-sas-impact-motions-to-amend-and-claim-construction/	21

I. INTRODUCTION

Petitioner held off filing its five petitions against U.S. Patent No. 9,535,490 (the '490 patent) until after a full hearing on the same underlying issues in an International Trade Commission Investigation (“the ITC Investigation”) and a mere nine months before trial in the Southern District of California. With knowledge of the schedules in both parallel proceedings, Petitioner made the strategic decision to wait one full year before filing its redundant attack on the validity of the '490 patent. More significantly, Petitioner waited almost nine months after identifying the only ground asserted in this Petition before filing at the PTAB. In doing so, Petitioner received the benefit of Patent Owner’s expert briefing and a full ITC hearing on the same underlying issues raised in this Petition. Now, after having its arguments fully heard at the ITC, and with the ITC and Southern District of California scheduled to decide the same underlying issues long before this Board’s final written decision, Petitioner asks the PTAB to waste its resources and allow Petitioner to litigate for a *third* time what will be a decided issue. The Board should not reward Petitioner for its dilatory efforts and should instead exercise its discretion under 35 U.S.C. § 314(a) and deny institution.

If that were not enough, by spreading two grounds of unpatentability across

five petitions to avoid the Supreme Court’s *SAS* all-or-nothing institution mandate,¹ Petitioner shows that it has no confidence in its positions. The PTAB and the Federal Circuit have read the *SAS* decision to require the PTAB to institute on “all challenges raised in the petition” or none. *See* April 26, 2018, Guidance on the Impact of SAS on AIA Trial Proceedings; *Adidas AG v. Nike, Inc.*, 894 F.3d 1256, 1258 (Fed. Cir. 2018). During its April 30, 2018, Chat with the Chief presentation, then-Chief Judge Ruschke cautioned that the presence of weak grounds in a petition could result in a complete denial of institution even if other unpatentability allegations met the threshold for institution.² Realizing that ineffectual positions could scuttle an entire petition, Petitioner has divided its ’490 patent challenges that would normally fit into one petition (*i.e.*, two grounds challenging 22 claims) across *five* petitions, hoping

¹ *See SAS Institute v. Iancu*, 138 S. Ct. 1348 (2018).

² *See* “Chief Judge Guidance: SAS Impact, Motions to Amend, and Claim Construction,” PTAB Litigation Blog, June 5, 2018, available at: <http://www.ptablitigationblog.com/chief-judge-guidance-sas-impact-motions-to-amend-and-claim-construction/> (“Instead, the panel would evaluate the challenges and determine whether, in the interests of efficient administration of the USPTO and integrity of the patent system (*see* 35 USC § 316(b)), the entire petition should be denied under 35 USC § 314(a).”).

to increase its odds of institution. But petition filing tactics that unduly multiply the number of proceedings are ripe for exercise of the PTAB's discretion under 35 U.S.C. § 314(a). *See American Honda Motor Co., Inc. v. Intellectual Ventures II LLC*, IPR2018-00349, Paper 9 at 21 (PTAB, June 27, 2018). The Board should not entertain Petitioner's end run around the Supreme Court's *SAS* mandate and should deny the five petitions outright.

Beyond these compelling reasons for the Board to exercise is § 314(a) discretion to deny all five petitions, the instant Petition suffers from substantive deficiencies justifying denial on the merits. For example, the Petition fails to establish a motivation to combine U.S. Patent No. 9,329,671 ("Heinrich") with U.S. Patent No. 8,160,000 ("Balasubramanian") – a finding recently confirmed by Administrative Law Judge Thomas B. Pender in the ITC Investigation. And even if the Board were to find that Heinrich and Balasubramanian could be combined, neither reference discloses a key limitation of independent claim 1, from which challenged claims 9 and 11-13 depend, and independent claims 26 and 27. Accordingly, if the Board reaches the merits of the Petition, the Board should deny institution for any of these substantive reasons.

II. BACKGROUND

Mobile computing devices, such as smart phones and tablets, are increasingly expected to perform a myriad of functions and communicate across numerous

networks. While standard desktop devices are generally immune to power concerns because they are plugged in to a wall socket, mobile devices must strive for a balance between functionality and power consumption. As more functionality is added to mobile devices, more power is consumed and battery life shortens. The power consumption concerns are heightened as network improvements have increased data rates. As data rates increase, the mobile devices must send, receive, and process larger amounts of data. This requires faster processors, quicker interconnectivity buses, and expanded memory, all of which increase power consumption.

Increased power consumption attributed to interconnectivity buses is particularly concerning. In a mobile device, a first microprocessor in the device is typically connected to another microprocessor over a wired interconnectivity bus. One or both of these microprocessors may be specially purposed to perform certain activities (*e.g.*, a modem processor configured to ready data for wireless transmission and for unpackaging data received at the device). The processors use the interconnectivity bus to exchange information. The introduction of faster interconnectivity buses, such as the peripheral component interconnect express (PCIe) standard and universal serial bus (USB) 3.0 and higher standard, in combination with overall increased data transmission volumes, have resulted in significantly increased power consumption by interconnectivity buses.

A. The '490 Patent

U.S. Patent No. 9,535,490 (the '490 patent) is directed to a novel approach for power-saving in interprocessor communications (IPC). The '490 patent is titled "Power Saving Techniques in Computing Devices" and claims priority to applications as far back as December 16, 2013.

The '490 patent describes power-saving techniques that organize data traffic on an interconnectivity bus in a manner that allows the interconnectivity bus to spend less time in an active state, and also in a manner that results in less-frequent changes between active and inactive states. Of course, the interconnectivity bus uses less power when it is in its inactive state than in its active state. But each transition from the inactive state to the active state, and vice versa, is further associated with a power cost. *See* Ex. 1401, 8:9-14 ("While placing the interconnectivity bus 36 in a sleep mode generally saves power, such sleep modes do have a drawback in that they consume relatively large amounts of power as they transition out of sleep mode."). The invention disclosed in the '490 patent addresses reductions of both time the interconnectivity bus is in an active state and the total number of active/inactive transitions that the interconnectivity bus undergoes.

Prior to the '490 patent, interconnectivity buses operated as shown for example in FIG. 3 below, sending and receiving data on demand multiple times during a single time slot. This caused the interconnectivity bus to be in an active

state for longer periods of time and to transition between states frequently:

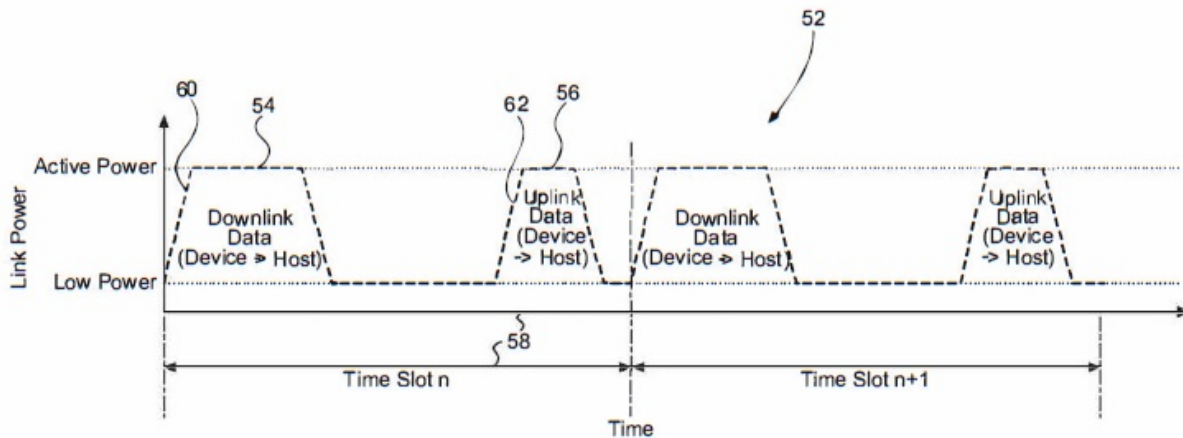


FIG. 3

The prior approach was satisfactory for interconnectivity buses with lower data rates for less data demanding implementations. But faster operating interconnectivity buses providing larger bandwidth, such as PCIe and USB 3.0 and higher, resulted in excessive power consumption by the interconnectivity buses due largely to the increased numbers of state transitions per time slot. The '490 patent notes that one time slot 58 of the interconnectivity bus spans one millisecond. *Id.*, 9:32-34. And, as illustrated in FIG. 3, multiple downlink and uplink transmissions could occur within a single time slot, each transmission being only microseconds in length. Interconnectivity bus state transitions on a microsecond scale consume significant amounts of power. *See id.*, 8:9-14.

The '490 patent teaches mechanisms for organizing the data traffic across the interconnectivity bus so that the interconnectivity bus makes fewer state transitions and does not spend as much cumulative time in the active state. One way to organize the traffic to save power is to delay, or hold, data between two processors (for example, a modem processor and an application processor) instead of immediately sending it across the interconnectivity bus when that data is available. The modem processor can hold its downlink data rather than sending it across the bus right away. And the application processor can hold its uplink data too. By holding the data, the interconnectivity bus does not have to transition to a high power state separately for every quantum of data to be sent. But the held data does still need to be transmitted at some point. The '490 patent recognizes that by waiting to accumulate a set of held data, and then sending all of the data as a group across the interconnectivity bus in both directions, the interconnectivity bus can still move all of the traffic it needs to. But it does it with fewer state transitions and with more time where the interconnectivity bus is sleeping. FIG. 5 of the '490 patent illustrates the grouping of data transmissions across the interconnectivity bus:

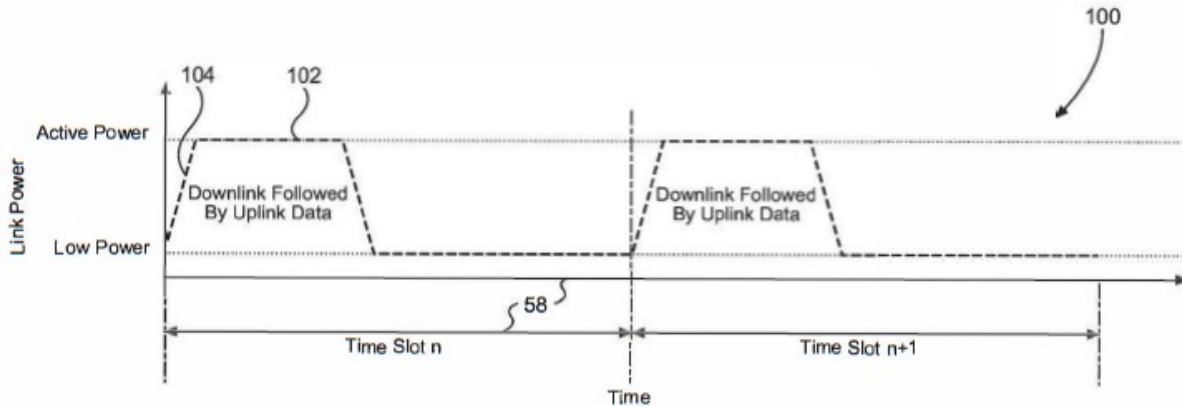


FIG. 5

The '490 patent discloses mechanisms that can be used to hold the data for the right period of time. For example, a “modem timer” can be used by the modem processor to hold its downlink data until the timer elapses. Ex. 1401, 5:18-21. And an “uplink timer” can be used by the application processor to hold its uplink data until the timer elapses. When the timers run out, all of the data that was held gets flushed out over the interconnectivity bus together. *Id.*, 9:37-40. The timer values can be set to a number that is long enough to group the data together, but short enough to avoid unacceptable latency.

The '490 patent teaches another way to further improve the IPC traffic: the modem processor and application processor can coordinate to send their data at the same or similar time. By synchronizing traffic in both directions, the interconnectivity bus can sleep even more, where what used to be two or more active

bus states becomes just one, providing power savings. *Id.*, 5:32-35.

One synchronization solution described in the '490 patent is to use a modem timer. The modem processor holds its downlink data until the modem timer elapses. At the same time, the application processor is also holding its uplink data. The application processor is set up to release its uplink data when it detects that the modem processor is sending downlink data to it. Thus, when the modem timer fires, the modem processor sends all of the grouped data across the bus to the application processor. *Id.*, 5:21-23. And when the application processor starts to receive that data, it knows that it is a good time to synchronize and releases the uplink data that it was holding. *Id.*, 5:23-26. Traffic flows in both directions at the same time across the interconnectivity bus, before the interconnectivity bus can go to sleep.

In another '490 patent solution, two different timers, a modem timer and an uplink timer, can both be used at the same time. The modem timer is set to a shorter value than the uplink timer. When the modem timer elapses, the traffic is transmitted the same as before: the modem processor sends any queued downlink data, and in response the application processor sends its uplink data. The uplink timer is then reset. *Id.*, 5:31-32. Sometimes the modem timer can elapse, but the modem processor does not have any held data to send. In this case, the modem processor does not send anything to the application processor over the interconnectivity bus, and the uplink timer expires because it has not been reset by a modem processor

transmission. The application processor, upon expiration of its timer, sends the uplink data that it has been holding to avoid excessive latency of its application-to-modem processor transmission. *Id.*, 5:27-31.

The '490 patent teaches one further way to coordinate traffic synchronization. Rather than the modem processor and the application processor both having responsibility to transmit or push their held data, the modem processor can be put in full control. The modem processor can push its downlink data across the bus when the modem timer elapses. But it can also ensure that the traffic is synched in both directions by pulling the uplink data from the application processor across the bus at the same time or shortly after. This can be accomplished for example via the modem processor controlling data structures that it can use to pull data from a shared memory without involvement of the application processor. By synchronizing its data push and pull operations, the modem process can limit interconnectivity bus transitions.

Claims 1 (from which claims 9 and 11-13 depend), 26, and 27 of the '490 patent illustrate three embodiments of the claimed invention:

1. A mobile terminal comprising:

a modem timer;

a modem processor, the modem processor configured to hold modem processor to application processor data until

expiration of the modem timer;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

26. A mobile terminal comprising:

a modem byte accumulation limit counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of bytes has been reached by the modem byte accumulation limit counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

27. A mobile terminal comprising:

a modem packet counter;

a modem processor, the modem processor configured to hold modem processor to application processor data until a predefined threshold of packets has been reached by the modem packet counter;

an application processor;

an interconnectivity bus communicatively coupling the application processor to the modem processor; and

the application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor

to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

B. Prosecution History

U.S. Patent Application No. 14/568,694 (“the ’694 application”) was filed on December 12, 2014, and claims priority to U.S. Provisional Application No. 61/916,498, filed on December 16, 2013 and U.S. Provisional Application No. 62/019,073, filed on June 30, 2014. The ’694 application issued as the ’490 patent. In its initial Office Action, the Patent Office rejected the pending claims as being unpatentable under 35 U.S.C. § 103(a) based on the combination of International Publication No. WO 2009/039034 to John et al. (“John”) and U.S. Patent No. 6,021,264 to Morita (“Morita”). Ex. 1403, 90-99.

To overcome the § 103(a) rejection, Applicant amended original claims 1, 24, and 25, which ultimately issued as independent claims 1 and 26, and 27, respectively. Applicant amended claim 1 to additionally recite:

The application processor configured to hold application processor to modem processor data until triggered by receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor

through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.

Ex. 1403, 33. Applicant amended claims 24 and 25 in the same manner. *Id.*, 37-38.

In view of these amendments and the accompanying arguments advanced by Applicant, the Examiner allowed the claims and issued the Notice of Allowance. *Id.*, 11-14.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”)

Patent Owner agrees with Petitioner’s assessment that a POSITA would have had (1) a Master’s degree in Electrical Engineering, Computer Engineering, or Computer Science, plus at least two years of relevant experience, or (2) a Bachelor’s degree in one of those fields plus at least four years of relevant experience, where “relevant experience” in the context of the ’490 patent refers to experience with mobile device architecture and multiprocessor systems.

IV. CLAIM CONSTRUCTION

37 C.F.R. 42.100(b) states that claims must be given their broadest reasonable interpretation in light of the specification (“BRI standard”). Patent Owner submits that no terms must be construed at this stage in the proceeding, and that the Board should deny institution under any claim construction it adopts. Patent Owner reserves the right to put forth constructions of particular claim terms and to rebut constructions proffered in the Petition as relevant to the patentability of the claims

should trial be instituted.

V. THE BOARD SHOULD EXERCISE ITS DISCRETION UNDER 35 U.S.C. § 314(A) TO DENY INSTITUTION

A. The Petition Should Be Denied In View Of The Advanced Stage Of The Parallel ITC Investigation And District Court Litigation

35 U.S.C. § 314(a) provides the Director with discretion to deny a petition. When determining whether to exercise this discretion, the Director must “consider the effect . . . on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.” 35 U.S.C. § 316(b). The Board’s decisions and its updated Trial Practice Guide instruct when it is appropriate to deny a petition, including when there are “events in other proceedings related to the same patent, either at the Office, in district courts, or the ITC.” Trial Practice Guide (Aug. 2018), at *10. *See also NetApp, Inc. v. Realtime Data LLC*, IPR2017-01195, Paper 9 at 12–13 (PTAB Oct. 12, 2017) (denying institution under § 314(a) where, due to petitioner’s delay, the Board likely would not have been able to rule on patentability until after the district court trial date); *Nautilus Hyosung, Inc. v. Diebold, Inc.*, IPR2017-00426, Paper 17 (PTAB June 22, 2017) (denying institution where, among other factors, the ITC already issued its Initial Determination of validity of the same patent over some of the same prior art references); *NHK Spring Co. v. Intri-Plex Tech., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (denying

institution where a district court trial will occur prior to the Board issuing a final written decision, the Board explaining that “instituting a trial under the facts and circumstances here would be an inefficient use of Board resources . . . and inconsistent with ‘an objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.’”).

The instant facts justify the Board exercising its §314(a) discretion to deny institution. Patent Owner filed an ITC Complaint on July 7, 2017.³ Petitioner had knowledge of and actively participated in the ITC Investigation no later than July 20, 2017. The Scheduling Order in the ITC Investigation issued September 19, 2017, and set a hearing date of June 18, 2018 through June 26, 2018. Ex. 2003. The Scheduling Order also set deadlines to serve initial invalidity contentions (October 23, 2017), final invalidity contentions (February 20, 2018), initial expert reports (March 16, 2018), rebuttal expert reports (March 30, 2018), and a Final

³ Though Petitioner Intel was not a named respondent in the ITC Investigation, Intel filed a Statement on the Public Interest on July 20, 2017 urging the ITC to deny Patent Owner’s request for an exclusion order. Ex. 2001. Moreover, IPR real-party-in-interest Apple *is* a named respondent in the ITC Investigation. Ex. 2002, 14.

Determination target date (January 14, 2019). *Id.*⁴

Though Petitioner challenges claims here that were not at issue in the ITC Investigation, the same underlying issues exist across the claims challenged in this Petition, including the combinability of the same prior art references and whether the same prior art references disclose or suggest similar claim limitations. Due to the similarity between the claims, Petitioner relies on the exact same prior art combination to challenge claims 9, 11-13, 26, and 27 as it relies on to challenge claim 31 in the ITC Investigation. That combination, Heinrich and Balasubramanian, was first identified when Petitioner and Apple served their initial invalidity contentions on October 24, 2017. With full knowledge of the schedule in the ITC Investigation, Petitioner made the strategic decision to wait one full year before filing its redundant attack on the validity of the '490 patent. More significantly, Petitioner waited almost nine months after identifying the Heinrich and Balasubramanian combination before filing this Petition. Thus, before filing the Petition, Petitioner already received the benefit of Patent Owner's expert briefing

⁴ The ITC subsequently extended the Final Determination target date to January 28, 2019 due to the retirement of the originally assigned ALJ. Ex. 2004. The originally assigned ALJ then returned from retirement to complete the ITC Investigation.

and a full ITC hearing on the same underlying issues raised in this Petition.

Moreover, real-party-in-interest Apple has challenged the validity of claims 5 and 31 in the parallel district court case *Qualcomm Incorporated v. Apple Inc.*, Case No. 3:17-CV-01375 (S.D. Cal) (“the District Court case”). Like in the Petition here, Apple relies on the combination of Heinrich and Balasubramanian to invalidate claims 5 and 31. The District Court case will decide the same underlying issues as the ITC and as raised in this Petition, and is scheduled to go to trial March 4, 2019. Ex. 2005.

The Board has previously found lesser facts weigh in favor of denying institution. In *NHK Spring Co.*, the Board denied institution where the parallel district court case was scheduled to go to trial approximately seven months after the institution decision. There, like here, the petitioner relied on the same prior art and the parallel proceeding will resolve the same issues before any trial on the petition concludes. The Board held that “instituting a trial under the facts and circumstances here would be an inefficient use of Board resources.” *NHK Spring Co.*, Case IPR2018-00752 at *19-20.

In *Nautilus*, the Board cited the patent owner’s “persuasive evidence that the ITC investigation involving Petitioner as a respondent and [the same asserted patent] involves some of the same prior art” as one of the primary factors in denying institution. *Nautilus*, Case IPR2017-00426 at *12-13. Here, the overlapping issues

are even more pronounced; Petitioner relies on the exact same prior art combination in the ITC Investigation, the District Court case, and the instant Petition.

Moreover, in *Nautilus*, the Board considered the potential inequity of a petitioner filing serial attacks against a patent, “while benefitting from patent owner’s arguments and/or the Board’s decision in prior cases,” which also weighed in favor of denying institution. *Id.*, *12-13. Here, Petitioner received the benefit of Patent Owner’s expert briefing on the same underlying issues, not just “some of the prior art” like in *Nautilus*, as well as a full hearing on the merits and the Commission Investigative Staff’s (“the ITC Staff”) pre-hearing memorandums, all before filing the Petition. Like in *Nautilus*, the factors here weigh in favor of denying institution.

Finally, by filing the Petition so late, Petitioner and Apple seek to re-litigate an issue that has already been fully litigated in a different forum and will be decided in *two* different forums well before the Board can reach a final written decision. With the Final Determination due January 28, 2019, the ITC Investigation will be complete around the same time as the Board’s institution decision and the District Court trial will be less than two months away. Critically, both the ITC Investigation and the District Court case will have had the opportunity to be appealed and fully briefed by the time the Board’s final written decision is due. The Federal Circuit will publish an opinion and issue its mandate long before an appeal of the Board’s final written decision can be resolved. When another forum will decide the same

issues earlier than the Board, this fact weighs in favor of denying institution. *See NetApp*, Case IPR2017-01195 at *12–13 (denying institution under § 314(a) where, due to petitioner’s delay, the Board likely would not have been able to rule on patentability until after the district court trial date); *NHK Spring Co.*, Case IPR2018-00752 at 20 (finding that the advanced state of a parallel proceeding, where a trial was scheduled to occur six months prior to the Board’s deadline to issue a final written decision, would be an inefficient use of Board resources and weighed in favor of denying the petition under § 314(a)).

Petitioner should not be rewarded for its dilatory efforts with an opportunity to re-litigate the same issues that multiple forums will already decide. For the reasons discussed above, the Board should exercise its discretion under §314(a) and deny institution.

B. Filing Five Separate Petitions Against the Same Patent Is An Unnecessary and Abusive Duplication of Proceedings

Shortly after the Supreme Court’s *SAS* decision, the Patent Office decided that, if it instituted an IPR, it would do so not only on all claims, as is clearly required by *SAS*, but also “on all challenges raised in the petition.” *See* PTAB “Guidance on the Impact of SAS on AIA Trial Proceedings,” April 26, 2018 ([https://www.uspto.gov/sites/default/files/documents/guidance_on_the_impact_of_sas_on_aia_trial_proceedings_%20\(april_26,_2018\).pdf](https://www.uspto.gov/sites/default/files/documents/guidance_on_the_impact_of_sas_on_aia_trial_proceedings_%20(april_26,_2018).pdf)). The Federal Circuit has

since ratified that stance, explaining that “equal treatment of claims and grounds for institution purposes has pervasive support in *SAS*.” *Adidas AG v. Nike, Inc.*, 894 F.3d 1256, 1258 (Fed. Cir. 2018) (quoting *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018)). During its April 30, 2018, Chat with the Chief presentation, then-PTAB Chief Judge Ruschke cautioned that the presence of weak grounds in a petition could result in a complete denial of institution even if other unpatentability allegations met the threshold for institution.⁵ Realizing this, Petitioner has divided its challenges to the ’490 patent claims that would normally fit into one petition (*i.e.*, two grounds challenging 22 claims) across *five* petitions, hoping to increase its odds of institution.

But petition filing tactics that unduly multiply the number of proceedings are ripe for exercise of the PTAB’s discretion under 35 U.S.C. § 314(a). *See American*

⁵ *See* “Chief Judge Guidance: SAS Impact, Motions to Amend, and Claim Construction,” PTAB Litigation Blog, June 5, 2018, available at: <http://www.ptablitigationblog.com/chief-judge-guidance-sas-impact-motions-to-amend-and-claim-construction/> (“Instead, the panel would evaluate the challenges and determine whether, in the interests of efficient administration of the USPTO and integrity of the patent system (*see* 35 USC § 316(b)), the entire petition should be denied under 35 USC § 314(a).”).

Honda Motor Co., Inc. v. Intellectual Ventures II LLC, IPR2018-00349, Paper 9 at 21 (PTAB June 27, 2018). This discretion under § 314(a) is “guided by the statutory requirement [to consider] the efficient administration of the Office [and] the ability of the Office to timely complete proceedings.” *Tittex International, Ltd. v. Precision Fabrics Group, Inc.*, IPR2015-01671, Paper 7 at 6 (PTAB Feb. 11, 2016) (citing 35 U.S.C. § 316(b)). Needless duplication of proceedings is certainly not in the interest of “efficient administration of the Office,” nor does it promote “the ability of the Office to timely complete proceedings.”

Instead, such tactics unnecessarily multiply the amount of material that the Board and Patent Owner must traverse to assess the patentability of the '490 patent claims. Patent Owner is now tasked with the expense of analyzing and responding to five petitions at the preliminary, and possibly trial phases, for no reason beyond Petitioner game playing to avoid the Supreme Court's *SAS* edict. Just as “[m]ultiple, staggered petitions challenging the same patent and same claims raise the potential for abuse” in the *General Plastic* context, so too does such shenanigans in the *SAS* context, where Board and Patent Owner resources are wasted solely to increase Petitioner's perceived institution odds.

Petitioner provides no explanation for its convoluted filing strategy and why it requires 70,000 words (5 * 14,000) to make its case that 22 claims of the '490 patent are unpatentable based on two grounds. The Board has repeatedly instructed

petitioners to explain off-nominal filing strategies to avoid the PTAB's exercise of its § 314(a) discretion. *See Alere Inc. v. Rembrandt Diagnostics, LP*, IPR2017-01130, Paper 10 at 10 (PTAB Sept. 28, 2017) (“[A] petitioner should explain why the second review proceeding is appropriate. Petitioner provides no such reasoning here. Thus, we find this factors weighs strongly in favor of non-institution.”); *see also General Plastic* factor (5).

Petitioner's ruse to circumvent a Supreme Court directive should not be entertained. Petitioner, without explanation, gratuitously duplicates the proceedings, increasing Board and Patent Owner burdens. The PTAB has broad discretion to deny petitions that exhibit abusive tactics under 35 U.S.C. § 314(a). The Board should exercise that discretion here in the interests of efficient operation and integrity of the Office.

VI. THE PETITION SHOULD ALSO BE DENIED ON THE MERITS

The Petition should also be denied because it fails to establish a *prima facie* case of obviousness of the challenged claims. The Petition and supporting declaration fail to establish a motivation to combine Heinrich and Balasubramanian, a finding recently confirmed by ALJ Pender in the ITC Investigation. Furthermore, the Petition and supporting declaration fail to establish that Heinrich or Balasubramanian, alone or in combination, disclose a key limitation of independent claims 1 (from which challenged claims 9 and 11-13 depend), 26, and 27. Because

the proposed ground fails to evidence a motivation to combine the references, and furthermore both references fail to disclose a key limitation of claims 1, 26, and 27, the Petition fails to meet the minimum standard for institution. 37 C.F.R. § 42.108(c).

A. The Asserted References

1. Heinrich

U.S. Patent No. 9,329,671 (“Heinrich”) issued on May 3, 2016 and was filed on January 29, 2013 as Application No. 13/753,174. Heinrich is entitled “Power-Efficient Inter Processor Communication Scheduling.”

Heinrich notes that “for computer systems implemented on user devices, such as mobile smart phones and tablets, it is important to keep the power consumption of the computer system at a low level, because, for example, the power supply to the user device may be limited.” Ex. 1404, 1:14-18. Power consumption can be kept low if processing functions are split across two or more subprocessors rather than all functions being run on an single processor. *Id.*, 1:18-39. FIG. 1 of Heinrich, as annotated below, illustrates its physical assembly of the components:

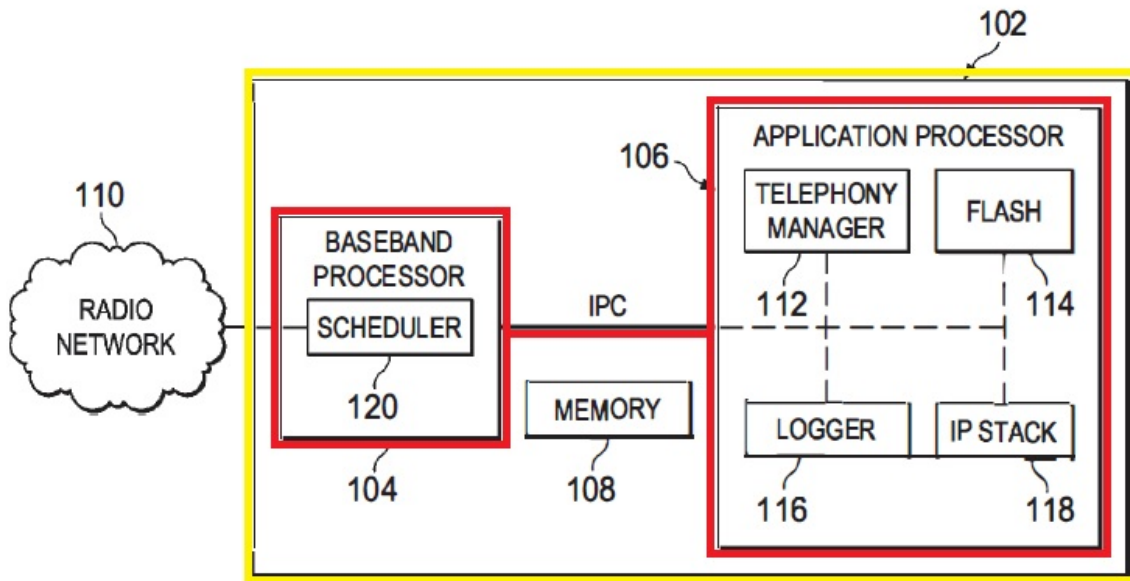


FIG. 1

User device 102, identified above by the yellow box, is a “a mobile phone, a tablet, a laptop computer or other embedded device able to connect to the network 110.” Ex. 1404, 4:22-23. The user device implements a computer system having two sub-systems, each sub-system having a separate processor. *Id.*, 4:23-26. These separate processors are identified above by the two red boxes. There is a physical interface between the two processors for carrying IPC, identified by the red line connecting the two processors. Heinrich defines these communications as “[c]ommunication between the two sub-systems (*i.e.* between the processors of the two sub-systems).” *Id.*, 1:40-42. Heinrich refers to the communications themselves as “IPC activities.” *Id.*, 1:42-43. The focus of Heinrich is thus limited to the activities within a single user device.

Heinrich teaches that the processors may be put into various power modes, for example a sleep mode or an awake mode. *Id.*, 1:54-2:8. In the “awake” mode, a processor is “able to process IPC activities.” *Id.*, 5:19-22. In the “sleep” mode, the processor is not capable of “process[ing] IPC activities.” *Id.*, 5:22-24. Heinrich describes “delaying IPC activities” so that IPC between a first processor and a second processor occurs when the second processor is in an “awake” mode. *See, e.g., id.*, 3:50-4:5.

Heinrich discusses a way for a “scheduler” to “register[] to the underlying physical IPC interface in order to receive notifications of state changes of the IPC interface.” *Id.*, 9:51-53. If the IPC interface is in an active state, that is a clue that the processor on the other side of the interface is also active. *Id.*, 9:54-57 (“The scheduler 120 can perform the determination that the application processor 106 is in the awake mode by receiving a notification that the physical IPC interface is in an active state.”). In other words, the power state of the IPC interface is not interesting by itself in Heinrich, but only as a proxy for the power state of the other processor. Heinrich further suggests using other mechanisms to detect the power state of the processor because the power state of the IPC interface may not change even if the processor is active. *Id.*, 10:37-41. Heinrich’s techniques aim solely at keeping the power state of the processors—not any bus—low. *See, e.g., id.*, 11:49-51; 10:44-51.

A centralized scheduler 120 on a processor “schedules the communication of

IPC activities between the [two] processors.” *Id.*, 7:8-27. The scheduler 120 “identifies IPC activities that are not real-time sensitive and which can be delayed until it is deemed profitable to run them.” *Id.*, 7:65-8:1. On the other hand, IPC activities that are real-time sensitive “are communicated over the IPC interface . . . without delay.” *Id.*, 8:18-20.

Only in the case of non-real-time IPC activities, the scheduler 120 “delays at least one of the identified IPC activities to thereby group the identified IPC activities together into a group.” *Id.*, 8:25-27. This applies to one direction of the traffic between the processors, for example from a secondary processor to the application processor. *Id.*, 8:37-39. Heinrich states that the “method is simple to implement and addresses the problem that IPC activities are asynchronous to each other by grouping non real-time activities together.” *Id.*, 9:30-32. Even in cases where each processor has its own scheduler, the scheduler still only groups together transmissions on one side of the connection. *See, e.g., id.*, 12:47-59.

Heinrich also describes a “lazy timer” scheme that is “inaccurate by design” and is “not provided with a time at which [it] is supposed to fire.” *Id.*, 9:2-8. Each IPC activity is associated with a “lazy timer,” and when any one of the lazy timers on a delayed IPC transmission fires, all delayed IPC activities are transmitted to the other processor. *Id.*, 9:10-21. The lazy timer is described as having a duration in seconds, which is particularly suited for non-essential and non-real time information.

See id., 11:19-20; 11:23-27. This lazy timer approach again only groups data transmissions in one direction.

2. Balasubramanian

U.S. Patent No. 8,160,000 (“Balasubramanian”) was filed as Application No. 11/538,400 on Oct. 3, 2006 and issued on Apr. 17, 2012. Balasubramanian is entitled “Achieving Power Savings Through Packet Grouping.”

Balasubramanian describes how user devices on a WiFi network may be put into a power save mode. Ex. 1405, 1:35-39 (“A communication protocol such as Wi-Fi (based on the IEEE 802.11-related specifications) may support power savings in a wireless communication device by defining procedures that enable the device to transition to a power save mode when it is not transmitting or receiving data.”). Alternatively, a transceiver on a user device may be put into a power save mode. *See, e.g., id.*, 2:55-59 (“In some aspects a method of conserving power in user equipment comprises queueing, in user equipment, a plurality of packets while a transceiver of the user equipment is in a suspended state, and transmitting, by the user equipment, the queued packets during a single wake state of the transceiver.”); 4:63-5:4; 5:30-35; 9:56-58. WiFi packets may be grouped on a particular device in a WiFi network before being sent as a group, in order to reduce power consumption. *Id.*, 1:52-60; 4:1-5.

Balasubramanian thus aims to reduce power consumed by a user device

connected to a network by managing the data transmissions to and from the network.

The physical assembly of components is illustrated in annotated FIG. 1:

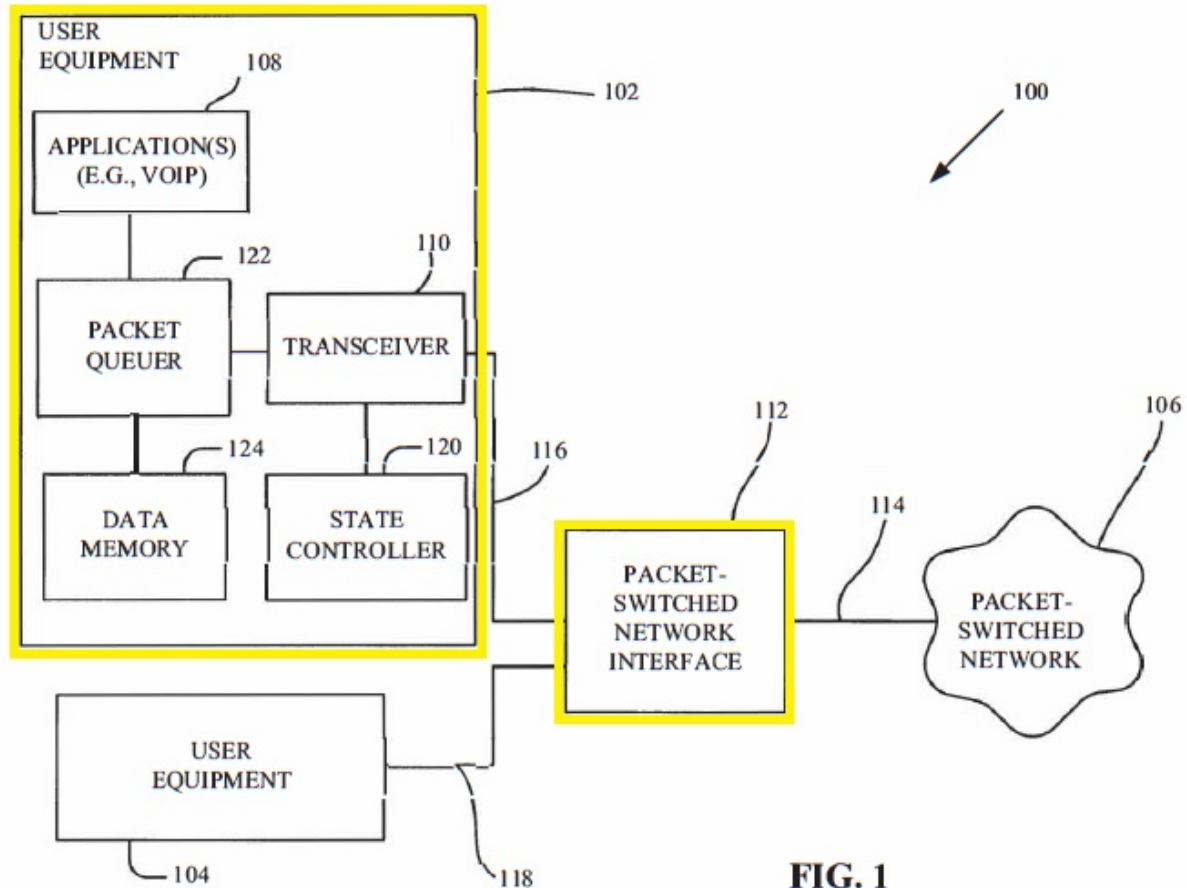


FIG. 1

Ex. 1405, FIG. 1 (annotated). The yellow box on the left encloses a device referred to as “user equipment” 102. Balasubramanian broadly describes “user equipment” 102 and 104 as being “a cellular phone, a smart phone, a cordless phone, a laptop computer, a PDA, a wireless device, a wireless modem, a mobile device, a handset, a handheld device, a satellite radio, a global positioning system, or some other communication device.” Ex. 1405, 4:25-29. The yellow box on the right encloses

a different device referred to as a packet-switched network interface 112. The packet-switched network interface 112 is part of “a sub-network such as a local area network (“LAN”), a personal area network (“PAN”) or some other type of network.” Ex. 1405, 4:45-48. The two different devices communicate with each other in the LAN or PAN over communication links 116 and 118, which may use “a wire-based protocol or a wireless-based protocol.” *Id.*, 4:48-53.

Balasubramanian reduces power consumption by syncing uplink and downlink data transmissions. First, Balasubramanian queues uplink packets in the transceiver 110 and queues downlink packets in the packet-switched network interface 112.⁶ *See id.*, 5:47-51 (“To increase the amount of time the transceiver 110 is in the suspended state (and thereby conserve more power), the user equipment 102 and/or the network interface 112 may be adapted to queue packets while the transceiver 110 is in the suspended state.”). Balasubramanian then transmits the queued uplink packets from the transceiver over the LAN or PAN to the packet-switched network interface. *See, e.g.*, Ex. 1405, 6:60-65 (“For example, the transceiver 110 may acquire access to a communication channel as represented by communication link 116. As represented by block 208, the transceiver 110 then

⁶ Petitioner characterizes the transceiver 110 as a first processing node and the packet-switched network interface 112 as a second processing node. Petition, p. 26.

transmits the queued uplink packets over the communication link 116.”). Upon receiving the uplink packets, the packet-switched network interface transmits its queued downlink packets over the LAN or PAN to the user device’s transceiver in an attempt to get those downlink packets to the user device before the user device’s wake state terminates. *Id.*, 7:4-8 (“For example, the network interface 112 may use the receipt of an uplink packet as a trigger to transmit any downlink packets in its queue.”); 10:21-24. Balasubramanian’s packet-switched network interface provides this reply data relatively quickly to avoid unnecessary user device wake state transitions, not to maintain the wake state of any communication bus, which is not applicable in a multi-path, packet-switched environment.

B. The Petition Fails To Establish A Motivation To Combine Heinrich With Balasubramanian

If the Board reaches the merits, it should deny the Petition because Petitioner has failed to meet its burden of showing a motivation to combine Heinrich with Balasubramanian.

Petitioner challenges claims 9, 11-13,⁷ 26, and 27 as obvious over the

⁷ Claims 9 and 11-13 depend from independent claim 1, which is not challenged in this Petition but was challenged in a related petition. The following

combination of Heinrich and Balasubramanian. Petitioner proposes that a POSITA would have combined Heinrich and Balasubramanian for four reasons: 1) they “are in the same field (communications between processing nodes) and are concerned with the same issues—power consumption when transitioning from low power-to-high power states;” 2) they “both solve the power consumption problem in the same way: minimizing the number of transitions from low-power-to-high power states;” 3) “Heinrich is open to modification in that it discloses the detection state of the physical IPC interface in making decisions about when to transmit data;” and 4) a POSITA “would have been motivated to piggyback the transmission from the application processor back to the baseband processor during the same ‘active’ mode time period and right after data is sent from the baseband processor to the application processor, reducing the number of times the processor enters and exits the active mode.” Petition at 49-52.

Petitioner’s analysis depends on an overly broad characterization of both the relevant field and Balasubramanian’s teachings. For example, both Petitioner and Patent Owner agree that a POSITA would have experience in “mobile device architecture and multiprocessor systems.” *Supra* at 14; Petition at 19.

discussion focuses primarily on claim 1 due to the dependency of claims 9 and 11-13.

Multiprocessor systems are relevant here because the patent is directed to “a mobile terminal” comprising “an application processor” and “a modem processor.” *See* Ex. 1401, claims 1, 16, 22, 26, 27, 28, 29, 31. That is, a multiprocessor system is a user device having multiple processors. Petitioner then drastically expands the relevant field by framing Balasubramanian’s processing components as “a first processing node” and a “second processing node” and relying on the communications between the two, while ignoring that the first processing node is in a user device, and the second processing node is in an entirely different device. Petitioner’s reliance on Balasubramanian is misplaced because the cited passages have nothing to do with grouping data transmissions between two processors in a single user device.

Petitioner’s liberties taken with regard to Balasubramanian are further exposed when Petitioner argues “both Heinrich and Balasubramanian teach similar architectures that include two processing nodes coupled by a bus.” Petition at 49. But the cited passages in Balasubramanian never mention a bus, nor do they refer to communications between two processors in a single user device. Rather, Balasubramanian is concerned with packet-switched network communications between a user device and a network. This is in contrast with Heinrich, which is exclusively concerned with a single user device having multiple processors. *See, e.g.,* Ex. 1404, 4:21-26 (“The user device 102 may be, for example, a mobile phone, a tablet, a laptop computer or other embedded device able to connect to the network

110. The user device 102 is configured to implement a computer system including two sub systems, which each implement a separate processor. FIG. 1 shows the computer system of the user device 102.”); FIG. 1; 1:6-7 (“This disclosure relates to computers and, more specifically, inter processor communication”); 1:24-53; 2:65-3:17; 4:18-50. The alleged “similar architectures” of Heinrich and Balasubramanian are in fact unrelated.

Moreover, Petitioner’s articulation of the problems addressed by Heinrich and Balasubramanian – “power consumption when transitioning from low power-to-high power states” – obscures the fact that Heinrich is concerned with the power states of the *processors*, Balasubramanian is concerned with the power state of a *transceiver*, and neither are concerned with the power state of an interconnectivity bus, like in the ’490 patent.

In the related ITC Investigation, ALJ Pender agreed with Patent Owner and issued an Initial Determination holding that there is no motivation to combine the references:

“[Qualcomm’s expert] provided credible testimony that the Heinrich and Balasubramanian references cannot be combined because their power goals are incompatible with each other, as well as with the ’490 patent. Specifically, Heinrich is focused on power savings for the processor, and Balasubramanian teaches turning a radio transceiver

or an entire device off. By contrast, the '490 patent focuses on saving power on the bus.”

Ex. 2006, 92 (citations to transcript omitted). ALJ Pender further explained:

“Neither Heinrich nor Balasubramanian discloses or otherwise identifies the problem that is addressed by the claimed invention, which is achieving power savings for a mobile terminal with separate modem and application processors by reducing the frequency of power state transitions being made by the interconnectivity bus connecting the processors.”

Id. The ALJ went on to explain that Heinrich and Balasubramanian cannot be combined because they are in different, dissimilar fields:

“Heinrich and the '490 patent are in the field of interprocessor communication (“IPC”), but Balasubramanian does not relate to IPC and is directed almost exclusively to voice over IP (“VoIP”) communications on a WiFi network Due to the many differences between the two fields, Balasubramanian does not suggest that its techniques are applicable to IPC, and Heinrich does not suggest that its IPC techniques could apply to a network like that taught in Balasubramanian.”

Id., 93. Finally, ALJ Pender found that “references cannot be combined because Heinrich’s results alone were outstanding, which would suggest to a person of

ordinary skill in the art that Heinrich's approach should not be modified." *Id.*
"Modifying Heinrich from a push-only system into a very different system wherein
pushes would be coupled with pulls would increase the demands on the application
processor and thus risk the large power savings that Heinrich had already achieved."
Id. at 94.

For these reasons, Petitioner fails to establish a motivation to combine
Heinrich with Balasubramanian, and therefore Petitioner fails to establish a
reasonable likelihood that it would prevail on challenged claims 9, 11-13, 26, and
27. Accordingly, the Petition should be denied.

**C. The Cited References, Alone Or In Combination, Fail To Teach
Or Disclose The Claim 1, 26, And 27 Limitation "the application
processor configured to hold application processor to modem
processor data until triggered by receipt of the modem processor
to application processor data from the modem processor through
the interconnectivity bus after which the application processor to
modem processor data is sent to the modem processor through the
interconnectivity bus responsive to the receipt of the modem
processor to application processor data from the modem
processor through the interconnectivity bus"**

Petitioner relies on the data transmission scheme of Balasubramanian,
combined with the application processor and modem processor of Heinrich, to
purportedly teach the claim 1, 26, and 27 limitation "the application processor
configured to hold application processor to modem processor data until triggered by
receipt of the modem processor to application processor data from the modem

processor through the interconnectivity bus after which the application processor to modem processor data is sent to the modem processor through the interconnectivity bus responsive to the receipt of the modem processor to application processor data from the modem processor through the interconnectivity bus.” See Petition, 35-48, 66, 68-69.

As an initial matter, ALJ Pender found “Balasubramanian is not directed to inter-processor communications within a mobile device terminal and thus, Balasubramanian does not disclose any of the claim 31 limitations.” Ex. 2006, 90. Though the ALJ addressed only claim 31, the analysis applies equally to claims 1, 26 and 27. Like claim 31, claims 1, 26, and 27 involve inter-processor communications within a mobile device terminal. The ALJ’s recognition that “Balasubramanian is not directed to inter-processor communications within a mobile device terminal” necessarily means that Balasubramanian also does not disclose any of the claim 1, 26, and 27 limitations.⁸

But even if the Board chooses to look past this fundamental failing of Balasubramanian, the Board would find that, at most, Balasubramanian discloses using the transmission of *uplink* data packets as a trigger for receiving *downlink* data

⁸ For the same reasons, Balasubramanian also does not disclose any of the claim 9 and 11-13 limitations.

packets queued in the packet-switched network interface. *See* Ex. 1405, 7:4-11 (disclosed embodiment stating only “the network interface 112 may use the receipt of an uplink packet as a trigger to transmit any downlink packets in its queue. Alternatively, the transceiver 110 may send a message to the network interface 112 requesting transmission of all queued packets”). This is the opposite of claims 1, 26, and 27, each of which recite that the receipt of “modem processor to application processor data” (in other words, downlink data), triggers the transmission of “the application processor to modem processor data” (in other words, uplink data). *See* Ex. 1401, 10:46-50 (“While it is conceivable that the uplink data 56 could be sent before the downlink data 54..., such is generally not considered optimal because there are usually far more downlink packets than uplink packets.”).

In discussing the similar limitation in claim 31, ALJ Pender found that Balasubramanian does not disclose the transmission scheme of that claim. Ex. 2006, 91. Claims 1, 26, 27, and 31 all recite the use of downlink data to dictate the transmission of uplink data. Therefore, the ALJ’s finding that Balasubramanian does not disclose the transmission scheme of claim 31 applies with equal weight to claims 1, 26, and 27.

Heinrich does not remedy Balasubramanian’s deficiencies, nor does Petitioner allege that it does. Even if Petitioner had relied on Heinrich in this matter, ALJ Pender considered the merits of Heinrich and found that:

“Heinrich thus neither teaches nor discloses the claim 31 limitations requiring ‘an application processor configured to hold application processor to modem processor data until the modem processor pulls data from the application processor after transmission of the modem processor to application processor data’ and ‘a modem processor [that] is further configured pull data from the application processor after transmission of the modem processor to application processor data.’”

Ex. 2006, 89. Claims 1, 26, and 27 have similar limitations that recite the use of downlink data to dictate the transmission of uplink data. Accordingly, the ALJ’s analysis applies with equal weight to claims 1, 26, and 27. Simply put, “Heinrich does not disclose synchronizing data transmissions in two directions across an IPC bus.” Ex. 2006, 89. Neither does Balasubramanian. *Supra* at 36-38. For these reasons, Petitioner fails to establish a reasonable likelihood that the combination of Heinrich and Balasubramanian discloses this limitation in claims 1, 26, and 27.

For the foregoing reasons, Petitioner fails to establish a reasonable likelihood that it would prevail on claims 1, 26, and 27. Challenged claims 9 and 11-13 depend from claim 1 and therefore, for at least the same reasons as with claim 1, Petitioner fails to establish a reasonable likelihood that it would prevail on challenged claim 9 and 11-13.

VII. CONCLUSION

For the reasons set forth above, Qualcomm respectfully requests that the Board deny institution of the petition for *inter partes* review.

Date: November 21, 2018

/ David M. Maiorana /
David M. Maiorana, Reg. No. 41,449
David B. Cochran, Reg. No. 39,142
Joseph M. Sauer, Reg. No. 47,919
JONES DAY
901 Lakeside Avenue
Cleveland, OH 44114
Tel: (216) 586-7499

Matthew W. Johnson, Reg. No. 59,108
Joshua R. Nightingale, Reg. No. 67,865
JONES DAY
500 Grant Street, Suite 4500
Pittsburgh, PA 15219

Counsel for Patent Owner

TABLE OF EXHIBITS

Exhibit	Description
2001	Intel Corporation's Statement on the Public Interest
2002	ITC Complaint
2003	ITC Scheduling Order
2004	ITC Order No. 44: Initial Determination Extending the Target Date
2005	Southern District of California Scheduling Order
2006	ITC Initial Determination, Excerpts of Public Version

CERTIFICATE OF COMPLIANCE

I, the undersigned, certify that the above Patent Owner Preliminary Response complies with the applicable type-volume limitations of 37 C.F.R. § 42.24 (b)(1). Exclusive of the portions exempted by 37 C.F.R. § 42.24(a), this Preliminary Response, including footnotes, contains 8,276 words, as counted by the word count function of Microsoft Word. This is less than the limit of 14,000 words as specified by 37 C.F.R. § 42.24(a)(i).

Date: November 21, 2018

/ David M. Maiorana /
David M. Maiorana
JONES DAY
901 Lakeside Avenue
Cleveland, OH 44114
Tel: (216) 586-7499

Counsel for Patent Owner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned hereby certifies that a complete and entire copy of the foregoing **PATENT OWNER PRELIMINARY RESPONSE** was served on November 21, 2018 by email, as follows:

David L. Cavanaugh, Esq.
david.cavanaugh@wilmerhale.com

Richard Goldenberg, Esq.
richard.goldenberg@wilmerhale.com

Nina Tallon, Esq.
nina.tallon@wilmerhale.com

Joseph Mueller, Esq.
joseph.mueller@wilmerhale.com

Todd Zubler, Esq.
todd.zubler@wilmerhale.com

Kathryn Zalewski, Esq.
kathryn.zalewski@wilmerhale.com

Theodoros Konstantakopoulos, Esq.
theodoros.konstantakopoulos@wilmerhale.com

Respectfully submitted,

Date: November 21, 2018

/ David M. Maiorana /
David M. Maiorana
JONES DAY
901 Lakeside Avenue
Cleveland, OH 44114
Tel: (216) 586-7499

Counsel for Patent Owner