

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS  
AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR LLC  
Petitioner

v.

INVENSAS CORPORATION  
Patent Owner

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U.S. Patent No. 6,849,946

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**PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 6,849,946**

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1010	Declaration of Martin Cross Regarding Translation of References from Japanese to English
1011	U.S. Patent No. 5,302,551 to Iranmanesh et al.
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1014	U.S. Patent No. 6,109,775 to Tripathi et al.
1015	U.S. Patent No. 6,309,956 to Chiang et al.
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## I. INTRODUCTION

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively “Samsung”) request *inter partes* review (“IPR”) of Claims 16-22 of U.S. Patent No. 6,849,946 (“the ’946 Patent”; Ex-1001), assigned to Invensas Corporation (“Patent Owner”). The ’946 Patent relates to a planar integrated circuit topography that comprises a plurality of “dummy conductors” of intermediate size that are located between a wide conductive line and a series of narrow conductive lines. The use of intermediate-sized dummy lines located between a wide conductive line and narrow lines, however, was well known in the art.

This Petition presents a ground of invalidity that was not considered during prosecution and was not presented in the prior Petition for *inter partes* review filed by Broadcom, in which Broadcom challenged Claim 16 based on Takahashi alone. *Broadcom Limited v. Invensas Corporation*, IPR2017-00107 (“*Broadcom*”), Paper No. 1. Takahashi, the reference previously presented in *Broadcom*, discloses nearly all of the limitations of the asserted claims. The Board, however, previously found that Takahashi does not disclose a plurality of intermediate-sized dummy lines between a wide conducting line and a series of narrow conducting lines. The Board found instead that while Figures 4A-4D of Takahashi visually depict this arrangement, the Takahashi specification neither states that its figures are drawn to

scale nor describes the widths of the conducting lines. *Broadcom*, Paper No. 7 at

9. Thus, the Board denied the Takahashi-based grounds proposed by Broadcom.

*Id.*

This Petition presents Takahashi in combination with Tonishi, which discloses the limitation that the Board previously found to be missing in Takahashi—addresses the claimed arrangement of narrow and wide conducting lines with intermediate-sized dummy lines. Tonishi makes clear that the use of narrow and wide lines was conventional, with narrow conducting lines used to form electrical connections between integrated circuit features, wide conducting lines used to conduct signals between integrated circuit components, wide conducting lines used to transmit power, and intermediate-sized dummy lines disposed between narrow and wide lines. Tonishi thereby discloses the limitation that the Board previously found to be missing in Takahashi. This Petition, accordingly, should be granted on all grounds resulting in cancellation of the challenged claims. The petition is further supported by the Declaration of Dr. Michael Thomas, an expert in the semiconductor manufacturing technologies claimed by the '946 Patent. See Ex-1002, ¶¶6-14.

## **II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8**

**Real Parties-in-Interest:** Samsung identifies the following real parties-in-interest: Samsung Electronics Co., Ltd, Samsung Electronics America, Inc., and

Samsung Austin Semiconductor, LLC.

**Related Matters:** Patent Owner has asserted that Samsung entities infringe the '946 Patent in two separate district court actions: *Invensas Corp. v. Samsung Electronics Co., Ltd. et al.*, Civ. No. 2:17-cv-00670-RWS-RSP (E.D. Tex.) and *Invensas Corp. v. Samsung Electronics Co., Ltd. et al.*, Civ. No. C.A. No. 17-1363-VAC-SRF (D. Del.).

**Lead and Back-Up Counsel:**

Pursuant to 37 C.F.R. § 42.8(b)(3), Samsung identifies the following lead and back-up counsel:

SAMSUNG'S LEAD AND BACK-UP COUNSEL	
Lead Counsel	Brian M. Berliner (Reg. No. 34,549) Email: bberliner@omm.com O'Melveny & Myers LLP 400 South Hope Street, 18th Floor Los Angeles, CA 90071 Telephone: (213) 430-6000 Fax: (213) 430-6407
Back-Up Counsel	Ryan Yagura (Reg. No. 47,191) Email: ryagura@omm.com Nicholas Whilt (Reg. No. 72,081) Email: nwhilt@omm.com  O'Melveny & Myers LLP 400 South Hope Street, 18th Floor Los Angeles, CA 90071 Telephone: (213) 430-6000 Fax: (213) 430-6407

SAMSUNG'S LEAD AND BACK-UP COUNSEL	
	<p>John Kappos (Reg. No. 37,861) O'Melveny &amp; Myers LLP 610 Newport Center Drive, 17th Floor Newport Beach, California 92660 Telephone: 949-823-6900 Fax: 949-823-6994 Email: jkappos@omm.com</p> <p>Mark Liang (Reg. No. L1031) O'Melveny &amp; Myers LLP 2 Embarcadero Ctr., 28th Floor San Francisco, California 94111 Telephone: 415-984-8700 Fax: 415-984-8701 Email: mliang@omm.com</p>

**Service Information:** Samsung may be served at the addresses provided above for lead and back-up counsel. Samsung consents to electronic service at the address: INVENSASSAMSUNGTX17670OMM@omm.com.

### III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

In accordance with 37 C.F.R. § 42.103(a), the Office is authorized to charge an amount in the sum of \$30,500 to Deposit Account No. 50-2862 for the fee set forth in 37 C.F.R. § 42.15(a), and any additional fees that may be due.

### IV. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104(a), Samsung certifies that the '946 Patent is available for *inter partes* review and that Samsung is not barred or otherwise estopped from requesting *inter partes* review on the grounds identified herein.



## **V. PRECISE RELIEF REQUESTED**

Samsung respectfully requests review of Claims 16-22 (the “Challenged Claims”) of the ’946 Patent, and cancellation of these claims, based on the grounds listed below.

- Ground 1: Claims 16-22 are obvious under 35 U.S.C. § 103 over Takahashi in view of Tonishi.

## **VI. OVERVIEW OF THE RELEVANT TECHNOLOGY**

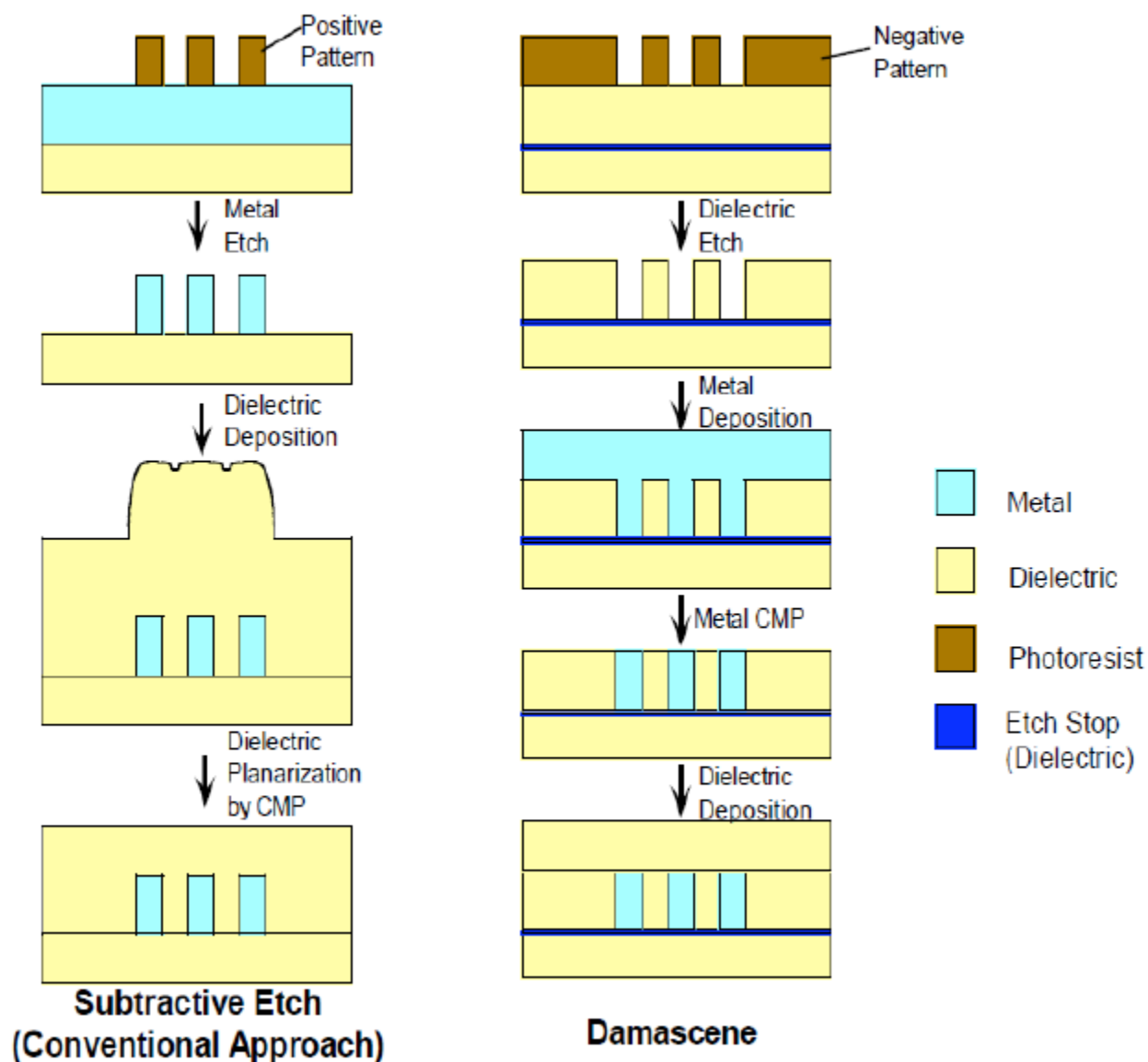
The ’946 Patent is directed generally to technology for forming interconnects in integrated circuits. Ex-1002, ¶18. Interconnects form electrical connections between the transistors and other components in an integrated circuit that allow for power and signal transfer. *Id.* Prior to the mid-1990’s integrated circuits were commonly formed from aluminum interconnects using a “subtractive” etch process, in which metal or conductive material is layered and unwanted material is etched away to leave behind conducting interconnects. However, some integrated circuits formed using non-aluminum conductors were instead formed using an additive “damascene” process in which trenches are formed and conductive material is added. *See, e.g.*, Ex-1011; Ex-1002, ¶18.

By the mid-1990s, the industry began shifting toward the use of copper interconnects that were expected to have improved performance due to lower resistivity compared to aluminum. Ex-1002, ¶19. The industry recognized that

without a move from the existing aluminum-based interconnects to a faster copper-based interconnect system, interconnect performance would limit future integrated circuit device performance. Ex-1012, 10; Ex-1002, ¶19. In September 1997, IBM announced the commercial manufacturing implementation of damascene and dual damascene process technology using copper wiring to replace aluminum-based interconnect systems. Ex-1013; Ex-1002, ¶19. After IBM's disclosure, other companies, such as Motorola and Intel, adopted copper interconnects that remains in use today. Ex-1002, ¶19.

Because copper interconnects are easier to pattern using damascene rather than subtractive etching techniques, use of the additive damascene process to form interconnects increased significantly. Figure 1 below shows the difference between the subtractive and damascene processes, where oxide chemical mechanical polishing (CMP) in the subtractive process (aluminum based) is replaced by metal CMP (copper damascene). Ex-1002, ¶20. In the subtractive method on the left, a layer of metal is deposited on dielectric, a pattern is imaged on the metal with a resist mask, and the metal is etched away leaving behind the metal interconnects. *Id.* In the damascene method on the right, a negative pattern is imaged with a resist mask over the dielectric, and trenches are etched in the dielectric. *Id.* Metal is then added over the dielectric and into the trenches, and the top layer of metal is removed using metal CMP, leaving behind the metal

interconnects within the trenches. *Id.* A final thin layer of dielectric is deposited over the planar interface to prepare the next metallization level. *Id.*



Despite certain differences between subtractive etch and damascene technologies, many of the same principles of integrated circuit manufacturing apply to each. In both the subtractive and damascene processes, planarization by CMP is used to form a flattened, regular semiconductor. By 1997, it was known

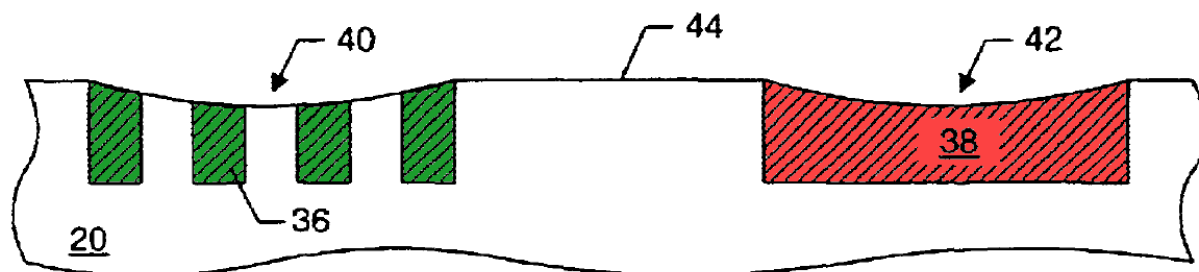
throughout the semiconductor industry that damascene copper CMP processes were susceptible to flatness variations caused principally by interactions between the design layout density and processing of the interconnect with polishing pads/equipment. Ex-1014, 2:27-42; Ex-1002, ¶21. The over-polishing of copper/oxide structures results in two major problems, “dishing” and “erosion.” Ex-1009, 15-16; Ex-1002, ¶21. Dishing is the over-polishing of a region caused by a more rapid etching compared to the surrounding material, and it often occurs on bond pads and power buses—wide interconnects used to transmit large currents. Ex-1002, ¶21. Erosion creates an uneven height of the polished oxide compared to the original oxide thickness, which often occurs within an array of metal signal lines. Ex-1002, ¶21. These problems can adversely affect the yield, reliability and performance of an integrated circuit. Ex-1002, ¶21.

Solutions to improving planarization were also already known. One commonly known solution to the dishing and erosion problems was the addition of “dummy” structures—e.g., conductive lines that are not electrically connected to the circuit, but serve to promote a more even polishing of the integrated circuit as a whole. Ex-1002, ¶22; Ex-1014–1018. By 1998, the use of dummy structures to improve planarization of interconnect layers was already known.

## **VII. THE '946 Patent**

### **A. The Patent Specification**

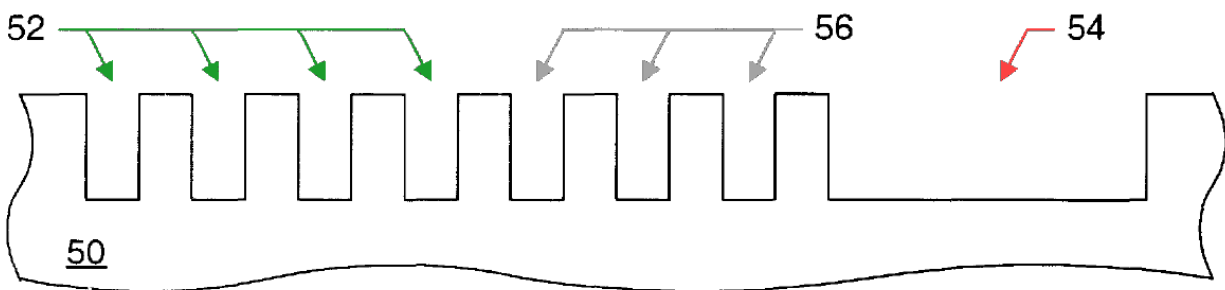
The '946 Patent, entitled “Planarized Semiconductor Interconnect Topography and Method for Polishing a Metal Layer to Form Interconnect,” describes the generation of a “substantially planarized interconnect topography and method for making spaced interconnect by forming a plurality of dummy features in a dielectric between a relatively wide interconnect structure and a series of relatively narrow interconnect structures.” Ex-1001, 1:13-18; Ex-1002, ¶23. According to the '946 Patent, “CMP is commonly used to form a planarized level of an integrated circuit containing interconnect laterally spaced from each other” which is referred to as a “damascene process.” Ex-1001, 2:10-13; Ex-1002, ¶23. The '946 Patent states that “planarization may become quite difficult in a region where there is a relatively large distance between a series of relatively narrow interconnect, or if there is a relatively wide interconnect such as that found in, for example, a bond pad.” Ex-1001, 2:33-37; Ex-1002, ¶23. The '946 Patent describes the dishing and erosion problems known in the art and discussed above. Ex-1001, 2:37-3:44; Ex-1002, ¶23. Annotated Figure 4 shows oxide erosion in the narrow metal interconnects (green) and dishing in the wide interconnect (red).



**FIG. 4**  
**(Related Art)**

The '946 Patent's proposed solution for the dishing and erosion problems is the addition of dummy features, so that the areas with the dummy features are planarized at the same rate as the narrow and wide interconnects. Ex-1002, ¶24.

Figure 5 depicts the addition of dummy trenches 56 (gray arrows) between existing narrow trenches 52 (green arrows) and wide trench 54 (red arrow):



**FIG. 5**

Figure 6 depicts the addition of conductive material 58 (yellow) in accordance with the damascene process:

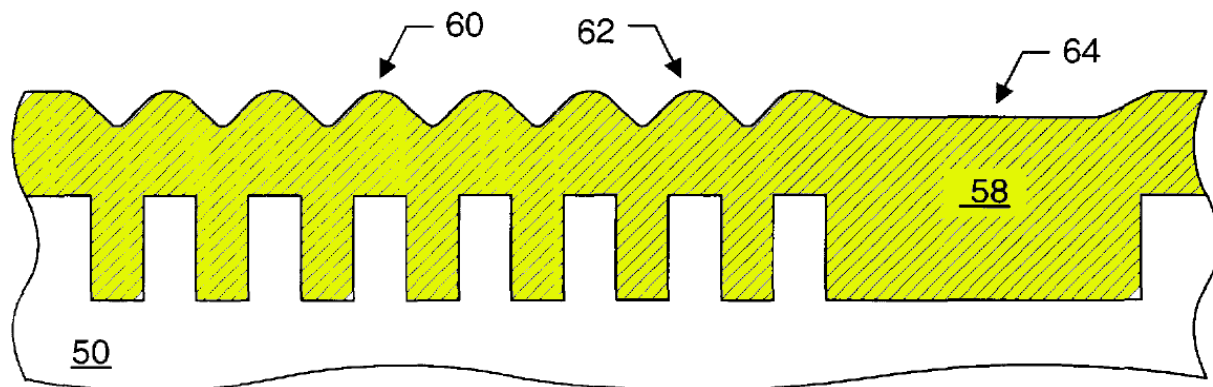


FIG. 6

CMP then occurs, and Figure 7 depicts the resulting planarization of the narrow lines 66 (green), the wide interconnect 72 (red), and the added dummy features 68 (gray):

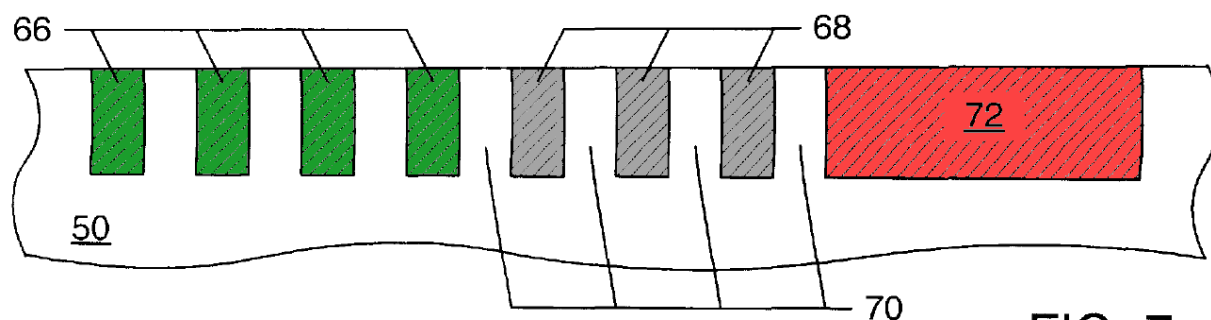


FIG. 7

## B. Prosecution History

The application that eventually issued as the '946 Patent, U.S. Application No. 09/779,123, is a division of U.S. Application No. 09/143,723, which issued as U.S. Patent No. 6,232,231. On July 3, 2002, the Examiner issued a non-final rejection under §103 based on U.S. Patent No. 6,093,631 to Jaso et al. ("Jaso") in view of the admitted prior art disclosed in Figures 1-4 and the related discussion.

Ex-1004, 161-166. After rejection, the Applicant and Examiner exchanged numerous amendments and rejections, with the Examiner issuing a total of four rejections based primarily on Jaso. *Id.*, 161-166, 183-190, 226-232, and 249-255. On April 28, 2004, the Examiner objected to the claims for indefiniteness for using the terms “relatively wide trench” and “relatively narrow trenches,” but no longer rejected the claims based on Jaso. *Id.*, 275-279. Applicant amended the claims to their current form, and on September 30, 2004, the claims were allowed because the Examiner found that Jaso did not “teach nor suggest that the *second* trenches is relatively narrow compared to the first trench” as required by Claims 16-22 at issue in this Petition. *Id.*, 301-303.

## **VIII. LEGAL STANDARDS**

### **A. Claim Construction**

Because the '946 Patent is set to expire on August 31, 2018, before a final written decision, its claims should be construed consistent with the standard for claim construction set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *In re CSB-System Int'l, Inc.*, 832 F.3d 1335, 1341-42 (Fed. Cir. 2016).<sup>1</sup> For the purposes of this proceeding, Samsung does not believe any term

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<sup>1</sup> In addition, the Board has proposed a rule change to apply the *Phillips* standard in all IPR proceedings. 83 FR 21221.



needs construction.

**B. Level Of Ordinary Skill In The Art**

A person of ordinary skill in the art at the time of the purported invention of the '946 Patent ("POSA") would have had a bachelor-level degree in mechanical engineering, materials science, physics, chemistry, electrical engineering, or a related field and 3–5 years of experience or equivalent post-graduate education and training in semiconductor manufacturing. Ex-1002, ¶15.

**C. Review of Previously Considered Prior Art**

Under 35 U.S.C. §325(d), the Board may exercise its discretion to reject consideration of a petition because "the same or substantially the same prior art or arguments previously were presented to the Office." To determine whether to apply §325(d), the Board "first must determine whether any of the grounds asserted in this Petition present the 'same or substantially the same prior art or arguments' as those previously presented to the Office." *Unified Patents Inc. v. Berman*, IPR2016-01571, Paper 10 at 9 (P.T.A.B. Dec. 14, 2016) (informative). If so, the Board then decides whether "it is appropriate to exercise [its] discretion to deny institution" of the asserted grounds. *Id.* at 12.

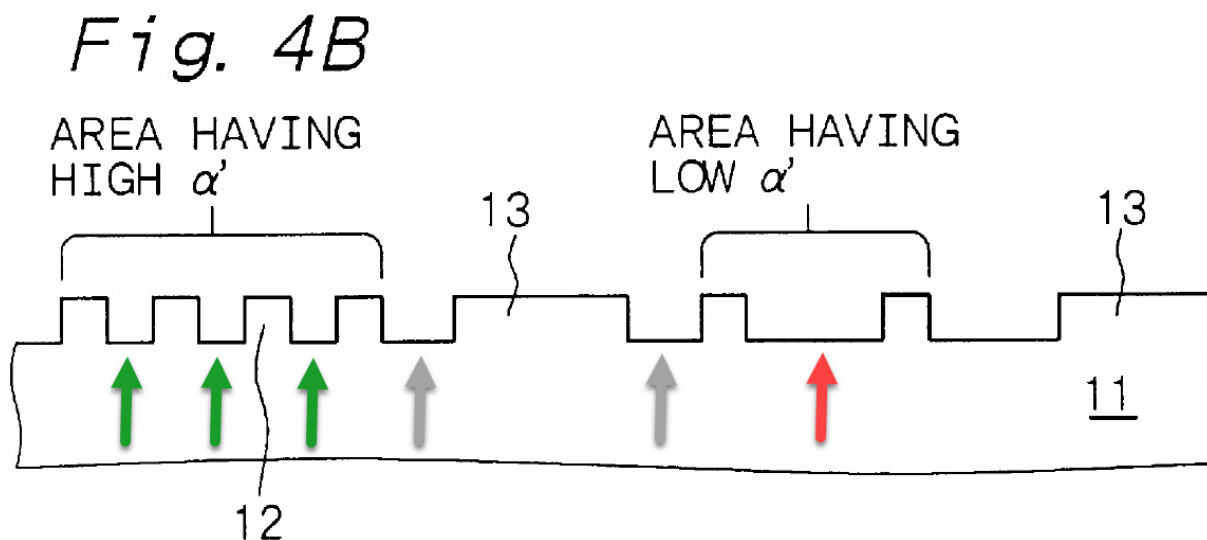
**IX. 35 U.S.C. §325(d) DOES NOT PRECLUDE INSTITUTION OF GROUNDS PRESENTED IN THIS PETITION**

Where a Petition combines previously-presented art with new art that discloses a limitation missing from the previously-presented art, the Petition is not

directed to the same or substantially the same prior art or arguments. In *Unified Patents*, the Board instituted review on a combination of references where the new reference disclosed a key missing limitation not found in the previously considered reference. *Unified Patents*, IPR2016-01571, Paper No. 10 at 11-12 (informative). Similarly, in *L-3 Comms. Holdings Inc. et al. v. Power Survey, LLC*, IPR2014-00834, Paper 9 at 17 (P.T.A.B. Nov. 26, 2014), the Board instituted review on a combination of previously-presented art with new art where the new art was cited “to teach at least some of the features” found absent in the previously-presented reference.

Similarly, this Petition presents new art—Tonishi—that disclose the features the Board found to be missing in a previously-considered reference—Takahashi. In *Broadcom*, the Board determined that Takahashi did not anticipate Claim 16 because it did not disclose the claim’s lateral dimension limitations, which require placing intermediate-sized dummy trenches between a series of narrow trenches and a wide trench. *Broadcom*, Paper No. 7 at 8-9. Figure 4B of Takahashi, annotated below, depicts a series of narrow trenches (green), a wide trench (red), and a pair of intermediate-sized dummy trenches (gray). However, the Board found this disclosure to be insufficient because “patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Broadcom*, Paper No. 7

at 8-9.



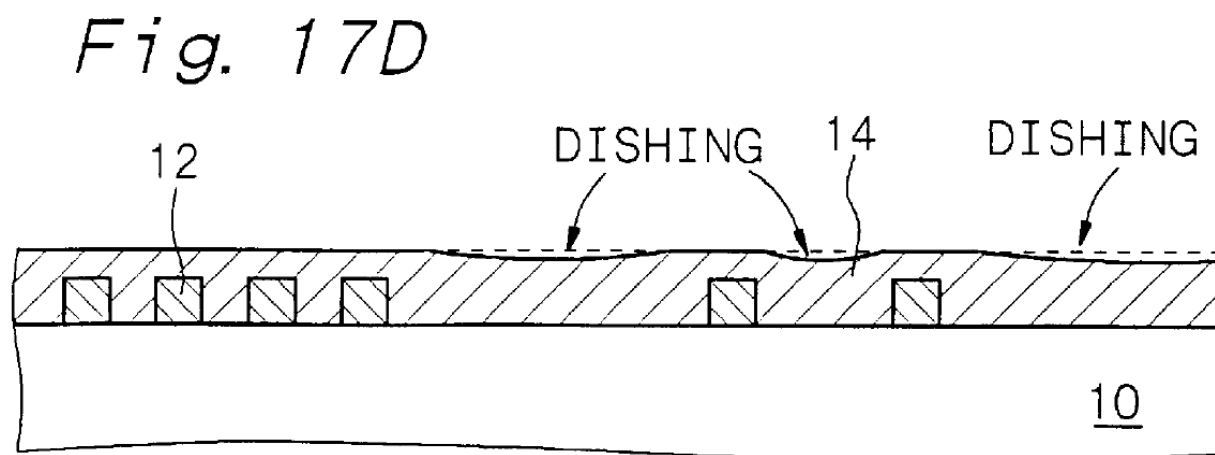
Here, this Petition combines Takahashi with Tonishi—which was not previously considered by the Board—to address the deficiency noted by the Board. As detailed below, Tonishi discloses placing intermediate-sized dummy lines between wide and narrow wires. A POSA would have found it advantageous to combine these teachings with Takahashi in order to improve planarization of these conventional integrated circuits. Therefore, Ground 1, relating to the combination of Takahashi and Tonishi, is neither “the same” nor “substantially the same” as the previously presented ground based on Takahashi. The Board should institute review on the proposed Ground.

## X. OVERVIEW OF PRIOR ART

### A. U.S. Patent No. 5,948,573 (“Takahashi”) (Ex-1005)

Takahashi was filed on February 19, 1998. Ex-1005, Cover. Takahashi is therefore effective as prior art under at least §102(e).

Takahashi is directed to the same object as the '946 Patent of improving planarization and reduce dishing and erosion through the use of dummy features. Ex-1002, ¶30. Takahashi describes how the problem of dishing can occur, using as an example prior art implementing subtractive etch technology as depicted in Figure 17D below:

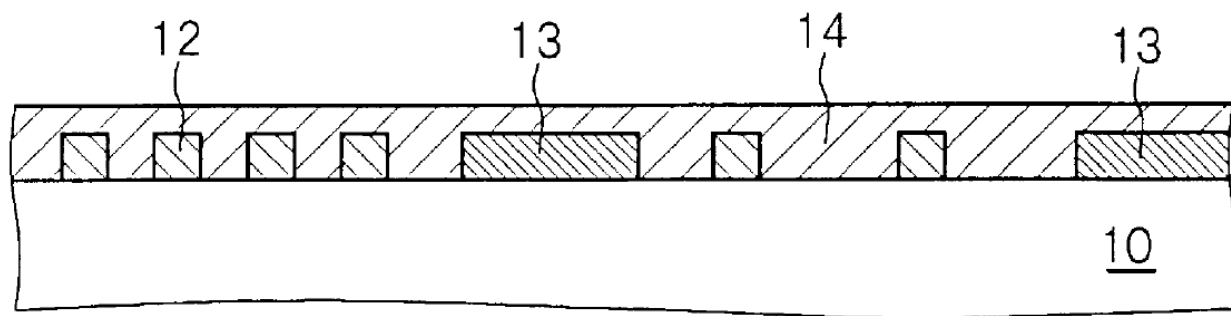


Ex-1005, Figure 17D, 1:56-2:8; Ex-1002, ¶30.

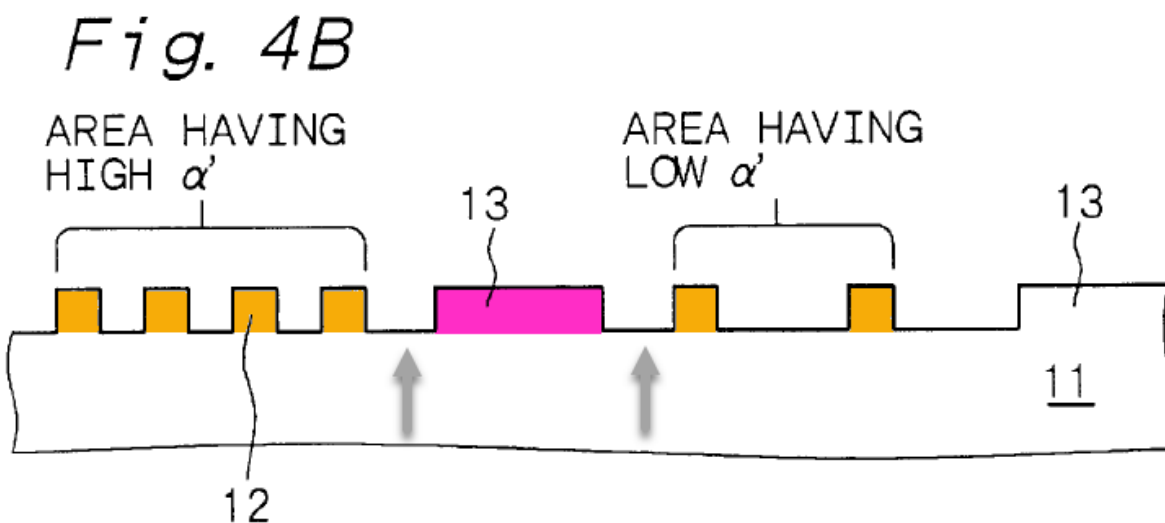
Similar to the '946 Patent, Takahashi discloses placing dummy conductors between interconnects. Ex-1002, ¶31. Figures 3A-D depict the use of dummy metals for a subtractive etch, while Figures 4A-D depict the use of dummy conductors for a damascene process. *Id.* In Figure 3D, the dummy conductor is

described as a “dummy pattern” 13, which is formed from the same material as the wiring. Ex-1005, 15:56-62, 6:35-36; Ex-1002, ¶31.

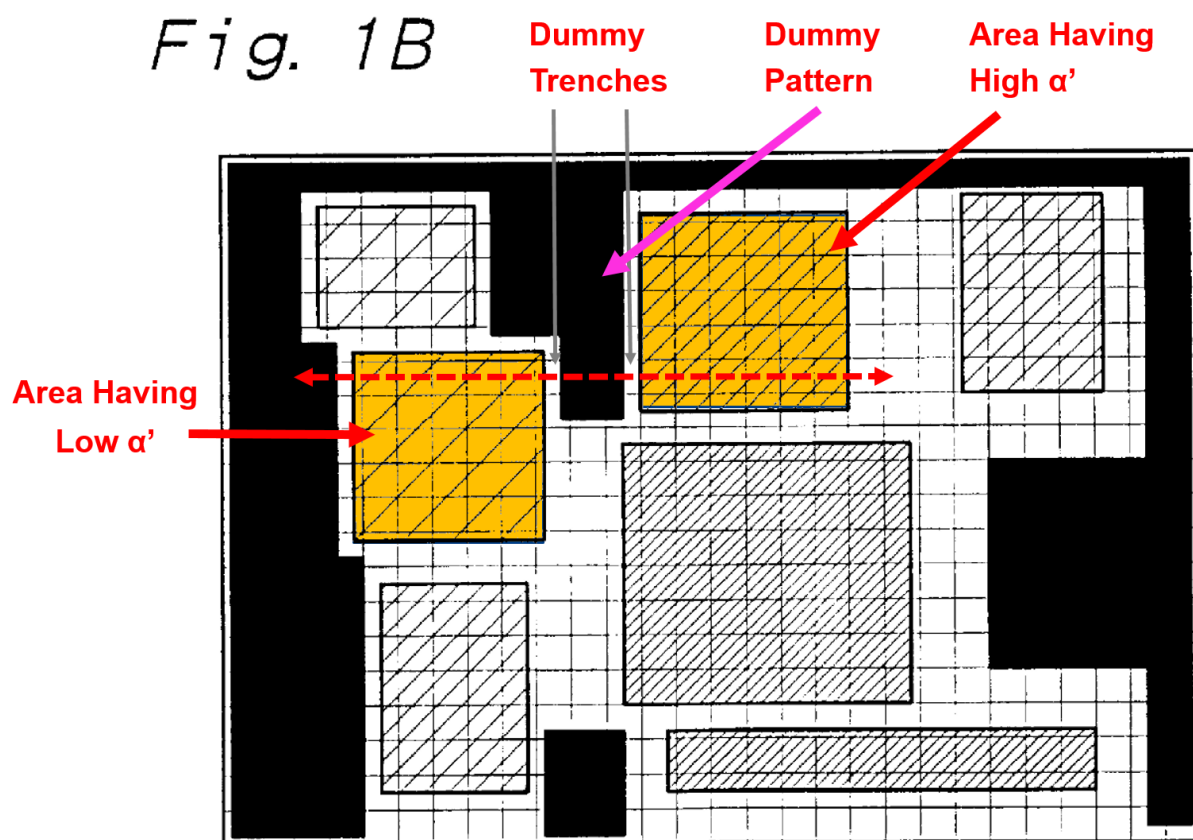
*Fig. 3D*



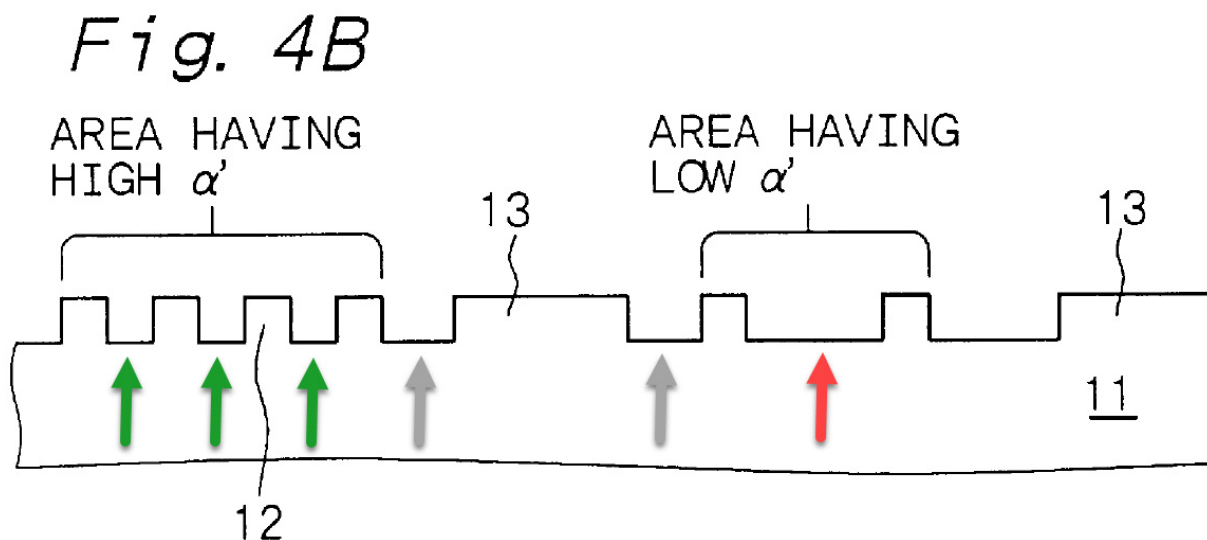
Figures 4A-4D depict the inverse of Figure 3, as it applies the concept of dummy conductors to the additive damascene process instead of the subtractive etch process. Ex-1002, ¶32. There, the dummy pattern is formed of oxide instead of metal. Ex-1005, 16:18-28; Ex-1002, ¶32. The dummy pattern (pink) is separated from the pattern (orange) on each side of the dummy pattern by a space that is, for example, 5  $\mu\text{m}$  in width. Ex-1005, 7:35-40; Ex-1002 ¶32. These two spaces (marked by gray arrows) are dummy trenches.



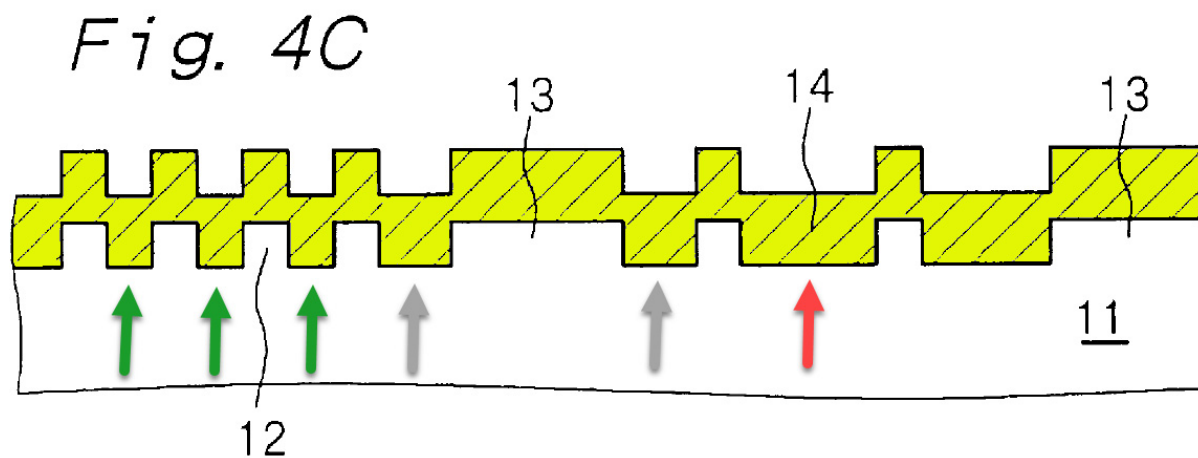
The dummy trenches are also depicted in Figure 1B's plan view as spaces between the circuit blocks (orange) and the dummy pattern (black).



The dummy trenches (gray) are located between a first interconnect trench (red) and a plurality of second interconnect trenches (green):

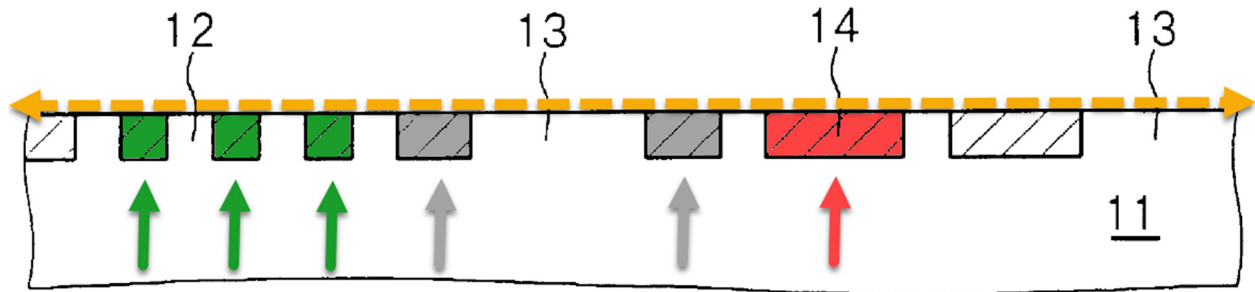


Ex-1005, Figure 4B, 16:18-28; Ex-1002, ¶34. Takahashi depicts adding a metal layer 14 in accordance with the damascene process:



Ex-1005, Fig. 4C, 16:29-43; Ex-1002, ¶34. CMP then occurs, and Figure 4D depicts the resulting planarization of the surface due to the addition of dummy features (gray). Ex-1002, ¶34.

Fig. 4D



As the Board noted in *Broadcom*, although Figures 4A-4D depict placing intermediate-sized dummy trenches (gray) between a wide trench (red) and narrow trenches (green), Takahashi does not expressly state that the images in Figures 4A-4D are drawn to scale.

**B. Japanese Patent Application 4-262535 (“Tonishi”) (Ex-1007)<sup>2</sup>**

Tonishi was published on September 17, 1992. Ex-1007, Cover. Tonishi is effective as prior art under at least §§102(a), (b), and (e). Tonishi was not considered during the prosecution of the ’946 Patent or during the *Broadcom* IPR.

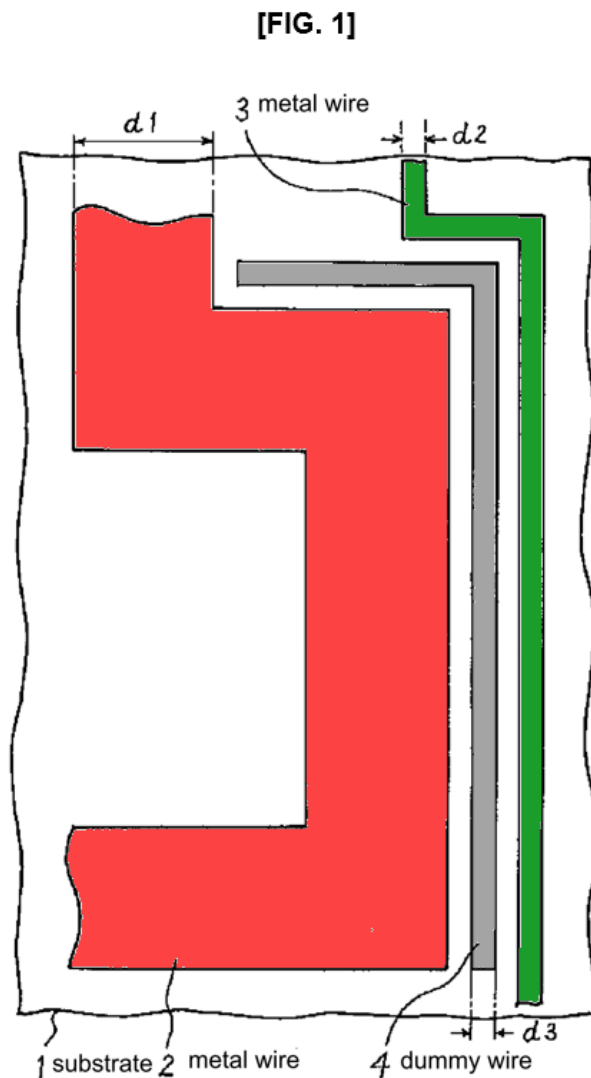
Like the ’946 Patent and Takahashi, Tonishi discloses the use of dummy conductors in an integrated circuit. Ex-1002, ¶37. Specifically, Tonishi discloses

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<sup>2</sup> Throughout this Petition, Samsung refers to the certified translation of Tonishi. A copy of Tonishi in the original Japanese is attached as Ex-1006. A declaration by the translator Martin Cross is included also attached as Ex-1010 certifying that Ex-1007 is a true and correct translation of Ex-1006.



using a dummy wire to prevent lateral hillocks, which are metallic protrusion defects that can occur and ultimately grow to a sufficient size to cause short circuits with adjacent wires. Ex-1007, ¶6; Ex-1002, ¶37. Figure 1 shows one embodiment, in which a dummy wire (gray) is located between a wide wire (red) and a narrow wire (green). Ex-1007, Fig. 1, ¶16-17; Ex-1002, ¶37.



Tonishi further discloses width dimensions for the wide and narrow wires. Ex-1002, ¶38. Specifically, Tonishi explains that in a DRAM or semiconductor

integrated circuit device, “the widths of these metal wires are, for example, a minimum wire-width of approximately 0.8  $\mu\text{m}$  to 1.2  $\mu\text{m}$  for metal wires that transmit electrical signals, and is approximately 40  $\mu\text{m}$  to 80  $\mu\text{m}$  for the thickest metal wires, such as power supply wires and ground wires.” Ex-1007, ¶3; Ex-1002, ¶38. Tonishi also discloses the relative size and position of the dummy wire: “a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.” Ex-1007, ¶11; Ex-1002, ¶38. The dummy wire may be set at a “predetermined wire-width [of] 5  $\mu\text{m}$ .” Ex-1007, ¶12; Ex-1002, ¶38.

Tonishi explains what would have been well known to a POSA—that wire widths are selected to be wide enough to carry current and yet narrow enough to fit highly integrated circuits in a small area. Ex-1002, ¶39. Specifically, Tonishi states that “[t]he wire-widths of the metal wires in this conventional semiconductor integrated circuit device are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life; for example, a wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires, than for other metal wires.” Ex-1007, ¶4; Ex-1002, ¶39. “Meanwhile, with increasing levels of integration in semiconductor integrated circuit devices, it is necessary to arrange metal wires

having wire-widths sufficient to satisfy the conditions described above in a limited area.” Ex-1007, ¶4-5; Ex-1002, ¶39. Tonishi therefore discloses the well-known benefits of using wide, current-carrying lines and narrow interconnect lines. Ex-1002, ¶39.

## **XI. EXPLANATION OF GROUNDS FOR INVALIDITY**

### **A. Ground 1: Takahashi And Tonishi Render Obvious Challenged Claims 16-22**

As discussed below, Takahashi expressly discloses each limitation of Claims 16-22 of the '946 Patent, except for intermediate-sized dummy conductors, a wide interconnect and a plurality of narrow interconnects. A POSA would have found it obvious to apply conventional, prior art arrangements of interconnect and dummy line sizes as disclosed in multiple secondary references, such as Tonishi, in which wide interconnects supply power for the integrated circuit, narrow interconnects are used to connect transistors and carry signals, and intermediate-sized dummy lines. Ex-1002, ¶40. Thus, Takahashi in view of Tonishi renders each of Claims 16-22 invalid as obvious. *Id.*

#### **1. Motivation To Combine Takahashi with Tonishi**

A POSA would have been motivated to utilize the wire width dimensions of Tonishi with the teachings of Takahashi, thereby achieving the purported invention of the challenged claims. Ex-1002, ¶41. There are several reasons why a POSA would be motivated to apply Tonishi's teachings relating to wire width dimensions

to Takahashi:

- First, the uses of wide interconnects, narrow signal lines, and intermediate-sized dummy lines are driven by commonly known design considerations. For example, a POSA would have known that a wide wire is necessary to conduct power to allow large current flow and electromigration life. A POSA would have also known to minimize the width of signal connection wires between transistors to maximize the density of the integrated circuit. A POSA would have further known that dummy lines can be of intermediate size for ease of manufacture. Tonishi expressly teaches such uses and reasons. Thus, a POSA would have known to use the dimensions disclosed by Tonishi in Takahashi because such a combination involves only the use of a known technique to improve a similar device with no unexpected results. *Id.*
- Second, Takahashi and Tonishi each discloses using dummy lines to achieve the overall goal of increasing yields at high integrated circuit densities through improved planarization and prevention of short circuits. Given that they are in a common field of endeavor and disclose similar approaches involving the use of dummy lines, a POSA would have found it obvious to combine the teachings of

Takahashi and Tonishi. *Id.*

**a) A POSA Would Have Been Motivated To Apply  
Tonishi's Interconnect Sizes to Takahashi**

Tonishi discloses reasons and benefits for selecting various wire-widths in integrated circuits that are generally applicable to all integrated circuit designs, including the design disclosed in Takahashi.

Specifically, Tonishi teaches that different wire widths are used in an integrated circuit to transmit signals, provide ground, route power and provide other functions (i.e., resistors, fuses and capacitors, etc.). Ex-1007, ¶1-5; Ex-1002, ¶43. In order to achieve high circuit density, the finest interconnect wires—which were, for example, approximately 0.8-1.2µm—are used to transmit signals between the transistors. Ex-1007, ¶3; Ex-1002, ¶43. Wide wires, typically 40-80µm, were used to serve as power source wires to drive a block, or large blocks of a device, and as the ground wires used for the power return paths. Ex-1007, ¶3; Ex-1002, ¶43. For local power distribution and application specific designs, intermediate sized wires between 5-20µm, were employed. Ex-1007, ¶3; Ex-1002, ¶43.

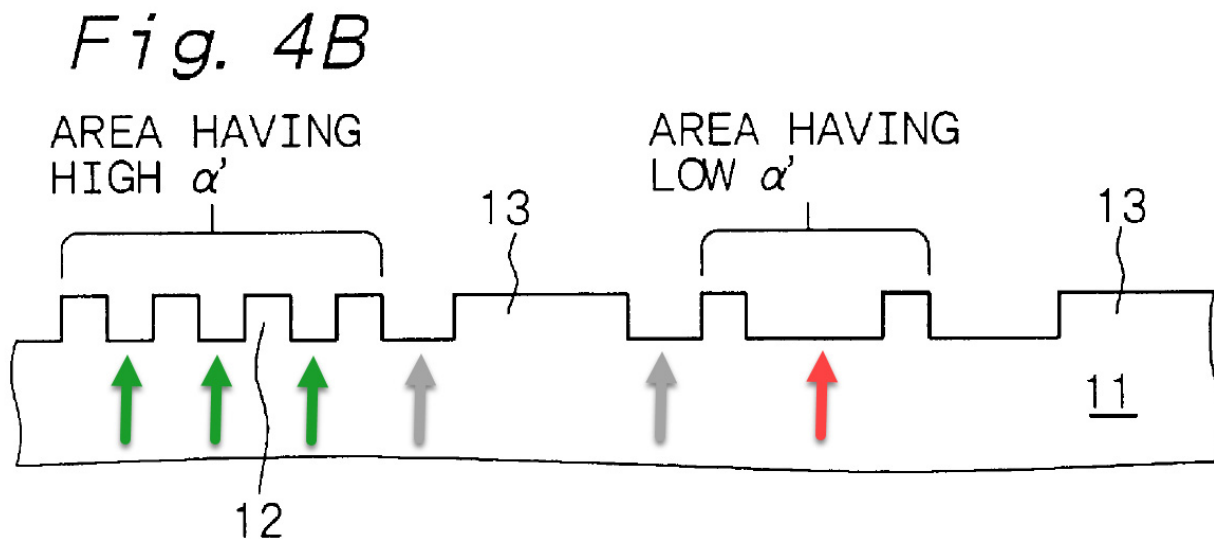
Tonishi discloses the functional benefits of applying various wire widths. A “wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires” in order to reduce noise, provide a stable power source, and improve reliability by minimizing the effects of electromigration. Ex-1007, ¶4. Using narrow wires to conduct signals allows for

“increas[ed] levels of integration” by packing a larger number of circuit components in the same chip area. *Id.*, ¶5. Even as transistor and interconnect sizes scaled to be smaller in the late 1990s, a POSA would have recognized that Tonishi’s teachings relating to the relative sizes of power and signals interconnects are applicable to any design. Ex-1002, ¶44. Thus, a POSA would have been motivated by the benefits taught by Tonishi—such as noise reduction, stable power source, and improved reliability—to select relatively wide wires to transmit power/ground. *Id.* Similarly, a POSA would have been motivated by the benefits taught by Tonishi—such as increased circuit density—to select relatively narrow wires to transmit data signals. *Id.* Accordingly, a POSA would have been motivated by these benefits to apply Tonishi’s wire width selection to Takahashi.

Moreover, Tonishi discloses dummy wires with a preferred “predetermined wire-width [of] 5  $\mu\text{m}$ ”—which is wider than the signal wires but narrower than the power wires. Ex-1007, ¶3, 12; Ex-1002, ¶45. Such sizes are more practical for dummy wires due to the ease of manufacture compared to the very narrow or very wide interconnects. Ex-1002, ¶45. A POSA would have understood and employed interconnects of these various sizes in their circuits and therefore applied the dimensions disclosed by Tonishi to the semiconductor device of Takahashi.

The fact that Takahashi suggests an example of the relative widths that are explicitly described in Tonishi along with dummy conductors of 5 $\mu\text{m}$  further

motivates the combination of the references. Ex-1002, ¶46. Although Takahashi is silent on whether its figures are drawn to scale, its figures must be viewed based on the knowledge of a POSA, as reflected by Tonishi. In *Paice LLC v. Ford Motor Co.*, 722 F. App'x 1015 (Fed. Cir. 2018), the Federal Circuit acknowledged that while the prior art figure alone was insufficient to disclose a limitation, “Ibaraki’s Figure 11, **in combination with the understanding of a person of skill**, thus provides substantial evidence” for finding a disclosure of a claim element. *Id.* at 1021 (emphasis added). Here, Figure 4B of Takahashi depicts the arrangement of trenches in a circuit, including a first trench (red), a set of second trenches (green), and a plurality of dummy trenches (gray).



Ex-1005, Figure 4B, 16:18-28; Ex-1002, ¶46. Figure 4B depicts narrower trenches (green arrows) in the region described as having a high pattern area ratio  $\alpha'$ , and wider trenches (red arrow) in the region described as having a low pattern area

ratio  $\alpha'$ . Ex-1005, 16:18-28; Ex-1002, ¶46. To the extent a POSA would not have understood this width difference from Takahashi alone, Tonishi expressly describes that an integrated circuit typically has wide interconnects, which may be power lines and ground lines for transmitting large amounts of current, and narrow interconnects, which are signal lines for electrically connecting circuit components. Ex-1007, ¶4; Ex-1002, ¶46. A POSA would have, therefore, found it obvious to apply the conventionally-sized wiring dimensions disclosed in Tonishi to Takahashi. Ex-1002, ¶46. Such a combination involves only the use of a known technique (as disclosed in Tonishi) to improve a similar device (as disclosed in Takahashi) with no unexpected results. *Id.*

**b) A POSA Would Have Combined The Complementary Disclosures of Dummy Lines In Takahashi and Tonishi to Improve Yield**

A POSA would have further been motivated to combine Takahashi with Tonishi because both references aim to improve manufacturing yield of semiconductors through the use of dummy features. Ex-1002, ¶47. A POSA would have known that production yield differences of a few percent can make or break the economic viability of a semiconductor production line. *Id.*; see Ex-1019, 1:15-18. Two of the greatest drivers of integrated device manufacturability are yield and density. Ex-1002, ¶47. To achieve high density and yield, a semiconductor manufacturer needs to squeeze every advantage out of the



lithographic process to print minimum sized features without line and space variations. *Id.*; see Ex-1007, ¶5.

Because of the density requirements for these devices, planarization of the interconnect levels was very important towards achieving the highest device yields possible. Ex-1002, ¶48. Poor planarization across the die negatively impacts printed lithographic interconnect feature fidelity, formed by either the subtractive or damascene processes. *Id.* Takahashi teaches that metal dishing can occur during poor flattening. Ex-1005, Fig. 17D, 1:56-2:8; Ex-1002, ¶48. By employing dummy metal interconnect features into a layout between small and larger metal features, Takahashi teaches one how to achieve improved interconnect level planarization with less dishing (i.e., Ex-1005, Fig 17D and 2:6-8) for either subtractive or damascene processes (*id.*, 6:29-56, 15:38-16:6, 16:7-44). The resulting increase in interconnect process margins would improve metal feature fidelity, reliability and yield (*id.* 27:15-19) not only within an interconnect level but between levels. Ex-1002, ¶48.

Tonishi is also directed towards improving device yields. *Id.*, ¶49. It discusses the importance of having a reliable interconnect wiring system that has good electromigration resistance, and is especially resistant to the effects of lateral “hillocks,” which consist of extruded metal that protrudes from the periphery of especially large wires during subsequent heat treatment processes and can

ultimately contact and short-circuit other adjacent metal wires. Ex-1007, ¶4, 10; Ex-1002, ¶49. Tonishi proposes using an interposed dummy metal wire that lies between the unused real estate of a small wire and larger wire to avoid lateral hillock shorting without hindering increases in integration, thereby also increasing yields. Ex-1007, ¶10-12, Claims 1-2; Ex-1002, ¶49.

Thus, a POSA would have been motivated to combine the disclosure of dummy lines in Takahashi to promote greater interconnect level “flatness” with the dummy lines in Tonishi to act as a barrier to shorting, resulting in an attractive solution to enhance the yield of an integrated circuit. Ex-1002, ¶50. Takahashi teaches that flattening treatments (or planarization) using dummy metal trenches are viable for interconnect processes that use either subtractive or damascene processes. *Id.*; *see also* Section X.A., *infra* (discussing how Takahashi is applicable to both subtractive or damascene processes). Takahashi further teaches the use of 5 $\mu$ m dummy trenches. Ex-1005, 7:39-40; Ex-1002, ¶50. Tonishi teaches interposing intermediate-sized dummy lines (5-20 $\mu$ m, with 5 $\mu$ m being a representative width) between wide power supply and ground wires (40-80 $\mu$ m), and narrow signal wires (0.8-1.2 $\mu$ m). Ex-1007, ¶1-5, 11-13; Ex-1002, ¶50. The dummy lines help flatten the surface and act as a barrier to shorting, thereby generating high yield interconnect for multiple “flattened” interconnect levels. Ex-1002, ¶50.

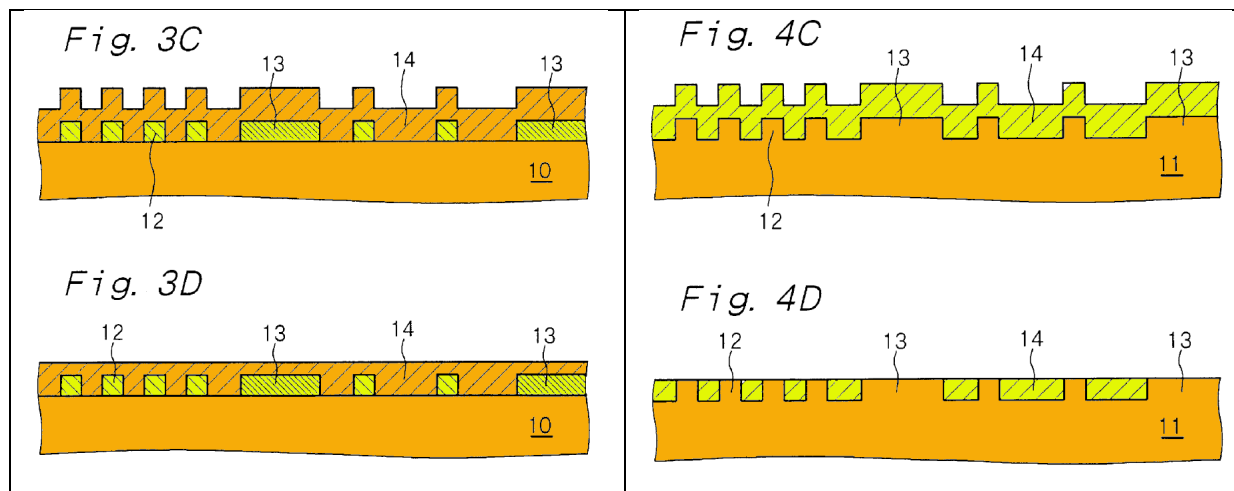
Given that Takahashi and Tonishi are directed to the same field of integrated circuit interconnects, disclose the same objective of increasing yield in high density integrated circuits, and disclose the same approach of using dummy lines to achieve these objectives, and given that these objectives and techniques are shared by the '946 Patent itself, a POSA would have been motivated to apply the teachings of Tonishi to Takahashi to interpose dummy lines of around 5 $\mu$ m between narrow signal lines (e.g., 0.8-1.2 $\mu$ m) and wide power lines (e.g., 40-80 $\mu$ m). Ex-1002, ¶52. Because such a combination would be nothing more than applying known techniques to similar systems, a POSA would have expected the combination to yield a predictable result and be successful. *Id.*, ¶52.

**c) Takahashi Demonstrates That The Dimensions Disclosed In Tonishi Are Applicable To Both Damascene and Subtractive Processes**

Although Tonishi discloses a subtractive process as opposed the damascene process, a POSA would have understood that Tonishi's teachings relating to wire dimensions are applicable to both subtractive and damascene processes. Ex-1002, ¶53. The design considerations relating to the selection of wide wires for power/ground connections and the selection of narrow wires for signal connections are generally applicable to any circuit design regardless of the manufacturing technique used to fabricate its interconnects. Ex-1002, ¶53.

Takahashi confirms that teachings relating to dummy lines are applicable to

both subtractive and damascene processes. Ex-1002, ¶54. Takahashi teaches that the principles of planarization apply regardless of whether it is the dielectric being planarized in the subtractive method or, instead, it is the metal being planarized in the damascene method. *Id.*, see Ex-1005, 6:29-56 (listing numerous exemplary combinations including both dielectric and metal top layers). Takahashi further explains that the metal CMP process shown in Figures 4A-D (“Example 3”) of the specification is a variant of the dielectric CMP process shown in Figures 3A-D (“Example 2”). Ex-1005, 15:38-16:6. Figure 3 thus implements a polycrystalline silicon doped “conductor” and oxide CMP to flatten the overlying oxide, while Figure 4 implements an underlying oxide trench pattern with metal CMP to flatten the overlying metal. Ex-1002, ¶54. The following diagram compares the processes, showing oxide in orange and metal in yellow:



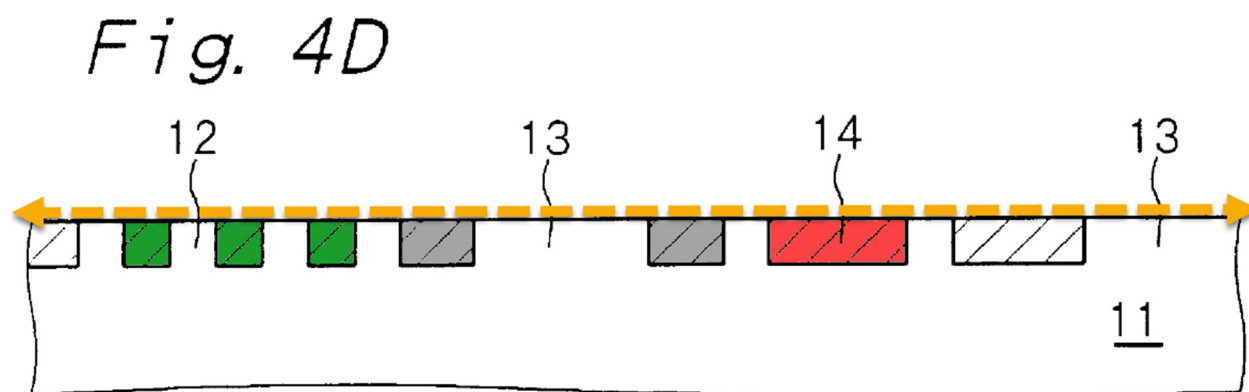
Similarly, a POSA would have understood that design considerations

relating to the selection of wire widths disclosed by Tonishi, like the use of dummy structures, is not dependent on the manufacturing technique. *Id.*, ¶55. Tonishi's teachings are thus fully applicable to Takahashi, which teaches planarization in both a subtractive and damascene process.

## 2. Claim 16

### a) “[a] substantially planar semiconductor topography” (16[pre])

Takahashi discloses using a flattening process, such as chemical-mechanical polishing, to generate a planar semiconductor topography. Ex-1005, 16:18-43; Ex-1002, ¶56. The semiconductor is “**uniformly polished**” due to the use of a dummy pattern 13 (Ex-1005, 16:29-43), resulting in the planar semiconductor topography shown in Figure 4D:



The surface of Figure 4D is “substantially planar” as contrasted with the prior art disclosure of “dishing.” *See, e.g.*, Ex-1005, Figure 17, 2:2-8. Also highlighted in Figure 4D are electrically conductive features shown in the green, gray, and red annotations above. As will be discussed below, green represents

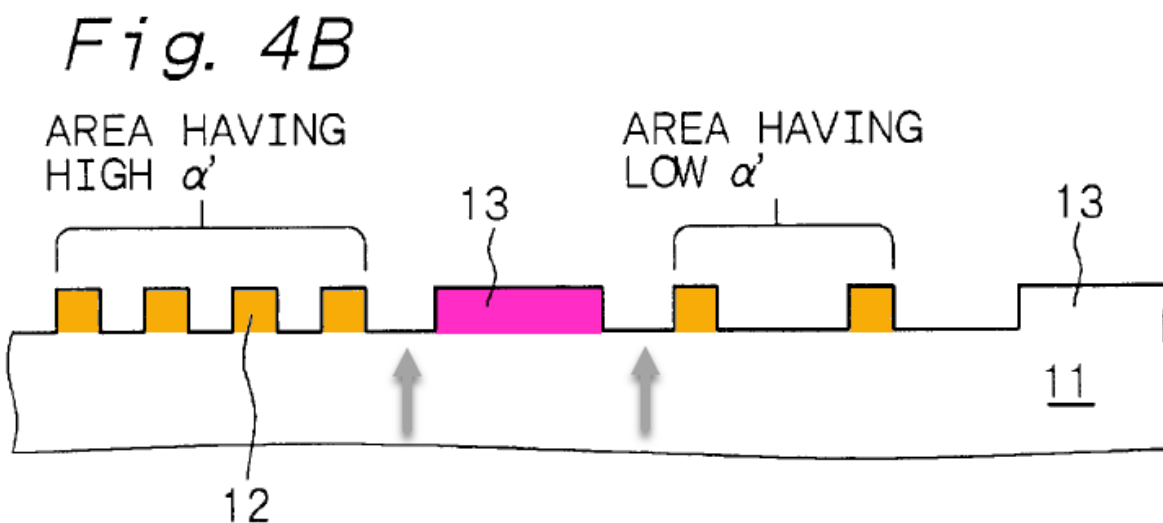
metal signal lines, gray represents dummy lines, and red represents wide metal lines.

Thus, to the extent the preamble is limiting, Takahashi discloses the limitations recited by the preamble.

- b) **“a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches, wherein each of the second trenches is relatively narrow compared to the first trench and wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches” (16[a])**

Takahashi in combination with Tonishi discloses a plurality of intermediate-sized dummy trenches between a series of narrow trenches and a wide trench. Ex-1005, 16:21-25; Ex-1002, ¶58.

Takahashi discloses “a **dummy pattern 13** [] formed concurrently in the first layer 11” as illustrated below in annotated Figure 4B. Ex-1005 16:18-28. The dummy pattern (pink region) is formed of oxide, **“does not overlap a pattern and has a space, e.g., of 5  $\mu\text{m}$  between the pattern and the dummy pattern.”** *Id.*, 7:35-40; Ex-1002 ¶59. As shown in Figure 4B below, there are two spaces (marked by gray arrows) between the dummy pattern (pink) and the pattern (orange).

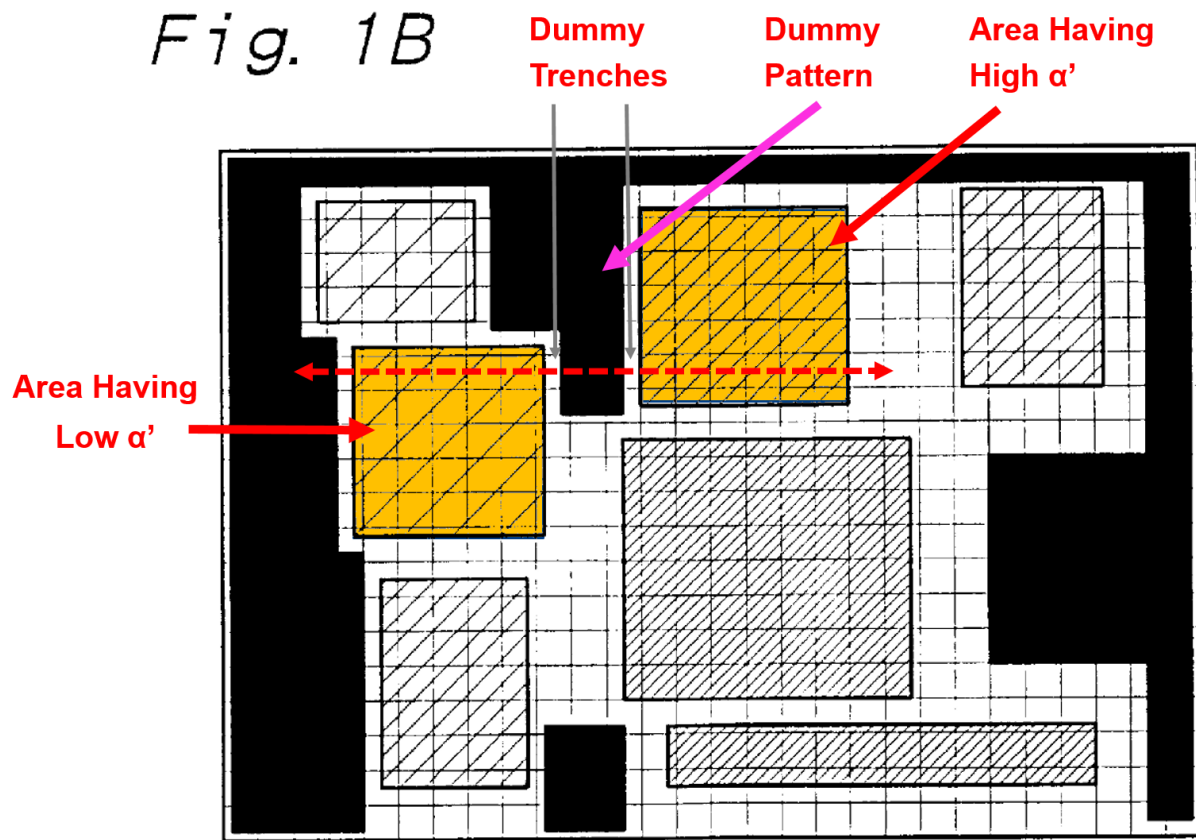


The two spaces (gray arrows) are both “dummy trenches” because they do not connect to or form part of an integrated circuit. Ex-1002, ¶60. Rather, only the two non-dummy “pattern” areas (orange) in Figure 4B, bounded by brackets and labeled the “area having high  $\alpha'$ ” and “area having low  $\alpha'$ ,” form part of an integrated circuit. Ex-1005, Fig. 4B (identifying the pattern as the raised oxide), 7:10-26 (comparing and contrasting “mask pattern” and “dummy pattern”); Ex-1002, ¶60. By contrast, all trenches and raised oxide portions outside of these brackets and labels in Figure 4B are not part of any integrated circuit and are therefore dummy trenches and dummy patterns, respectively.

This understanding of Figure 4B’s boundaries between the integrated circuit patterns (orange) and dummy pattern (pink) and trenches (gray arrows), is confirmed by Figure 1B below, which shows a plan view of these features. In Figure 1B, “rectangular regions surrounded by thick lines show the circuit blocks,

and the circuit blocks having higher pattern area ratios are indicated by hatching more densely.” Ex-1005, 15:13-16. In addition, “the dummy patterns are blackened.” *Id.*, 15:21-22. A cross-section taken of a segment of Figure 1B (dashed red line) corresponds to Figures 4B-4D. Between the dummy pattern (black) and the circuit blocks (orange) are spaces (gray arrows) that, in a damascene process, constitute trenches between the dummy pattern and the circuit blocks. Ex-1002, ¶61. The circuit block area having high  $\alpha'$  with dense hatching is on the right, and the circuit block area having low  $\alpha'$  with sparse hatching is on the left. Further, a space of 5 $\mu\text{m}$  is present between the dummy pattern and the circuit blocks. Ex-1005, 7:39-40; Ex-1002, ¶61.

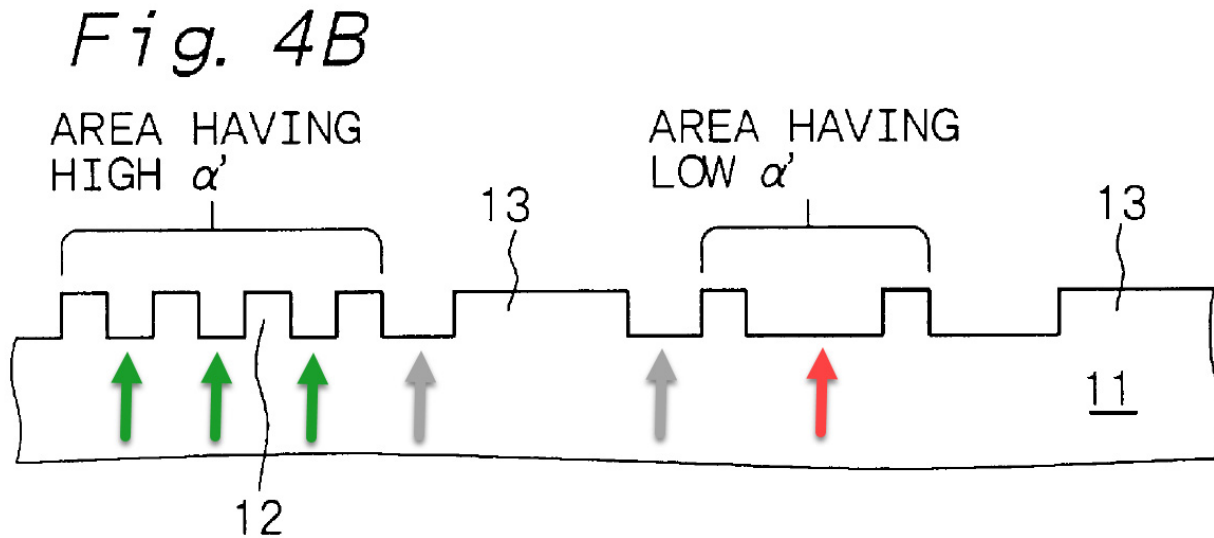




Thus, in Figures 1B and 4B-D, the two spaces located between the patterns or circuit blocks (orange) and dummy pattern 13 (pink or black) are trenches that are not part of any integrated circuit and are therefore dummy trenches. Ex-1002, ¶62.

The pair of dummy trenches are located between a first trench (red arrow) and a series of second trenches (green arrows) as illustrated below in annotated 4B. Ex-1005, 16:18-28. Figure 4B depicts narrow trenches (green arrows) in the region described as having a high pattern area ratio  $\alpha'$ , wide trenches (red arrow) in the region described as having a low pattern area ratio  $\alpha'$ , and intermediate-sized

trenches (gray arrow) in between. *Id.*, 16:18-28; Ex-1002, ¶63.

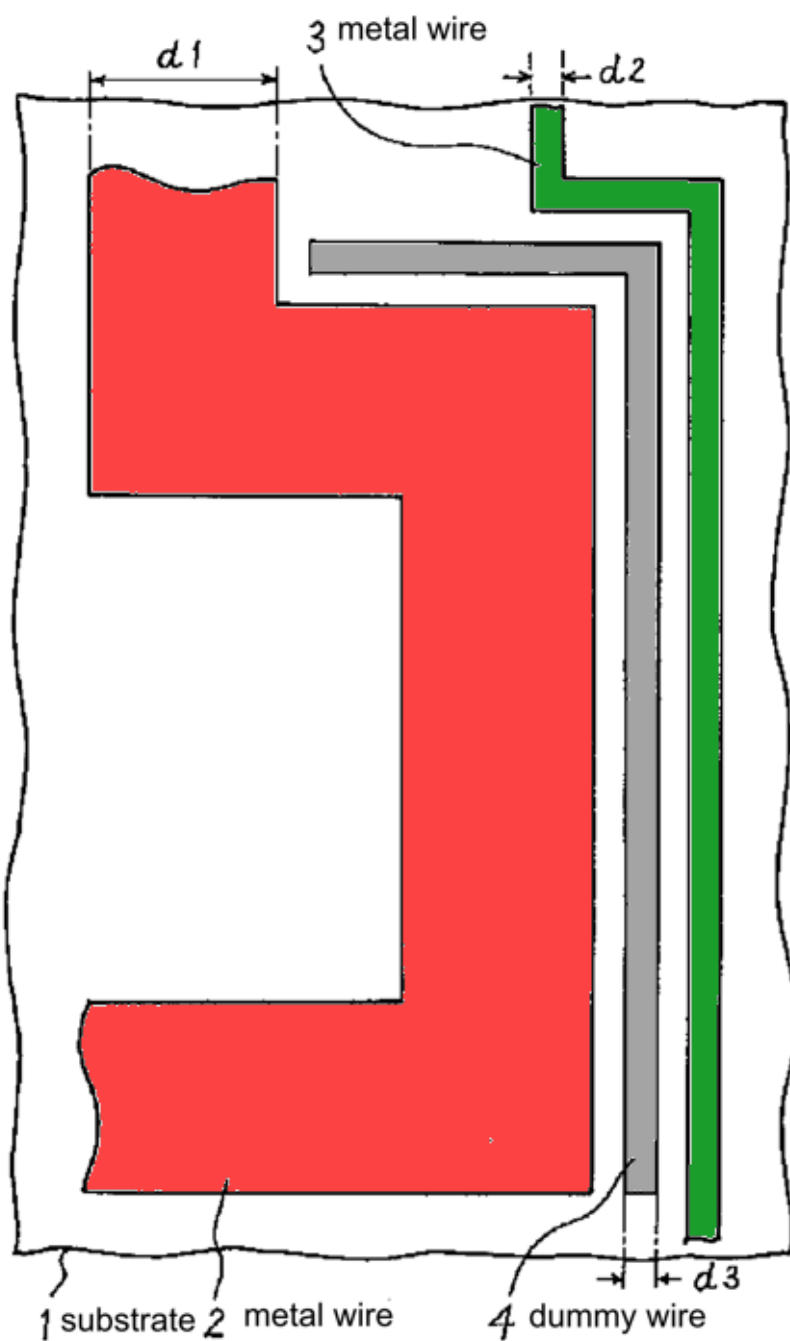


Takahashi does not expressly disclose the lateral dimensions of its first or second, trenches. As discussed in Section X.A., Takahashi suggests an example in which trenches in the low pattern area ratio  $\alpha'$  region (red) have a wider width and trenches in the high pattern area ratio  $\alpha'$  region (green) have a narrower width. Ex-1002, ¶64. A POSA would have found the lateral dimension limitations of Claim 1 obvious from Takahashi in light of Tonishi, which expressly discloses the dimensions of a typical set of interconnects meeting the limitations. It would have been obvious for a POSA to combine with Takahashi for the reasons discussed in Section XI.A.1. *Id.*

Tonishi discloses a configuration in which “[a] dummy wire 4 is provided between a first metal wire having a wide [wire-width] and a second metal wire 3 having a narrow wire-width.” Ex-1007, Abstract. With respect to the wide

and narrow wires, Tonishi teaches that their widths are conventionally selected to meet minimal current flow needs—with wider widths to allow for large current flow and electromigration life, and narrower widths to allow more features to be integrated into the same space. *Id.*, ¶4-5; Ex-1002, ¶65. Tonishi thus explains that “[t]he wire-widths of the metal wires in this conventional semiconductor integrated circuit are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life. . . . [T]he minimum wire-width of each of the metal wires is defined according to the individual application.” Ex-1007, ¶4. Tonishi specifies conventional sizes of such features is **“for example, a minimum wire-width of approximately 0.8  $\mu\text{m}$  to 1.2  $\mu\text{m}$  for metal wires that transmit electrical signals, and is approximately 40  $\mu\text{m}$  to 80  $\mu\text{m}$  for the thickest metal wires.”** *Id.*, ¶3. In describing Figure 1, Tonishi contrasts a wide wire—*e.g.*, a power supply wire or a ground wire—of 40  $\mu\text{m}$  (red) from a narrow electrical signal wire of 1  $\mu\text{m}$  (green). Disposed between these wires is a dummy wire (gray).

[FIG. 1]



Ex-1007, Fig. 1, ¶16; Ex-1002, ¶65.

A POSA would have understood that Tonishi's teachings relating to the use of wide power wires and narrow signal wires—with the signal wires being used to

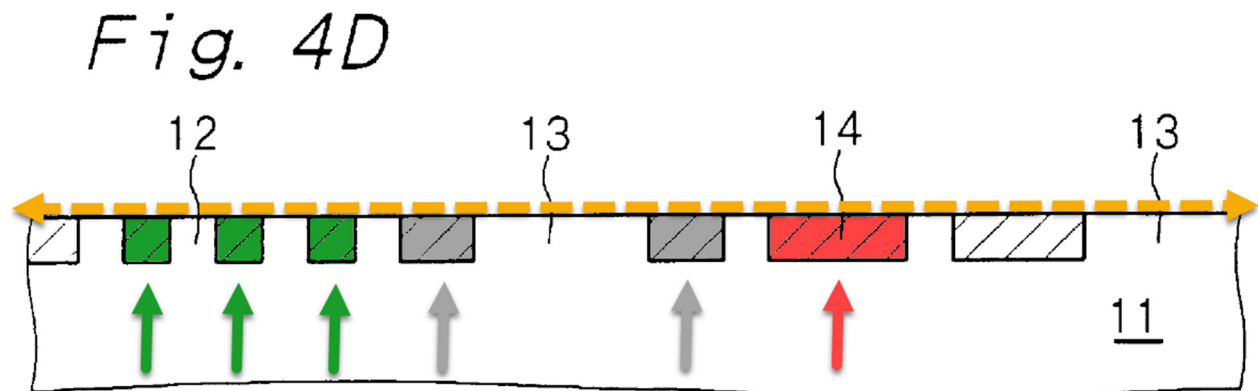
achieve higher density and the power wires being wider to carry greater current—are conventional in the art and applicable to all circuit designs, including the Takahashi device. Ex-1002, ¶66. Moreover, a POSA would have recognized that the benefits disclosed by Tonishi for its selection of relative wire widths (as explained above in Section XI.A.1) are applicable to Takahashi. *Id.* Applying the teachings of Tonishi to Takahashi, a POSA would have understood that the trenches used to form these interconnects would consist of a wide trench and a series of narrow trenches, with dummy wires to both improve planarity and prevent lateral hillocks. The reasons to combine are further explained above in Section XI.A.1.

With respect to the dummy wire, although the specific dummy wire (gray) embodied by Figure 1 is described in some passages of Tonishi as being “substantially equal to” the narrow metal line (green), Ex-1007, ¶16, other passages disclose more generally a first wire “wider than a predetermined wire-width,” a second wire “narrower than a predetermined wire-width,” and **“a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width.”** Ex-1007, ¶13, Claim 1; Ex-1002, ¶67. Thus, Tonishi discloses a dummy conductor of intermediate size located between a narrow conductor and wide conductor.

Thus, Takahashi in combination with Tonishi discloses this claim limitation.

- c) “dummy conductors in said laterally spaced dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and” (16[b])

Takahashi in combination with Tonishi discloses this limitation. Takahashi discloses that once the conductive material is deposited, the second layer 14 is polished, i.e., “flattened by a CMP process using, for example, the polishing apparatus shown in FIG. 11,” resulting in the planar topography shown in annotated Figure 4D below.

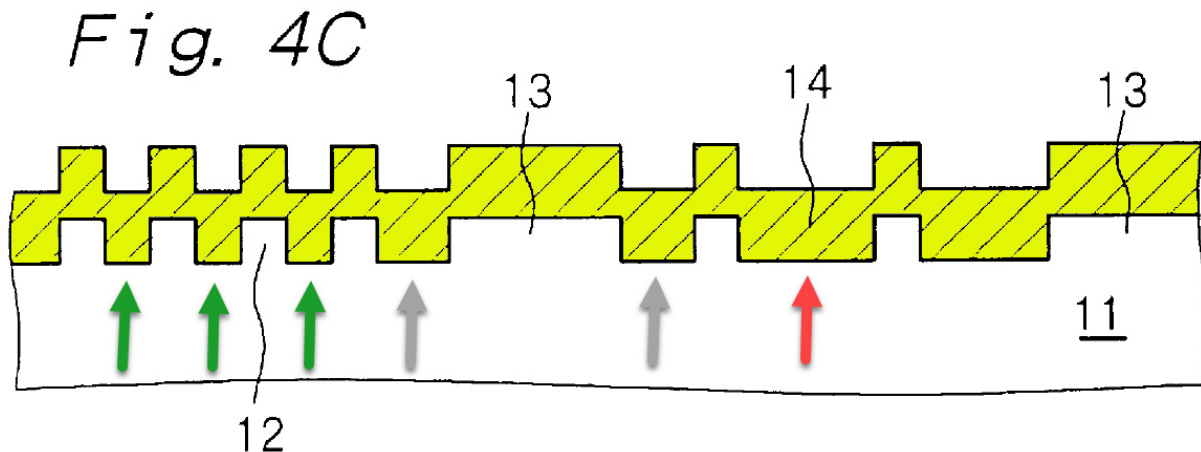


Ex-1005, 16:34-36 and Fig. 4D; Ex-1002, ¶69. Polishing and flattening the second layer 14 until the patterned first layer 12 is exposed results in conductive material in the trenches—dummy (gray), first (red) and second (green) trenches. *Id.* (“As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first later 11 can be effectively prevented, or the excessive polishing of the second layer 14 can also be effectively prevented”); Ex-1002, ¶69. The conductive material exclusively in the dummy trenches (red arrows) form the dummy conductors (red boxes) and the

conductive material exclusively in the first trench (red arrows) and second trenches (green arrows) form the interconnects (red and green boxes).

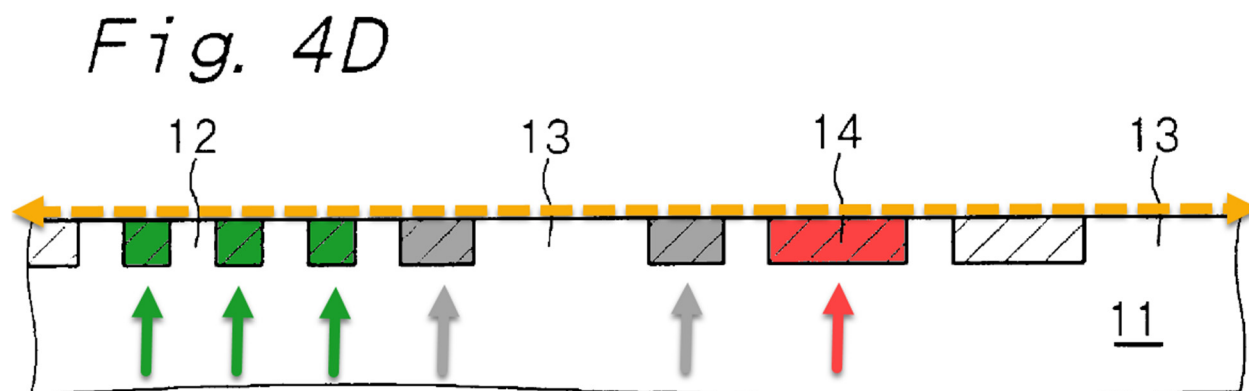
Takahashi's dummy conductors are electrically separate from other "electrically conductive features." Takahashi explicitly directs that the "dummy pattern" **"means a pattern which does not constitute any circuit of an integrated circuit."** Ex-1005, 7:25-26; Ex-1002, ¶70. Takahashi further explains that **"a dummy pattern [] does not overlap a pattern and has a space, e.g., of 5  $\mu\text{m}$  between the pattern and dummy pattern."** Ex-1005, 7:38-40; Ex-1002, ¶70. As discussed in limitation 1[a], the space between the circuit and the dummy pattern constitutes a dummy trench.

That trench, which "does not overlap a pattern" that forms part of the circuit is filled with conducting material. Ex-1005, Fig. 4C, 16:29-34; Ex-1002, ¶71.



The metal is then flattened leaving behind conductors that are not part of the circuit pattern—i.e. dummy conductors that are electrically separate from the

interconnects and other conducting features. Ex-1005, Fig. 4D, 16:34-36; Ex-1002, ¶72.



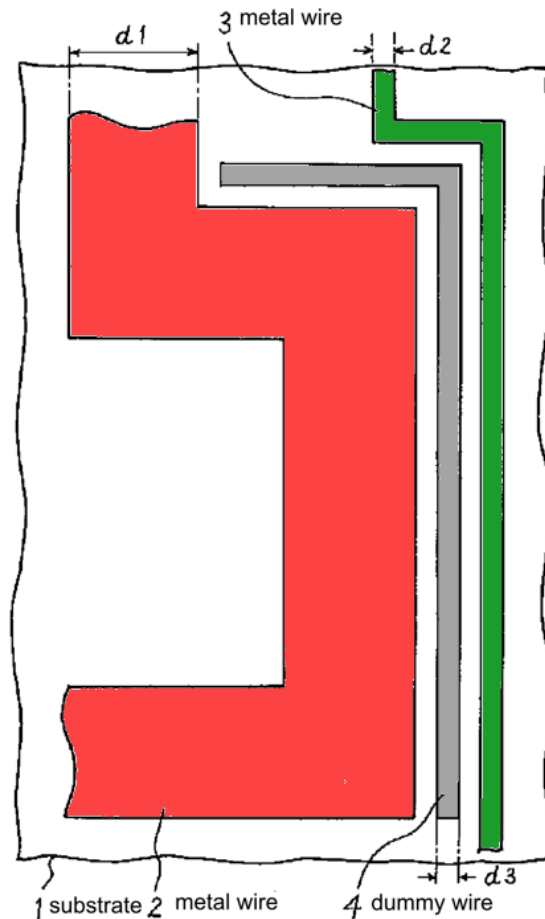
Takahashi further discloses additional conducting features below these electrically separate dummy conductors. Ex-1002, ¶73. The conductive material in Figure 4D is formed in a “first layer 11” “deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub>.” Ex-1005, 16:20-21. Takahashi also discloses that Figure 4D’s “Example 3” embodiment is part of a “method of manufacturing an **integrated circuit**,” where “for example, a buried (embedded) wiring can be formed” and this “wiring” refers to the thin wiring in region 12 (green) and wide wiring 14 (red). *Id.*, 16:13-17, 16:29-36. Takahashi further discloses an “Example 6” embodiment that, like “Example 3,” is a variant of the same “first aspect of the present invention” and for Example 6, Takahashi clarifies that “the underlayer is composed of a plurality of layers (N layers).” *Id.*, 18:56-58; *see Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) (finding that teachings of two related embodiments in prior art patent could



be considered together). A POSA would understand that in this “integrated circuit,” each of these layers would comprise additional conductive features such as transistors, inductors, and additional metal lines, and therefore these electrically conductive features are under the dummy conductors in Figure 4D. Ex-1002, ¶73. The dummy conductors are electrically separate from electrically conductive integrated circuit features below them. In particular, the dummy conductors are electrically separate from constituent conductive features of “an integrated circuit” on a “substrate 21 composed of, for example, a silicon semiconductor substrate.” Ex-1005, 16:46-65; Ex-1002, ¶73.

Tonishi also discloses the use of dummy connectors that are electrically separate from other electrical features. Ex-1002, ¶74. Tonishi discloses variations on the use of dummy wires. In one embodiment, as shown in Figure 1, the dummy wires are electrically separate from electrically conductive features. Ex-1007, Figure 1, ¶16 (“a dummy wire 4 that . . . is formed between the first metal wire 2 and the second metal wire 3, **electrically isolated from the first and second metal wires 2 and 3.**”).

[FIG. 1]



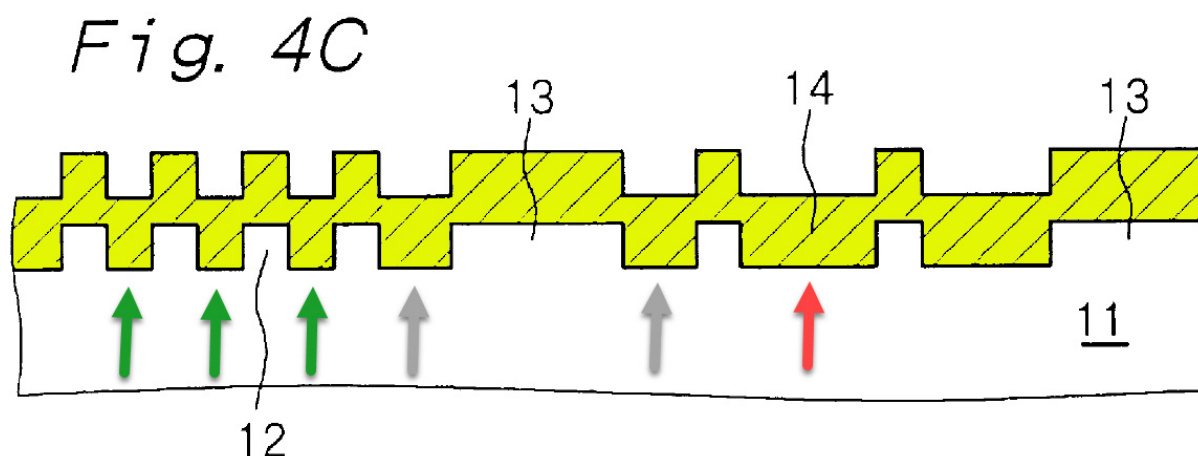
A DRAM semiconductor integrated circuit as disclosed in Tonishi would consist of multiple layers of interconnects beneath the dummy line that are likewise electrically separate from the dummy line. Ex-1002, ¶75. The reasons to combine Takahashi and Tonishi are explained above in Section XI.A.1.

Thus, Takahashi in combination with Tonishi discloses this claim limitation.

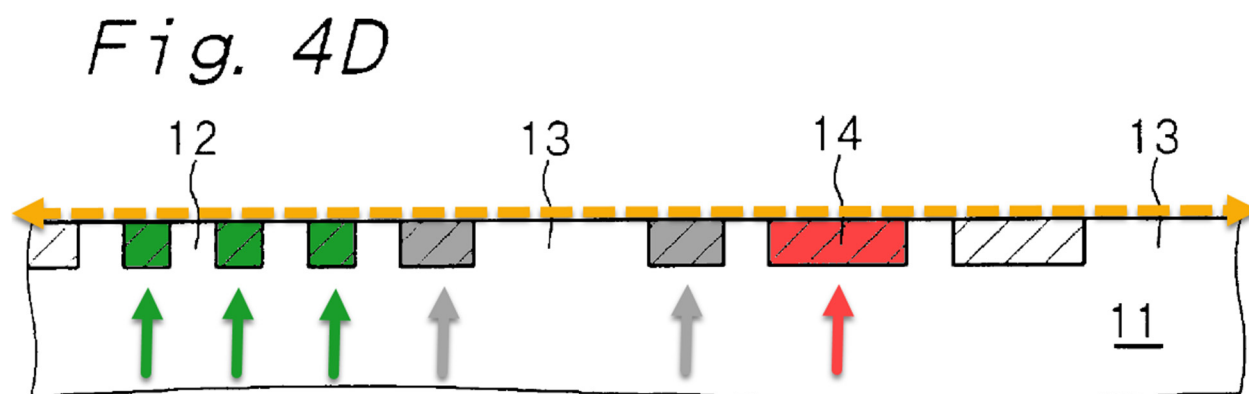
- d) **“conductive lines in said series of second trenches and said first trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces” (16[c])**

Takahashi in combination with Tonishi discloses this limitation. Takahashi

discloses that the upper surface of the conductive lines are coplanar with the dummy conductor upper surfaces. Takahashi discloses a damascene process where a metal layer 14 is deposited on the entire surface of the semiconductor covering the dummy trenches (gray arrows), first trench (red arrow) and second trenches (green arrows), as shown in annotated Figure 4C:



The metal layer is “**flattened by a [CMP] process** using, for example, the polishing apparatus shown in FIG. 11,” resulting in a planar topography shown in annotated Figure 4D:



Ex-1005, Fig. 4D. Takahashi discloses “**uniform polishing**” to form the planar

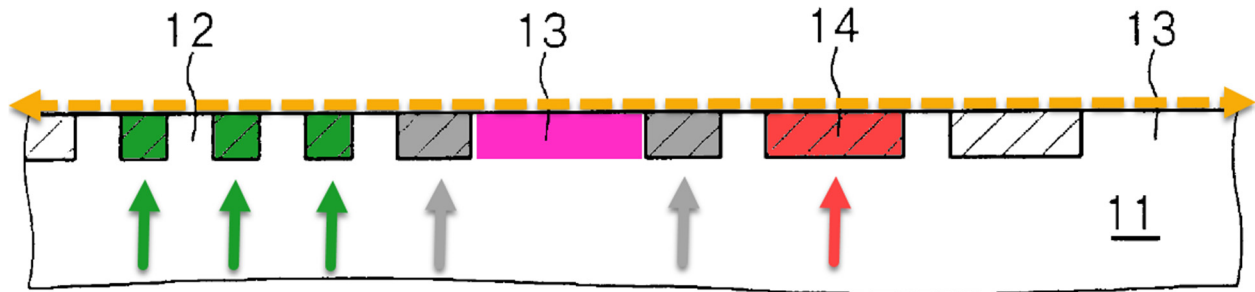
topography. Ex-1005, 18:50-55; 16:36-39 (“Even when there is a great fluctuation in pattern area ratio  $\alpha'$  in the patterned first layer 12, the second layer 14 can be uniformly polished since the dummy pattern 13 is formed”); Ex-1002, ¶78. As a result, the upper surfaces of the conductive lines (green and red) are coplanar with the upper surfaces of the dummy lines (gray).

Thus, Takahashi in combination with Tonishi discloses this claim limitation. Accordingly, Takahashi in combination with Tonishi renders obvious Claim 16.

**3. Claim 17: “The substantially planar semiconductor topography of claim 16, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces”**

Takahashi in combination with Tonishi discloses this claim. Takahashi discloses polishing of a metal layer 14 above a first dielectric layer 11. The metal layer is “**flattened by a [CMP] process** using, for example, the polishing apparatus shown in FIG. 11,” and “the second layer 14 can be **uniformly polished** since the dummy pattern 13 is formed.” Ex-1005, 16:32-39; Ex-1002, ¶80. The result is the planar topography shown in annotated Figure 4D:

Fig. 4D



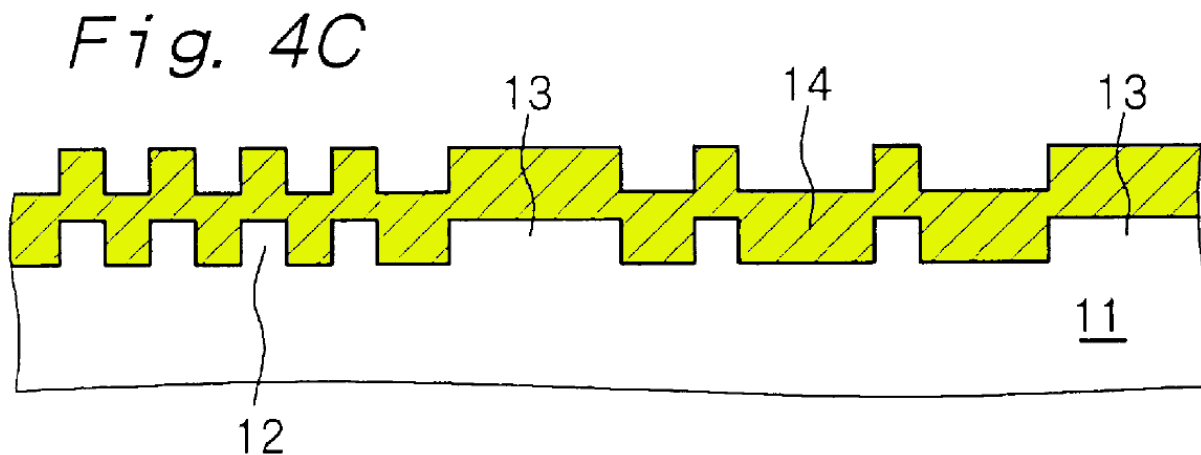
Takahashi discloses the metal interconnects and dummy lines (green, red, and gray) separated by dielectric material 11, such as SiO<sub>2</sub>. Ex-1005, 16:18-21. That includes the dummy pattern 13 (pink) formed from such dielectric material between adjacent pairs of dummy trenches (gray). Ex-1002, ¶81. That dummy pattern constitutes a dielectric protrusion. Because the semiconductor layer has been “**uniformly polished**,” the upper surface of the dummy dielectric protrusion and the adjacent dummy conductor surfaces are coplanar. *Id.* This pattern is repeated numerous times across the semiconductor wafer being processed. Ex-1005, 14:43-44 (“[A] plurality of chips are produced on one wafer with the mask.”); 16:9-17 and Figures 3A-3D (showing a plurality of “dummy patterns”); Figures 4A-4D (showing a plurality of dummy conductors in “a variant of” Figures 3A-3D); Ex-1002, ¶81.

Thus, Takahashi in combination with Tonishi renders obvious Claim 17.

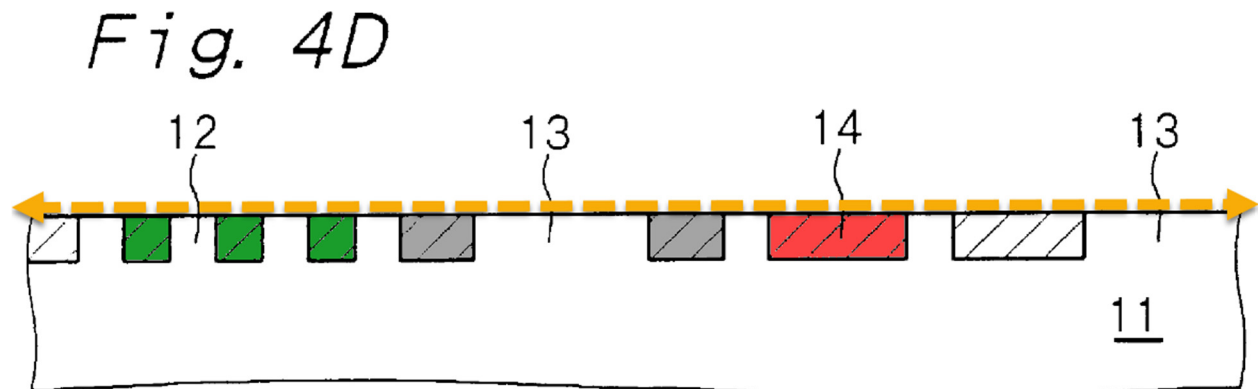
4. **Claim 18: “The substantially planar semiconductor topography of claim 16, wherein said dummy conducts comprise a metal selected from the group consisting of a**

**aluminum, copper, tungsten, molybdenum, tantalum,  
titanium, and alloys thereof**

Takahashi in combination with Tonishi discloses this claim. Takahashi discloses depositing a second “**metal wiring material layer**” 14 over the first dielectric layer 11 by known methods such as CVD, as shown in Figure 4C below to create both the dummy conductors and the conductive lines:



Ex-1005, 16:29-43 and Fig. 4C. Takahashi teaches that the second layer 14 can be a “layer of metal such as an **aluminum alloy, tungsten, copper, or silver.**” *Id.*, 6:47-48. That layer then forms the dummy conductors and conductive lines.

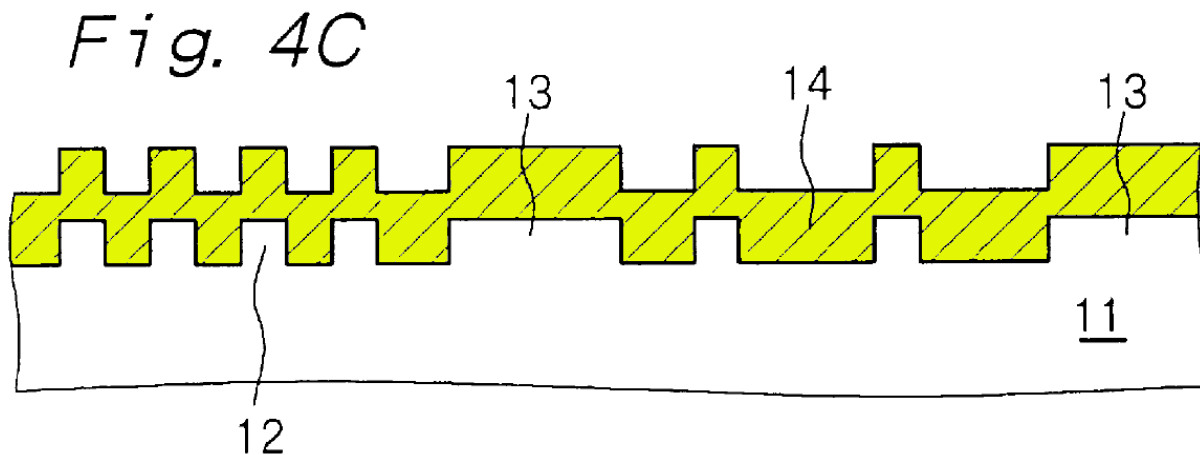


Tonishi also discloses that “[t]he metal wires 2 and 3 and the dummy wire 4 are formed of **aluminum or an aluminum based alloy.**” Ex-1007, ¶16.

Thus, Takahashi in combination with Tonishi renders obvious Claim 18.

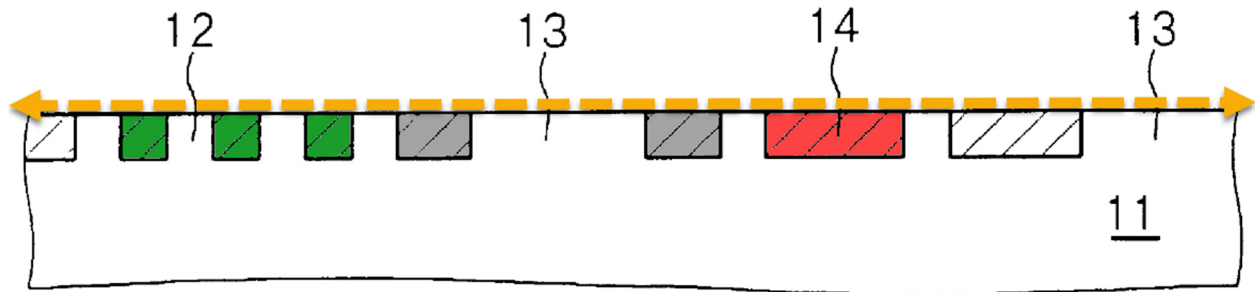
5. **Claim 19: “The substantially planar semiconductor topography of claim 16, wherein said conductive lines comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof”**

Takahashi in combination with Tonishi discloses this claim. Takahashi discloses depositing a second “metal wiring material layer” 14 over the first dielectric layer 11 by known methods such as CVD, as shown in Figure 4C below to create both the dummy conductors and the conductive lines:



Ex-1005, 16:29-43 and Fig. 4C. Takahashi teaches that the second layer 14 can be a “layer of metal such as an **aluminum alloy, tungsten, copper, or silver.**” *Id.*, 6:47-48. That layer then forms the dummy conductors and conductive lines.

Fig. 4D



Tonishi also discloses that “[t]he metal wires 2 and 3 and the dummy wire 4 are formed of **aluminum or an aluminum based alloy.**” Ex-1007, ¶16.

Thus, Takahashi in combination with Tonishi renders obvious Claim 19.

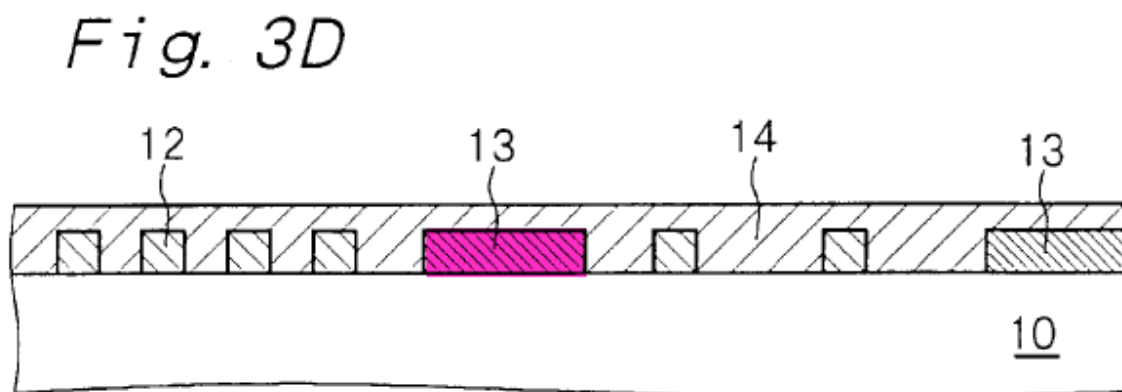
**6. Claim 20: “The substantially planar semiconductor topography of claim 16, wherein lateral dimensions of the laterally spaced dummy trenches are between approximately 1 micron and approximately 5 microns”**

Takahashi in combination with Tonishi discloses this claim. Tonishi discloses the narrower range of 1-5 $\mu$ m as being a favored size for dummy lines. With reference to Figure 1, Tonishi discloses a lower bound where the dummy line is “substantially equal” to the narrow line, with a width of “for example **1 $\mu$ m.**” Ex-1007, ¶16; Ex-1002, ¶89. Alternatively, Tonishi specifically discloses a “predetermined wire-width [of] **5 $\mu$ m,**” for the dummy wires. Ex-1007, ¶13; *see id.* ¶¶11-13 and claims 1-3; Ex-1002, ¶89. Because Tonishi discloses both 1 $\mu$ m and 5 $\mu$ m dummy lines, Tonishi discloses dummy trenches having lateral dimensions between approximately 1-5 $\mu$ m. *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015) (“When a patent claims a range, as in this case, that



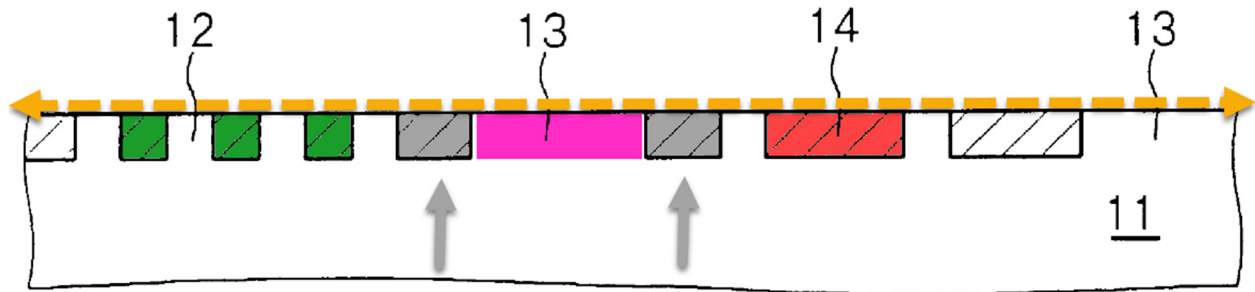
range is anticipated by a prior art reference if the reference discloses a point within the range.”); see MPEP 2144.05; *In re Wertheim*, 541 F.2d 257, 267 (CCPA 1976) (obviousness where claimed ranges “overlap or lie inside ranges disclosed by the prior art”); *In re Woodruff*, 919 F.2d 1575, 1577 (Fed. Cir. 1990) (prior art disclosure of carbon monoxide concentration of “about 1-5%” renders obvious claims reciting concentration of “more than 5%” since “ ‘about 1-5%’ does allow for concentrations slightly above 5%”).

Takahashi also discloses this limitation. Takahashi discloses the use of dummy wires of various sizes, including dummy wires of 5 $\mu$ m. Ex-1002, ¶90. For example, in the subtractive process shown in Figure 3D, the dummy pattern 13 (pink) is shown as a metal dummy wire:



Conversely, in the damascene process shown in Figure 4D, the dummy pattern 13 (pink) is shown as an oxide protrusion 13 set apart by two dummy lines:

*Fig. 4D*



Takahashi teaches that there is “a space, e.g., of **5  $\mu\text{m}$**  between the pattern and the dummy pattern.” Ex-1005, 7:39-40; Ex-1002, ¶91. In the damascene process of Figure 4D, then, the space between the oxide dummy pattern 13 and the oxide pattern 12 is the dummy lines in gray. Ex-1002, ¶91. Takahashi teaches that those dummy lines are 5  $\mu\text{m}$  wide. *Id.* Thus, Takahashi discloses dummy lines of 5  $\mu\text{m}$ , which overlaps with the range cited in Claim 20 and renders obvious the limitation. *Ineos*, 783 F.3d at 869.

Thus, Takahashi in combination with Tonishi renders obvious Claim 20.

**7. Claim 21: “The substantially planar semiconductor topography of claim 16, wherein the lateral dimension of the first trench is greater than approximately 50 microns”**

Tonishi gives representative widths of wide power supply and ground wires of “**approximately 40  $\mu\text{m}$  to 80  $\mu\text{m}$** ” and discloses the example of Figure 1, in which the metal wire is a power supply wire or ground wire. Ex-1007, ¶3, 16; Ex-1002, ¶94. This overlaps with the claimed range of “greater than approximately 50 microns.”

To the extent that the Patentee argues there is a distinction between the range of 40-80 $\mu$ m disclosed in Tonishi and the range of “greater than approximately 50 microns,” recited in Claim 21, there is no evidence that the distinction is “critical” or achieves “unexpected results.” *See In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003). The ’946 Patent acknowledges that “[t]he widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria.” Ex-1001, 4:17-20. The ’946 Patent fails to disclose how the use of a wide trench of less than 50 $\mu$ m would lead to distinct or unexpected results, or otherwise be critical to the claimed invention.

Thus, Takahashi in combination with Tonishi renders obvious Claim 21.

**8. Claim 22: “The substantially planar semiconductor topography of claim 16, wherein the series of the second trenches comprise sub-micron lateral dimensions”**

Tonishi discloses narrow signal lines with “a minimum wire-width of approximately 0.8  $\mu$ m to 1.2  $\mu$ m,” and discloses the example of Figure 1, in which the narrow wire is “for transmitting electrical signals.” Ex-1007, ¶3, 16; Ex-1002, ¶97. As applied to Takahashi, the signal lines would be formed in trenches of the same size using the damascene process. A signal line and corresponding trench under 1 $\mu$ m is sub-micron. Ex-1002, ¶97.

To the extent that the Patentee argues there is a distinction between the range of 0.8-1.2 $\mu$ m disclosed in Tonishi and the range of “sub-micron lateral

dimensions,” recited in Claim 22, there is no evidence that the distinction is “critical” or achieves “unexpected results.” The ’946 Patent acknowledges that “[t]he widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria.” Ex-1001, 4:17-20. The ’946 Patent fails to disclose how the use of a narrow trenches between 1.0-1.2 $\mu$ m or under 0.8 $\mu$ m would lead to distinct or unexpected results, or otherwise be critical to the claimed invention.

Thus, Takahashi and Tonishi disclose or render obvious Claim 22.

## **XII. CONCLUSION**

For the reasons given above, Samsung requests institution of IPR for Claims 16-22 of the ’946 Patent based on each of the grounds specified in this Petition. Ex-1002, ¶100.

Dated: July 13, 2018

By: /s/ Brian M. Berliner  
Brian M. Berliner (Reg. No. 34,549)

**Certification of Word Count**

Pursuant to 37 C.F.R. § 42.24(d), Samsung certifies that this petition includes 8,892 words, as measured by Microsoft Word, plus any words included in figures, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, and word count, and exhibits.

## **CERTIFICATE OF SERVICE**

The undersigned certifies pursuant to 37 C.F.R. § 42.6(e) and § 42.105 that on July 13, 2018, a true and correct copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,849,946** was served via express mail on the Patent Owner at the following correspondence address of record:

DAFFER McDANIEL, LLP  
P.O. Box 164345  
Austin, TX 78716

A courtesy copy was sent to Patent Owner's litigation counsel via electronic mail (INVENSASTX17-670.LWTEAM@lw.com):

Lawrence J. Gotts  
Matthew J. Moore  
Alan M. Billharz  
Latham & Watkins LLP  
555 Eleventh St., N.W., Ste. 1000  
Washington, DC 20004-1304  
Tel.: (202) 637-2200

Joseph H. Lee  
Latham & Watkins LLP  
650 Town Center Dr., 20<sup>th</sup> Fl.  
Costa Mesa, CA 92626  
Tel.: (714) 540-1235

Clement J. Naples  
Latham & Watkins LLP  
885 Third Ave.  
New York, NY 10022  
Tel.: (212) 906-1200

Amit Makker  
Brian W. Lewis  
Latham & Watkins LLP  
505 Montgomery St., Ste. 2000  
San Francisco, CA 94111  
Tel.: (415) 391-0600

Respectfully submitted,

/s/ Brian M. Berliner

Brian M. Berliner (Reg. No. 34,549)  
Email: bberliner@omm.com  
O'Melveny & Myers LLP  
400 South Hope Street, 18th Floor  
Los Angeles, CA 90071  
Telephone: (213) 430-6000  
Attorney for Petitioner