

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS  
AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR LLC.  
Petitioner

v.

INVENSAS CORPORATION  
Patent Owner

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U.S. Patent No. 6,849,946

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**DECLARATION OF DR. MICHAEL THOMAS  
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 6,849,946**

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1. I, Dr. Michael Thomas, declare as follows:

## **I. INTRODUCTION**

2. I have been retained by Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively “Samsung”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”).

3. I have been asked to consider whether certain references teach or suggest the features recited in Claims 16-22 (“the Challenged Claims”) of U.S. Patent No. 6,849,946 (“the ’946 Patent”) (Ex-1001), which I understand is allegedly owned by Invensas Corporation (“Patent Owner”). My opinions and the bases for my opinions are set forth below. In forming my opinions, I have reviewed and relied upon the exhibits attached to the present ’946 IPR Petition.

4. I am being compensated at my ordinary and customary consulting rate of \$650 per hour for my work.

5. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

## **II. QUALIFICATIONS**

6. My academic and professional pursuits are closely related to the subject matter of the ’946 Patent. Based on my education and work experience, I

am well qualified to serve as a technical expert in this matter. A summary of my educational and professional experience is set forth in my curriculum vitae (CV), attached as Exhibit 1004.

7. I have been working in the area of interconnect research, development, and manufacturing for over thirty years. Much of my work has focused on metal, dielectric, and semiconductor materials used in semiconductor products, particularly interconnect technologies. I joined Fairchild Semiconductor Corporation (“Fairchild”) in Palo Alto, California in 1979, shortly before completing my Ph.D. in Materials Science and Engineering at Stanford University. My positions at Fairchild included Engineering Project Manager and Senior Staff Engineer. During my time at Fairchild, I performed extensive research on refractory metal silicides, refractory barrier layers, and performed electromigration studies of aluminum alloys. I also worked closely with industry visitors and university professors and students in our laboratories on yield modeling of interconnect processes and new process tool concepts and also helped layout research activities related to the students’ advanced degree research. I also developed processes and specifications for advanced multilevel interconnect technologies.

8. In 1987, National Semiconductor Corporation (“National Semiconductor”) acquired Fairchild. During my 12 years at National

Semiconductor, my positions included Engineering Project Manager and Senior Member of Research Staff. While at National Semiconductor, I identified new research and development areas related to submicron interconnect technology. I integrated advanced interconnect technologies into commercial product production flows; and I mentored professors and students performing chemical vapor deposition (CVD) of metals at University at Albany, State University of New York. I also participated as an Industrial Advisory Board Member to the Deans of Engineering at San Jose State University and San Francisco State University. My work has helped the semiconductor industry in the promotion and introduction of refractory metal silicides, nitrides and pure metals, and metal alloys as interconnect materials; these materials are presently being used in advanced integrated circuit devices.

9. In the 1990–1999 timeframe, I participated in two National Technology Roadmap Councils (through SEMATECH, a not-for-profit consortium that performs research and development to advance chip manufacturing) as the Co-Chair for Interconnect Technology Working Group. Our task was to provide a 15-year interconnect technology vision for the semiconductor industry. I also was on a panel of top scientists and engineers from the largest U.S. semiconductor companies called the Semiconductor Research Corporation (SRC) under the auspices of the Semiconductor Industry Association (SIA). The SRC helped

provide funding for semiconductor research programs at major universities throughout the United States from a pool of funds supplied by SRC industry members and the U.S. government. My area focused on funding university research for the development of new materials and the processes for future semiconductor device generations. In addition, I participated in site selection committees for the construction of Centers of Excellence for university interconnect programs, on behalf of the SRC. These efforts focused on the future development of new technologies and technologists for the semiconductor industry. In this capacity, I provided research direction and critique to many professors and students at different universities, such as Stanford University, Massachusetts Institute of Technology, and Carnegie Mellon University.

10. In 1999, I became the Chief Technology Officer of Honeywell Electronic Materials Corporation in Sunnyvale, CA. While at Honeywell, I helped construct a 50 million dollar state of the art Materials Technology Center for Interconnect Materials. I also led an 80+ person research team to assemble a facility for the development of new cutting-edge semiconductor interconnect materials and microfabrication techniques and I participated in establishing the first International Interconnect Technology Conference (IITC) Organizing Committee in 1998 to promote the dissemination of interconnect knowledge required for advanced technologies.

11. In 2003, I formed my own consulting business, providing technical expertise to industrial clients in the areas of semiconductor process technology and intellectual property.

12. I am an inventor on over 50 U.S. patents in the areas of semiconductor and microminiaturization technology and have authored over 40 technical publications in the semiconductor field. Additional information on these topics can be found in my CV. Ex-1004.

13. I have been working in thin film deposition and interconnect formation for roughly three decades. My experience as a technologist included depositing a wide range of conductors, barrier films, and insulating films and etching those films. Specifically, in the years prior to becoming an engineering manager, I did my own hands-on work with copper films for integration onto IC devices. I have sputtered, evaporated, and plated copper films. This occurred in the first 10 years of my career from 1978-1988 when I was a staff engineer at Fairchild Research Center in Palo Alto, CA. In the lab, members of my group who were directed by me, performed extensive studies on interconnect systems that involved copper formation and growth issues. I was performing copper interconnect research in the early 1990's through the decade. As I became more senior, I managed a group of engineers with respect to interconnect research and development. Copper work was going on in our labs in parallel with the still



mainstream aluminum technology.

14. I also worked with many professors through the SRC, on an industry wide U.S. university research review panel. I visited many universities for example, at RPI and SUNY, regarding copper studies related to damascene issues along with being my company representative for interconnect issues at Sematech. I have given invited talks on the future of copper at the Schumacher SRC Copper Workshop, where Schumacher was one of the major copper precursor manufacturers for the formation of CVD Cu.

### **III. LEVEL OF ORDINARY SKILL IN THE ART**

15. Based on my review of the '946 Patent specification, claims, file history, and prior art, I believe a person of ordinary skill in the art at the time of the purported invention of the '946 Patent would have had a bachelor-level degree in mechanical engineering, chemical engineering, physics, materials science, electrical engineering, or a related field and 3–5 years of experience or equivalent post-graduate education and training in semiconductor manufacturing.

16. In determining the level of ordinary skill in the art, I was asked to consider, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

17. My opinions concerning the '946 Patent claims and the prior art are from the perspective of a person of ordinary skill in the art ("POSA"), as set forth above.

#### **IV. TECHNOLOGICAL BACKGROUND**

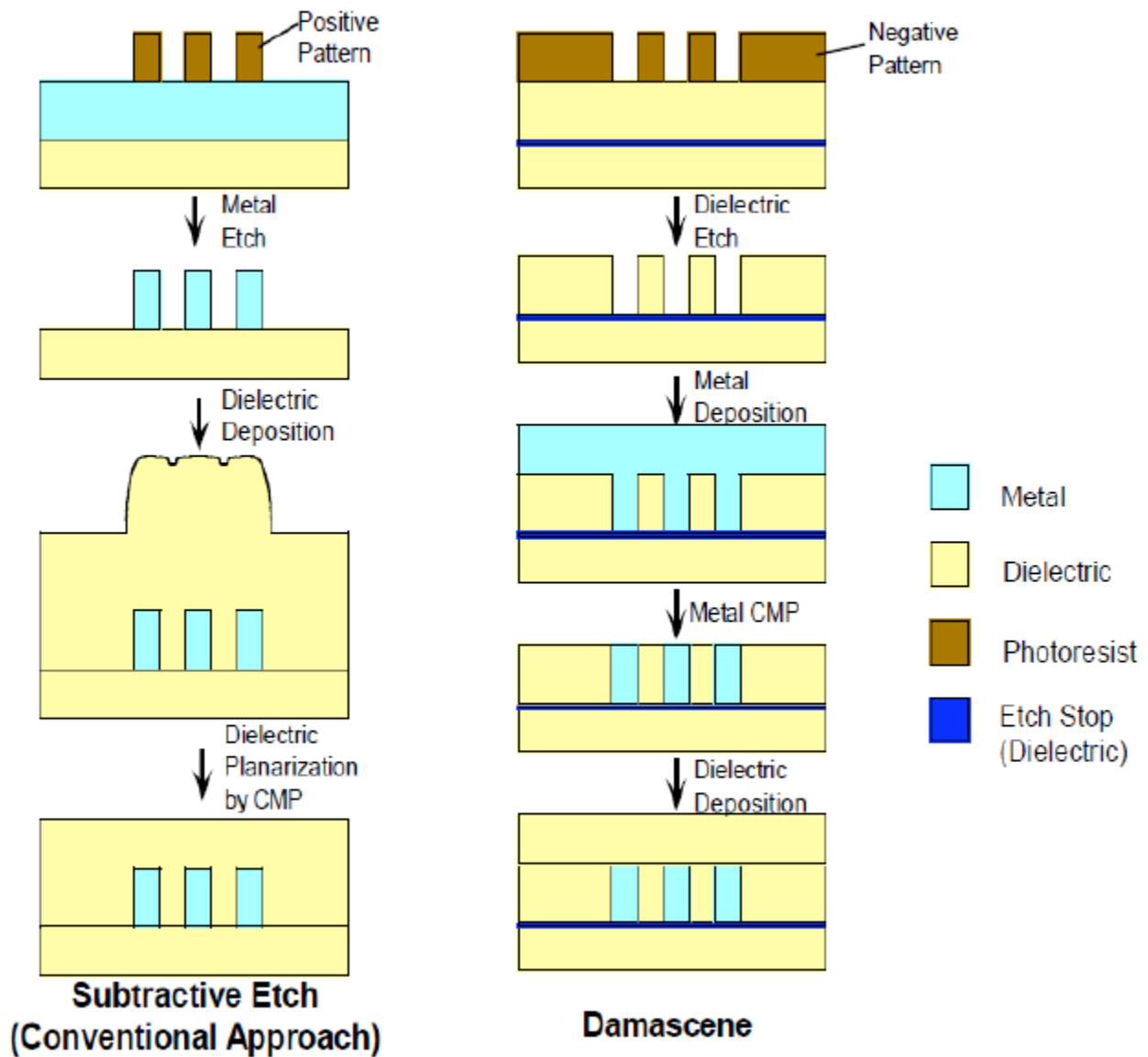
18. The '946 Patent is directed generally to technology for forming interconnects in integrated circuits. Interconnects form electrical connections between the transistors and other components in an integrated circuit that allow for power and signal transfer. Prior to the mid-1990's, integrated circuits were commonly formed from aluminum interconnects using a "subtractive" etch process, in which metal or conductive material is layered and unwanted material is etched away to leave behind conducting interconnects. However, some integrated circuits using non-aluminum conductors were formed using an additive "damascene" process in which trenches are formed and conductive material is added. Polycrystalline silicon (polysilicon) and tungsten are examples of early conductive materials that applied the damascene process. *See, e.g.*, Ex-1011.

19. By the mid-1990s, it became apparent that using aluminum to form interconnects, which had served the industry for well over three decades, could not deliver the performance required for future generations of integrated circuits. Instead, the industry began shifting to copper interconnects, which were expected to have improved performance due to lower resistivity compared to aluminum. In

1997, a National Technology Roadmap for Semiconductors Report stated that without a move from the existing aluminum-based interconnects to a faster copper-based interconnect system, interconnect performance would limit future integrated circuit device performance. Ex-1012, 10. Shortly after, in September 1997, IBM announced the commercial manufacturing implementation of damascene and dual damascene process technology using copper wiring to replace aluminum-based interconnect systems. *See, e.g.*, Ex-1013. After IBM's disclosure, many other companies, such as Motorola and Intel, adopted copper interconnects that remains in use today.

20. Because copper interconnects are more difficult to pattern using subtractive etching techniques, the industry moved to applying the additive damascene process to form interconnects. Figure 1 below shows the difference between the subtractive and damascene processes, where oxide chemical mechanical polishing (CMP) in the subtractive process (aluminum based) is replaced by metal CMP (copper damascene). In the subtractive method on the left, a layer of metal is deposited on dielectric, a pattern is imaged on the metal with a resist mask, and the metal is etched away leaving behind the metal interconnects. In the damascene method on the right, a negative pattern is imaged with a resist mask over the dielectric, and trenches are etched in the dielectric. Metal is then added over the dielectric and into the trenches, and the top layer of metal is

removed using metal CMP, leaving behind the metal interconnects within the trenches. A final thin layer of dielectric is deposited over the planar interface to prepare the next metallization level.



21. Despite certain differences between subtractive etch and damascene technologies, many of the same principles of integrated circuit manufacturing apply to each. In both the subtractive and damascene processes, planarization by

CMP is used to form a flattened, regular semiconductor. By 1997, it was known throughout the semiconductor industry that damascene copper CMP processes were susceptible to flatness variations caused principally by interactions between the design layout density and processing of the interconnect with polishing pads/equipment. Ex-1014, 2:27-42. The over-polishing of copper/oxide structures results in two major problems, referred to as “dishing” and “erosion.” Ex-1009, 15-16. Dishing is the over-polishing of a region caused by a more rapid etching compared to the surrounding material, and it often occurs on bond pads and power buses—wide interconnects used to transmit large currents. Erosion creates an uneven oxide height of the polished oxide compared to the original oxide thickness, which often occurs within an array of metal signal lines. These problems can adversely affect the yield, reliability and performance of an integrated circuit.

22. Solutions to improving planarization were also already known. One commonly known solution to the dishing and erosion problems was the addition of “dummy” structures—e.g., conductive lines that are not electrically connected to the circuit, but serve to promote a more even polishing of the integrated circuit as a whole. Ex-1014–1018. By 1998, the use of dummy structures to improve planarization of interconnect layers was already known.

**V. THE '946 Patent**

**A. The Patent Specification**

23. The '946 Patent, entitled "Planarized Semiconductor Interconnect Topography and Method for Polishing a Metal Layer to Form Interconnect," relates to integrated circuit manufacturing. The '946 Patent describes the generation of a "substantially planarized interconnect topography and method for making spaced interconnect by forming a plurality of dummy features in a dielectric between a relatively wide interconnect structure and a series of relatively narrow interconnect structures." Ex-1001, 1:13-18. According to the '946 Patent, "CMP is commonly used to form a planarized level of an integrated circuit containing interconnect laterally spaced from each other." *Id.*, 2:10-13. The '946 Patent states that "planarization may become quite difficult in a region where there is a relatively large distance between a series of relatively narrow interconnect, or if there is a relatively wide interconnect such as that found in, for example, a bond pad." *Id.*, 2:33-37. The '946 Patent describes the dishing and erosion problems known in the art and discussed above. *Id.*, 2:37-3:44. Annotated Figure 4 shows oxide erosion in the narrow metal interconnects (green) and dishing in the wide interconnect (red).

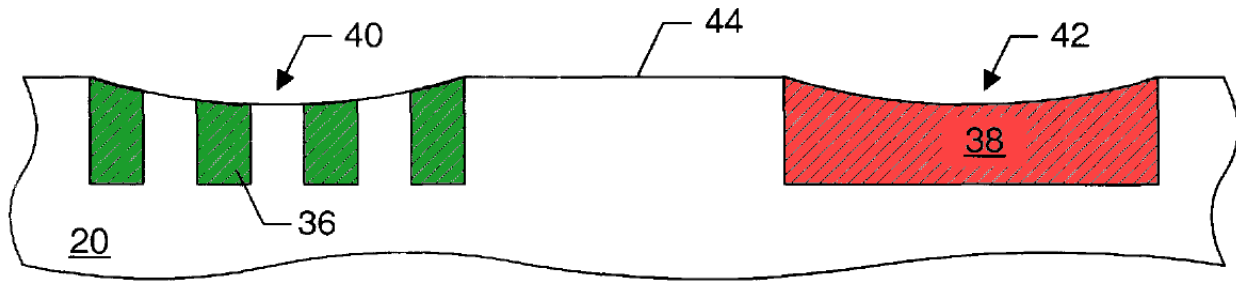


FIG. 4

24. The '946 Patent's proposed solution for the dishing and erosion problems is the addition of dummy features, so that the areas with the dummy features are planarized at the same rate as the narrow and wide interconnects. Figure 5 depicts the addition of dummy trenches 56 (gray arrows) between existing narrow trenches 52 (green arrows) and wide trench 54 (red arrow):

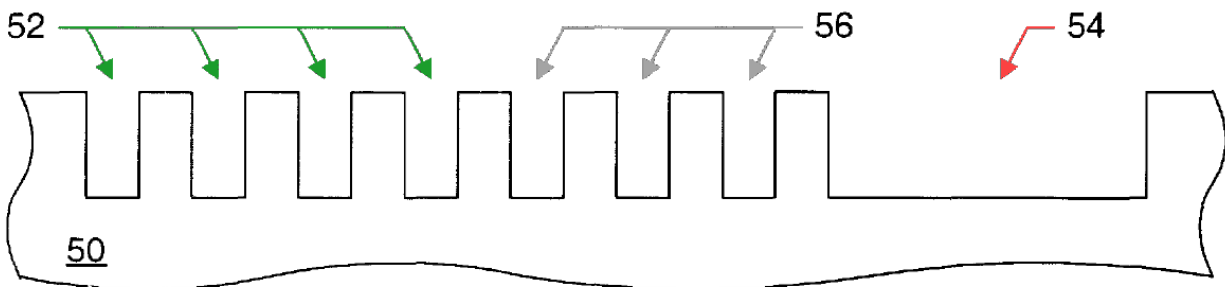


FIG. 5

25. Figure 6 depicts the addition of conductive material 58 (yellow) in accordance with the damascene process:

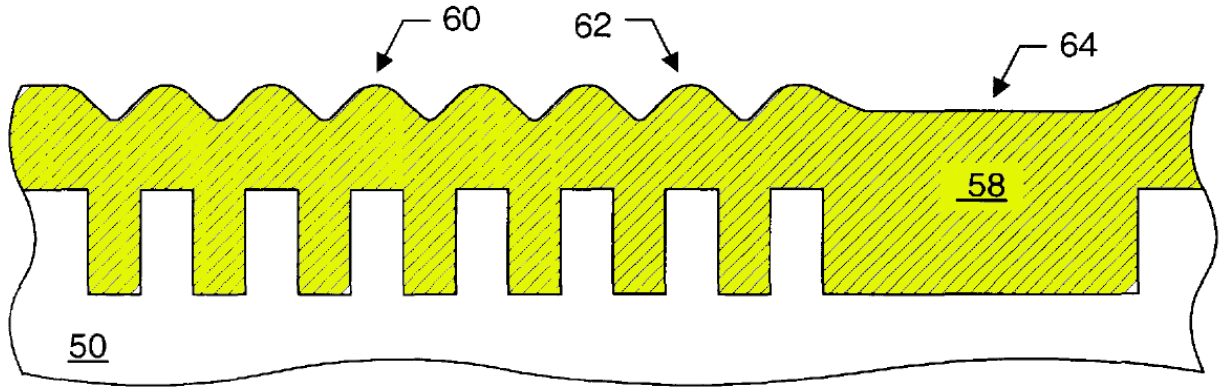


FIG. 6

26. CMP then occurs, and Figure 7 depicts the resulting planarization of the narrow lines 66 (green), the wide interconnect 72 (red), and the added dummy features 68 (gray):

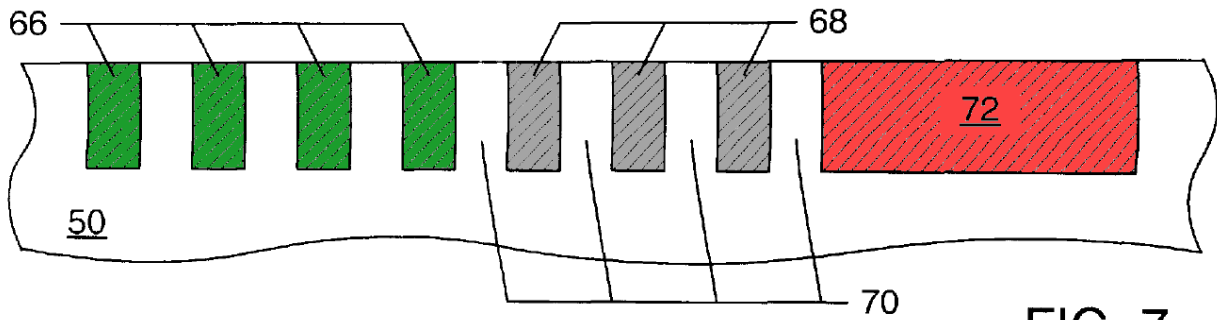


FIG. 7

## B. Prosecution History

The application that eventually issued as the '946 Patent, U.S. Application No. 09/779,123, is a division of U.S. Application No. 09/143,723, which issued as U.S. Patent No. 6,232,231. On July 3, 2002, the Examiner issued a non-final rejection under §103 based on U.S. Patent No. 6,093,631 to Jaso et al. ("Jaso") in view of the admitted prior art disclosed in Figures 1-4 and the related discussion.



Ex-1004, 161-166. After rejection, the Applicant and Examiner exchanged numerous amendments and rejections, with the Examiner issuing a total of four rejections based primarily on Jaso. *Id.*, 161-166, 183-190, 226-232, and 249-255. On April 28, 2004, the Examiner objected to the claims for indefiniteness for using the terms “relatively wide trench” and “relatively narrow trenches,” but no longer rejected the claims based on Jaso. *Id.*, 275-279. Applicant amended the claims to their current form, and on September 30, 2004, the claims were allowed because the Examiner found that Jaso did not “teach nor suggest that the *second* trenches is relatively narrow compared to the first trench” as required by Claims 16-22 at issue in this Petition. *Id.*, 301-303.

## **VI. SUMMARY OF OPINIONS**

27. In preparing this declaration, I have reviewed at least the documents labeled Exhibits 1001-1019 and other materials referred to here. In addition to these materials, I have relied on my education, experience, and my knowledge of practices and principles in the relevant field. My opinions have also been guided by my appreciation of how one of ordinary skill in the art would have understood the claims and specification of the '946 Patent around the time of the alleged invention, which I have been asked to assume is the earliest claimed priority date of August 31, 1998.

28. Based on my experience and expertise, it is my opinion that certain

references teach or suggest all the features recited in Claims 16-22 of the '946

Patent, as explained in detail below. Specifically, it is my opinion that:

- Ground 1: Claims 16-22 are obvious under 35 U.S.C. § 103 over U.S.

Patent No. 5,948,573 ("Takahashi") in view of Japanese Patent

Application 4-262535 ("Tonishi");

## **VII. THE PRIOR ART TEACHES OR SUGGESTS EVERY STEP AND FEATURE OF THE CHALLENGED CLAIMS OF THE '946 PATENT**

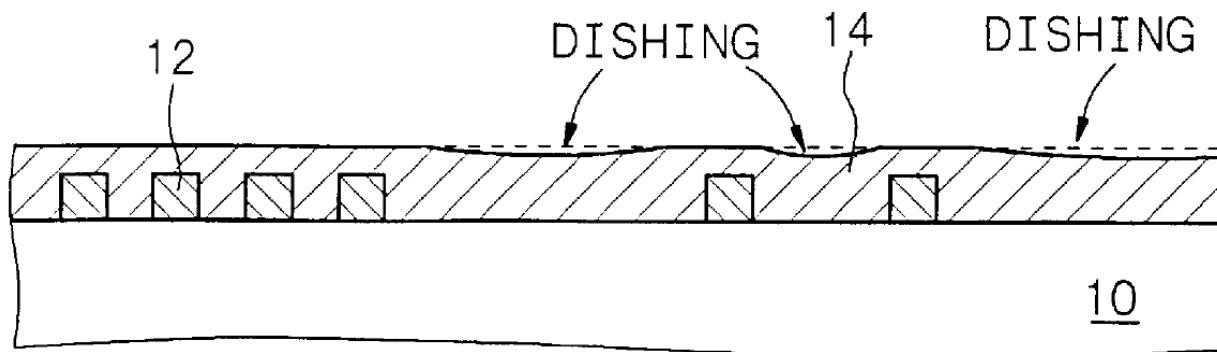
### **A. Overview Of The Prior Art References**

#### **1. U.S. Patent No. 5,948,573 ("Takahashi") (Ex-1005)**

29. Takahashi was filed on February 19, 1998. Ex-1005, Cover.

30. Takahashi is directed to the same object as the '946 Patent of improving planarization and reduce dishing and erosion through the use of dummy features. Takahashi describes how the problem of dishing can occur, using as an example prior art implementing subtractive etch technology as depicted in Figure 17D below.

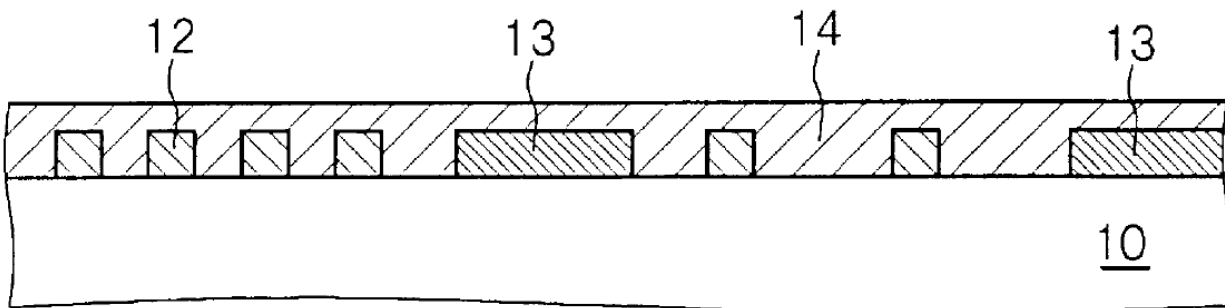
*Fig. 17D*



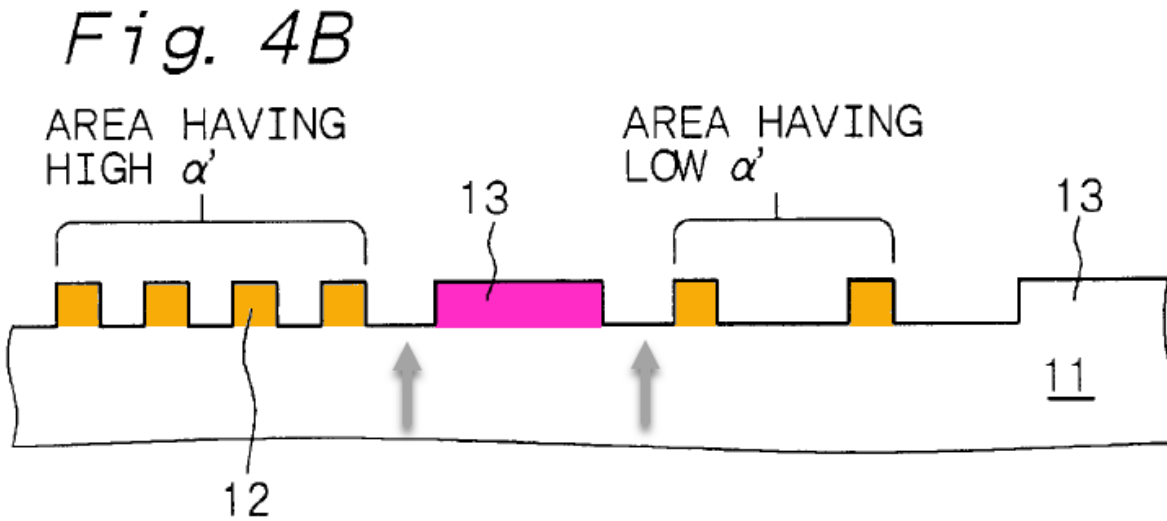
*Id.*, Figure 17D, 1:56-2:8.

31. Similar to the '946 Patent, Takahashi discloses placing dummy trenches between a wide interconnect and a series of narrow interconnects. Figures 3A-D depict the use of dummy interconnects for a subtractive etch, while Figures 4A-D depict the use of dummy interconnects for a damascene process. In Figure 3D, the dummy conductor is described as a “dummy pattern” 13, which is formed from the same material as the wiring. *Id.*, 15:56-62, 6:35-36.

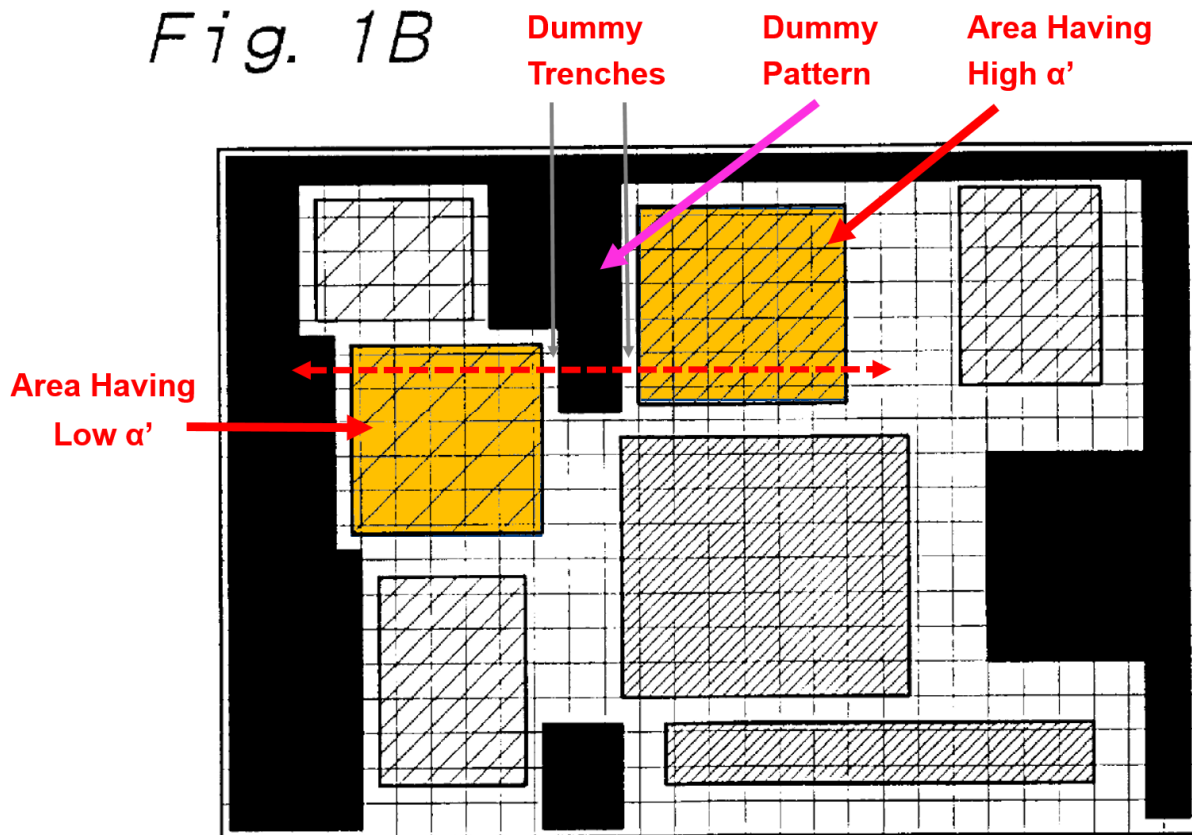
*Fig. 3D*



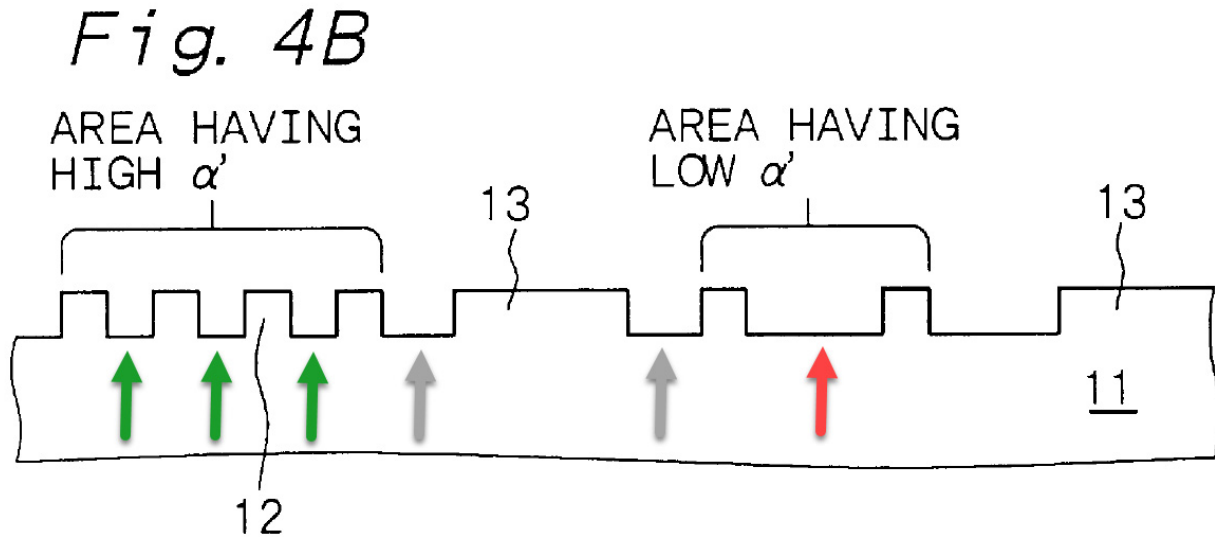
32. Figures 4A-4D depict the inverse of Figure 3, as it applies the concept of dummy conductors to the additive damascene process instead of the subtractive etch process. There, the dummy pattern is formed of oxide instead of metal. *Id.*, 16:18-28. The dummy pattern (pink) is separated from the pattern (orange) on each side of the dummy pattern by a space that is, for example, 5  $\mu\text{m}$  in width. *Id.*, 7:35-40. These two spaces (marked by gray arrows) are dummy trenches.



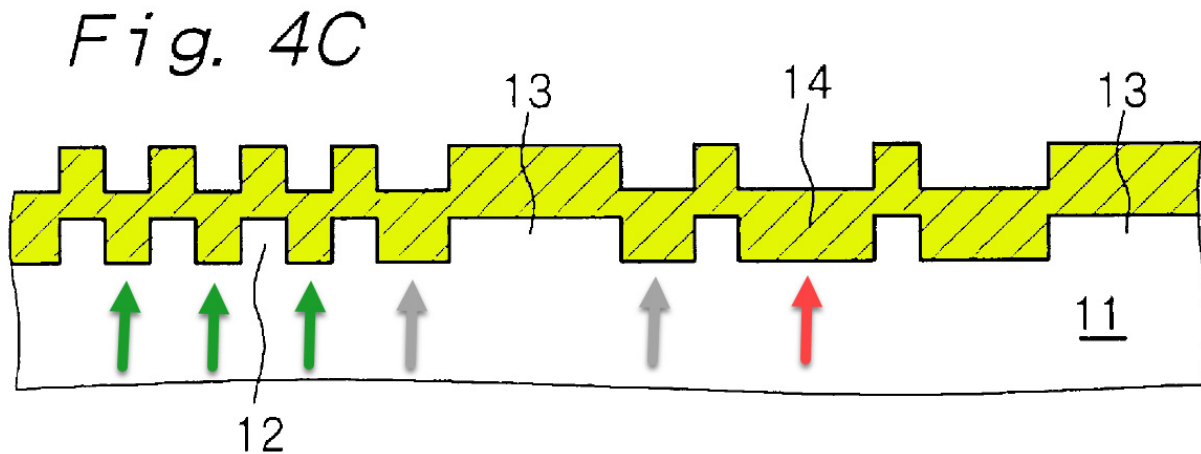
33. The dummy trenches are also depicted in Figure 1B's plan view as spaces between the circuit blocks (orange) and the dummy pattern (black).



34. The dummy trenches (gray) are located between a first interconnect trench (red) and a plurality of second interconnect trenches (green):

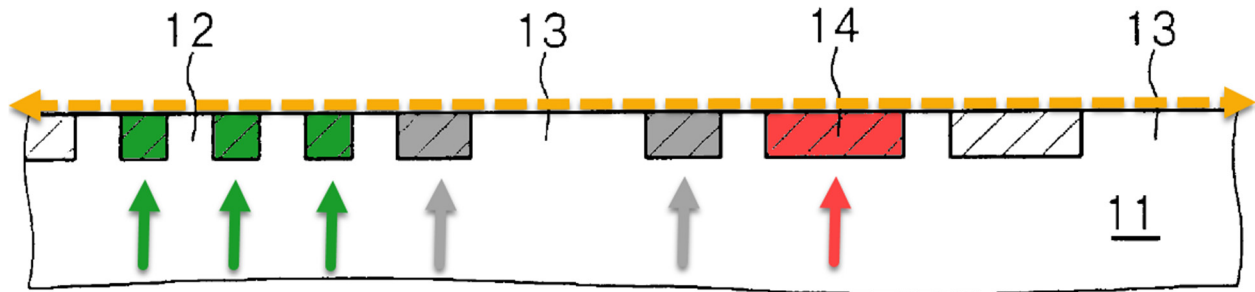


*Id.*, Figure 4B, 16:18-28. Takahashi depicts adding a metal layer 14 in accordance with the damascene process:



*Id.*, Fig. 4C, 16:29-43. CMP then occurs, and Figure 4D depicts the resulting planarization of the surface due to the addition of dummy features (gray).

*Fig. 4D*



35. As the Board noted in *Broadcom*, although Figures 4A-4D depict placing dummy trenches (gray) between a wide trench (red) and narrow trenches (green), Takahashi does not expressly state that the images in Figures 4A-4D are drawn to scale.

**2. Japanese Patent Application 4-262535 (“Tonishi”) (Ex-1007)<sup>1</sup>**

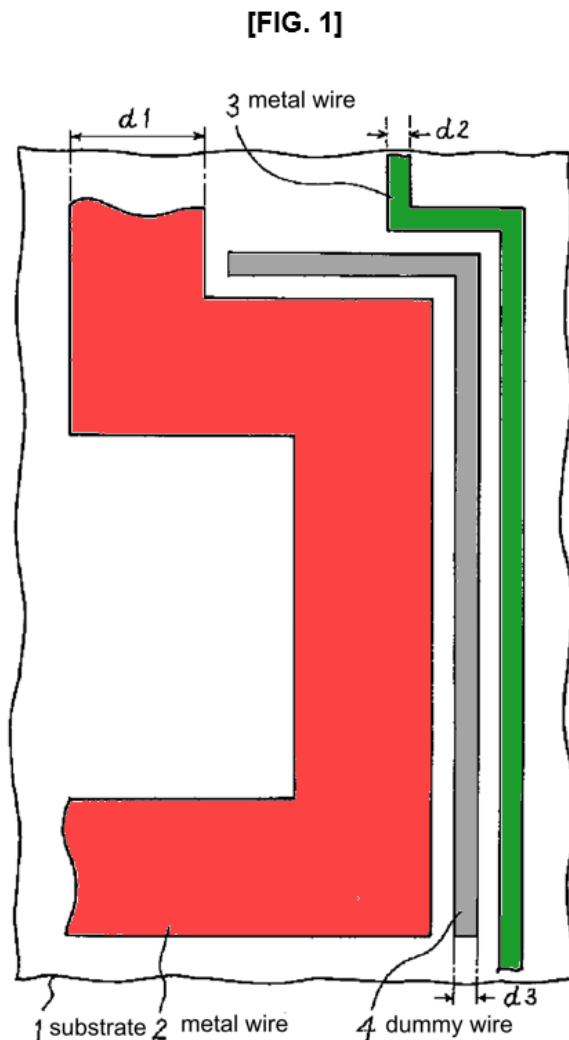
36. Tonishi was published on September 17, 1992. Ex-1007, Cover. Tonishi was not considered during the prosecution of the '946 Patent or during the *Broadcom* IPR.

37. Like the '946 Patent and Takahashi, Tonishi discloses the use of dummy conductors in an integrated circuit. Specifically, Tonishi discloses using a

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<sup>1</sup> Throughout this Declaration, I refer to the certified translation of Tonishi. A copy of Tonishi in the original Japanese is attached as Ex. 1006. A declaration by the translator Martin Cross is included also attached as Ex. 1011 certifying that Ex. 1007 is a true and correct translation of Ex. 1006.

dummy wire to prevent lateral hillocks, which are metallic protrusion defects that can occur and ultimately grow to a sufficient size to cause short circuits with adjacent wires. *Id.*, ¶6. Figure 1 shows one embodiment, in which a dummy wire (gray) is located between a wide wire (red) and a narrow wire (green). *Id.*, Fig. 1, ¶¶16-17.



38. Tonishi further discloses width dimensions for the wide and narrow wires. Specifically, Tonishi explains that in a DRAM or semiconductor integrated

circuit device, “the widths of these metal wires are, for example, a minimum wire-width of approximately 0.8  $\mu\text{m}$  to 1.2  $\mu\text{m}$  for metal wires that transmit electrical signals, and is approximately 40  $\mu\text{m}$  to 80  $\mu\text{m}$  for the thickest metal wires, such as power supply wires and ground wires.” *Id.*, ¶3. Tonishi also discloses the relative size and position of the dummy wire: “a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.” *Id.*, ¶11. The dummy wire may be set at a “predetermined wire-width [of] 5  $\mu\text{m}$ .” *Id.*, ¶12.

39. Tonishi explains what would have been well known to a POSA—that wire widths are selected to be wide enough to carry current and yet narrow enough to fit highly integrated circuits in a small area. Specifically, Tonishi states that “[t]he wire-widths of the metal wires in this conventional semiconductor integrated circuit device are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life; for example, a wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires, than for other metal wires.” *Id.*, ¶4. “Meanwhile, with increasing levels of integration in semiconductor integrated circuit devices, it is necessary to arrange metal wires having wire-widths sufficient to satisfy the conditions described above in a limited area.” *Id.*, ¶¶4-5. Tonishi



therefore discloses the well-known benefits of using wide, current-carrying lines and narrow interconnect lines.

**B. Ground 1: Takahashi And Tonishi Render Obvious Challenged Claims 16-22**

40. As discussed below, Takahashi expressly discloses each limitation of Claims 16-22 of the '946 Patent, except for intermediate-sized dummy conductors, a wide interconnect and a plurality of narrow interconnects. A POSA would have found it obvious to apply conventional, prior art arrangements of interconnect and dummy line sizes as disclosed in multiple secondary references, such as Tonishi, in which wide interconnects supply power for the integrated circuit, narrow interconnects are used to connect transistors and carry signals, and intermediate-sized dummy lines. Thus, Takahashi in view of Tonishi renders each of Claims 16-22 invalid as obvious. *Id.*

**1. Motivation To Combine Takahashi with Tonishi**

41. A POSA would have been motivated to utilize the wire width dimensions of Tonishi with the teachings of Takahashi, thereby achieving the purported invention of the challenged claims. There are several reasons why a POSA would be motivated to apply Tonishi's teachings relating to wire width dimensions to Takahashi:

- First, the uses of wide interconnects, narrow signal lines, and intermediate-sized dummy lines are driven by commonly known

design considerations. For example, a POSA would have known that a wide wire is necessary to conduct power to allow large current flow and electromigration life. A POSA would have also known to minimize the width of signal connection wires between transistors to maximize the density of the integrated circuit. A POSA would have further known that dummy lines can be of intermediate size for ease of manufacture. Tonishi expressly teaches such uses and reasons. Thus, a POSA would have known to use the dimensions disclosed by Tonishi in Takahashi because such a combination involves only the use of a known technique to improve a similar device with no unexpected results.

- Second, Takahashi and Tonishi each discloses using dummy lines to achieve the overall goal of increasing yields at high integrated circuit densities through improved planarization and prevention of short circuits. Given that they are in a common field of endeavor and disclose similar approaches involving the use of dummy lines, a POSA would have found it obvious to combine the teachings of Takahashi and Tonishi.

**a) A POSA Would Have Been Motivated To Apply  
Tonishi's Interconnect Sizes to Takahashi**

42. Tonishi discloses reasons and benefits for selecting various wire-

widths in integrated circuits that are generally applicable to all integrated circuit designs, including the design disclosed in Takahashi.

43. Specifically, Tonishi teaches that different wire widths are used in an integrated circuit to transmit signals, provide ground, route power and provide other functions (i.e., resistors, fuses and capacitors, etc.). Ex-1007, ¶¶1-5. In order to achieve high circuit density, the finest interconnect wires—which were, for example, approximately 0.8-1.2 $\mu$ m—are used to transmit signals between the transistors. *Id.*, ¶3. Wide wires, typically 40-80 $\mu$ m, were used to serve as power source wires to drive a block, or large blocks of a device, and as the ground wires used for the power return paths. *Id.* For local power distribution and application specific designs, intermediate sized wires between 5-20 $\mu$ m, were employed. *Id.* Tonishi discloses the reasons behind its selection of wire widths. For example, Tonishi teaches that “a wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires” in order to reduce noise, provide a stable power source, and improve reliability by minimizing the effects of electromigration. *Id.*, ¶4. Tonishi also teaches that using narrow wires to conduct signals allows for “increas[ed] levels of integration” by packing a larger number of circuit components in the same chip area. *Id.*, ¶5. A POSA would have understood that these design considerations, and the benefits associated with using narrow and wide wires, are generally applicable to any

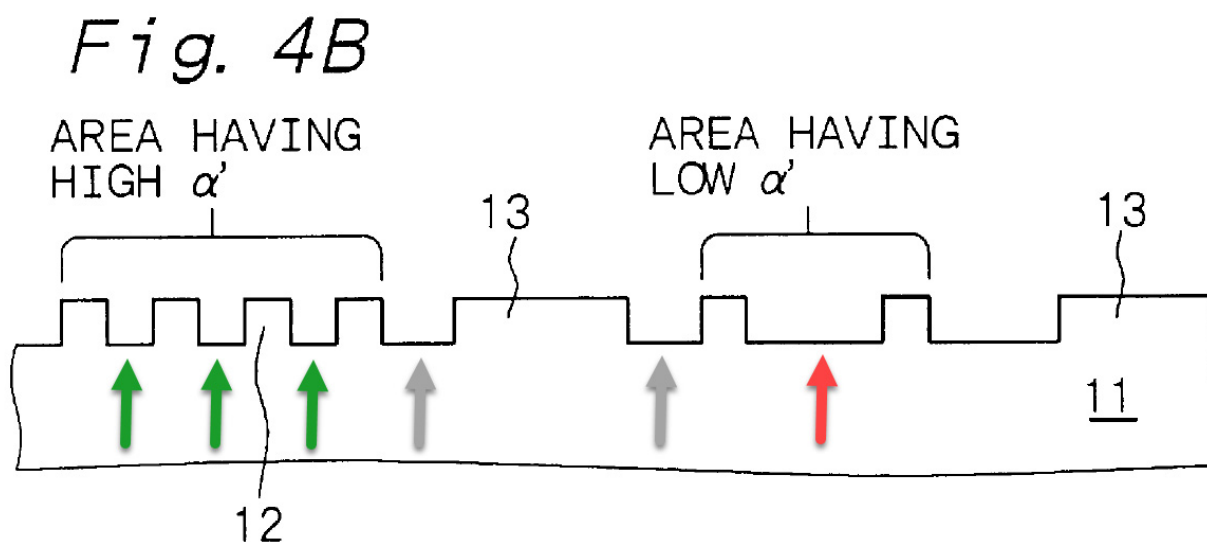
integrated circuit design.

44. The sizes described in Tonishi are driven by design considerations well-known to a POSA—wire widths are selected to be wide enough to carry current and yet narrow enough to fit highly integrated circuits in a small area. Even as transistor and interconnect sizes scaled to be smaller in the late 1990s, a POSA would have recognized that Tonishi’s teachings relating to the relative sizes of power and signals interconnects are applicable to any design. Thus, a POSA would have been motivated by the benefits taught by Tonishi—such as noise reduction, stable power source, and improved reliability—to select relatively wide wires to transmit power/ground. Similarly, a POSA would have been motivated by the benefits taught by Tonishi—such as increased circuit density—to select relatively narrow wires to transmit data signals. Accordingly, a POSA would have been motivated by these benefits to apply Tonishi’s wire width selection to Takahashi.

45. Moreover, Tonishi discloses dummy wires with a preferred “predetermined wire-width [of] 5  $\mu\text{m}$ ”—which is wider than the signal wires but narrower than the power wires. *Id.*, ¶¶3, 12. Such sizes are more practical for dummy wires due to the ease of manufacture compared to the very narrow or very wide interconnects. A POSA would have understood and employed interconnects of these various sizes in their circuits and therefore applied the dimensions

Declaration of Dr. Michael Thomas in Support of Petition for *Inter Partes* Review  
Patent No. 6,849,946  
disclosed by Tonishi to the semiconductor device of Takahashi.

46. The fact that Takahashi suggests an example of the relative widths that are explicitly described in Tonishi along with dummy conductors of  $5\mu\text{m}$  further motivates the combination of the references. Although Takahashi is silent on whether its figures are drawn to scale, its figures must be viewed based on the knowledge of a POSA, as reflected by Tonishi. Here, Figure 4B of Takahashi depicts the arrangement of trenches in a circuit, including a first trench (red), a set of second trenches (green), and a plurality of dummy trenches (gray).



Ex-1005, Figure 4B, 16:18-28. Figure 4B depicts narrower trenches (green arrows) in the region described as having a high pattern area ratio  $\alpha'$ , and wider trenches (red arrow) in the region described as having a low pattern area ratio  $\alpha'$ . *Id.*, 16:18-28. To the extent a POSA would not have understood this width difference from Takahashi alone, Tonishi expressly describes that an integrated

circuit typically has wide interconnects, which may be power lines and ground lines for transmitting large amounts of current, and narrow interconnects, which are signal lines for electrically connecting circuit components. Ex-1007, ¶4. A POSA would have, therefore, found it obvious to apply the conventionally-sized wiring dimensions disclosed in Tonishi to Takahashi. Such a combination involves only the use of a known technique (as disclosed in Tonishi) to improve a similar device (as disclosed in Takahashi) with no unexpected results. *Id.*

**b) A POSA Would Have Combined The Complementary Disclosures of Dummy Lines In Takahashi and Tonishi to Improve Yield**

47. A POSA would have further been motivated to combine Takahashi with Tonishi because both references aim to improve manufacturing yield of semiconductors through the use of dummy features. A POSA would have known that production yield differences of a few percent can make or break the economic viability of a semiconductor production line. *See* Ex-1019, 1:15-18. Two of the greatest drivers of integrated device manufacturability are yield and density. To achieve high density and yield, a semiconductor manufacturer needs to squeeze every advantage out of the lithographic process to print minimum sized features without line and space variations. *See* Ex-1007, ¶5.

48. Because of the density requirements for these devices, planarization of the interconnect levels was very important towards achieving the highest device

yields possible. Poor planarization across the die negatively impacts printed lithographic interconnect feature fidelity, formed by either the subtractive or damascene processes. Takahashi teaches that metal dishing can occur during poor flattening. Ex-1005, Fig. 17D, 1:56-2:8. By employing dummy metal interconnect features into a layout between small and larger metal features, Takahashi teaches one how to achieve improved interconnect level planarization with less dishing (i.e., *id.*, Fig 17D and 2:6-8) for either subtractive or damascene processes (*id.*, 6:29-56, 15:38-16:6, 16:7-44). The resulting increase in interconnect process margins would improve metal feature fidelity, reliability and yield (*id.* 27:15-19) not only within an interconnect level but between levels.

49. Tonishi is also directed towards improving device yields. It discusses the importance of having a reliable interconnect wiring system that has good electromigration resistance, and is especially resistant to the effects of lateral “hillocks,” which consist of extruded metal that protrudes from the periphery of especially large wires during subsequent heat treatment processes and can ultimately contact and short-circuit other adjacent metal wires. Ex-1007, ¶¶4, 10. Tonishi proposes using an interposed dummy metal wire that lies between the unused real estate of a small wire and larger wire to avoid lateral hillock shorting without hindering increases in integration, thereby also increasing yields. *Id.*, ¶¶10-12, Claims 1-2.

50. Thus, a POSA would have been motivated to combine the disclosure of dummy lines in Takahashi to promote greater interconnect level “flatness” with the dummy lines in Tonishi to act as a barrier to shorting, resulting in an attractive solution to enhance the yield of an integrated circuit. Takahashi teaches that flattening treatments (or planarization) using dummy metal trenches are viable for interconnect processes that use either subtractive or damascene processes. *See also* Section VII.A.1, *infra* (discussing how Takahashi is applicable to both subtractive or damascene processes). Tonishi teaches interposing intermediate-sized dummy lines between wide and narrow lines to block lateral hillocks. The dummy lines help flatten the surface and act as a barrier to shorting, thereby generating high yield interconnect for multiple “flattened” interconnect levels.

51. Takahashi does not explicitly disclose the dimensions of the trenches, except for the 5 $\mu$ m dummy trench. Tonishi teaches the similar use of small, dummy and wide interconnect features to improve device yield but also explicitly identifies a range of interconnect width dimensions. Tonishi gives representative widths of wide power supply and ground wires (40-80 $\mu$ m), narrow signal wires (0.8-1.2 $\mu$ m) and intermediate wires (5-20 $\mu$ m), with 5 $\mu$ m being a representative intermediate wire width. *Id.*, ¶¶1-5, 11-13. A POSA reading both Takahashi and Tonishi would have been motivated to concomitantly use dummy conductors to improve device yield by improving the planarity of one or more interconnect



layers, and suppressing lateral hillocks in the wiring by employing dummy conductors having preferred sizes. The improved cross-sectional control from combining Takahashi and Tonishi would yield greater electromigration resistance and reliability.

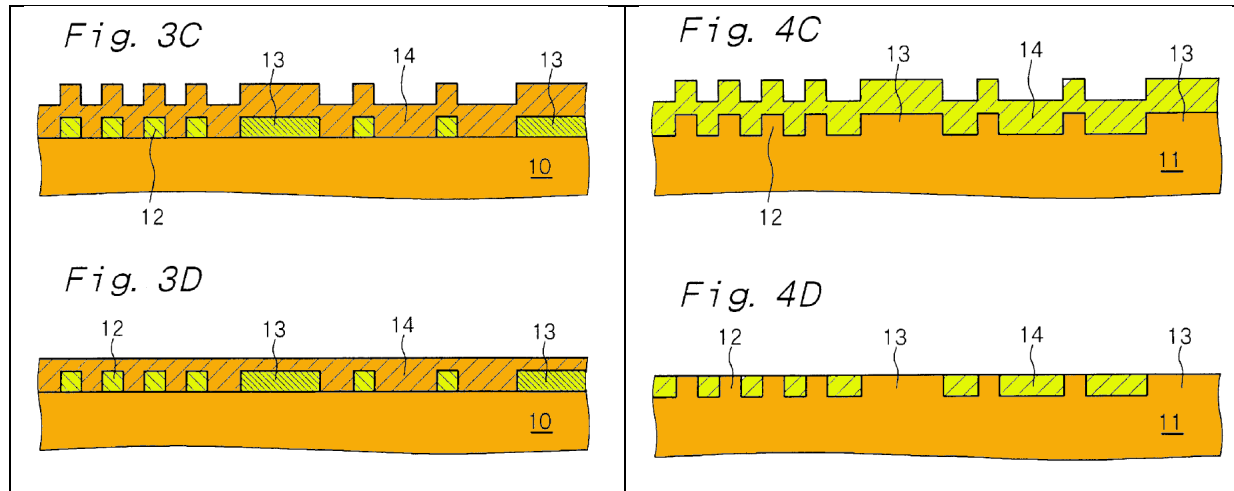
52. Given that Takahashi and Tonishi are directed to the same field of integrated circuit interconnects, disclose the same objective of increasing yield in high density integrated circuits, and disclose the same approach of using dummy lines to achieve these objectives, and given that these objectives and techniques are shared by the '946 Patent itself, a POSA would have been motivated to apply the teachings of Tonishi to Takahashi to interpose dummy lines of around 5 $\mu$ m between narrow signal lines (e.g., 0.8-1.2 $\mu$ m) and wide power lines (e.g., 40-80 $\mu$ m). Because such a combination would be nothing more than applying known techniques to similar systems, a POSA would have expected the combination to yield a predictable result and be successful.

**c) Takahashi Demonstrates That The Dimensions Disclosed In Tonishi Are Applicable To Both Damascene and Subtractive Processes**

53. Although Tonishi discloses a subtractive process as opposed the damascene process, a POSA would have understood that Tonishi's teachings relating to wire dimensions are applicable to both subtractive and damascene processes. The design considerations relating to the selection of wide wires for

power/ground connections and the selection of narrow wires for signal connections are generally applicable to any circuit design regardless of the manufacturing technique used to fabricate its interconnects.

54. The general applicability of Tonishi's teachings is further confirmed by Takahashi. Takahashi explains that its teachings relating to dummy lines are applicable to both subtractive and damascene processes. Takahashi teaches that the principles of planarization apply regardless of whether it is the dielectric being planarized in the subtractive method or, instead, it is the metal being planarized in the damascene method. *See* Ex-1005, 6:29-56 (listing numerous exemplary combinations including both dielectric and metal top layers). Takahashi further supports this teaching in explaining that the metal CMP process shown in Figures 4A-D ("Example 3") of the specification is a variant of the dielectric CMP process shown in Figures 3A-D ("Example 2"). *Id.*, 15:38-16:6. Figure 3 thus implements a polycrystalline silicon doped "conductor" and oxide CMP to flatten the overlying oxide, while Figure 4 implements an underlying oxide trench pattern with metal CMP to flatten the overlying metal. The following diagram compares the processes, showing oxide in orange and metal in yellow:



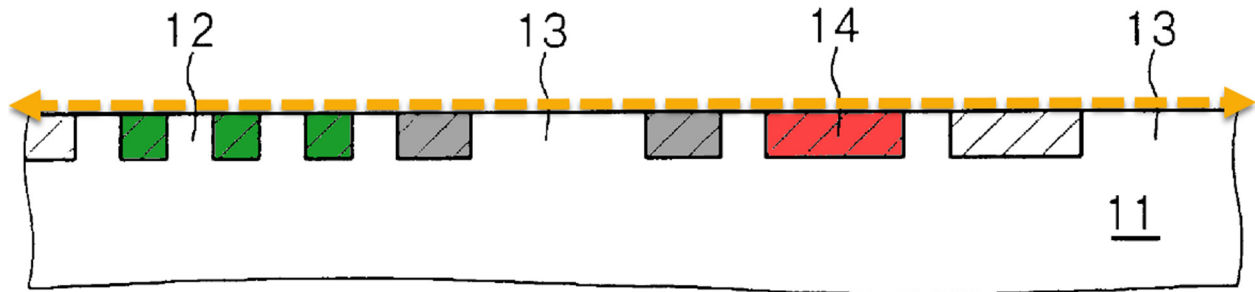
55. Similarly, a POSA would have understood that design considerations relating to the selection of wire widths disclosed by Tonishi, like the use of dummy structures, is not dependent on the manufacturing technique. Tonishi's teachings are thus fully applicable to Takahashi, which teaches planarization in both a subtractive and damascene process.

## 2. Claim 16

### a) [1 pre]: “[a] substantially planar semiconductor topography”

56. Takahashi discloses using a flattening process, such as chemical-mechanical polishing, to generate a planar semiconductor topography. Ex-1005, 16:18-43. The semiconductor is “**uniformly polished**” due to the use of a dummy pattern 13 (*id.*, 16:29-43), resulting in the planar semiconductor topography shown in Figure 4D:

*Fig. 4D*



The surface of Figure 4D is “substantially planar” as contrasted with the prior art disclosure of “dishing.” *See, e.g., id.*, Figure 17, 2:2-8.

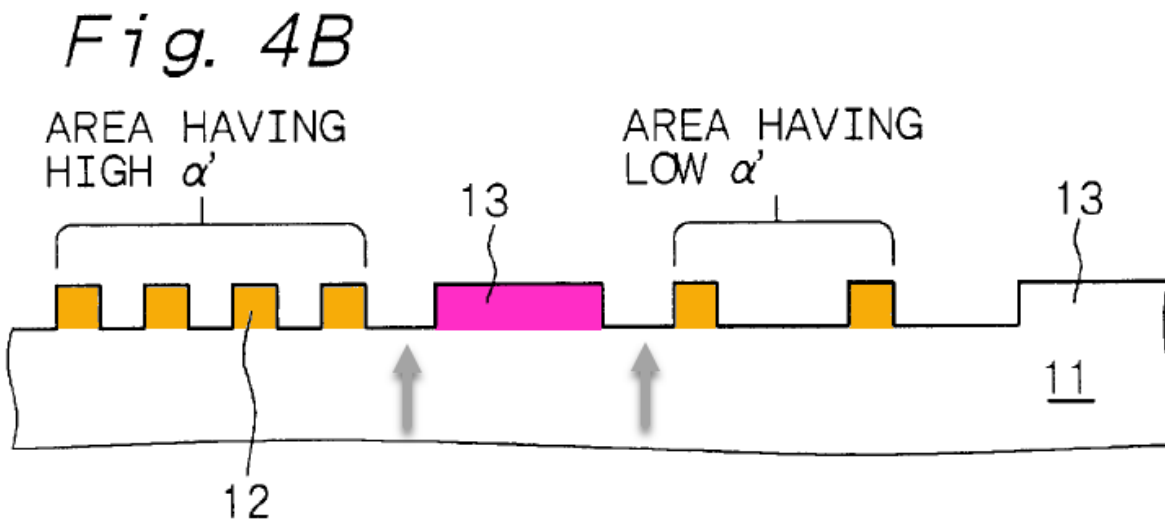
57. Thus, to the extent the preamble is limiting, Takahashi discloses the limitations recited by the preamble.

- b) [16 a]: “a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches, wherein each of the second trenches is relatively narrow compared to the first trench and wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches”

58. Takahashi in combination with Tonishi discloses a plurality of intermediate-sized dummy trenches between a series of narrow trenches and a wide trench. Ex-1005, 16:21-25.

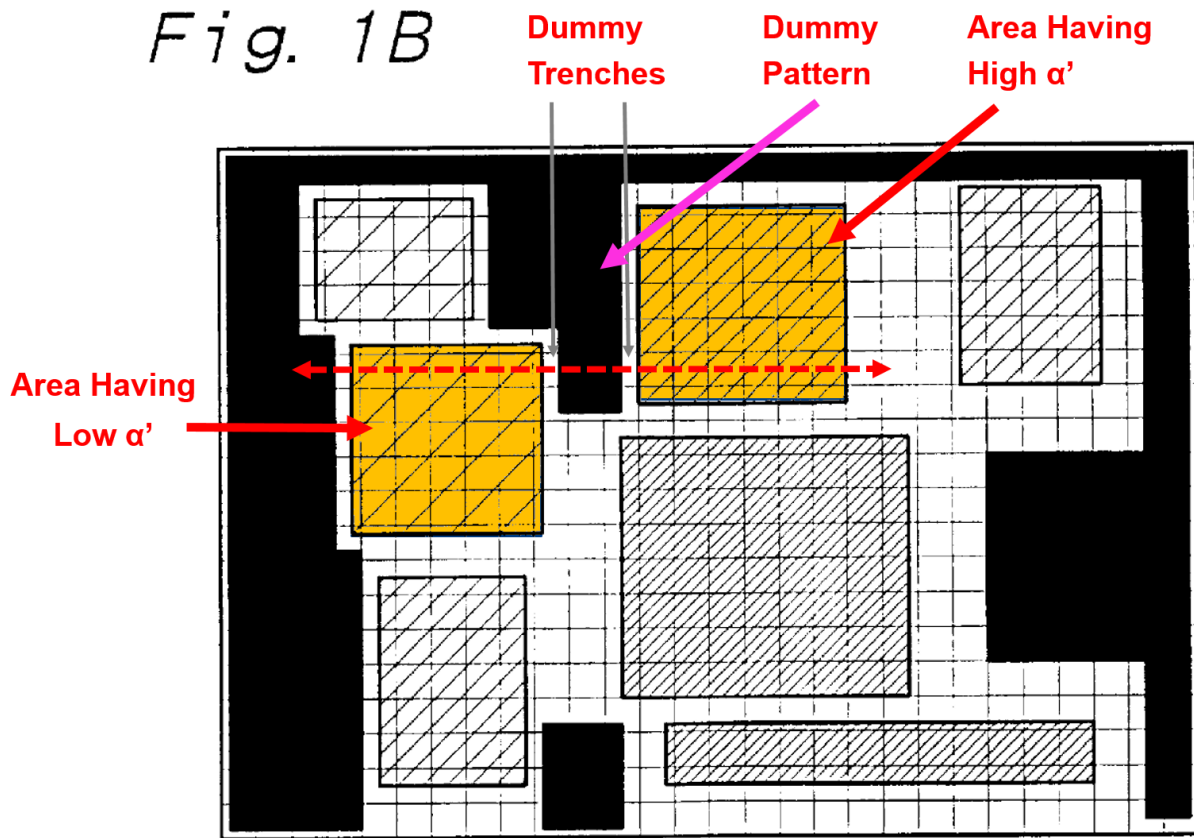
59. Takahashi discloses etching a plurality of laterally spaced dummy trenches (gray arrows) as part of “a **dummy pattern 13** []” formed concurrently in the first layer 11” between a first trench (red arrow) and a series of second trenches

(green arrows) as illustrated below in annotated Figure 4B. *Id.*, 16:18-28. The dummy pattern (pink region) is formed of oxide, “**does not overlap a pattern and has a space, e.g., of 5  $\mu\text{m}$  between the pattern and the dummy pattern.**” *Id.*, 7:35-40. As shown in Figure 4B below, there are two spaces (marked by gray arrows) between the dummy pattern (pink) and the pattern (orange).



60. The two spaces (gray arrows) are both “dummy trenches” because they do not connect to or form part of an integrated circuit. Rather, only the two non-dummy “pattern” areas (orange) in Figure 4B, bounded by brackets and labeled the “area having high  $\alpha'$ ” and “area having low  $\alpha'$ ,” form part of an integrated circuit. *Id.*, Fig. 4B (identifying the pattern as the raised oxide), 7:10-26 (comparing and contrasting “mask pattern” and “dummy pattern”). By contrast, all trenches and raised oxide portions outside of these brackets and labels in Figure 4B are not part of any integrated circuit and are therefore dummy trenches and dummy patterns, respectively.

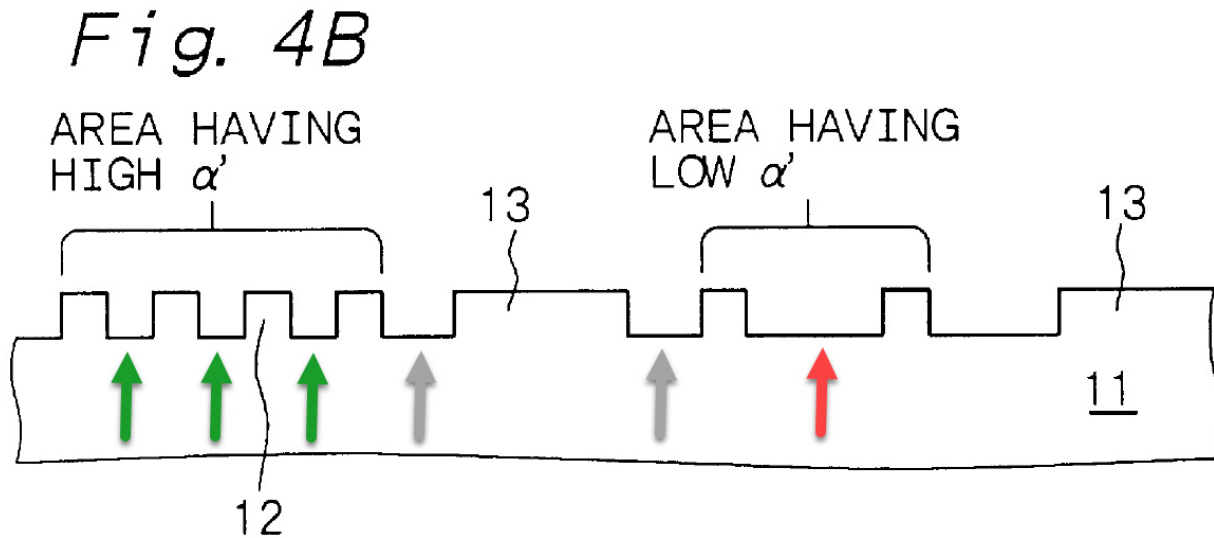
61. This understanding of Figure 4B's boundaries between the integrated circuit patterns (orange) and dummy pattern (pink) and trenches (gray arrows), is confirmed by Figure 1B below, which shows a plan view of these features. In Figure 1B, "rectangular regions surrounded by thick lines show the circuit blocks, and the circuit blocks having higher pattern area ratios are indicated by hatching more densely." *Id.*, 15:13-16. In addition, "the dummy patterns are blackened." *Id.*, 15:21-22. A cross-section taken of a segment of Figure 1B (dashed red line) corresponds to Figures 4B-4D. Between the dummy pattern (black) and the circuit blocks (orange) are spaces (gray arrows) that, in a damascene process, constitute trenches between the dummy pattern and the circuit blocks. The circuit block area having high  $\alpha'$  with dense hatching is on the right, and the circuit block area having low  $\alpha'$  with sparse hatching is on the left. Further, a space of 5 $\mu$ m is present between the dummy pattern and the circuit blocks. *Id.*, 7:39-40.



62. Thus, in Figures 1B and 4B-D, the two spaces located between the patterns or circuit blocks (orange) and dummy pattern 13 (pink or black) are trenches that are not part of any integrated circuit and are therefore dummy trenches.

63. The pair of dummy trenches are located between a first trench (red arrow) and a series of second trenches (green arrows) as illustrated below in annotated 4B. *Id.*, 16:18-28. Figure 4B depicts narrow trenches (green arrows) in the region described as having a high pattern area ratio  $\alpha'$ , wide trenches (red arrow) in the region described as having a low pattern area ratio  $\alpha'$ , and

intermediate-sized trenches (gray arrow) in between. *Id.*, 16:18-28.



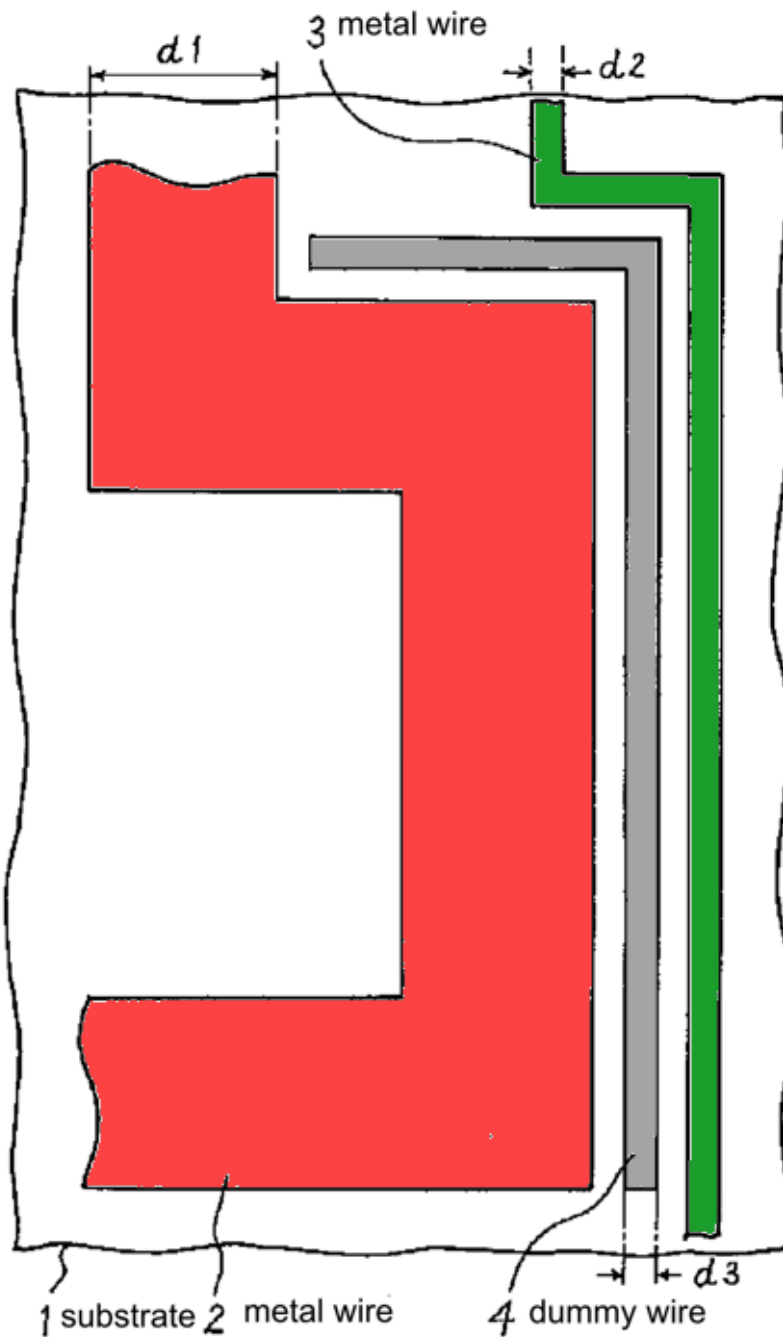
64. Takahashi does not expressly disclose the lateral dimensions of its first, second, and dummy trenches. As discussed in Section VII.A.1, Takahashi suggests an example in which trenches in the low pattern area ratio  $\alpha'$  region (red) have a wider width and trenches in the high pattern area ratio  $\alpha'$  region (green) have a narrower width. A POSA would have found the lateral dimension limitations of Claim 1 obvious from Takahashi in light of Tonishi, which expressly discloses the dimensions of a typical set of interconnects meeting the limitations. It would have been obvious for a POSA to combine with Takahashi for the reasons discussed in Section VII.B.1.

65. Tonishi discloses a configuration in which “[a] dummy wire 4 is provided between a first metal wire having a wide [wire-width] and a second metal wire 3 having a narrow wire-width.” Ex-1007, Abstract. With respect to



the wide and narrow wires, Tonishi teaches that their widths are conventionally selected to meet minimal current flow needs—with wider widths to allow for large current flow and electromigration life, and narrower widths to allow more features to be integrated into the same space. *Id.*, ¶¶4-5. Tonishi thus explains that “[t]he wire-widths of the metal wires in this conventional semiconductor integrated circuit are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life. . . . [T]he minimum wire-width of each of the metal wires is defined according to the individual application.” *Id.*, ¶4. Tonishi specifies conventional sizes of such features is “**for example, a minimum wire-width of approximately 0.8 μm to 1.2 μm for metal wires that transmit electrical signals, and is approximately 40 μm to 80 μm for the thickest metal wires.**” *Id.*, ¶3. In describing Figure 1, Tonishi contrasts a wide wire—*e.g.*, a power supply wire or a ground wire—of 40 μm (red) from a narrow electrical signal wire of 1 μm (green). Disposed between these wires is a dummy wire (gray).

[FIG. 1]



*Id.*, Fig. 1, ¶16.

66. A POSA would have understood that Tonishi's teachings relating to the use of wide power wires and narrow signal wires—with the signal wires being

used to achieve higher density and the power wires being wider to carry greater current—are conventional in the art and applicable to all circuit designs, including the Takahashi device. Moreover, a POSA would have recognized that the benefits disclosed by Tonishi for its selection of relative wire widths (as explained above in Section VII.B.1) are applicable to Takahashi. Applying the teachings of Tonishi to Takahashi, a POSA would have understood that the trenches used to form these interconnects would consist of a wide trench and a series of narrow trenches, with dummy wires to both improve planarity and prevent lateral hillocks. The reasons to combine are further explained above in Section VII.B.1.

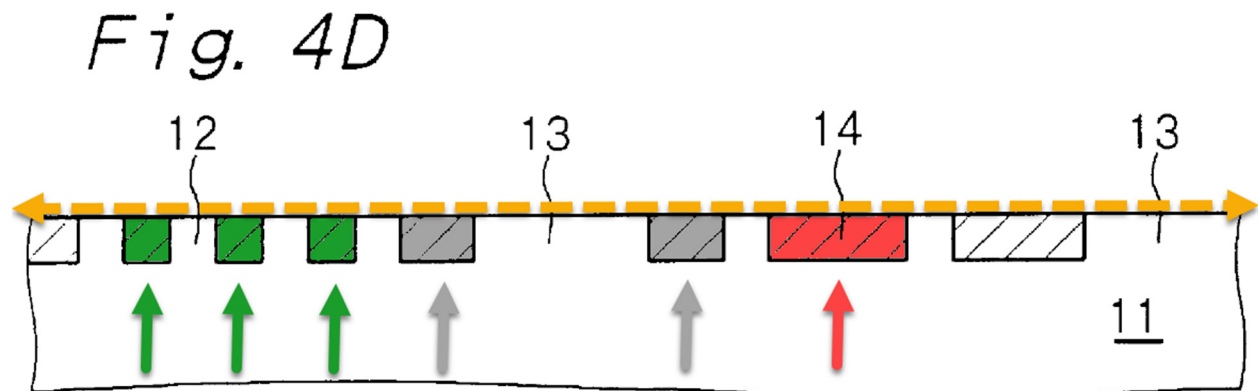
67. With respect to the dummy wire, although the specific dummy wire (gray) embodied by Figure 1 is described in some passages of Tonishi as being “substantially equal to” the narrow metal line (green), *id.*, ¶16, other passages disclose more generally a first wire “wider than a predetermined wire-width,” a second wire “narrower than a predetermined wire-width,” and **“a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width.”** *Id.*, ¶13, Claim 1. Tonishi thus discloses a dummy conductor of intermediate size located between a narrow conductor and wide conductor.

68. Thus, Takahashi in combination with Tonishi discloses this claim limitation.

c) [ 16 b]: “dummy conductors in said laterally spaced dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and” (16[b])

69. Takahashi in combination with Tonishi discloses this limitation.

Takahashi discloses that once the conductive material is deposited, the second layer 14 is polished, i.e., “flattened by a CMP process using, for example, the polishing apparatus shown in FIG. 11,” resulting in the planar topography shown in annotated Figure 4D below.

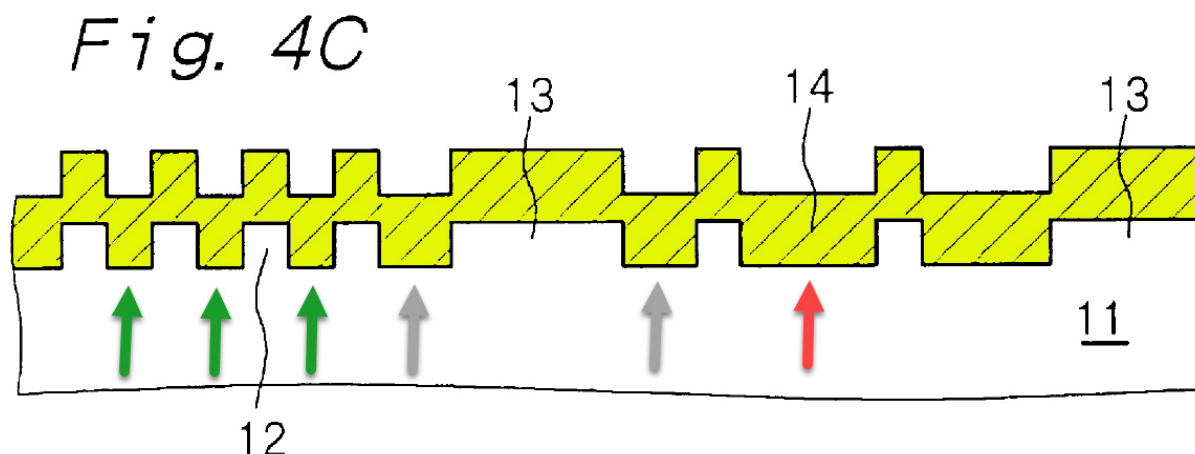


Ex-1005, 16:34-36 and Fig. 4D. Polishing and flattening the second layer 14 until the patterned first layer 12 is exposed results in conductive material in the trenches—dummy (gray), first (red) and second (green) trenches. *Id.* (“As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first later 11 can be effectively prevented, or the excessive polishing of the second layer 14 can also be effectively prevented”). The conductive material exclusively in the dummy trenches (red arrows) form the dummy conductors (red boxes) and the conductive

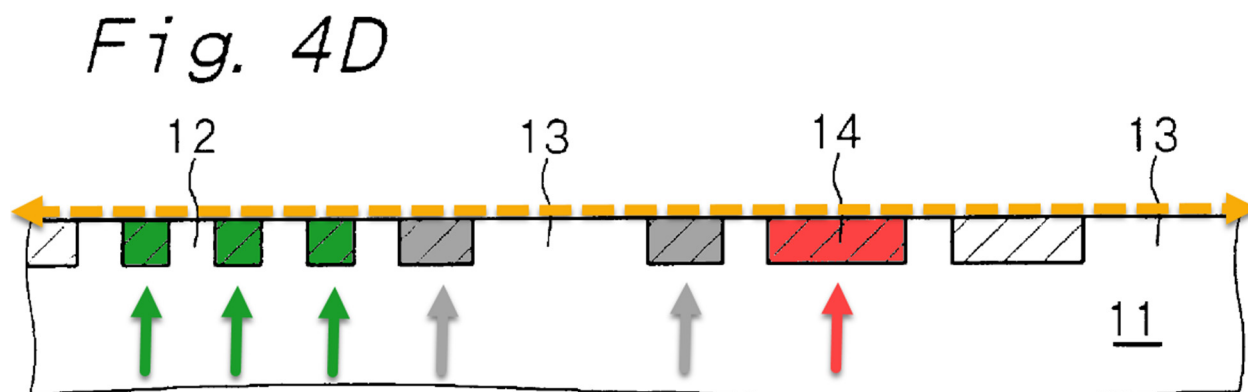
material exclusively in the first trench (red arrows) and second trenches (green arrows) form the interconnects (red and green boxes).

70. Takahashi's dummy conductors are electrically separate from electrically conductive features below said dummy conductors. The material in Figure 4D is "deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub>." *Id.*, 16:20-21. A POSA would understand that in an integrated circuit, each of these layers would comprise additional conductive features such as transistors, inductors, and additional metal lines, and therefore these electrically conductive features are under the dummy conductors in Figure 4D. Takahashi explicitly directs that the "dummy pattern" **"means a pattern which does not constitute any circuit of an integrated circuit."** *Id.*, 7:25-26. Takahashi further explains that **"a dummy pattern [] does not overlap a pattern and has a space, e.g., of 5 μm between the pattern and dummy pattern."** *Id.*, 7:38-40. As discussed in limitation 1[a], the space between the circuit and the dummy pattern constitutes a dummy trench.

71. That trench, which "does not overlap a pattern" that forms part of the circuit is filled with conducting material. *Id.*, Fig. 4C, 16:29-34.



72. The metal is then flattened leaving behind conductors that are not part of the circuit pattern—i.e. dummy conductors that are electrically separate from the interconnects and other conducting features. *Id.*, Fig. 4D, 16:34-36.



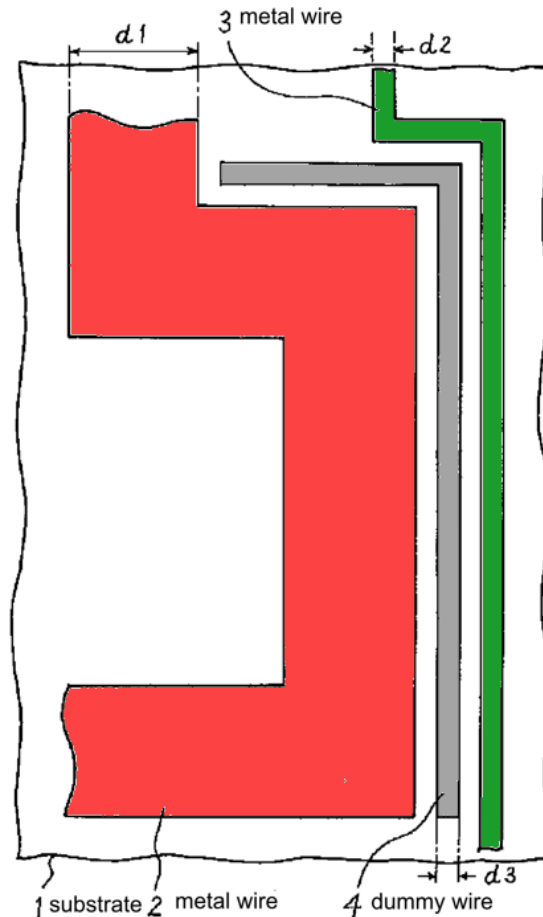
73. Takahashi further discloses additional conducting features below these electrically separate dummy conductors. The conductive material in Figure 4D is formed in a “first layer 11” “deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub>.” *Id.*, 16:20-21. Takahashi also discloses that Figure 4D’s “Example 3” embodiment is part of a “method of manufacturing an **integrated circuit**,” where “for example, a buried (embedded) wiring can be

formed” and this “wiring” refers to the thin wiring in region 12 (green) and wide wiring 14 (red). *Id.*, 16:13-17, 16:29-36. Takahashi further discloses an “Example 6” embodiment that, like “Example 3,” is a variant of the same “first aspect of the present invention” and for Example 6, Takahashi clarifies that “the underlayer is composed of a plurality of layers (N layers).” *Id.*, 18:56-58. I understand that teachings of two related embodiments in prior art patent could be considered together. A POSA would understand that in this “integrated circuit,” each of these layers would comprise additional conductive features such as transistors, inductors, and additional metal lines, and therefore these electrically conductive features are under the dummy conductors in Figure 4D. The dummy conductors are electrically separate from electrically conductive integrated circuit features below them. In particular, the dummy conductors are electrically separate from constituent conductive features of “an integrated circuit” on a “substrate 21 composed of, for example, a silicon semiconductor substrate.” *Id.*, 16:46-65.

74. Tonishi also discloses the use of dummy connectors that are electrically separate from other electrical features. Tonishi discloses variations on the use of dummy wires. In one embodiment, as shown in Figure 1, the dummy wires are electrically separate from electrically conductive features. Ex-1007, Figure 1, ¶16 (“a dummy wire 4 that . . . is formed between the first metal wire 2 and the second metal wire 3, **electrically isolated from the first and second**

metal wires 2 and 3.”).

[FIG. 1]



75. A DRAM semiconductor integrated circuit as disclosed in Tonishi would consist of multiple layers of interconnects beneath the dummy line that are likewise electrically separate from the dummy line. The reasons to combine Takahashi and Tonishi are explained above in Section VII.B.1.

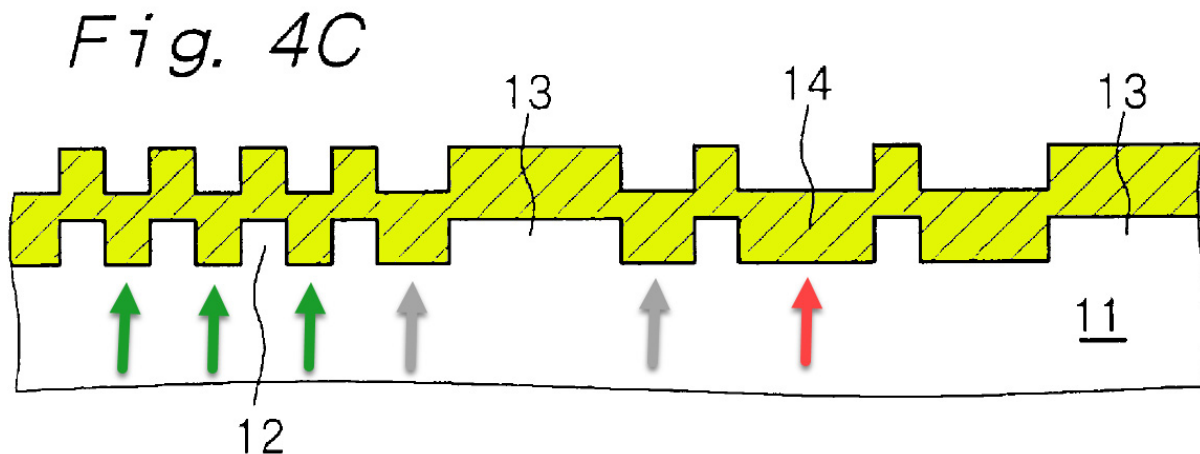
76. Thus, Takahashi in combination with Tonishi discloses this claim limitation.



- d) [16 c]: “conductive lines in said series of second trenches and said first trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces”

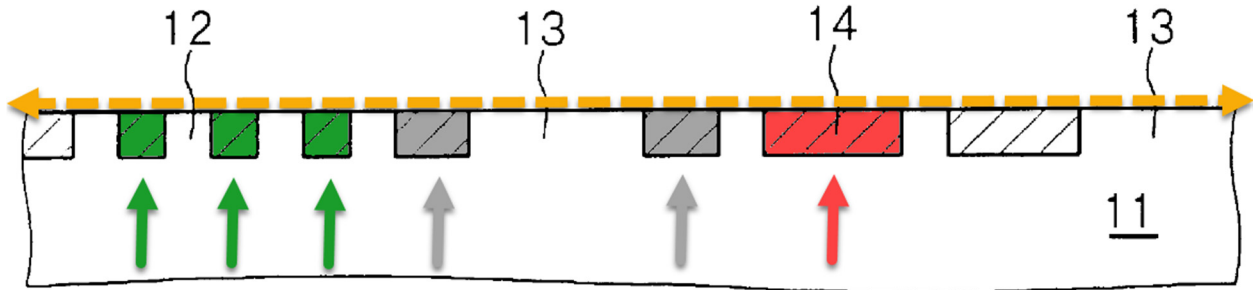
77. Takahashi in combination with Tonishi discloses this limitation.

Takahashi discloses that the upper surface of the conductive lines are coplanar with the dummy conductor upper surfaces. Takahashi discloses a damascene process where a metal layer 14 is deposited on the entire surface of the semiconductor covering the dummy trenches (gray arrows), first trench (red arrow) and second trenches (green arrows), as shown in annotated Figure 4C:



78. The metal layer is “**flattened by a [CMP] process** using, for example, the polishing apparatus shown in FIG. 11,” resulting in a planar topography shown in annotated Figure 4D:

Fig. 4D



Ex-1005, Fig. 4D. Takahashi discloses “**uniform polishing**” to form the planar topography. *Id.*, 18:50-55; 16:36-39 (“Even when there is a great fluctuation in pattern area ratio  $\alpha'$  in the patterned first layer 12, the second layer 14 can be uniformly polished since the dummy pattern 13 is formed”). As a result, the upper surfaces of the conductive lines (green and red) are coplanar with the upper surfaces of the dummy lines (gray).

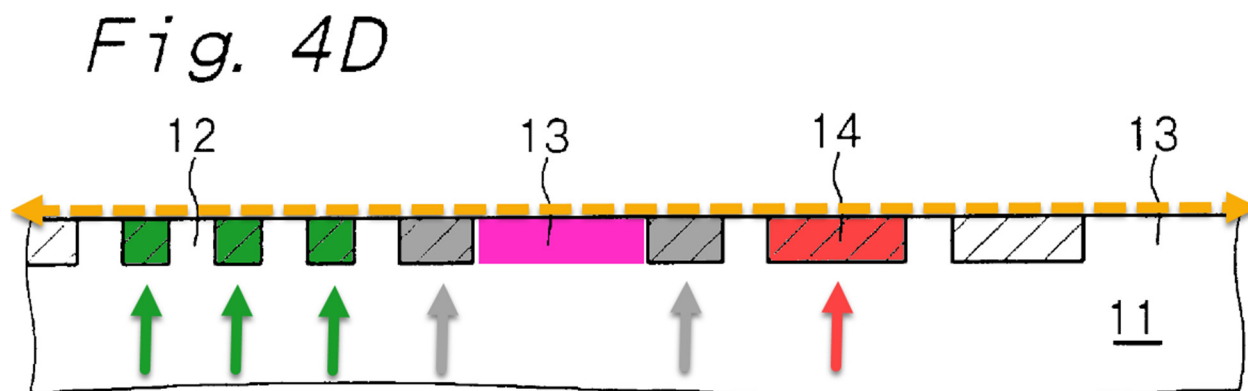
79. Thus, Takahashi in combination with Tonishi discloses this claim limitation. Accordingly, Takahashi in combination with Tonishi renders obvious Claim 16.

3. **Claim 17: “The substantially planar semiconductor topography of claim 16, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces”**

80. Takahashi in combination with Tonishi discloses this claim.

Takahashi discloses polishing of a metal layer 14 above a first dielectric layer 11.

The metal layer is “**flattened by a [CMP] process** using, for example, the polishing apparatus shown in FIG. 11,” and “the second layer 14 can be **uniformly polished** since the dummy pattern 13 is formed.” Ex-1005, 16:32-39. The result is the planar topography shown in annotated Figure 4D:



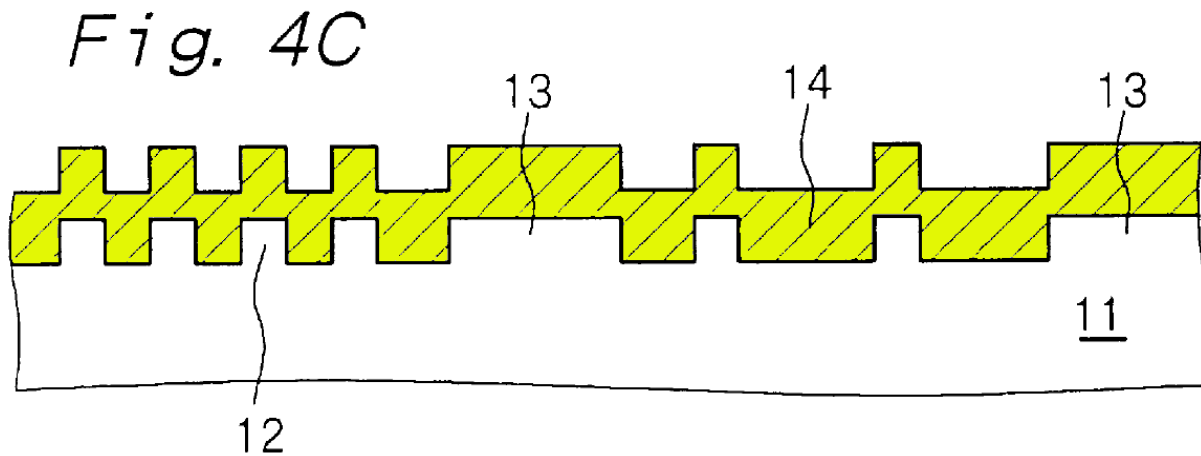
81. Takahashi discloses the metal interconnects and dummy lines (green, red, and gray) separated by dielectric material 11, such as SiO<sub>2</sub>. *Id.*, 16:18-21. That includes the dummy pattern 13 (pink) formed from such dielectric material between adjacent pairs of dummy trenches (gray). That dummy pattern constitutes a dielectric protrusion. Because the semiconductor layer has been “**uniformly polished**,” the upper surface of the dummy dielectric protrusion and the adjacent dummy conductor surfaces are coplanar. This pattern is repeated numerous times across the semiconductor wafer being processed. *Id.*, 14:43-44 (“[A] plurality of chips are produced on one wafer with the mask.”); 16:9-17 and Figures 3A-3D (showing a plurality of “dummy patterns”); Figures 4A-4D (showing a plurality of dummy conductors in “a variant of” Figures 3A-3D).

82. Thus, Takahashi in combination with Tonishi renders obvious Claim 17.

4. **Claim 18: “The substantially planar semiconductor topography of claim 16, wherein said dummy conducts comprise a metal selected from the group consisting of a aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof”**

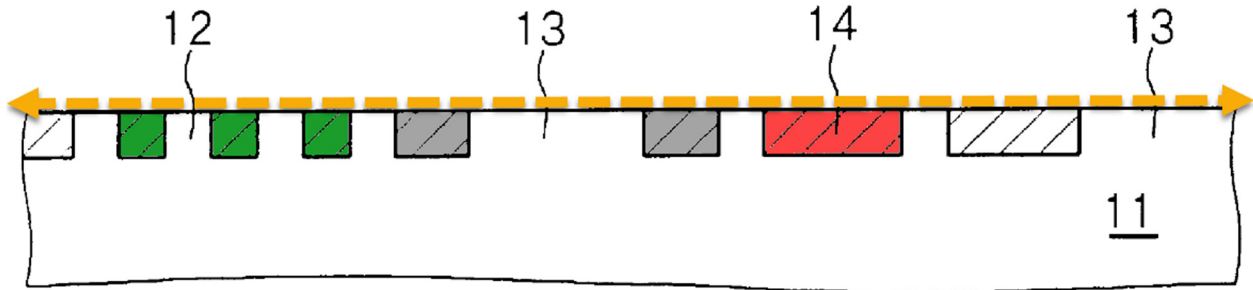
83. Takahashi in combination with Tonishi discloses this claim.

Takahashi discloses depositing a second “**metal wiring material layer**” 14 over the first dielectric layer 11 by known methods such as CVD, as shown in Figure 4C below to create both the dummy conductors and the conductive lines:



Ex-1005, 16:29-43 and Fig. 4C. Takahashi teaches that the second layer 14 can be a “layer of metal such as an **aluminum alloy, tungsten, copper, or silver.**” *Id.*, 6:47-48. That layer then forms the dummy conductors and conductive lines.

*Fig. 4D*



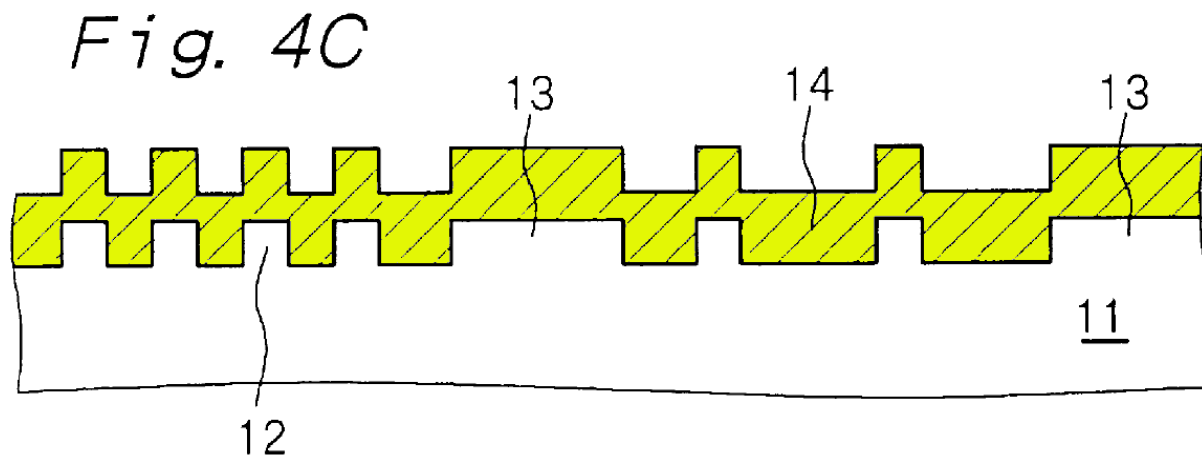
84. Tonishi also discloses that “[t]he metal wires 2 and 3 and the dummy wire 4 are formed of **aluminum or an aluminum based alloy.**” Ex-1007, ¶16.

85. Thus, Takahashi in combination with Tonishi renders obvious Claim 18.

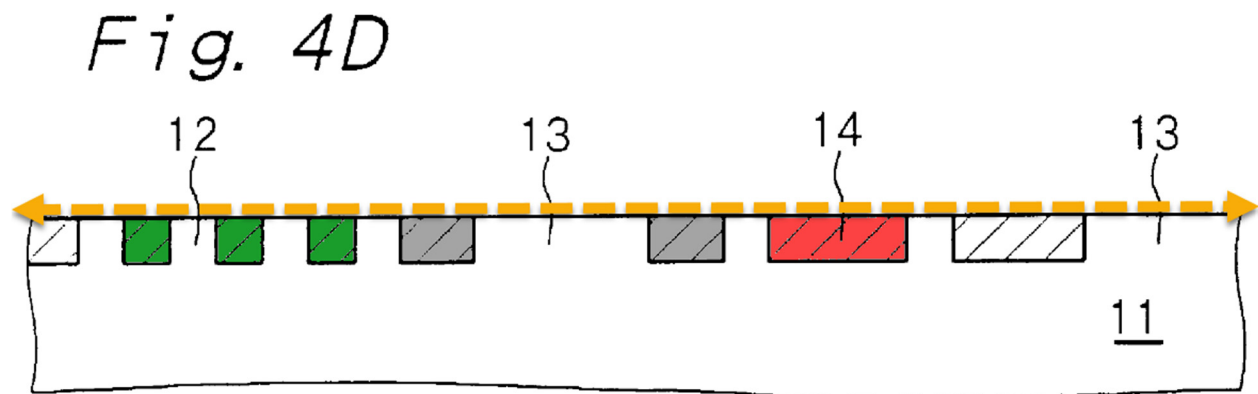
5. **Claim 19: “The substantially planar semiconductor topography of claim 16, wherein said conductive lines comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof”**

86. Takahashi in combination with Tonishi discloses this claim.

Takahashi discloses depositing a second “metal wiring material layer” 14 over the first dielectric layer 11 by known methods such as CVD, as shown in Figure 4C below to create both the dummy conductors and the conductive lines:



Ex-1005, 16:29-43 and Fig. 4C. Takahashi teaches that the second layer 14 can be a “layer of metal such as an **aluminum alloy, tungsten, copper, or silver.**” *Id.*, 6:47-48. That layer then forms the dummy conductors and conductive lines.



87. Tonishi also discloses that “[t]he metal wires 2 and 3 and the dummy wire 4 are formed of **aluminum or an aluminum based alloy.**” Ex-1007, ¶16.

88. Thus, Takahashi in combination with Tonishi renders obvious Claim 19.

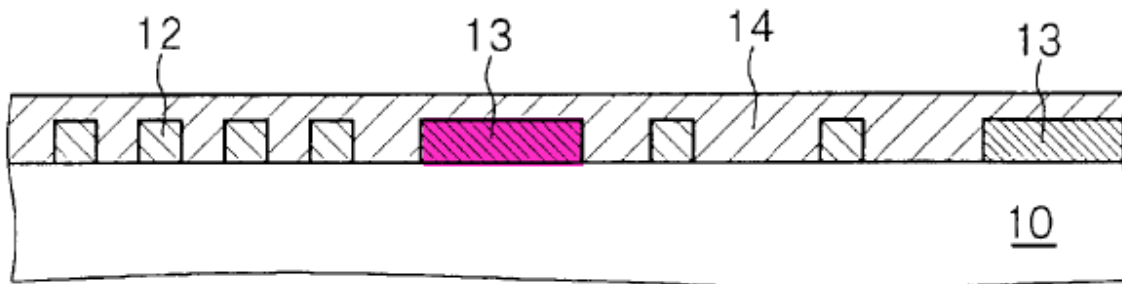
6. **Claim 20: “The substantially planar semiconductor topography of claim 16, wherein lateral dimensions of the**

**laterally spaced dummy trenches are between  
approximately 1 micron and approximately 5 microns”**

89. Takahashi in combination with Tonishi discloses this claim. Tonishi discloses the narrower range of 1-5 $\mu$ m as being a favored size for dummy lines. With reference to Figure 1, Tonishi discloses a lower bound where the dummy line is “substantially equal” to the narrow line, with a width of “for example **1 $\mu$ m.**” Ex-1007, ¶¶16. Alternatively, Tonishi specifically discloses a “predetermined wire-width [of] **5 $\mu$ m,**” for the dummy wires. *Id.*, ¶13; *see id.* ¶¶11-13 and claims 1-3. I understand that when a patent claims a range, it is anticipated by a prior art reference which discloses a point within the range. Thus, because Tonishi discloses both 1 $\mu$ m and 5 $\mu$ m dummy lines, Tonishi discloses dummy trenches having lateral dimensions between approximately 1-5 $\mu$ m.

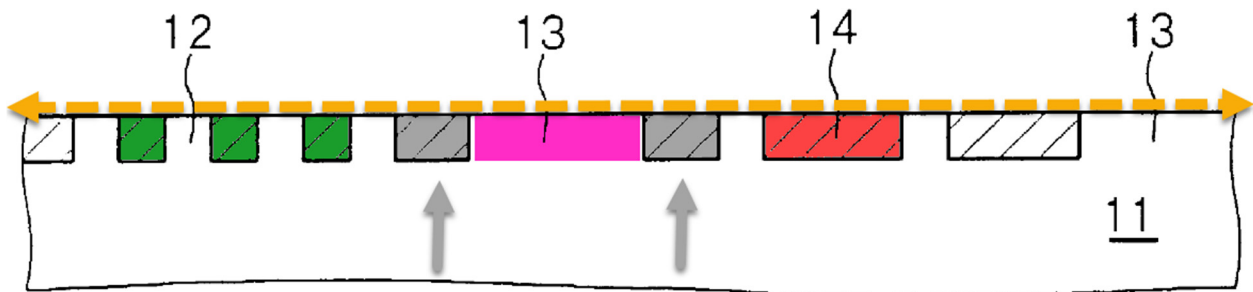
90. Takahashi also discloses this limitation. Takahashi discloses the use of dummy wires of various sizes, including dummy wires of 5 $\mu$ m. For example, in the subtractive process shown in Figure 3D, the dummy pattern 13 (pink) is shown as a metal dummy wire:

*Fig. 3D*



91. Conversely, in the damascene process shown in Figure 4D, the dummy pattern 13 (pink) is shown as an oxide protrusion 13 set apart by two dummy lines:

*Fig. 4D*



92. Takahashi teaches that there is “a space, e.g., of **5  $\mu\text{m}$**  between the pattern and the dummy pattern.” Ex-1005, 7:39-40. In the damascene process of Figure 4D, then, the space between the oxide dummy pattern 13 and the oxide pattern 12 is the dummy lines in gray. Takahashi teaches that those dummy lines are 5  $\mu\text{m}$  wide. Thus, Takahashi discloses dummy lines of 5  $\mu\text{m}$ , which overlaps with the range cited in Claim 20 and renders obvious the limitation. *Ineos*, 783



F.3d at 869.

93. Thus, Takahashi in combination with Tonishi renders obvious Claim 20.

**7. Claim 21: “The substantially planar semiconductor topography of claim 16, wherein the lateral dimension of the first trench is greater than approximately 50 microns”**

94. Tonishi gives representative widths of wide power supply and ground wires of “**approximately 40  $\mu\text{m}$  to 80  $\mu\text{m}$** ” and discloses the example of Figure 1, in which the metal wire is a power supply wire or ground wire. Ex-1007, ¶¶3, 16. This overlaps with the claimed range of “greater than approximately 50 microns.”

95. To the extent that the Patentee argues there is a distinction between the range of 40-80 $\mu\text{m}$  disclosed in Tonishi and the range of “greater than approximately 50 microns,” recited in Claim 21, there is no evidence that the distinction is “critical” or achieves “unexpected results.” *See In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003). The ’946 Patent acknowledges that “[t]he widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria.” Ex-1001, 4:17-20. The ’946 Patent fails to disclose how the use of a wide trench of less than 50 $\mu\text{m}$  would lead to distinct or unexpected results, or otherwise be critical to the claimed invention.

96. Thus, Takahashi in combination with Tonishi renders obvious Claim

21.

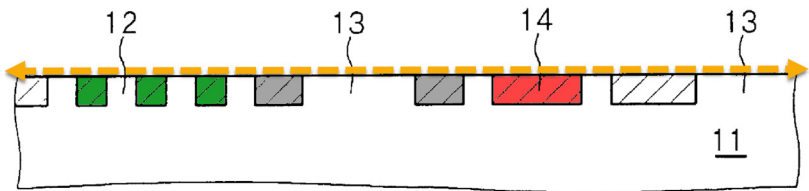
**8. Claim 22: “The substantially planar semiconductor topography of claim 16, wherein the series of the second trenches comprise sub-micron lateral dimensions”**

97. Tonishi discloses narrow signal lines with “a minimum wire-width of approximately 0.8  $\mu\text{m}$  to 1.2  $\mu\text{m}$ ,” and discloses the example of Figure 1, in which the narrow wire is “for transmitting electrical signals.” Ex-1007, ¶¶3, 16. As applied to Takahashi, the signal lines would be formed in trenches of the same size using the damascene process. A signal line and corresponding trench under 1 $\mu\text{m}$  is sub-micron.

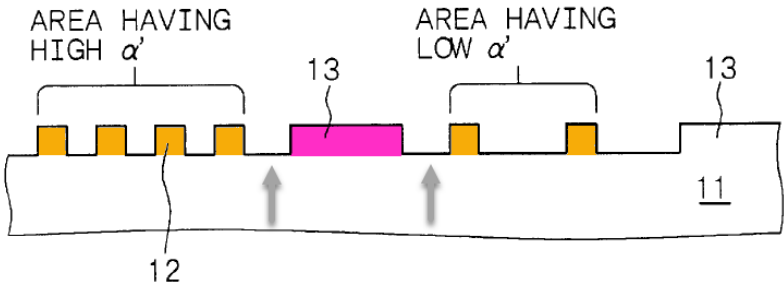
98. To the extent that the Patentee argues there is a distinction between the range of 0.8-1.2 $\mu\text{m}$  disclosed in Tonishi and the range of “sub-micron lateral dimensions,” recited in Claim 22, there is no evidence that the distinction is “critical” or achieves “unexpected results.” The ’946 Patent acknowledges that “[t]he widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria.” Ex-1001, 4:17-20. The ’946 Patent fails to disclose how the use of a narrow trenches between 1.0-1.2 $\mu\text{m}$  or under 0.8 $\mu\text{m}$  would lead to distinct or unexpected results, or otherwise be critical to the claimed invention.

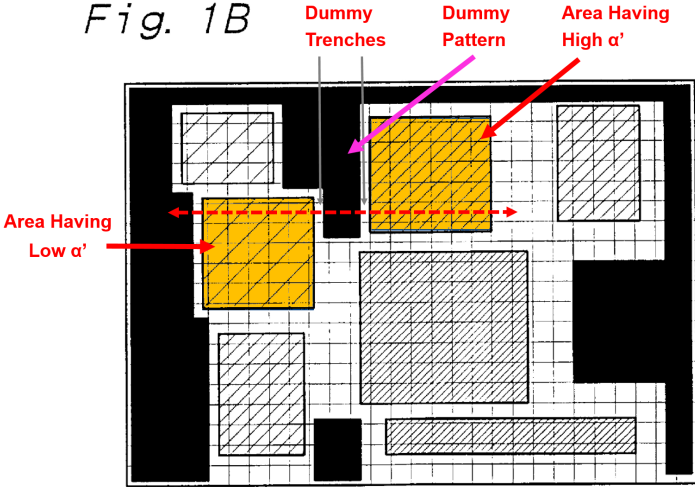
99. Thus, Takahashi and Tonishi disclose or render obvious Claim 22.

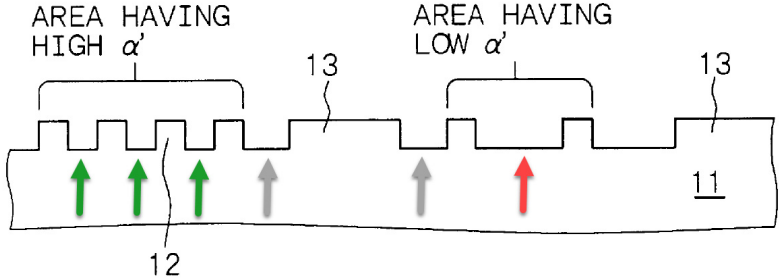
9. Claim Chart

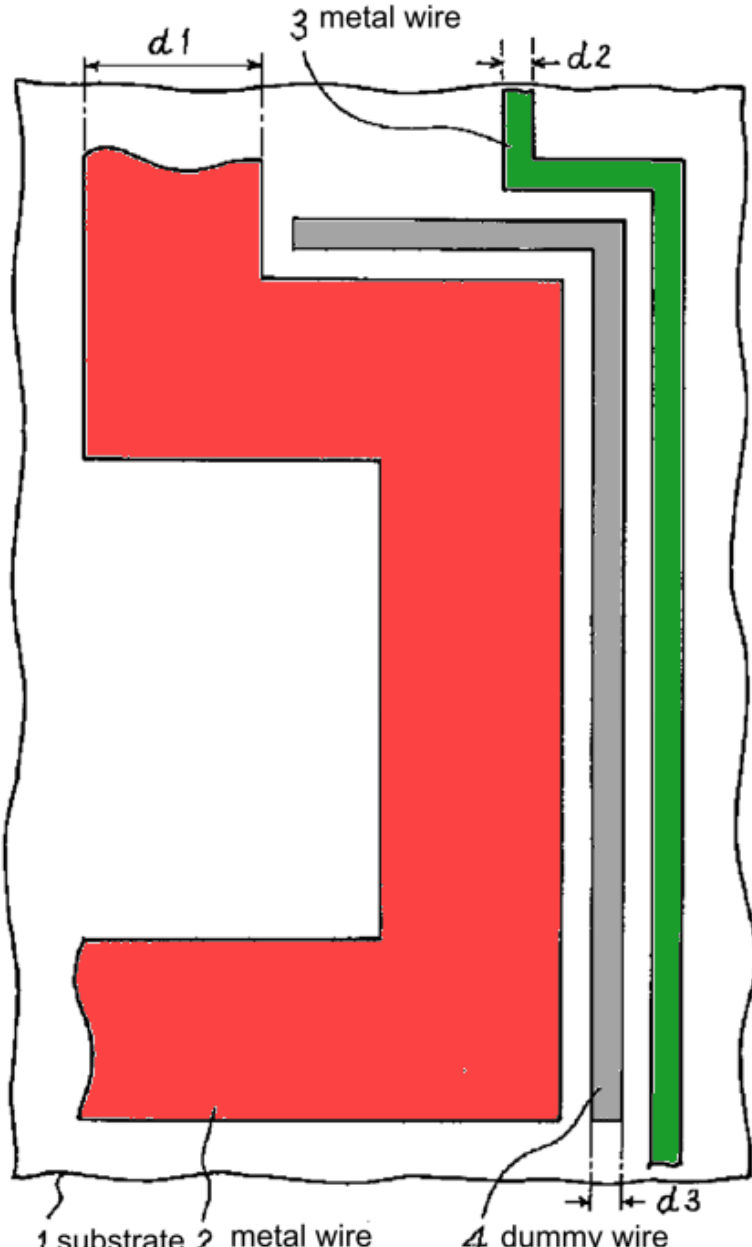
| I.  | U.S. Patent No. 6,849,946                                    | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     | <b>Claim 16</b>                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 16P | A substantially planar semiconductor topography, comprising: | <p>Takahashi at Abstract (“A method of designing a mask pattern to be formed in a mask used for manufacturing an integrated circuit by forming a pattern in a first layer deposited on a substrate, on the basis of lithography to which said mask is applied, then depositing a second layer on the substrate including the patterned first layer and <b>flattening the second layer by a chemical/mechanical polishing process</b>, the method comprising the steps of (A) dividing the mask pattern into meshes having the form of a lattice and having a predetermined size, and determining pattern area ratios <math>\alpha_0(i,j)</math> of the meshes(i,j), respectively, (B) determining an average pattern area ratio <math>\beta(i,j)</math> within a predetermined region including a mesh(i,j) as the central point in the predetermined region with regard to each of all the meshes in the mask pattern, and (C) providing a dummy pattern to each of the meshes(i,j) which have been found in the step (B) to have the average pattern area ratios <math>\beta(i,j)</math> smaller than a predetermined value.”)</p> <p>Fig. 4D of Takahashi (reproduced and annotated below) depicts a planar topography, as indicated by the orange line.</p> <p><i>Fig. 4D</i></p>  <p>Takahashi 16:18-43 (“As shown in the schematic partial cross-sectional view of FIG. 4A, first, a first layer 11 composed of, for example, SiO<sub>2</sub> is deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub> by a CVD method. Then, a pattern is</p> |

| I.  | U.S. Patent<br>No. 6,849,946                                                                                                                                                | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                                                                                                                                                                             | <p>formed in the first layer 11 by lithography using a mask produced on the basis of the method of designing a mask pattern explained in Example 1 and by etching (see FIG. 4B). The above pattern is, for example, a concave portion (groove portion) formed in the first layer 11. The mask has a dummy pattern, and a dummy pattern 13 is also formed concurrently in the first layer 11. Then, a second layer 14 (for example, metal wiring material layer) is deposited on the entire surface, e.g., by a CVD method or a sputtering method (see FIG. 4C), and the second layer 14 is flattened by a CPM process using, for example, the polishing apparatus shown in FIG. 11 (see FIG. 4D). In Example 3, the second layer 14 is flattened by a CMP process such that the surface of the patterned first layer 12 is exposed. Even when there is a great fluctuation in pattern area ratios <math>\alpha'</math> in the patterned first layer 12, <b>the second layer 14 can be uniformly polished since the dummy pattern 13 is formed.</b> As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first layer 11 can be effectively prevented, or the excessive polishing of the second layer 14 can be also effectively prevented.”)</p> |
| 16A | <p>a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches, wherein each of the second trenches is</p> | <p>ig. 4B of Takahashi (reproduced and annotated below) depicts patterned areas that form part of the circuit (orange) as well as a dummy pattern (pink). The areas forming the circuit are bounded by brackets and labeled the “area having high <math>\alpha</math>” and “area having low <math>\alpha</math>” that form part of an integrated circuit. There is a space between the pattern and the dummy pattern that constitutes the dummy trenches (gray arrows).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| I. | U.S. Patent No. 6,849,946                                                                                                                                                                                                                                                                | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
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|    | <p>relatively narrow compared to the first trench and wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches;</p> | <p><i>Fig. 4B</i></p>  <p>Takahashi at 7:21-26 (“In the method of designing a mask pattern according to the first, second or third aspect of the present invention, or in the method of manufacturing an integrated circuit according to the first, second or third aspect of the present invention, <b>the term ‘dummy pattern’ means a pattern which does not constitute any circuit of an integrated circuit.</b>”)</p> <p>Takahashi at 7:35-44 (“On the other hand, when a mesh(i,j) where a dummy pattern is to be provided has a pattern area ratio <math>\alpha_0(i,j)</math> other than 0, the mesh can be provided with a <b>dummy pattern which does not overlap a pattern and has a space, e.g., of 5 <math>\mu\text{m}</math> between the pattern and the dummy pattern.</b> When the above space cannot be provided, or when the dummy pattern to be provided is too small (smaller than a size about twice as large as a minimum design size), it is not necessary to provide such dummy pattern.”)</p> <p>Fig. 1B of Takahashi (reproduced and annotated below) includes a cross-section taken of a segment (dashed red line) that corresponds to Figures 4B-4D. Between the dummy pattern (black) and the circuit blocks (orange) are spaces (gray arrows) that, in a damascene process, constitute trenches between the dummy pattern and the circuit blocks. The circuit block area having high <math>\alpha'</math> with dense hatching is on the right, and the circuit block area having low <math>\alpha'</math> with sparse hatching is on the left.</p> |

| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>Further, a space of 5<math>\mu</math>m is present between the dummy pattern and the circuit blocks.</p> <p><i>Fig. 1B</i></p>  <p>Takahashi at 15:13-17 (“In FIGS. 1A and 1B, rectangular regions surrounded by thick lines show the circuit blocks, and the <b>circuit blocks having higher pattern area ratios are indicated by hatching more densely</b>. Further, squares formed by vertical lines and horizontal lines indicate meshes.”)</p> <p>Takahashi at 15:18-22 (“FIG. 1B schematically shows a state in which meshes(i,j) in which <math>\beta(i,j) &lt; 0.9 (= \beta_0)</math> are provided with dummy patterns after the average pattern area ratios <math>\beta(i,j)</math> are determined based on the equations (1-1) and (1-2). <b>In FIG. 1B, the dummy patterns are blackened.</b>”)</p> <p>Fig. 4B of Takahashi (reproduced and annotated below) depicts the plurality of dummy trenches (gray arrows) laterally spaced between a first trench (red arrow) and a series of second trenches (green arrows). The first trench (red arrow) is depicted as having a greater lateral dimension than the plurality of second trenches (green arrows). The dummy trenches (gray arrows) are depicted as having an intermediate width.</p> |

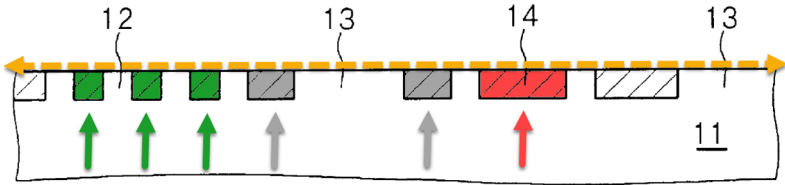
| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p><i>Fig. 4B</i></p>  <p>Takahashi at 16:18-28 (“As shown in the schematic partial cross-sectional view of FIG. 4A, first, a first layer 11 composed of, for example, SiO<sub>2</sub> is deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub> by a CVD method. Then, <b>a pattern is formed in the first layer 11 by lithography using a mask produced on the basis of the method of designing a mask pattern explained in Example 1 and by etching (see FIG. 4B).</b> The above pattern is, for example, a concave portion (groove portion) formed in the first layer 11. The mask has a dummy pattern, and a dummy pattern 13 is also formed concurrently in the first layer 11.”)</p> <p>Tonishi at Abstract (“A dummy wire 4 is provided between a first metal wire 2 having a wide and a second metal wire 3 having a narrow wire-width. <b>The wire-width of the dummy wire 4 is between the wire-width of the first metal wire 2 and the wire-width of the second metal wire 3.</b>”)</p> <p>Fig. 1 of Tonishi (reproduced and annotated below) depicts a laterally spaced dummy line (gray) between a wide metal line (red) and a narrow metal line (green).</p> |

| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 ("Takahashi") in view of<br>Japanese Patent Application 4-262535 ("Tonishi")                                                                                                                                                                                                                                                       |
|----|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p style="text-align: center;"><b>[FIG. 1]</b></p>  <p>Tonishi at ¶3 ("For example, in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, <b>the widths of these metal wires</b></p> |



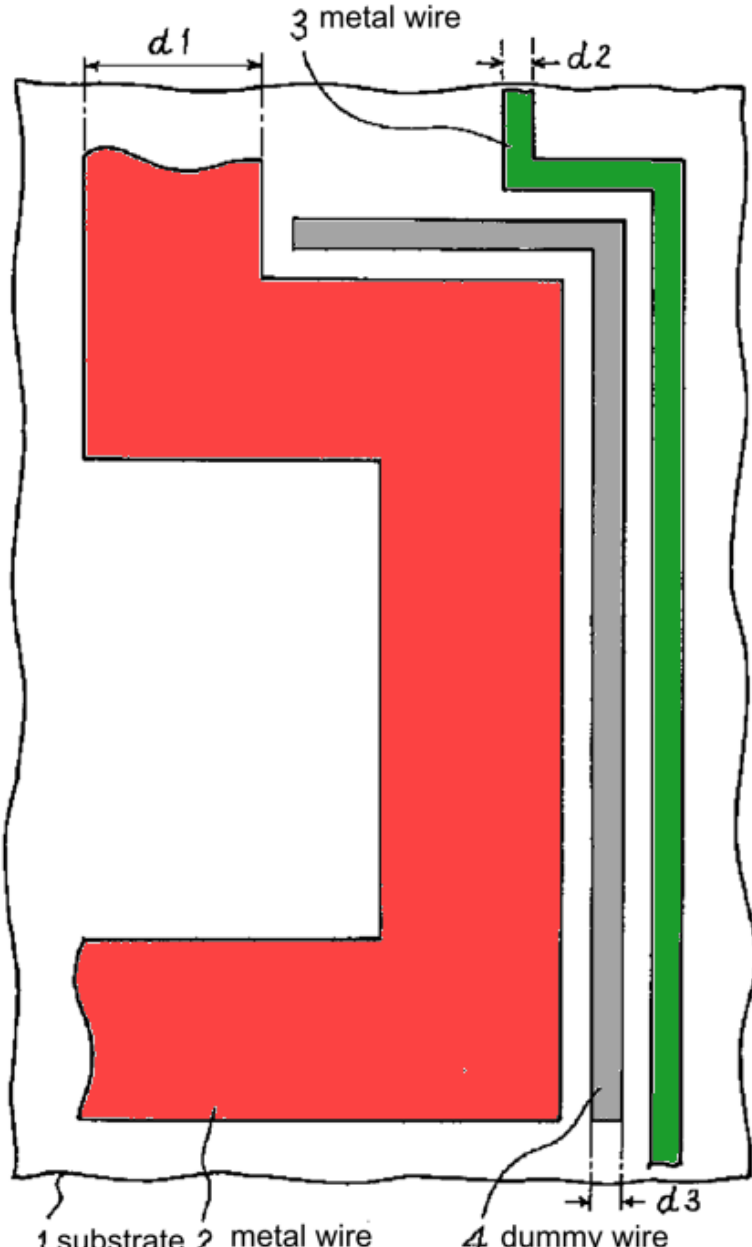
| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>are, for example, a minimum wire-width of approximately 0.8 <math>\mu\text{m}</math> to 1.2 <math>\mu\text{m}</math> for metal wires that transmit electrical signals, and is approximately 40 <math>\mu\text{m}</math> to 80 <math>\mu\text{m}</math> for the thickest metal wires, such as power supply wires and ground wires; furthermore, this is approximately 5 <math>\mu\text{m}</math> to 20 <math>\mu\text{m}</math> for the intermediate metal wires, with various wire-widths being used depending on the applications thereof.”)</p> <p>Tonishi at ¶4 (“The wire-widths of the metal wires in this conventional semiconductor integrated circuit device are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life; for example, a wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires, than for other metal wires. Furthermore, <b>for metal wires where one wishes to avoid the influence of noise to as great an extent as possible, and where one wishes to achieve a stable potential, for example, ground wires and various signal wires, the wire-width is made wider than or equal to requirements based on the electromigration life.</b> In any case, the minimum wire-width of each of the metal wires is defined according to the individual application, and these are always designed so as to be greater than or equal to this wire-width.”)</p> <p>Tonishi at ¶5 (“Meanwhile, <b>with increasing levels of integration in semiconductor integrated circuit devices, it is necessary to arrange metal wires having wire-widths sufficient to satisfy the conditions described above in a limited area, and therefore the spacing between the metal wires is also narrowed,</b> such that in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, the minimum wire spacing is approximately 0.8 <math>\mu\text{m}</math> to</p> |

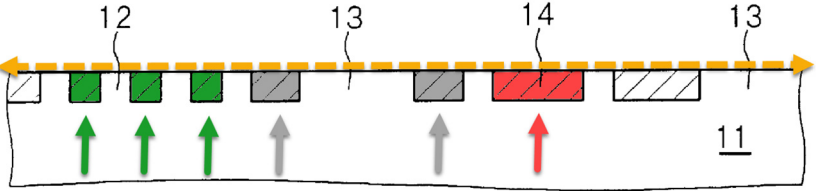
| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>1.2 <math>\mu\text{m}</math>.”)</p> <p>Tonishi at ¶11-13 (“[0011] [Means for Solving the Problems] The semiconductor integrated circuit device of the present invention comprises, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; <b>and a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width</b> and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.</p> <p>[0012] Furthermore, this has a structure <b>wherein a plurality of second metal wires having differing second widths are formed, and the third width of the dummy wire is greater than or equal to the minimum wire-width among the second wires and less than or equal to the wire-width of the first wire.</b></p> <p>[0013] Furthermore, this has a structure wherein the <b>predetermined wire-width is 5 <math>\mu\text{m}</math>.</b>”)</p> <p>Tonishi at ¶16 (“This embodiment has a structure comprising, on substrate 1: <b>a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 <math>\mu\text{m}</math>) that is wider than 5 <math>\mu\text{m}</math> and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 <math>\mu\text{m}</math>) that is narrower than 5 <math>\mu\text{m}</math> and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to</b></p> |

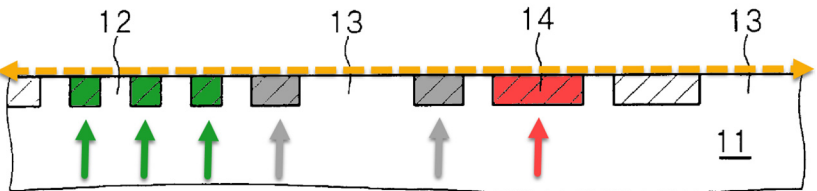
| I.  | U.S. Patent No. 6,849,946                                                                                                                                 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                                                                                                                                                           | <p>the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.”)</p> <p>Tonishi at Claim 1 (“A semiconductor integrated circuit device characterized by comprising, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; and <b>a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width</b> and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.”)</p> |
| 16B | dummy conductors in said laterally spaced dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and | <p>Fig. 4D of Takahashi (reproduced and annotated below) depicts dummy conductors (gray rectangles) in the dummy trenches. They are electrically separate from electrically conductive features below the dummy conductors (not depicted).</p> <p><i>Fig. 4D</i></p>  <p>Takahashi at 16:18-28 (“As shown in the schematic partial cross-sectional view of FIG. 4A, first, <b>a first layer 11 composed of, for example, SiO<sub>2</sub></b> is deposited on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub> by a CVD method. Then, a pattern is</p>                                                                                                                                                                                                                                                                                                                                              |

| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>formed in the first layer 11 by lithography using a mask produced on the basis of the method of designing a mask pattern explained in Example 1 and by etching (see FIG. 4B). The above pattern is, for example, a concave portion (groove portion) formed in the first layer 11. The mask has a dummy pattern, and a dummy pattern 13 is also formed concurrently in the first layer 11.”)</p> <p>Takahashi at 7:21-44 (“In the method of designing a mask pattern according to the first, second or third aspect of the present invention, or in the method of manufacturing an integrated circuit according to the first, second or third aspect of the present invention, <b>the term "dummy pattern" means a pattern which does not constitute any circuit of an integrated circuit.</b> The predetermined value <math>\beta_0</math> which is compared with the average pattern area ratios <math>\beta(i,j)</math> may be, for example, 0.8, while the predetermined value <math>\beta_0</math> shall not be limited thereto and can be determined as required depending upon a mask pattern to be designed. When a mesh(i,j) where a dummy pattern is to be provided has a pattern area ratio <math>\alpha_0(i,j)</math> of 0, a dummy pattern can be provided in the entire area of the mesh(i,j). In this case, the pattern area ratio <math>\alpha_0(i,j)</math> of the mesh provided with the dummy pattern is 1. On the other hand, when a mesh(i,j) where a dummy pattern is to be provided has a pattern area ratio <math>\alpha_0(i,j)</math> other than 0, the mesh can be provided with <b>a dummy pattern which does not overlap a pattern and has a space, e.g., of 5 <math>\mu\text{m}</math> between the pattern and the dummy pattern.</b> When the above space cannot be provided, or when the dummy pattern to be provided is too small (smaller than a size about twice as large as a minimum design size), it is not necessary to provide such dummy pattern.”)</p> <p>Takahashi at 16:13-17 (“According to the method of manufacturing <b>an integrated circuit in Example 3, for example, a buried (embedded) wiring</b> can be formed.</p> |

| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>The method of manufacturing an integrated circuit in Example 3 will be explained with reference to FIGS. 4A to 4D hereinafter.”)</p> <p>Takahashi at 18:56-65 (“When <b>the underlayer is composed of a plurality of layers (N layers)</b>, the equation (2) or (3) can be applied depending upon whether or not a CPM process is applied to each layer. That is, when <b>the underlayer is composed of a first layer, a second layer, . . . an N-th layer</b>, <math>\alpha_0(i,j)</math> of each layer can be determined on the basis of the following equation (19-1), (19-2), (19-3) or (19-4) depending upon whether or not a CPM process is applied to the layers. In the equations (19-1) and (20-1), a subscript “n” is the number of a layer constituting the underlayer, and <math>n=1, 2, \dots N-1</math>.”)</p> <p>Fig. 1 of Tonishi (reproduced and annotated below) depicts a dummy wire (gray) electrically separate from the wide metal wire (red) and narrow metal wire (green).</p> |

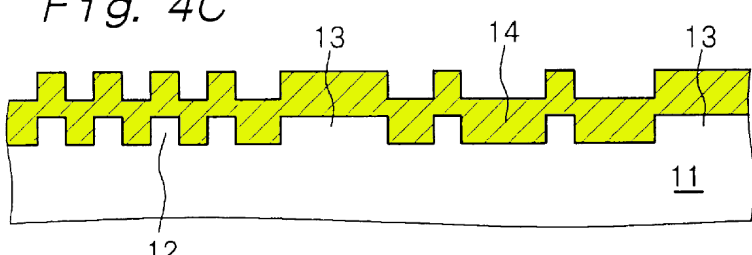
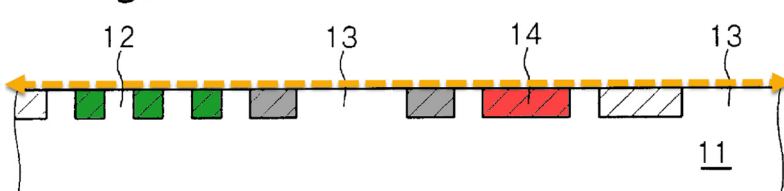
| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                    |
|----|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p style="text-align: center;"><b>[FIG. 1]</b></p>  <p>Tonishi at ¶16 (“This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a</p> |

| I.  | U.S. Patent No. 6,849,946                                                                                                                                                                        | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                                                                                                                                                                                                  | <p>predetermined wire-width d1 (for example, 40 <math>\mu\text{m}</math>) that is wider than 5 <math>\mu\text{m}</math> and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 <math>\mu\text{m}</math>) that is narrower than 5 <math>\mu\text{m}</math> and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, <b>electrically isolated from the first and second metal wires 2 and 3</b>. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.”)</p>                                                                                                                                 |
| 16C | <p>conductive lines in said series of second trenches and said first trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.</p> | <p>Fig. 4D of Takahashi (reproduced and annotated below) depicts conductive lines (red and green rectangles) in the respective first and second trenches, and dummy conductors (gray) in the respective dummy trenches. The upper surfaces of the conductive lines are substantially coplanar with the upper surfaces of the dummy conductors, as indicated by the orange arrow.</p> <p><i>Fig. 4D</i></p>  <p>Takahashi at 16:29-43: (“Then, a second layer 14 (for example, metal wiring material layer) is deposited on the entire surface, e.g., by a CVD method or a sputtering method (see FIG. 4C), and the second layer 14 is flattened by a CPM process using, for example, the polishing apparatus shown in FIG. 11 (see FIG. 4D). In Example 3, the second layer 14 is flattened by a CMP process such that the surface of the patterned first layer</p> |

| I. | U.S. Patent No. 6,849,946                                                                                                                                                                        | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                                                                                                                                                                                  | <p>12 is exposed. Even when there is a great fluctuation in pattern area ratios <math>\alpha'</math> in the patterned first layer 12, <b>the second layer 14 can be uniformly polished since the dummy pattern 13 is formed.</b> As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first layer 11 can be effectively prevented, or the excessive polishing of the second layer 14 can be also effectively prevented.”)</p> <p>Takahashi at 18:50-55 (“Therefore, the equations (18-1) and (18-2) are divided by <math>h_5</math>, to give the equations (2) and (3). In Example 6, in the above manner, a so-called pattern volume ratio is made uniform within a mask pattern. That is, <b>the second layer (layer) can be uniformly flattened by providing dummy patterns</b> to the meshes having small pattern volume ratios.”)</p> |
|    | <b>Claim 17</b>                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 17 | <p>The substantially planar semiconductor topography of claim 16, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy</p> | <p>Fig. 4D of Takahashi (reproduced and annotated below) depicts a dummy dielectric protrusion (pink) between a pair of dummy trenches with dummy conductors (gray), where the upper surface of the dielectric material is coplanar with the upper surface of the dummy conductors, as indicated by the orange arrow.</p> <p><i>Fig. 4D</i></p>  <p>Takahashi at 14:32-56 (“In Example 1, meshes having the form of a lattice have a predetermined size of <math>100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}</math>. Average pattern area ratios <math>\beta(i,j)</math> were determined on the basis of the following equations (1-1)</p>                                                                                                                                                                                           |

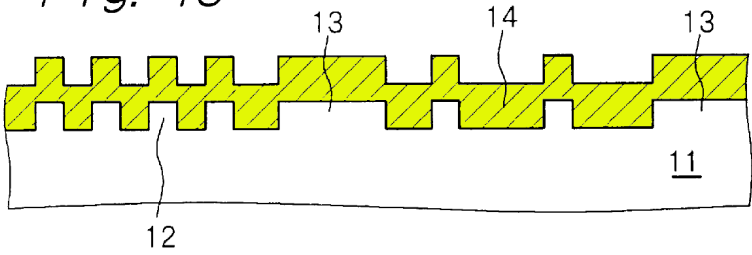
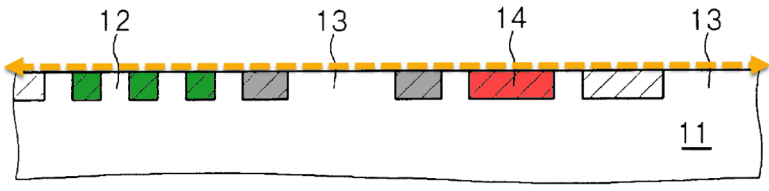


| I. | U.S. Patent No. 6,849,946                                                                                                      | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----|--------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    | dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces. | <p>and (1-2). In the equation (1-1), 10 was used as a value of <math>m</math>, and 9 was used as a value of <math>Q</math>. That is, a predetermined region of a mask pattern including a <math>mesh(i,j)</math> as the central point in the predetermined region has a size of <math>2100\ \mu m \times 2100\ \mu m</math>. In other words, the average pattern area ration <math>\beta(i,j)</math> is determined as an average of pattern area ratios within a <math>2100\ \mu m \times 2100\ \mu m</math> region including the <math>mesh(i,j)</math> as the central point. Further, the value of <math>\alpha_{q+1}(i,j)</math> was smoothed (averaged) 10 times. Generally, since <b>a plurality of chips are produced on one wafer with the mask</b>, when a position of a mesh <math>(i+1,j+k)</math> in the equation (1-1) deviates from the mask pattern of one chip, a corresponding pattern area ratio <math>\alpha_0</math> in the region of a mask pattern of one adjacent chip may be used. Further, 0.9 was used as a predetermined value <math>\beta_0</math> in the average pattern area ratios <math>\beta(i,j)</math>. Alternatively, a value of <math>\{\text{maximum value of } \beta(i,j)\} - 1!</math> may be used as a predetermined value of <math>\beta_0</math>. When the above value is used as a predetermined value of <math>\beta_0</math>, the value of <math>\beta_0</math> changes after a dummy pattern is provided. It is therefore preferred to repeat the steps (A), (B) and (C), and the arrangement of the dummy patterns can be therefore more optimized. ##EQU2## wherein <math>q=0, 1, 2, \dots, Q</math>.”)</p> <p>Takahashi at 16:18-28 (“As shown in the schematic partial cross-sectional view of FIG. 4A, first, <b>a first layer 11 composed of, for example, SiO<sub>2</sub> is deposited</b> on a flattened underlayer (not shown) composed of, for example, SiO<sub>2</sub> by a CVD method. Then, a pattern is formed in the first layer 11 by lithography using a mask produced on the basis of the method of designing a mask pattern explained in Example 1 and by etching (see FIG. 4B). The above pattern is, for example, a concave portion (groove portion) formed in the first layer 11. The mask has a dummy pattern, and a dummy pattern 13 is also formed concurrently in the first layer 11.”)</p> |

| I. | U.S. Patent No. 6,849,946                                                                                                                                                                          | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                                                                                                                                                                                    | <p>Takahashi at 16:29-43 (“Then, a second layer 14 (for example, metal wiring material layer) is deposited on the entire surface, e.g., by a CVD method or a sputtering method (see FIG. 4C), and the second layer 14 is flattened by a CPM process using, for example, the polishing apparatus shown in FIG. 11 (see FIG. 4D). In Example 3, the second layer 14 is flattened by a CMP process such that the surface of the patterned first layer 12 is exposed. Even when there is a great fluctuation in pattern area ratios <math>\alpha'</math> in the patterned first layer 12, <b>the second layer 14 can be uniformly polished since the dummy pattern 13 is formed. As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first layer 11 can be effectively prevented, or the excessive polishing of the second layer 14 can be also effectively prevented.”)</b></p> |
|    | <b>Claim 18</b>                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 18 | <p>The substantially planar semiconductor topography of claim 16, wherein said dummy conducts comprise a metal selected from the group consisting of a aluminum, copper, tungsten, molybdenum,</p> | <p>Figs. 4C and 4D of Takahashi (reproduced and annotated below) depicts the conductive material that is deposited and polished to form the interconnects and dummy conductors, which may include aluminum, tungsten, or copper.</p> <p><i>Fig. 4C</i></p>  <p><i>Fig. 4D</i></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| I. | U.S. Patent No. 6,849,946               | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    | tantalum, titanium, and alloys thereof. | <p>Takahashi at 6:29-56 (“In the method of designing a mask pattern according to the first or fourth aspect of the present invention, or in the method of manufacturing an integrated circuit according to the first or fourth aspect of the present invention, examples of the (first layer)/(<b>second layer</b>) combination include (polysilicon layer doped with an impurity)/(insulation layer), (<b>layer of a metal such as an aluminum alloy, tungsten, copper or silver</b>)/(insulation layer), (layer of a metal compound such as tungsten silicide or titanium silicide)/(insulation layer), (stacked structure composed of a polysilicon layer doped with an impurity and a layer of a metal compound such as tungsten silicide or titanium silicide)/(insulation layer) and (stacked structure composed of a polysilicon layer doped with an impurity, a layer of a metal compound such as tungsten silicide or titanium silicide and an insulation film)/(insulation layer). Further, examples of the (first layer)/(<b>second layer</b>) combination include (insulation layer)/(polysilicon layer doped with an impurity), (insulation layer)/(<b>layer of a metal such as an aluminum alloy, tungsten, copper or silver</b>), (insulation layer)/(layer of a metal compound such as tungsten silicide or titanium silicide), (insulation layer)/(stacked structure composed of a polysilicon layer doped with an impurity and a layer of a metal compound such as tungsten silicide or titanium silicide) and (insulation layer)/(stacked structure composed of a polysilicon layer doped with an impurity, a layer of a metal compound such as tungsten silicide or titanium silicide and an insulation film).”)</p> <p>Takahashi at 16:29-43 (“Then, a second layer 14 (for example, metal wiring material layer) is deposited on the entire surface, e.g., by a CVD method or a sputtering method (see FIG. 4C), and the second layer 14 is flattened by a CPM process using, for example, the</p> |

| I. | U.S. Patent<br>No. 6,849,946                                                | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
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|    |                                                                             | <p>polishing apparatus shown in FIG. 11 (see FIG. 4D). In Example 3, the second layer 14 is flattened by a CMP process such that the surface of the patterned first layer 12 is exposed. Even when there is a great fluctuation in pattern area ratios <math>\alpha'</math> in the patterned first layer 12, the second layer 14 can be uniformly polished since the dummy pattern 13 is formed. As a result, the surface of the exposed first layer 12 is not deeply polished, and therefore, the excessive polishing of the surface of the first layer 11 can be effectively prevented, or the excessive polishing of the second layer 14 can be also effectively prevented.”)</p> <p>Tonishi at ¶16: (“This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 <math>\mu\text{m}</math>) that is wider than 5 <math>\mu\text{m}</math> and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 <math>\mu\text{m}</math>) that is narrower than 5 <math>\mu\text{m}</math> and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and <b>the dummy wire 4 are formed of aluminum or an aluminum-based alloy.</b>”)</p> |
|    | <b>Claim 19</b>                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19 | The substantially planar semiconductor topography of claim 16, wherein said | Fig. 4C and 4D of Takahashi (reproduced and annotated below) depicts the conductive material that is deposited and polished to form the interconnects and dummy conductors, which may include aluminum, tungsten, or copper.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

| I. | U.S. Patent No. 6,849,946                                                                                                                               | U.S. Patent No. 5,948,573 ("Takahashi") in view of Japanese Patent Application 4-262535 ("Tonishi")                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    | conductive lines comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. | <p><i>Fig. 4C</i></p>  <p><i>Fig. 4D</i></p>  <p>Takahashi 6:29-56 ("In the method of designing a mask pattern according to the first or fourth aspect of the present invention, or in the method of manufacturing an integrated circuit according to the first or fourth aspect of the present invention, examples of the (first layer)/(second layer) combination include (polysilicon layer doped with an impurity)/(insulation layer), (layer of a metal such as an <b>aluminum alloy, tungsten, copper</b> or silver)/(insulation layer), (layer of a metal compound such as tungsten silicide or titanium silicide)/(insulation layer), (stacked structure composed of a polysilicon layer doped with an impurity and a layer of a metal compound such as tungsten silicide or titanium silicide)/(insulation layer) and (stacked structure composed of a polysilicon layer doped with an impurity, a layer of a metal compound such as tungsten silicide or titanium silicide and an insulation film)/(insulation layer). Further, examples of the (first layer)/(second layer) combination include (insulation layer)/(polysilicon layer doped with an impurity), (insulation layer)/(layer of a metal such as an <b>aluminum alloy, tungsten, copper or silver</b>),</p> |

| I. | U.S. Patent<br>No. 6,849,946                                                                                      | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----|-------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                                                                                                   | <p>(insulation layer)/(layer of a metal compound such as tungsten silicide or titanium silicide), (insulation layer)/(stacked structure composed of a polysilicon layer doped with an impurity and a layer of a metal compound such as tungsten silicide or titanium silicide) and (insulation layer)/(stacked structure composed of a polysilicon layer doped with an impurity, a layer of a metal compound such as tungsten silicide or titanium silicide and an insulation film).”)</p> <p>Tonishi at ¶16 (“This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 μm) that is wider than 5 μm and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 μm) that is narrower than 5 μm and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. <b>The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.</b>”)</p> |
|    | <b>Claim 20</b>                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 20 | The substantially planar semiconductor topography of claim 16, wherein lateral dimensions of the laterally spaced | Takahashi at 7:21-44 (“In the method of designing a mask pattern according to the first, second or third aspect of the present invention, or in the method of manufacturing an integrated circuit according to the first, second or third aspect of the present invention, the term "dummy pattern" means a pattern which does not constitute any circuit of an integrated circuit. The predetermined value $\beta_0$ which is compared with the average pattern area ratios $\beta(i,j)$ may be, for example, 0.8, while the predetermined value $\beta_0$ shall not be limited thereto and can be determined as required                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| I. | U.S. Patent No. 6,849,946                                                      | U.S. Patent No. 5,948,573 (“Takahashi”) in view of Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
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|    | dummy trenches are between approximately 1 micron and approximately 5 microns. | <p>depending upon a mask pattern to be designed. When a mesh(i,j) where a dummy pattern is to be provided has a pattern area ratio <math>\alpha_0</math> (i,j) of 0, a dummy pattern can be provided in the entire area of the mesh(i,j). In this case, the pattern area ratio <math>\alpha_0</math> (i,j) of the mesh provided with the dummy pattern is 1. On the other hand, when a mesh(i,j) where a dummy pattern is to be provided has a pattern area ratio <math>\alpha_0</math> (i,j) other than 0, <b>the mesh can be provided with a dummy pattern which does not overlap a pattern and has a space, e.g., of 5 <math>\mu</math>m between the pattern and the dummy pattern.</b> When the above space cannot be provided, or when the dummy pattern to be provided is too small (smaller than a size about twice as large as a minimum design size), it is not necessary to provide such dummy pattern.”)</p> <p>Tonishi at Claim 1 (“A semiconductor integrated circuit device characterized by comprising, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; and <b>a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width</b> and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.”)</p> <p>Tonishi at Claim 2 (“The semiconductor integrated circuit device according to claim 1, wherein a plurality of second metal wires having differing second widths are formed, and <b>the third width of the dummy wire is greater than or equal to the minimum wire-width among the second wires and less than or equal to the wire-width of the first wire.</b>”)</p> |

| I. | U.S. Patent<br>No. 6,849,946 | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                              | <p>Tonishi at Claim 3: (“The semiconductor integrated circuit device according to claim 1, wherein <b>the predetermined wire-width is 5 <math>\mu\text{m}</math>.</b>”)</p> <p>Tonishi at ¶11 (“The semiconductor integrated circuit device of the present invention comprises, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; and <b>a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width and is formed between the first metal wire and the second metal wire</b>, electrically isolated from the second metal wire.”)</p> <p>Tonishi at ¶12 (“Furthermore, this has a structure wherein a plurality of second metal wires having differing second widths are formed, and <b>the third width of the dummy wire is greater than or equal to the minimum wire-width among the second wires and less than or equal to the wire-width of the first wire.</b>”)</p> <p>Tonishi at ¶13 (“Furthermore, this has a structure wherein <b>the predetermined wire-width is 5 <math>\mu\text{m}</math>.</b>”)</p> <p>Tonishi at ¶16: (“This embodiment has a structure comprising, on substrate 1: <b>a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 <math>\mu\text{m}</math>) that is wider than 5 <math>\mu\text{m}</math> and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 <math>\mu\text{m}</math>) that is narrower than 5 <math>\mu\text{m}</math> and is formed at a predetermined spacing</b></p> |



| I. | U.S. Patent<br>No. 6,849,946                                                                                                                               | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
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|    |                                                                                                                                                            | <b>along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2</b> and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|    | <b>Claim 21</b>                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 21 | The substantially planar semiconductor topography of claim 16, wherein the lateral dimension of the first trench is greater than approximately 50 microns. | <p>Tonishi at ¶3 (“For example, in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, the widths of these metal wires are, for example, a minimum wire-width of approximately 0.8 <math>\mu\text{m}</math> to 1.2 <math>\mu\text{m}</math> for metal wires that transmit electrical signals, and is <b>approximately 40 <math>\mu\text{m}</math> to 80 <math>\mu\text{m}</math></b> for the thickest metal wires, such as power supply wires and ground wires; furthermore, this is approximately 5 <math>\mu\text{m}</math> to 20 <math>\mu\text{m}</math> for the intermediate metal wires, with various wire-widths being used depending on the applications thereof.”)</p> <p>Tonishi at ¶16 (“This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 <math>\mu\text{m}</math>) that is wider than 5 <math>\mu\text{m}</math> and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 <math>\mu\text{m}</math>) that is narrower than 5 <math>\mu\text{m}</math> and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.”)</p> |

| I. | U.S. Patent<br>No. 6,849,946                                                                                                                     | U.S. Patent No. 5,948,573 (“Takahashi”) in view of<br>Japanese Patent Application 4-262535 (“Tonishi”)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
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|    |                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|    | <b>Claim 22</b>                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10 | The substantially planar semiconductor topography of claim 16, wherein the series of the second trenches comprise sub-micron lateral dimensions. | <p>Tonishi at ¶3 (“For example, in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, the widths of these metal wires are, for example, a minimum wire-width of <b>approximately 0.8 μm to 1.2 μm</b> for metal wires that transmit electrical signals, and is approximately 40 μm to 80 μm for the thickest metal wires, such as power supply wires and ground wires; furthermore, this is approximately 5 μm to 20 μm for the intermediate metal wires, with various wire-widths being used depending on the applications thereof.”)</p> <p>Tonishi at ¶16 (“This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 μm) that is wider than 5 μm and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 μm) that is narrower than 5 μm and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.”)</p> |

### **VIII. CONCLUSION**

100. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: July 13, 2018

By:  \_\_\_\_\_  
Dr. Michael Thomas