

Curriculum Vitae of Dr. Michael E. Thomas

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Areas of Knowledge

Industrial Engineering Management, Semiconductor Dielectric and Metal Materials Research, Expertise in PVD and CVD Processing of Materials, Interconnect Manufacturing Processes, Packaging Materials Development, Student and Professor Mentoring. Experience in establishment of IP protection and development strategies.

Experience

2003 – Present: Michael E. Thomas – Semiconductor Technology Consultant - Thomas Consulting
Los Altos CA

Activities focused on providing technical expertise and counsel to industrial clients in the areas of semiconductor process technology and intellectual property. Technical expertise in the areas of state of the art thin film electronic materials, the history of materials use in the semiconductor industry and new methods of using opto-electronic interconnect materials. Below is a summary of my major consulting activities to date:

- 4/2015- 8/2015 Provided consulting services to Kenyon and Kenyon, LLP, regarding patent litigation between Micron v. MIT. Case resolved prior to any Court proceedings.
- 6/2014-10/2014. Provided short term consulting services to Steptoe and Johnson LLP, regarding patent litigation involving Raytheon vs. Samsung, SONY, Apple and OmniVision. Consulting for Raytheon. Consulting services concluded prior to Court hearing.
- 4/2014 – 6/2015. Provided Consulting service as expert to Cabot Microelectronics in pending litigation of CMC vs. Davies regarding slurry technology. Case settled out of court.
- 2/2011 – 4/2014. Provided Consulting Services for Elpida Corporation vs. Intellectual Ventures and Elpida Corporation vs. MOSAID through the Law Offices of Kenyon and Kenyon, New York, N.Y. - Case settled.
- 10/2011: Providing Consulting Services for Microchip Corporation for Microchip Corporation vs. LSI/Agere Corporation through the Law Offices of Covington and Burling, LLP. San Diego, CA – Case settled out of Court
- 7/2008 – 9/2010 Acted as an Expert Witness for the Defendants in the Samsung vs. AMD litigation representing Samsung. Worked with Covington and Burling Law Offices. Case settled out of Court.
- 5/2008-7/2009 Provided Analysis and Testimony as Expert Witness for Invalidity portion in ITC Court Case # 337-TA-648 as the Expert for the Defense of Multiple Corporations - Nanya, IDT, Jazz, Tower, Powerchip, Qimonda AG and Grace Semiconductor vs. LSI/Agere Corporation. The Court Hearing in Washington, D.C. on 7/20/2009 resulted in the defendants prevailing in this case, which involved the restriction of imported devices. The Agere/LSI patents '335 which was addressed in my opinions and testimony was found to be invalid in by the Judge and ITC 6 member board and no damages were ascribed to my clients. This case was

favorably resolved out of Court for the other defense litigants in this case (National, UMC, ProMOS, Dongbu, Micronas, Microchip, Elpida, Microchip, and others).

- 1/2008 – Settled . Acted as an Expert Witness in the case of SONY vs. Agere, where SONY was the defendant. Worked with the law firm of Kenyon and Kenyon, N.Y. representing SONY.
- 1/2007 – 11/2009. Acted as professional consultant (not Expert) for SMIC (ongoing) in Court action regarding SMIC vs. TSMC regarding trade secret issues. Case has not yet gone to Court. Working with law firm of Wilson, Sonsini, Goodrich and Rosatti in Palo Alto, CA representing SMIC.
- 8/2006 – 10/2007. Testimony as Expert Witness for ROHM Corporation in Arbitration hearing on nine Agere technology patents in ROHM vs. Agere Corporation, which was completed in October 2007 in San Francisco, CA. Worked with Fish Richardson of New York, the law firm representing ROHM. Outcome was favorable to ROHM.
- 1/2006 – 6/2007. Expert Witness consulting for SEL of Japan regarding two LCD related patent litigations with Toppoly vs. SEL which was resolved out of Court and Chi Mei vs. SEL which was resolved by Court ruling. Worked with Jenner and Block law firm in Chicago in representing SEL as plaintiff in both cases.
- 12/2005 – 7/2006. Participated as Expert Witness in litigation between AMD and Oki Electric regarding CVD W interconnect technology. Worked with Kellog, Huber, Hansen, Todd, Evans & Figel, P.L.L., Washington, D.C. representing Oki Electric, Corp. Settled out of Court.
- 6/2003 – 6/2006. Provided Analysis and Testimony as Expert Witness for Atmel Corporation in Court Case of Agere vs. Atmel Corporation held in Philadelphia, PA in March of 2005 in collaboration with the legal offices of Heller Ehrmann. Atmel prevailed in this case as the defendant, which involved over \$137 million dollars in potentially claimed damages by Agere. All four Agere patents, three of which were addressed in my opinions and testimony were found to be invalid in a jury trial and no damages were ascribed to Atmel. This case was resolved out of Court in June 2006
- 12/2005 – Provided Technical Consulting advice for White and Case, LLP in Palo Alto regarding sputtering gun technology.

1999-2003 Honeywell Electronic Materials Corporation
Sunnyvale, CA 94089

Position: Chief Technology Officer – Electronic Materials Division, Sunnyvale, CA

Responsibility as Chief Technical Officer was to construct a \$50M+ state-of-the-art Materials Technology Center for Interconnect Materials solutions. Organized a 80+ person research team to assemble a facility to develop and evaluate low k dielectric, PVD metallization and lithography products for deep submicron manufacturing technologies. Oversaw new packaging materials development centered around thermal management and high I/O count interconnect for BGA and high power applications. Established a strong IP based research group which averaged over 60 patent filings / year with approximately 20 US patents granted/year. Established a formal patent filing and review process to generate IP as a strategic and tactical resource to protect technical investments from

competitors and avoid early product commoditization. Spearheaded the technical aspects of global marketing effort for the organization and established guidelines for the disclosure of sensitive technical information to our customers. Responsible for hiring and establishing a world class technical staff with a diverse skill set which married new materials synthesis and development with integrated circuit process engineering. Generated industry-wide technical reviews related to new low k dielectric materials and transport phenomena in structures at submicron feature sizes. Participated in the International Interconnect Technology Conference Organizing Committee (IITC) to promote greater knowledge of the required interconnect technology for advanced circuit requirements.

1987-1999 National Semiconductor Corporation
Santa Clara, CA 95052

Position: Engineering Project Mgr./Sr. Member of Research Staff

Responsible for identifying and examining new R&D areas related to deep submicron interconnect technology. Performed extensive yield analyses associated with interconnect processing. Conducting studies on the integration of new low e dielectrics and refractory metal/ Al alloy conductor systems into production process flows. Used cost models to examine MCM technologies as a competitive cost effective alternative to monolithic VLSI devices. Mentoring Professors and students performing CVD metal deposition research at SUNY/Albany under the sponsorship of the Semiconductor Research Corporation (SRC) Program and yield programs at Carnegie-Mellon University. Member of Selection Committee for the establishment of MARCO through the SRC. Examined new interconnect alternatives to provide low noise generation and better signal integrity in VLSI circuits. Participated as an Industrial Advisory Board Member to the Deans of Engineering at San Jose State University and San Francisco State University. Co-Chair for the SIA National Roadmap Committee for Interconnect Technology representing National Semiconductor.

1983-1987: Fairchild Research Center, Fairchild Semiconductor
Corporation, Palo Alto, CA 94304

Position: Engineering Project Mgr. / Sr. Staff Engineer

Responsibilities involved material and process R&D for micron and submicron multilevel interconnect technologies. Areas of expertise involved the fabrication of barrier and interconnect metallizations, inorganic interlevel dielectrics and novel thin film conductor structures. Generated specifications for fine pitched 3 level metal for production in advanced bipolar and CMOS memory and logic.

1982-1983: Gate Array Division, Fairchild Semiconductor Corp.

Position: Sr. Staff Engineer

Developed spin-on glass dielectrics and metal lift-off processes for use in Gate Array devices.

1979-1982: Fairchild Research Center, Fairchild Semiconductor
Corporation, Palo Alto, CA 94304

Position: Member of Technical Staff

Basic Research performed on sputtered Pt and wide gamut of refractory metal silicides for device applications. Also performed a large number of studies on potential barrier layer materials such as nitrides, carbides and borides. Integrated TaSi₂/Poly Si films into 64K MOS memories. Performed electromigration studies on a wide range of Al alloys.

Educational Background

1. 1973-1980 MSE and PhD. In Materials Science and Engineering

Stanford University, Stanford, California

Ph.D. Thesis: A Study of CO Chemisorption on Mica Supported Microsurfaces of Pd and Ni Using the Thermal Desorption Spectroscopy / Transmission Electron Microscopy / Transmission Electron Microscopy Technique.

Advisor: Professor Guy Marshall Pound

2. 1969-1973 BSE In Chemical Engineering and BSE In Metallurgical Engineering (Double Major).

University of Michigan, Ann Arbor, Michigan

Advisor: Professor Richard Flinn

Journal Publications

1. M.E. Thomas, J.T. Dickinson, H. Poppa and G.M. Pound, "Chemisorption of CO on Pd Particles Supported on Mica", J. Vac. Sci. Technol. 15(2) (1978) 475.
2. M.E. Thomas, H. Poppa and G.M. Pound, " The Study of Microsurfaces" Using Thermal Desorption Spectroscopy", Thin Solid Films, 58 (1979) 273.
3. J.M. Pierce and M.E. Thomas, " Electromigration in Aluminum Conductors which are Chains of Single Crystal Grains", Appl.Phys. Lett, 39(2) (1981) 165.
4. R.R. Razouk, M.E. Thomas, "Oxidation of TaSi₂/Polycrystalline Silicon Structures in Dry Oxygen", J. Appl. Physics, 53(7) (1982) 5342.
5. J.M. De Blasi, R.R. Razouk and M.E. Thomas, " Characteristics of TaSi₂ / Poly Si Films in steam for VLSI Applications", J. Electrochem. Soc., 130(12), (1983), 2478.
6. R. Beyers, R. Sinclair and M.E. Thomas, " The Effect of Oxygen in Cosputtered Ti and Si Films ", Mat. Res. Symp. Proc. 14(1983) 423.
7. R. Beyers, R. Sinclair and M.E. Thomas, " Phase Equilibria in Thin Film Metallizations", Jour. Vac. Sci. Technol. B2(4), (1984) pp. 781-784.
8. R. Beyers, R. Sinclair and M.E. Thomas, " Ternary Reactions Between Integrated Circuit Materials", Proc. of Electrochem. Soc., Fall Meeting, Las Vegas, (1986), pp. 1-3.
9. R. Beyers, M.E. Thomas and R. Sinclair, "TEM studies of cosputtered titanium silicide (TiSi₂) films containing excess silicon", Materials Research Society Symposium Proceedings , 25 (Thin Films Interfaces 2) (1984), pp. 601-605.
10. M.E. Thomas, T.K. Keyser, and E.K.W. Goo, "Interfacial CuAl₂ Precipitate Nucleation and Growth During the Deposition of Al-4%Cu-1.5%Si Alloys", J. Appl. Phys. 59(11) (1986) pp. 3768 - 3773.
11. A.K. Kapoor, M.E. Thomas, and M.B. Vora, " A Low Barrier Schottky Process Using MoSi₂", IEEE Trans. Electron Dev. , ED-33, No.6, June (1986)., pp. 772-778.
12. W. Maly, M.E. Thomas, J.D. Chinn and D.M. Campbell, " Double Bridge Test Structure for the Evaluation of Type, Size and Density of Spot Defects", Carnegie Mellon Report # CMUCAD-87-2, February (1987).

13. J. A. Doi, M.E. Thomas, W. Maly, "Detection and physical characterization of spot defects in metal IC interconnections.", Electrochemical Society (1988), 88-13 (Proc. Symp. Autom. Integr. Circuits Manuf., 3rd, (1987), pp. 119-35.
14. W. Maly, M.E. Thomas, J.D. Chinn and D.M. Campbell, " Double Bridge Test Structure for the Evaluation of Type, Size and Density of Spot Defects", Published in the "International Workshop on Designing for Yield, Oxford, England, July (1987). Also Published in "Yield Modelling and Defect Tolerance", Editor W. Moore et al, Adam Hilger Publ., Bristol, 1988.
15. M.E. Thomas and W. Maly, " Multilevel Interconnect Yield Estimates Using the Double Bridge Test Structure", V-MIC Conf., (1988) 229.
16. M.E. Thomas, M.P. Hartnett, J.E. McKay, A.K. Kapoor and J.D. Chinn , "The Potential of Using Refractory Metals and Barrier Layers to Generate High Temperature Interconnects", V-MIC Conf., (1988) 183.
17. A.K. Kapoor, M.E. Thomas, J.F. Ciacchella and M.P. Hartnett, " Tantalum Nitride - p - Si High Voltage Schottky Diodes", IEEE Trans. on Electron Dev., Vol. 35(8) (1988) pp. 1372 -1377.
18. M.E. Thomas, M.P. Hartnett and J.E. McKay, " The Use of Surface Profilometers for the Measurement of Wafer Curvature ", J. Vac. Sci. Technol., A 6(4) (1988) 2570.
19. W. Maly, R.A. Hughes, M.E. Thomas and D.M. Campbell, " Methodology for Multilevel Interconnect Yield Prediction" 1989 Sympos. on VLSI Circuits, Kyoto, Japan.
20. M.P. Brassington, M. El-Diwany, R.R. Razouk, M.E. Thomas and P.T. Tuntasood, "An Advanced Single-Level Polysilicon Submicrometer BiCMOS Technology", IEEE Trans. on Electron Dev., Vol. 36(4) (1989) pp. 712.- 719.
21. P. Renteln, M.E. Thomas and J.M. Pierce, "Characterization of Mechanical Planarization Processes", V-MIC Conf. (1990) 57.
22. M.E. Thomas, S. Sekigahama and S.A. Myers, "Issues Associated with the Use of Electroless Cu Films for Submicron Multilevel Interconnections", V-MIC Conf. (1990) 335.
23. M.E. Thomas, S. Sekigahama, P. Renteln and J.M. Pierce , " The Mechanical Planarization of Interlevel Dielectrics for Multilevel Interconnect Applications", V-MIC Conf. (1990) 438.
24. M.E. Thomas, I.A. Saadat and S. Sekigahama, "VLSI Multilevel Micro-Coaxial Interconnects for High Speed Devices", IEDM Dec. (1990) 3.5.1.
25. J. Khare, B. Daniels, D. Campbell, M.E. Thomas and W. Maly, " Extraction of Defect Characteristics for Yield Estimation Using the Double Bridge Test Structure", Intern. Sympos. on VLSI Tech, Systems, and Applications, Taipei, Taiwan, May (1991) 424.
26. I.A. Saadat and M.E. Thomas, "VLSI Interconnect Options for On-Chip High Performance Applications", Wescon, Nov. (1991) 318.
27. M.E. Thomas, I.A. Saadat and S. Sekigahama, " Multilevel Microcoaxial Interconnect for Microwave Applications", GOMAC (1991) 609.
28. M.E. Thomas, S. Sekigahama, P. Renteln and J.M. Pierce , " Mechanical Planarization Process Characterization," Invited Paper, 1990 Semicon Japan Technical Session Proc., Chiba, Japan, Dec. (1991) 295.
29. F.A. Sherrima, I.A. Saadat, S. Sekigahama, A. Abdo, J. O'Brien and M.E. Thomas, " Manufacturing Studies of BCB as the Interlevel Dielectric Material for Multilevel Interconnect and VLSI Applications" ISHM, San Francisco, Oct (1992) pp. 596-600.
30. W. J. Dressick, C. S. Dulcey, J. M. Calvert, J. H. Georger, G. S. Calabrese, M. E. Thomas, H. A. Stever, "Selective Electroless Metalization of Patterned Ligand Surfaces", , Materials Research Society Symposium Proceedings (1992), 260 (Advanced Metallization and Processing for Semiconductor Devices and Circuits-II), pp. 659-64
31. A.E. Gattiker, W. Maly and M.E. Thomas, " Are There Any Alternatives to Known Good Die?" , MultiChip Module Conference, Santa Cruz, (1994) 102.
32. M.E. Thomas, " Manufacturing Considerations for VLSI Interconnect Systems", Materials

- Research Society Symposium Proceedings 337 (1994), - (Advanced Metallization for Devices and Circuits: Science, Technology and Manufacturability), pp. 13-24.
33. M.E. Thomas, "Manufacturing Considerations for VLSI interconnect systems", Overview paper. Materials Chemistry and Physics (1995), 41(3), pp.167-72.
 34. W.Maly, D.B.I. Feltham, A.E. Gattiker, M.D. Hobaugh, K. Backus and M.E. Thomas, "Smart-Substrate Multichip Module Systems", IEEE Design and Test, 1994, pp. 63-74.
 35. K. Gadepally, S. Geha, E. Myers and M.E. Thomas, " Electromigration Properties and correlation to the Physical Characteristics of Multilevel Metallizations", MRS Symposium Proceedings - Spring Meeting, 338 (1994) pp.301-306.
 36. Q.T. Jiang, M.E. Thomas, G. Bersuker, B. Foran, R. Mikkola, B. Carpenter and J. Ormando, "Electroplated Cu Recrystallization in Damascene Structures at Elevated Temperatures", Materials Research Society Symposium Proceedings (1999), 564(Advanced Interconnects and Contacts), pp. 429-434.
 37. J.A. Babcock, P. Francis, R. Bashir, A. E. Kabir, D.K. Schroder, M.S.L. Lee, T. Dhayagude, W. Yindeepol, S.J. Prasad, A. Kalnitsky, A.; Thomas, M. E.; Haggag, H.; Egan, K.; Bergemont, A.; Jansen, P. , "Precision Electrical Trimming of Very Low TCR poly-SiGe Resistors", IEEE Electron Device Letters (2000), 21(6), pp.283-285.
 38. Q.T. Jiang and M.E. Thomas, "Recrystallization Effects in Cu Electrodeposits Used in Fine Line Damascene Structures" J. Vac. Sci and Technology, : Microelectronic and Nanometer Structures (2001), pp. 762-766.
 39. M.E. Thomas, "Spin-on stacked films for low-keff dielectrics", Solid State Technology (2001), v. 44(7), pp. 105-113.
 40. M.E. Thomas, D.M. Smith, S. Wallace, N. Iwamoto, "Transport considerations in porous low k and metal interconnect systems approaching atomic dimensions", Proceedings of the IEEE International Interconnect Conference (IITC), June 3-5, 2002 (2002), pp. 223-225.
 41. M.E. Thomas, D.M. Smith, S. Wallace, N. Iwamoto, "Transport phenomena in porous low-k dielectrics", Semiconductor International (2002), v. 25(6), pp. 105-112.

Book Publications

1. M.E. Thomas and R. H. Havemann: "Overview of Interconnect", in Yoshio Nishi and Robert Doering (ed): Handbook of Semiconductor Manufacturing Technologies, Chapter 10, Marcel Dekker, Inc., New York, 2000

Special Conference Presentations

1. M.E. Thomas, H. Poppa and G.M. Pound, " The Study of Microsurfaces" Using Thermal Desorption Spectroscopy", Presented at the 4th Intern. Congress on Thin Films, Loughborough, Gt. Britain, Sept 11-15th, 1978.
2. M.E. Thomas, "Metallization Processes for Submicron VLSI", Invited Talk, IEEE Electron Device Society Mtg., May 17, 1988, Santa Clara, Ca.
3. M.E. Thomas, S. Sekigahama, P. Renteln and J.M. Pierce , " Mechanical Planarization Process Characterization," Invited Talk, 1990 Semicon Japan Technical Session Proc., Chiba, Japan, Dec. (1991) 295.
4. M.E. Thomas, " Issues Associated with High Temperature Interconnections", Transactions of the First Internatl. High Temp. Electronics Conf., Albuquerque, NM., (1991) 116.
5. M.E. Thomas, I.A. Saadat and S. Sekigahama, " The Use of Conformal Dielectrics and Metals in the Formation of Coaxial VLSI Interconnects", Invited Talk at the 1992 Schumacher CVD

Symposium.

6. M.E. Thomas, "Architectural and Materials Considerations for VLSI Interconnect Systems", SRC Copper Workshop, RPI, August 16th, (1993).
7. M.E. Thomas, "Architectural and Materials Considerations for VLSI Interconnect Systems", SEMI Workshop, RPI, Feb 23, (1994).
8. Schumacher Symposium, Invited Interconnect Talk, Feb. 6, 1995, Cornado Hotel. San Diego CA.
9. M.E. Thomas, " IC Scaling Trends, Challenges, & Potential Solutions through 2016", Hot Chips – A Symposium on High Performance Chips, IEEE Computer Society, Stanford Workshop on Interconnect, Invited talk , Aug. 18th-20th, 2002.

Conference Symposia Organized / Chaired / Professional Support Activities

1. Organized and Chaired Session on High Temperature Materials Chemistry., 172nd Meeting of the ECS (Fall), October 18 -23 , 1987.
2. Chair for VLSI Multilevel Interconnection Planarization Processes, VMIC Conf. (1988).
3. Organizing Committee for the Annual Electronic Materials Symposium (EMS) held in Santa Clara from 1990 to 1992.
4. Expert Working Group member in the establishment of MARCO Interconnect Focus Center for the SRC (1997).
5. Founding member for the establishment of the International Interconnect Technology Conference, Participated as Conference Treasurer of the Organization from 1998 through 2002.

U.S. Patents

1. T.K. Keyser, M.E. Thomas, J.M. Pierce and J.M. Cleaves, " Impregnation of Aluminum Interconnects with Copper", U.S. Patent 4,489,482. Granted on December 25, 1984.
2. M.E. Thomas, M.B. Vora and A.K. Kapoor, " Method and Structure for Inhibiting Dopant Outdiffusion", U.S. Patent 4,640,004. Granted February 3, 1987.
3. M.E. Thomas and R.L. Brown, " Process for Forming Vias on an Integrated Circuit", U.S. Patent 4,670,091, Granted June 2, 1987.
4. M.E. Thomas, M.B. Vora and A.K. Kapoor, " Structure for Inhibiting Dopant Out-Diffusion", U.S. Patent 4,829,363. Granted May 9, 1989.
5. W. Maly and M.E. Thomas, "Apparatus and Method for Detecting Spot Defects in Integrated Circuits", U.S. Patent 4,835,466. Granted May 30, 1989.
6. M.E. Thomas, " High Temperature Interconnect System for an Integrated Circuit", U.S. Patent 4,920,071. Granted April 24, 1990.
7. M.E. Thomas, " High Temperature Interconnect System for an Integrated Circuit", U.S. Patent 4,933,743. Granted June 12, 1990.
8. M.E. Thomas and J.D. Chinn, "Method of forming a High Performance Interconnect system for an Integrated Circuit", U.S. Patent 5,000,818, Granted March 19, 1991
9. W. Maly and M.E. Thomas, "Apparatus and Method for Detecting Vertically Propagated Defects in Integrated Circuits", U.S. Patent 5,051,690. Granted Sept. 24, 1991.
10. M.E. Thomas, " Ion Milling to Obtain Planarization", U.S. Patent 5,091,048. Granted Feb 25, 1992.
11. H. Hingarh, A. Ascunson, M.E. Thomas and R.L. Brown, "Thick Bus Metallization Interconnect Structure to Reduce Bus Area", U.S. Patent 5,111,276. Granted May 5, 1992.
12. M.E. Thomas and K.V. Anand, " High Value Tantalum Oxide Capacitor" U.S. Patent 5,111,355.

Granted May 5, 1992.

13. M.E. Thomas and J.D. Chinn, "High Performance Interconnect System for an Integrated Circuit", U.S. Patent 5,117,276. Granted May 26, 1992.
14. M.E. Thomas, "Optical Interconnects", U.S. Patent 5,123,078. Granted June 16, 1992.
15. M.E. Thomas, E. van de Van, E.K. Broadbent, "Gas-Based Backside Protection During Substrate Processing", U.S. Patent 5,133,284. Granted July 28, 1992.
16. M.E. Thomas and K.V. Anand, "Integrated Circuit Electronic Grid Device and Method", U.S. Patent 5,150,019. Granted Sept. 22, 1992.
17. M.E. Thomas, S. Sekigahama and R. von Salsa Brown, "Wafer Carrier", U.S. Patent 5,195,729. Granted March 23, 1993.
18. M.E. Thomas, "Polishing Pad for Planarization", U.S. Patent 5,197,999. Granted March 30, 1993.
19. M.E. Thomas, "Method of Fabricating an Optical Interconnect Structure", U.S. Patent 5,198,008, Granted March 30, 1993.
20. M.E. Thomas, "Optical Interconnects", U.S. Patent 5,235,663. Granted August 10, 1993.
21. M.E. Thomas, "Method of Bonding Semiconductor Chips to a Substrate", U.S. Patent 5,249,732. Granted Oct. 5, 1993.
22. M.E. Thomas, "Gas Distribution Head for Plasma Deposition and Etch Systems", U.S. Patent 5,266,153. Granted Nov. 30, 1993.
23. M.E. Thomas and I.A. Saadat, "Process for Making Microcomponent Integrated Circuits", U.S. Patent 5,279,988, Granted Jan 18, 1994.
24. M.E. Thomas, "Apparatus and Method for High Accuracy Alignment", U.S. Patent 5,317,141, May, 31, 1994.
25. M.E. Thomas, "Method of Making Electrostatic Switches for Integrated Circuits", U.S. Patent 5,410,799, Granted May 2, 1995.
26. M.E. Thomas, "High Temperature Interconnect System for an Integrated Circuit", U.S. Patent 5,414,301, Granted May 9, 1995.
27. M.E. Thomas and I.A. Saadat, "Method for Making an Integrated Microwave Interconnect and Components", U.S. Patent 5,453,154, Granted Sept. 26, 1995.
28. M.E. Thomas and K.V. Anand, "Integrated Circuit Vertical Electronic Grid Device and Method", U.S. Patent 5,572,042, Granted Nov. 6, 1996.
29. M.E. Thomas, "Curing Hydrogen Silsequioxane Resin with an Electron Beam", U.S. Patent 5,609,925, Granted Mar. 11, 1997.
30. M.E. Thomas, E. van de Van, E.K. Broadbent, "Method for Preventing Substrate Backside Deposition during a Chemical Vapor Deposition Operation", U.S. Patent 5,679,405, Granted October 21, 1997.
31. M.E. Thomas, R. P. Kovacs and E. Yoon, "Method of Providing a Dielectric Structure for Semiconductor Devices", U.S. Patent 5,688,724, Granted Nov. 18, 1997.
32. M.E. Thomas and K.V. Anand, "Method of Making an Integrated Circuit Vertical Electronic Grid Device", U.S. Patent 5,713,774. Granted Feb. 3, 1998.
33. M.E. Thomas and I.A. Saadat, "Integrated Circuit Magnetic Memory Element Having a Magnetizable Member and at Least Two Conductive Windings", U.S. Patent 5,748,523, Granted May 5, 1998.
34. M.E. Thomas, "Method of Performing Charged Particle Lithography", U.S. Patent 5,783,363, Granted Jul, 21, 1998.
35. M.E. Thomas, "Programmable Anti-fuses Using Laser Writing", U.S. Patent 5,904,507, Granted May 18, 1999.
36. M.E. Thomas and B. Daniels, "A Method for Silicide Stringer Removal in the Fabrication of Semiconductor Integrated Circuits", U.S. Patent 6,004,878, Granted Dec. 21, 1999.

37. M.E. Thomas, "High Efficiency Semiconductor Coating Apparatus and Method", U.S. Patent 6,017,585 , Granted Jan. 25, 2000.
38. M.E. Thomas, " Box Isolation Technique for Integrated Circuit Structures", U.S. Patent 6,074,929, Granted Jun 13, 2000.
39. M.E. Thomas, "Method for Solid State Formation of Diamond", U.S. Patent 6,099,639, Granted Aug. 8th, 2000.
40. V. Kitch and M.E. Thomas, "Self Aligned Interconnect Using High selectivity Metal Pillars and a Via Exclusion Mask", U.S. Patent 6,103,629, Granted Aug. 15, 2000.
41. M.E. Thomas and B. Daniels, "Semiconductor Device with Self Aligned Contacts Having Integrated Silicide Stringer Removal and Method Thereof", U.S. Patent 6,242,354, Granted Jun 5, 2001.
42. V. Kitch and M.E. Thomas, "Method for Decreasing the Contact Resistance of an Electrode Positioned in a Misaligned Via for Multilevel Interconnects", U.S. Patent 6,277,726, Granted Aug. 21, 2001.
43. M.E. Thomas and J.Shu, "Dielectric Gap Fill Process That Effectively Reduces Capacitance Between Narrow Metal Lines using HDP-CVD", U.S. Patent 6,348,421, Granted Feb. 19, 2002.
44. M.E. Thomas, P. Sethna and J. Shu, "Method of Using Organic Material to Enhance STI Planarization or Other Planarizing Processes", U.S. Patent 6,383,933, Granted May 7, 2002.
45. M.E. Thomas, "Thermal Oxidation Method Utilizing Atomic Oxygen to Reduce Dangling Bonds in Silicon Dioxide Grown on Silicon", U.S. Patent 6,509,283, Granted Jan 21, 2003.
46. M.E. Thomas. J. Perry, R. Razouk, R. Sabsowitz and A. Simmons, "Method of Preparing Light Sensitive Integrated Circuits for Packaging", U.S. Patent 6,548,323, Granted April 15, 2003.
47. M.E. Thomas, "Semiconductor Device with Sidewall Spacers Having Minimized Area Contacts", U.S. Patent 6,590,265, Granted July 8, 2003.
48. J. Shu and M.E. Thomas, "Dielectric Gap Fill Process that Effectively Reduces Capacitance Between Narrow Metal Lines Using HDP-CVD", U.S. Patent 6,593,615, Granted July 15, 2003
49. N. Hacker, M.E. Thomas and J.Drage, " Method to Restore Hydrophobicity in Dielectric Films and Materials", U.S. Patent 7,029,826, Granted April 18, 2006.
50. N. Hacker, M.E. Thomas and J.Drage, " Method to Restore Hydrophobicity in Dielectric Films and Materials", U.S. Patent 7,858,294, Granted. December 28.2010.
51. Wenya. Fan, Victor Liu, Michael Thomas, Brian Daniels, Tiffany Nguyen, De-Ling Zhou, Ananth Naman, Lei Jin and Anil Bhanap, "Repair and Restoration of Damaged Dielectric Materials and Films", U.S. Patent 7,915,181, Granted. March 29,2011
52. N. Hacker, M.E. Thomas and J.Drage, "Method to restore hydrophobicity in dielectric films and materials", U.S Patent 8,440,388, Granted May 14, 2013.
53. B. Daniels, E.H.Lee, M.E. Thomas, S.P. Turner, "Low Temperature Salicide forming materials and Sputtering Targets formed therefrom", World Patent Organization WO2004032184 A3, Granted June 24, 2004.
54. E.H.Lee and M.E. Thomas, "Thin films, structures having thin films, and methods of forming thin films, World Patent Organization WO 2003063243 A8, Granted December 4, 2003.

At present, Dr. Thomas has approximately 3 patents applications pending with the USPTO /WPO that are under review.

	<u>US PUB. APP. NO.</u>	<u>Title</u>
1	20030052000	Fine grain size material, sputtering target, methods of forming, and micro-arc reduction method
2	20040123920	Homogenous solid solution alloys for sputter-deposited thin films
3	20040137153	Layered stacks and methods of production thereof

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