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Atty. Dkt. No. 5298-02501 PM98019C Inventor(s):

> Anantha R. Sethuraman Christopher A. Seams

Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT



UTILITY PATENT APPLICATION TRANSMITTAL

(For new non-provisional applications under 37 CFR § 1.53(b))

This is a Continuation Application of prior application no. 09/143,723 filed August 31, 1998 and assigned to Cypress Semiconductor, recorded at Reel 9435, Frame 0506.

Enclosed are the following items:

- 1. A fee authorization for the amount of \$710.00.
- 2. Request & Certification under 35 U.S.C. 122(b)(2)(B)(i).
- 3. Specification as originally submitted including informal drawings.
- Formal drawings of Figs. 1 8 on 3 sheets.
- Copy of Declaration/Power of Attorney from prior application (see 37 CFR 1.63(d)).
- 6. Copy of Assignment papers from prior application.
- 7. Information Disclosure Statement w/form PTO-1449.
- 8. Return receipt postcard(s).

Please amend the specification by inserting before the first line the sentence: -This is a continuation application from prior application no. 09/143,723, filed August 31, 1998.

E.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: <u>February 7, 2001</u>

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Atty. Dkt. No. 5298-02501 PM98019C	§ 8
Inventor(s): Anantha R. Sethuraman Christopher A. Seams	S S CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10 "Express Mail" mailing label no. <u>EL726370210US</u> Date of Deposit: <u>February 7, 2001</u>
Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT	 I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to: Assistant, Commissioner for Patents, Box Patent Application, Washington, DC 20231. Derrick Brown

FEE AUTHORIZATION

Assistant Commissioner for Patents Washington, D.C. 20231

The Commissioner is hereby authorized to charge the following fee to Conley, Rose & Tayon, P.C. deposit account no. 50-1505/5298-02501^{*}.

Item:Filing feeAmount:\$710.00Atty. Dkt. No.5298-02501

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

^{*} If the above listed account is found to have insufficient funds, the Commissioner is authorized to charge Conley, Rose & Tayon, P.C. deposit account no. 50-1623/5298-02501.

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Approved for use through 10/31/2002. OMB 0651-0031

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CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. §1.10 "Express Mail" mailing label number: EL726370210US DATE OF DEPOSIT: February 7, 2001		REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to		Oocket Number:	5298-02501	
		lamed Inventor:	Anantha R. Sethuraman et al.	
Assistant Commissioner for Patents Box Patent Application Washington, DC 20231 Derrick Brown	Title:	INTERCONN	D SEMICONDUCTOR ECT TOPOGRAPHY AND METHOD ING A METAL LAYER TO FORM ECT	

I hereby certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

February 7, 2001 Date

Kevin L. Daffer, Reg. No. 34,146

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the annount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents. Washington, DC 20231.

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Inventor(s):	ş
Anantha R. Sethuraman	ş
Christopher A. Seams	§
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Title: PLANARIZED SEMICONDUCTOR	§
INTERCONNECT TOPOGRAPHY	ş
AND METHOD FOR POLISHING	§
A METAL LAYER TO FORM	ş
INTERCONNECT	§
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with the Un Office to A the date inc Commission	ertify that this paper or fee is being deposited nited States Postal Service "Express Mail Post Addressee" service under 37 C.F.R. §1.10 on dicated above and is addressed to: Assistant, oner for Patents, Box Patent Application, n, DC 20231.

PRELIMINARY AMENDMENT

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Commissioner for Patents Washington, D.C. 20231

Dear Sir/Madam:

The captioned application is a continuation application pursuant to 37 C.F.R. § 1.53(b) from prior application 09/143,723 filed August 31, 1998. Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

Please amend the specification as follows. A "marked-up" version of these amendments is included in Attachment A.

Please replace the paragraph on pg. 4, line 13 - pg. 5, line 3 with the following:

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results

from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem when forming a relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

Please replace the paragraph on pg. 5, line 19 - pg. 6, line 4 with the following:

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs to be polished as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

Please replace the paragraph on pg. 13, line 15 - pg. 14, line 2 with the following:

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. The trenches may be formed by lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF4 plasma etch.

In the Claims:

Please amend claims 1, 9, and 17 to read as follows. A "marked-up" version of these amendments is included in Attachment A.

1. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said narrow and wide trenches, wherein said dummy conductors are electrically separate from of electrically conductive features of an ensuing integrated circuit.

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9. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said narrow and wide trenches, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims

21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

CONCLUSION

In the present Amendment, the Specification and claims 1, 9, and 17 have been amended; claims 21 and 22 have been added. Therefore, pending claims 1-22 are presented for consideration by the Examiner. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

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ATTACHMENT A

"Marked-up" amendments as follows:

In the Specification:

Page 4, line 25, after the phrase "when forming" please delete "an" and substitute therefor --a--.

Page 5, line 26, after the phrase "wide interconnect needs" please insert --to--.

Page 13, lines 23-24, after the phrase "from 0.5 micron to 50 micron" please delete the following text: [Gentlemen, are the dimensions and spacings listed here for the trenches correct?].

In the Claims:

1. (Amended) A method [for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said [dummy trenches and said wide and narrow] trenches with a conductive material;

polishing said conductive material to form dummy conductors [exclusively] in said dummy trenches and interconnect [exclusively] in said narrow and wide trenches, wherein said dummy conductors are electrically separate from [said plurality of] electrically conductive features [and co-planar with said interconnect] of an ensuing integrated circuit.

9. (Amended) A method [for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive [a] relatively narrow interconnect [feature] <u>features</u>;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors [bounded exclusively within], wherein said dummy [trenches] conductors are electrically separate from [said] electrically conductive features[, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features] of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography [elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit], comprising:

a plurality of laterally spaced dummy trenches [residing within] in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors [bounded exclusively within] <u>in</u> said dummy trenches and electrically separate from [said plurality of] electrically conductive features <u>below said</u> <u>dummy conductors</u>; and

[interconnect bounded exclusively within] <u>conductive lines in</u> said narrow and wide trenches, wherein [interconnect] upper surfaces <u>of said conductive lines</u> are substantially coplanar with dummy conductor upper surfaces.

21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

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A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

By:

Anantha R. Sethuraman Christopher A. Seams

Atty. Dkt. No.: 5298-02500

Kevin L. Daffer/MLH Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, TX 78767-0398 Ph: (512) 476-1400

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to integrated circuit manufacturing and, more particularly, to a substantially planarized interconnect topography and method for making spaced interconnect by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect structure and a series of relatively narrow interconnect structures.

10 2. Description of the Related Art

Fabrication of an integrated circuit involves numerous processing steps. After implant regions (e.g., source/drain regions) have been placed within a semiconductor substrate and gate areas defined upon the substrate, an interlevel dielectric is formed across the topography to isolate the gate areas and the implant regions from overlying conducting regions. Interconnect routing is then patterned across the interlevel dielectric and connected to the implant regions and/or the gate areas by ohmic contacts formed through the interlevel dielectric. Alternating levels of interlevel dielectric and interconnect may be placed across the semiconductor topography to form a multi-level integrated circuit.

As successive layers are deposited across previously patterned layers of an integrated circuit, elevational disparities develop across the surface of each layer. If left unattended, the elevational disparities in each level of an integrated circuit can lead to various problems. For example, when a dielectric, conductive, or semiconductive material is deposited over a

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topological surface having elevationally raised and recessed regions, step coverage problems may arise. Step coverage is defined as a measure of how well a film conforms over an

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underlying step and is expressed by the ratio of the minimum thickness of a film as it crosses a step to the nominal thickness of the film over horizontal regions. Also, stringers may arise from incomplete etching over severe steps. Furthermore, correctly patterning layers upon a topological surface containing fluctuations in elevation may be difficult using optical

5 lithography. The depth-of-focus of the lithography alignment system may vary depending upon whether the resist resides in an elevational "hill" or "valley" area. The presence of such elevational disparities therefore makes it difficult to print high resolution features.

Techniques involving chemical and mechanical abrasion (e.g., chemical-mechanical polishing) to planarize or remove the surface irregularities have grown in popularity. As shown 10 in FIG. 1, a typical chemical-mechanical polishing ("CMP") process involves placing a semiconductor wafer 12 face-down on a polishing pad 14 which lies on or is attached to a rotatable table or platen 16. A popular polishing pad medium comprises polyurethane or polyurethane-impregnated polyester felts. During the CMP process, polishing pad 14 and semiconductor wafer 12 may be rotated while a carrier 10 holding wafer 12 applies a downward 15 force F upon polishing pad 14. An abrasive, fluid-based chemical suspension, often referred to as a "slurry", is deposited from a conduit 18 positioned above pad 14 onto the surface of polishing pad 14. The slurry may fill the space between pad 14 and the surface of wafer 12. The polishing process may involve a chemical in the slurry reacting with the surface material being polished. The rotational movement of polishing pad 14 relative to wafer 12 causes abrasive 20 particles entrained within the slurry to physically strip the reacted surface material from wafer 12. The pad 14 itself may also physically remove some material from the surface of the wafer 12. The abrasive slurry particles are typically composed of silica, alumina, or ceria.

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CMP is commonly used to form a planarized level of an integrated circuit containing interconnect laterally spaced from each other in what is generally referred to as the "damascene"

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process. Laterally spaced trenches are first etched in an interlevel dielectric configured upon a semiconductor topography comprising electrically conductive features. A conductive material is then deposited into the trenches and on the interlevel dielectric between trenches to a level spaced above the upper surface of the interlevel dielectric. CMP is applied to the surface of the

5 conductive material to remove that surface to a level substantially commensurate with that of the upper surface of the interlevel dielectric. In this manner, interconnect that are isolated from each other by the interlevel dielectric are formed exclusively in the trenches. CMP can planarize only localized regions of the interconnect surface such that all interconnect traces have a co-planar upper surface, provided certain conditions are met. The localized area must contain trenches that are consistently, and closely spaced from each other. Moreover the trenches must be relatively narrow in lateral dimension. If those rather restrictive requirements are not met, then thicknesses of a given interconnect layer can vary to such a degree that local regions of interconnect may suffer severe current carrying limitations.

In particular, planarization may become quite difficult in a region where there is a relatively large distance between a series of relatively narrow interconnect, or if there is a relatively wide interconnect such as that found in, for example, a bond pad. FIGS. 2-4 illustrate a typical damascene process and the localized thinning or "dishing" problem experienced by conventional metal CMP processes.

As shown in FIG. 2, a series of relatively narrow trenches 22 and a relatively wide trench 24 are formed in an interlevel dielectric 20 using well-known lithography and etch techniques. The series of narrow trenches 22 and the wide trench 24 are laterally separated by a region of interlevel dielectric having a smooth upper surface 26. FIG. 3 illustrates a conductive material 28, e.g., a metal, such as Al, W, Ta, and Ti, deposited across the topography to a level spaced above upper surface 26. Due to the conformal nature of the sputter or CVD process used to

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apply the conductive material, the conductive material takes on an upper surface topography having a first region 30 formed over closely spaced hill and valley areas spaced above the surface of narrow trenches 22. The topography also includes a second region 32 having a single wide valley area spaced above the wide trench 24 and a substantially flat third region 34 spaced above

5 smooth upper surface 26. Conductive material 28 is then polished, as shown in FIG 4, using CMP to remove conductive material 28 from the upper surface of interlevel dielectric 20. As a result of CMP, a series of relatively narrow interconnect 36 are formed exclusively in narrow trenches 22 and a relatively wide interconnect 38 is formed exclusively in wide trench 24. The narrow interconnect 36 may serve to electrically connect underlying active devices and conductive elements of the semiconductor topography. The wide interconnect 38 may subsequently function as, e.g., a bond pad.

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem

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when forming an relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions

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of the CMP pad, the metal is not, and thus allows significant flexing of the pad. Such flexing of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

In addition, the topological surface includes a recessed area 40 arranged over the set of narrow interconnect 36. It is believed that such a recessed area 40 forms due to so-called "oxide erosion" of interlevel dielectric 20, assuming that the dielectric is composed of silicon oxide. The CMP slurry chosen to polish the metal of the interconnect includes a chemical component that reacts with metal at a faster rate than with oxide. As such, even after the metal surface has
been removed to a level commensurate with that of the oxide surface, its removal may continue at a faster rate than that of the oxide. The metal surface thus becomes spaced below that of the oxide, creating steps in the topological surface. At this point, the relatively small, elevated oxide regions are removed by the CMP pad at a faster rate than large area oxide regions, or even the adjacent, recessed metal regions. Because the oxide outside the area comprising the densely
packed interconnect has no elevational disparity, its removal rate is relatively slow. Therefore, the oxide in the dense interconnect area becomes recessed below the oxide outside the dense interconnect area.

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base

25 perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs be polished

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as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

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SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by an embodiment of the present invention in which a substantially planar semiconductor topography is formed by placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide 5 interconnect and another region defined by a series of relatively narrow interconnect. A plurality of electrically conductive features are embodied within the topography. The dielectric layer may be placed between an interconnect level and an underlying semiconductor substrate upon and within which active devices have been formed. Alternatively, the dielectric layer may be placed between successive interconnect levels. The dielectric layer may comprise a material having a relatively low dielectric constant, e.g. glass- or silicate-based dielectric, preferably oxide.

According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria. The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively. The depth of the wide, dummy, and narrow trenches is preferably 2,000 Å to 1 micron. The dummy trenches, the wide trench, and the narrow trenches are filled with a conductive material, e.g., a metal, such as aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner,

dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy

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trenches, and interconnect are formed exclusively in the narrow and wide trenches. The dummy conductors are electrically separate from electrically conductive features of the ensuing integrated circuit. As such, the dummy conductors preferably serve no purpose except to improve the planarization of the interconnect level in which they reside. The dummy conductors

therefore do not contain transitory voltages and/or current associated with or connected to active 5 and passive devices within the semiconductor topography. Most likely, the dummy conductors are connected to a power supply or ground, but not to any gate inputs or source/drain outputs of a active transistors, nor are they connected to any terminals of passive resistors or capacitors.

10 In one embodiment, the conductive material may be polished using well-known CMP. That is, the frontside of the semiconductor topography may be forced against a CMP polishing pad while the polishing pad and the topography are rotated relative to each other. A CMP slurry entrained with abrasive particles, e.g., ceria, silica, or alumina, is dispensed upon the polishing pad surface to aid in the removal of the conductive material. In an alternate embodiment, a "fixed-abrasive" technique is used to polish the conductive material. The fixed-abrasive 15 technique involves placing a liquid which is substantially free of particulate matter between the surface of the conductive material and an abrasive polishing surface of a polishing pad. The liquid contains no chemical constituent that could react with the topography. The abrasive polishing surface is moved relative to the semiconductor topography so as to polish the 20 conductive material. The liquid applied to the polishing surface preferably comprises deionized

- water, however, other liquids which have a near-neutral pH value may alternatively be directed onto the abrasive polishing surface. The pH that is chosen for the polishing process is one suitable for the conductive material and the polishing pad. The polishing surface comprises a polymer-based matrix entrained with particles selected from the group consisting of cerium
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oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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The abrasive polishing surface belongs to a polishing pad which is substantially resistant to deformation even when placed across an elevationally recessed region of relatively large lateral dimension (e.g., over 200 microns lateral dimension). Therefore, the pad is relatively

5 non-conformal to the underlying surface and thus does not come in contact with elevationally recessed regions of the conductive material. It is believed that the particles dispersed throughout the abrasive polishing surface in combination with the polishing liquid interact chemically and physically with the elevated regions of the conductive material to remove those regions. However, the liquid alone may be incapable of removing the conductive material in elevationally recessed regions. As such, elevationally raised regions of the conductive material are removed at a substantially faster rate than elevationally recessed regions. The polish rate slows down significantly as the topological surface of the interconnect level approaches planarity.

Whatever polishing technique is applied to the conductive material, the presence of the
plurality of dummy conductors between the series of relatively narrow interconnect and the
relatively wide interconnect provides for global planarization of the topography employing the
trenches. In particular, the dummy conductors and the interposing dielectric protrusions replace
a relatively wide dielectric region absent of any conductive material. It is theorized that the
metal of the dummy conductors, being softer than the dielectric, contracts when a polishing pad
is forced against it. Consequently, the surface of the polishing pad extending over the dummy
conductors and the wide interconnect during polishing remains substantially flat when pressure is
applied thereto. That is, the surface area of the dielectric protrusions between the dummy
conductors is not sufficient to withstand the force of the polishing pad, and thus does not cause
the pad to flex. Therefore, dishing of the conductive material in the wide trench is less likely to

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Also, the dummy conductors help prevent surface disparity that could result from erosion of the dielectric layer. The conductive material may continue to be polished more rapidly than the dielectric once the surface of the conductive material has been removed to the same elevational plane as the dielectric. The dielectric protrusions between the dummy conductors and

- 5 the closely spaced narrow interconnect may thus become elevated above the conductive material. Consequently, the entire topological surface of the interconnect level has surface disparities, causing the polish rate of the elevated dielectric protrusions to become greater than that of the recessed dummy conductors and interconnect. As the polishing process continues, the dielectric protrusions are again made substantially coplanar with the dummy conductors and the
- 10 interconnect. This cycle may be repeated until it is desirable to stop the polishing process.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

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FIG. 1 depicts a side plan view of an apparatus that may be used to chemical-mechanical polish a semiconductor topography;

FIG. 2 depicts a partial cross-sectional view of a conventional semiconductor topography,
wherein a series of relatively narrow trenches are formed within an interlevel dielectric a spaced distance from a relatively wide trench;

FIG. 3 depicts a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the trenches to a level spaced above an upper surface of the interlevel dielectric;

FIG. 4 depicts a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed from the upper surface of the interlevel dielectric using a conventional CMP technique, thereby forming a topological surface having elevational disparities;

FIG. 5 depicts a partial cross-sectional view of a semiconductor topography according to an embodiment of the present invention, wherein a plurality of laterally spaced dummy trenches are formed in a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

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FIG. 6 is a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the dummy trenches, the narrow trenches, and the wide trench to a level spaced above the upper surface of the dielectric layer;

FIG. 7 is a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed to a level substantially commensurate with that of the upper surface of the dielectric layer using a planarization process according to an embodiment of the present invention, thereby forming a planarized topological surface; and

FIG. 8 is a process flow diagram of a fixed-abrasive polishing technique that may be used to polish the conductive material.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Turning to FIG. 5, a partial cross-section of a semiconductor topography is presented. Electrically conductive features may be embodied within the topography. A dielectric layer 50 is shown which may comprise a dielectric material having a relatively low dielectric constant. 5 Dielectric layer 50 may comprise, e.g., a glass- or silicate- based material, such as an oxide that has been deposited by chemical-vapor deposition ("CVD") from either a tetraethyl orthosilicate ("TEOS") source or a silane source and doped with an impurity, e.g., boron or phosphorus. Dielectric layer 50 may serve as a poly-metal interlevel dielectric ("PMD") between a doped polycrystalline silicon ("polysilicon") gate layer and an ensuing metal interconnect layer. It is to be understood that the gate layer may comprise other conductive materials besides polysilicon. Alternatively, dielectric 50 may form an inter-metal interlevel dielectric ("IMD") between an underlying metal interconnect layer and an ensuing overlying metal interconnect layer.

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. [Gentlemen, are the dimensions and spacings listed here for the trenches correct?] The trenches may be formed by

25 lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions

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of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

As shown in FIG. 6, a conductive material 58 may subsequently be deposited into the
trenches and across dielectric layer 50 to a level spaced above the uppermost horizontal surface of dielectric layer 50. Conductive material 58 may comprise a metal, e.g., aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. Such a metal may be sputter deposited from a metal target or MOCVD (i.e., metal organic CVD) deposited from a metal organic source. The as-deposited conductive material 58 has an elevationally disparate surface
that includes a first region 60 above narrow trenches 52, a second region 62 above dummy trenches 56, and a third region 64 above wide trench 54. The valley areas of regions 60, 62, and 64 are directly above respective trenches, while the hill areas are directly above respective dielectric protrusions that are positioned between the trenches.

Turning to Fig. 7, conductive material 58 may then be polished to a level substantially coplanar with the uppermost surface of dielectric layer 50. As a result of polishing conductive material 58, relatively narrow interconnect 66 are formed exclusively in trenches 52, dummy conductors 68 are formed in dummy trenches 56, and a relatively wide interconnect 72 is formed in trench 54. Dummy conductors 68 are laterally spaced from each other and/or from interconnect 66 and 72 by dummy dielectric protrusions 70. Placing dummy conductors 68 in the region between the series of narrow interconnect 66 and the wide interconnect 72 affords global planarization of the topological surface. That is, the polish rate is substantially uniform across the entire topological surface. Also, the polish rate of elevationally raised regions is

greater than that of elevationally recessed regions. Further, a surface having elevational disparity

is polished at a faster rate than a substantially flat surface.

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It is believed that the presence of dummy conductors 68 helps prevent the polishing pad from deforming about the length of the pad into relatively wide trench 54 when subjected to normal pressure. Further, it is postulated that placing dummy conductors 68 between dummy dielectric protrusions 70 ensures that elevational fluctuations are present in different regions of the topological surface at the same time. That is, no particular region of the topological surface

5 the topological surface at the same time. That is, no particular region of the topological surface becomes substantially planarized before other regions and thereby causes fluctuations in the polish rate across the surface. Thus, the polish rate does not slow down until the entire topological surface is substantially free of elevational disparity.

Dummy conductors 68 are not connected to any active or passive device which forms an integrated circuit of the semiconductor topography shown in FIG. 7. While dummy conductors can carry power or ground voltages, they do not carry transitory voltages or current associated with an operable circuit. Nor are they associated or connected in any way with active circuit elements and/or features such as a contact, implant, gate, etc., of a transistor, capacitor, resistor, etc.

FIG. 8 illustrates a process flow diagram of a fixed abrasive CMP technique that may be used to polish conductive material 58, and thereby form the substantially planar topography shown in FIG. 7. Conductive material 58 may be polished using an apparatus similar in some respects to that shown in Fig. 1. The apparatus in Fig. 1 may be purposefully modified to accommodate an abrasive polishing surface and a conduit for delivering a particle-free solution to the polishing surface. Alternatively, a conventional CMP process may be employed for polishing conductive material 58. The CMP slurry may include a component that chemically reacts with conductive material 58.

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ц. Ц As described in block 72, a particle-free liquid is dispensed onto an abrasive polishing surface of a polishing pad having a substantially rigid supportive backing. An appropriate polishing pad is commercially available from Minnesota Mining and Manufacturing Company. The polishing surface comprises a polymer-based matrix entrained with abrasive particles. Appropriate materials that may be used for the particles include, but are not limited to, ceria, α alumina, γ alumina, silicon dioxide, titania, chromia, and zirconia. Preferably, the polishing liquid forwarded onto the abrasive polishing surface is deionized water. The polishing liquid may also be other types of liquids which have a near-neutral pH. As shown in block 74 of FIG. 8, the semiconductor topography depicted in FIG. 6 may be positioned face-down upon the polishing surface. The polishing liquid is positioned at the interface between the semiconductor topography and the abrasive polishing surface.

As indicated by block 76 of FIG. 8, the semiconductor topography and the abrasive polishing surface may be rotated relative to each other while the frontside of the topography is forced against the polishing surface. It is believed that contact between the high elevation regions of conductive material 58 and the abrasive particles as well as the polishing liquid causes the surface material of conductive material 58 in those elevated regions to be released from bondage with the bulk of the conductive material. The particles extending from the abrasive polishing surface have a sufficient hardness to dislodge the reacted surface material during abrasion of the high elevation regions. The rigidness of the polishing pad may be sufficient to prevent the abrasive polishing surface from contacting recessed regions of conductive material 58. Accordingly, very little of the conductive material 58 in the recessed regions is removed.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method for forming a substantially planar semiconductor topography by placing a plurality of dummy conductors in a dielectric layer laterally between a

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relatively wide interconnect and a series of relatively narrow interconnect. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, electrically conductive features isolated from each other by a dielectric may subsequently be formed upon the planarized semiconductor

5 topography. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.



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WHAT IS CLAIMED IS:

1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

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etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said dummy trenches and said wide and narrow trenches with a conductive material;

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said narrow and wide trenches, wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

2. The method of claim 1, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

35 7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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9. A method for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive a relatively narrow interconnect feature;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors bounded exclusively within said dummy trenches electrically separate from said electrically conductive features, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features.

10. The method of claim 9, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

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14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

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15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

10 17. A substantially planar semiconductor topography elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit, comprising:

a plurality of laterally spaced dummy trenches residing within a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors bounded exclusively within said dummy trenches and electrically separate from said plurality of electrically conductive features; and

interconnect bounded exclusively within said narrow and wide trenches, wherein interconnect upper surfaces are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

The substantially planar semiconductor topography of claim 17, wherein said dummy
 conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten,
 molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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ABSTRACT OF THE DISCLOSURE

The present invention advantageously provides a substantially planarized semiconductor 5 topography and method for making the same by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect and a series of relatively narrow interconnect. According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The dummy trenches, the wide trench, and the narrow trenches are filled with a 10 conductive material, e.g., a metal. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner, dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy trenches, and interconnect are formed exclusively in the narrow and wide trenches. The topological surface of the resulting interconnect level is substantially void of surface disparity.

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT," the specification of which:

is attached hereto.
is attached hereto.
as Application Serial No.
and was amended on
(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

Prior Foreign Application No.	Country	Filing Date (mm/dd/yy)	Priority Claimed	Cert. copy Attached
N/A				
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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Provisional Application No. Filing Date (mm/dd/yy)

N/A

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Parent Application No.	Filing Date (mm/dd/yy)	Parent Patent No. (if applicable) or Status
N/A		

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The Assignee hereby revokes any previous Powers of Attorney and appoints Andrew D. Fortney, Reg. No. 34,600 of Cypress Semiconductor Corporation, and Kevin L. Daffer, Reg. No. 34,146; B. Noel Kivlin, Reg. No. 33,929; and, Eric B. Meyertons, Reg. No. 34,876 of the firm of Conley, Rose & Tayon, as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications to:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Phone: (512) 476-1400

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Full Name:	Anantha R. Sethuraman			
Inventor's Signature:	en	ent	Date: Angen	A 21, 1998
City and State (or Foreign Country) of F	Residence!	Fremont, CA	Citizenship:	India
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(Include numbe	r, street name, city, state	and zip code)	
Inventor's Full Name:	n An	Christopher A. Sear	ms	
Inventor's Signature:	MI	$\overline{}$	Date: 0/	21/98
City and State (or Foreign Country) of R	Residence:	Pleasanton, CA	Citizenship:	U.S.A.
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(r, street name, city, state		

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5 11-02500g UNITED STATES DEPARTMENT OF COMMERCE



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RECORDATION DATE: 08/31/1998

REEL/FRAME: 9435/0506 NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR: SETHURAMAN, ANANTHA R.

DOC DATE: 08/21/1998

ASSIGNOR: SEAMS, CHRISTOPHER A.

DOC DATE: 08/21/1998

ASSIGNEE: CYPRESS SEMICONDUCTOR CORP. 3901 N. 1ST STREET SAN JOSE, CALIFORNIA 95134

SERIAL NUMBER: 09143723 PATENT NUMBER: FILING DATE: 08/31/1998 ISSUE DATE:

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LAWAN FLETCHER, EXAMINER ASSIGNMENT DIVISION OFFICE OF PUBLIC RECORDS

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FORM PTO-1595 1-31-92 MAA 8-31-98	09-14-1998	U.S. DEPARTMENT OF COMMERC Patent and Trademark Offic Atty Dkt. 5298-02500
To the Honorable Commissioner of Patents and Trademi	100827846	opy thereof. d address of receiving party(ies):
 Name of conveying party(ies): ANANTHA R. SETHURAMAN CHRISTOPHER A. SEAMS 		Cypress Semiconductor Corp.
Additional name(s) of conveying party(ies) attached?	es No Street Addre	tes: 3901 N. 1st Street 600
	City <u>San</u> Additional n	Jose State CA ZIP 95134 name(s) & address(es) attached? Yes
Nature of Conveyance: Assignment Merger Security Agreement Change of Name Other		
A. Patent Application No.(s) B. Patent No.(s)	olication, the execution date of this app	lícation is: August 31, 1998
A	dditional numbers attached? 🔲 Yes	s 🖬 No
Name and address of party to whom correspondence concerning document should be mailed: ame: <u>Kevin L. Daffer</u>	6. Total nur	nber of applications and patents involved: 1
ternal Address: <u>Conley, Rose & Tayon, P.C.</u> reet Address: <u>P.O. Box 398</u>		
ity <u>Austin</u> State <u>TX</u> ZIP <u>78767-039</u>	7. Total fee	(37 CFR 3.41):
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Statement and Signature.	1.1	
To the best of my knowledge and belief, the foregoing Kevin L. Daffer Name of Person Signing	information is for and dereft and any	v attached copy is a true copy of the original document. August 31, 1998 Date

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ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned, does hereby:

SELL, ASSIGN AND TRANSFER to <u>CYPRESS SEMICONDUCTOR</u> <u>CORPORATION</u> (the "Assignee"), having a place of business at <u>3939 North First Street</u>, <u>San Jose, CA, 95134</u> the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith, and is entitled <u>"A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM</u> <u>INTERCONNECT</u>", such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee; and

COVENANT AND AGREE that the above is and will be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

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TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

FURTHER COVENANT that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

167-21,1998 Date: H (Signature) Anantha R. Sethuraman 8 21 98 Date: (Signature) Christopher/ ams

Please direct all communication as follows:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Ph: (512) 476-1400

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Atty. Dkt. No. 5298-02501 PM98019C Inventor(s):

> Anantha R. Sethuraman Christopher A. Seams

Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT



UTILITY PATENT APPLICATION TRANSMITTAL

(For new non-provisional applications under 37 CFR § 1.53(b))

This is a Continuation Application of prior application no. 09/143,723 filed August 31, 1998 and assigned to Cypress Semiconductor, recorded at Reel 9435, Frame 0506.

Enclosed are the following items:

- 1. A fee authorization for the amount of \$710.00.
- 2. Request & Certification under 35 U.S.C. 122(b)(2)(B)(i).
- 3. Specification as originally submitted including informal drawings.
- Formal drawings of Figs. 1 8 on 3 sheets.
- Copy of Declaration/Power of Attorney from prior application (see 37 CFR 1.63(d)).
- 6. Copy of Assignment papers from prior application.
- 7. Information Disclosure Statement w/form PTO-1449.
- 8. Return receipt postcard(s).

Please amend the specification by inserting before the first line the sentence: -This is a continuation application from prior application no. 09/143,723, filed August 31, 1998.

E.

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Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: <u>February 7, 2001</u>

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No. 5298-02501 PM98019C	§ 8
Inventor(s): Anantha R. Sethuraman Christopher A. Seams	S S CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10 "Express Mail" mailing label no. <u>EL726370210US</u> Date of Deposit: <u>February 7, 2001</u>
Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT	 I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to: Assistant, Commissioner for Patents, Box Patent Application, Washington, DC 20231. Mathematication, Derrick Brown

FEE AUTHORIZATION

Assistant Commissioner for Patents Washington, D.C. 20231

The Commissioner is hereby authorized to charge the following fee to Conley, Rose & Tayon, P.C. deposit account no. 50-1505/5298-02501^{*}.

Item:Filing feeAmount:\$710.00Atty. Dkt. No.5298-02501

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

^{*} If the above listed account is found to have insufficient funds, the Commissioner is authorized to charge Conley, Rose & Tayon, P.C. deposit account no. 50-1623/5298-02501.

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	First Named Inventor:		Anantha R. Sethuraman et al.
Assistant Commissioner for Patents Box Patent Application Washington, DC 20231 Derrick Brown	Title:	INTERCONN	D SEMICONDUCTOR ECT TOPOGRAPHY AND METHOD ING A METAL LAYER TO FORM ECT

I hereby certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

February 7, 2001 Date

Kevin L. Daffer, Reg. No. 34,146

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the annount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents. Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Invent	cor(s):	§
	Anantha R. Sethuraman	ş
	Christopher A. Seams	§
		§
Title:	PLANARIZED SEMICONDUCTOR	ş
	INTERCONNECT TOPOGRAPHY	ş
	AND METHOD FOR POLISHING	§
	A METAL LAYER TO FORM	ş
	INTERCONNECT	ş
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PRELIMINARY AMENDMENT

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Commissioner for Patents Washington, D.C. 20231

Dear Sir/Madam:

The captioned application is a continuation application pursuant to 37 C.F.R. § 1.53(b) from prior application 09/143,723 filed August 31, 1998. Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

Please amend the specification as follows. A "marked-up" version of these amendments is included in Attachment A.

Please replace the paragraph on pg. 4, line 13 - pg. 5, line 3 with the following:

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results

from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem when forming a relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

Please replace the paragraph on pg. 5, line 19 - pg. 6, line 4 with the following:

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs to be polished as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

Please replace the paragraph on pg. 13, line 15 - pg. 14, line 2 with the following:

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. The trenches may be formed by lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF₄ plasma etch.

In the Claims:

Please amend claims 1, 9, and 17 to read as follows. A "marked-up" version of these amendments is included in Attachment A.

1. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said narrow and wide trenches, wherein said dummy conductors are electrically separate from of electrically conductive features of an ensuing integrated circuit. 9. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said narrow and wide trenches, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims

21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

CONCLUSION

In the present Amendment, the Specification and claims 1, 9, and 17 have been amended; claims 21 and 22 have been added. Therefore, pending claims 1-22 are presented for consideration by the Examiner. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

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ATTACHMENT A

"Marked-up" amendments as follows:

In the Specification:

Page 4, line 25, after the phrase "when forming" please delete "an" and substitute therefor --a--.

Page 5, line 26, after the phrase "wide interconnect needs" please insert --to--.

Page 13, lines 23-24, after the phrase "from 0.5 micron to 50 micron" please delete the following text: [Gentlemen, are the dimensions and spacings listed here for the trenches correct?].

In the Claims:

1. (Amended) A method [for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said [dummy trenches and said wide and narrow] trenches with a conductive material;

polishing said conductive material to form dummy conductors [exclusively] in said dummy trenches and interconnect [exclusively] in said narrow and wide trenches, wherein said dummy conductors are electrically separate from [said plurality of] electrically conductive features [and co-planar with said interconnect] of an ensuing integrated circuit.

9. (Amended) A method [for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive [a] relatively narrow interconnect [feature] <u>features</u>;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors [bounded exclusively within], wherein said dummy [trenches] conductors are electrically separate from [said] electrically conductive features[, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features] of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography [elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit], comprising:

a plurality of laterally spaced dummy trenches [residing within] in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors [bounded exclusively within] <u>in</u> said dummy trenches and electrically separate from [said plurality of] electrically conductive features <u>below said</u> <u>dummy conductors</u>; and

[interconnect bounded exclusively within] <u>conductive lines in</u> said narrow and wide trenches, wherein [interconnect] upper surfaces <u>of said conductive lines</u> are substantially coplanar with dummy conductor upper surfaces.

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21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

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A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

By:

Anantha R. Sethuraman Christopher A. Seams

Atty. Dkt. No.: 5298-02500

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to integrated circuit manufacturing and, more particularly, to a substantially planarized interconnect topography and method for making spaced interconnect by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect structure and a series of relatively narrow interconnect structures.

10 2. Description of the Related Art

Fabrication of an integrated circuit involves numerous processing steps. After implant regions (e.g., source/drain regions) have been placed within a semiconductor substrate and gate areas defined upon the substrate, an interlevel dielectric is formed across the topography to isolate the gate areas and the implant regions from overlying conducting regions. Interconnect routing is then patterned across the interlevel dielectric and connected to the implant regions and/or the gate areas by ohmic contacts formed through the interlevel dielectric. Alternating levels of interlevel dielectric and interconnect may be placed across the semiconductor topography to form a multi-level integrated circuit.

As successive layers are deposited across previously patterned layers of an integrated circuit, elevational disparities develop across the surface of each layer. If left unattended, the elevational disparities in each level of an integrated circuit can lead to various problems. For example, when a dielectric, conductive, or semiconductive material is deposited over a

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topological surface having elevationally raised and recessed regions, step coverage problems may arise. Step coverage is defined as a measure of how well a film conforms over an

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underlying step and is expressed by the ratio of the minimum thickness of a film as it crosses a step to the nominal thickness of the film over horizontal regions. Also, stringers may arise from incomplete etching over severe steps. Furthermore, correctly patterning layers upon a topological surface containing fluctuations in elevation may be difficult using optical

5 lithography. The depth-of-focus of the lithography alignment system may vary depending upon whether the resist resides in an elevational "hill" or "valley" area. The presence of such elevational disparities therefore makes it difficult to print high resolution features.

Techniques involving chemical and mechanical abrasion (e.g., chemical-mechanical polishing) to planarize or remove the surface irregularities have grown in popularity. As shown 10 in FIG. 1, a typical chemical-mechanical polishing ("CMP") process involves placing a semiconductor wafer 12 face-down on a polishing pad 14 which lies on or is attached to a rotatable table or platen 16. A popular polishing pad medium comprises polyurethane or polyurethane-impregnated polyester felts. During the CMP process, polishing pad 14 and semiconductor wafer 12 may be rotated while a carrier 10 holding wafer 12 applies a downward 15 force F upon polishing pad 14. An abrasive, fluid-based chemical suspension, often referred to as a "slurry", is deposited from a conduit 18 positioned above pad 14 onto the surface of polishing pad 14. The slurry may fill the space between pad 14 and the surface of wafer 12. The polishing process may involve a chemical in the slurry reacting with the surface material being polished. The rotational movement of polishing pad 14 relative to wafer 12 causes abrasive 20 particles entrained within the slurry to physically strip the reacted surface material from wafer 12. The pad 14 itself may also physically remove some material from the surface of the wafer 12. The abrasive slurry particles are typically composed of silica, alumina, or ceria.

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CMP is commonly used to form a planarized level of an integrated circuit containing interconnect laterally spaced from each other in what is generally referred to as the "damascene"

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process. Laterally spaced trenches are first etched in an interlevel dielectric configured upon a semiconductor topography comprising electrically conductive features. A conductive material is then deposited into the trenches and on the interlevel dielectric between trenches to a level spaced above the upper surface of the interlevel dielectric. CMP is applied to the surface of the

5 conductive material to remove that surface to a level substantially commensurate with that of the upper surface of the interlevel dielectric. In this manner, interconnect that are isolated from each other by the interlevel dielectric are formed exclusively in the trenches. CMP can planarize only localized regions of the interconnect surface such that all interconnect traces have a co-planar upper surface, provided certain conditions are met. The localized area must contain trenches that are consistently, and closely spaced from each other. Moreover the trenches must be relatively narrow in lateral dimension. If those rather restrictive requirements are not met, then thicknesses of a given interconnect layer can vary to such a degree that local regions of interconnect may suffer severe current carrying limitations.

In particular, planarization may become quite difficult in a region where there is a relatively large distance between a series of relatively narrow interconnect, or if there is a relatively wide interconnect such as that found in, for example, a bond pad. FIGS. 2-4 illustrate a typical damascene process and the localized thinning or "dishing" problem experienced by conventional metal CMP processes.

As shown in FIG. 2, a series of relatively narrow trenches 22 and a relatively wide trench 24 are formed in an interlevel dielectric 20 using well-known lithography and etch techniques. The series of narrow trenches 22 and the wide trench 24 are laterally separated by a region of interlevel dielectric having a smooth upper surface 26. FIG. 3 illustrates a conductive material 28, e.g., a metal, such as Al, W, Ta, and Ti, deposited across the topography to a level spaced above upper surface 26. Due to the conformal nature of the sputter or CVD process used to

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apply the conductive material, the conductive material takes on an upper surface topography having a first region 30 formed over closely spaced hill and valley areas spaced above the surface of narrow trenches 22. The topography also includes a second region 32 having a single wide valley area spaced above the wide trench 24 and a substantially flat third region 34 spaced above

5 smooth upper surface 26. Conductive material 28 is then polished, as shown in FIG 4, using CMP to remove conductive material 28 from the upper surface of interlevel dielectric 20. As a result of CMP, a series of relatively narrow interconnect 36 are formed exclusively in narrow trenches 22 and a relatively wide interconnect 38 is formed exclusively in wide trench 24. The narrow interconnect 36 may serve to electrically connect underlying active devices and conductive elements of the semiconductor topography. The wide interconnect 38 may subsequently function as, e.g., a bond pad.

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem

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when forming an relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions

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of the CMP pad, the metal is not, and thus allows significant flexing of the pad. Such flexing of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

In addition, the topological surface includes a recessed area 40 arranged over the set of narrow interconnect 36. It is believed that such a recessed area 40 forms due to so-called "oxide erosion" of interlevel dielectric 20, assuming that the dielectric is composed of silicon oxide. The CMP slurry chosen to polish the metal of the interconnect includes a chemical component that reacts with metal at a faster rate than with oxide. As such, even after the metal surface has
been removed to a level commensurate with that of the oxide surface, its removal may continue at a faster rate than that of the oxide. The metal surface thus becomes spaced below that of the oxide, creating steps in the topological surface. At this point, the relatively small, elevated oxide regions are removed by the CMP pad at a faster rate than large area oxide regions, or even the adjacent, recessed metal regions. Because the oxide outside the area comprising the densely
packed interconnect has no elevational disparity, its removal rate is relatively slow. Therefore, the oxide in the dense interconnect area becomes recessed below the oxide outside the dense interconnect area.

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base

25 perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs be polished

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as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

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SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by an embodiment of the present invention in which a substantially planar semiconductor topography is formed by placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide 5 interconnect and another region defined by a series of relatively narrow interconnect. A plurality of electrically conductive features are embodied within the topography. The dielectric layer may be placed between an interconnect level and an underlying semiconductor substrate upon and within which active devices have been formed. Alternatively, the dielectric layer may be placed between successive interconnect levels. The dielectric layer may comprise a material having a relatively low dielectric constant, e.g. glass- or silicate-based dielectric, preferably oxide.

According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The widths, lengths, and depths of the dummy trenches, the wide trench, and the narrow trenches may vary according to design preferences and criteria. The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively. The depth of the wide, dummy, and narrow trenches is preferably 2,000 Å to 1 micron. The dummy trenches, the wide trench, and the narrow trenches are filled with a conductive material, e.g., a metal, such as aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner,

dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy

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trenches, and interconnect are formed exclusively in the narrow and wide trenches. The dummy conductors are electrically separate from electrically conductive features of the ensuing integrated circuit. As such, the dummy conductors preferably serve no purpose except to improve the planarization of the interconnect level in which they reside. The dummy conductors

therefore do not contain transitory voltages and/or current associated with or connected to active 5 and passive devices within the semiconductor topography. Most likely, the dummy conductors are connected to a power supply or ground, but not to any gate inputs or source/drain outputs of a active transistors, nor are they connected to any terminals of passive resistors or capacitors.

10 In one embodiment, the conductive material may be polished using well-known CMP. That is, the frontside of the semiconductor topography may be forced against a CMP polishing pad while the polishing pad and the topography are rotated relative to each other. A CMP slurry entrained with abrasive particles, e.g., ceria, silica, or alumina, is dispensed upon the polishing pad surface to aid in the removal of the conductive material. In an alternate embodiment, a "fixed-abrasive" technique is used to polish the conductive material. The fixed-abrasive 15 technique involves placing a liquid which is substantially free of particulate matter between the surface of the conductive material and an abrasive polishing surface of a polishing pad. The liquid contains no chemical constituent that could react with the topography. The abrasive polishing surface is moved relative to the semiconductor topography so as to polish the 20 conductive material. The liquid applied to the polishing surface preferably comprises deionized

- water, however, other liquids which have a near-neutral pH value may alternatively be directed onto the abrasive polishing surface. The pH that is chosen for the polishing process is one suitable for the conductive material and the polishing pad. The polishing surface comprises a polymer-based matrix entrained with particles selected from the group consisting of cerium
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- oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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The abrasive polishing surface belongs to a polishing pad which is substantially resistant to deformation even when placed across an elevationally recessed region of relatively large lateral dimension (e.g., over 200 microns lateral dimension). Therefore, the pad is relatively

5 non-conformal to the underlying surface and thus does not come in contact with elevationally recessed regions of the conductive material. It is believed that the particles dispersed throughout the abrasive polishing surface in combination with the polishing liquid interact chemically and physically with the elevated regions of the conductive material to remove those regions. However, the liquid alone may be incapable of removing the conductive material in elevationally recessed regions. As such, elevationally raised regions of the conductive material are removed at a substantially faster rate than elevationally recessed regions. The polish rate slows down significantly as the topological surface of the interconnect level approaches planarity.

Whatever polishing technique is applied to the conductive material, the presence of the
plurality of dummy conductors between the series of relatively narrow interconnect and the
relatively wide interconnect provides for global planarization of the topography employing the
trenches. In particular, the dummy conductors and the interposing dielectric protrusions replace
a relatively wide dielectric region absent of any conductive material. It is theorized that the
metal of the dummy conductors, being softer than the dielectric, contracts when a polishing pad
is forced against it. Consequently, the surface of the polishing pad extending over the dummy
conductors and the wide interconnect during polishing remains substantially flat when pressure is
applied thereto. That is, the surface area of the dielectric protrusions between the dummy
conductors is not sufficient to withstand the force of the polishing pad, and thus does not cause
the pad to flex. Therefore, dishing of the conductive material in the wide trench is less likely to
occur as a result of the polishing process.

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Also, the dummy conductors help prevent surface disparity that could result from erosion of the dielectric layer. The conductive material may continue to be polished more rapidly than the dielectric once the surface of the conductive material has been removed to the same elevational plane as the dielectric. The dielectric protrusions between the dummy conductors and

- 5 the closely spaced narrow interconnect may thus become elevated above the conductive material. Consequently, the entire topological surface of the interconnect level has surface disparities, causing the polish rate of the elevated dielectric protrusions to become greater than that of the recessed dummy conductors and interconnect. As the polishing process continues, the dielectric protrusions are again made substantially coplanar with the dummy conductors and the
- 10 interconnect. This cycle may be repeated until it is desirable to stop the polishing process.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

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FIG. 1 depicts a side plan view of an apparatus that may be used to chemical-mechanical polish a semiconductor topography;

FIG. 2 depicts a partial cross-sectional view of a conventional semiconductor topography,
wherein a series of relatively narrow trenches are formed within an interlevel dielectric a spaced distance from a relatively wide trench;

FIG. 3 depicts a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the trenches to a level spaced above an upper surface of the interlevel dielectric;

FIG. 4 depicts a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed from the upper surface of the interlevel dielectric using a conventional CMP technique, thereby forming a topological surface having elevational disparities;

FIG. 5 depicts a partial cross-sectional view of a semiconductor topography according to an embodiment of the present invention, wherein a plurality of laterally spaced dummy trenches are formed in a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

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FIG. 6 is a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the dummy trenches, the narrow trenches, and the wide trench to a level spaced above the upper surface of the dielectric layer;

FIG. 7 is a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed to a level substantially commensurate with that of the upper surface of the dielectric layer using a planarization process according to an embodiment of the present invention, thereby forming a planarized topological surface; and

FIG. 8 is a process flow diagram of a fixed-abrasive polishing technique that may be used to polish the conductive material.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Turning to FIG. 5, a partial cross-section of a semiconductor topography is presented. Electrically conductive features may be embodied within the topography. A dielectric layer 50 is shown which may comprise a dielectric material having a relatively low dielectric constant. 5 Dielectric layer 50 may comprise, e.g., a glass- or silicate- based material, such as an oxide that has been deposited by chemical-vapor deposition ("CVD") from either a tetraethyl orthosilicate ("TEOS") source or a silane source and doped with an impurity, e.g., boron or phosphorus. Dielectric layer 50 may serve as a poly-metal interlevel dielectric ("PMD") between a doped polycrystalline silicon ("polysilicon") gate layer and an ensuing metal interconnect layer. It is to be understood that the gate layer may comprise other conductive materials besides polysilicon. Alternatively, dielectric 50 may form an inter-metal interlevel dielectric ("IMD") between an underlying metal interconnect layer and an ensuing overlying metal interconnect layer.

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. [Gentlemen, are the dimensions and spacings listed here for the trenches correct?] The trenches may be formed by

25 lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions

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of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

As shown in FIG. 6, a conductive material 58 may subsequently be deposited into the
trenches and across dielectric layer 50 to a level spaced above the uppermost horizontal surface of dielectric layer 50. Conductive material 58 may comprise a metal, e.g., aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. Such a metal may be sputter deposited from a metal target or MOCVD (i.e., metal organic CVD) deposited from a metal organic source. The as-deposited conductive material 58 has an elevationally disparate surface
that includes a first region 60 above narrow trenches 52, a second region 62 above dummy trenches 56, and a third region 64 above wide trench 54. The valley areas of regions 60, 62, and 64 are directly above respective trenches, while the hill areas are directly above respective dielectric protrusions that are positioned between the trenches.

Turning to Fig. 7, conductive material 58 may then be polished to a level substantially coplanar with the uppermost surface of dielectric layer 50. As a result of polishing conductive material 58, relatively narrow interconnect 66 are formed exclusively in trenches 52, dummy conductors 68 are formed in dummy trenches 56, and a relatively wide interconnect 72 is formed in trench 54. Dummy conductors 68 are laterally spaced from each other and/or from interconnect 66 and 72 by dummy dielectric protrusions 70. Placing dummy conductors 68 in the region between the series of narrow interconnect 66 and the wide interconnect 72 affords global planarization of the topological surface. That is, the polish rate is substantially uniform across the entire topological surface. Also, the polish rate of elevationally raised regions is

greater than that of elevationally recessed regions. Further, a surface having elevational disparity

is polished at a faster rate than a substantially flat surface.

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It is believed that the presence of dummy conductors 68 helps prevent the polishing pad from deforming about the length of the pad into relatively wide trench 54 when subjected to normal pressure. Further, it is postulated that placing dummy conductors 68 between dummy dielectric protrusions 70 ensures that elevational fluctuations are present in different regions of the topological surface at the same time. That is, no particular region of the topological surface

5 the topological surface at the same time. That is, no particular region of the topological surface becomes substantially planarized before other regions and thereby causes fluctuations in the polish rate across the surface. Thus, the polish rate does not slow down until the entire topological surface is substantially free of elevational disparity.

Dummy conductors 68 are not connected to any active or passive device which forms an integrated circuit of the semiconductor topography shown in FIG. 7. While dummy conductors can carry power or ground voltages, they do not carry transitory voltages or current associated with an operable circuit. Nor are they associated or connected in any way with active circuit elements and/or features such as a contact, implant, gate, etc., of a transistor, capacitor, resistor, etc.

FIG. 8 illustrates a process flow diagram of a fixed abrasive CMP technique that may be used to polish conductive material 58, and thereby form the substantially planar topography shown in FIG. 7. Conductive material 58 may be polished using an apparatus similar in some respects to that shown in Fig. 1. The apparatus in Fig. 1 may be purposefully modified to accommodate an abrasive polishing surface and a conduit for delivering a particle-free solution to the polishing surface. Alternatively, a conventional CMP process may be employed for polishing conductive material 58. The CMP slurry may include a component that chemically reacts with conductive material 58.

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As described in block 72, a particle-free liquid is dispensed onto an abrasive polishing surface of a polishing pad having a substantially rigid supportive backing. An appropriate polishing pad is commercially available from Minnesota Mining and Manufacturing Company. The polishing surface comprises a polymer-based matrix entrained with abrasive particles. Appropriate materials that may be used for the particles include, but are not limited to, ceria, α alumina, γ alumina, silicon dioxide, titania, chromia, and zirconia. Preferably, the polishing liquid forwarded onto the abrasive polishing surface is deionized water. The polishing liquid may also be other types of liquids which have a near-neutral pH. As shown in block 74 of FIG. 8, the semiconductor topography depicted in FIG. 6 may be positioned face-down upon the polishing surface. The polishing liquid is positioned at the interface between the semiconductor topography and the abrasive polishing surface.

As indicated by block 76 of FIG. 8, the semiconductor topography and the abrasive polishing surface may be rotated relative to each other while the frontside of the topography is forced against the polishing surface. It is believed that contact between the high elevation regions of conductive material 58 and the abrasive particles as well as the polishing liquid causes the surface material of conductive material 58 in those elevated regions to be released from bondage with the bulk of the conductive material. The particles extending from the abrasive polishing surface have a sufficient hardness to dislodge the reacted surface material during abrasion of the high elevation regions. The rigidness of the polishing pad may be sufficient to prevent the abrasive polishing surface from contacting recessed regions of conductive material 58. Accordingly, very little of the conductive material 58 in the recessed regions is removed.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method for forming a substantially planar semiconductor topography by placing a plurality of dummy conductors in a dielectric layer laterally between a

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relatively wide interconnect and a series of relatively narrow interconnect. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, electrically conductive features isolated from each other by a dielectric may subsequently be formed upon the planarized semiconductor

5 topography. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.



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WHAT IS CLAIMED IS:

1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

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etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said dummy trenches and said wide and narrow trenches with a conductive material;

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said narrow and wide trenches, wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

2. The method of claim 1, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

35 7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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9. A method for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive a relatively narrow interconnect feature;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors bounded exclusively within said dummy trenches electrically separate from said electrically conductive features, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features.

10. The method of claim 9, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

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14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

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15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

10 17. A substantially planar semiconductor topography elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit, comprising:

a plurality of laterally spaced dummy trenches residing within a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors bounded exclusively within said dummy trenches and electrically separate from said plurality of electrically conductive features; and

interconnect bounded exclusively within said narrow and wide trenches, wherein interconnect upper surfaces are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

The substantially planar semiconductor topography of claim 17, wherein said dummy
 conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten,
 molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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ABSTRACT OF THE DISCLOSURE

The present invention advantageously provides a substantially planarized semiconductor 5 topography and method for making the same by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect and a series of relatively narrow interconnect. According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The dummy trenches, the wide trench, and the narrow trenches are filled with a 10 conductive material, e.g., a metal. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner, dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy trenches, and interconnect 15 are formed exclusively in the narrow and wide trenches. The topological surface of the resulting interconnect level is substantially void of surface disparity.

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DECLARATION AND POWER OF ATTORNEY

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My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT," the specification of which:

is attached hereto.
is attached on ______as Application Serial No. _______
and was amended on ______(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

Prior Foreign Application No.	Country	Filing Date (mm/dd/yy)	Priority Claimed	Cert. copy Attached
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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Provisional Application No. Filing Date (mm/dd/yy)

N/A

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Parent Application No.	Filing Date (mm/dd/yy)	Parent Patent No. (if applicable) or Status
N/A		

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The Assignee hereby revokes any previous Powers of Attorney and appoints Andrew D. Fortney, Reg. No. 34,600 of Cypress Semiconductor Corporation, and Kevin L. Daffer, Reg. No. 34,146; B. Noel Kivlin, Reg. No. 33,929; and, Eric B. Meyertons, Reg. No. 34,876 of the firm of Conley, Rose & Tayon, as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications to:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Phone: (512) 476-1400

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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JANUARY 04, 1999

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RECORDATION DATE: 08/31/1998

REEL/FRAME: 9435/0506 NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR: SETHURAMAN, ANANTHA R.

DOC DATE: 08/21/1998

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DOC DATE: 08/21/1998

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SERIAL NUMBER: 09143723 PATENT NUMBER: FILING DATE: 08/31/1998 ISSUE DATE:

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To the best of my knowledge and belief, the foregoing information is Kevin L. Daffer Name of Person Signing Reg. No. 34,146	ry and equiper and any attached copy is a true copy of the original document. August 31, 1998

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned, does hereby:

SELL, ASSIGN AND TRANSFER to <u>CYPRESS SEMICONDUCTOR</u> <u>CORPORATION</u> (the "Assignee"), having a place of business at <u>3939 North First Street</u>, <u>San Jose, CA, 95134</u> the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith, and is entitled <u>"A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM</u> <u>INTERCONNECT</u>", such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee; and

COVENANT AND AGREE that the above is and will be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

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FURTHER COVENANT that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

167-21,1998 Date: H (Signature) Anantha R. Sethuraman 8 21 98 Date: (Signature) Christopher/ ams

Please direct all communication as follows:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Ph: (512) 476-1400

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SEARCH NOTES (INCLUDING SEARCH STRATEGY) Date Exmr. EBST attacked (USPAT; USPS; 47/2 Epo; Jpo; IBM; Derwant) 20 consulted with \$42 Le Wall Fahmy about "relatively Wide" and "relatively narrow" (broad not indefiniti) ENST attached Le cuspati uspai 5/2/03 EpoispoisBmi Dernvent) (RIGHT OUTSIDE)

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Atty. Dkt. No. 5298-02501 PM98019C Inventor(s):

Anantha R. Sethuraman Christopher A. Seams

Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

	ATE OF EXPRESS MAIL DER 37 C.F.R. § 1.10
"Express Mail" maili Date of Deposit: Fel	ng label no. <u>EL726370210US</u> bruary 7, 2001
with the United State Office to Addressee" the date indicated abo	his paper or fee is being deposited s Postal Service "Express Mail Post service under 37 C.F.R. §1.10 on ove and is addressed to: Assistant, tents, Box Patent Application, 31.

Derrick Brown



UTILITY PATENT APPLICATION TRANSMITTAL

(For new non-provisional applications under 37 CFR § 1.53(b))

This is a Continuation Application of prior application no. 09/143,723 filed August 31, 1998 and assigned to Cypress Semiconductor, recorded at Reel 9435, Frame 0506.

Enclosed are the following items:

- A fee authorization for the amount of \$710.00.
- Request & Certification under 35 U.S.C. 122(b)(2)(B)(i).
- Specification as originally submitted including informal drawings.
- Formal drawings of Figs. 1 8 on 3 sheets.
 - 5. Copy of Declaration/Power of Attorney from prior application (see 37 CFR 1.63(d)).
 - Copy of Assignment papers from prior application.
 - Information Disclosure Statement w/form PTO-1449.
 - Return receipt postcard(s).

Please amend the specification by inserting before the first line the sentence: - This is a

continuation application from prior application no. 09/143,723, filed August 31, 1998.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

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Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10

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Derrick Brow

FEE AUTHORIZATION

Assistant Commissioner for Patents Washington, D.C. 20231

The Commissioner is hereby authorized to charge the following fee to Conley, Rose & Tayon, P.C. deposit account no. 50-1505/5298-02501^{*}.

Item:	Filing fee
Amount:	\$710.00
Atty. Dkt. No.	5298-02501

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

^{*} If the above listed account is found to have insufficient funds, the Commissioner is authorized to charge Conley, Rose & Tayon, P.C. deposit account no. 50-1623/5298-02501.

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> > Derrick Brown

REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)

 Atty Docket Number:
 5298-02501

 First Named Inventor:
 Anantha R. Sethuraman et al.

 Title:
 PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

February 7, 2001 Date

Kevin L. Daffer, Reg. No. 34,146

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer. U.S. Patent and Trademark Office. Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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FIG. 8

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Trademarks, BOX PATENT APPLICA 20231	TION, Washington, D.C.
Roger Combs	

A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

By:

Anantha R. Sethuraman Christopher A. Seams

Atty. Dkt. No.: 5298-02500

Kevin L. Daffer/MLH Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, TX 78767-0398 Ph: (512) 476-1400

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BACKGROUND OF THE INVENTION

Field of the Invention

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This invention relates to integrated circuit manufacturing and, more particularly, to a substantially planarized interconnect topography and method for making spaced interconnect by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect structure and a series of relatively narrow interconnect structures.

2. 10 Description of the Related Art

Fabrication of an integrated circuit involves numerous processing steps. After implant regions (e.g., source/drain regions) have been placed within a semiconductor substrate and gate areas defined upon the substrate, an interlevel dielectric is formed across the topography to isolate the gate areas and the implant regions from overlying conducting regions. Interconnect routing is then patterned across the interlevel dielectric and connected to the implant regions and/or the gate areas by ohmic contacts formed through the interlevel dielectric. Alternating levels of interlevel dielectric and interconnect may be placed across the semiconductor topography to form a multi-level integrated circuit.

As successive layers are deposited across previously patterned layers of an integrated circuit, elevational disparities develop across the surface of each layer. If left unattended, the elevational disparities in each level of an integrated circuit can lead to various problems. For example, when a dielectric, conductive, or semiconductive material is deposited over a

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topological surface having elevationally raised and recessed regions, step coverage problems may arise. Step coverage is defined as a measure of how well a film conforms over an

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underlying step and is expressed by the ratio of the minimum thickness of a film as it crosses a step to the nominal thickness of the film over horizontal regions. Also, stringers may arise from incomplete etching over severe steps. Furthermore, correctly patterning layers upon a topological surface containing fluctuations in elevation may be difficult using optical

5 lithography. The depth-of-focus of the lithography alignment system may vary depending upon whether the resist resides in an elevational "hill" or "valley" area. The presence of such elevational disparities therefore makes it difficult to print high resolution features.

Techniques involving chemical and mechanical abrasion (e.g., chemical-mechanical 10 polishing) to planarize or remove the surface irregularities have grown in popularity. As shown in FIG. 1, a typical chemical-mechanical polishing ("CMP") process involves placing a semiconductor wafer 12 face-down on a polishing pad 14 which lies on or is attached to a rotatable table or platen 16. A popular polishing pad medium comprises polyurethane or polyurethane-impregnated polyester felts. During the CMP process, polishing pad 14 and TU 15 semiconductor wafer 12 may be rotated while a carrier 10 holding wafer 12 applies a downward force F upon polishing pad 14. An abrasive, fluid-based chemical suspension, often referred to as a "slurry", is deposited from a conduit 18 positioned above pad 14 onto the surface of polishing pad 14. The slurry may fill the space between pad 14 and the surface of wafer 12. The polishing process may involve a chemical in the slurry reacting with the surface material being 20 polished. The rotational movement of polishing pad 14 relative to wafer 12 causes abrasive particles entrained within the slurry to physically strip the reacted surface material from wafer 12. The pad 14 itself may also physically remove some material from the surface of the wafer 12. The abrasive slurry particles are typically composed of silica, alumina, or ceria.

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> CMP is commonly used to form a planarized level of an integrated circuit containing interconnect laterally spaced from each other in what is generally referred to as the "damascene"

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process. Laterally spaced trenches are first etched in an interlevel dielectric configured upon a semiconductor topography comprising electrically conductive features. A conductive material is then deposited into the trenches and on the interlevel dielectric between trenches to a level spaced above the upper surface of the interlevel dielectric. CMP is applied to the surface of the

5 conductive material to remove that surface to a level substantially commensurate with that of the upper surface of the interlevel dielectric. In this manner, interconnect that are isolated from each other by the interlevel dielectric are formed exclusively in the trenches. CMP can planarize only localized regions of the interconnect surface such that all interconnect traces have a co-planar upper surface, provided certain conditions are met. The localized area must contain trenches that are consistently, and closely spaced from each other. Moreover the trenches must be relatively narrow in lateral dimension. If those rather restrictive requirements are not met, then thicknesses of a given interconnect layer can vary to such a degree that local regions of interconnect may suffer severe current carrying limitations.

In particular, planarization may become quite difficult in a region where there is a relatively large distance between a series of relatively narrow interconnect, or if there is a relatively wide interconnect such as that found in, for example, a bond pad. FIGS. 2-4 illustrate a typical damascene process and the localized thinning or "dishing" problem experienced by conventional metal CMP processes.

As shown in FIG. 2, a series of relatively narrow trenches 22 and a relatively wide trench 24 are formed in an interlevel dielectric 20 using well-known lithography and etch techniques. The series of narrow trenches 22 and the wide trench 24 are laterally separated by a region of interlevel dielectric having a smooth upper surface 26. FIG. 3 illustrates a conductive material 28, e.g., a metal, such as Al, W, Ta, and Ti, deposited across the topography to a level spaced above upper surface 26. Due to the conformal nature of the sputter or CVD process used to

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apply the conductive material, the conductive material takes on an upper surface topography having a first region 30 formed over closely spaced hill and valley areas spaced above the suites of narrow trenches 22. The topography also includes a second region 32 having a single wide valley area spaced above the wide trench 24 and a substantially flat third region 34 spaced above

5 smooth upper surface 26. Conductive material 28 is then polished, as shown in FIG 4, using CMP to remove conductive material 28 from the upper surface of interlevel dielectric 20. As a result of CMP, a series of relatively narrow interconnect 36 are formed exclusively in narrow trenches 22 and a relatively wide interconnect 38 is formed exclusively in wide trench 24. The narrow interconnect 36 may serve to electrically connect underlying active devices and 10 conductive elements of the semiconductor topography. The wide interconnect 38 may subsequently function as, e.g., a bond pad.

A print lots from the literation of the state and the state of the sta Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem

when forming an relatively wide interconnect between regions of a dielectric that is substantially 25 more dense than the metal. While the dielectric is hard enough to support the overlying regions

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of the CMP pad, the metal is not, and thus allows significant flexing of the pad. Such flexing of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

In addition, the topological surface includes a recessed area 40 arranged over the set of 5 narrow interconnect 36. It is believed that such a recessed area 40 forms due to so-called "oxide erosion" of interlevel dielectric 20, assuming that the dielectric is composed of silicon oxide. The CMP slurry chosen to polish the metal of the interconnect includes a chemical component that reacts with metal at a faster rate than with oxide. As such, even after the metal surface has 10 been removed to a level commensurate with that of the oxide surface, its removal may continue at a faster rate than that of the oxide. The metal surface thus becomes spaced below that of the oxide, creating steps in the topological surface. At this point, the relatively small, elevated oxide regions are removed by the CMP pad at a faster rate than large area oxide regions, or even the adjacent, recessed metal regions. Because the oxide outside the area comprising the densely 15 packed interconnect has no elevational disparity, its removal rate is relatively slow. Therefore, the oxide in the dense interconnect area becomes recessed below the oxide outside the dense interconnect area.

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in

the space between the series of narrow interconnect and the wide interconnect needs be polished

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as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

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SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by an embodiment of the present invention in which a substantially planar semiconductor topography is formed by placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide interconnect and another region defined by a series of relatively narrow interconnect. A plurality of electrically conductive features are embodied within the topography. The dielectric layer may be placed between an interconnect level and an underlying semiconductor substrate upon and within which active devices have been formed. Alternatively, the dielectric layer may be placed between successive interconnect levels. The dielectric layer may comprise a material having a relatively low dielectric constant, e.g. glass- or silicate-based dielectric, preferably oxide.

According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The widths, lengths, and depths of the dummy trenches, the wide trench, and the 15 narrow trenches may vary according to design preferences and criteria. The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively. The depth of the wide, dummy, and narrow trenches is preferably 2,000 Å to 1 micron. The dummy trenches, the wide trench, 20 and the narrow trenches are filled with a conductive material, e.g., a metal, such as aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above 25 the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner,

dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy

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trenches, and interconnect are formed exclusively in the narrow and wide trenches. The dummy conductors are electrically separate from electrically conductive features of the ensuing integrated circuit. As such, the dummy conductors preferably serve no purpose except to improve the planarization of the interconnect level in which they reside. The dummy conductors

therefore do not contain transitory voltages and/or current associated with or connected to active 5 and passive devices within the semiconductor topography. Most likely, the dummy conductors are connected to a power supply or ground, but not to any gate inputs or source/drain outputs of a active transistors, nor are they connected to any terminals of passive resistors or capacitors.

10 In one embodiment, the conductive material may be polished using well-known CMP. That is, the frontside of the semiconductor topography may be forced against a CMP polishing pad while the polishing pad and the topography are rotated relative to each other. A CMP slurry entrained with abrasive particles, e.g., ceria, silica, or alumina, is dispensed upon the polishing pad surface to aid in the removal of the conductive material. In an alternate embodiment, a "fixed-abrasive" technique is used to polish the conductive material. The fixed-abrasive 15 technique involves placing a liquid which is substantially free of particulate matter between the surface of the conductive material and an abrasive polishing surface of a polishing pad. The liquid contains no chemical constituent that could react with the topography. The abrasive polishing surface is moved relative to the semiconductor topography so as to polish the 20 conductive material. The liquid applied to the polishing surface preferably comprises deionized water, however, other liquids which have a near-neutral pH value may alternatively be directed onto the abrasive polishing surface. The pH that is chosen for the polishing process is one suitable for the conductive material and the polishing pad. The polishing surface comprises a polymer-based matrix entrained with particles selected from the group consisting of cerium 25 oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and

zirconium oxide.

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The abrasive polishing surface belongs to a polishing pad which is substantially resistant to deformation even when placed across an elevationally recessed region of relatively large lateral dimension (e.g., over 200 microns lateral dimension). Therefore, the pad is relatively

- 5 non-conformal to the underlying surface and thus does not come in contact with elevationally recessed regions of the conductive material. It is believed that the particles dispersed throughout the abrasive polishing surface in combination with the polishing liquid interact chemically and physically with the elevated regions of the conductive material to remove those regions. However, the liquid alone may be incapable of removing the conductive material in elevationally recessed regions. As such, elevationally raised regions of the conductive material are removed at
 - a substantially faster rate than elevationally recessed regions. The polish rate slows down significantly as the topological surface of the interconnect level approaches planarity.

Whatever polishing technique is applied to the conductive material, the presence of the
plurality of dummy conductors between the series of relatively narrow interconnect and the
relatively wide interconnect provides for global planarization of the topography employing the
trenches. In particular, the dummy conductors and the interposing dielectric protrusions replace
a relatively wide dielectric region absent of any conductive material. It is theorized that the
metal of the dummy conductors, being softer than the dielectric, contracts when a polishing pad
is forced against it. Consequently, the surface of the polishing pad extending over the dummy
conductors and the wide interconnect during polishing remains substantially flat when pressure is
applied thereto. That is, the surface area of the dielectric protrusions between the dummy
conductors is not sufficient to withstand the force of the polishing pad, and thus does not cause
the pad to flex. Therefore, dishing of the conductive material in the wide trench is less likely to
occur as a result of the polishing process.

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المراجع من المراجع الم المراجع 20 Also, the dummy conductors help prevent surface disparity that could result from erosion of the dielectric layer. The conductive material may continue to be polished more rapidly than the dielectric once the surface of the conductive material has been removed to the same elevational plane as the dielectric. The dielectric protrusions between the dummy conductors and

- 5 the closely spaced narrow interconnect may thus become elevated above the conductive material. Consequently, the entire topological surface of the interconnect level has surface disparities, causing the polish rate of the elevated dielectric protrusions to become greater than that of the recessed dummy conductors and interconnect. As the polishing process continues, the dielectric protrusions are again made substantially coplanar with the dummy conductors and the
- 10 interconnect. This cycle may be repeated until it is desirable to stop the polishing process.

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BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

FIG. 1 depicts a side plan view of an apparatus that may be used to chemical-mechanical polish a semiconductor topography;

FIG. 2 depicts a partial cross-sectional view of a conventional semiconductor topography,
wherein a series of relatively narrow trenches are formed within an interlevel dielectric a spaced distance from a relatively wide trench;

FIG. 3 depicts a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the trenches to a level spaced above an upper surface of the interlevel dielectric;

FIG. 4 depicts a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed from the upper surface of the interlevel dielectric using a conventional CMP technique, thereby forming a topological surface having elevational disparities;

FIG. 5 depicts a partial cross-sectional view of a semiconductor topography according to an embodiment of the present invention, wherein a plurality of laterally spaced dummy trenches are formed in a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

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FIG. 6 is a partial cross-sectional view of the semiconductor topography, wherein a conductive material is deposited into the dummy trenches, the narrow trenches, and the wide trench to a level spaced above the upper surface of the dielectric layer;

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FIG. 7 is a partial cross-sectional view of the semiconductor topography, wherein the surface of the conductive material is removed to a level substantially commensurate with that of the upper surface of the dielectric layer using a planarization process according to an embodiment of the present invention, thereby forming a planarized topological surface; and

FIG. 8 is a process flow diagram of a fixed-abrasive polishing technique that may be used to polish the conductive material.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Turning to FIG. 5, a partial cross-section of a semiconductor topography is presented. Electrically conductive features may be embodied within the topography. A dielectric layer 50 is shown which may comprise a dielectric material having a relatively low dielectric constant. Dielectric layer 50 may comprise, e.g., a glass- or silicate- based material, such as an oxide that has been deposited by chemical-vapor deposition ("CVD") from either a tetraethyl orthosilicate ("TEOS") source or a silane source and doped with an impurity, e.g., boron or phosphorus. Dielectric layer 50 may serve as a poly-metal interlevel dielectric ("PMD") between a doped

polycrystalline silicon ("polysilicon") gate layer and an ensuing metal interconnect layer. It is to 10 be understood that the gate layer may comprise other conductive materials besides polysilicon. Alternatively, dielectric 50 may form an inter-metal interlevel dielectric ("IMD") between an underlying metal interconnect layer and an ensuing overlying metal interconnect layer.

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. [Gentlemen, are the dimensions and spacings listed here for the trenches correct?] The trenches may be formed by

25 lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions

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of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

As shown in FIG. 6, a conductive material 58 may subsequently be deposited into the
trenches and across dielectric layer 50 to a level spaced above the uppermost horizontal surface of dielectric layer 50. Conductive material 58 may comprise a metal, e.g., aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. Such a metal may be sputter deposited from a metal target or MOCVD (i.e., metal organic CVD) deposited from a metal organic source. The as-deposited conductive material 58 has an elevationally disparate surface
that includes a first region 60 above narrow trenches 52, a second region 62 above dummy trenches 56, and a third region 64 above wide trench 54. The valley areas of regions 60, 62, and 64 are directly above respective trenches, while the hill areas are directly above respective dielectric protrusions that are positioned between the trenches.

Turning to Fig. 7, conductive material 58 may then be polished to a level substantially coplanar with the uppermost surface of dielectric layer 50. As a result of polishing conductive material 58, relatively narrow interconnect 66 are formed exclusively in trenches 52, dummy conductors 68 are formed in dummy trenches 56, and a relatively wide interconnect 72 is formed in trench 54. Dummy conductors 68 are laterally spaced from each other and/or from interconnect 66 and 72 by dummy dielectric protrusions 70. Placing dummy conductors 68 in the region between the series of narrow interconnect 66 and the wide interconnect 72 affords global planarization of the topological surface. That is, the polish rate is substantially uniform across the entire topological surface. Also, the polish rate of elevationally raised regions is greater than that of elevationally recessed regions. Further, a surface having elevational disparity is polished at a faster rate than a substantially flat surface.

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It is believed that the presence of dummy conductors 68 helps prevent the polishing pad from deforming about the length of the pad into relatively wide trench 54 when subjected to normal pressure. Further, it is postulated that placing dummy conductors 68 between dummy dielectric protrusions 70 ensures that elevational fluctuations are present in different regions of

5 the topological surface at the same time. That is, no particular region of the topological surface becomes substantially planarized before other regions and thereby causes fluctuations in the polish rate across the surface. Thus, the polish rate does not slow down until the entire topological surface is substantially free of elevational disparity.

10 Dummy conductors 68 are not connected to any active or passive device which forms an integrated circuit of the semiconductor topography shown in FIG. 7. While dummy conductors can carry power or ground voltages, they do not carry transitory voltages or current associated with an operable circuit. Nor are they associated or connected in any way with active circuit elements and/or features such as a contact, implant, gate, etc., of a transistor, capacitor, resistor, 15 etc.

FIG. 8 illustrates a process flow diagram of a fixed abrasive CMP technique that may be used to polish conductive material 58, and thereby form the substantially planar topography shown in FIG. 7. Conductive material 58 may be polished using an apparatus similar in some respects to that shown in Fig. 1. The apparatus in Fig. 1 may be purposefully modified to accommodate an abrasive polishing surface and a conduit for delivering a particle-free solution to the polishing surface. Alternatively, a conventional CMP process may be employed for polishing conductive material 58. The CMP slurry may include a component that chemically reacts with conductive material 58.

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As described in block 72, a particle-free liquid is dispensed onto an abrasive polishing surface of a polishing pad having a substantially rigid supportive backing. An appropriate polishing pad is commercially available from Minnesota Mining and Manufacturing Company. The polishing surface comprises a polymer-based matrix entrained with abrasive particles.

Appropriate materials that may be used for the particles include, but are not limited to, ceria, α alumina, γ alumina, silicon dioxide, titania, chromia, and zirconia. Preferably, the polishing liquid forwarded onto the abrasive polishing surface is deionized water. The polishing liquid may also be other types of liquids which have a near-neutral pH. As shown in block 74 of FIG.
8, the semiconductor topography depicted in FIG. 6 may be positioned face-down upon the polishing surface. The polishing liquid is positioned at the interface between the semiconductor topography and the abrasive polishing surface.

As indicated by block 76 of FIG. 8, the semiconductor topography and the abrasive polishing surface may be rotated relative to each other while the frontside of the topography is forced against the polishing surface. It is believed that contact between the high elevation regions of conductive material 58 and the abrasive particles as well as the polishing liquid causes the surface material of conductive material 58 in those elevated regions to be released from bondage with the bulk of the conductive material. The particles extending from the abrasive polishing surface have a sufficient hardness to dislodge the reacted surface material during abrasion of the high elevation regions. The rigidness of the polishing pad may be sufficient to prevent the abrasive polishing surface from contacting recessed regions of conductive material 58. Accordingly, very little of the conductive material 58 in the recessed regions is removed.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method for forming a substantially planar semiconductor topography by placing a plurality of dummy conductors in a dielectric layer laterally between a

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relatively wide interconnect and a series of relatively narrow interconnect. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, electrically conductive features isolated from each other by a dielectric may subsequently be formed upon the planarized semiconductor

5 topography. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

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1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said dummy trenches and said wide and narrow trenches with a conductive material;

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said narrow and wide trenches, wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

2. The method of claim 1, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tangsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

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7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. A method for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive a relatively narrow interconnect feature;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors bounded exclusively within said dummy trenches electrically separate from said electrically conductive features, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features.

10. The method of claim 9, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

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15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

17. A substantially planar semiconductor topography elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit, comprising:

a plurality of laterally spaced dummy trenches residing within a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors bounded exclusively within said dummy trenches and electrically separate from said plurality of electrically conductive features; and

interconnect bounded exclusively within said narrow and wide trenches, wherein interconnect upper surfaces are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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ABSTRACT OF THE DISCLOSURE

	The present invention advantageously provides a substantially planarized semiconductor
5	topography and method for making the same by forming a plurality of dummy features in a
	dielectric layer between a relatively wide interconnect and a series of relatively narrow
	interconnect. According to an embodiment, a plurality of laterally spaced dummy trenches are
	first etched in the dielectric layer between a relatively wide trench and a series of relatively
	narrow trenches. The dummy trenches, the wide trench, and the narrow trenches are filled with a
10	conductive material, e.g., a metal. The conductive material is deposited to a level spaced above
	the upper surface of the dielectric layer. The surface of the conductive material is then polished
	to a level substantially coplanar with that of the upper surface of the dielectric layer.
	Advantageously, the polish rate of the conductive material above the dummy trenches and the
	wide and narrow trenches is substantially uniform. In this manner, dummy conductors spaced
15	apart by dielectric protrusions are formed exclusively in the dummy trenches, and interconnect
	are formed exclusively in the narrow and wide trenches. The topological surface of the resulting
	interconnect level is substantially void of surface disparity.

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT," the specification of which:

is attached hereto.

Contraction and a second second	
as Application Serial No.	
(if applicable).	_
	as Application Serial No

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

Prior Foreign Application No.	Country	Filing Date (mm/dd/yy)	Priority Claimed	Cert. copy Attached
N/A	ale sees			
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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Provisional Application No.

N/A

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Ciling Data

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Parent Application No.	Filing Date (mm/dd/yy)	Parent Patent No. (if applicable) or Status
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Docket No. 5298-02500 PM98019

The Assignee hereby revokes any previous Powers of Attorney and appoints Andrew D.Fortney, Reg. No. 34,600 of Cypress Semiconductor Corporation, and Kevin L.Daffer, Reg. No. 34,146; B. Noel Kivlin, Reg. No. 33,929; and, Eric B. Meyertons, Reg. No. 34,876 of the firm of Conley, Rose & Tayon, as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications to:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Phone: (512) 476-1400

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(Includ	e number, street name, city, state	e and zip code)	
Terrent de To II Manue			
Inventor's Full Name:	Christopher A. Sea		
Inventor's Signature:	AV	Date: B	
		Date.	21/98
City and State (or Foreign Country) of Residen	ice: Pleasanton, CA	Citizenship:	21/98 U.S.A.
	nce: Pleasanton, CA 0 562 Trebbiand Place, Ple	Citizenship:	U.S.A.

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PATENT 5298-02500 PM98019

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned, does hereby:

SELL, ASSIGN AND TRANSFER to <u>CYPRESS SEMICONDUCTOR</u> <u>CORPORATION</u> (the "Assignee"), having a place of business at <u>3939 North First Street</u>, <u>San Jose, CA, 95134</u> the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith, and is entitled <u>"A PLANARIZED SEMICONDUCTOR INTERCONNECT</u> <u>TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM</u> <u>INTERCONNECT</u>", such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee; and

COVENANT AND AGREE that the above is and will be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

Page 1 of 2





PATENT 5298-02500 PM98019 4. .

TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

FURTHER COVENANT that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(Signature) Anantha R. Sethus man (Signature) Christopher ams

Date: Anguer 21, 1998

8/21/98 Date:

Please direct all communication as follows:

Kevin L. Daffer Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, Texas 78767-0398 Ph: (512) 476-1400

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Page 125 of 329



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JANUARY 04, 1999

CONLEY ROSE & TAYON, P.C. KEVIN L. DAFFER P.O. BOX 398 AUSTIN, TX 78767-0398 UNITED STATES DEPARTMENT OF COMMERCE Patent and Trademark Office ASSISTANT SECRETARY AND COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231

97-02500



UNITED STATES PATENT AND TRADEMARK OFFICE NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT



PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 703-308-9723. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, ASSIGNMENT DIVISION, BOX ASSIGNMENTS, CG-4, 1213 JEFFERSON DAVIS HWY, SUITE 320, WASHINGTON, D.C. 20231.

RECORDATION DATE: 08/31/1998

REEL/FRAME: 9435/0506 NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR: SETHURAMAN, ANANTHA R.

DOC DATE: 08/21/1998

DOC DATE: 08/21/1998

ASSIGNOR: SEAMS, CHRISTOPHER A.

ASSIGNEE: CYPRESS SEMICONDUCTOR CORP. 3901 N. 1ST STREET SAN JOSE, CALIFORNIA 95134

SERIAL NUMBER: 09143723 PATENT NUMBER: FILING DATE: 08/31/1998 ISSUE DATE:

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MRA 8-31-98	09-14-1998	U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office Atty Dkt. 5298-02500
To the Honorable Commissioner of Patents and Tradema	100827846	:opy thereof.
I. Name of conveying party(ies):	2. Name and add	ress of receiving party(ies):
ANANTHA R. SETHURAMAN CHRISTOPHER A. SEAMS	Name: <u>Cypres</u> Internal Address:	ss Semiconductor Corp.
Additional name(s) of conveying party(ies) attached?	Street Address:	3901 N. 1st Street
	City <u>San Jose</u>	State CA ZIP 95134
Other Execution Date: August 21, 1998 Application number(s) or patent number(s): If this document is being filed together with a new app		
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A. Patent Application No.(s) B. Patent No.(s) A. A. Name and address of party to whom correspondence concerning document should be mailed: Name: Kevin L. Daffer Internal Address: Conley, Rose & Tayon, P.C.	dditional numbers attached? Yes 6. Total number of 3 7. Total fee (37 C Finlos Author 8. Deposit accourt	PFR 3.41):
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PATENT APPLICATION SERIAL NO.

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE FEE RECORD SHEET

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Atty. Dkt. No. 5298-02501 PM98019C Inventor(s):

Anantha R. Sethuraman Christopher A. Seams

Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10 "Express Mail" mailing label no. <u>EL726370210US</u>

Date of Deposit: <u>February 7, 2001</u> I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to: Assistant, Commissioner for Patents, Box Patent Application,

Derrick Brown

Washington, DC 20231.

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Applicant requests consideration of the references listed on the attached Form PTO-1449, The references listed on the Form PTO-1449 were previously cited in application serial no. 09/143,723 to which the captioned application is seeking priority under 35 U.S.C. § 120; therefore, a copy of each reference is not enclosed.

No fee is believed to be required. If a fee is required, the Commissioner is authorized to charge Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-02501.

т

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: February 7, 2001

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List c For	of Paten Applic Disclos	O-1449 (modified) its and Publications cant's Information sure Statement sheets if necessary)	ATTY, DOC APPLICANT FILING DAT	SERIAL NO: Unknown GROUP: Unknown 2823			
		U.:	DOCUMENTS			50	
EXAM. NITIALS			DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
Le		3,629,023	12/21/71	Strehlow			
1		3,979,239	9/7/76	Walsh			
		4,256,535	3/17/81	Banks			
	17.01	4,261,791	4/14/81	Shwartzman			
1		4,373,991	2/15/83	Banks			
	1	4,505,720	3/19/85	Gabor et al.			
		4,600,469	7/15/86	Fusco et al.			
		4,677,043	6/30/87	Cordes, III et al.	-		
		4,768,883	9/6/88	Waldo et al.		6	
	6.01	4,778,532	10/18/88	McConnell et al.			
		4,789,648	12/6/88	Chow et al.			1
	_	4,879,258	11/7/89	Fisher			
		4,933,715	6/12/90	Yamada et al.			
	-	4,944,836	7/31/90	Beyer et al.	1.2.1		
		4,954,141	9/4/90	Takiyama et al.			
	de la d	4,956,313	9/1990	Cote et al.		1.	
		4,962,423	10/9/90	Yamada et al.	12.1		
		4,968,381	11/6/90	Prigge et al.			1
		4,986,878	1/22/91	Malazgirt et al.			
		5,032,203	7/16/91	Doy et al.	1		
		5,057,462	10/15/91	Eisenberg et al.	1		
		5,064,683	11/12/91	Poon et al.			
		5,084,419	1/28/92	Sakao			
		5,209,816	5/11/93	Yu et al.		L.,	1
	1.1	5,262,354	11/1993	Cote et al.			
1.0/	12.25	5,273,558	12/28/93	Nelson et al.		-	

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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Information Disclosure Statement--PTO 1449 (modified)

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)

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ATTY. DOCKET NO: 5298-02501

APPLICANT: Sethuraman et al.

FILING DATE: Herewith

GROUP: Unknown

<u>، 89/ 779</u> SERIAL NO: Unknow

2823

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE I APPROPRIATI
Lee		5,288,333	2/22/94	Tanaka et al.			
, _		5,312,777	5/1994	Cronin et al.			
		5,320,706	6/14/94	Blackwell			
		5,320,978	6/14/94	Hsu			
		5,340,370	8/23/94	Cadien et al.			
		5,346,584	9/13/94	Nasr et al.			
		5,362,668	11/8/94	Tasaka			
		5,362,669	11/8/94	Boyd et al.			
		5,363,550	11/15/94	Aitken et al.			
		5,376,482	12/27/94	Hwang et al.			
		5,389,194	2/14/95	Rostoker et al.		<u></u>	
		5,389,579	2/14/95	Wells			
		5,392,361	2/21/95	Imaizumi et al.			
		5,395,801	3/7/95	Doan et al.			
		5,397,741	3/1995	O'Connor et al.			
		5,401,691	3/28/95	Caldwell			
		5,406,111	4/11/95	Sun			
		5,435,772	7/25/95	Yu			1
		5,436,488	7/25/95	Poon et al.			
		5,441,094	8/15/95	Pasch			
		5,453,639	9/1995	Cronin et al.			
		5,459,096	10/17/95	Venkatesan et al.			1
		5,468,983	11/21/95	Hirase et al.			1
		5,486,265	1/23/96	Salugsugan			1
		5,492,858	2/20/96	Bose et al.			
		5,494,857	2/27/96	Cooperman et al.			
Y.		5,503,962	4/2/96	Caldwell		· · · ·	<u></u>

U.S. PATENT DOCUMENTS

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Page 2 of 4

Information Disclosure Statement--PTO 1449 (modified)

List c For	of Paten Applic Disclos	D-1449 (modified) ts and Publications eant's Information ure Statement sheets if necessary)	ATTY. DOC APPLICANT FILING DAT	SERIAL NO: Unknown ^{09/} /779,/23 GROUP: Unknown 2823					
		U .:	S. PATENT DOCUMENTS						
EXAM.	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE		
Lee	121	5,525,840	6/11/96	Tominaga	1		0		
1		5,531,861	7/2/96	Yu et al.					
		5,541,427	7/30/96	Chappell et al.					
		5,551,986	9/3/96	Jain		-			
		5,573,633	11/12/96	Gambino et al.	1				
	1	5,578,523	11/26/96	Fiordalice et al.					
		5,591,239	1/7/97	Larson et al.	1				
		5,595,937	1/21/97	Mikagi	210.00				
		5,607,345	3/4/97	Barry et al.					
		5,616,513	4/1/97	Shepard					
	21	5,629,242	5/13/97	Nagashima et al.					
	ñ., n.	5,643,406	7/1/97	Shimomura et al.					
	1.1.1	5,643,823	7/1/97	Ho et al.		1			
		5,643,836	7/1/97	Meister et al.		1			
		5,652,176	7/29/97	Maniar et al.			1		
-		5,656,097	8/12/97	Olesen et al.					
		5,664,990	9/9/97	Adams et al.					
		5,665,202	9/9/97	Subramanian et al.		-			
		5,666,985	9/16/97	Smith, Jr. et al.					
	1	5,676,587	10/1997	Landers et al.	1 1				
		5,702,977	12/30/97	Jang et al.		1			
1		5,721,172	8/1999	Jang et al.					
		5,728,308	3/17/98	Muroyama		-			
		5,776,808	7/7/98	Muller et al.					
		5,837,612	11/17/98	Ajuria et al.		2	· · · · · · · · · · · · · · · · · · ·		
P		5,906,532	5/25/99	Nakajima et al.					

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Page 3 of 4

Information Disclosure Statement--PTO 1449 (modified)

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)			ATTY. DOC APPLICANT FILING DAT	SERIAL NO: Unknow n 09/719,123 GROUP: Unknown 2823			
		U.	S. PATENT	DOCUMENTS	1		
EXAM. NITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE I APPROPRIATE
Ler		5,919,082	7/6/99	Walker et al.		1.1.1	1.1
Le		5,928,959	7/1999	Huckels et al.	1,227		
h		5,943,590	8/1999	Wang et al.			
L		5,952,687	9/14/99	Kawakubo et al.			
		FORE	IGN PATEN	T DOCUMENTS			
EXAM. NITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
the 1	e	/ 0 303 061	2/15/89	Europe			11.
stde	P.	Singer, "CMP Developers	Take Aim at STI	, Title, Date, Pertinent I Applications" and "Slurry-F nal, Volume 21, No. 2, p. 40	Free CMP I		ishing,
affect	fr	October 1994, pp. 63-68.		of Interlayer Dielectric: A R			0.00
11/	de	Sivaram et al., "Developme Dielectrics," International		les Used in the Chemical M olid State Devices & Materi			
fife a	Ke	Wolf, Silicon Processing fo	or the VLSI Era V	Volume 2: Process Integratio	n, Lattice l	Press 1990.	, pp. 189-191.

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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Information Disclosure Statement--PTO 1449 (modified)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Atty. Dkt. No. 5298-02501 PM98019C Inventor(s):

> Anantha R. Sethuraman Christopher A. Seams

Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

	CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10
	Mail" mailing label no. <u>EL726370210US</u> eposit: <u>February 7, 2001</u>
with the U Office to A the date in Commissi	ertify that this paper or fee is being deposited Inited States Postal Service "Express Mail Post Addressee" service under 37 C.F.R. §1.10 on idicated above and is addressed to: Assistant, oner for Patents, Box Patent Application, on, DC 20231.

PRELIMINARY AMENDMENT

Commissioner for Patents Washington, D.C. 20231

Dear Sir/Madam:

The captioned application is a continuation application pursuant to 37 C.F.R. § 1.53(b) from prior application 09/143,723 filed August 31, 1998. Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

Please amend the specification as follows. A "marked-up" version of these amendments is included in Attachment A.

Please replace the paragraph on pg. 4, line 13 - pg. 5, line 3 with the following:

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Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results

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from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem when forming a relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

Please replace the paragraph on pg. 5, line 19 - pg. 6, line 4 with the following:

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs to be polished as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

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Please replace the paragraph on pg. 13, line 15 - pg. 14, line 2 with the following:

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. The trenches may be formed by lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

In the Claims:

Please amend claims 1, 9, and 17 to read as follows. A "marked-up" version of these amendments is included in Attachment A.

(Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive/material;

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polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said narrow and wide trenches, wherein said dummy conductors are electrically separate from of electrically conductive features of an ensuing integrated circuit.

9. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;



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filling said plurality of dummy renches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said narrow and wide trenches, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims

21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

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AND ADD

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

CONCLUSION

In the present Amendment, the Specification and claims 1, 9, and 17 have been amended; claims 21 and 22 have been added. Therefore, pending claims 1-22 are presented for consideration by the Examiner. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon P.O. Box 398 Austin, TX 78767-0398 Date: <u>February 7, 2001</u>

માં સેન્દ્ર છે. તે તેમને માંના વેલ્યો છે. તેમ માંના માંના બેન્ટ છે. તે તે પ્રે મિલ્લે પ્રે સ્ટે પ્રે મિલ્લે મે માંના તેમને છે. તેમ બેન્ટને માંના વેલ્યો છે. તેમના માંના બેન્ટને બેન્ટ છે. તેમ બેન્ટને પ્રે મેન્ટ પ્રે મેન્ટ પ્

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ATTACHMENT A

"Marked-up" amendments as follows:

In the Specification:

Page 4, line 25, after the phrase "when forming" please delete "an" and substitute therefor --a--.

Page 5, line 26, after the phrase "wide interconnect needs" please insert --to--.

Page 13, lines 23-24, after the phrase "from 0.5 micron to 50 micron" please delete the following text: [Gentlemen, are the dimensions and spacings listed here for the trenches correct?].

In the Claims:

1. (Amended) A method [for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said [dummy trenches and said wide and narrow] trenches with a conductive material;

polishing said conductive material to form dummy conductors [exclusively] in said dummy trenches and interconnect [exclusively] in said narrow and wide trenches, wherein said dummy conductors are electrically separate from [said plurality of] electrically conductive features [and co-planar with said interconnect] of an ensuing integrated circuit.

9. (Amended) A method [for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive [a] relatively narrow interconnect [feature] <u>features</u>;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors [bounded exclusively within], wherein said dummy [trenches] conductors are electrically separate from [said] electrically conductive features[, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features] of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography [elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit], comprising:

a plurality of laterally spaced dummy trenches [residing within] in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors [bounded exclusively within] <u>in</u> said dummy trenches and electrically separate from [said plurality of] electrically conductive features <u>below said</u> <u>dummy conductors;</u> and

[interconnect bounded exclusively within] <u>conductive lines in</u> said narrow and wide trenches, wherein [interconnect] upper surfaces <u>of said conductive lines</u> are substantially coplanar with dummy conductor upper surfaces.

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21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.

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FEB-08-2001 THU 04:33 PM CONLEY ROSE & TAYON Approved for use through 10/31/2002. OMB 0651-0451 Mireling U.S. Patent and Trademark Office; U.S. DEPAR TMENT OF COMMERCE ction of information unless it displays a valid OMB control number. RQUEST TO RESCUE NONPERE FAX NO. 5127031250 e' +1 collection of information unless it displays a valid OMB control number. Under the Paperwork Reduction Act of 1995, no persons are required to respond to CERTIFICATE OF EXPRESS MAIL **REQUEST TO RESCIND PREVIOUS** UNDER 37 C.F.R. §1.10 NONPUBLICATION REQUEST "Express Mail" mailing label number: EL726369888US 35 U.S.C. 122(b)(2)(B)(iI) DATE OF DEPOSIT: February 8, 2001 Thereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addresson" service under 37 C.P.R. §1-10 on the date indicated above and is addressed to: Application No. Unknown February 7, 2001 Filing Date Assistant Commissioner for Potents First Named Inventor: Anantha R. Sethuraman et al. Washington, DC 20231 Atty Docket No. 5298-02501 -Group Art Unit Unknown Derrick Brown Examiner Unknown Title PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT I hereby rescind the previous request that the above-identified application not be published under 35 U.S.C. 122(b). February 8, 2001 Date Kevin L. Daffer, Reg. No. 34,146 This request must be signed in compliance with 37 CFR 1.33(b). Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that un application not be published under 35 U.S.C. 123(b) (and the PTO to process that request). Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any contactus on the atmount of time you are required to complete this form should be sant to the Chief Information Officer. U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 2023).

tome	PATENT 9 5298-02502/PM98019C
TRADEMAN IN THE UNITED STATES PA	TENT AND TRADEMARK OFFICE
n re Application of: Sethuraman et al.	§ Group Art Unit: Unknown § Examiner: Unknown
erial No. 09/779,123	\$ Atty. Dkt. No. 5298-02502
Filed: February 7, 2001 For: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT	S Atty. Dkt. No. 5298-02502 S I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated plow S 4/05/01 Date Kevin L. Daffer S 5 S 6 S 7 S 7 S 7 S 7 S 7 S 7 S 7 S 7
Assistant Commissioner for Patents	RECEIVED
Vashington, D.C. 20231	ARN

1. This Information Disclosure Statement is submitted:

a.

- within 3 months of the filing date of the above identified application, or within 3 months of entry into National stage prosecution of an International application, or before the mailing date of the first Office Action on the merits, and thus no certification and/or fee is required.
- b. after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus:
 - the certification of paragraph 2 below is provided, or a fee of \$180.00 is enclosed.

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c.	after the mailing date of a final Office Action or a Notice of Allowance
	and prior to payment of the issue fee, and thus:

the certification of paragraph 2 below is provided, and a fee of \$180.00 is enclosed.

2. It is hereby certified:

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> that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

> that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

- 3. Consideration of the following additional information (including any copending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:
- 4. For each non-English language reference listed on the attached Form PTO-1449:
 - reference is made to an English language translation submitted herewith, and/or
 - reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or
 - reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or
 - reference is made to the concise explanation contained in the specification of the present application at page(s) ______, and/or
 - reference is made to the concise explanation set forth below:
- 5. Applicant also offers the following comments for the Examiner's consideration:
- 6. Also enclosed is a copy of a foreign search report citing these references.
- 7. The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.



SAMSUNG EXHIBIT 1004

Samsung v. Invensas

8. Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-02501.

Respectfully submitted,

Kévin L. Daffer Reg. No. 34,146 Attorney for Applicant(s)

CONLEY, ROSE & TAYON, P.C. P. O. Box 398 Austin, Texas 78767 (512) 476-1400

Date: _______

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List of For	Applic	O-1449 (modified) tts and Publications cant's Information File Statement I sheets (necessary)	APPLICAN	. NO. 5298-02502 T: Sethuraman et al. TE: February 7, 2001		IAL NO. 0 DUP: U nk 2f:	10.00
	APR 2	7 2001 U.	S. PATENT I	DOCUMENTS			
EXAM	REF. DES.	DOCUMENT NUMBER 4,010,583	DATE	NAME	CLASS	SUB CLASS	FILING DATE I
Lee	BRAI	4,010,583	3/1977	Highberg	5/	284	
Lee	B2	4,393,628	7/1983	Ottman et al.	51	281	
L	B3	5,294,570	3/1994	Fleming, Jr. et al.	438	Fro	
2	B4	5,602,423	2/1997	Jain	257	752	
J-	B5	5,662,769	9/1997	Schonauer et al.	438	633	
L	B6	5,695,572	12/1997	Brunner et al.	134	3	
L	B7	5,782,675	7/1998	Southwick	451	56	
P	B8	5,786,260	7/1998	Jang et al.	438	401	
Per	B9	5,919,082	7/1999	Walker et al.	45/	41	
8m	B10	5,963,841	10/1999	Karlsson et al.	438	952	
P	B11	5,972,124	10/1999	Sethuraman	134438	694-7	
P	B12	5,972,792	10/1999	Hudson	438	691	
P.	B13	6,010,964	1/2000	Glass	438	692	
h	B14	6,016,000	1/2000	Moslehi	257	522	
for	B15	6,042,996	3/2000	Lin et al.	430	317	
P	B16	4,193,226	3/1980	Gill, Jr. et al.	5/	124R	
P.	B17	4,811,522	3/1989	Gill, Jr.	17/	13/1	
P	B18	5,421,769	6/1995	Schultz et al.	45/	287	
	-	FORE	IGN PATEN	T DOCUMENTS			
EXAM.	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	- 54	OTHER ART (Inc	luding Author	, Title, Date, Pertinent	Pages, Etc.)		
L	B19	Malkoe et al., "Effect of R 2001, pp. 519-522.	etaining Ring Sy	stem on the Polishing of	300 mm Ox	ide-Wafers	," March

EXAMINER: Initial if citation considered whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)

L Number	Hits	Search Text	DB	Time stamp
1	838	dummy with (patterns or conductors)	USPAT;	2002/06/27 13:13
			US-PGPUB	
2	144	(USPAT;	2002/06/27 13:13
		dielectric and (trenches or grooves or	US-PGPUB	
		openings or holes)		
3	77	((dummy with (patterns or conductors))	USPAT;	2002/06/27 13:13
		and dielectric and (trenches or grooves	US-PGPUB	9 1
		or openings or holes)) and @ad<=19980831		
4	985	dummy with (patterns or conductors)	EPO; JPO;	2002/06/27 13:13
			DERWENT;	
			IBM TDB	
5	6	(dummy with (patterns or conductors)) and	EPO; JPO;	2002/06/27 13:14
		dielectric and (trenches or grooves or	DERWENT;	
		openings or holes)	IBM_TDB	

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CLIPPEDIMAGE= JP411265866A PAT-NO: JP411265866A DOCUMENT-IDENTIFIER: JP 11265866 A TITLE: PLANARIZATION OF DAMASCENE METALLIC CIRCUIT PATTERN PUBN-DATE: September 28, 1999 INVENTOR-INFORMATION: COUNTRY NAMÉ JASO, MARK A N/A SCHNABEL, RAINER F N/A ASSIGNEE-INFORMATION: NAME COUNTRY INTERNATL BUSINESS MACH CORP < IBM> N/A SIEMENS AG N/A APPL-NO: JP11005128 APPL-DATE: January 12, 1999 INT-CL (IPC): H01L021/304 ABSTRACT: PROBLEM TO BE SOLVED: To polish efficiently a work covered with a metal layer applying a damascene method by a method wherein a wafer covered with the metal layer is polished unit the metal layer is stopped leaving on the outside of a desired circuit **pattern** and the outside of an arbitrary dummy circuit pattern. SOLUTION: Opening parts 15a, 15b, 15c and 15d for interconnecting opening parts are formed in a silicon dioxide dielectric layer 14 laminated on a silicon substrate 13, a metal layer 16, which is extended from the surface of the layer 14 to the surface of the silicon wafer 13, is covered on the upper surface of the layer 14 and the opening parts 15a to 15d and dummy opening parts 20 are filled with the layer 16, but a metallization on the

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surface of a region 17 is evenly executed. The metallized wafer is placed on a chemical polishing machine using a well-know means and the layer 16 is removed up to the surface of the layer 14. The surface of the remaining layer 14, which is shown at the end parts 14a and 14b on both sides of the layer 14, is substantially formed horizontally extending over the whole region 17 of chips.

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DERWENT-ACC-NO: 2001-059432 DERWENT-WEEK: 200107 COPYRIGHT 1999 DERWENT INFORMATION LTD TITLE: CMP uniformity increasing method, obtaining consistent density and distribution of active regions on one chip INVENTOR: GUO, J; JIAN, S ; LI, T ; LIAU, W PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN] PRIORITY-DATA: 1998TW-0115165 (September 11, 1998) PATENT-FAMILY: PUB-NO PUB-DATE LANGUAGE MAIN-IPC PAGES TW 388932 A May 1, 2000 N/A 015 H01L 021/304 APPLICATION-DATA: PUB-NO APPL-DESCRIPTOR APPL-NO APPL-DATE TW 388932A 1998TW-0115165 N/A September 11, 1998 INT-CL (IPC): H01L021/304 ABSTRACTED-PUB-NO: TW 388932A BASIC-ABSTRACT: NOVELTY - Method comprises providing semiconductor substrate at least including first and second circuit regions. Separately forming plurality of trenches in circuit regions, trenches having various sizes in circuit regions. Separately forming dummy pattern on trenches having larger size through program analysis procedure, and forming dielectric layer covering substrate for planarization process by CMP. USE - A method of increasing the uniformity of chemical mechanical polishing

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(CMP).

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ADVANTAGE - Consistent density and distribution of active regions on one chip can be obtained

CHOSEN-DRAWING: Dwg.1a/2

TITLE-TERMS: CMP UNIFORM INCREASE METHOD OBTAIN CONSISTENT DENSITY DISTRIBUTE ACTIVE REGION ONE CHIP

DERWENT-CLASS: U11

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EPI-CODES: U11-C06A1A;

SECONDARY-ACC-NO: Non-CPI Secondary Accession Numbers: N2001-044317 DOCUMENT-IDENTIFIER: US 6093631 A TITLE: **Dummy patterns** for aluminum chemical polishing (CMP)

----- KWIC -----

APD: 19980115

TTL:

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Dummy patterns for aluminum chemical polishing (CMP)

ABPL:

A method and apparatus is provided for planarizing damascene metallic circuit **patterns** of a plurality of discrete integrated circuit chips on a metal coated silicon wafer wherein the circuitry on the chips on the wafer are either designed to be within a defined high metal density circuit range and low density metal circuit range and/or to provide dummy circuitry in the damascene process to provide a substantially uniform circuit density over the chip and the wafer surface. It is preferred that each chip on the surface of the wafer be divided into a plurality of regions and that each region be provided with dummy metallization, if necessary, to provide a relatively uniform circuit density in that region and consequently on the wafer surface. The invention also contemplates adding dummy circuitry to the periphery of the wafer in areas which are not formed into chips (chip fragments). The invention also provides semiconductor wafers made using the method and/or apparatus of the invention. BSPR: One method for forming the interconnects is to use a

damascene method wherein,

in general, a via or trench pattern is etched into a planar · **dielectric** layer

and then the pattern is filled by metal. Excess metal is typically applied and covers the upper surface of <u>dielectric</u>. The excess metal is then polished away to the patterned metal surface. As with other steps in the fabrication process, it is of extreme importance that the polished interconnect damascene layer be planar.

BSPR:

With regard to the semiconductor devices formed from the wafer, the devices typically include a plurality of interlayered circuits such as metal lines forming an integrated circuit which are interconnected by vias or interconnects between the layers. In the damascene process, metallization of the interconnects is performed by etching the desired circuitry in the **dielectric** layer down to the active region of the device. A thin layer of conductive metal is deposited by, for example, vacuum evaporation, sputtering or chemical vapor deposition (CVD) techniques, over the entire BSPR: Both single damascene structures and double damascene layers may be made by the same process and both processes require a CMP process to polish the wafer down to the surface of the interconnects and provide a planar surface. Unfortunately, problems such as dishing occur causing a non-planar surface. The dishing effect is particularly serious since the polishing needs to be carried out until the metal is cleared on the entire wafer, i.e., wherein the metal is left exclusively in previously etched lines without any metal on the surface of the **dielectric**. It has been found that a significant overpolish is typically needed which results in erosion of **dielectric** and dishing of metal as much as 100 nm below the level of the **dielectric** surface.

As a consequence, the thickness of the interconnects in overpolished areas is severely reduced resulting in an increased sheet resistance as compared to interconnects in other areas of the wafer and/or the individual integrated circuit device. Additionally, an uneven topography is introduced on the wafer surface after CMP which will be repeated with slight attenuation after subsequent deposition of dielectric layers problems at later steps in the fabrication process. BSPR: In areas of high pattern factor (HPF), e.g., 60% it has been found that the metal surface, after deposition, is lower than in areas of low pattern factor (LPF) areas, e.g., 20% due to mass conservation during the sputtering or other deposition process. As a consequence, during the CMP process, the metal above the dielectric is removed differently in HPF areas as compared to LPF areas. Since the polishing needs to be carried out until the patterned metal is cleared on the entire wafer leaving metal exclusively in previously etched lines, HPF areas generally experience a significant overpolish resulting in erosion of the dielectric and dishing of metal up to 100 nm below the level of the dielectric surface. As a result, the thickness or height of lines (interconnects) in HPF areas is thinner or shorter resulting in increased sheet resistance as compared to the thicker lines in LPF areas. BSPV: forming both the desired circuit pattern and any dummy circuit pattern as openings in a dielectric layer on each chip;

BSPV: coating the patterned **dielectric** layer with a layer of metal which metal fills

the openings forming the desired circuit pattern and any dummy circuit pattern and covers the surface of the wafer including the circuit patterns; and BSPV: polishing the metal coated wafer until no metal remains outside the desired and any dummy circuit patterns. DEPR: Referring now to FIGS. 11A-11D, the method of the invention of adding dummy metallization to a region of the chip is shown. In FIG. 11A, a silicon substrate 13 is shown having a silicon dioxide dielectric layer 14 thereon. In the dielectric layer 14 openings 15a, 15b, 15c and 15d are formed for interconnect openings and extend from the surface of layer 14 to the surface of silicon wafer 13. This configuration is similar to the configuration as shown in FIG. 3A. FIG. 11B shows the addition of dummy lines 20 which are the same as the addition of the dummy lines as shown in FIG. 3B. In FIG. 11C, a metal layer 16 is coated on top of **dielectric** layer 14 filling the **openings** 15a-15d and the dummy openings 20. The surfaces 16a and 16b of metal layer 16 at the opposed sides of region 17 are shown as being substantially horizontal (planar) indicating uniform metallization on the surface of region 17. The height of the openings in the dielectric layer 14 is shown as h. The metallized wafer of FIG. 11C is now chemical mechanically polished using conventional means to remove metal layer 16 down to the surface of dielectric 14. It can be seen that the remaining **dielectric** surface as indicated by opposed ends 14a and 14b is substantially horizontal over the region 17 of the chip. DEPR: FIGS. 11A-11D showing the method of the invention using

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dummy circuitry to provide a uniform metallized **dielectric** surface is to be contrasted with FIGS. 10A-10C which show a method of planarization of a damascene layer of the prior art. Thus, in FIG. 10A, a region 17 of the chip has a silicon substrate 13 and a dielectric layer 14 thereon. Openings having a height h are provided in the dielectric and are identified as 15a-15d. In FIG. 10B, a metal layer 16 is deposited on the surface of **dielectric** layer 14 filling the openings 15a-15d and covering the complete surface of the dielectric. Because of the conservation of mass, the metal 16 deposited on **dielectric** surface 14 will be uneven (non-planar) having a lower height shown as 16a compared to a higher level 16b. The lower level 16a is over the high pattern factor area including openings 15a, 15b and 15c as compared to the higher level 16b which is over a lower pattern factor area including only opening 15d. DEPR: The wafer of FIG. 10B is then chemically-mechanically polished resulting in removal of metal layer 16 down to the openings in dielectric layer 14. As can be seen in FIG. 10C, the height h' of the high pattern factor area shown as having **openings** 15a, 15b and 15c is lower than the height h of the low pattern factor area which only has opening 15d therein. DEPR: The above description has been directed to silicon wafers and the use of a silicon dioxide as the **dielectric**. It will be appreciated by those skilled in the art that any wafer material and **dielectric** material may suitably be used in

the method of the invention. Likewise, any metal may be used to metallize the damascene **openings** in the wafer surface with suitable

metals including aluminum, copper, tungsten and the like. Typically, the thickness of the metal layer above the surface of the **dielectric** is about 0.5 to 1 microns. CLPR: 6. The method of claim 1 wherein dummy circuit patterns or the setting of a maximum and/or minimum metal density are provided for chip fragments at the edge of the wafer. CLPV: forming both the desired circuit pattern and any dummy circuit pattern as openings in a dielectric layer on each chip; CLPV: coating the patterned **dielectric** layer with a layer of metal which metal fills the **openings** forming the desired circuit pattern and any dummy circuit pattern and covers the surface of the wafer including the circuit patterns; and

CLPV: polishing the metal coated wafer until no metal remains outside the desired and any **dummy** circuit **patterns**.

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UNT			UNITED STATES DEPARTM United States Patens and T Address COMMISSIONER OF P. Washington, D.C. 20231 www.uspin.gov	TENTS AND TRADEMARK
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
75	90 07/03/2002			
Conley, Rose	& Tayon		EXAMI	NER
P.O. Box 398 Austin, TX 78	767-0398		LEE, HSIE	N MING
			ART UNIT	PAPER NUMBER
			2823 DATE MAILED: 07/03/2002	1

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Page 161 of 329

· · · · · · · · · · · · · · · · · · ·	Application No.	Applicant(s)
-		
Office Action Summary	09/779,123	SETHURAMAN ET AL.
onice Action Summary	Examiner	Art Unit
The MAILING DATE of this communication	Hsien-Ming Lee	2823
Period for Reply	appears on the cover sheet with the t	
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO - Extensions of time may be available under the provisions of 37 CFI after SIX (6) MONTHS from the mailing date of this communication - If the period for reply specified above is less than thirty (30) days, a - If NO period for reply is specified above, the maximum statutory pe - Failure to reply within the set or extended period for reply will, by st - Any reply received by the Office later than three months after the m earned patent term adjustment. See 37 CFR 1.704(b). Status	N. R 1.136(a). In no event, however, may a reply be tir reply within the statutory minimum of thirty (30) day riod will apply and will expire SIX (6) MONTHS from atute, cause the application to become ABANDONE	nely filed /s will be considered timely. the mailing date of this communication. ED (35 U.S.C. § 133).
1) Responsive to communication(s) filed on (07 February 2001 .	
2a) This action is FINAL . 2b)	This action is non-final.	
3) Since this application is in condition for all	owance except for formal matters, p	rosecution as to the merits is
closed in accordance with the practice und Disposition of Claims		
4)⊠ Claim(s) <u>1-22</u> is/are pending in the applica	tion.	
4a) Of the above claim(s) is/are with		
5) Claim(s) is/are allowed.		
6)⊠ Claim(s) <u>1-22</u> is/are rejected.		
7) Claim(s) is/are objected to.		
8) Claim(s) are subject to restriction an	d/or election requirement.	
Application Papers	• • • •	
9) The specification is objected to by the Exam	iner.	
10)⊠ The drawing(s) filed on <u>07 February 2001</u> is	/are: a)□ accepted or b)⊠ objected to	by the Examiner.
Applicant may not request that any objection to	o the drawing(s) be held in abeyance. S	ee 37 CFR 1.85(a).
11) The proposed drawing correction filed on	is: a) 🗌 approved b) 🔲 disappro	oved by the Examiner.
If approved, corrected drawings are required in	reply to this Office action.	
12) The oath or declaration is objected to by the	Examiner.	
Priority under 35 U.S.C. §§ 119 and 120		
13) Acknowledgment is made of a claim for fore	eign priority under 35 U.S.C. § 119(a	a)-(d) or (f).
a) All b) Some * c) None of:		
1. Certified copies of the priority docum	ents have been received.	
2. Certified copies of the priority docum	ents have been received in Applicati	on No
3. Copies of the certified copies of the p application from the International * See the attached detailed Office action for a	Bureau (PCT Rule 17.2(a)).	-
14) Acknowledgment is made of a claim for dome	estic priority under 35 U.S.C. § 119(e	e) (to a provisional application).
a) The translation of the foreign language 15) Acknowledgment is made of a claim for dom		
Attachment(s)	p	
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Notice of Disclosure Statement(s) (PTO-1449) Paper Note 	5) 🔲 Notice of Informal I	/ (PTO-413) Paper No(s) Patent Application (PTO-152)
I.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Office	e Action Summary	Part of Paper No. 6

DETAILED ACTION

Drawings

1. Figures 1-4 should be designated by a legend such as --Prior Art--. Particularly, the brief description of drawings indicates that they are from the conventional techniques. See MPEP § 608.02(g).

Claim Objections

2. Claims 2-8, 10-16, 18-20 are objected to because the lines are too closely together, making reading and entry of amendments difficult. Substitute claims with lines one and one-half or double spaced on good quality paper are required. See 37 CFR 1.52(b).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, at lines 10-11, the limitation " from of electrically conductive features of an ensuring integrated circuit" is not well understood.

5. Claim 2, at line 18 and claim 10, at line 22 recites the limitation "said group consisting of

." Claim 7, at line 37 and claim 15, at line 3 recites the limitation "**the** group consisting of ." There is insufficient antecedent basis for the limitation in the respective claim.

6. Claim 1, at line 9; claim 3, at line 22; claim 11, at line 26 and claim 17, at line 9, recite the limitation "said wide and narrow trench." There is insufficient antecedent basis for the limitation in the respective claim because "relatively wide" (e.g. claim 1, line 4) is <u>not</u> equal to "wide" (claim 1, line 9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

 Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaso et al. (US 6,093,631) in view of applicants' admitted prior art (AAPA), including pages 1-6 and Figs.
 1-4.

With respect claims 1, 3, 9, 11, 17, 21 and 22, Jaso et al. teach a method, comprising:

- etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14 between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);
- filling the dummy trenches 20 and the first 15d and the series of second trenches 15a/15b/15c with a conductive material 16 (Fig. 11C); and
- polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c, wherein the dummy conductor are electrically separate from the plurality of electrically conductive features and co-planar with the interconnect.

Jaso et al. do not teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches. AAPA, however, in an analogous art teaches forming a relatively wide trench 24, a series of relatively narrow trenches 22 (Fig. 2); filling the relatively wide trench 24 and the series of relatively narrow trenches 22 with a conductive material 28 (Fig. 3); polishing the conductive material 16 to form conductors in the series of relatively narrow

trenches 22 and interconnect in the relatively wide trench 24, wherein a common dishing problem occurs at the upper surfaces of the conductors and the interconnect due to the presence of a dense material (dielectric layer 20) between the conductors and the interconnect.

Therefore, at the time of the invention was made, one artisan in the art would have been motivated to apply the method of Jaso et al. to solve the dishing problem as demonstrated by AAPA, wherein the relatively wide trench 24 of AAPA can be treated as the first trench 15d of Jaso et al. and relatively narrow trenches 22 can be treated as the second trenches 15a/15b/15c of Jaso et al. The motivation/suggestions by doing so would be to apply the method of Jaso et al. to solve the <u>dishing</u> problem after polishing the conductors (narrow ones), the interconnect (wide one) and the dielectric layer existing between the conductors and the interconnect as shown in AAPA, i.e. to make the upper surfaces of conductors, the interconnect and the dielectric layer to be substantially <u>coplanar</u> as shown in Fig. 11D of Jaso et al.

Regarding claims 2, 10, 19 and 20, Jaso et al. teach that the conductive material comprises a metal , which can be a conventional metal such as Al, W, Ta or Ti, as evidenced by AAPA (page 3, lines 24-25).

Regarding claims 4, 12 and 18, the combination of Jaso et al. and AAPA teaches the polishing resulting in dummy dielectric protrusions between adjacent pairs of the dummy trenches, the dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of the dummy conductors.

Regarding claims 5-8, 13-16, Jaso et al. teach that the polishing comprises applying a polishing solution; applying an abrasive polishing surface to upper surface of the conductive material while moving the abrasive polishing surface relative to the upper surface, wherein the

abrasive polishing surface comprises particles partially fixed into a polymer-based matrix and the particles comprises aluminum oxide or silicon dioxide (col. 1, lines 37-61).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee June 27, 2002

SUPERVISORY PRIMARY EXTERNAL TECHNOLOGY CENTER

Notice of References Cit d	Application/Control No.	Applicant(s)/Pater Reexamination SETHURAMAN E	
Notice of References Cit u	Examiner	Art Unit	
	Hsien-Ming Lee	2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	А	US-6,093,631	07-2000	Jaso et al.	438/618
	в	US-			
	с	US-			
	D	US-			
	Е	US-			
1	F	US-			
	G	US-			
	н	US-			
	1	US-			
	L	US-			
	к	US-			
	L	US-			
	м	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	x	

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)

Notice of References Cited

002	IN THE UNITED STATES PA	FENT	S298-02502/PM9801
Di re l	Application of:	ş	Group Art Unit: 2823
0e.	Sethuraman et al.	§	
Serial	No. 09/779,123	00 00	Atty. Dkt. No. 5298-02502
Filed:	February 7, 2001	200 00	CERTIFICATE OF TRANSMISSION 37 C.F.R. § 1.8
For:	PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCOONNECT	00 000 000 000 00	I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below:

REQUEST FOR APPROVAL OF DRAWING CHANGES UNDER 37 C.F.R. §1.121

Box Non-Fee Amendment Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. §1.121 (d), it is respectfully requested that the changes shown in red in the attached drawings be approved by the Examiner in the above-referenced case. The notation "Related Art" has been added to FIGS. 1-4. Support for these changes can be found within the Specification, for example, on pages 2-5. No new elements have been added to the drawings by these changes. Accordingly, these changes do not present new matter.

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ctfully submitted, Res

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicant(s)

Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, TX 78767-0398 Ph: (512) 476-1400 Date: <u>October 3, 2002</u> AMM



(Related Art)

SAMSUNG EXHIBIT 1004 Samsung v. Invensas

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FIG. 6



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C'10			#8/3
2002			5298-02502/PM980196
ADEMAIT	NUTHE INTER OT ATTEC DA	TENT	
	IN THE UNITED STATES PA	TENT	AND TRADEMARK OFFICE Group Art Unit: 2823 Examiner: Lee, H. Atty. Dkt. No. 5298-02502
In re Application of:		ş	Group Art Unit: 2823
	Sethuraman et al.	ş	Examiner: Lee, H. E S O
		ş	ER
Serial No. 09/779,123		ş	Atty. Dkt. No. 5298-02502
		ş	
Filed:	February 07, 2001	ş	I hereby certify that this correspondence is being deposited
-		ş	with the U.S. Postal Service with sufficient postage as First Class
For:	A PLANARIZED SEMICONDUCTOR	ş	Mail in an envelope addressed to: Box: Non-Fee Amendment,
	INTERCONNECT TOPOGRAPHY	8	Commissioner for Patents, Washington, D.C. 20231, on the dr 3 indicated below:
	AND METHOD FOR POLISHING A	ş	
	METAL LAYER TO FORM	ş	VIIIN C
			October 3, 2002

AMENDMENT; RESPONSE TO OFFICE ACTION MAILED JULY 3, 2002

Commissioner for Patents Washington, D.C. 20231

Dear Sir/ Madam:

This paper is submitted in response to the Office Action mailed July 3, 2002 to further highlight reasons why the application is in condition for allowance.

Please amend the case as follows:

In the Claims:

Please replace claims 1-3, 10-11, and 17 with the amended claims below. A "marked-up" version of each amendment is included in Attachment A.

SN 09/779,123 Response to Office Action dated 7/3/02

Page 1 of 11

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1. (Twice Amended) A method, comprising:



etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;



polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

2. (Amended) The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Amended) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

10. (Amended) The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Amended) The method of claim, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

17. (Twice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

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conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

REMARKS

Claims 1-3, 10-11, and 17 have been amended. Claims 1-22 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Objections to the Drawings:

FIGS. 1-4 of the Drawings were objected to for failing to denote that only that which is old in the art is illustrated. The objection has been obviated by the amendments to the Drawings presented in the accompanying Request for Approval of Drawing Changes. For example, the addition of the designation "(Related Art)" obviates the objection to the Drawings under MPEP §608.02(g). The intent of MPEP §608.02(g) is to ensure that Drawings depicting unclaimed subject matter may be distinguished from Drawings depicting embodiments of the claimed invention. For example, MPEP §608.02(g) only requires the addition of a legend "such as 'Prior Art'." (Emphasis added.) Since the addition of the legend "(Related Art)" serves to distinguish those Figures representing unclaimed subject matter (e.g., FIGS. 1-4) from the other Figures in the application, the amendments to the Drawings satisfy MPEP §608.02(g). It is submitted that this objection has now been overcome.

Objections to the Claims:

Claims 2-8, 10-16, and 18-20 were objected to because the lines are too closely together. A copy of all claims in the case, incorporating all amendments, with lines one and one-half spaced on good quality paper as required under 37 CFR 1.52(b) is included in Attachment A. Therefore, removal of the objections to claims 2-8, 10-16, and 18-20 is respectfully requested.

Section 112, 2nd Paragraph, Rejections:

Claims 1, 2, 3, 7, 10, 11, 15, and 17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Claims 1, 2, 3, 10, 11, and 17 have been amended. These amendments are believed to clarify the claim language in a manner that addresses the concerns about those claims expressed in the Office Action.

Claims 2 and 10 have been amended for consistency with accepted Markush claim practice (see MPEP § 2173.05(h)). As the Examiner will note from MPEP § 2173.05(h), claims 7 and 15 were filed in accordance with accepted Markush claim practice. Accordingly, removal of the § 112, second paragraph, rejection of claims 1, 2, 3, 7, 10, 11, 15, and 17 is respectfully requested.

Section 103 Rejections:

Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (hereinafter "Jaso") in view of pages 1-6 of Applicant's Specification and Figs. 1-4 of Applicant's Drawings. As set forth in more detail below, the rejections of claims 1-22 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond*, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches. Amended independent claim 1 recites in part: "[a] method, comprising: etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches." Independent claims 9 and 17 recite a similar limitation.

Jaso discloses a method and apparatus for planarizing damascene metallic circuit patterns. Jaso, however, does not teach or suggest etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches. As stated in the Office

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Action, "Jaso et al. do not teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches." (Office Action -- page 3). Therefore, Jaso cannot teach or suggest etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches, as recited in claim 1.

Pages 1-6 and Figs. 1-4 of Applicant's disclosure are not available as prior art against the Claims in this case. When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejection. *In re Nomiya*, 509 F.2d 566, 184 USPQ 607, 610 (CCPA 1975). MPEP § 2129. Neither Applicant nor Applicant's representative has ever stated or "admitted" that pages 1-6 and Figs. 1-4 of Applicant's disclosure are prior art. The text on these pages and Figs. 1-4 were included in the Related Art section because Applicant did not intend to claim this subject matter. There is no evidence on record that pages 1-6 and Figs. 1-4 of Applicant's disclosure are actually prior art to the claims. Therefore, pages 1-6 and Figs. 1-4 of Applicant's disclosure cannot be used in an obviousness rejection against the claims in the case.

Hypothetically speaking, even if the text on pages 1-6 and Figs. 1-4 of Applicant's disclosure were contained in a document that is available as prior art against the claims in this case, the text on pages 1-6 and Figs. 1-4 cannot be properly considered as prior art. For example, as stated in the Specification, "FIGS. 2-4 illustrate a typical damascene process and the localized thinning or "dishing" problem experienced by conventional metal CMP processes." (Specification -- page 3, lines 17-19). Therefore, pages 1-6 and Figs. 1-4 of Applicant's disclosure present a problem with metal CMP processes (i.e., localized thinning or dishing). This disclosure of the problem in pages 1-6 and Figs. 1-4, however, does not constitute a "nonpreferred embodiment" of the disclosure that may be properly considered as prior art. An example of a non-preferred embodiment may be an "unattractive" method of etching dummy trenches or an "unattractive" spacing of dummy trenches. In contrast, dummy trenches are not even mentioned in the "Description of the Related Art" on pages 1-6 or illustrated in Figs. 1-4 of Applicant's disclosure.

Assuming, for the sake of argument, that pages 1-6 and Figs. 1-4 of Applicant's disclosure are available as prior art against the claims, pages 1-6 and Figs. 1-4 of Applicant's disclosure do not disclose etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches, as recited in claim 1. Therefore, since neither Jaso nor pages 1-6 and Figs. 1-4 of Applicant's disclosure teach or suggest all limitations of claim 1, the

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combination of Jaso and pages 1-6 and Figs. 1-4 of Applicant's disclosure also does not teach or suggest all limitations of claim 1.

The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious <u>unless the prior art also suggests the desirability of the combination</u>. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). MPEP 2143.01.

Even if the cited art can be modified, as suggested by the Office Action, the resultant modifications are not obvious because the prior art does not suggest the desirability of the modifications. For example, Jaso states that "it is one aspect of the invention to decrease the difference in pattern factor across the chip surface by providing a uniform metal density (pattern factor) across the surface of the chip and, concomitantly, of the wafer." (Jaso -- col. 3, lines 34-37). In addition, Jaso states that "the pattern factor for a particular area or region may be defined as the area covered by the metal divided by the total area of the particular area or region." (Jaso - col. 3, lines 7-10). Therefore, if the definition of pattern factor disclosed by Jaso is applied to Figs. 2-4 of Applicant's disclosure, then a pattern factor for a first area containing <u>narrow trenches</u> 22 and a second area containing wide trench 24 would be approximately the same according to Jaso. Jaso also states that "to overcome the dishing effect and other nonplanarization, the invention decreases the differences in pattern factors for regions on the chip." (Jaso -col. 3, lines 29-31). Jaso further states that "in another preferred aspect of the invention, the lower pattern factor design limit can be artificially generated for any given region on the chip or wafer surface by using a dummy circuit design." (Jaso -- col. 3, lines 57-60). As such, Jaso teaches that because the two areas of Figs. 2-4 of Applicant's disclosure have approximately equal pattern factors, these areas would not suffer from the dishing effect and other non-planarization. Consequently, Jaso teaches that there would be no need for including a dummy circuit design in either area of Figs. 2-4. Jaso, therefore, does not teach, suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of Applicant's disclosure. In addition, pages 1-6 and Figs. 1-4 of Applicant's disclosure do not teach, suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in either area of the semiconductor topography illustrated in Figs. 2-4. Therefore, none of the cited art, alone or in combination, suggests the desirability of the modifications proposed in the Office Action. As such, the modifications proposed by the Office Action are not obvious.

For at least the reasons stated above, none of the cited art teaches or suggests the limitations of claims 1, 9, and 17. Therefore, claims 1, 9, and 17, and claims dependent therefrom, are patentably

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distinct over the cited art. Accordingly, removal of the § 103(a) rejections of claims 1-22 is respectfully requested.

NOTICE OF CHANGE OF ATTORNEY DOCKET NUMBER

The Commissioner is requested to change the attorney docket number for the above-identified patent application as set forth below.

Old Number:	5298-02501	
New Number:	5298-02502	

CONCLUSION

In this response, claims 1-3, 10-11, and 17 have been amended. Rejections of claims 1-22 have been addressed. Therefore, this response constitutes a complete response to all of the issues raised in the Office Action mailed July 3, 2002. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-22 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

The Commissioner is authorized to charge any required fees or credit any overpayment to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-02502.

Respectfully submitted,

Kevin L. Daffer Reg. No. 34,146 Attorney for Applicants

Conley, Rose & Tayon, P.C. P.O. Box 398 Austin, TX 78767-0398 Ph: (512) 476-1400 Date: <u>October 3, 2002</u> AMM

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ATTACHMENT A "Marked-Up" Amendments

IN THE CLAIMS:

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Please amend claims 1-3, 10-11, and 17 as follows:

1. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide [trenches] trench, wherein said dummy conductors are electrically separate from [of] electrically conductive features of an ensuing integrated circuit.

2. (Amended) The method of claim 1, wherein said conductive material comprises a metal selected from [said] the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Amended) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [wide and] series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

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6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

A method, comprising:

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etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

10. (Amended) The method of claim 9, wherein said conductive material comprises a metal selected from [said] the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [wide and narrow] said trench and said series of trenches.

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12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

17. (Twice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said <u>series of relatively</u> narrow [and wide] trenches <u>and said relatively wide</u> <u>trench</u>, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

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18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

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L Number	Hits	Search Text		Time stamp
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1	1	("6232231").PN.	USPAT; US-PGPUB	2002/12/28 10:39
2	73	(narrow with trench) and (wide with trench) and (trench with conductive)	USPAT; US-PGPUB	2002/12/28 10:44
3	2	(narrow with trench) and (wide with trench) and (trench with conductive)	EPO; JPO; DERWENT; IBM TDB	2002/12/28 10:45

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			UNITED STATES DEFARTM United States Patent and Tr. Address COMMISSIONER OF PA Washington, D.C. 20221 www.uepto.gov	ademark Office
PPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
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Conley, Rose	& Tayon		EXAMIN	JER
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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	,	Application No.	Applicant(s)
•		09/779,123	SETHURAMAN ET AL.
	Office Action Summary	Examiner	Art Unit
		Hsien-Ming Lee	2823
	The MAILING DATE of this communication		
Period fo			
THE - Exte after - If the - If NC - Failt - Any	ORTENED STATUTORY PERIOD FOR R MAILING DATE OF THIS COMMUNICATI ensions of time may be available under the provisions of 37 C r SIX (6) MONTHS from the mailing date of this communication a period for reply specified above is less than thirty (30) days, D peniod for reply is specified above, the maximum statutory p ure to reply within the set or extended period for reply will, by reply received by the Office later than three months after the ed patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no event, however, may a on. a reply within the statutory minimum of thin period will apply and will expire SIX (6) MOI statute, cause the application to become A	reply be timely filed rty (30) days will be considered timely. NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).
1)⊠	Responsive to communication(s) filed on	08 October 2002 .	
2a)⊠	This action is FINAL . 2b)	This action is non-final.	
3) Disposit	Since this application is in condition for a closed in accordance with the practice un ion of Claims		
4)🖂	Claim(s) 1-22 is/are pending in the applic	ation.	
	4a) Of the above claim(s) is/are with	hdrawn from consideration.	
5)	Claim(s) is/are allowed.		
6)🖂	Claim(s) <u>1-22</u> is/are rejected.		
7)	Claim(s) is/are objected to.		
8)	Claim(s) are subject to restriction a	nd/or election requirement.	
Applicat	ion Papers		
	The specification is objected to by the Example 1		
10)	The drawing(s) filed on is/are: a)□ a		
	Applicant may not request that any objection	- · · ·	
4 4 57		18 Optobor 2002 is: $21 Y $ oppre	oved b) disapproved by the Examin
11) 🛛	The proposed drawing correction filed on <u>0</u>		
	If approved, corrected drawings are required	in reply to this Office action.	
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12) ☐ Priority (13) ☐ a) (* 5 14) ☐ A a	If approved, corrected drawings are required The oath or declaration is objected to by the under 35 U.S.C. §§ 119 and 120 Acknowledgment is made of a claim for fo All b) Some * c) None of: 1. Certified copies of the priority docur 2. Certified copies of the priority docur 3. Copies of the certified copies of the application from the International See the attached detailed Office action for a Acknowledgment is made of a claim for dom Acknowledgment is made of a claim for dom	in reply to this Office action. le Examiner. breign priority under 35 U.S.C. ments have been received. ments have been received in A priority documents have been al Bureau (PCT Rule 17.2(a)). a list of the certified copies not mestic priority under 35 U.S.C. e provisional application has b	§ 119(a)-(d) or (f). Application No received in this National Stage received. § 119(e) (to a provisional applicatione en received.

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DETAILED ACTION

1. The objection to drawings, to claims 2-8, 10-16, 18-20 and 112-second-paragraph

rejection to claims 1, 2, 3, 7, 10, 11, 15 and 17 are withdrawn in response to applicants' amendment filed 10/8/02.

2. Claims 1-22 are pending in the application.

3. Corrected drawings submitted on 10/8/02 are approved by the examiner.

Grounds of Rejection

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaso et al.

(US 6,093,631) in view of applicants' admitted prior art (AAPA), including pages 1-6 and Figs.

1-4.

With respect claims 1, 3, 9, 11, 17, 21 and 22, Jaso et al. teach a method, comprising:

- etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14 between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);
- filling the dummy trenches 20 and the first 15d and the series of second trenches

15a/15b/15c with a conductive material 16 (Fig. 11C); and

polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c, wherein the dummy conductor are electrically separate from the plurality of electrically conductive features and co-planar with the interconnect.

Jaso et al. do not teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches. AAPA, however, in an analogous art teaches forming a relatively wide trench 24, a series of relatively narrow trenches 22 (Fig. 2); filling the relatively wide trench 24 and the series of relatively narrow trenches 22 with a conductive material 28 (Fig. 3); polishing the conductive material 16 to form conductors in the series of relatively narrow trenches 22 and interconnect in the relatively wide trench 24, wherein a common dishing problem occurs at the upper surfaces of the conductors and the interconnect due to the presence of a dense material (dielectric layer 20) between the conductors and the interconnect.

Therefore, at the time of the invention was made, one artisan in the art would have been motivated to apply the method of Jaso et al. to solve the dishing problem as demonstrated by AAPA, wherein the relatively wide trench 24 of AAPA can be treated as the first trench 15d of Jaso et al. and relatively narrow trenches 22 can be treated as the second trenches 15a/15b/15c of Jaso et al. The motivation/suggestions by doing so would be to apply the method of Jaso et al. to solve the <u>dishing</u> problem after polishing the conductors (narrow ones), the interconnect (wide one) and the dielectric layer existing between the conductors and the interconnect as shown in AAPA, i.e. to make the upper surfaces of conductors, the interconnect and the dielectric layer to be substantially <u>coplanar</u> as shown in Fig. 11D of Jaso et al.

Regarding claims 2, 10, 19 and 20, Jaso et al. teach that the conductive material comprises a metal , which can be a conventional metal such as Al, W, Ta or Ti, as evidenced by AAPA (page 3, lines 24-25).

Regarding claims 4, 12 and 18, the combination of Jaso et al. and AAPA teaches the polishing resulting in dummy dielectric protrusions between adjacent pairs of the dummy trenches, the dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of the dummy conductors.

Regarding claims 5-8, 13-16, Jaso et al. teach that the polishing comprises applying a polishing solution; applying an abrasive polishing surface to upper surface of the conductive material while moving the abrasive polishing surface relative to the upper surface, wherein the abrasive polishing surface comprises particles partially fixed into a polymer-based matrix and the particles comprises aluminum oxide or silicon dioxide (col. 1, lines 37-61).

Response to Arguments

6. Applicant's arguments filed 10/8/02 have been fully considered but they are not persuasive because of the reasons as follow.

Applicant' argument is on the ground that Figs.1-4 and related text ("AAPA") described in the present application is not prior art; and there is no desirability for modifying Jaso teachings with AAPA.

Applicant argues that neither applicant nor applicant's representative has ever stated or admitted that pages 1-6 and Figs.1-4 of applicant's disclosure are prior art. (second paragraph) This argument is not convincing.

In response to the denial of the prior art, the description of the drawings expressly states " Fig.2 depicts a partial cross-sectional view of a **conventional** semiconductor topography" (**page 10**); and "Fig. 4 depicts a partial cross-sectional view using a **conventional** CMP technique, thereby forming a topological surface having elevational disparities;" (**page 10**); and " in FIG.1, a **typical** chemical-mechanical polishing (**page 2**, **line 11**). Accordingly, it would have been obvious to one of the ordinary skill in the art to appreciate that the conventional and typical techniques taught in Figs. 1-4 and related text are the **common knowledge** generally available to one of ordinary skill in the art **before** the filing date of the present application, i.e. prior art.

Applicant further argues that Jaso does not teach or suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of application's disclosure. (third paragraph, page 6)

Contrary to the argument, Jaso **does** suggest the motivation to modify the teachings to apply in the situation demonstrated in Figs. 2-4 of application's disclosure. In particular, Jaso suggest that " in another aspect of the invention, a method is provided to set a predetermined high pattern factor designed limit of say 60-90%, preferably 70-80%. Using this method, the difference between the high pattern factor areas and the low pattern factor areas is minimized." (see **col. 3, lines 38-42**) Jaso further suggest that using a dummy circuit pattern layout in the invention would minimize the difference circuit density over the chip and wafer surface and provide a uniform metal surface after CMP. (col.3, lines 61-64). In other words, Jaso **inherently teaches or suggests** that by using the invention the dishing effect as shown in AAPA can be minimized between "a relatively narrow trenches", which is corresponding to the " low pattern

factor areas" and "a relatively wide trenches", which is corresponding to the "high pattern factor areas.' The pattern factor, according to Jaso, is defined by the area covered by the metal (i.e. conductive material) divided by the total area of the particular area or region. (col.3, lines 3-13) That is to say that Jaso's method would minimize the pattern factor difference as stated above but the difference **does** exist.

Therefore, at the time of the invention was made, one of the ordinary skill in the art would have been motivated to apply the method of Jaso et al. to solve the dishing problem as demonstrated by AAPA by including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of application's disclosure.

Therefore, the 103(a) rejection as set forth in the previous Office action in view of the amendment filed 10/8/02 is deemed proper.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ien Ming Lee

December 28, 2002

George Fourson **Primary Examiner** 2827

E .	REFLY UNDER 37 C.F.R ST. ACK EXPEDITED PROCEDURE EXAMINING GROUP 28/3
1 2003 IN THE UNITED STATES PATE	5298-02502/PM980195
In re Application of:	Group Art Unit: 2823
Sethuraman et al.	Examiner: Lee, H.
Serial No. 09/779,123	Atty. Dkt. No. 5298-02502
Filed: February 7, 2001	I hereby certify that this correspondence is being forwarded
For: A PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT	the date indicated below:

AMENDMENT; RESPONSE AFTER FINAL REJECTION PURSUANT TO 37 CFR § 1.116

Box AF Commissioner for Patents Washington, D.C. 20231

Dear Sir/Madam:

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IL RO	2003	VED

This paper is submitted in response to the Office Action mailed December 31, 200 to further highlight reasons why the application is in condition for allowance.

Please amend the case as follows.

IN THE CLAIMS

Please cancel claims 5, 6, 13, 14 and 16 without prejudice or disclaimer as to the subject matter recited therein. Please replace claims 1, 7, 9, 11, 15, and 17 with the amended claims below. A "marked-up" version of each amendment is included in **Attachment A**.

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1. (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

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filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

7. (Amended) The method of claim 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

9. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

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15. (Amended) The method of claim 9, wherein said abrasive polishing surface comprises particles at
least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected
from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium
oxide, chromium oxide, and zirconium oxide.

17. (Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims:

23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.

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REMARKS

To expedite prosecution, claims 5, 6, 13, 14, and 16 have been canceled; claims 1, 7, 9, 11, 15, and 17 have been amended; claims 23-25 have been added. Thus, claims 1-4, 7-12, 15, and 17-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 103 Rejections

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Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (hereinafter "Jaso") in view of pages 1-6 of Applicant's Specification and Figs. 1-4 of Applicant's Drawings (hereinafter "Applicant's Background Disclosure"). To expedite prosecution, claims 5, 6, 13, 14 and 16 have been canceled, thereby rendering their rejections moot. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond*, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below. Accordingly, removal of the § 103(a) rejection of claims 1-22 is respectfully requested.

None of the cited art teaches or suggests polishing a conductive material to form dummy conductors between a relatively wide interconnect feature and a series relatively narrow interconnect features by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material. Amended claim 1 recites, in part:

A method, comprising: etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches; filling said trenches with a conductive material; and polishing said conductive material to form dummy conductors in said dummy trenches, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

Amended claim 9 includes a similar limitation. Support for the amendments to claims 1 and 9 may be found, for example, on page 8, lines 14-17 of the Specification, "In an alternate embodiment, a "fixed-abrasive" technique is used to polish the conductive material. The fixed-abrasive technique involves

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placing a liquid which is substantially free of particulate matter between the surface of the conductive material and an abrasive polishing surface of a polishing pad."

Neither Jaso nor the Applicant's Background Disclosure teaches or suggests polishing a topography using fixed abrasive techniques to form dummy structures therein. More specifically, neither Jaso nor the Applicant's Background Disclosure teaches or suggests polishing a conductive material to form dummy conductors between a relatively wide interconnect feature and a series relatively narrow interconnect features by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material as recited in the presently claimed case. On the contrary, Jaso and the Applicant's Background Disclosure restrict their discussions of polishing to techniques which include applying an abrasive chemical slurry between a polishing pad and a topography. There is no discussion within Jaso or the Applicant's Background Disclosure of using a polishing pad with abrasive particles embedded therein or a polishing solution which is substantially absent of particulate matter. In fact, Jaso specifically teaches that, "... the chemical-mechanical planarization (CMP) process involves pressing a semiconductor wafer against a moving polishing surface that is wetted with a chemically reactive, abrasive slurry ... The polishing surfaces typically are a planar pad made of a relatively soft, porous material ..." (Emphasis added. Jaso, column 1, lines 40-46). Since none of the cited art teaches or suggests the limitations of claims 1 and 9, none of the cited can provide any motivation to teach the limitations of claims 1 and 9. As such, claims 1 and 9 are asserted to be patentably distinct over the cited art.

None of the cited art teaches or suggests a semiconductor topography with a plurality of laterally spaced dummy trenches between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches. Amended claim 17 recites, in part:

A substantially planar semiconductor topography, comprising: a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches ...

Support for the amendment to claim 17 may be found, for example, on page 13, lines 17-19, "... dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have submicron widths, and the wide trench 54 is preferably greater than 50 microns in width."

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A. 8.2

As noted in the Office Action and in a response to a previous Office Action mailed July 3, 2002, Jaso does not disclose a topography with dummy trenches interposed between a relatively wide trench and a series of relatively narrow trenches. As such, Jaso cannot teach or suggest a topography with a dummy trench having a lateral dimension which is less than a lateral dimension of an adjacent relatively wide trench and greater than a lateral dimension of an adjacent series of relatively narrow trenches as recited in claim 17. Moreover, the Applicant's Background Disclosure does not even disclose a topography with a dummy trench, much less a topography with a dummy trench having a lateral dimension of trenches arranged adjacent to the dummy trench. Consequently, the Applicant's Background Disclosure can neither teach a topography with the limitations of claim 17 nor be combined with Jaso to teach a topography with such limitations. Since none of the cited art teaches or suggests the limitations of claim 17, none of the cited can provide any motivation to teach the limitations of claim 17. As such, claim 17 is asserted to be patentably distinct over the cited art.

Patentability of Added Claims

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The present Amendment adds claims 23-25. Claims 23-25 are dependent from base claim 17 and, therefore, are patentably distinct over the cited art for at least the same reasons as that claim. Accordingly, allowance of added claims 23-25 is respectfully requested.

NOTICE OF CHANGE OF ATTORNEY DOCKET NUMBER

The Commissioner is requested to change the attorney docket number for the above-identified patent application as set forth below.

Old Number: New Number: 5298-02501 5298-02502

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CONCLUSION

This response constitutes a complete response to all issues raised in the final Office Action mailed December 17, 2002. In view of the remarks traversing rejections presented therein, Applicants assert that pending claims 1-4, 7-12, 15, and 17-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

ectfully submitted, Re Kevin L. Daffer

Reg. No. 34,146 Attorney for Applicant(s)

Conley Rose, P.C. P.O. Box 684908 Austin, TX 78768-4908 Ph: (512) 476-1400 Date: January 31, 2003 MEL

SN 09/779,123 Response to Final Office Action mailed December 31, 2002

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SAMSUNG EXHIBIT 1004 Samsung v. Invensas

ATTACHMENT A "Marked-Up" Amendments

IN THE CLAIMS

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Please cancel claims 5, 6, 13, 14, and 16. Please amend claims 1, 7, 9, 11, 15, and 17 as follows. Also following is list of all remaining pending claims.

1. (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. (Canceled)

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6. (Canceled)

. . .

7. (Amended) The method of claim [5] $\underline{1}$, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [said] trench and said series of trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

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14. (Canceled)

15. (Amended) The method of claim [13] 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

Please add the following claims:

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23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.

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UNITED STATES EPARTMENT OF COMMERCE Patent and Trademark Office Change ASSISTANT SECRETARY AND COMMISSIONER #12 ai Address OF PATENTS AND TRADEMARKS Washington, D.C. 20231 3-24-03 2 estates 2600 inkil 11

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CHANGE OF ADDRESS/POWER OF ATTORNEY

FILE LOCATION 28C1 SERIAL NUMBER 09779123 PATENT NUMBER THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 35617 THE PRACTITIONERS OF RECORD HAVE BEEN CHANGED TO CUSTOMER # 35617 THE FEE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 35617 ON 02/07/03 THE ADDRESS OF RECORD FOR CUSTOMER NUMBER 35617 IS:

> CONLEY ROSE, P.C. P.O. BOX 684908 AUSTIN TX 78768

AND THE PRACTITIONERS OF RECORD FOR CUSTOMER NUMBER 35617 ARE: 34146 36609 44366 44800 45093 48405 50484

> PTO INSTRUCTIONS: PLEASE TAKE THE FOLLOWING ACTION WHEN THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER NUMBER: RECORD, ON THE NEXT AVAILABLE CONTENTS LINE OF THE FILE JACKET, ADDRESS CHANGE TO CUSTOMER NUMBER'. LINE THROUGH THE OLD ADDRESS ON THE FILE JACKET LABEL AND ENTER ONLY THE 'CUSTOMER NUMBER' AS THE NEW ADDRESS. FILE THIS LETTER IN THE FILE JACKET. WHEN ABOVE CHANGES ARE ONLY TO FEE ADDRESS AND/OR PRACTITIONERS OF RECORD, FILE LETTER IN THE FILE JACKET. THIS FILE IS ASSIGNED TO GAU 2823.

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Page 202 of 329

			UNITED STATES DEFARTM United States Patent and Tr Addrews COMMISSIONER OF PA Washington, D.C. 20221 www.nepto.gov	ademark Office
PPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
35617 7	590 03/19/2003			
CONLEY RO			EXAMI	NER
P.O. BOX 6849 AUSTIN, TX	- (*)		LEE, HSIE	N MING
			ART UNIT	PAPER NUMBER
			2823	

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Page 203 of 329

SAMSUNG EXHIBIT 1004 Samsung v. Invensas

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		Uni
	Application No.	Applicant(s)
Advisory Action	09/779,123	SETHURAMAN ET AL.
-	Examiner	Art Unit
	Hsien-Ming Lee	2823
The MAILING DATE of this communication ap	pears on the cover she t with the	correspondence address
THE REPLY FILED 03 March 2003 FAILS TO PLACE Therefore, further action by the applicant is required to final rejection under 37 CFR 1.113 may <u>only</u> be either: (condition for allowance; (2) a timely filed Notice of Appe Examination (RCE) in compliance with 37 CFR 1.114.	avoid abandonment of this appli 1) a timely filed amendment whi	cation. A proper reply to a ch places the application in
PERIOD FOR F	REPLY [check either a) or b)]	
a) 🔲 The period for reply expiresmonths from the mai	ling date of the final rejection.	
b) The period for reply expires on: (1) the mailing date of this no event, however, will the statutory period for reply expire ONLY CHECK THIS BOX WHEN THE FIRST REPLY W/ 706.07(f).	e later than SIX MONTHS from the mail AS FILED WITHIN TWO MONTHS OF	ing date of the final rejection. THE FINAL REJECTION. See MPEP
Extensions of time may be obtained under 37 CFR 1.136(a). The fee have been filed is the date for purposes of determining the period fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of (2) as set forth in (b) above, if checked. Any reply received by the O timely filed, may reduce any earned patent term adjustment. See 37	d of extension and the corresponding an of the shortened statutory period for repl ffice later than three months after the m	nount of the fee. The appropriate extension y originally set in the final Office action; or
1. A Notice of Appeal was filed on Appellant 37 CFR 1.192(a), or any extension thereof (37 CI		
2. The proposed amendment(s) will not be entered	because:	
(a) 🖂 they raise new issues that would require furt	her consideration and/or search	(see NOTE below);
(b) they raise the issue of new matter (see Note		
(c) they are not deemed to place the application issues for appeal; and/or	in better form for appeal by mat	erially reducing or simplifying the
(d) 🔲 they present additional claims without cance	eling a corresponding number of	finally rejected claims.
NOTE: See Continuation Sheet.	• • •	
3. Applicant's reply has overcome the following reject	ction(s):	
4. Newly proposed or amended claim(s) woul canceling the non-allowable claim(s).	d be allowable if submitted in a s	separate, timely filed amendment
5. The a) affidavit, b) exhibit, or c) request for application in condition for allowance because:		sidered but does NOT place the
6. The affidavit or exhibit will NOT be considered be raised by the Examiner in the final rejection.	cause it is not directed SOLELY	to issues which were newly
7. For purposes of Appeal, the proposed amendment explanation of how the new or amended claims w		
The status of the claim(s) is (or will be) as follows	:	
Claim(s) allowed:		
Claim(s) objected to:		
Claim(s) rejected:		
Claim(s) withdrawn from consideration:		
8. The proposed drawing correction filed on is	s a) approved or b) disap	proved by the Examiner.
9. Note the attached Information Disclosure Stateme		
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10. Other:		
S. Patent and Trademark Office		······································
PTO-303 (Rev. 04-01) Ad	visory Action	Part of Paper No. 11

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Continuation of 2. NOTE: The newly added limitations to claims 1, 9, 17 and newly added claims 23-25 change the scope of the invention and raise new issues.

It chile

Olik Chaudhuri Supervisory Patent Examiner Technology Center 2800

MAR-28-2003 FRI 11:01 AM CONLEY ROSE & TAYON

FAX NO. 5127031250

Uniter the Preparwork Reduction Act of 1995, no persons are not Request	The second statements of the	09/779,123
For	Application Number	February7, 2001
Continued Examination (RCE)	Filing Date	Anantha R. Selhuraman
Transmittal	First Named Inventor	2823
Address to: Commissioner for Patents	Art Unit	
Box RCE	Examiner Name	Lee, Hslen Ming
Washington, DC 20231	Attorney Docket Number	5298-02502
No is a Request for Continued Examination (RCE) equest for Continued Examination (RCE) practice under 37 95, or to any design application. See Instruction Sheet for f	CER 1 114 does not apoly to any util	tily or plant application filed prior to June 8.
a. Previously submitted I. Consider the amendment(s)/reply und (Any unantered amendment(s) referred to a II. Consider the arguments in the Appeal III. Other b. Consider the arguments in the Appeal III. Other b. Amendment/Reply II. Alfidavit(s)/ Declaration(s) Miscellaneous a. Provide the action on the above-identifie b. Other Foes The RCE fee under 37 CFR 1.17(e) is requ The Director is hereby authorized to charge be posit Account No. 03-2769 I. RCE fee required under 37 CFR 1.17(III. Extension of time fee (37 CFR 1.136 and (SHORT W000000(03 GN&769 09779123)	Brief or Rely Brief previously filed of iii. Information iv. Other d application is requested under 37 (nsion shall not exceed 3 months; Fee under inced by 37 CFR 1.114 when the RCE the following fees, or credit any over e) 1.17)	CFR 1.103(c) for a Ser 37 CFR 1.17() required)
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c. Payment by credit card (Form PTO-2038 error WARNING: Information on this form be Included on this form. Provide c	ned) May become public. Credit card Ir	
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gnature Kovin Platter		lion No. (Attomey/Agent) 31,116 March 28, 2003
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proby cartify that this correspondence is being deposited with the U drossout to: Commissioner For Patents, Box RDE, Washington, DC i own below.		
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Commissionar for Patanta, Box RCE, Washington, DC 20231. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-785-9199) and solact option 2.

Received from < 5127031250 > at 3/28/03 12:01:33 PM [Eastern Standard Time]

P. 01

	υ	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
1			US 6143663 A	20001107	16	Employing deionized water and an abrasive surface to polish a semiconductor topography	
2			US 6114215 A	20000905	10	Generating non-planar topology on the surface of planar and near-planar substrates	438/401
3		⊠	US 5922620 A	19990713	12	Chemical-mechanical polishing (CMP) method for controlling polishing rate using ionized water, and CMP apparatus	438/693
4			US 5602423 A	19970211	10	Damascene conductors with embedded pillars	257/752

05/02/2003, EAST Version: 1.03.0002

	Current XRef	Retrieval Classif	Inventor	s	c	P	2	3	4	5	Image Doc. Displayed	PT
1	257/E21.245; 257/E21.304; 438/692; 438/693		Koutny, Jr., William W. C.						D		US 6143663	
2	257/E23.179; 438/633; 438/692; 438/693		Osugi, Richard S. et al.	⊠				٥	0		US 6114215	
3	257/E21.23; 257/E21.304; 438/4; 438/690; 438/692; 438/692; 451/60		Shimomura, Mariko et al.								US 5922620	
4	257/760; 257/763; 257/764; 257/765; 257/767; 257/768; 257/768; 257/E21.575		Jain, Manoj K.	⊠							US 5602423	

L Number	Hits	Search Text	DB	Time stamp
1	1	("6232231").PN.	USPAT;	2003/05/02 14:04
			US-PGPUB	
2	3		USPAT;	2003/05/02 14:24
		("5928959")).PN.	US-PGPUB	
3	7	trench same CMP same deionized	USPAT;	2003/05/02 14:27
1.	_		US-PGPUB	
4	0	trench same CMP same deionized	EPO; JPO;	2003/05/02 14:27
{			DERWENT;	
	_		IBM_TDB	
5	1	trench and (CMP same deionized)	EPO; JPO;	2003/05/02 14:28
			DERWENT;	
6	92	trench and (CMP same deionized)	IBM_TDB	2002/05/02 14:42
0	92	(Tench and (CMP same defonized)	USPAT; US-PGPUB	2003/05/02 14:43
17	2385	438/691,692,697,700.ccls.	USPAT;	2003/05/02 14:41
	2303	430/031/032/03///00.0013.	US-PGPUB	2003/03/02 14.41
8	634	438/691,692,697,700.ccls. and trench and	USPAT;	2003/05/02 14:52
		cmp	US-PGPUB	
12	84	(438/691,692,697,700.ccls. and trench and	USPAT;	2003/05/02 14:52
		cmp) and (deionized)	US-PGPUB	

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US-PAT-NO: 6114215

DOCUMENT-IDENTIFIER: US 6114215 A

TITLE: Generating non-planar topology on the surface of planar and near-planar substrates

----- KWIC -----

FIGS. 2A-2C show some major steps involved in the fabrication of one of alignment marks 16 on a surface of an IC substrate 20. The fabrication of alignment mark 16 may begin when a trench 24 is etched in a dielectric layer 22, as shown in FIG. 2A. According to FIG. 2B, a layer of metal 26 is then deposited on the surface of IC substrate 20, filling trench 24. Next, the surface of IC substrate 20 is subjected to chemical-mechanical polishing for polishing layer of metal 26 disposed above dielectric layer 22 and form alignment mark 16 as shown in FIG. 2C. Chemical-mechanical polishing (sometimes referred to as "CMP") typically involves mounting IC substrates face down on a substrate holder and rotating the IC substrate against a polishing pad mounted on a platen, which is in turn rotating or is in orbital state. A slurry containing a chemical that chemically interacts with the facing IC substrate layer and an abrasive that physically removes that layer is flowed between the IC substrate and the polishing pad or on the pad near the IC substrate. In semiconductor wafer fabrication, this technique is used to planarize various wafer layers such as dielectric layers, metallization layers etc.

05/02/2003, EAST Version: 1.03.0002

The step of fabricating the alignment mark may include: (i) etching a **trench** in a surface of a dielectric layer that is disposed above the integrated circuit substrate surface; (ii) blanket depositing the alignment mark fill material on the surface of the dielectric layer and filling the **trench**; and (iii) polishing the integrated circuit substrate surface to remove the alignment mark fill material deposited above the surface of the dielectric layer and excessive amounts of the alignment mark fill material deposited above the **trench** and thereby form the alignment mark.

The dielectric layer may be silicon dioxide. The **trench** may have a width that is between about 0.5 and about 8 .mu.m and a length that is between about 80 and about 120 .mu.m. The depth of the **trench** may depend on the thickness of the dielectric layer, for example, and is generally between about 3000 Angstroms and about 2 .mu.m. The alignment mark fill material may include a metal, e.g., tungsten.

FIG. 3A shows a partially fabricated integrated circuit (IC) substrate, e.g., a partially fabricated semiconductor wafer, 100 having a modified alignment mark 116, according to one embodiment of the present invention, that is formed in a dielectric layer 122. Alignment mark 116 includes a trench 124 partially filled with an alignment mark fill material 126, which is similar to a plug composition, i.e. a contact or via plug composition, and therefore may include a metal like tungsten, for example. Trench 124 may have a width that is between about 0.5 and about 8 .mu.m and a length that is between about 80 and about 120 .mu.m. A depth of trench 124 may depend on the application and

05/02/2003, EAST Version: 1.03.0002

thickness of dielectric layer 122 and is generally between about 3000 Angstroms and about 2 .mu.m.

In an another embodiment, step 204 of the present invention is performed during fine polishing of the partially fabricated IC substrate surface. Typically during fine polishing, also well known in the art as "buffing," an IC substrate surface undergoes polishing that is far less coarse than the CMP process described in step 202. Fine polishing is typically carried out in the presence of a buffing solution, which generally does not contain abrasive particles to initiate any abrasions on the IC substrate surface during fine polishing. This step is typically employed in some IC substrate fabrication applications to remove a contaminated IC substrate layer, i.e. including contaminants from the slurry residue and/or eroded material, resulting from the CMP process. Conventionally, the buffing solution includes a dilute solution of a surfactant, such as between about 1% and about 3% (in volume) of ammonium hydroxide (NH.sub.4 OH) in deionized water. According to one embodiment of the present invention, however, the metal etchant described above is admixed with the buffing solution. Consequently, at least some of the alignment mark fill material is selectively removed from the IC substrate surface during the fine polishing of the IC substrate surface and a step is introduced into the alignment mark as shown in FIG. 3A.

In yet another embodiment, step 204 of the present invention is performed in a wet storage station that typically follows <u>CMP</u> or fine polishing. Typically, the IC substrates are soaked or drenched in a bath of <u>deionized</u> water, before they are subjected to vigorous cleaning in a wafer scrubber

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by various cleaning solutions. In this embodiment, the metal etchant mentioned above is admixed with the soaking solution, e.g., including <u>deionized</u> water, employed in the wet storage station to selectively remove the alignment mark fill material from IC substrate surface and thereby introduce a step into the alignment mark.

etching a **trench** in a surface of a dielectric layer that is disposed above said integrated circuit substrate surface;

blanket depositing said alignment mark fill material on said surface of said dielectric layer and filling said **trench**; and

polishing said integrated circuit substrate surface to remove said alignment mark fill material deposited above said surface of said dielectric layer and excessive amounts of said alignment mark fill material deposited above said **trench** and thereby form said alignment mark.

4. The process of claim 2, wherein said **trench** has a width that is between about 0.5 and about 8 .mu.m.

5. The process of claim 2, wherein said **trench** has a length that is between about 80 and about 120 .mu.m.

6. The process of claim 2, wherein said **trench** has a depth that is between about 3000 Angstroms and about 2 .mu.m.

05/02/2003, EAST Version: 1.03.0002

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US-PAT-NO: 5922620

DOCUMENT-IDENTIFIER: US 5922620 A

TITLE: Chemical-mechanical polishing (CMP) method for ionized water, and CMP

apparatus

----- KWIC -----

FIGS. 3A and 3B show an application of the CMP method used in a process for separating trench elements. After an SiO.sub.2 film 2 is formed by thermal oxidation of the surface of the semiconductor substrate 1, an Si.sub.3 N.sub.4 film 7 which will serve as a stopper film is formed by the CVD method. Subsequently, the films 2 and 7 are patterned by lithography to form grooves 9. Those surface portions of the semiconductor substrate 1 which constitute the inner surfaces of the grooves 9 are oxidized, and then boron is injected into the bottoms of the grooves 9 to form channel cut regions 10. Thereafter, a polysilicon film 3 is formed by the CVD method on the Si.sub.3 N.sub.4 film 7 and in the grooves 9 (FIG. 3A). An SiO.sub.2 film may be used in place of the polysilicon film. Then, the polysilicon film 3 on the semiconductor substrate 1 is polished until the Si.sub.3 N.sub.4 film 7 is exposed (FIG. 3B). In this case, a polishing rate as low as about 1/10-1/200 is employed, and hence the polishing can be stopped when the Si.sub.3 N.sub.4 film 7 is exposed. Thus, the polysilicon film 3 is formed only in the grooves 9. As is evident from the above, the polishing can be stopped just when the stopper

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film is exposed, by using, as the stopper film, a film of a polishing rate lower than that of a film to be polished, and designating an appropriate polishing period of time.

2. The **CMP** method according to claim 1, wherein the ionized water is created by electrolyzing **deionized** water.

11. The **CMP** method according to claim 10, wherein the ionized water is created by electrolyzing **deionized** water.

Miyashita et al., "A New Post CMP Cleaning Method for **Trench** Isolation Process," First International Chemical-Mechanical Polish (C.M.P.) for VLSI/ULSI Multilevel Interconnection Conference (CMP-MIC), pp. 159-168, 1996.

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US-PAT-NO:

5602423

DOCUMENT-IDENTIFIER: US 5602423 A

TITLE: Damascene conductors with embedded pillars

----- KWIC -----

An improved damascene process is claimed by Cote et al. in U.S. Pat. No. 5,262,354, issued on Nov. 16, 1993. Cote et al. cite several problems with damascene polishing used directly on low resistivity, soft metals such as Al-Cu alloys, including scratching, smearing, corrosion, and dishing (conducting material may be removed to a level below the top surface of the insulator). Their approach to this problem involves depositing the soft metal such that the channels are filled to between a few hundred nm and a few hundred .ANG. of the top surface of the dielectric, and capping this with a wear-resistant, higher resistivity layer (e.q. a refractory metal such as tungsten) before polishing. One difficulty with such an approach is the exacting control required for an anisotropic deposition of the soft metal to the required depth tolerance, particularly given normal variations in trench depth and metal deposition rate across a wafer. The higher resistivity refractory cap layer also results in an increase in resistance for all conductors fabricated on a given level, unless compensations in conductor height and/or width are incorporated in the design.

During damascene polishing, polish conditions are generally selected which provide a much faster relative polish rate for the

05/02/2003, EAST Version: 1.03.0002
conductive film, as compared to the polish rate of the underlying insulating layer. The present invention therefore realizes that pillars of an appropriate height may be dispersed within a large channel as wear-resistant polish pad supports, before deposition of a conducting film. The pillars serve structurally to prevent overetching or dishing in such a large channel by acting as an etch stop for polishing of the conducting material deposited over a wide trench. One method of forming such pillars is to make provision for them on the mask used to pattern the channels, such that a pillar of the underlying insulating layer material remains after the channel is formed. Alternately, a separate layer of either insulating or conducting material (harder to polish than a subsequent conducting film) may be deposited and patterned to form a pillar within a channel. FIG. 2B shows a wide inlaid conductor 30 and a narrow

inlaid conductor 32 remaining in channels 24 and 26, respectively, after polishing to remove unneeded sections of film 28. Polishing is preferably accomplished by chemical-mechanical polishing (CMP), wherein a wafer containing substrate 20 and/or a polishing pad are rotatably mounted and brought into contact with each other under rotation. A slurry providing both abrasive and chemically reactive components is supplied, typically to the pad, during polishing. The abrasive component is typically comprised of finely ground colloidal silica or alumina particles. For metal polishing, the chemically reactive component is typically diluted acid and/or hydrogen peroxide, with the remainder of the slurry comprised of deionized water. In general, it is desirable that the slurry composition and polishing conditions (e.g. rotational velocity, polish force,

temperature) be adjusted such that the conducting film is selectively removed at a faster rate than the insulating layer (30:1 being a typical ratio) during CMP. One drawback of such a process, however, is illustrated in FIG. 2B. The top surface of narrow conductor 32 is shown as slightly dished but substantially coplanar with the upper surface of insulating layer 22. Wide conductor 30, shown here as 3 times the width of the small conductor (some conductors may be much wider on a given circuit), is shown as both recessed (i.e. overetched) and severely dished. In extreme cases, sections of a wide conductor may be completely removed from the channel during polishing.

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US-PAT-NO: 6027554

DOCUMENT-IDENTIFIER: US 6027554 A

TITLE: Polishing composition

----- KWIC -----

On the other hand, a study is being made to apply the CMP technique to planarization of an interlayer dielectric such as a silicon dioxide film, a wiring material such as an aluminum, tungsten or copper film, or a polysilicon film, to separation of elements and to other applications. A shallow <u>trench</u> isolation method may be mentioned as one of methods for isolation of elements, which have been studied in recent years. This method comprises forming a shallow <u>trench</u> in silicon, forming a silicon dioxide film thereon, followed by planarization by the CMP technique, whereby isolation of elements can be made in a narrower area, and it has attracted an attention as a technique useful for densification of semiconductor devices.

Technical objectives in carrying out the shallow **trench** isolation are to uniformly finish without excessive or insufficient stock removal by polishing the surface for planarization and to complete the polishing at a predetermined level of stock removal. Usually, it is common to provide a harder silicon nitride film beneath a silicon dioxide film to be polished, so that the silicon nitride film serves as a stopper during the polishing. It should readily be understood that as a polishing agent to be used here, it is preferred to employ a polishing agent which is capable of efficiently polishing the silicon dioxide film and which, on the other hand, is incapable of polishing the silicon nitride film.

The water to be used in the present invention is not particularly limited, and it may, for example, be industrial water, city water, **deionized** water, distilled water or ultrapure water. The content of the water in the polishing composition is usually from 30 to 99.899 wt %, preferably from 65 to 98.995 wt %.

438/692

05/02/2003, EAST Version: 1.03.0002

US-PAT-NO: 5922620

DOCUMENT-IDENTIFIER: US 5922620 A

TITLE: Chemical-mechanical polishing (CMP) method for controlling polishing rate using ionized water, and CMP apparatus

----- KWIC ------

FIG. 1 is a schematic sectional view, showing a general CMP apparatus for flattening a wafer surface. As is shown in FIG. 1, a turn table 16, which includes a polishing disc 17 and a support unit 15, is placed on a stage 11 with a bearing 13 interposed therebetween. A polishing pad 19 is attached to the upper surface of the polishing disc 17 for polishing a wafer. A driving shaft 21 is provided for rotating the turn table 16. The driving shaft 21 is rotated by a motor 23 via a rotating belt 25. On the other hand, a semiconductor wafer 20 is supported by a wafer carrier 33. The wafer carrier 33 has a retainer ring 29 and an adsorption pad 31 for holding the wafer by a vacuum force or the tension of water. The wafer 20 has its position controlled by the wafer carrier 33 such that it is opposed to the polishing pad 19. The wafer carrier 33 is connected to a driving shaft 35. The driving shaft 35 is rotated by a motor 37 via gears 39 and 40, and <u>fixed</u> to a driving unit 43 for vertically move the shaft 35.

FIGS. 3A and 3B show an application of the CMP method used in a process for separating **trench** elements. After an SiO.sub.2 film 2 is formed by thermal oxidation of the surface of the semiconductor substrate 1, an Si.sub.3 N.sub.4 film 7 which will serve as a stopper film is formed by the CVD method. Subsequently, the films 2 and 7 are patterned by lithography to form grooves 9.

Those surface portions of the semiconductor substrate 1 which constitute the inner surfaces of the grooves 9 are oxidized, and then boron is injected into the bottoms of the grooves 9 to form channel cut regions 10. Thereafter, a polysilicon film 3 is formed by the CVD method on the Si.sub.3 N.sub.4 film 7 and in the grooves 9 (FIG. 3A). An SiO.sub.2 film may be used in place of the polysilicon film. Then, the polysilicon film 3 on the semiconductor substrate 1 is polished until the Si.sub.3 N.sub.4 film 7 is exposed (FIG. 3B). In this case, a polishing rate as low as about 1/10-1/200 is employed, and hence the polysilicon film 3 is formed only in the grooves 9. As is evident from the above, the polishing can be stopped just when the stopper film is exposed, by using, as the stopper film, a film of a polishing rate lower than that of a film to be polished, and designating an appropriate polishing period of time.

It is not considered preferable these days to use a fluorine-based solvent such as fleon, etc. in manufacturing semiconductor devices, since it adversely affects the environment. In place of the fluorine-based solvent, <u>deionized</u> water has recently been used as the safest solvent. <u>Deionized</u> water is of high purity with a resistance of about 5 to 18 M.OMEGA.cm, which contains almost no impurities including ions, fine particles, microbes, organic matters, etc. A water purifying apparatus (deionizer) very efficiently removes materials suspended or dissolved in water, thereby creating extremely pure water. <u>Deionized</u> water may also be called "pure water" when its electric conductivity .rho. is lower than 10 .mu.Scm, and "extrapure water" when it is lower than 0.055 .mu.Scm.

In the present invention, **deionized** water is electrolyzed to create highly-oxidizable positive-ionized water which contains oxygen and ozone, and highly-reducible negative-ionized water. These positive-ionized water and negative-ionized water are used for chemical-mechanical polishing.

Ionized water supplied from the ionized-water supply pipe 52 can be classified into alkaline ionized water and acidic ionized water. Ionized water of a desired pH is created by electrolyzing, at a low voltage, **deionized** water

which contains no electrolyte, i.e. no metal impurity, in an electrolytic bath with a solid electrolyte contained therein. Where alkaline ionized water is used and the polishing rate is changed during polishing, the rate can be increased in a stable manner by increasing the pH value of alkaline ionized water, and can be reduced in a stable manner by reducing the pH value of alkaline ionized water. On the other hand, in the case of using acidic ionized water, the polishing rate can be increased in a stable manner by reducing the pH value of acidic ionized water, and can be reduced in a stable manner by increasing the pH value of acidic ionized water.

In the electrolytic bath 60, a diluent electrolyte solution 69 with a supporting electrolyte (e.g. ammonium chloride) contained therein is mixed with **deionized** water, and a power voltage is applied thereto from the battery 66, thereby electrolyzing the **deionized** water. Negative-ionized water 73 created on the side of the cathode 63 as a result of electrolyzation is alkaline ionized water, while positive-ionized water 74 created on the side of the anode 64 is acidic ionized water. Moreover, if **deionized** water is electrolyzed in the bath 60 using oxalic acid as the supporting electrolyte, both negative-ionized water created on the side of the anode exhibit acidic properties. The negative-ionized water 73 in the cathode chamber 61 is supplied to the outside through a negative-ionized water supply pipe 71, and the positive-ionized water in the anode chamber 62 is supplied to the outside through a positive-ionized water supply pipe 72.

Ionized water can be classified into alkaline ionized water and acidic ionized water. Ionized water of a desired pH is created by electrolyzing, at a low voltage, <u>deionized</u> water which contains no electrolyte, i.e. no metal impurity, in an electrolytic bath with a solid electrolyte contained therein. Where in the case of using alkaline ionized water, the polishing rate is changed during polishing, it can be increased in a stable manner by increasing the pH value of alkaline ionized water, and can be reduced in a stable manner by reducing the pH value of alkaline ionized water. On the other hand, in the case of using acidic ionized water, the polishing rate can be increased in a

stable manner by reducing the pH value of acidic ionized water, and can be reduced in a stable manner by increasing the pH value of acidic ionized water.

2. The CMP method according to claim 1, wherein the ionized water is created by electrolyzing **deionized** water.

11. The CMP method according to claim 10, wherein the ionized water is created by electrolyzing **deionized** water.

438/692

Miyashita et al., "A New Post CMP Cleaning Method for **Trench** Isolation Process," First International Chemical-Mechanical Polish (C.M.P.) for VLSI/ULSI Multilevel Interconnection Conference (CMP-MIC), pp. 159-168, 1996.

There we used			UNITED STATES DEPARTM United States Patent and Tr Address: COMMISSIONER OF PATE P.O. Box 1450 Alexandra, Vingnia: 22313-145 www.unito.gov	edemark Office NTS AND TRADEMARKS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
CONLEY RC			EXAMI	NER
P.O. BOX 684			LEE, HSIE	N MING
AUSTIN, TX	78768			

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Page 225 of 329

	•	Application No	Apr	plicant(s)	1
		09/779,123	SE	SETHURAMAN ET AL.	
	Office Action Summary	Examiner	Art	Unit	
		Hsien-Ming Le	e 282	13	
	The MAILING DATE of this comm	unication appears on the cove	ar she t with the corres	spondenc address	
THE - Externanterna enternanternanternanternanternanternanternanternanternanternanternanternanternanternanternanternanternanternaterna	ORTENED STATUTORY PERIOD MAILING DATE OF THIS COMMU nsions of time may be available under the provisi SIX (6) MONTHS from the mailing date of this ca period for reply specified above is less than third period for reply specified above is less than third period for reply specified above, the maximum re to reply within the set or extended period for me pely received by the Office later than three mont ad patent term adjustment. See 37 CFR 1.704(b)	INICATION. ons of 37 CFR 1.136(a). In no event, how ommunication. y (30) days, a reply within the statutory min n statutory period will apply and will expire apply will, by statute, cause the application on after the mailing date of this communic	vever, may a reply be timely file inimum of thirty (30) days will b a SIX (6) MONTHS from the ma to become ABANDONED (35	ed be considered timely. ailing date of this communica U.S.C. § 133).	ation.
1)⊠	Responsive to communication(s	filed on 28 March 2003 .			
2a)	This action is FINAL.	2b) This action is non-	final.		
3) Dispositi	Since this application is in condit closed in accordance with the pr ion of Claims				ts is
4)🛛	Claim(s) 1-4,7-12,15 and 17-25 i	s/are pending in the application	on.		
	4a) Of the above claim(s) is	are withdrawn from conside	ration.		
5)	Claim(s) is/are allowed.				
6)🛛	Claim(s) 1-4,7-12,15 and 17-25 is	/are rejected.			
7)	Claim(s) is/are objected to				
	Claim(s) are subject to res on Papers	triction and/or election require	ement.		
9)🛛	The specification is objected to by	the Examiner.			
10)	The drawing(s) filed on is/a	e: a) accepted or b) object	ted to by the Examine	ſ.	
	Applicant may not request that any				
11)	The proposed drawing correction f			by the Examiner.	
	If approved, corrected drawings are		stion.		
	The oath or declaration is objected	to by the Examiner.			*
Priority u	inder 35 U.S.C. §§ 119 and 120				
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a)[All b) Some * c) None o	Ê			
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14) 🗌 A	cknowledgment is made of a claim	n for domestic priority under 3	5 U.S.C. § 119(e) (to	a provisional applic	ation)
) The translation of the foreign Acknowledgment is made of a clair				
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2) 🗌 Notic	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review nation Disclosure Statement(s) (PTO-1449		Notice of Informal Patent		÷¢

DETAILED ACTION

Remarks

1. Applicants' request for RCE and cancellation to claims 5, 6, 13, 14, and 16 is

acknowledged.

2. Claims 1-4, 7-12, 15 and 17-25 are pending in the application.

Specification

3. The disclosure is objected to because of the following informalities: on page 1, the

"CROSS RELATED APPLICATION DATA" needs to be updated, i.e. "application no.

09/143,723, filed August 31,1998" should be -- application no. 09/143,723, filed August

31,1998, now U.S. Patent 6,232,231 --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7-12, 15 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Jaso et al. (US 6,093,631) in view of Koutny (US 6,143,663).

In re claims 1, 2, 9 and 10, Jaso et al. teach a method, comprising:

• etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14

between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);

- filling the dummy trenches 20 and the first 15d and the series of second trenches
 15a/15b/15c with a conductive material 16 (i.e. copper or aluminum or tungsten)(
 Fig. 11C and col.7, lines 3-7); and
- polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c.

Jaso et al. do not expressly teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches.

However, Jaso *does* suggest the teachings can be applied to the situation of wide-andnarrow trenches. Particularly, in col.3, lines 38-43 Jaso suggest that the teachings can be applied to minimize the difference between the high pattern factor areas (i.e. *equivalent to the "relatively wide trenches"*) and the low pattern factor areas (i.e. *equivalent to the "relatively narrow trenches"*). In other words, Jaso et al. *inherently suggest* that by using the teachings the *dishing effect* between the "relatively narrow trenches" and the "high pattern factor areas" can be minimized.

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to apply the same teachings of Jaso et al. to the alternative situation where the first trench is equivalent to the "relatively wide trench" and the series of second trenches are equivalent to the "relatively narrow trenches", since Jaso et al. suggest the *desirability of modifying* the teachings to apply to the situation of wide-and-narrow trenches (col.7, lines 11-18 and col.3, lines 38-43).

Still, Jaso et al. do not teach polishing the conductive material by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

However, Koutny in an analogous art of CMP technique teaches polishing the conductive material (e.g. aluminum formed in trench, col.5, lines 38-47) by applying a *liquid substantially free of particulate matter* (i.e. deionized water or an acidic liquid, see col.4, lines 50-59 and col. 5, lines 48-53) between an abrasive polishing surface and the conductive material for the purpose of shortening the polishing time (col.6, lines 9-16).

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to substitute the CMP process of Jaso et al. with the CMP process utilizing the liquid substantially free of particulate matter as taught by Koutny, since by doing so it would shorten the polishing time and avoid abrasive particles left on the polishing surface (col.4, lines 34-38 and col. 6, lines 9-16).

In re claims 3 and 11, Jaso et al. in view of Koutny also inherently teach that polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches 20 and said series of relatively narrow trenches (i.e. equivalent to trenches 15a-15c) and said relatively wide trench (i.e. equivalent to trench 15d) because of the presence of the dummy interconnects filled in trench 20, which, in turn, would avoid uneven polishing rate with respect to the areas of the "relatively wide trench" and the "relatively narrow trench."

In re claims 4, 12, 18, 21 and 22, Jaso et al. in view of Koutny also teach that said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches 20, said dummy dielectric protrusions having first upper surfaces *substantially coplanar* with second

upper surfaces of said dummy conductors; and the dummy conductors filled in trench 20 are substantially co-planar with the interconnect filled in trenches 15a-15d, as illustrated in Fig 11D of Jaso et al.

In re claims 7 and 15, Jaso et al. in view of Koutny also teach that said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide (col.4, lines 50-58, Koutny).

In re claim 8, Jaso et al. in view of Koutny also teach that said polishing comprises placing a CMP slurry onto a polishing pad surface and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface (col. 5, lines 57-60 and col.12, claims 5-6, Koutny).

In re claims 17, 19 and 20, the aforementioned teachings of Jaso et al. in view of Koutny also disclose a substantially planar semiconductor topography, comprising:

• a plurality of laterally spaced dummy trenches 20 in a dielectric layer 14, between a relatively wide trench (i.e. equivalent to trench 15d) and a series of relatively narrow trenches (i.e. equivalent to trenches 15a-15c) wherein a lateral dimension of at least one of the dummy trenches 20 is less than a lateral dimension of the wide trench 15d and greater than a lateral dimension of at least one of the series of relatively narrow trenches 15a-15c (Fig.11B);

- Application/Control Number: 09/779,123 Art Unit: 2823
 - dummy conductors (i.e. copper or aluminum or tungsten, col.7, lines 3-5) in said dummy trenches 20 and electrically separate from electrically conductive features below said dummy conductors; and
 - conductive lines in said series of relatively narrow trenches 15a-15c and said relatively wide trench 15d, wherein upper surfaces of said conductive lines (i.e. the conductive material filled in trenches 15a-15d) are substantially coplanar with dummy conductor (i.e. the conductor filled in the dummy trench 20) upper surfaces (Fig.11D).

In re claims 23-25, the selection of the lateral dimensions of the dummy trenches, the wide trench and the narrow trenches is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In particular, Jaso et al. suggest that the teachings can be applied to provide a uniform distribution of interconnect filled in the trenches where the pattern factor (PF) is ranging from 20% (i.e. LPF) to 90 % (i.e.HPF) (col.3, lines 3-56, Jaso et al.). In other words, Jaso's teachings would provide a substantially planar semiconductor topography in which a conductive material is filled in the relatively wide trench and the relatively narrow trenches. In this case, applicants are required to demonstrate the criticality, generally by showing that the claimed dimensions would achieve <u>unexpected</u> results relative to the prior art. See M.P.E.P. 2144.05 III

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W David Coleman Primary Examiner Art Unit 2823

ill.

Hsien Ming Lee May 2, 2003 Le

Application/Control No. 09/779,123	Applicant(s)/Patent Under Reexamination SETHURAMAN ET AL.	
Examiner	Art Unit	Page 1 of 1
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	09/779,123	09/779,123 Reexamination SETHURAM

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
12	A	US-6,093,631	07-2000	Jaso et al.	438/618
	в	US-6,143,663	11-2000	Koutny	438/691
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FOREIGN PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)

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n re A	pplication of:	§ Group Art I	
	Sethuraman et al.	§ Examiner:	Lee, H.
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Serial 1	No. 09/779,123	§ Atty. Dkt. N	lo. 5298-02502
	F 1	8	<u> </u>
Filed:	February 7, 2001	8 I hereby certify that this c	prrespondence is being deposited with
For:	PLANARIZED SEMICONDUCTOR		th sufficient postage as First Class Mail
01.	INTERCONNECT TOPOGRAPHY		to: MS: Non-Fee Amendment, , P.O. Box 1450, Alexandria, VA
	AND METHOD FOR POLISHING A	8 22313, on the date indicat	
	METAL LAYER TO FORM	8	0 1 1 -1
		§ August 6, 2003	Camela Derik
	INTERCONNECT		

41

AMENDMENT; RESPONSE TO OFFICE ACTION DATED MAY 8, 2003

MS: Non-Fee Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313

Dear Sir/ Madam:

This paper is submitted in response to the Office Action dated May 8, 2003 to further highlight reasons why the application is in condition for allowance.

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

SN 09/779,123 Response to Office Action Mailed 5/8/2003

Page 1 of 5

2823



Amendments to the Specification:

. .

Please replace the paragraph beginning on page 1, line 1 with the following rewritten paragraph:

This is a continuation application from prior application no. 09/143,723, filed August 31, 1998, which is now U.S. Patent No. 6,232,231.

REMARKS

No amendments, cancellations, or additions have been made to the claims of the presently claimed case. As such, claims 1-4, 7-12, 15, and 17-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Objections to the Specification

The Specification was objected to for informalities. As noted above, the Specification has been amended to include the suggested change noted in the Office Action. Since the Specification has been amended for clarifications purposes only, the changes do not present new matter. Consequently, the removal of the objection to the Specification is respectfully requested.

Section 103(a) Rejections

Claims 1-4, 7-12, 15, and 17-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (heredinafter referred to as "Jaso") in view of U.S. Patent No. 6,143,663 to Koutny, Jr. (hereinafter referred to as "Koutny"). As will be set forth in more detail below, the § 103(a) rejections are respectfully traversed.

Koutny is not available as prior art for the current rejection. As noted above, claims 1-4, 7-12, 15, and 17-25 were rejected over a combination of Koutny and Jaso. Because the current application has a priority date of August 31, 1998, Koutny is available as prior art against the present claims <u>only</u> under 35 U.S.C. § 102(e). Under the American Inventors Protection Act of 1999 ("the AIPA"), prior art available only under 35 U.S.C. § 102(e) is not usable in a 35 U.S.C. § 103 rejection if the art meets the common ownership requirements of 35 U.S.C. § 103(c) as amended.

The following is a quotation of the revised 35 U.S.C. §103(c) (as of December 14, 2000):

Subject matter developed by another person, which qualifies as prior art only under one of more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

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The AIPA, therefore, amended 35 U.S.C. § 103(c) to state that art which qualifies as prior art only under 35 U.S.C. § 102(e), (f), or (g) is not available for rejections under 35 U.S.C. § 103 if that art was commonly owned or subject to an obligation of assignment at the time the subject invention was made. This change to 35 U.S.C. § 103(c) is effective for any application filed on or after November 29, 1999.

It is noted that upon filing of the present application, the patent to Koutny and the present application were commonly owned by or subject to an obligation of assignment to the same assignee, Cypress Semiconductor Corporation of San Jose, CA. In addition, the present application is an application for patent filed after November 29, 1999 and, thus, is subject to the amendments to § 103(c) made by the AIPA. Consequently, Koutny is not available as prior art against claims of the present application.

Since Koutny is not available as prior art under the current rejection, no combination of Koutny with other cited art may used for the current rejection. As such, the combination of the references cited in the Office Action for the § 103(a) rejections cannot be used against the presently claimed case. Accordingly, removal of the 35 U.S.C. § 103(a) rejection of claims 1-4, 7-12, 15 and 17-25 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all of the issues raised in the Office Action mailed May 8, 2003. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-4, 7-12, 15, and 17-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required or credit any overpayment to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

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Respectfully submitted,

llie E. Zettarg

Mollie E. Lettang Reg. No. 48,405 Agent for Applicants

Conley Rose, P.C. P.O. Box 684908 Austin, TX 78768-4908 Ph: (512) 476-1400 Date: <u>August 6, 2003</u> MEL

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ATTACHMENT A "Marked-Up" Amendments

IN THE CLAIMS

f.5

Please cancel claims 5, 6, 13, 14, and 16. Please amend claims 1, 7, 9, 11, 15, and 17 as follows. Also following is list of all remaining pending claims.

1) (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnection said series of relatively narrow trenches and said relatively wide trench, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. (Canceled)

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6. (Canceled)

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7. (Amended) The method of claim [5] <u>1</u>, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [said] trench and said series of trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

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13. (Canceled)

14. (Canceled)

15. (Amended) The method of claim [13] 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

(Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

Please add the following claims:

23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively same narrow trenches comprise sub-micron lateral dimensions.

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L Number	Hits	Search Text	DB	Time stamp
r	3	(("6545287") or ("20030073295") or ("20030001242")).PN.	USPAT; US-PGPUB	2003/11/11 16:15
2	2	(("6143663") or ("6093631")).PN.	USPAT; US-PGPUB	2003/11/11 16:16
3	1	("6232231").PN.	USPAT; US-PGPUB	2003/11/11 16:30
4	30030	<pre>cmp or(chemical adj mechanical adj (polish or polishing))</pre>	USPAT; US-PGPUB	2003/11/11 16:31
5	468		USPAT; US-PGPUB	2003/11/11 16:31
6	416		USPAT; US-PGPUB	2003/11/11 16:32
7	54	(((cmp or(chemical adj mechanical adj (polish or polishing))) and (free with (abrasive or particulate))) and (conductive or conductor or metal or conducting)) and Gad<19980831	USPAT; US-PGPUB	2003/11/11 16:32

Search History 11/11/03 4:50:13 PM

Page 1

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US-PAT-NO: 5972792

DOCUMENT-IDENTIFIER: US 5972792 A

TITLE: Method for chemical-mechanical planarization of a substrate on a fixed-abrasive

polishing pad

----- KWIC ------

Abstract Text - ABTX (1): A method for chemical-mechanical planarization of a substrate on a fixed-abrasive polishing pad in which a planarizing solution is dispensed onto the fixed-abrasive polishing pad. The planarizing solution is preferably an abrasive-free planarizing solution that oxidizes a surface layer on the substrate without passing the surface layer into solution, and the fixed-abrasive pad has a substantially uniform distribution of abrasive particles fixedly bonded to a suspension medium. The surface layer of the substrate is then pressed against the fixed-abrasive pad in the presence of planarizing solution, and at least one of the fixed-abrasive pad or the substrate moves relative to the other to remove material from the surface of the substrate. In operation, the planarizing solution forms a rough, scabrous layer of non-soluble oxides on the surface layer that are readily removed by the abrasive surface of the polishing pad. In one embodiment of the invention, the pH of the planarizing solution is controlled to oxidize the material of the surface layer without passing it into solution.

Brief Summary Text - BSTX (12):

11/11/2003, EAST version: 1.04.0000

The inventive CMP process preferably increases the polishing rate and reduces defects in fixed-abrasive pad CMP. In an embodiment of the invention for planarizing a metal surface layer on a substrate, an abrasive-free planarizing solution is dispensed onto a fixed-abrasive polishing pad. The abrasive-free planarizing solution preferably has an oxidant that oxidizes the metal on the surface of the substrate without passing the metal into solution. The fixed-abrasive pad has a suspension medium and a substantially uniform distribution of abrasive particles fixedly bonded to the suspension medium. The surface layer of the substrate is then pressed against the fixed-abrasive pad in the presence of the planarizing solution, and at least one of the fixed-abrasive pad or the substrate moves relative to the other. In operation, the planarizing solution forms a rough, scabrous layer of non-soluble oxides on the surface layer that is removed by the abrasive particles of the polishing pad. The non-soluble oxides are generally easier to detach from the substrate with mechanical force than the non-oxidized material. Brief Summary Text - BSTX (14): The inventive CMP process may be used to form electrically isolated conductive features on a semiconductor wafer by depositing an upper layer of conductive material onto a top surface of an insulating

depressions in the insulating layer. A portion of the

is removed with the inventive CMP process until the

between the depressions in the insulating layer. More

conductive layer is preferably removed by dispensing an

oxidizing planarizing solution onto a fixed-abrasive pad;

11/11/2003, EAST Version: 1.04.0000

layer and into

abrasive-free,

pressing the upper

upper conductive layer

specifically, the upper

insulating layer is exposed

conductive layer against the fixed-abrasive pad in the presence of the planarizing solution; and moving the upper conductive layer and the fixed-abrasive pad relative to each other. The remaining portions of the upper conductive layer in the depressions of the insulating layer form electrically isolated conductive features.

Detailed Description Text - DETX (2): The present invention is a method for quickly planarizing a surface layer on a semiconductor wafer or other substrate with a fixed-abrasive polishing pad. An important aspect of an embodiment of the invention is to planarize the surface layer on a fixed-abrasive polishing pad covered with an abrasive-free planarizing solution that oxidizes and/or roughens the material of the surface layer without dissolving the material of the surface layer. The thin, roughened layer on the wafer is readily removed by the abrasive particles in the fixed-abrasive polishing pad, which increases the polishing rate of fixed-abrasive pad CMP. The method of the invention, therefore, increases the throughput of CMP processes using fixed-abrasive pads. Detailed Description Text - DETX (7): The present invention is particularly useful for planarizing metal layers from the front face 14 of the wafer 12 to form conductive features such as damascene lines and interlayer plugs. To planarize a conductive layer of tungsten from the wafer 12, the planarizing solution preferably has a pH below 5.0 and contains at least one of the following oxidants: ferric nitrate, hydrogen peroxide, potassium iodate, and bromine. In a specific example, a layer of tungsten may be quickly planarized with a silica-ceria fixed-abrasive

11/11/2003, EAST Version: 1.04.0000

SAMSUNG EXHIBIT 1004 Samsung v. Invensas

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polishing pad and a particle<u>-free</u> potassium iodate planarizing solution at a pH of 4.5. One suitable planarizing solution is a modified QCTT1011-14B potassium iodate planarizing solution manufactured by Rodel Corporation of Newark, Del. The QCTT1011-14B solution is a conventional slurry with abrasive particles that has been used only on conventional, non-abrasive polishing pads. To modify the QCTT1101-14B solution for use in the present invention, the **abrasive** particles are removed to form an **abrasive-free** solution and the solution is used on a fixed<u>-abrasive</u> pad.

Detailed Description Text - DETX (14): One advantage of the preferred embodiment of the present invention is that it enhances the throughput of wafers planarized with fixed-abrasive polishing pads without sacrificing the planarity of the wafers. Unlike slurries that dissolve the material of the surface layer, the present invention uses an abrasive-free planarizing solution that oxidizes the material of the surface layer without passing it into solution. As discussed above, the abrasive particles in the fixed-abrasive polishing pad remove scabrous, oxidized material faster than non-oxidized material. Additionally, because the planarizing solution merely oxidizes the material of the surface layer without passing it into solution, the top surface of conductive features are not etched below the top surface of an insulating layer. Therefore, the method of the invention increases throughput and produces highly planar surfaces.

Detailed Description Text - DETX (18): From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for

11/11/2003, EAST Version: 1.04.0000

			UNITED STATES DEPAR United States Patent and Address COMMISSIONER F P.D. Box 1450 Alexandra, Virgina 223 www.uspto.gov	Frademark Office OR PATENTS
PPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
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P.O. BOX 6849	208			

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Page 249 of 329

	Applic	ation No.	Applicant(s)	12
	09/77	9,123	SETHURAMAN E	T AL.
Office Action Summary	Exami	ner	Art Unit	
	Hsien-	Ming Lee	2823	
The MAILING DATE of this commu Period for Reply	inication appears on	the coversh et w	ith th correspond nce ad	ldr ss
A SHORTENED STATUTORY PERIOD THE MAILING DATE OF THIS COMMUN - Extensions of time may be available under the provision after SIX (6) MONTHS from the mailing date of this con of the period for reply specified above, is less than thirty of NO period for reply specified above, the maximum - Failure to reply within the set or extended period for rep - Any reply received by the Office later than three months earned patent term adjustment. See 37 CFR 1.704(b). Status	NICATION. ns of 37 CFR 1.136(a). In no munication (30) days, a reply within the statutory period will apply an statutory period will apply an sitter the mailing date of this after the mailing date of this	o event, however, may a / statutory minimum of thir id will expire SIX (6) MON application to become AB	eply be timely filed ty (30) days will be considered time! THS from the mailing date of this cr SANDONED (35 U.S.C. § 133).	y. ommunication
1) Responsive to communication(s) fi	iled on <u>11 August 20</u>	<u>003</u> .		
2a) This action is FINAL.	2b) This action is	s non-final.		
3) Since this application is in conditio closed in accordance with the prac	n for allowance exci	ept for formal matt Quayle, 1935 C.C	ers, prosecution as to the 0, 11, 453 O.G. 213.	e merits is
Disposition of Claims		Sector States		
4) Claim(s) 1-4,7-12,15 and 17-25 is/	are pending in the a	opplication.		
4a) Of the above claim(s) is/				
5) Claim(s) is/are allowed.				
6) Claim(s) <u>1-4.7-12,15 and 17-25</u> is/	are rejected.			
7) Claim(s) is/are objected to.				
8) Claim(s) are subject to restr	riction and/or electio	n requirement.		
Application Papers				
9) The specification is objected to by t	he Examiner.			
10) The drawing(s) filed on is/an	e: a) accepted or	r b) Objected to	by the Examiner.	
Applicant may not request that any obj	ection to the drawing(s) be held in abeya	nce. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including	[2] C. A. Li, J. S. S. Mandala, C.	Carl March Street Street and Street Stre		
11) The oath or declaration is objected	to by the Examiner.	Note the attache	d Office Action or form P1	FO-152.
Priority under 35 U.S.C. §§ 119 and 120				
12) Acknowledgment is made of a claim a) All b) Some * c) None of		under 35 U.S.C.	§ 119(a)-(d) or (f).	
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a) The translation of the foreign la				100 20
14) Acknowledgment is made of a claim reference was included in the first se				
Attachment(s)				
1) X Notice of References Cited (PTO-892)			Summary (PTO-413) Paper No(
 2) D Notice of Draftsperson's Patent Drawing Review 3) Information Disclosure Statement(s) (PTO-1449) 		5) Notice of 1 6) Other:	nformal Patent Application (PTC	D-152)
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DETAILED ACTION

Remarks

1. Claims 1-4, 7-12, 15 and 17-25 are pending in the application.

2. The objection to specification is withdrawn.

Claim Rejections - 35 USC § 103

3 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 7-12, 15 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Jaso et al. (US 6,093,631) in view of Hudson (US 5,972,792).

In re claims 1, 2, 9 and 10, Jaso et al. teach a method, comprising:

etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14

between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);

filling the dummy trenches 20 and the first 15d and the series of second trenches

15a/15b/15c with a conductive material 16 (i.e. copper or aluminum or tungsten)(

Fig. 11C and col.7, lines 3-7); and

 polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c.

Jaso et al. do not expressly teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches.

Page 2

However, Jaso et al. do suggest the teachings can be applied to the situation of wide-andnarrow trenches. Particularly, in col.3, lines 38-43 Jaso et al suggest that the teachings can be applied to minimize the difference between the high pattern factor areas (i.e. *equivalent to the "relatively wide trenches"*) and the low pattern factor areas (i.e. *equivalent to the "relatively narrow trenches"*). In other words, Jaso et al. *inherently suggest* using the teachings to minimize a *dishing effect* between the "relatively narrow trenches" and the "high pattern factor areas' can be minimized.

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to apply the same teachings of Jaso et al. to the alternative situation where the first trench is equivalent to the "relatively wide trench" and the series of second trenches are equivalent to the "relatively narrow trenches", since Jaso et al. suggest the *desirability of modifying* the teachings to apply to the situation of wide-and-narrow trenches (col.7, lines 11-18 and col.3, lines 38-43).

Still, Jaso et al. do not teach polishing the conductive material by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

However, Hudson, in an analogous art of CMP technique, teaches polishing the conductive material 17 (i.e. copper, Fig.3) by applying a *liquid 144 free of particulate matter* (i.e. a planarizing solution comprising deionized water with nitric acid and ethanol, col.4, lines 50-65) between an abrasive polishing surface 143 and the conductive material 17 for the purpose of shortening the polishing time and reducing defects (col.2, lines 25-29).

Page 3

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141

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to substitute the CMP process of Jaso et al. with the CMP process utilizing the liquid substantially free of particulate matter as taught by Hudson, since by doing so it would increasing polishing rate and reducing defects (col.2, lines 25-29, Hudson).

In re claims 3 and 11, Jaso et al. in view of Hudson also inherently teach that polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches 20 and said series of relatively narrow trenches (i.e. equivalent to trenches 15a-15c) and said relatively wide trench (i.e. equivalent to trench 15d) because of the presence of the dummy interconnects filled in trench 20, which, in turn, would avoid uneven polishing rate with respect to the areas of the "relatively wide trench" and the "relatively narrow trench."

In re claims 4, 12, 18, 21 and 22, Jaso et al. in view of Hudson also teach that said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches 20, said dummy dielectric protrusions having first upper surfaces *substantially coplanar* with second upper surfaces of said dummy conductors; and the dummy conductors filled in trench 20 are substantially co-planar with the interconnect filled in trenches 15a-15d, as illustrated in Fig 11D of Jaso et al.

In re claims 7 and 15, Jaso et al. in view of Hudson also teach that said abrasive polishing surface 143 comprises particles 147 at least partially fixed into a polymer-based matrix, and wherein said particles 143 comprise a material selected from the group consisting of cerium oxide, cerium dioxide and silicon dioxide(i.e. silica) (col.4, lines 38-40, Hudson).

In re claim 8, Jaso et al. in view of Hudson also teach that said polishing comprises placing a CMP slurry onto a polishing pad surface and contacting said polishing pad surface with an upper

Page 4

surface of said conductive material while rotating said polishing pad surface relative to said upper surface (Fig. 2, Hudson).

In re claims 17, 19 and 20, the aforementioned teachings of Jaso et al. in view of Hudson also disclose a substantially planar semiconductor topography, comprising:

- a plurality of laterally spaced dummy trenches 20 in a dielectric layer 14, between a relatively wide trench (i.e. equivalent to trench 15d) and a series of relatively narrow trenches (i.e. equivalent to trenches 15a-15c) wherein a lateral dimension of at least one of the dummy trenches 20 is less than a lateral dimension of the wide trench 15d and greater than a lateral dimension of at least one of the series of relatively narrow trenches 15a-15c (Fig. 11B);
- dummy conductors (i.e. copper or aluminum or tungsten, col.7, lines 3-5) in said dummy trenches 20 and electrically separate from electrically conductive features below said dummy conductors; and
- conductive lines in said series of relatively narrow trenches 15a-15c and said relatively wide trench 15d, wherein upper surfaces of said conductive lines (i.e. the conductive material filled in trenches 15a-15d) are substantially coplanar with dummy conductor (i.e. the conductor filled in the dummy trench 20) upper surfaces (Fig.11D).

In re claims 23-25, the selection of the lateral dimensions of the dummy trenches, the wide trench and the narrow trenches is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is

obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In particular, Jaso et al. suggest that the teachings can be applied to provide a uniform distribution of interconnect filled in the trenches where the pattern factor (PF) is ranging from 20% (i.e. LPF) to 90 % (i.e. HPF) (col.3, lines 3-56, Jaso et al.). In other words, Jaso's teachings would provide a substantially planar semiconductor topography in which a conductive material is filled in the relatively wide trench and the relatively narrow trenches. In this case, applicants are required to demonstrate the criticality, generally by showing that the claimed dimensions would achieve <u>unexpected</u> results relative to the prior art. See M.P.E.P. 2144.05 III

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Patent Examiner Hsien Ming Lee Art Unit 2823

Lu

November 12, 2003

Notice of References Cited	Application/Control No. 09/779,123	Applicant(s)/Patent Under Reexamination SETHURAMAN ET AL.				
Notice of References Cited	Examiner Hsien-Ming Lee	Art Unit 2823	Page 1 of			

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-6,093,631	07-2000	Jaso et al.	438/618
X	в	US-5,972,792	10-1999	Hudson, Guy F.	438/691
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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Notice of References Cited

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Part of Paper No. 111103



Application No.	Applicant(s)	
09/779,123	SETHURAMAN ET AL	
Examiner	Art Unit	
Hsien-Ming Lee	2823	

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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SAMSUNG EXHIBIT 1004 Samsung v. Invensas

Page 259 of 329

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Title of Invention	TOPO	ARIZED SEMICOND GRAPHY AND METH DRM INTERCONNEC	HOD FOR POLIS		TAL LAYER
Application Num Date: First Named App Attorney Docket Art Unit: Examiner:	200 Ilicant: Ar Number: 529 283	01-02-07 hantha R. Sethuraman 98-02502			
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	Fee D	escription	Fee Code	Amount \$	Fee Paid \$
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Page 1 of 1

Page 260 of 329



Electronic Filing System (EFS) Data Electronic Patent Application Submission USPTO Use Only

EFS ID:	53978	
Application ID:	09779123	
	PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY	
Title of Invention:	AND METHOD FOR POLISHING A	1
	METAL LAYER TO FORM	
	INTERCONNECT	
First Named Inventor:	Anantha Sethuraman	
Domestic/Foreign Application:	Domestic Application	
Filing Date:	2001-02-07	
Effective Receipt Date:	2004-01-20	
Submission Type:	Information Disclosure Statement	
Filing Type:	- Statement	
Confirmation number:	9269	
Attorney Docket Number:	5298-02502	
Total Fees Authorized:	180.0	
Payment Category:	Deposit Account	
Deposit Account Number:	32769	
Deposit Account Name:	Kevin L. Daffer	
Access Code:	****	
RAM Payment Status:	RAM success	
RAM User ID:	EFSPROD	
RAM Accounting Date:	2004-01-20	
RAM Sequence Number:	4	

Digital Certificate Holder: cn=Kevin L. Daffer,ou=Registered Attorneys,ou=Patent and Trademark Office,ou=Department of Commerce,o=U.S. Government,c=US Certificate Message Digest: 9099fb8e14cf0e12f779738052769534f3ce595c

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PAGE 1/9 * RCVD AT 2/16/2004 4:33:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:5127031250 * DURATION (mm-ss):06-00

Remarks begin on page 6 of this paper.

Dear Sir/ Madam:

P.O. Box 1450

Alexandria, VA 22313

In re Application of:

Serial No. 09/779,123

For:

Filed: February 7, 2001

Sethuraman et al.

highlight reasons why the application is in condition for allowance.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

This paper is submitted in response to the Office Action mailed November 14, 2003 to further

Mail Stop: Non-Fee Amendment **Commissioner** for Patents

INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

PLANARIZED SEMICONDUCTOR

Group Art Unit: 2823

	Examiner: Lcc, H.
	Atty. Dkt. No. 5298-02502
22	I hereby certify that this correspondence is being transmitted via thesimile or deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope of messed to: Commissioner for Patents, P.O. Byg 2450 Alexandria, VA

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AMENDMENT; RESPONSE TO OFFICE ACTION DATED NOVEMBER 14, 2003

Amendm nts t Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

 ≈ 1

1. (Previously Presented) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

tilling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. (Previously Presented) The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Previously Presented) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. (Original) The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. - 6. (Canceled)

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7. (Previously Presented) The method of claim 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

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8. (Original) The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Previously Presented) A method, comprising:

ctching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said polishing comprises. applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. (Original) The method of claim 9, wherein said conductive material comprises a metal selected from - the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Previously Presented) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

12. (Original) The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. - 14. (Canceled)

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15. (Previously Presented) The method of claim 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Previously Presented) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. (Original) The substantially planar semiconductor topography of claim 17, further comprising dummy, dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. (Original) The substantially planar semiconductor topography of claim 17, wherein said durnmy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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20. (Original) The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof. 21. (Previously Presented) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect. 22. (Previously Presented) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect. 5.5 23. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein a semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 ^a microns. 24. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns. 25. (Previously Presented) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions. ÷. 26. (New) The method of claim I, wherein said polishing comprising applying a liquid consisting essentially of deionized water at a substantially neutral pH. 27. (New) The method of claim 9, wherein said polishing comprising applying a liquid consisting

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essentially of deionized water at a substantially neutral pH.

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<u>REMARKS</u>

Claims 26 and 27 have been added. Accordingly, claims 1-4, 7-12, 15, and 17-27 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 103(a) Rejections

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Claims 1-4, 7-12, 15, and 17-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (hereinafter referred to as "Jaso") in view of U.S. Patent No. 5,972,792 to Hudson (hereinafter referred to as "Hudson"). To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond*, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited and does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below. As such, the § 103(a) rejections of claims 1-4, 7-12, 15, and 17-25 is respectfully traversed.

Neither Jaso nor Hudson teach or suggest etching a plurality of laterally spaced dummy trenches into a dielectric between a relatively wide trench and a series of relatively narrow trenches. Claim 1 recites in part: "[a] method, comprising: etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches" Claim 9 includes a similar limitation. Hudson fails to disclose the inclusion of dummy structures in the method described therein and, therefore, provides no motivation to teach the limitations of claims 1 and 9. In addition, as noted on page 2 of the Office Action, "Jaso [does] not expressly teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches."

The Office Action, however, interprets Jaso as suggesting that the teachings therein can be applied to a situation of wide and narrow trenches. In particular, the Office Action cites column 3, lines 38-43 of Jaso, "[in] another aspect of the invention, a method is provided to set a predetermined high pattern factor design limit of say 60-90%, preferably 70-80%. Using this method, the difference between the high pattern factor areas and the low pattern factor areas is minimized due to the lower upper design limit of the HPF areas." There is no teaching or suggestion within such a passage, h wever, of etching dummy

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PAGE 6/9 * RCVD AT 2/16/2004 4:33:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:5127031250 * DURATION (mm-ss):06-00

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trenches specifically between different size trenches. Rather, the cited passage merely refers to minimizing the density distribution differences between regions of the wafer. Jaso teaches minimizing density distributions by adding dummy lines to regions of a wafer. In particular, Jaso illustrates and describes different arrangements of dummy lines 20 in region 17 of Figs. 3a-9b, relative to lines 15. As shown in Figs. 3a-9b, Jaso specifically teaches the addition of dummy lines 20 between lines 15 which are uniform in width. Without a specific teaching or suggestion that a dummy trench may be placed between trenches of differing widths and produce a substantially planar surface having conductive structures formed therefrom, there is no inherent teaching in the passage cited in the Office Action of the limitations of claims 1 and 9 are asserted to be unobvious in light of the cited att.

None of the cited art teaches or suggests a semiconductor topography with a plurality of laterally spaced dummy trenches between a relatively wide trench and a series of relatively narrow. trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches. Claim 17 recites in part:

A substantially planar semiconductor topography, comprising: a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches ...

Jaso does not teach or suggest a topography with a dummy trench having a different lateral dimension than an adjacent relatively wide trench and/or an adjacent series of relatively narrow trenches. In fact, Jaso illustrates dummy lines 20 having the same dimensions as lines 15a-15d, which all have the same dimensions as shown in Fig. 11D. Consequently, the statements in the Office Action eiting that trench 15d in Jaso is equivalent to a relatively wide trench and trenches 15a-15c are equivalent to a series of relatively narrow trenches are asserted to be erroneous. As noted above with regard to the patentability of claims 1 and 9, Jaso does not teach, suggest or provide motivation to create a topography with dummy trenches interposed between trenches of varying widths. As such, there is no motivation within Jaso to teach the limitations of claim 17.

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For the sake of argument, even if Jaso suggested a topography comprising trenches with varying widths, there is no motivation within Jaso to create a topography having a dummy trench with a different width than trenches arranged adjacent thereto. In particular, in addition to the illustration of Fig. 11D, Jaso specifically teaches that it is preferred "... to mimic the size of the chip circuitry." (Jaso, column 4, lines 5-6) and, therefore, does not teach, suggest or provide any motivation to have dummy trenches with different widths than adjacent trenches. Hudson does not disclose a topography with a dummy trench and, therefore cannot be used to teach the limitations of claim 17 alone or in combination with Jaso. As such, claim 17 is asserted to be patentably distinct over the cited art.

For at least the reasons set forth above, none of the cited art, either individually or in combination, teaches, suggests, or provides motivation for all limitations of independent claims 1, 9, or 17. Therefore, claims 1, 9, and 17, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Patentability of the Added Claims

The present Amendment adds claims 26 and 27, which are dependent upon claims 1 and 9, respectively. Accordingly, added claims 26 and 27 are patentably distinct for at least the same reasons as their respective base claim. Support for the limitations of the added claims may be found, for example, on page 16, lines 6-8: "[p]referably, the polishing liquid forwarded onto the abrasive polishing surface is deionized water. The polishing liquid may also be other types of liquids which have a near-neutral pH." Accordingly, approval of added claims 26 and 27 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed November 14, 2003. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-4, 7-12, 15, and 17-27 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

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enfully submitted, Rest in L. Daffer

Reg. No. 34,146 Attorney for Applicants

Conley Rose, P.C. P.O. Box 684908 Austin, TX 78768-4908 Ph: (512) 476-1400 Date: <u>February 16, 2004</u> MFL

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PAGE 9/9 * RCVD AT 2/16/2004 4:33:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:5127031250 * DURATION (mm-ss):06-00



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L Number	Hits	Search Text	DB	Time stamp
1	1	("20020187629").PN.	USPAT; US-PGPUB	2004/04/20 16:16
2	2	(("5958794") or ("5972124")).PN.	USPAT; US-PGPUB	2004/04/20 16:16
3	24	dummy adj trenches	USPAT; US-PGPUB	2004/04/20 16:19
4	13	dummy adj trenches	EPO; JPO; DERWENT; IBM TDB	2004/04/20 16:19

Search History 4/20/04 4:27:14 PM Page 1

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			UNITED STATES DEPAR United States Patent and T Address COMMISSIONER F P.O. Box 1450 Alexandria, Virginia 223 www.uspio.gov	OR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
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P.O. BOX 6849 AUSTIN, TX			ARTUNIT	PAPER NUMBER
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			DATE MAILED: 04/28/2004	1

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
	09/779,123	SETHURAMAN ET AL
Office Action Summary	Examiner	Art Unit
	Hsien-Ming Lee	2823
The MAILING DATE of this communica Period for Reply	ation appears on the cover sheet	with the correspondence address
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNICA - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this commun - If the period for reply specified above is less than thirty (30) of - If NO period for reply is specified above, the maximum statud - Failure to reply within the set or extended period for reply will Any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b).	ATION. 37 CFR 1.136(a). In no event, however, may ication. days, a reply within the statutory minimum of tory period will apply and will expire SIX (6) A II, by statute, cause the application to becom	v a reply be timely filed thirty (30) days will be considered timely. IONTHS from the mailing date of this communication. ABANDONED (35 U.S.C. § 133).
Status		
1) Responsive to communication(s) filed	on 16 February 2004	
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3) Since this application is in condition fo		atters, prosecution as to the merits is
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Disposition of Claims	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
4)⊠ Claim(s) 1-4,7-12,15 and 17-27 is/are	pending in the application	
4a) Of the above claim(s) is/are	The second se	
5) Claim(s) is/are allowed.		
6) Claim(s) is/are rejected.		
7) Claim(s) 1-4,7-12,15 and 17-27 is/are	objected to.	
8) Claim(s) are subject to restriction	CONCERNMENT OF THE ARREST OF A DECEMBER AND	
Application Papers		
9) The specification is objected to by the I	Evaminer	
10) The drawing(s) filed on is/are: a		to by the Examiner
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Replacement drawing sheet(s) including th		아니는 영상에서 집안에 가지 않는 것이 많이 많이 많다.
11) The oath or declaration is objected to t	and the second second second second second second	a. The state of
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim fo	r foreign priority under 35 U.S.C	C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:		
1. Certified copies of the priority do		
2. Certified copies of the priority do		
	이 같이 가지 않는 것을 알 것 같아요. 것 같아요. 이 것 같아요. 이 것 같아요. 이 것 같아요.	en received in this National Stage
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* See the attached detailed Office action	for a list of the certified copies r	not received.
Attachment(s)	a Else a	
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTC 		w Summary (PTO-413) No(s)/Mail Date
3) Information Disclosure Statement(s) (PTO-1449 or PT		of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date	6) Other:	

DETAILED ACTION

Remarks

1. Claims 26 and 27 are newly added. Claims 1-4, 7-12, 15 and 17-27 are pending in the application.

Claim Objections

2. Claims 1, 9, 17 are objected to because of the following informalities:

The terms "relatively wide trench" and "relatively narrow trenches" are relative terms and render indefinite because the terms do not provide a standard for measuring the degree intended. See M.P.E.P. 2173.05 (b) The following changes are suggested:

Changing "relatively wide trench" into – a first trench relatively wide compared to a second trench --; and changing "relatively narrow trenches" into – second trenches relatively narrow compared to the first trench --.

In addition, in-consistent term appears in the same claim, i.e. "laterally spaced dummy trenches" (claim 9, line 2 and claim 17, line 2) versus "dummy trenches" (claim 9, line 5 and claim 17, line 4).

Allowable Subject Matter

3. Claims 1, 9 and 17 are would be allowable if rewritten or amended to overcome the objection as set forth in this Office action.

4. Claims 2-4, 7, 8, 10-12, 15, 22, 27, 19-26 are objected to as being dependent upon a objected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record, Jaso et al. to US 6,093,631, teaches a method, comprising:

- etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14
 between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);
- filling the dummy trenches 20 and the first 15d and the series of second trenches
 15a/15b/15c with a conductive material 16 (i.e. copper or aluminum or tungsten)(
 Fig. 11C and col.7, lines 3-7); and
- polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c.

In contrast, Jaso et al. at least neither teach nor suggest that the first trench 15d is a *relatively wide trench compared to second* trenches 15a-15c and the series of second trenches 15a-15c are *relatively narrow trenches compared to the first* trench 15d; that polishing the conductive material by applying a liquid substantially *free of particulate matter* between an abrasive polishing surface and the conductive material.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

> Hsien-Ming Lee Examiner Art Unit 2823

April 21, 2004

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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TOPOG	RAPHY AND	METHOD FOR			
nber: 9269 licant: Ananti Number: 5298-(2823 Hsien- (5958 DCUMENTS	ha Sethuraman 02502 Ming Lee 794 or 5972124)	.pn.			
Patent No.	Date	Patentee	Kind	Class	Subclass
5958794	1999-09-28	Bruxvoort et al.			
5972124	1999-10-26	Sethuraman et al.			
	TOPOG LAYER ber: 09/779 mber: 9269 licant: Anant Number: 5298-1 2823 Hsien- (5958 ocuments not required to Patent No. 5958794	TOPOGRAPHY AND LAYER TO FORM IN ber: 09/779123 mber: 9269 licant: Anantha Sethuraman Number: 5298-02502 2823 Hsien-Ming Lee (5958794 or 5972124) Ocuments not required to submit a paper of Patent No. Date 5958794 1999-09-28	TOPOGRAPHY AND METHOD FOR LAYER TO FORM INTERCONNECT ber: 09/779123 mber: 9269 licant: Anantha Sethuraman Number: 5298-02502 2823 Hsien-Ming Lee (5958794 or 5972124).pn. Ocuments anot required to submit a paper copy of cited US Patent Patent No. Date Patent No. Date 5958794 1999-09-28 Bruxvoort et al.	TOPOGRAPHY AND METHOD FOR POLIS LAYER TO FORM INTERCONNECT ber: 09/779123 mber: 9269 licant: Anantha Sethuraman Number: 5298-02502 2823 Hsien-Ming Lee (5958794 or 5972124).pn. Ocuments not required to submit a paper copy of cited US Patent Docume Patent No. Date Patent No. Date Patent No. Date Patent No. Bruxvoort et al.	ber: 09/779123 mber: 9269 licant: Anantha Sethuraman Number: 5298-02502 2823 Hsien-Ming Lee (5958794 or 5972124).pn. Ocuments not required to submit a paper copy of cited US Patent Documents Patent No. Date Patentee Kind Class 5958794 1999-09-28 Bruxvoort et al.

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U.S. Patent and Trademark Office

Part of Paper No. 042104



Application No.	Applicant(s)
09/779,123	SETHURAMAN ET AL.
Examiner	Art Unit
Hsien-Ming Lee	2823

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U.S. Patent and Trademark Office

Part of Paper No. 042104

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In re /	Application of: Sethuraman et al.	-	Group Art Unit: 2823 Examiner: Lee, H. OFFICIA
Scrial	No. 09/779,123	0000	Atty. Dkt. No. 5298-02502
Filed:	February 7, 2001	8	I hereby certify that this correspondence is being transmitted via
For:	PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISIING A METAL LAYER TO FORM INTERCONNECT	0 00 00 00 00 00	facsimile ar deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope, addressed to: Commissioner for Patents, P. 61. Box 1/361 Alexandria, VA 22313, on the date indicated below July 19, 2004 Date Kevin't Daffer

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AMENDMENT; RESPONSE TO OFFICE ACTION MAILED APRIL 28, 2004

Mail Stop Non-Fee Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313

Dear Sir/ Madam:

This paper is submitted in response to the Office Action mailed April 28, 2004 to further highlight reasons why the application is in condition for allowance.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper,

Remarks begin on page 2 of this paper,

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Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively first wide trench and a series of relatively narrowsecond trenches, wherein each of the second trenches is relatively narrow compared to the first trench;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said <u>laterally.spaced</u> dummy trenches and interconnect in said series of <u>relatively narrowsccond</u> trenches and said <u>relatively wide first</u> trench, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. (Previously Presented) The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Currently Amended) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said <u>laterally spaced</u> dummy trenches and said series of relatively-narrowscond trenches and said relatively widefirst trench.

4. (Currently Amended) The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said <u>laterally spaced</u> dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5.-6, (Canceled)

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7. (Previously Presented) The method of claim 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. (Original) The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Currently Amended) A method, comprising:

ctching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide<u>first</u> interconnect feature and a series of trenches which are to receive relatively narrowa series of second interconnect features, wherein the first interconnect feature is relatively wide compared to each of the series of second interconnect features:

filling said plurality of laterally spaced dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. (Original) The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Currently Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said <u>laterally spaced</u> dummy trenches and said trench and said series of trenches.

12. (Currently Amended) The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said <u>laterally spaced</u> dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

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13. - 14. (Canceled)

15. (Previously Presented) The method of claim 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Currently Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide [jrst trench and a series of relatively narrow second trenches, wherein each of the second <u>trenches</u> is relatively narrow compared to the first trench, and wherein a lateral dimension of at least one of the <u>laterally spaced</u> dummy trenches is less than a lateral dimension of the wide first trench and greater than a lateral dimension of at least one of the series of relatively narrowscond trenches;

dummy conductors in said <u>laterally spaced</u> dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrowsecond trenches and said relatively widefirst trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. (Original) The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. (Original) The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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20. (Currently Amended) The substantially planar semiconductor topography of claim 17, wherein said interconnect-conductive lines comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. (Previously Presented) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Currently Amended) The method of claim 9, wherein said dummy conductors are substantially coplanar with said <u>first</u> interconnect <u>feature</u> and said series of second interconnect features.

23. (Currently Amended) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the laterally <u>spaced</u> dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Currently Amended) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide <u>first</u> trench is greater than approximately 50 microns.

25. (Currently Amended) The substantially planar semiconductor topography of claim 17, wherein the relatively narrowscrice of the second trenches comprise sub-micron lateral dimensions.

26. (Previously Presented) The method of claim 1, wherein said polishing comprising applying a liquid consisting essentially of deionized water at a substantially neutral pH.

27. (Previously Presented) The method of claim 9, wherein said polishing comprising applying a liquid consisting essentially of deionized water at a substantially neutral pH.

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REMARKS

Claims 1, 3, 4, 9, 11, 12, 17, 20, and 22-25 have been amended. As such, claims 1-4, 7-12, 15, and 17-27 arc currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Allowable Subject Matter

Claims 1, 9, and 17 were deemed allowable if rewritten to overcome claim objections noted below. Applicant sincerely appreciates the Examiner's recognition of the patentable subject matter recited in these claims. To expedite prosecution, claims 1, 9, and 17 have been amended to overcome the claim objections noted below, placing the claims in condition for allowance.

Claims 2-4, 7, 8, 10-12, 15, and 19-27 were deemed allowable if rewritten in independent form. Applicant sincerely appreciates the Examiner's recognition of the patentable subject matter recited in these claims. As noted above, however, claims 1, 9, and 17 have been amended to place them in condition for allowance. Accordingly, dependent claims 2-4, 7, 8, 10-12, 15, and 19-27 are also in condition for allowance. Therefore, Applicants respectfully request removal of this objection. It is noted that although claim 18 was not specifically objected to, it is also in condition for allowance as being dependent from elaim 17.

Objections to the Claims

Claims 1, 9, and 17 were objected for informalities. In particular, the claims terms "relatively wide trench" and "relatively narrow trenches" were rendered indefinite because the terms do not provide a standard for measuring the degree intended. In addition, claims terms "laterally spaced dummy trenches" and "dummy trenches" were cited as being inconsistent. To expedite prosecution, claims 1, 9, and 17 have been amended to clarify the claim language in a manner that addresses the concerns expressed in the Office Action for those claims. Accordingly, removal of this objection is respectfully requested.

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PAGE 6/7 * RCVD AT 7/19/2004 2:17:44 PM [Eastern Daylight Time] * SVR: USPTO-EFXRF-1/8 * DNIS:8729306 * CSID:5127031250 * DURATION (mm-ss):04-24
CONCLUSION

This response constitutes a complete response to the issues raised in the Office Action mailed April 14, 2004. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-4, 7-12, 15, and 17-27 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney carnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

Respectfully submitted,

Reg. No. 34,146 Attorney for Applicants

Conley Rose, P.C. P.O. Box 684908 Austin, TX 78768-4908 Ph: (512) 476-1400 Date: July 19, 2004 MEL

SN 09/779,123 Response to Office Action Mailed 4/28/2004

Page 7 of 7

PAGE 7/7 * RCVD AT 7/19/2004 2:17:44 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/8 * DNIS:8729306 * CSID:5127031250 * DURATION (mm-ss):04-24

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1		with trenches)	DERWENT;	14:05
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Search History 9/16/04 2:19:07 PM Page 1

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DERWENT-ACC-NO: 2000-085654

DERWENT-WEEK: 200104

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TITLE: Forming a dual damascene structure for IC fabrication

INVENTOR: HUANG, Y; YANG, M ; YOU, T ; YEW, T

PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN]

PRIORITY-DATA: 1998TW-0110352 (June 26, 1998)

PAT	ENT-FAMILY			
PUE	B-NO		PUB-DATE	
LAN	IGUAGE	PAGES	MAIN-IPC	
US	6001733 A		December 14, 1999	N/A
	014	H01L	021/44	
ΤW	396524 A		July 1, 2000	N/A
	000	H01L	021/768	
JP	2000021879	А	January 21, 2000	N/A
	009	H01L	021/3205	

APPLICATION-DATA:		
PUB-NO	APPL-DESCRIPTOR	APPL-NO
APPL-DATE		
US 6001733A	N/A	
1998US-0164856	October 1, 1998	
TW 396524A	N/A	
1998TW-0110352	June 26, 1998	
JP2000021879A	N/A	
1998JP-0313158	November 4, 1998	

INT-CL (IPC): H01L021/3205, H01L021/44, H01L021/768

ABSTRACTED-PUB-NO: US 6001733A

BASIC-ABSTRACT:

NOVELTY - A dual damascene structure is formed for IC fabrication by forming

09/16/2004, EAST Version: 1.4.1

metal line trenches and a via hole in a dielectric layer as well as shallow dummy line trenches to decrease the area of an adhesion layer to be polished. DETAILED DESCRIPTION - The method comprises: - forming a first inter-metal dielectric layer and stop laver on a substrate; - etching a via hole and dummy metal line pattern in the stop layer using a photoresist mask; - adding a second inter-metal dielectric layer; - pattern etching second and third **metal** line **trenches** and a via hole in the second dielectric layer, the second metal-line trench being above the first **metal** line and communicating with the via hole, the surface of the first metal line being exposed at the bottom of the via hole opening, and the third **metal** trench being beside the second metal line trench where no dummy metal line trench exists; - adding an adhesion layer and a metal layer; - and chemical-mechanical polishing to form the dual damascene structure. USE - Forming a dual damascene with dummy metal lines. ADVANTAGE - The dummy metal lines reduce the area of adhesion layer to be polished so that over-polishing of the metal lines is avoided. The thickness of the dummy metal lines is small so that parasitic capacitance is low. DESCRIPTION OF DRAWING(S) - The drawing shows a dual damascene structure formed by the method of the invention. First metal line 302

09/16/2004, EAST Version: 1.4.1

Shallow dummy metal lines 318a

Adhesion layer 328

Stop layer 306

Second metal line trench 322a

Inter-metal dielectric 317

Third metal line trenches 326

Via hole 324

CHOSEN-DRAWING: Dwg.3E/3

TITLE-TERMS: FORMING DUAL STRUCTURE IC FABRICATE

DERWENT-CLASS: LO3 U11

CPI-CODES: L04-C13B;

EPI-CODES: U11-C05D3;

SECONDARY-ACC-NO: CPI Secondary Accession Numbers: C2000-023888 Non-CPI Secondary Accession Numbers: N2000-067157 UNITED STATES PATENT AND TRADEMARK OFFICE



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UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.usto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 09/30/2004

CONLEY ROSE, P.C. P.O. BOX 684908 AUSTIN, TX 78768 EXAMINER LEE, HSIEN MING ART UNIT PAPER NUMBER

2823

DATE MAILED: 09/30/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269

TITLE OF INVENTION: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FO INTERCONNECT

APPLN, TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	12/30/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATEN <u>PROSECUTION ON THE MERITS IS CLOSED</u>. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHT THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPO PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN <u>THREE MONTHS</u> FROM TH MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. <u>TH</u> <u>STATUTORY PERIOD CANNOT BE EXTENDED</u>. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOV REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (O AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WIL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:	If the SMALL ENTITY is shown as NO:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.	A. Pay TOTAL FEE(S) DUE shown above, or
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or	B. If applicant claimed SMALL ENTITY status before, or is n claiming SMALL ENTITY status, check box 5a on Part B - Fee Transmittal and pay the PUBLICATION FEE (if required) and 1 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) w your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 4

PTOL 85 (Rev 09/04) Approved for use through 04/30/2007

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: <u>Mail</u>	N
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ail Stop ISSUE FEE Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed wh	or <u>Fax</u>	(703) 746-4000
appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" maintenance fee notifications.	appropriate. All further correspondence including the Patent, advance orders and notification indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new	on of maintenance fees will be mailed to the current correspondence address

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CONLEY ROSE, P.O. BOX 684908 AUSTIN, TX 7876				I hereby certify that States Postal Servic addressed to the M transmitted to the U	Certificate of Mailing or Tran t this Fee(s) Transmittal is bei e with sufficient postage for f fail Stop ISSUE FEE addres SPTO (703) 746-4000, on the	ismission ng deposited with the Un irst class mail in an envel s above, or being facsim date indicated below.
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APPLICATION NO.	FILING DATE		FIRST NAMED	INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001		Anantha R. Se	ethuraman	5298-02501	9269
TITLE OF INVENTION: INTERCONNECT	PLANARIZED SEMICOND	UCTOR INTER	CONNECT TO	POGRAPHY AND MET	HOD FOR POLISHING A N	METAL LAYER TO FO
APPLN. TYPE	SMALL ENTITY	ISSUE F	EE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
35617 75	590 09/30/2004		EXAM	NER
CONLEY ROSE	, P.C.		LEE, HSIE	N MING
P.O. BOX 684908 AUSTIN, TX 7876	8		ART UNIT	PAPER NUMBER
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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 77 day(s). If the issue fee is paid on the date that is three months after t mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a ha months) after the mailing date of this notice, the Patent Term Adjustment will be 77 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date th determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retriev (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL 85 (Rev 09/04) Approved for use through 04/30/2007

Page 299 of 329

Page 3 of 4

			UNITED STATES DEPAR United States Patent and T Address: COMMISSIONER FC P.O. Box 1450 Alexandra, Virginia 2231 www.uspto.gov	rademark Office OR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269
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P.O. BOX 684908 AUSTIN, TX 7876	8		ART UNIT	PAPER NUMBER
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			DATE MAILED: 09/30/2004	

Notice of Fee Increase on October 1, 2004

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2004, then t amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" because some fees w increase effective October 1, 2004. See Revision of Patent Fees for Fiscal Year 2005; Final Rule, 69 Fed. Reg. 5260 52606 (May 10, 2004).

The current fee schedule is accessible from WEB site (http://www.uspto.gov/main/howtofees.htm).

If the fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due" but not the correct amount in vie of the fee increase, a "Notice of Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processi delays associated with mailing of a "Notice of Pay Balance of Issue Fee," if the response to the Notice of Allowan is to be filed on or after October 1, 2004 (or mailed with a certificate of mailing on or after October 1, 2004), t issue fee paid should be the fee that is required at the time the fee is paid. See Manual of Patent Examining Procedu (MPEP), Section 1306 (Eighth Edition, Rev. 2, May 2004). If the issue fee was previously paid, and the response the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue f now due, then the difference between the issue fee amount at the time the response is filed and the previously-pa issue fee should be paid. See MPEP Section 1308.01.

Effective October 1, 2004, 37 CFR 1.18 is amended by revising paragraphs (a) through (c) to read as set forth below

Section 1.18 Patent post allowance (including issue) fees.

(a) Issue fee for issuing each original or reissue patent, except a design or plant patent:

By a small entity (Sec. 1.27(a))	\$685.00
By other than a small entity	\$1,370.00

- (b) Issue fee for issuing a design patent: By a small entity (Sec. 1.27(a))......\$245.00 By other than a small entity.....\$490.00
- (c) Issue fee for issuing a plant patent: By a small entity (Sec. 1.27(a))......\$330.00 By other than a small entity.....\$660.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of t Office of Patent Publication at (703) 305-8283.

	Application No.	Applicant(s)
Notice of Allowability	09/779,123 Examiner	SETHURAMAN ET AL.
-		
	Hsien-Ming Lee	2823
The MAILING DATE of this communication apper All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this ap or other appropriate communication IGHTS. This application is subject	pplication. If not included on will be mailed in due course. THIS
1. This communication is responsive to <u>7/19/2004</u> .		
 2.	e Examiner	
4. Acknowledgment is made of a claim for foreign priority ur		
a) \square All b) \square Some* c) \square None of the:	Idel 33 0.3.0. § 119(a)-(d) 01 (1).	
1. Certified copies of the priority documents have	e been received.	
2. Certified copies of the priority documents have		
3. Copies of the certified copies of the priority do	cuments have been received in this	s national stage application from the
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		y complying with the requirements
5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give		
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") mus	st be submitted.	
(a) including changes required by the Notice of Draftspers		D-948) attached
1) 🗌 hereto or 2) 🗌 to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner' Paper No./Mail Date		
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t		
7. DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT		
Attachment(s) 1. Notice of References Cited (PTO-892)	5 🔲 Notice of Informal	Patent Application (PTO-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summar	
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3. Information Disclosure Statements (PTO-1449 or PTO/SB/ Paper No./Mail Date	Jo), 7. 📋 Examiner's Ameno	
4. Examiner's Comment Regarding Requirement for Deposit		nent of Reasons for Allowance
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DETAILED ACTION

Remarks

- 1. The objection to claims 1, 9 and 17 is withdrawn.
- 2. The corrected drawings filed 10/8/2002 have been approved.

Allowable Subject Matter

- 3. Claims 1-4, 7-12, 15 and 17-27 are allowed.
- 4. The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Jaso et al. to US 6,093,631, teaches a method, comprising:

- etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14 between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);
- filling the dummy trenches 20 and the first 15d and the series of second trenches
 15a/15b/15c with a conductive material 16 (i.e. copper or aluminum or tungsten)(
 Fig. 11C and col.7, lines 3-7); and
- polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c.

In contrast, Jaso et al. at least neither teach nor suggest that the *second* trenches is a relatively narrow compared to the first trench and that polishing the conductive material by applying a liquid substantially *free of particulate matter* between an abrasive polishing surface and the conductive material.

Therefore, the instant invention is neither anticipated nor rendered obvious over the prior art of record.

Application/Control Number: 09/779,123 Art Unit: 2823

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday $(8:00 \sim 6:00)$.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HSIEN-MING LEE PRIMARY EXAMINER 9/21/2004

Hsien-Ming Lee **Primary Examiner**

Sep. 21, 2004

Issue Classification			09/779,123 SETH			Applicant SETHUR Art Unit	nt(s) RAMAN ET AL.							
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Page 308 of 329

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	Examiner Name	Hsien Ming Lee	
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SAMSUNG EXHIBIT 1004 Samsung v. Invensas

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FIG. 7

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FIG. 8

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Sethuraman et al.

Serial No. 09/779,123 Filed: February 7, 2001

Patent No. 6,849,946 Issued: February 1, 2005

For: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT Atty. Docket No. 5298-02502

Group Art Unit: 2823

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on the date indicated below:

TRANSMITTAL LETTER

Certificate

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of Correction

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313

Dear Sir:

Transmitted herewith for filing in the captioned case are the following:

- Form PTO-1050, submitted in duplicate. Errors which occur at important points in the captioned patent or which may otherwise affect the understanding or interpretation of the patent are thereon corrected.
- (2) A return postcard to acknowledge receipt of these materials. Please stamp and return this postcard to the undersigned.

All of the errors shown in PTO-1050 are due to Patent Office oversights. A Certificate of Correction is requested under 35 U.S.C. § 254. Applicants believe that no fees are required, however, should any fees be required, please deduct them from deposit account number 50-3268/5298-02502.

Respectfully submitted,

Molle E. Lettarg

Mollie E. Lettang Reg. No. 48,405 Agent for Applicant(s)

Daffer McDaniel, LLP P.O. Box 684908 Austin, TX 78768-4908 (512) 476-1400 Date: October 27, 2005

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SAMSUNG EXHIBIT 1004 Samsung v. Invensas

Page 313 of 329

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. 6,849,946

DATED: February 1, 2005

INVENTOR(S): Sethuraman et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

Claim 3 at col. 9, line 28: Please delete "relatively narrow."

Claim 12 at col. 10, lines 10-11: Please delete "conducts" and substitute therefor -- conductors --.

Claim 18 at col. 10, lines 48: Please delete "conducts" and substitute therefor -- conductors--.

MAILING ADDRESS OF SENDER: Mollie E. Lettang DAFFER McDANIEL, LLP P.O. Box 684908 Austin, TX 78768-4908 PATENT NO. <u>6.849,946</u> No. of add'l. copies

Page 1 of 1

Certificate of Correction (PTO Form 1050)

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. 6,849,946

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DATED: February 1, 2005

INVENTOR(S): Sethuraman et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

Claim 3 at col. 9, line 28: Please delete "relatively narrow."

Claim 12 at col. 10, lines 10-11: Please delete "conducts" and substitute therefor -- conductors--.

Claim 18 at col. 10, lines 48: Please delete "conducts" and substitute therefor -- conductors--.

MAILING ADDRESS OF SENDER: Mollie E. Lettang DAFFER McDANIEL, LLP P.O. Box 684908 Austin, TX 78768-4908 PATENT NO. <u>6,849,946</u> No. of add'l. copies

Page 1 of 1

Certificate of Correction (PTO Form 1050)

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Page 315 of 329

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,849,946 B1 DATED : February 1, 2005 INVENTOR(S) : Sethuraman et al. Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

1

Column 10, Lines 10-11 and 48, delete "conducts" and substitute -- conductors --.

Signed and Sealed this

Third Day of January, 2006

JON W. DUDAS Director of the United States Patent and Trademark Office

Case 1:16-cv-01033-LPS-CJB Document 3 Filed 11/07/16 Page 1 of 1 PageID #: 124

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DOCKET NO.	DATE FILED 11/7/2016	U.S. DISTRICT COURT District of Delaware				
PLAINTIFF Invensas Corporation			DEFENDANT Avago Technologies Limited, Avago Technologies U.S. Inc., Emulex Corporation, LSI Corporation, and PLX Technology Inc.			
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK				
i US 6,849,946 B2	2/1/2005	Invensas Corporation				
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In the above-entitled case, the following patent(s)/ trademark(s) have been included:

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In the above-entitled case, the following decision has been rendered or judgement issued:

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Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

Trials@uspto.gov 571-272-7822

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Paper 7 Entered: March 15, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BROADCOM LTD., BROADCOM CORP., AVAGO TECHNOLOGIES LTD., and AVAGO TECHNOLOGIES U.S., INC., Petitioner,

v.

INVENSAS CORP., Patent Owner.

Case IPR2017-00107 Patent 6,849,946 B2

Before MICHAEL R. ZECHER, LYNNE E. PETTIGREW, and KAMRAN JIVANI, *Administrative Patent Judges*.

JIVANI, Administrative Patent Judge.

DECISION Denying Institution of Inter Partes Review 35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

Page 318 of 329

I. INTRODUCTION

Broadcom Ltd., Broadcom Corp., Avago Technologies Ltd., and Avago Technologies U.S., Inc. (collectively, "Petitioner") requested, on October 18, 2016, an *inter partes* review of claims 16–20 and 22 (the "Challenged Claims") of U.S. Patent No. 6,849,946 B2 (the "'946 patent"). Paper 1 ("Petition" or "Pet."). On January 27, 2017, Patent Owner, Invensas Corp., filed a Preliminary Response. Paper 6 ("Prelim. Resp."); *see also* Paper 4, 1 ("Patent Owner's Mandatory Notices").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless it is determined that there is a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition. Applying this standard, we are not persuaded Petitioner has shown a reasonable likelihood that it would prevail with respect to at least one of the Challenged Claims because the Petition does not account properly for all the limitations recited in independent claim 16. Accordingly, we deny the Petition and decline to institute *inter partes* review of the Challenged Claims for the reasons set forth below.

II. BACKGROUND

A. The '946 patent (Ex. 1001)

The '946 patent relates to manufacturing interconnects in integrated circuits. Ex. 1001, 1:14. A process known as chemical-mechanical polishing ("CMP") is used to form a planarized layer during manufacturing of integrated circuit interconnects. *Id.* at 1:53–59. The '946 patent describes undesirable elevational disparities that may result during this process, making it difficult to print high resolution features. *Id.* at 1:31–52. In

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particular, the '946 patent describes two such disparities: (i) metal "dishing" and (ii) oxide erosion. Figure 4 of the '946 patent is reproduced below.



According to the '946 patent, Figure 4 depicts a series of relatively narrow interconnects 36 formed in narrow trenches and a relatively wide interconnect 38 formed in a wide trench. *Id.* at 2:58–62. The narrow interconnects 36 electrically connect underlying active devices with conductive elements of the semiconductor. *Id.* at 2:62–64. The wide interconnect 38 serves as, *inter alia*, a bond pad. *Id.* at 2:64–65.

Recessed area 42 depicts a localized thinning or "dishing" problem experienced by conventional metal CMP processes. *Id.* at 2:38–39, 3:3–4. The metal dishing causing recessed area 42 results from the polishing pad used in the CMP process flexing or conforming to initial deformities in the metal used to create interconnect 38. *Id.* at 3:4–24.

Recessed area 40 depicts a disparity known as oxide erosion. *Id.* at 3:26–28. Dielectric 20 is composed of silicon oxide. *Id.* at 3:28–29. During the CMP process, an abrasive chemical is used to polish the metal of narrow interconnects 36. *Id.* at 3:29–32. A component of this chemical reacts with the metal at a faster rate than with the silicon oxide, creating metal "steps" below the level of the oxide. *Id.* at 3:29–37. The polishing pad used in the

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CMP process removes oxide surrounding the "steps," resulting in recessed area 40. *Id.* at 3:37-44.

The '946 patent seeks to avoid metal dishing and oxide erosion through "a polishing process which can achieve global planarization across the entire topological surface of an interconnect level." *Id.* at 3:45–47. The '946 patent discloses "placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide interconnect and another region defined by a series of relatively narrow interconnect." *Id.* at 4:1–5. Figure 7 of the '946 patent is reproduced below.



Figure 7 depicts a series of relatively narrow interconnects 66, a series of dummy conductors 68, and a relatively wide interconnect 72. *Id.* at 7:42–46. Dummy conductors 68 and interposing dielectric protrusions 70 "replace a relatively wide dielectric region absent of any conductive material," such as area 44 of Figure 4. *Id.* at 5:31–34.

According to one embodiment, dummy conductors 68 are formed by etching dummy trenches into the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. *Id.* at 4:14–16. "The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively." *Id.* at 4:20–23. Conductive material is then

deposited in the dummy trenches forming dummy conductors, which "serve no purpose except to improve the planarization of the interconnect level in which they reside." *Id.* at 4:29–42.

The '946 patent describes dummy conductors 68 as preventing metal dishing because the metal of the dummy conductors is softer than the surrounding dielectric and, therefore, does not cause flexing or contracting of the polishing pad during the CMP process. *Id.* at 5:34–45. The '946 patent further describes dummy conductors 68 as preventing oxide erosion because the metal dummy conductors "may continue to be polished more rapidly than" the surrounding dielectric. *Id.* at 5:47–51. This allows dummy conductors 68 and narrow interconnects 66 to be polished down to a consistent level below the surrounding dielectric, which is itself "again made substantially coplanar with the dummy conductors and the interconnect." *Id.* at 5:51–60.

B. Illustrative Claim

Claim 16 is the only independent claims at issue. Claim 16 is representative of the Challenged Claims and reproduced below with additional spacing added.

16. A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches,

wherein each of the second trenches is relatively narrow compared to the first trench and

wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the

first trench and greater than a lateral dimension of at least one of the series of second trenches;

dummy conductors in said laterally spaced dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of second trenches and said first trench,

wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Ex. 1001, 10:23–40.

C. Evidence Relied Upon

Petitioner relies on the following references:

- Takahashi, U.S. Patent No. 5,948,573, issued Sept. 7, 1999 (Ex. 1003, "Takahashi").
- Iijima et al., U.S. Patent No. 5,529,954, issued June 25, 1996 (Ex. 1004, "Iijima").
- Kishii, Japanese Patent Publication No. H08-264534, published Oct. 11, 1996 (Ex. 1008, "Kishii").

Petitioner further relies on the Declaration of Dr. Joseph Cecchi (Ex. 1009, "Cccchi Declaration").

D. Proposed Grounds of Unpatentability

Petitioner argues the following grounds of unpatentability (Pet. 3-4):

Reference(s)	Grounds	Challenged Claim(s)
Takahashi	§ 102(b)	16–20
Takahashi and Iijima	§ 103(a)	22

Reference(s)	Grounds	Challenged Claim(s)
Kishii	§ 103(a)	16–19
Kishii and Takahashi	§ 103(a)	20
Kishii and Iijima	§ 103(a)	22

E. Related Proceedings

Patent Owner identifies the following litigations involving the '946 patent: *Tessera, Inc. v. Broadcom Corp.*, No. 1:16-cv-00379-LPS-CJB (D. Del.), filed on May 23, 2016 and *Invensas Corp: v. Avago Technologies Ltd.*, No. 1:16-cv-01033-LPS-CJB (D. Del.), filed on Nov. 8, 2016. *See* Patent Owner's Mandatory Notices, 1. Patent Owner further identifies the following investigation involving the '946 patent: *In the Matter of Certain Semiconductor Devices, Semiconductor Device Packages, and Products Containing Same*, Inv. No. ITC-337-TA-1010. *Id.*

III. CLAIM CONSTRUCTION

"A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b); *see also Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard as the claim construction standard to be applied in an *inter partes* review proceeding). When applying that standard, we interpret the claim language as it would be understood by one of ordinary skill in the art in light of the specification. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed.

Cir. 2010). Thus, we give claim terms their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning 'is the meaning that the term would have to a person of ordinary skill in the art in question."").

Neither Petitioner nor Patent Owner asks us to construe any terms of the Challenged Claims. Pet. 14; Prelim. Resp. 23. Only terms which are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.,* 200 F.3d 795, 803 (Fed. Cir. 1999). Accordingly, we do not interpret expressly any claim term and instead simply read the claims according to the standards set forth above.

IV. ANALYSIS

A. Anticipation of Claim 16 by Takahashi

Independent claim 16 recites in relevant part "wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches" (hereinafter the "Dimensional Limitation"). Petitioner contends Takahashi anticipates claim 16, citing testimony from Dr. Cecchi and pointing to Takahashi's Figure 4B as meeting the Dimensional Limitation. Pet. 19 (citing Ex. 1003, Fig. 4B, Ex. 1009 ¶ 82). Dr. Cecchi's testimony, in turn, relies only upon Takahashi's Figure 4B as meeting the Dimensional Limitation. Ex. 1009 ¶ 82 (citing Ex. 1003 Fig. 4B).

Patent Owner contends that Petitioner's reliance upon Takahashi's Figure 4B is insufficient. Prelim. Resp. 32. We agree with Patent Owner.

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"[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (internal citations omitted). Petitioner fails to identify passages of Takahashi's specification describing the proportions of Figure 4B in sufficient detail so as to anticipate the Dimensional Limitation. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claim 16 as anticipated by Takahashi.

B. Anticipation of Claims 17–20 by Takahashi

Claims 17–20 directly depend from independent claim 16. Petitioner's analysis of these dependent claims under Takahashi fails to repair the deficiencies in the analysis of claim 16 described above. Pet. 24– 29; *see supra* Section IV.A. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 17–20 as anticipated by Takahashi.

C. Obviousness of Claim 22 over Takahashi and Iijima

Claim 22 directly depends from independent claim 16. Petitioner's analysis of dependent claim 22 as rendered obvious by the combination of Takahashi and Iijima fails to repair the deficiencies in the analysis of claim 16 described above. Pet. 29–32; *see supra* Section IV.A. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claim 22 as obvious over the combination of Takahashi and Iijima.

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D. Obviousness of Claim 16 over Kishii

Petitioner contends Kishii renders obvious claim 16, citing testimony from Dr. Cecchi and pointing to Kishii's Figures 4B and 4C as teaching or suggesting the Dimensional Limitation. Pet. 37–38 (citing Ex. 1008, Figs. 4B and 4C, Ex. 1009 ¶ 105). Dr. Cecchi's testimony, in turn, relies only upon Kishii's Figure 4B as meeting the Dimensional Limitation. Ex. 1009 ¶ 105 (citing Ex. 1008, Fig. 4B).

Patent Owner contends that Petitioner's reliance upon Kishii's Figures 4B and 4C is insufficient. Prelim. Resp. 32. We agree with Patent Owner. As discussed above, "it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." Hockerson-Halberstadt, 222 F.3d at 956. Petitioner fails to identify passages of Kishii's specification describing the proportions of Figures 4B and 4C in sufficient detail so as to teach or suggest the Dimensional Limitation. Further, we note Dr. Cecchi does not testify as to why one of ordinary skill in the art would have understood Figures 4B and 4C as teaching or suggesting the Dimensional Limitation. See Ex. 1009 ¶ 105. Rather, Dr. Cecchi summarily asserts that "FIG. 4B illustrates" the Dimensional Limitation without directing us to portions of Kishii's specification or other evidence that would warrant such a finding. Id. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claim 16 as obvious over Kishii.

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E. Obviousness of Claims 17–20 over Kishii alone or with various other references

Claims 17–20 and 22 directly depend from independent claim 16. Petitioner's analysis of these dependent claims as obvious over Kishii, either alone or in combination with other references, fails to repair the deficiencies in the analysis of claim 16 described above. Pet. 41–50; *see supra* Section IV.D. On this evidentiary record, we determine Petitioner has not established a reasonable likelihood of success in challenging claims 17–20 and 22 as obvious over Kishii, either alone or in combination with other references.

V. SUMMARY

We determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on its challenges to claims 16–20 and 22.

VI. ORDER

It is, therefore,

ORDERED that the Petition is denied and no trial is instituted.

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