

Framework for Characterization of Copper Interconnect in Damascene CMP Processes

by

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Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degrees of

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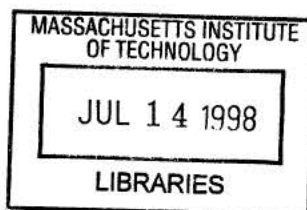
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Abstract

Aluminum interconnect has started to reach its performance and process limits for high performance circuits, and the new copper interconnect is being developed using a damascene or in-laid metal process with chemical mechanical polishing (CMP). Understanding process and integration issues as well as problems is critical in successfully developing copper metallization. To characterize in-laid metal polishing behaviors, a methodology is developed that builds upon the statistical metrology framework for oxide polishing. Previous works show characterizations of pattern dependencies for copper damascene CMP planarization but do not clearly examine important parameters such as density and interaction distance. The degree of dishing within individual copper lines and erosion (undesired polishing of surrounding oxide), two primary pattern dependencies, depends strongly on the specifics of the pattern being polished. This pattern dependency is a difficult implementation and process integration obstacle, with both yield and circuit performance impact. The central focus of this thesis is the development of methods to characterize and understand these pattern dependencies in copper CMP. This new methodology is carried out by experiments using a CMP characterization mask set and a newly designed electrical test mask through a collaborative work with SEMATECH.

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Chapter 1

Introduction

1.1 Background

As the technology in the semiconductor industry has improved to sub-micron dimensions, metallization and interconnect have begun to play a critical role in determining the performance of modern VLSI circuits. Traditionally, aluminum has been used in metal interconnect: adequate material properties and the ease of processing and integration have made it the metal of choice for over a decade. However, aluminum interconnect has started to reach its performance and process limits for high performance circuits. For example, its poor immunity to electromigration has made it more and more difficult to achieve the necessary high current densities with metal lines of sub-micron critical dimensions (CD), and fine metal lines are becoming harder and harder to pattern and etch. More importantly, the resistivity of aluminum lines limits the fundamental speed of signal propagation.

Thus, the need for a better conducting and more reliable material has become an important issue and motivates the development of copper interconnect for future technologies. Copper has many material advantages compared to aluminum. First, copper has lower resistivity than aluminum, with a resistivity of about $1.7 \mu\Omega\text{-cm}$ [1] compared to conventional aluminum interconnect with a resistivity of about $3.0 \mu\Omega\text{-cm}$ (99.5% Al/0.5% Cu) [2]. Second, copper has better electromigration performance than aluminum and is much more reliable for comparable current densities: aluminum has an electromigration limit of approximately 10^6 A/cm^2 , while copper is about 10 times better (10^7 A/cm^2) [2]. Another advantage of copper is that it is less susceptible to joule heating [2].

These material advantages directly translate to performance and reliability advantages. Reduced resistance of copper enables faster interconnect and chip speed. Another advantage is the reduced number of metal levels required for a given circuit. Because copper is more conductive and has higher electromigration resistance, it is possible to have narrower (smaller CD) interconnect lines with the same current density. It is projected that for 0.10 μ m technology, traditional aluminum interconnect will require 14 levels of metal while copper interconnect will only require about 12 levels [1]. Furthermore, the transition to copper interconnect from aluminum has a manufacturing cost reduction and benefit primarily through reduction or elimination of expensive process steps. In particular, copper interconnect formed using a damascene process will replace expensive or difficult inter-layer dielectric (ILD) polish and metal etch steps with oxide etch and metal polish. In addition, via deposition and aluminum line deposition steps will be replaced with a single copper deposition step in the dual damascene process.

1.2 Copper Metallization Process

Unlike traditional metallization of aluminum, where aluminum is deposited on top of ILD, patterned, and etched, copper metallization requires a different process because copper is almost impossible to etch. This alternative metal patterning approach is known as a damascene process. The name “damascene” is derived from the ancient artisans of Damascus who practiced the creation of metal patterns using an inlaid technique. In the modern semiconductor damascene process, ILD is first deposited and patterned to define “trenches” where the metal lines will lie. Then, metal is deposited to fill the patterned oxide trenches and polished to remove the excess metal outside the desired lines using chemical-mechanical polishing (CMP).

As mentioned, a key advantage of the damascene process is the elimination of the metal etch process. The second advantage is the better control of oxide CD patterning as opposed to metal CD patterning. A third advantage is the elimination of gap fill difficulties: as the pitch decreases to the deep sub-micron regime, it becomes harder and harder to fill small spaces between patterned metal lines with oxide dielectric. Finally, the damascene process eliminates the need for multiple oxide layer polishing steps, which can be quite expensive and time consuming; instead each interconnect layer is already planar in the damascene case.

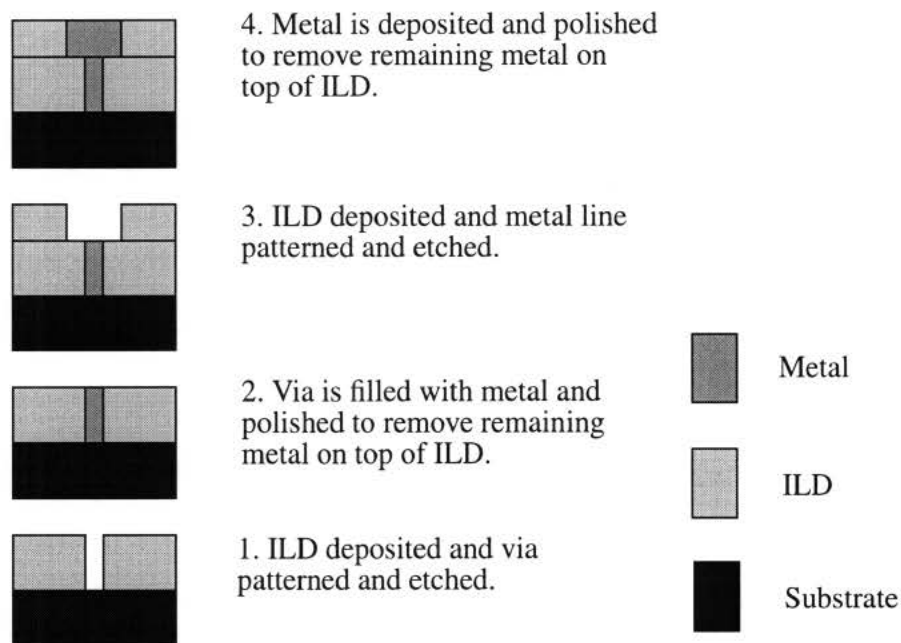


Figure 1.1: Single Damascene Process

Damascene processes can be divided into two types: single and dual damascene. As shown in Figure 1.1, two separate ILD deposition, patterning, and polishing sequences are used for metal lines and vias in the single damascene process. These two separate sequences are combined in the dual damascene process; Figure 1.2 shows three variations

of the dual damascene technique. In (a), a metal line is patterned first and then a via is patterned; a drawback is that developing and etching through the high aspect ratio photoresist is difficult for the via formation. In variant (b), a via is first patterned and then etched to solve the problem in (a), but the ashing or removal of photoresist in the via may be difficult. These two sequences also suffer from inaccurate stop or control of the trench depth. In Figure 1.2 (c), a silicon nitride layer is used as a via hard mask for the simultaneous etching of metal lines and vias. All three variants use only one metal fill and require at least two etches (i.e. in case (c), the etch stop has to be patterned).

Although the damascene process has many advantages compared to the conventional aluminum metallization, it has several process and integration difficulties and challenges. One such challenge is diffusion barrier layer formation for copper, necessary because copper diffuses readily into silicon. Ti, TiN, Ta, and TaN are some of the more common barrier layers under study. Besides being a good diffusion barrier layer to copper, the trench and via “liner” must also be thin so that it does not negatively impact the resistance of a metal line by reducing the effective line width and thickness. The liner also must be thin to minimize the contact resistance of contact holes and vias. Another challenge is developing and finding the best deposition technique for copper. Various techniques such as PVD, CVD, and electroplating are being researched [3, 4]. Furthermore, polishing of copper is crucial for process development and integration; the problems associated with copper polishing are described in detail in the following section.

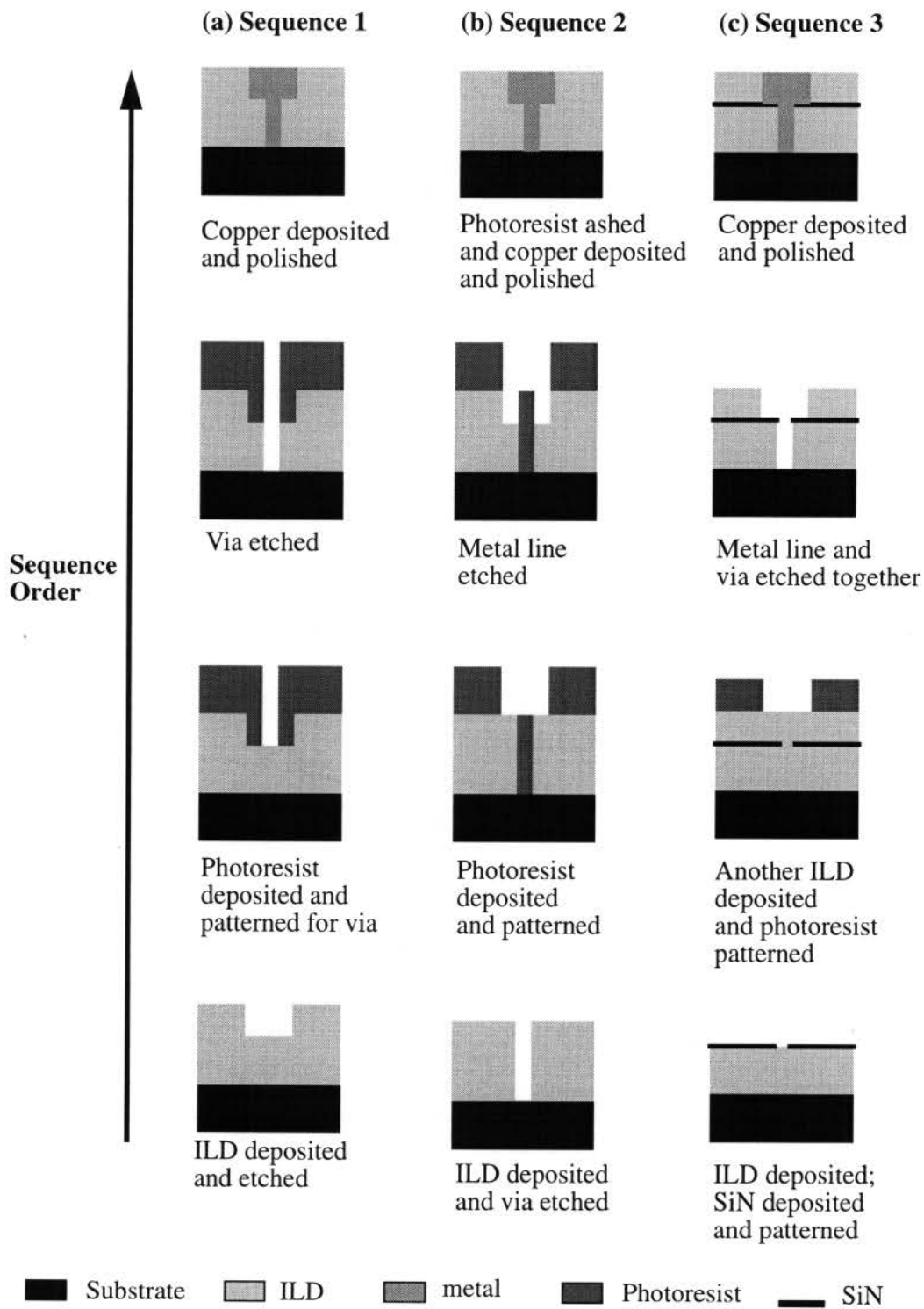


Figure 1.2: Dual Damascene Process [5]

1.3 Copper CMP Problems and Previous Work

CMP technology is already widely applied to ILD planarization [6, 7] as well as to metal planarization such as tungsten plugs [8, 9]. Oxide polishing has been extensively researched in both process and integration aspects, and the oxide planarization process is comparatively well understood. However, relatively little research has been reported on the copper damascene CMP process. The copper damascene CMP process is now in the development phase in industry to resolve various issues such as process integration, reliability, defect generation, and yield.

As mentioned in the earlier section, CMP planarization of the deposited copper poses another challenge. After patterning and etching trenches in oxide and depositing a barrier layer, copper is deposited over the entire wafer as shown in Figure 1.3. Then, CMP is used to polish away all the unwanted copper above the oxide region, and copper is left only in trenches and vias.

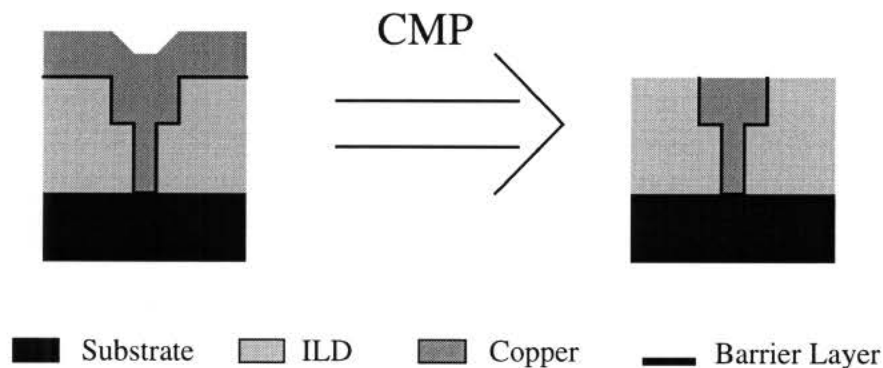


Figure 1.3: Copper Deposition and CMP Planarization

Ideally, the polished copper should be perfectly flat; unfortunately, an important non-ideality is that copper lines suffer from dishing and erosion due to CMP. Figure 1.4 shows a cross sectional view of the ideal case and a comparison to a realistic case suffering from

dishing and erosion. Dishing is defined as the recessed height of a copper line compared to the neighboring oxide, and erosion is defined as the height of polished oxide from its original thickness. To be more precise and consistent in the definition which varies in the literature, in this work the recessed height of a copper line for determination of dishing is measured at the lowest point in the line which is most typically at the midpoint of the copper line. Dishing also occurs within copper lines in eroded oxide regions. When erosion is also present, dishing is still measured from the most recessed copper level to the neighboring oxide right next to the copper line, not to the original oxide height against which erosion is measured. Erosion is always measured from the original oxide height to the most eroded point (again typically in the middle of the region of interest).

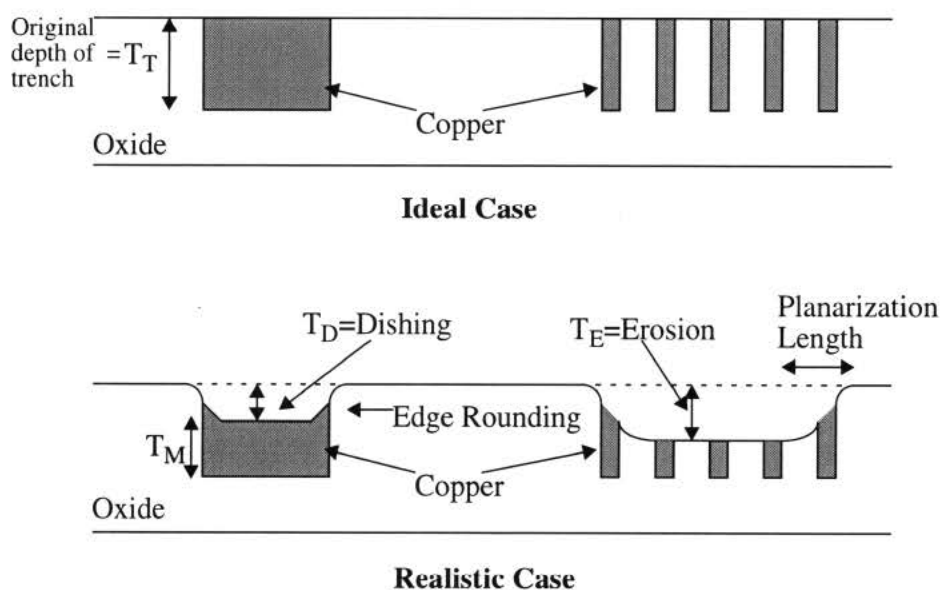


Figure 1.4: Ideal case vs. dishing and erosion in realistic copper polishing

In addition to the process and integration difficulties due to dishing and erosion, these pattern dependent variations severely affect line resistance and thus impact circuit performance. The sheet resistance of patterned copper lines is inversely proportional to the

thickness of the metal: $R_s = \rho/t$ where ρ is resistivity and t is metal thickness. The total remaining metal line thickness T_M is simply

$$T_M = T_T - (T_D + T_E) \quad (1.1)$$

where T_E is erosion depth, T_D is dishing depth, and T_T is the intended or patterned trench depth.

Previous work [10] by Steigerwald has shown strong pattern effects of pitch and density on dishing and erosion phenomena, respectively. His work also involved chemical and electrochemical analysis of copper polish. These pattern dependent variations are also reported by Landis [11]. However, these works do not examine the important concept of interaction distance which determines the region in which the pattern density should be computed [12]. Without a clear notion of this region, one can not clearly define pattern density. For example, even if a test structure which is $500\mu\text{m} \times 500\mu\text{m}$ is designed for 50% density, the effective density at the center of that structure might be different if the window size (interaction distance) exceeds the structure size; the neighboring environment may well have an impact on the effective density of the structure. These works also do not include sub-micron linewidths and line spaces which are the dimensions of interest for current technology. Additional work has been published that focuses on novel characterization of proximity effects of wide bus lines on the polishing of narrow metal lines [13]; work is needed to relate these effects to general density, linewidth, and line space effects.

1.4 Overview of Statistical Metrology and Oxide CMP Work

As mentioned earlier, Chemical Mechanical Polishing (CMP) has already become a dominant technology for multilevel interconnect planarization and is widely used in development and manufacturing environments. Here at MIT in the Statistical Metrology group,

the initial focus of research has been on characterizing and modeling pattern dependencies in CMP processes for ILD planarization using a statistical metrology framework [14].

Statistical metrology is a methodology to understand semiconductor fabrication process variations [15, 16, 17, 18]. This methodology identifies sources of variations, characterizes, and models these variations. In order to accomplish this task, the use of four basic elements are emphasized [19]. First, high throughput measurements (electrical or physical) are emphasized to obtain a large amount of statistically significant data. Second, short flow process steps are used to isolate the sources of variation so that variation analysis is simplified. Third, statistical design of experiments is incorporated to accurately identify and characterize variations that one seeks to find. Finally, technology computer aided design (TCAD or process/device simulation) tools are used to confirm electrical measurements and to extract or convert them to measurements of physical structures (e.g. capacitance to thickness).

Statistical metrology itself has three main components: variation assessment, variation modeling, and variation impact analysis. Variation assessment deals with understanding the source and amount of variation by answering two questions: where and how much? Variation modeling involves characterizing variations by systematically decomposing them into die-level, wafer-level, and other components. It also models any spatial and temporal process variations as a function of such factors as layout structures, process conditions, or equipment parameters. The final component of statistical metrology involves analysis of the circuit impact due to these variations.

After performing statistical experiments with well-defined process and analysis variables, and validating/extracting data to a proper format, statistical analysis (e.g. ANOVA) is performed to capture significance of different factors. Data decomposition is also used to filter raw data to wafer-level, die-level, wafer-die interactions, and residuals so that the

sources of variation can be separated [20, 21]. After careful analysis of filtered data, parameters of interests (e.g. ILD thickness) are examined as a function of process or layout variables (e.g. density). Then, an empirical model can be developed based on characterization across broad ranges of processes and variables, and the developed model can be used to predict outcomes of parameters for different processes, consumables, and layouts or products. These models can also be utilized to determine the impact of process variations on circuit performance.

Using this statistical metrology framework, a characterization mask set has been developed jointly by MIT, Sandia National Laboratories, and HP to understand the planarization characteristics of oxide CMP for various pattern effects including area, pitch, density, and aspect ratio [22]. Furthermore, a closed form model for ILD thickness variation has been developed based on the effect of pattern density which has the most prominent effect on ILD thickness variation [12, 23]. The model is being expanded to account for inlaid or dual material polishing processes such as shallow trench isolation (STI), where both oxide and nitride undergo polishing.

1.5 Contribution and Scope of This Thesis

This thesis builds upon the previous statistical metrology framework for oxide polishing to contribute a methodology for inlaid metal polishing characterization. Previous works show characterizations of pattern dependencies for copper damascene CMP planarization but do not clearly examine important parameters such as density and interaction distance as discussed earlier. The degree of dishing and erosion depends strongly on the specifics of the pattern being polished. This pattern dependency is a difficult implementation and process integration obstacle, with both yield and circuit performance impact. The central focus of this thesis is the development of methods to characterize and understand

these pattern dependencies in copper CMP. This new methodology is carried out by experiments using the characterization mask set and a newly designed electrical test mask through a collaborative work with SEMATECH.

1.6 Thesis Organization

This thesis is organized into three parts. First, Chapter 2 describes the statistical metrology framework used to characterize pattern dependency in inlaid metal planarization. This chapter also describes the overall copper development project through SEMATECH, including description of masks, process flow and splits, and an overview of metrology issues. Second, Chapter 3 contains the new electrical mask design and metrology, and discusses the extraction of copper line thickness from electrical resistance measurements. Third, Chapter 4 describes an experiment with the characterization mask set, measurement results, and data analysis of different pattern effects. Finally, Chapter 5 summarizes the work presented in this thesis and comments on limitations in the current mask design and improvements for the future electrical test mask. Future work and directions are also suggested at the end of this chapter.

Chapter 2

Methodology and Experimental Overview

This chapter describes the development of the statistical metrology methodology used to characterize and understand pattern dependency in copper interconnect planarization using the damascene process. This framework falls into the variation assessment part of statistical metrology described in Chapter 1. The new methodology consists of three stages: layout factor identification/selection, test structure and mask design, and finally characterization methods. First, the layout factor identification/selection focuses on identifying and selecting key layout patterns based on previous oxide CMP experiments [24] and previous research on inlaid metal polish [10, 25]. Second, test structure and mask design focus on appropriate test structure design and mask floor planning to capture each pattern dependency without being confounded with other patterns or structures. Finally, characterization methodology focuses on metrology and characterization methods for parameters of interest (e.g. copper thickness extraction from line resistance measurement).

This inlaid metal polish characterization methodology is demonstrated through an experiment carried out with SEMATECH which is introduced in this chapter and through the design of an electrical test mask specifically targeted to examine the pattern dependency in copper CMP. Section 2.1 explains the scope and different phases of the experiment, and Section 2.2 shows the short flow process and process splits used in the experiment. Then the following section, Section 2.3, investigates mask issues and describes the characterization mask set in detail. Finally, Section 2.4 comments on overall metrology issues and methods.

2.1 Scope of Overall Experiment

The overall copper CMP characterization project conducted by and with SEMATECH consists of three phases. The first phase involves general screening experiments for different consumable sets using SEMATECH's internal mask. Candidate polishing pads and slurries are examined to narrow down the choices to a small number of promising consumable sets. At the same time, different diffusion barrier layers are examined to find one that gives good adhesion to oxide and the best planarity as well as the least leakage current. All these screening experiments were done with one specific CMP tool. The criteria for the best planarity was based on the measurement of dishing and erosion on different metal lines and density blocks on the mask. After these screening experiments, consumable sets are chosen which are then used for further examination.

In the second phase, after finding one or two viable choices for the consumable set, a process DOE is performed to find an optimal process point to further reduce and study dishing and erosion using both SEMATECH's internal mask and the MIT CMP characterization mask set. The process DOE experiment with the chosen consumable sets are carried out on different CMP tools for tool comparison as well. Furthermore, besides the chosen consumable choices, more consumable sets are run with different CMP tools so that consumable vendors and equipment companies would each have an opportunity to evaluate their consumable sets, CMP tools, and processes.

Finally, a newly designed electrical test mask, which is specifically targeted and optimized to examine pattern dependency in inlaid copper polishing, is used not only to examine pattern dependencies of dishing and erosion but to also perform yield and defect analysis. Previously mentioned masks do not contain electrical test structures designed to accomplish these dual characterization needs; rather, the previous masks primarily support

optical and profilometry measurements. The details of the electrical test mask design and individual test structures are described in Chapter 3.

Again, this project is conducted as part of SEMATECH's copper metallization development; this thesis specifically examines pattern dependencies. For proprietary reasons, specific details of polishing pads, slurries, and CMP machines, are not detailed in this thesis; rather this thesis will focus on the copper pattern dependency characterization methodology and demonstration.

2.2 Short Flow Process and Process Splits

A short flow process is carried out to simplify process steps and to minimize sources of variation from unwanted processes. To further reduce sources of variation and ease the process, a single damascene technique is used rather than a dual damascene technique. In fact, a simplified single damascene process was implemented without the contact hole (or via) layer to focus on the copper polish issues only. Multilayer issues are important in single or dual damascene process. The short flow process used in this experiment examines only one metal layer; after understanding the problems and difficulties with one layer, the pattern issues associated with a contact hole layer and dual damascene process can be studied.

All processes are carried out using 8" (200 mm) wafers. First, a thick oxide is deposited on a bare silicon substrate. Then, oxide is patterned and etched to form trenches for the metal lines. A barrier layer is deposited next, followed by copper deposition of a seed layer and copper electroplating. Then, the wafer is polished until all copper is completely polished away from the oxide surface. As a part of the experiment, different degrees of overpolish are also performed on a subset of wafers. This short flow process is shown in Figure 2.1.

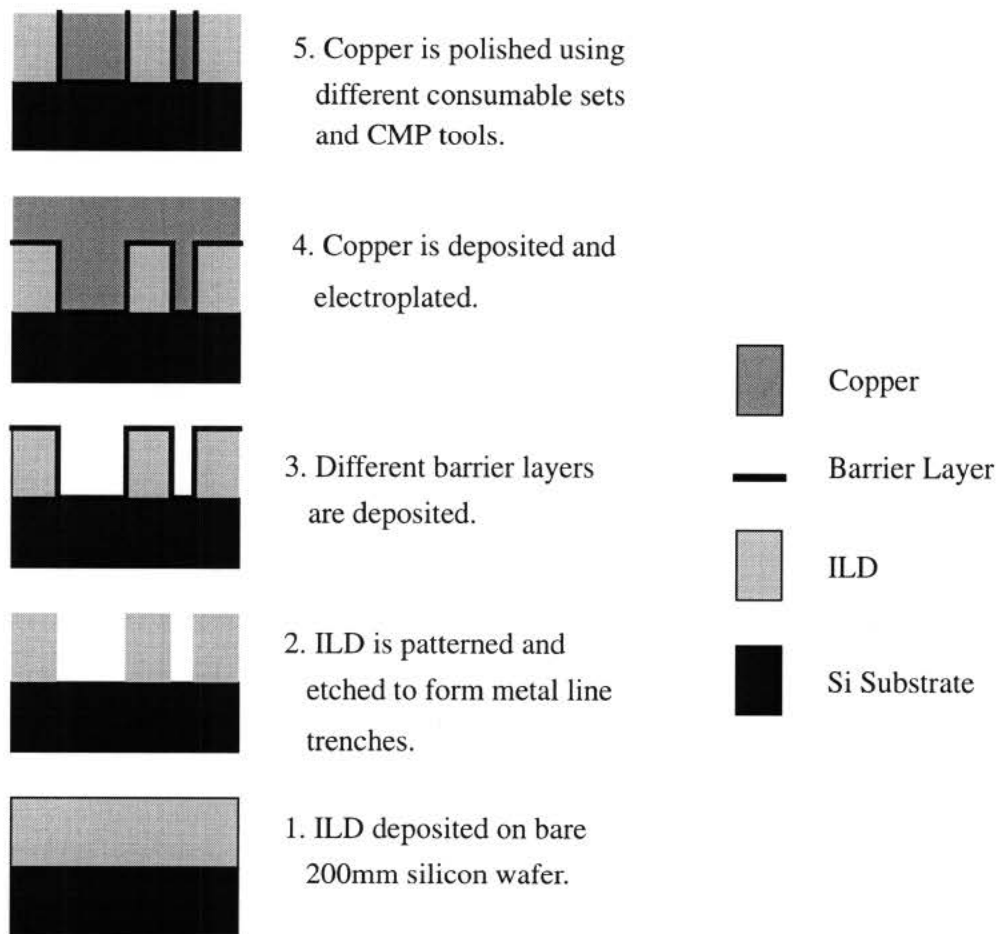


Figure 2.1: Short Flow Process

In this short flow process experiment, there are material splits and process splits. In material splits, different barrier layers are deposited for the wafers fabricated using SEMATECH's internal mask. These wafers are then polished using candidate consumable sets. In process splits, down force and table speed are varied (still maintaining the same removal rate) using different CMP tools with a specific consumable set assigned to each CMP tool. These process splits are done using wafers fabricated with a chosen barrier layer using the MIT density, area, and pitch masks.

2.3 Description of Masks

There are three mask sets used in the copper project: SEMATECH's internal mask, the MIT CMP characterization mask set, and the electrical test mask. The CMP characterization mask set is described below in detail, and the electrical test mask design is described in detail in Chapter 3. Each mask is a one-level mask. Due to contamination concerns, a polished copper wafer can only be reintroduced into a fabrication line for further process (e.g. oxide deposition for ILD) with great care. Since these masks are one-level masks, preliminary copper experimentation can be accomplished on conventional fab lines because the wafer need not re-enter for further processing after copper CMP. However, due to this limitation, the new electrical test mask has been designed as a one-level mask. A three-level mask set could also be designed to optimize the test vehicle, in which case, the first-level mask would have just the test structures without any bond pads, and the second-level mask would have contact holes to the third-level mask which would contain bond pads to make an electrical probe contact. Such three-level characterization masks is an area for future research.

The CMP characterization mask set is designed for rapid evaluation and characterization of CMP processes, consumables, and equipments. The mask set consists of four masks: area, pitch, density, and aspect ratio masks. As the name suggests, each mask is designed with one individual layout factor rather than with combined layout factors to target an individual source of contribution to CMP planarization variation. The four separate one-level masks are designed to examine structural area, line pitch, pattern density, and structure aspect ratio (or perimeter to area ratio) effects on CMP planarization. For rapid evaluation, these masks support a simplified metrology of optical film thickness and profilometry measurement. Each mask is designed with a 12mm x 12mm die size, but the lay-

out can be scaled to produce larger or smaller dies (e.g. 20mm x 20mm variants have also been made available).

The first mask, the area mask shown in Figure 2.2, has structures with varying sizes of area ranging from 20μm x 20μm to 3mm x 3mm. Each structure is filled with different patterns such as solid, 50% density lines, and metal 1 pattern of an conventional adder circuit. Table 2.1 shows the description of each structure.

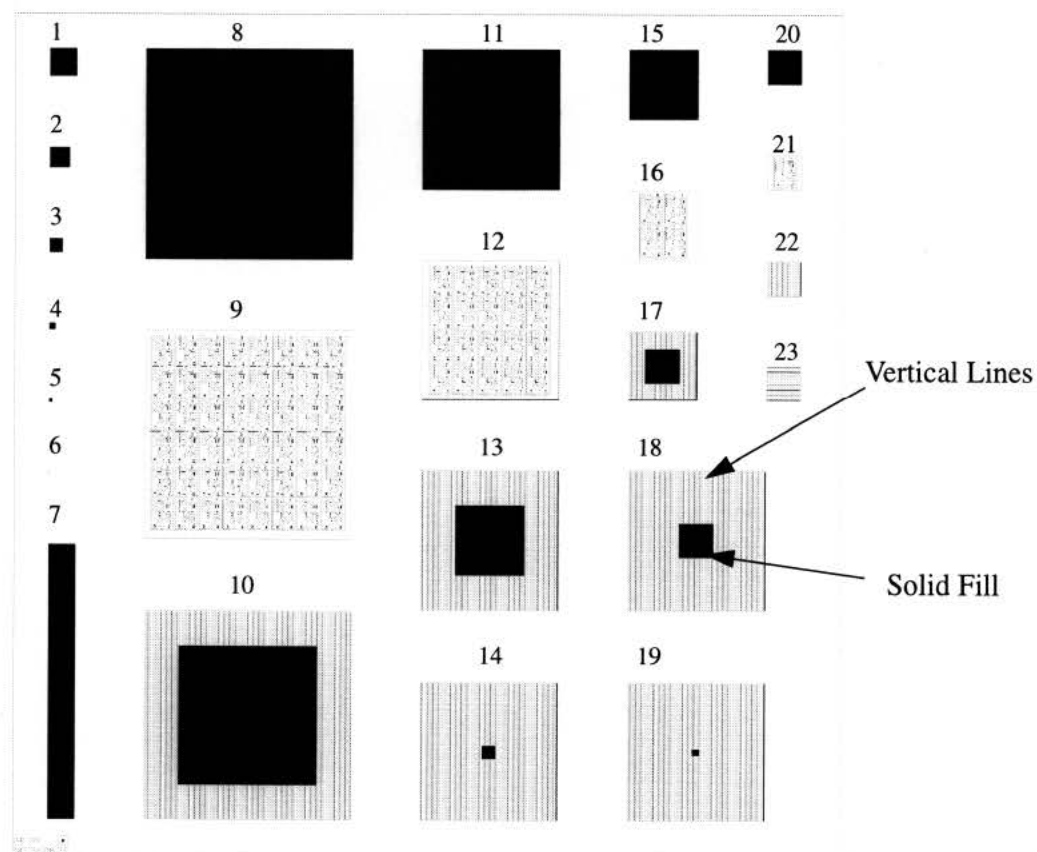


Figure 2.2: Area Mask. (A structure number is marked above each structure.)

Table 2.1: Area Mask Description

Structure No.	Size (μm)	Fill Pattern (μm)	Structure No.	Size (μm)	Fill Pattern (μm)
1	400 x 400	Solid	13	2000 x 2000	Vertical Lines with 1000 x 1000 solid
2	300 x 300	Solid	14	2000 x 2000	Vertical Lines with 200 x 200 solid
3	200 x 200	Solid	15	1000 x 1000	Solid
4	100 x 100	Solid	16	1000 x 1000	Adder Circuit
5	50 x 50	Solid	17	1000 x 1000	Vertical Lines with 500 x 500 solid
6	20 x 20	Solid	18	2000 x 2000	Vertical Lines with 500 x 500 solid
7	400 x 4000	Solid	19	2000 x 2000	Vertical Lines with 100 x 100 solid
8	3000 x 3000	Solid	20	500 x 500	Solid
9	3000 x 3000	Adder Circuit	21	500 x 500	Adder Circuit
10	3000 x 3000	Vertical Lines with 2000 x 2000 solid	22	500 x 500	Vertical Lines
11	2000 x 2000	Solid	23	500 x 500	Horizontal Lines
12	2000 x 2000	Adder Circuit			
Solid: Solid Block. Adder Circuit: metal 1 pattern of an adder circuit.					
Vertical Lines with ### x ### solid: Vertical lines (20μm in pitch) with specified solid metal fill in the center.					

The second mask, the pitch mask shown in Figure 2.3, has structures with different line pitch values ranging from 2μm to 1000μm, and each structure's density is fixed at 50%. There are a total of 36 structures, with each structure size of 2mm x 2mm. Replicates are used to separate spatial effects from purely pitch effects. Table 2.2 shows the description of each structure. One fixed pitch value of vertical lines for each structure is used,

except for the structure 26 where the pitch values are 2, 3, 4, 5, 6, 7, 8, 9, 10, and 15 μm from left to right with each block size of 200 μm x 2000 μm .

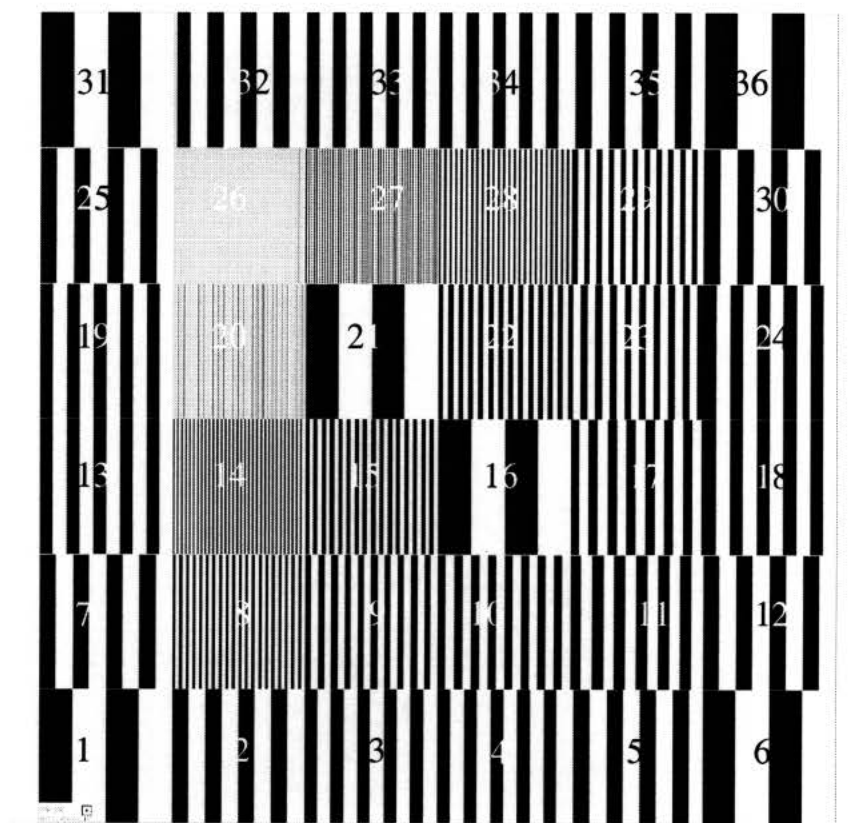


Figure 2.3: Pitch Mask. (A structure number is marked above each structure.)

Table 2.2: Pitch Mask Description

Structure No.	Pitch (μm)	Structure No.	Pitch (μm)	Structure No.	Pitch (μm)
1	1000	13	500	25	500
2	500	14	60	26	See Below
3	400	15	125	27	40

Table 2.2: Pitch Mask Description

Structure No.	Pitch (μm)	Structure No.	Pitch (μm)	Structure No.	Pitch (μm)
4	400	16	1000	28	80
5	500	17	285	29	180
6	1000	18	400	30	500
7	500	19	400	31	1000
8	100	20	20	32	500
9	200	21	1000	33	400
10	250	22	150	34	400
11	333	23	220	35	500
12	500	24	400	36	1000
Structure 26 contains 10 different pitch blocks. The pitch values are 2, 3, 4, 5, 6, 7, 8, 9, 10, and 15μm from left to right blocks. Each block is 200μm x 2000μm.					

The third mask, the density mask shown in Figure 2.4, has structures with varying local pattern densities from 4% (lower left corner) to 100% (upper right corner). Each block is 2mm x 2mm with a fixed pitch of 250μm, and the pattern density is increased gradually in increment of 4%. There is a 1mm wide border with a 50% density environment that acts as a buffer zone to reduce any strong interactions from a low density structure to a high density structure located in the next die. Table 2.3 shows the description of each structure.

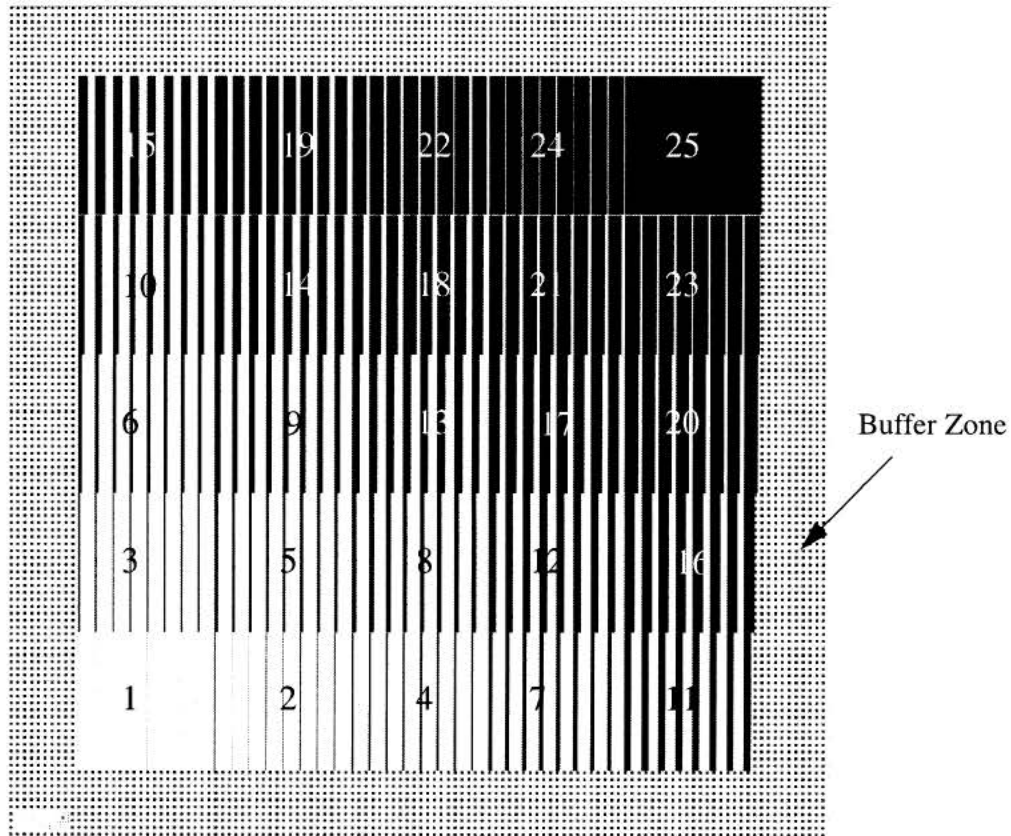


Figure 2.4: Density Mask. (A structure number is marked in the middle of each structure.)

Table 2.3: Density Mask Description

Structure No.	Density (%)	Structure No.	Density (%)	Structure No.	Density (%)
1	4	11	44	21	84
2	8	12	48	22	88
3	12	13	52	23	92
4	16	14	56	24	96
5	20	15	60	25	100
6	24	16	64		

Table 2.3: Density Mask Description

Structure No.	Density (%)	Structure No.	Density (%)	Structure No.	Density (%)
7	28	17	68		
8	32	18	72		
9	36	19	76		
10	40	20	80		

The fourth mask, aspect ratio mask, is not described in this thesis because it is not used in the experiment. This mask is not used because it was believed that there would be little effect of aspect ratio on inlaid copper polishing. Interested readers should consult the original CMP characterization mask set documentation [22] for more information on this mask as well as area, pitch, and density masks.

2.4 Metrology Issues

Measurement or metrology is often under-estimated in its importance and complexity but is a vital part in the statistical metrology framework. Besides the issues involving the actual method and tools used for measurement, the measurement capability is the limiting factor in test structure design and process. Wafers could be run with very fine features and complex designs, but if they are impossible or unreasonably difficult to measure, then the benefits of that design can not be realized. Thus, when designing a mask or even when running a process, understanding the limitation of each measurement tool is very crucial.

Measurement approaches for CMP pattern dependency characterization can be broadly divided into four categories: optical, profilometry, electrical, and AFM/SEM. Each technique has pros and cons, but by combining some or all of these techniques, the best result can be obtained.

2.4.1 Optical Interferometry and Ellipsometry

Optical interferometry and ellipsometry are commonly used to measure absolute film thicknesses. Tools in this category offer reasonable throughput with an automatic pattern recognition capability. One drawback in this technique is that it can not be used to measure metal thicknesses, which is a substantial limitation in the study of inlaid metal processes. Another limiting factor is the large spot size requirement of about $10\mu\text{m} \times 10\mu\text{m}$ ($20\mu\text{m} \times 20\mu\text{m}$ to be more confident in the measurement). Thus, small features less than $10\mu\text{m} \times 10\mu\text{m}$ can not be measured accurately with optical film measurement tools, particularly in an automatic fashion.

2.4.2 Profilometry

Another often used measurement tool is a profilometer. A profilometer uses a sharp stylus that scans across a surface of interest. Profilometry scans can be used in either 2-D or 3-D mode to get a single trace across a structure or to get a surface map over a region, respectively. In both cases, only the relative thickness is given. Due to stage tilt and wafer bow, measurements often suffer from leveling problems, especially when a long scan (greater than approximately $500\mu\text{m}$ to $1000\mu\text{m}$) is taken. This leveling problem can be corrected by taking several optical thickness measurements where the profilometry scan is taken and by forcing the profilometry trace to match the optical measurements. The accuracy of correction is determined by the number of optical measurements. About five measurement sites are needed to correct linear leveling problems, but more measurement sites may be needed to correct non-linear leveling problems. The resolution of a conventional profilometer due to the size of the stylus tip is limited to structures greater than $1\mu\text{m}$ or $2\mu\text{m}$, but a high resolution profilometer (HRP) can make traces down to sub-micron dimensions.

2.4.3 Electrical

Electrical test is a commonly used technique to measure sheet resistance, line resistance, contact chain resistance, capacitance, leakage current, and more. The main advantage of an electrical measurement is that features or conducting lines can be as narrow or as wide as they can be. However, care must be taken to make the ratio of length to width of a line large enough to yield the line resistance such that a probe station can measure it reliably. Furthermore, the limitation of current density must be met so that lines do not suffer from electromigration or joule heating problems. Another advantage is that the electric probe station can be programmed to collect the large amount of data necessary for statistical analysis.

The electrical mask presented in this thesis primarily makes use of line resistance measurement with Kelvin structures, and sheet resistance measurements with Van der Pauw structures. To obtain line resistance, a total of four pads are used as shown in Figure 2.5b for a conventional structure and in Figure 2.5c for the modified version used in this thesis. Two pads are used to force current and two inner pads are used to measure voltage. Then, using a ohmic relation, resistance is obtained by the voltage difference across the two pads divided by the forced current: $R = \Delta V / I$ where R is the line resistance, ΔV is the voltage difference, and I is the current forced. Figure 2.5a shows a typical Van Der Pauw structure and how it is measured. Current is forced from one pad to the next and the remaining two pads are used to measure the voltage difference: $R_s = (\pi / \ln 2) * (\Delta V / I)$ where R_s is sheet resistance, $\pi / \ln 2$ is a correction factor, ΔV is the voltage difference, and I is the current forced.

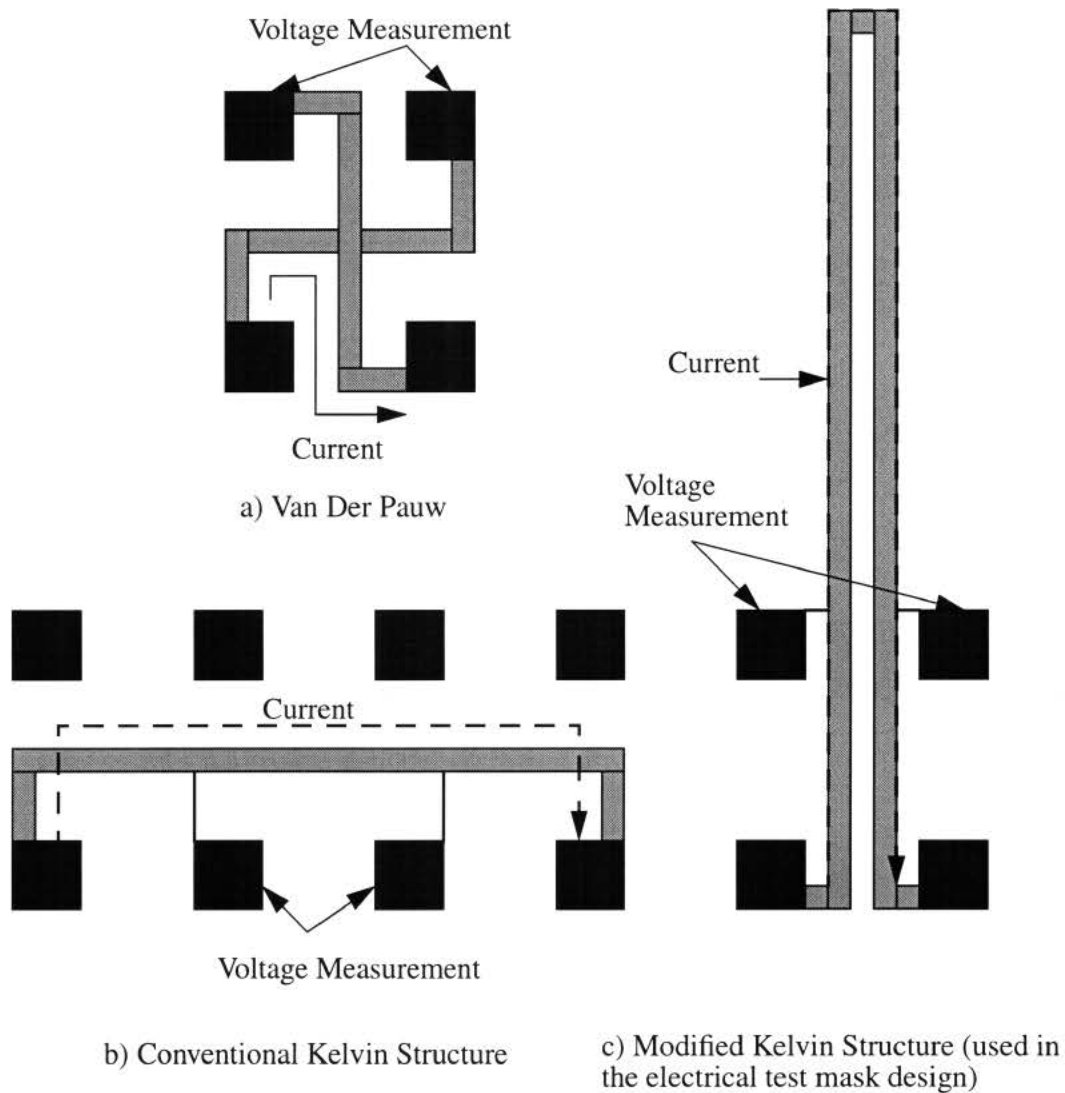


Figure 2.5: Van der Pauw and Kelvin Structures

Serpentine (also known as snake) and comb (also known as bridge) structures are also common electrical test structures as shown in Figure 2.6. Serpentine lines are used to test the continuity of a line by forcing current and measuring the voltage difference. This can be done using only 2 pads since the voltage is measured on the same pad that is used to force current. This method does not give an accurate voltage measurement as is the case

for Kelvin structures. However, an accurate measurement is not necessary for the determination of metal continuity, where we compare the measured voltage to an expected calculated voltage range. For comb structures, voltage rather than current is forced from one pad with the other pad at ground voltage, and the resulting current is measured to test for leakage current and shorts (current reading indicates metal shorts). Again since one is concerned only with whether any current is measured or not, only two pads can be used; current is measured on the same pad that is used to force voltage. If there are no metal shorts, the comb structure can then be used to measure a lateral capacitance (capacitance between lines), and provide information about metal line width and spacing.

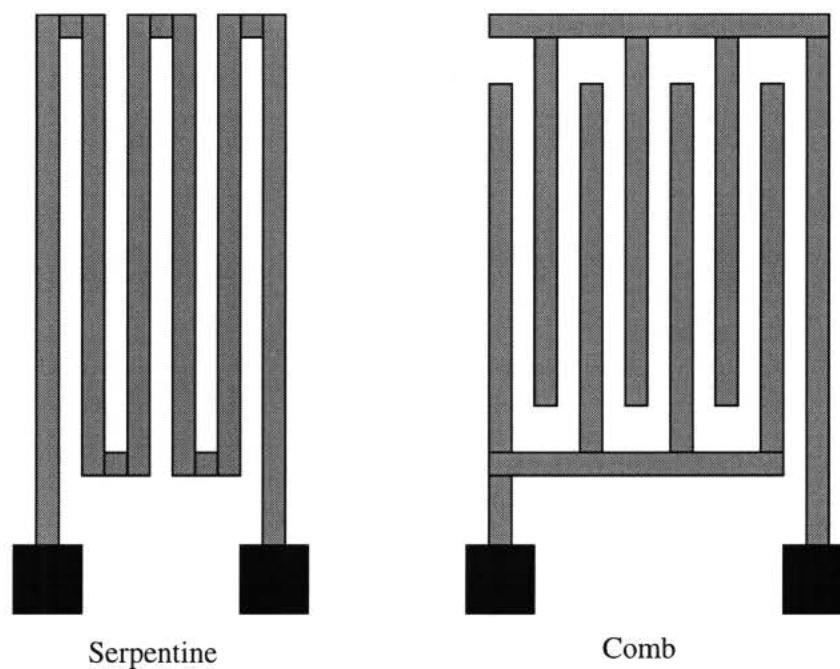


Figure 2.6: Serpentine and Comb Structures

2.4.4 SEM and AFM

Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) are time consuming metrology techniques but are often necessary and sometimes the only technique suitable to obtain high accuracy data or to validate other measurements. Features that are too small to be measured by optical and profilometry measurements can be measured in great detail, and any optical, profilometry, or electrical measurement in question can be validated. AFM works somewhat like a profilometer in a sense that it gives the surface profile but at a higher resolution. SEM, on the other hand, is invaluable for detailed film structure thicknesses and geometric features but requires a sample to be cleaved.

Chapter 3

Electrical Test Mask Description

In the previous chapter, we presented an overview of the copper polish pattern dependency experiments. The previously existing test masks were presented, which emphasize optical or profilometry measurements. In this chapter, we focus on a new test mask that utilizes electrical measurements to characterize copper polishing.

3.1 Introduction

The purpose of the new mask design is to support the study of damascene processes for copper interconnect. The mask is designed to enable methods for rapid characterization, empirical modeling, and comparison of pattern dependencies as a function of process, consumable, or equipment options. The test mask and measurements can also serve as a source of data for the calibration and validation of physical or semi-empirical modeling efforts.

While there are many module and integration issues in copper damascene processes, the mask presented here is specifically designed to characterize and explore issues relating to pattern dependencies, as well as yield/reliability issues, associated with planarization of copper by CMP processes. The characterization mask or variants of the mask presented here can also be utilized to investigate pattern dependencies in a variety of CMP applications, including traditional back-end, trench isolation, and damascene or other inlaid metal processes.

While previous work on oxide CMP back-end processes focused on single-factor mask vectors, the new characterization mask for the copper damascene process combines two main patterns of density and pitch into one mask and focuses on the rapid evaluation of

dishing and erosion phenomena. In addition to density and pitch patterns, the mask also includes electrical serpentine and comb test structures to characterize electrical yield for minimum pitch and fine linewidth metal lines.

The characterization mask utilizes only a single layer; there is no separate mask for bond pads although it is an option. The copper damascene CMP mask uses a single lithography short flow process as described in Section 2.2 with all the test structures and bond pads in one mask. The advantage of a single mask is simplified processing; for example, all patterning can be performed on a conventional fab line, without the need for copper-containing wafers to re-enter the line. On the other hand, the bond pads in the single layer approach have the potential to perturb the local density near test structures, and multilayer CMP pattern effects cannot be studied. The single layer mask does, however, provide the necessary structures for extensive evaluation of dishing and erosion effects that are of primary concern in this thesis.

3.2 Mask Floor Plan

The floor plan of the copper damascene mask is shown in Figure 3.1. The mask is composed of 3mm x 3mm blocks for the density structures, 2.5mm x 3.0mm blocks for the pitch structures, and smaller blocks for serpentine (Sx and SxD), comb (Cx), serpentine/comb combined (SC1), isolated line with bus and dummy environment (IsoLine), control lines (CL), oxide filled pads (Pad Ox Fill), and Van der Pauw (Rs) structures. At the bottom of the mask in the center is a pad layout (BasePad) without any structures which can be used in making initial probe tip contacts to a wafer on an automatic electrical probe station.

In the overall floor planning as well as structure design, the most crucial design factor is estimating the interaction distance for the copper damascene CMP process. Each den-

sity and pitch structure is to be designed with a large enough size so that any interactions from neighboring structures can be excluded. In oxide CMP, the interaction distance is found to be between 3mm and 4mm for most conventional polish processes and pads [26], and industrial feedback and speculation indicated that the interaction distance in copper polish may be considerably less than that of oxide polish. Thus, a structure size of 3mm x 3mm for the density structures is chosen, which should be large enough to allow decoupling of specific density dependency between structures. A slightly smaller block size, 2.5mm x 3mm, for the pitch structures is chosen since all pitch structures have fixed density of 50% and because the dishing within pitch structures is assumed to be minimally influenced by neighboring structures (dishing within features occurs at much shorter length scales than the interaction distance).

In this mask design, pitch is defined as linewidth plus linespace, and density is defined as the ratio of linewidth to pitch. Density, still maintaining the same definition, can also be thought of as the ratio of an area of copper within a given region to the total area of that region.

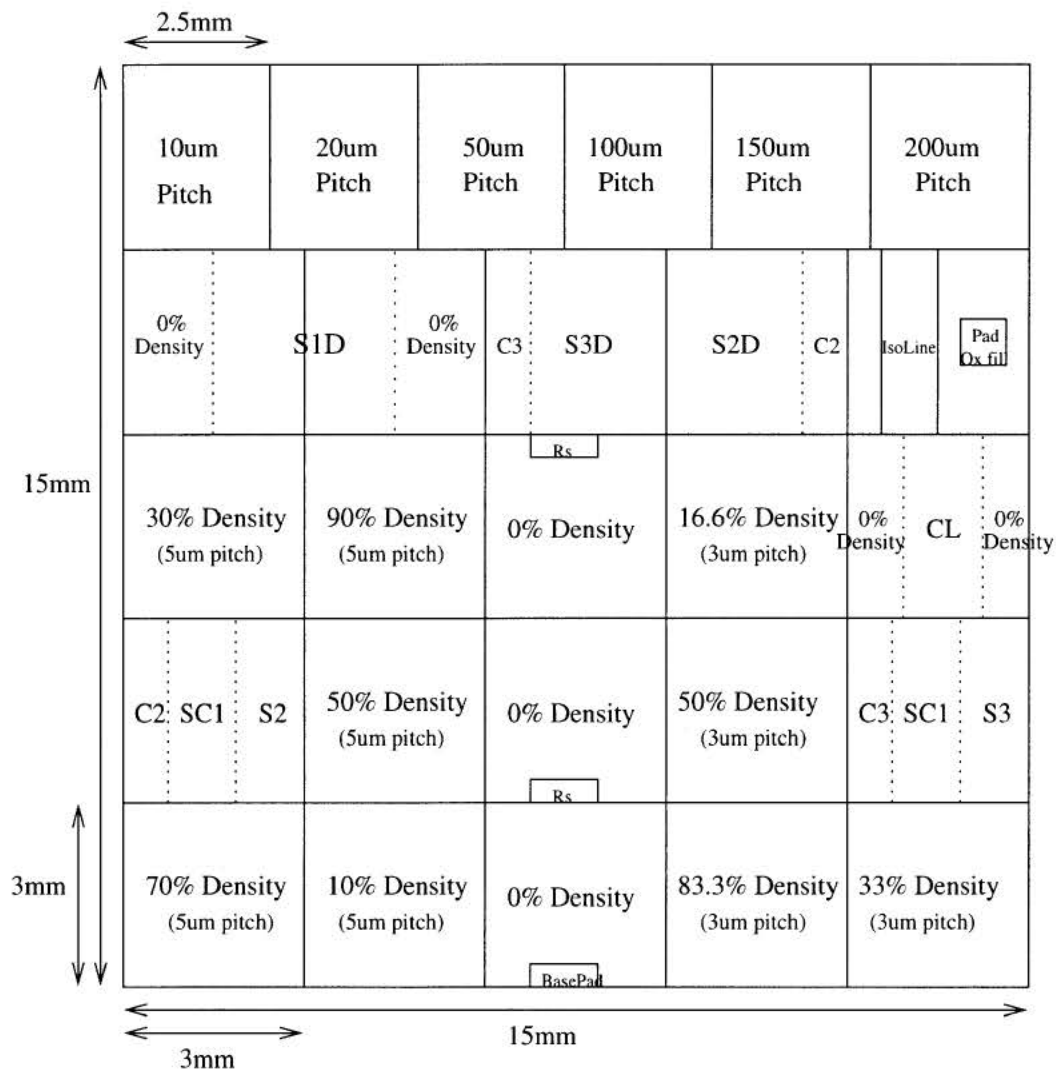


Figure 3.1: Mask Floor Plan

3.3 Description of Each Test Structure

The following sections describe each test structure, and electrical bond pad layout information is given. Interested readers should consult the original mask documentation for this mask design [27] for additional detailed specifications.

3.3.1 Pitch Structure

In the pitch structures, pitch values range from 10 μ m to 200 μ m as shown in the top row of Figure 3.1 with a fixed local density of 50%. The block size for each pitch structure is 2.5mm x 3mm, and each structure consists of 3mm long vertical lines as shown in Figure 3.2. Large pitch values are chosen for easy profilometry and optical measurements (in between copper lines). These structures are used to characterize pitch dependencies: dishing vs. pitch and erosion vs. pitch (if any dependence exists).

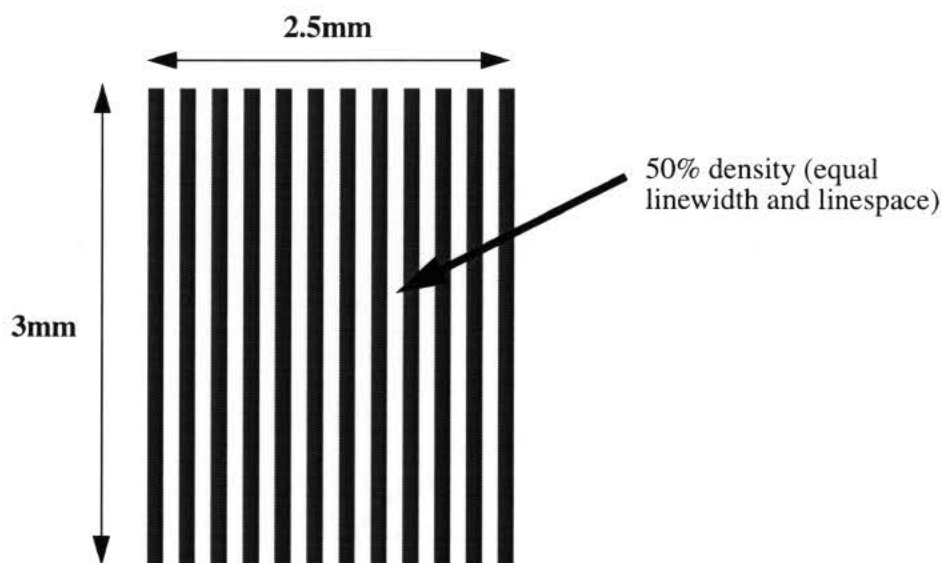


Figure 3.2: One Block of the Pitch Structure

3.3.2 Bond Pad Layout

The bond pad layout is shown in Figure 3.3 with relevant descriptions. Many structures are designed with pad sharing. For example, some of density structures have 2 x 18 probe layout: first 2 x 12 are measured, and then the rest 2 x 6 are measured with pad shar-

ing of 2 x 6 with the first 2 x 12. Refer to the next section on metrology for more information.

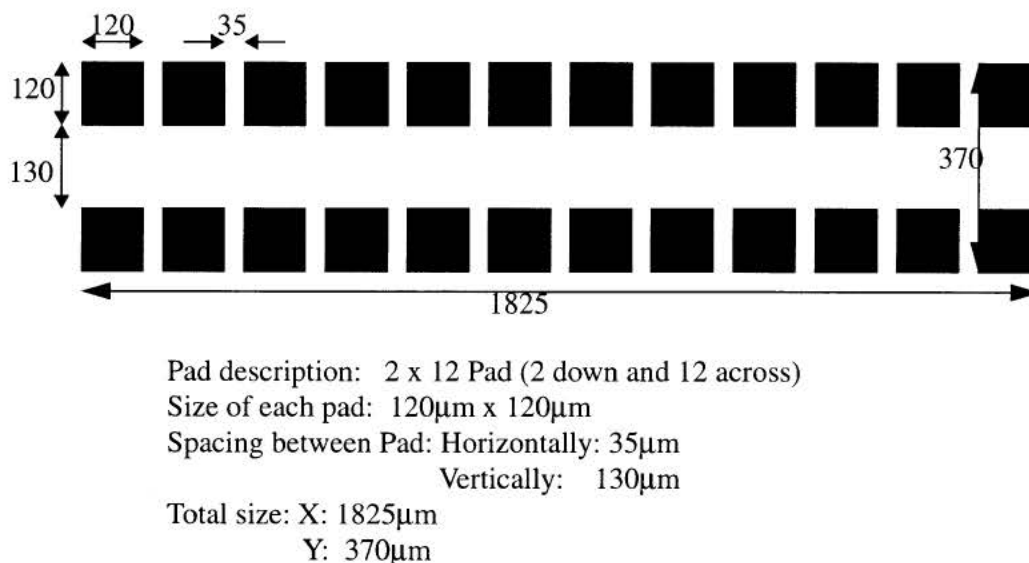


Figure 3.3: Bond Pad Configuration

3.3.3 Density Structure

In the density structures, density is varied for fixed pitch values of 3µm and 5µm. In the floor plan of Figure 3.1, one column of blank (0% density) regions is surrounded by other density structures ranging from 10% to 90% density to determine the interaction range and its possible dependence on density. The density structures are also placed so that there are notable differences in density between adjacent structures. Figure 3.4 shows one 3mm x 3mm density block structure, and Table 3.1 shows the linewidths and linespaces used for 3µm and 5µm pitch value structures. The 50% density structures are also treated

as pitch structures since these structures have the same pattern density of 50% as the pitch structures.

Bond pads are used on top and bottom of each structure to increase the number of measurements that can be made on each structure. Due to the bond pad layout (see the appendix), lines are measured at every $310\mu\text{m}$ using only the bottom pads, but if the top pads are also used, lines are measured at every $155\mu\text{m}$ (twice the sampling rate).

Note that the density structures are implemented with serpentine style lines. Thus, metal lines bend around at the top and bottom so that measurement can be made from either bottom and top pads. Serpentine lines also allows simultaneous resistance measurement for thickness extraction and continuity test of lines in the density structures.

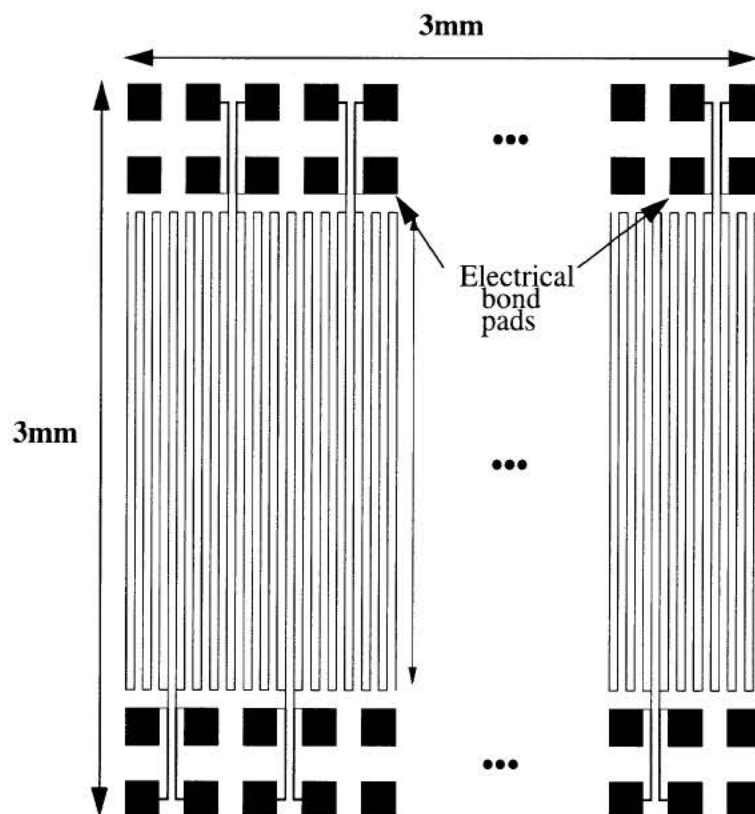


Figure 3.4: One block of the Density Structure and S1D Structure (S2D and S3D structures are designed the same way except the horizontal distance is 2.17mm, rather than 3mm)

Table 3.1: Linewidths and Linespaces in Density Structures (units in μm)

3 μm Pitch (linewidth/ linespace)	5 μm Pitch (linewidth/ linespace)
2.5/0.5 = 83.3%	4.5/0.5 = 90%
1.5/1.5 = 50%	3.5/1.5 = 70%
1.0/2.0 = 33%	2.5/2.5 = 50%
0.5/2.5 = 16.6%	1.5/3.5 = 30%
	0.5/4.5 = 10%

3.3.4 Serpentine and Comb Structures

The “SxD” structures are designed and treated the same way as the density structures for erosion study as well as continuity test. However, the structure size and total pad numbers may be different (shown together with a density structure in Figure 3.4). These S1D, S2D, and S3D structures are designed with specific linewidth and linespace combinations to test continuity of lines, rather than designing with a density factor. Lines up to a total length of nearly 10 meters (in S1D) are examined.

Serpentine (S2 and S3), comb (C2 and C3), and serpentine/comb combined (SC1) structures are used for continuity and shorting tests. In addition, comb and SC1 structures can be used for measuring lateral capacitance which is becoming more significant as the aspect ratio of metal lines becomes larger and larger. Linewidth and linespace used for the serpentine and comb structures are shown in Table 3.2. The serpentine and comb structures are replicated several times on the mask.

Table 3.2: Serpentine and Comb Structures (units in μm)

Serpentine (linewidth/linespace)	Comb (linewidth/ linespace)
SC1 & S1D: 0.35/0.35	SC1: 0.35/0.35
S2 & S2D: 0.7/0.35	C2: 0.35/0.7
S3 & S3D: 0.9/0.35	C3: 0.35/0.9

3.3.5 Control Lines

Control lines (CL) are used to monitor dishing on different pitch values of metal lines with a minimal amount of erosion; under this ideal case (no erosion), the line resistances and extracted thicknesses of corresponding metal lines used in the density structures can be calculated. The linewidths and line spaces shown in Table 3.3 are used. A dummy line environment which is $20\mu\text{m}$ wide on each side is used to reduce linewidth variation by mimicking the environment in the corresponding density structures. As it is with density structures, copper lines bend at the top so that lines start and end next to each other at the bottom where the pads are located.

Table 3.3: Control Lines (in μm)

Linewidth/ Linespace	Dummy Environment
0.35 /0.35	No
0.35 /0.35	Yes
0.5/2.5	No
0.5/2.5	Yes
0.5/4.5	No

Table 3.3: Control Lines (in μm)

Linewidth/ Linespace	Dummy Environment
0.5/4.5	Yes
1.5/1.5	Yes
1.5/3.5	Yes
2.5/0.5	Yes
2.5/2.5	Yes
3.5/1.5	Yes
4.5/0.5	Yes

3.3.6 Isolated line with bus and dummy fills

This structure is used to examine the effect of CMP on an isolated line (IsoLine) beside a wide bus and beside dummy lines, as illustrated in Figure 3.5. To examine the effect of a wide bus on an isolated line, three design factors are considered: bus width (20 μm and 40 μm , with linewidth and linespace of 0.5 μm), isolated line width (0.5 μm and 5 μm), and the space between line and bus (0.5 μm and 5 μm). Full factorial design is used, and a total of eight different combinations of these three factors are implemented. Also two isolated lines (linewidth of 0.5 μm and 5 μm) without the bus lines exist to compare isolated line and a line by a bus.

In the middle of the pads along with a Van der Pauw structure are isolated lines with and without dummy lines. The Van der Pauw structures and kelvin structures share pads. Dummy lines occupy about 10 μm on each side of an isolated line. Table 3.4 summarizes linewidth and linespace combinations used in this structure.

Table 3.4: IsoLine: Single Line with and without Dummy Lines

Single Line Linewidth	Dummy Lines: Linewidth/ Linespace
0.35 μm	0.35/0.35 μm
0.5 μm	0.5/0.5 μm
0.7 μm	0.7/0.7 μm

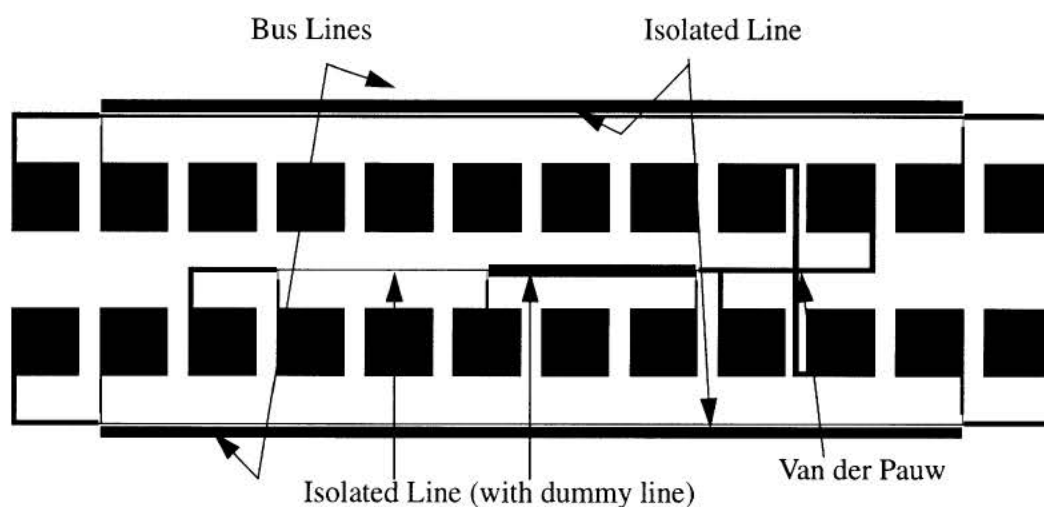


Figure 3.5: One Substructure in IsoLine

3.3.7 Oxide Filled Pads

A small region, denoted as “Pad Ox Fill”, is used to find the dishing effect on oxide filled metal bond pads as compared to conventional pure metal bond pads. Square oxide fills, 0.5 μm x 0.5 μm each, spaced 2 μm apart, are used in 120 μm x 120 μm bond pads as shown in Figure 3.6.

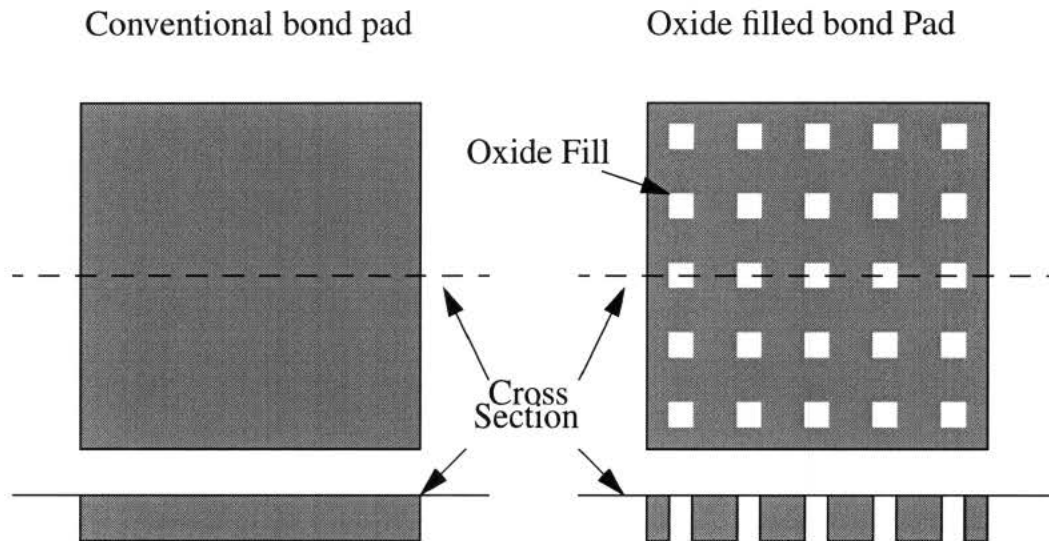


Figure 3.6: Oxide Filled Pad

3.3.8 Van der Pauw

In the 0% density blocks, there are Van der Pauw structures (Rs1 and Rs2) for sheet resistance measurements. Also, there is a comb structure beside the Van der Pauw structure in Rs1 to determine electrically if a wafer is underpolished. If any voltage reading due to forced current is measured in the comb structure, then the wafer should be considered underpolished. That is, metal paths above the oxide field still exist, which shorts the comb structure.

3.4 Metrology and Measurement

The main metrology tools and techniques needed to characterize copper thickness variation using this mask are profilometry, electrical, optical and SEM/AFM measurements. Profilometry is used to generate surface traces and profiles as well as surface maps

over an area of interest, and optical interferometry is used to measure oxide thicknesses. These optical measurements will also be used to correct leveling problems associated with stage tilt, bias, and wafer bow and warp in profilometry scans. Electrical measurements are used to obtain a statistically meaningful large amount of data and for electrical characterizations, especially for fine copper lines that are hard to measure with profilometry or optical measurement. SEM and AFM are used to verify some of profilometry and electrical measurements and to obtain deposition profiles. They are also used to obtain accurate fabricated linewidths and line spaces so that correct values can be used in extracting line thicknesses.

In the following subsections, we describe the recommended metrology for each of the structures described in the previous section.

3.4.1 Pitch Structure

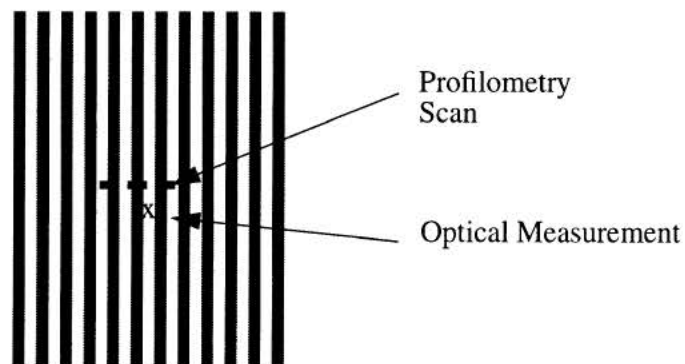


Figure 3.7: Profilometry Scan and Optical Measurement for Pitch Structures

A short profilometry scan across three or four copper lines in the center of each pitch structure is made, as shown in Figure 3.7, to find dishing for each line width. The dishing should be measured by the height difference from the oxide (right next to the copper line)

to the bottom of the dished copper line. This measurement is repeated for all pitch structures and for 50% density structures which also serve as pitch structures. Optical measurement is performed over oxide in the middle of each pitch structure to obtain oxide erosion depth.

The profilometry scan shown in Figure 3.8 serves two purposes: erosion characterization and finding the interaction distance (planarization length) using the density and SxD structures. If necessary optical measurements should also be used to correct any leveling problems. The erosion profile is measured from the initial oxide level to the bottom of the recessed region in each density block. The transition across the blank oxide region to nearby density blocks will be the interaction distance [28]; the scan is made across different density blocks to examine possible dependence of interaction distance on density.

Figure 3.8: Profilometry Scan for Density Structures

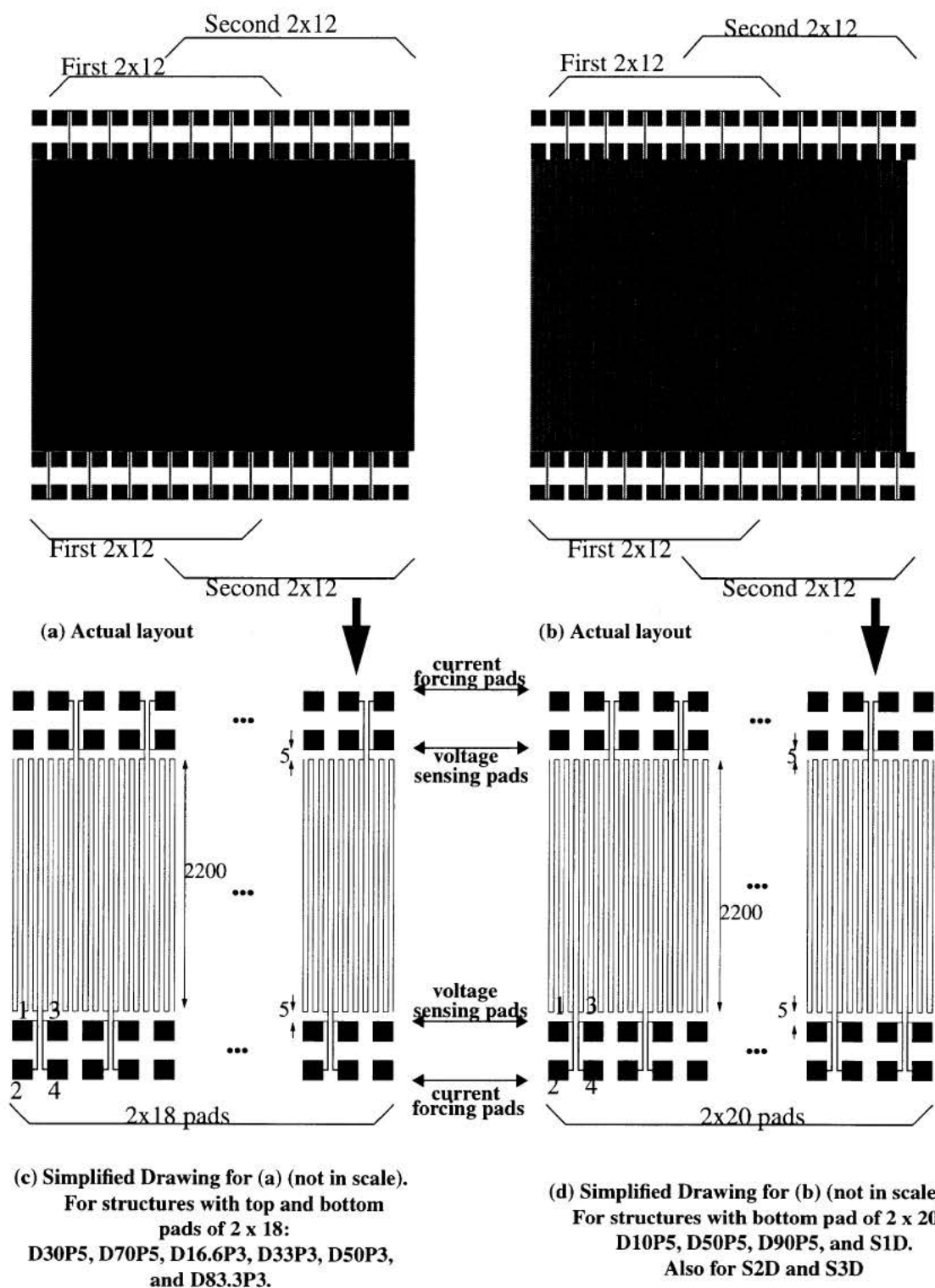


Figure 3.9: Electrical Test for Density Structures.

Figure 3.9 shows how electrical test is done with density and S1D structures. First, the bottom bond pads (below the structure) are used to measure line resistances, and then the top bond pads (above the structure) are used. These structures are designed with pad sharing. The first 2 x 12 are measured and then second 2 x 12 are measured with some of the pads shared with the first 2 x 12. When measuring the second 2 x 12, only the unmeasured portion of pads (2 x 6 or 2 x 8 for total of 2 x 18 or 2 x 20 pads, respectively) is measured. For each measurement of a specific line, four pads are used, two of which are current forcing pads and two of which are voltage sensing pads. For example, pad 2 and pad 4 are used as current forcing pads and pad 1 and pad 3 are used to measure the voltage across the copper line. This measurement is repeated for each line at both the top and bottom pads for all density structures. This same technique is used for S2D and S3D structures which have 2 x 12 for the top pad and 2 x 14 for the bottom pad. In each case, voltages induced due to forced current are measured and recorded, and this information is used to calculate each line resistance.

3.4.3 Serpentine and Comb

Structures C2_1, SC1_1, and S2 consist of total pad size of 2 x 19, and structures C3_2, SC1_2, and S3 also consist of total pad size of 2 x 19. The first 2 x 5 pads are used with comb (C2 and C3), the second 2 x 7 are used with SC1, and the remaining 2 x 7 pads are used with serpentine structures (S2 and S3). For comb structures (C2 and C3), pads 1, 3, 5, 7, and 9 are each tested for shorting of lines with pad 10 which serves as a “ground” comb. For SC1, each serpentine pads (pads 13, 17, and 21) are tested for shorting of lines with each comb pads, (pads 11, 15, 19, and 23), as well as with pad 24 (“ground” comb). If the structure yields (no shorting), then the continuity test is performed on pad 13 and pad 21. For shorting tests, the even numbered pads (except pad 10 and pad 24) could be used as current forcing pads, but since precise measurement is not necessary, only odd

numbered pads can be used. For the S2 and S3 serpentine structures, pad A and pad B are used to test the continuity of the long serpentine line connected between these two pads.

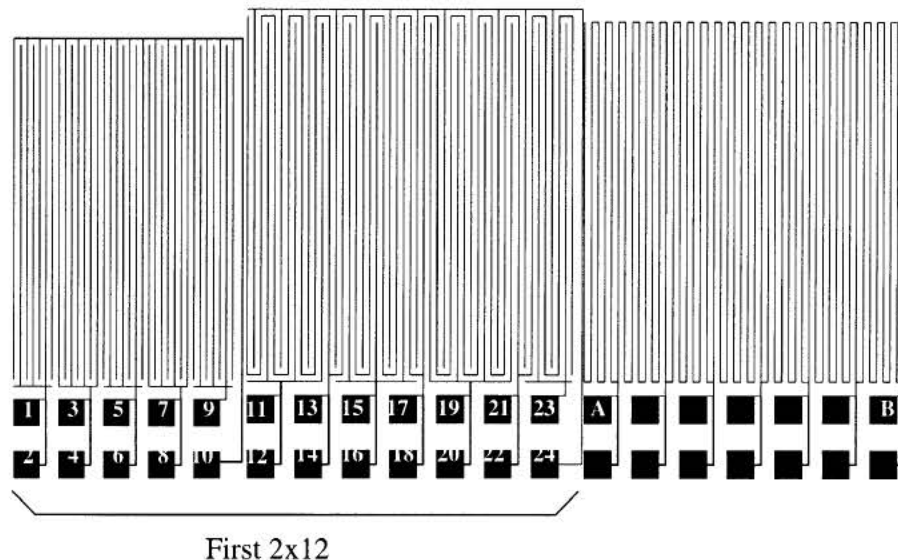


Figure 3.10: C2, SC1, S2, and C3, SC1, S3 structure (not in scale: vertical distance is larger than shown).

3.4.4 Control Lines

The same technique used for density structures can be used for CL structures, shown in Figure 3.11. This structure is easier to measure since both top and bottom pads are 2 x 12 and there is no pad sharing.

3.4.5 Isolated Line

All substructures A, B, C, and D are tested the same way for the isolated lines with bus above and below each 2 x 12 pad. As shown for substructure A in Figure 3.12, pad 2 and pad 24 are current forcing pads, and pad 4 and pad 22 are corresponding voltage sensing

The diagram illustrates a 2D array layout with the following components and labels:

- Linewidth/Space:** Indicated by an arrow pointing to the top of the array.
- forcing pads:** Located at the top right, with an arrow pointing left.
- voltage sensing pads:** Located in the middle right, with an arrow pointing left.
- voltage sensing pads:** Located in the bottom right, with an arrow pointing left.
- current forcing pads:** Located at the bottom right, with an arrow pointing left.
- Dummy Lines:** Indicated by an arrow pointing to the bottom of the array.
- B:** Indicated by an arrow pointing to the bottom of the array.
- Labels for columns:** 1, 2, 3, 4, ..., 10, 11, 12.
- Labels for rows:** 1, 2, 3, 4, ..., 5, ..., 2200, ..., 5, ..., 11, 12.
- Dimensions:** 0.35/0.35, 0.5/2.5, 4.5/0.5, 0.35/0.35, 0.5/0.25, 3.5/1.5.
- Other labels:** T, 2200, 5, ..., 11, 12.

54

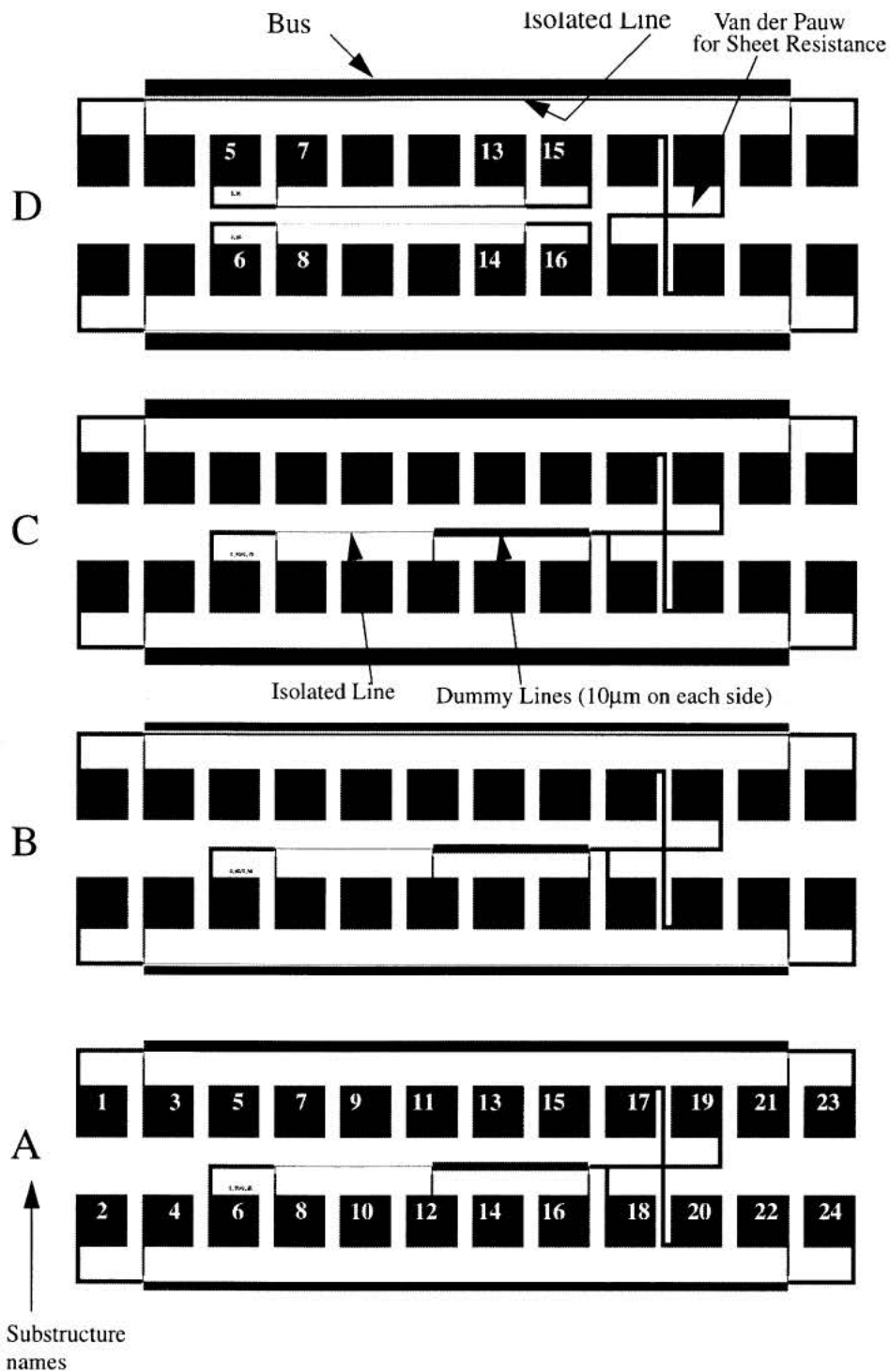


Figure 3.12: Isolated Line with Bus and with & without Dummy Lines. Pad numbers are shown in the middle of each pad. (Actual layout shown: many lines appear solid due to the resolution of printing.)

3.4.6 Oxide Filled Pad

Profilometry scans are made across the middle of each conventional and oxide filled bond pads as shown in Figure 3.13. Dishing should be measured from the top of surrounding oxide to the bottom of dished pads. Oxide thickness measurements are also recommended to account for any oxide erosion (shown as “x” in Figure 3.13).

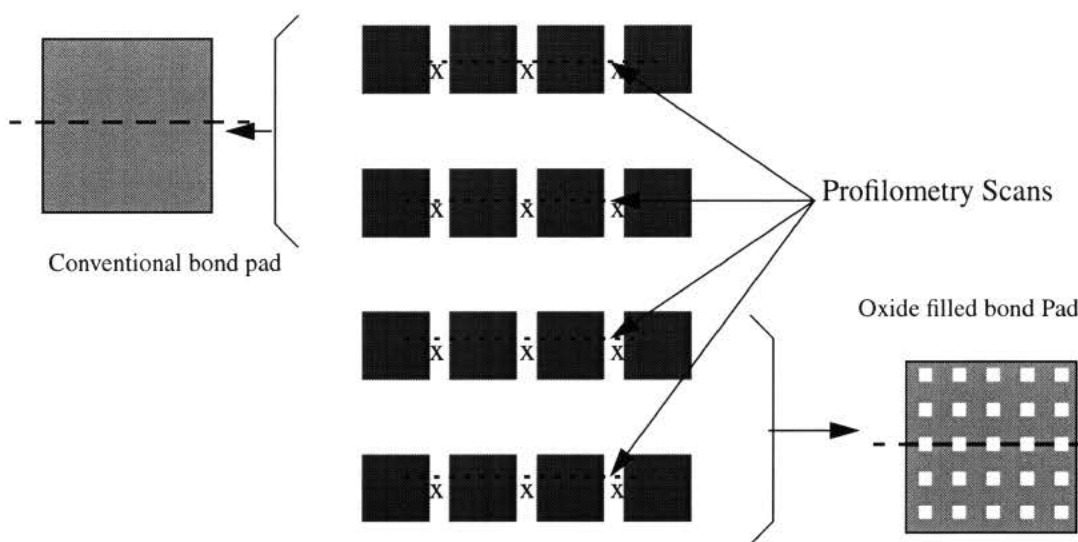


Figure 3.13: Oxide Filled Pad

3.4.7 Van der Pauw

As shown in Figure 3.14, pads 1, 2, 3, 4, and pads 21, 22, 23, 24 are used for sheet resistance measurement of Van der Pauw structures at each end of 2 x12 pad. The comb structure in the middle is used as a sanity check for underpolish of copper on top of oxide. Pad 12 and pad 14 are current forcing pads, and pad 11 and pad 13 are used sensing pads. However, pads 11 and 13 alone could be used to do the shorting test since precise measurement is not required.

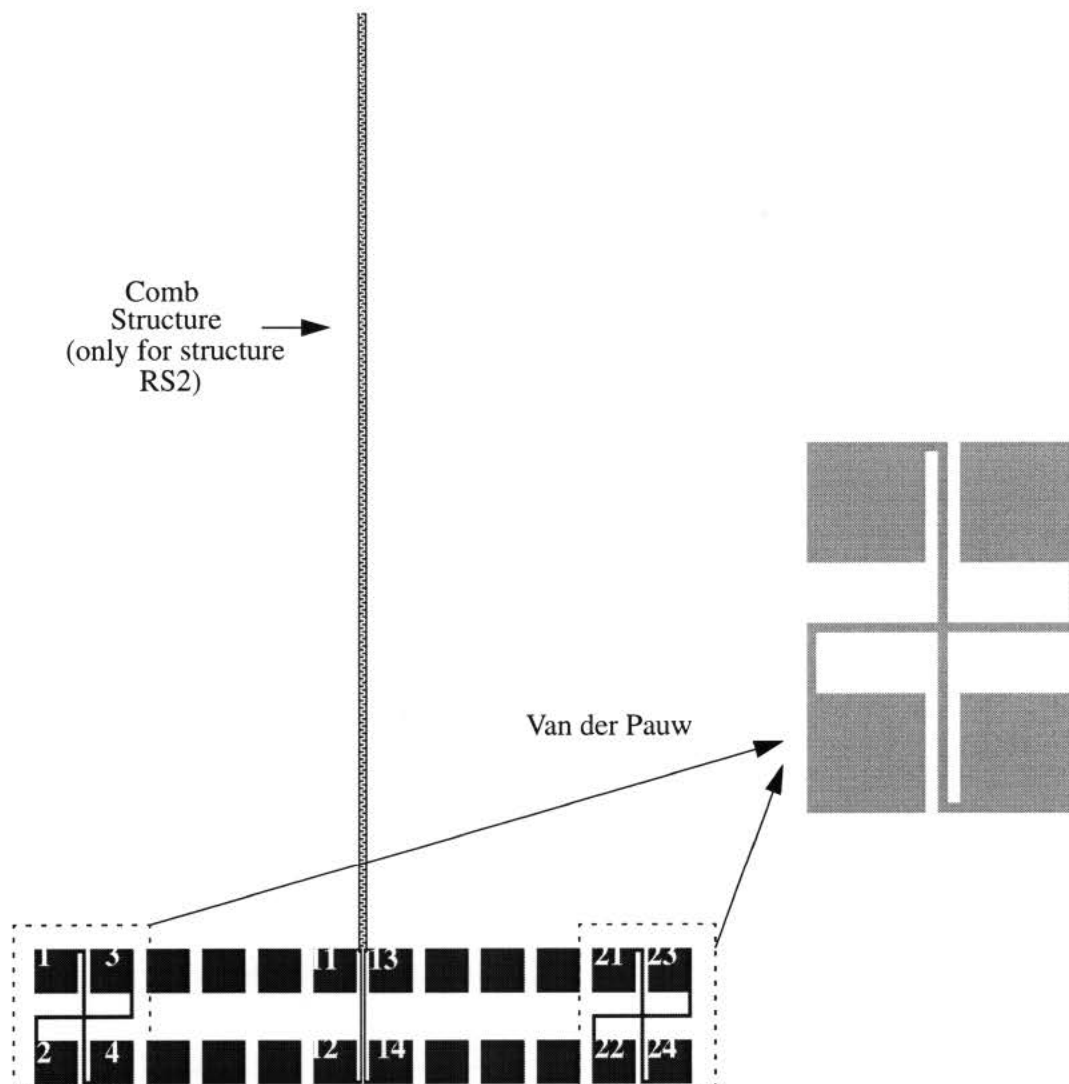


Figure 3.14: Van der Pauw with Comb

3.5 Copper Thickness Extraction Method

After the electrical measurements are made, the measured voltage (or current) and forced current (or voltage) are used to obtain each line resistance as described in the ear-

lier section. After line resistances are obtained, they are converted to copper thicknesses for an analysis. The copper thickness extraction method is based on the following equation:

$$R = R_s \times \frac{L}{W} \quad (3.5)$$

or by re-arranging variables

$$t = \frac{\rho}{R} \times \frac{L}{W} \quad (3.6)$$

where R is resistance, R_s (ρ/t) is sheet resistance, t is the thickness of a line, ρ is the resistivity of copper, L is the length of a line, and W is the width of a line.

In this equation, ρ and L are assumed to be constant, but W suffers from linewidth variations during lithography and etch processes. This linewidth variation must be accounted for to obtain the correct copper thickness from the line resistance measurement. In the conventional aluminum metallization practice, line width variation can be easily obtained by the following equation:

$$W = \frac{R}{R_s} \times L \quad (3.7)$$

This relation assumes that the aluminum thickness is the same for a metal line (measured for resistance) and for a nearby Van der Pauw structure (for sheet resistance measurement). However, this assumption is no longer valid in the copper damascene process where the thickness of a metal line changes depending on pattern and process variables. Thus, this simple method can no longer be used; other direct physical measurements are necessary. For wide linewidths (above $2\mu\text{m}$), a conventional profilometry scan can be used to obtain the exact W ; however, AFM or SEM is required for narrower linewidths.

Ideally, the linewidth estimation measurements should be made at different locations within a structure (e.g. density structure) to account for within structure variation. How-

ever, not all copper lines need to be measured to obtain exact linewidth variation. It is expected that all the regularly laid out vertical lines except those within $20\mu\text{m}$ of the edge of the structure will have the same amount of linewidth variation. For any line resistances measured near the edge, the corresponding lines should be measured to get the exact W , but due to the limitation of the bond pad layout, only one or sometimes zero lines lie in the $20\mu\text{m}$ edge region. Thus, a maximum of one linewidth measurement for edge lines and only three or four linewidth measurements are necessary for lines in the edge excluded region. This method is used for all density, S1D, S2D, and S3D structures. For the control line structure, all control lines should be measured to account for linewidth variation.

To be more accurate in the copper thickness extraction method, the impact of barrier liner should be accounted for. Equation 3.6 assumes the ideal case where the effect of liner is assumed negligible. However, as the critical dimension decreases to the sub-micron regime, the thickness of liner consumes a higher percentage of the total thickness of metal as well as width of the line. For the purpose of this study, we assume a constant liner thickness and a simplified dishing characteristic (i.e. a flat surface in the dished copper line and no edge rounding) as shown in Figure 3.15.

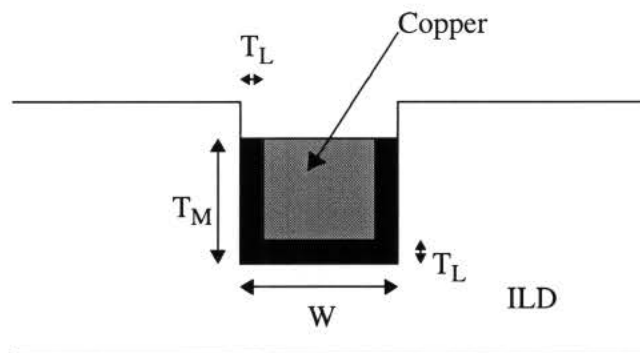


Figure 3.15: Idealized dishing of a copper line and liner.

First, we examine R_{Cu} and R_L (resistance due to copper and resistance due to liner). R_{Cu} and R_L can be represented as

$$R_{Cu} = \frac{\rho_{Cu} \times L}{(T_M - T_L) \times (W - 2T_L)} \quad (3.8)$$

$$R_L = \frac{\rho_L \times L}{(2T_M \times T_L) + ((W - 2T_L) \times T_L)} \quad (3.9)$$

where ρ_{Cu} is the resistivity of copper, ρ_L is the resistivity of liner, L is the length of a metal line, T_M is the remaining metal thickness, T_L is the thickness of liner, and W is the width of a metal line. The denominator terms in both equations give the cross sectional area. The resistivity of commonly used barrier liners are in the range of 50 to 100 $\mu\Omega\text{-cm}$ [2]. We assume the worse case scenario where ρ_L is 100 $\mu\Omega\text{-cm}$ and W is 0.35 μm (minimum line-width in the mask design). We also assume that T_M is about 4000 Å (half of the ideal trench height in this experiment) and T_L is 250 Å. By using these numbers in the equations above, the ratio of R_L to R_{Cu} is calculated to be about 200. This indicates that the copper and liner stack can be approximated just as a copper line with less than 0.5% error. Thus, Equation 3.6 can be rewritten to account for the liner effect as (i.e. by using R_{Cu} rather than $R_L \parallel R_{Cu}$)

$$t = \frac{\rho_{Cu}}{R} \times \frac{L}{(W - 2T_L)} + T_L \quad (3.10)$$

where R is the measured resistance; W is adjusted to exclude the thickness of liner, and T_L is added to get the total thickness of copper plus the liner. Note that while the liner resistance doesn't matter too much, the loss of liner thickness in the Cu line cross-section does matter quite a bit for the narrow lines (maybe for all lines, since it diminishes the thickness too).

Chapter 4

Experiment with Characterization Mask Set

This chapter presents experimental data that shows the dependence of Cu dishing and oxide erosion on pitch, pattern density, as well as on polishing process parameters including table speed, down force, and process sequence. Specifically, the data shows that the trends of dishing and erosion on density or pitch are similar for different polishing conditions, but the degree of dishing and erosion strongly depends on the processing parameters. Second, we find that a multiple step polish is able to achieve better polishing results compared to a single step polish process.

Using CMP to ensure that there is no Cu in the region between the trenches, and hence no shorting of any two Cu lines requires an overpolish step. Overpolishing leads to dishing of Cu and erosion of oxide. Dishing and erosion lead to an increase in the resistance of the Cu lines. There is therefore a pressing need to understand their dependence on pattern density (Cu line width divided by pitch) and pitch (Cu line width plus oxide space), as well as on polishing process parameters such as table speed, down force, etc., all in an effort to develop an optimized Cu damascene process.

4.1 Design of Experiment

4.1.1 Short Process Flow

The following process steps were carried out before CMP:

- Deposit 0.8 μm of TEOS on 8 inch silicon wafers.
- Pattern and etch 0.8 μm trenches in the deposited oxide.
- Deposit 0.025 μm of a common polish barrier.
- Deposit 1.5 μm of Cu on the entire wafer.

4.1.2 CMP Process Splits

Two sets of CMP experiments were then carried out. In the first experiment, CMP process conditions are varied to study the impact on dishing and erosion performance. These splits are all performed with the same consumable set (set “S1”), with process conditions summarized in Table 4.1. The back pressure is set at 1.0 psi. The goal in this experiment is to set the down force to a constant but different value for each of the three process splits, but to adjust the table speed and carrier speed such that the bulk removal rate of Cu will be the same for all three process splits. The polishing time is held approximately constant for all three process splits and is chosen to ensure complete removal of both the Cu and the polish barrier on top of the oxide.

In the second experiment, a single step polish (i.e. the slurry and process conditions are held constant throughout the polish) is compared to a three step polish, both with consumable slurry and pad set “S2” and a constant back pressure of 2.85 psi. In the third sub-step, a novel process modification was made to decrease the amount of chemical reaction and increase the mechanical component in the polishing. The polishing values are chosen such that the overpolishing time is the same for both the single step and the three step polishing processes, and the polishing time is long enough to ensure complete removal of the Cu and the polish barrier on top of the oxide, as in the first experiment. The process conditions are summarized in Table 4.2.

Table 4.1: Polishing Experiment #1

Process	Down force (psi)	Platen speed (rpm)	Carrier speed (rpm)
A	2.0	70	40
B	3.5	60	60
C	5.0	35	35

Table 4.2: Polishing Experiment #2 (Down force 1 is for step 1, etc.)

Process	Down force 1 (psi)	Down force 2 (psi)	Down force 3 (psi)	Orbital speed (rpm)
M	5	2	2	320
S	3	-	-	285

4.2 Mask Sets

The pitch and density masks from the MIT CMP characterization mask set are used in this study and are shown in Figure 2.3 and Figure 2.4 respectively in Chapter 2. As previously described, the pitch mask contains vertical lines with pitch in the range 2 μm - 1000 μm , at a constant pattern density of 50%. The density mask contains pattern densities in the range 4% to 100%, at a fixed pitch of 250 μm . Both masks have an outer dimension of 12 mm by 12 mm, and were designed for physical as opposed to electrical measurements. They have previously been used to study oxide CMP pattern dependencies.

4.3 Metrology

Copper dishing is measured with the use of a Tencor profilometer (P10), and the results are verified with AFM measurements. Oxide erosion, on the other hand, is measured using a Tencor UV1250 optical tool. SEM measurements are done to verify the line width of the Cu lines, the width of the oxide spaces, and the oxide thickness measurements done with the UV1250.

In order to average out the variation that occurs within the wafer, 9 dies are measured on a wafer, and the average of the dishing and erosion measurements for these dies is reported as the measured dishing and erosion for the entire wafer.

4.4 Experimental Results and Discussion

Figure 4.2 through Figure 4.5 show the results of the polishing experiments. Figure 4.1 is a sample profilometer scan done for a 400 μm pitch structure (50% pattern density). Figure 4.2 shows graphs of dishing versus pitch for a constant pattern density of 50%. It is seen from Figure 4.2a and Figure 4.2b that dishing increases with pitch for a constant density, as expected [10, 11, 29].

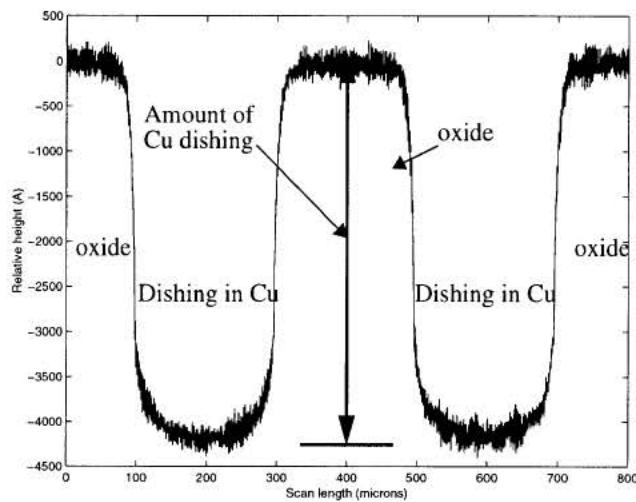


Figure 4.1: Profilometry scan of a 400 mm pitch structure (50% pattern density)

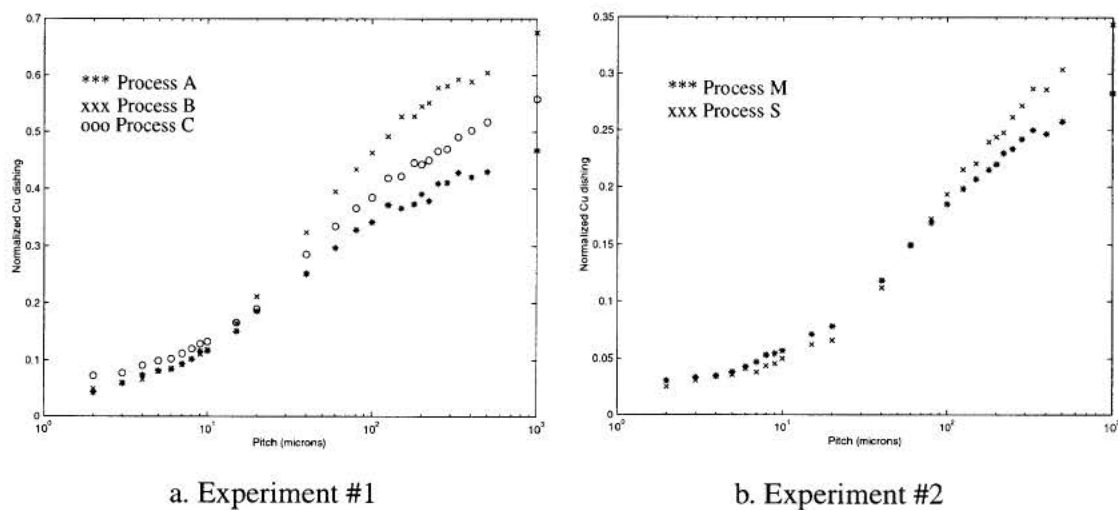


Figure 4.2: Cu Dishing vs. Pitch (50% pattern density)

Figure 4.3 shows graphs of erosion versus pitch for 50% pattern density. The figures show that at low pitch values, there is a considerable dependence of erosion on pitch. This is in agreement with the results presented by Fayolle et al., [29] but contradicts the results of Steigerwald et al., [10].

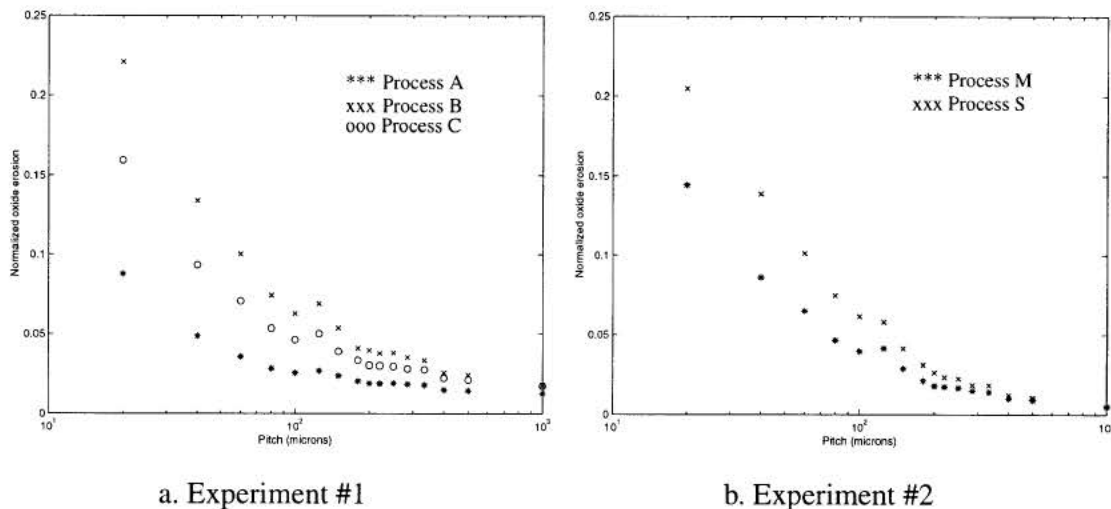
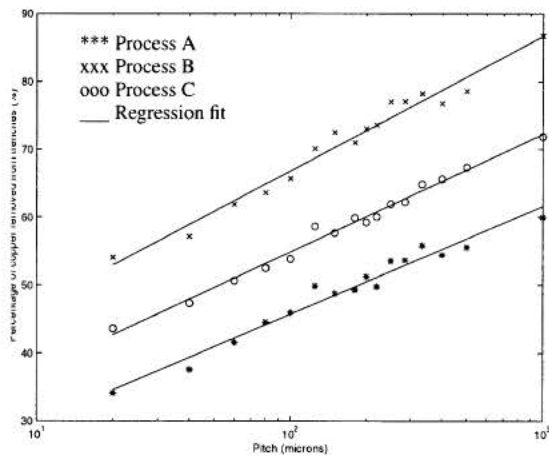
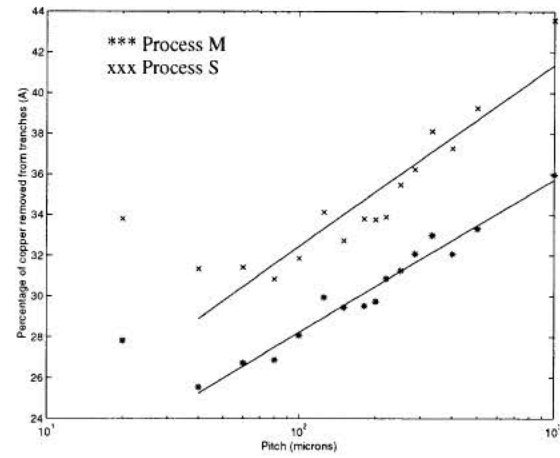


Figure 4.3: Oxide Erosion vs. Pitch (50% pattern density)

By adding Cu dishing to oxide erosion, the total amount of copper loss in the trenches is obtained. Figure 4.4 shows the percentage of Cu removed from the trenches plotted as a function of pitch, for 50% pattern density (that is, when line width and space are each equal to half the pitch). The figures show that the percentage of Cu removed from the trenches (and hence the percentage increase in Cu resistance caused by dishing and erosion) varies linearly with the logarithm of the pitch, for large pitch structures and a pattern density of 50%.

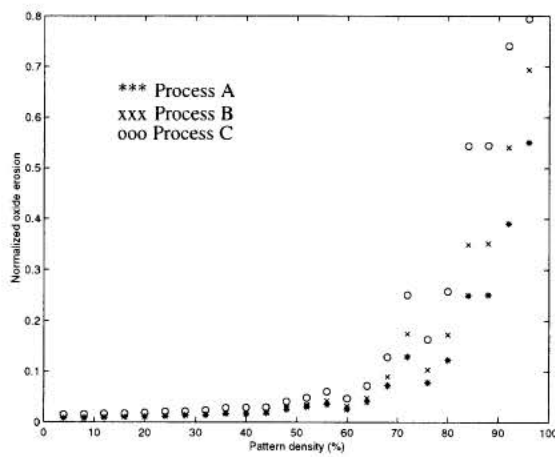


a. Experiment #1

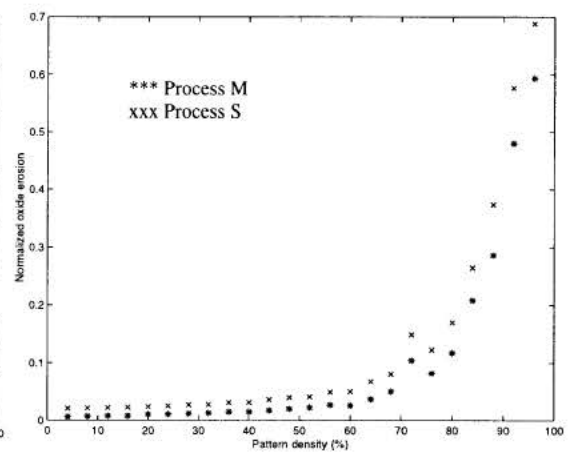


b. Experiment #2

Figure 4.4: Percentage of Cu removed from trenches vs. Pitch (50% pattern density)



a. Experiment #1



b. Experiment #2

Figure 4.5: Oxide erosion vs. pattern density (pitch is 250 μm)

Steigerwald et al., [10] and Fayolle et al., [29] have presented results that show that oxide erosion increases with pattern density. Figure 4.5 indicates oxide erosion plotted against pattern density, for a fixed pitch of 250 μm , confirming their findings. Examining both figures closely, it is found that the amount of oxide erosion only becomes significant at higher pattern densities with a break point occurring at approximately 60% pattern density.

From Figure 4.2 to Figure 4.5, the trends in dishing or erosion on pitch or pattern density are similar across all polishing conditions. However, the amount of dishing and erosion depends strongly on the polish settings as manifested by the shift in the curves in Figure 4.2 through Figure 4.5 when these parameters change values. This is in contradiction to the findings of Stavreva et al., [30].

4.5 Conclusions

The trends of Cu dishing or oxide erosion with respect to pitch or pattern density is similar for a range of polishing parameters and conditions. The degree of Cu dishing and oxide erosion depends on both the patterns (pitch and pattern density) and the polishing process parameters (down force, table speed, etc.). Furthermore, the percentage increase in Cu resistance caused by dishing and erosion varies approximately linearly with the logarithm of pitch for a 50% pattern density structure for large pitch structures. Finally, a multistep polishing process offers some improvement over a single step process in dishing and erosion performance.

Chapter 5

Conclusion and Future Work

5.1 Summary

This thesis has described a statistical metrology framework for characterization of pattern dependencies of copper interconnect thickness variation. Specifically, it has focused on the pattern dependencies of dishing and erosion in CMP planarization for a damascene process. This framework is primarily divided into methodology and experiment. First, the methodology covers layout factor identification and selection, test structure and mask design, and characterization method. Second, the experiment covers implementation of this methodology through the copper metallization development project by SEMATECH. This thesis has also examined the copper metallization process including the importance of the transition from Al to Cu, the overall fabrication process using the damascene technique, and problems associated with copper metallization especially due to CMP. Furthermore, this thesis has contributed a new single-level electrical mask for the study of Cu polish pattern dependencies. While experimental data using the mask is not yet available, the principles of the mask have been detailed, as well as guidelines provided for measurements using the mask.

This thesis has also presented the physical characterization (with optical and profilometry measurements) of dishing and erosion for different polishing parameters and conditions for wafers fabricated with the pitch and density masks from the previously existing CMP characterization mask set. The experimental results show that the trends of Cu dishing or oxide erosion with respect to pitch or density are similar for a range of polishing parameters and conditions, but the degree of Cu dishing and erosion depends on both the patterns and the polishing process parameters. It is also observed that the percentage of

copper removed from trenches, thus the percentage increase in Cu resistance, caused by dishing and erosion varies approximately linearly with the logarithm of pitch for a 50% pattern density for large pitch structures. Finally, although quantitative values could not be found from the experiment described in Chapter 4, the interaction distance for copper polishing is found to be roughly an order of magnitude less than that for oxide polishing. By measuring the transition between a large oxide region and a density region for wafers fabricated with an earlier SEMATECH mask, the interaction distance was found to be between 50 μ m and 500 μ m. This concept of interaction distance needs further study for copper polishing and should be possible once data is available from the new electrical test mask.

It is clearly seen from the experiments of Chapter 4 that dishing and erosion have greater than linear dependence on density or pitch. An inverse relationship as well as second order relationship exists whereas in oxide polishing only a linear dependence is observed between ILD thickness and density after reaching local planarity. This observation can be utilized as a starting point for modeling of the pattern dependencies as a function of pitch and density to better understand CMP planarization in a copper damascene process.

5.2 Oversights and Improvements for the E-Test Mask

Some oversights as well as improvements for structure designs of the electrical test mask and mask floor planning are discussed in this section. Many of the structures are designed with very little available information in copper and metal polishing. Thus, test structure design and mask floor plan had to partially rely on educated guesses and the understanding of oxide polishing characteristics. The following observation on the present

design should help guide the future design of test structures as well as mask floor planning.

First, the pitch structures do not cover important pitch values under $3\mu\text{m}$ with 50% pattern density. There is a discontinuity in the design from the pitch of $3\mu\text{m}$ to $0.7\mu\text{m}$. Addition of pitch values of $1\mu\text{m}$ and $2\mu\text{m}$ would better cover the design spectrum in this important region of design space. Furthermore, the pitch structures have all fixed density of 50%. It would be also beneficial to study these structures at different density environment (including an isolated line or near 0% density) since some data suggest a slight dependence of dishing on density with a fixed pitch value.

Another oversight of the pitch structure design is that it is hard to identify the border between two neighboring pitch structures (if there is not a large difference in the pitch values) because vertical lines all look similar under a profilometer. Putting a blank oxide region between each pitch structure will resolve this problem; since pitch structures are relatively large compared to the interaction distance found in copper polishing, a small blank oxide region would not disturb the design. These pitch structures could also be made to be probed electrically for fast data acquisition and e-test characterization. Finally, a number of larger pitch lines would be useful for constructing damascene CMP models.

Second, the density structures can be improved. The current design has a separate control line (CL) structure to monitor dishing on different pitch values (ones used in density structures) with a minimal amount of erosion. This implementation can be improved by designing one density block to contain all of the following three: an isolated line, an isolated line with dummy environment, and a density region. This type of design is feasible because the interaction distance has been found to be very short in copper polishing compared to oxide polishing. This improved design will facilitate and ease the e-test measurements and yield more information. This short interaction distance also allows the large 0%

oxide region to be reduced significantly or even eliminated in favor of more valuable structures. The shorter interaction distance indicates that interesting polish behavior occurs in a shorter range, and this can be best observed in the abrupt transition from an oxide region to a density region. To carefully study this region, a new structure similar to a density structure, but that takes many more line resistance measurements in the transition region, needs to be designed.

Finally, the pad design and usage can be improved. Because the interaction distance was not known at the time of design, the number of pads are fitted to a design space (e.g. 3mm x 3mm density structure), and this created structures containing different number of total pads such as 2 x 19 and 2 x 20 that exceed the basic pad layout of 2 x 12. Though this differences can be accommodated with an e-test program, a fixed pad layout such as 2 x 20 will be more user friendly.

5.3 Future Work

In developing a copper metallization process, there are still a number of issues that need to be explored. The experiment presented in this thesis examined the effect of down force with varying table speed to keep the removal rate constant. More extensive process experiments are necessary to fully understand the process effects on polishing. This DOE should include variation of individual process parameters, as well as consumable and machine comparison. With this study, wafer-level variation should also be examined.

So far, the work has focused on copper thickness variation due to dishing and erosion. Certainly this thickness variation affects the resistance of copper lines, but as the linewidth goes into the deep submicron regime, linewidth (or critical dimension, CD) variation will become more critical as well. CD variation, which is caused by photolithography and etch,

will need more systematic study to de-convolve CD variation and thickness variation, particularly in electrical measurements.

In addition to characterizing these pattern dependent problems, a study should be done to reduce the amount of variation. One such technique involves the use of oxide fills in copper lines. By introducing oxide pillars to support a polishing pad, a cross sectional conductance is lost, but the reduction of dishing will compensate and perhaps even increase the effective conductance of a copper line. Some of the variables in this study are oxide fill size and shape, distance between each fill, and fill patterns.

With copper metallization, the industry is also examining materials with low dielectric constants (k) as compared to conventional SiO_2 . The integration of low- k dielectrics with copper will enable still higher performance chips. Future experiments need to consider the use of low- k material; for example, the capacitance between comb lines may also provide information about the dielectric constant of low- k materials used in advanced interconnect.

Finally, multi-layer effects need to be examined. The masks presented in this thesis are all single layer masks to be used in a single layer process. To fully understand and develop copper metallization processes, multi-layer effects such as propagation of pattern dependencies from metal 1 to metal 2, via chains on different metal 1 topography and their yield, and polishing dependencies of metal 2 on metal 1 need attention. From the findings of the experiment presented in this thesis and e-test data to be collected on the e-test wafers, a new three-level mask (metal 1, via, and metal 2) design will enable and facilitate the full development of multi-layer copper interconnect and will help resolve associated process and integration issues.

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