

**DECLARATION OF MARTIN CROSS REGARDING TRANSLATION OF
REFERENCES FROM JAPANESE TO ENGLISH**

I, Martin Cross, declare, certify, and state as follows:

1. I possess advanced knowledge of the Japanese and English languages. My qualifications are as follows:

- More than 25 years as a technical Japanese translator
- 1986, York University, B.A. in English Literature
- 2008 to Present, Patent Translator, KLS, Inc.
- Co-author of the Japanese Patent Translator's Handbook, published by American Translators Association;
- United States district court recognition as an expert in Japanese technical translation for patent litigation; and
- Work experience including design and testing of electronic circuits for Research and Development Laboratories Waterloo Ltd.

2. I reviewed the original document entitled Japanese Unexamined Patent Application Bulletin No. JP-04-262535-A ("Tonishi") and translated it faithfully from Japanese to English.

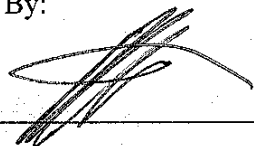
3. The translation is, to the best of my knowledge and belief, a true and accurate translation from Japanese to English of Tonishi.

4. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001).

5. I declare under penalty of perjury that all statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

Executed on April 18, 2018, in Vancouver, Canada

By:



Martin Cross

CERTIFICATION

Items translated: Japanese Unexamined Patent Application Bulletin
No. JP-04-262535-A

This is to certify that the above-stated items were translated by Martin Cross from
Japanese into English, and that they represent accurate and faithful renditions of the
original text to the best of my knowledge and belief.

By:

A handwritten signature in black ink, appearing to be 'Martin Cross', with a long, sweeping horizontal line extending to the right.

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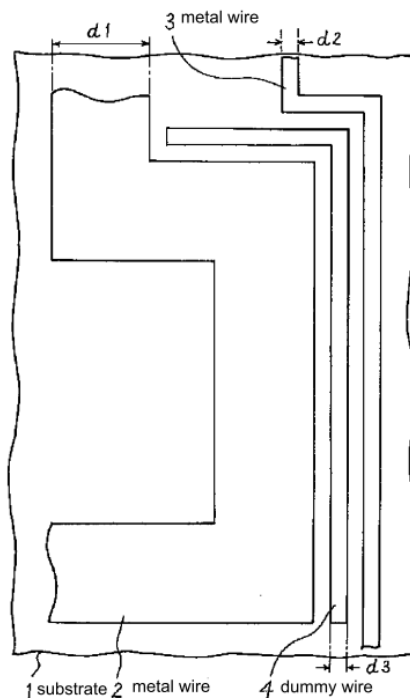
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(54) [Title of the Invention] Semiconductor Integrated Circuit Device

(57) [Abstract]

[Configuration] A dummy wire 4 is provided between a first metal wire 2 having a wide and a second metal wire 3 having a narrow wire-width. The wire-width of the dummy wire 4 is between the wire-width of the first metal wire 2 and the wire-width of the second metal wire 3.

[Effects] Growth of lateral hillocks that occurs on the first metal wire 2 having the wide wire-width is stopped by the dummy wire, such that short circuits between the first and second metal wires can be prevented.



[Claims]

[Claim 1] A semiconductor integrated circuit device characterized by comprising, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; and a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.

[Claim 2] The semiconductor integrated circuit device according to claim 1, wherein a plurality of second metal wires having differing second widths are formed, and the third width of the dummy wire is greater than or equal to the minimum wire-width among the second wires and less than or equal to the wire-width of the first wire.

[Claim 3] The semiconductor integrated circuit device according to claim 1, wherein the predetermined wire-width is 5 μm .

[Detailed Description of the Invention]**[0001]**

[Field of Industrial Application] The present invention relates to a semiconductor integrated circuit device, and particularly relates to a semiconductor integrated circuit device in which, adjacent to a metal wire having a wide wire-width of 5 μm or wider, a metal wire is formed having a narrower wire-width.

[0002]

[Prior Art] Generally, in semiconductor integrated circuit devices, metal wires are arranged primarily for the purpose of transmitting electric signals and for the purpose of connecting circuit elements and circuit blocks.

[0003] For example, in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, the widths of these metal wires are, for example, a minimum wire-width of approximately 0.8 μm to 1.2 μm for metal wires that transmit electrical signals, and is approximately 40 μm to 80 μm for the thickest metal wires, such as power supply wires and ground wires; furthermore, this is approximately 5 μm to 20 μm for the intermediate metal wires, with various wire-widths being used depending on the applications thereof.

[0004] The wire-widths of the metal wires in this conventional semiconductor integrated circuit device are established primarily in consideration of the amount of current flowing through the metal wire and the electromigration life; for example, a wider wire-width is considered necessary for metal wires with particularly large amounts of current, such as power source wires, than for other metal wires. Furthermore, for metal wires where one wishes to avoid the influence of noise to as great an extent as possible, and where one wishes to achieve a stable potential, for example, ground wires and various signal wires, the wire-width is made wider than or equal to requirements based on the electromigration life. In any case, the minimum wire-width of each of the metal wires is defined according to the individual application, and these are always designed so as to be greater than or equal to this wire-width.

[0005] Meanwhile, with increasing levels of integration in semiconductor integrated circuit devices, it is necessary to arrange metal wires having wire-widths sufficient to satisfy

the conditions described above in a limited area, and therefore the spacing between the metal wires is also narrowed, such that in a 1 Mbit DRAM, a 4 Mbit DRAM or a semiconductor integrated circuit device having approximately the same degree of integration as these, the minimum wire spacing is approximately 0.8 μm to 1.2 μm .

[0006] In metal wire forming processes for these semiconductor integrated circuit devices, although rare, a lateral hillock phenomenon sometimes occurs, in which minute protrusions similar to hillocks occur on the side of the metal wire, or minute irregularities occur along the crystal grain boundaries, which grow in subsequent heat treatment processes and ultimately short-circuit with other adjacent metal wires. The growth of these lateral hillocks is particularly pronounced if the wire-width of the metal wire is wide, because there is a considerable supply of charge and the like.

[0007]

[Problems to Be Solved by the Invention] Metal wires having wide wire-widths, such as power supply lines and ground lines, and metal wires having relatively narrow wire-widths that transmit electric signals are arranged in the conventional semiconductor integrated circuit devices described above, and because the spacing between these metal wires is narrowed so as to increase integration, lateral hillocks occur on these metal wires, and these metal wires ultimately short-circuit.

[0008] The simplest way to avoid this problem is the method of arranging the metal wires sufficiently spaced apart from other metal wires with wide wire-widths, but lateral hillocks sometimes extend to 2 to 3 μm , and thus there was a problem in so much as, if wire spacings sufficient to avoid this were provided, increases in integration were hindered.

[0009] Furthermore, another method is to cover the metal wire with a passivation film, and form this solidly, so as to suppress the occurrence of the lateral hillocks, but as this method is exacting in terms of stress migration, constraints occur in terms narrowing wire-widths, and thus there was a similar problem of hindering increases in integration.

[0010] An object of the present invention is to provide a semiconductor integrated circuit device capable of eliminating the adverse impact of lateral hillocks without hindering increases in integration.

[0011]

[Means for Solving the Problems] The semiconductor integrated circuit device of the present invention comprises, on a substrate: a first metal wire that has a first wire-width that is wider than a predetermined wire-width and is formed in a predetermined pattern; a second metal wire that has a second wire-width narrower than the predetermined wire-width and is formed at a predetermined spacing along the first metal wire; and a dummy wire that has a third wire-width that is less than or equal to the first wire-width and greater than or equal to the second wire-width and is formed between the first metal wire and the second metal wire, electrically isolated from the second metal wire.

[0012] Furthermore, this has a structure wherein a plurality of second metal wires having differing second widths are formed, and the third width of the dummy wire is greater than or equal to the minimum wire-width among the second wires and less than or equal to the wire-width of the first wire.

[0013] Furthermore, this has a structure wherein the predetermined wire-width is 5 μm .

[0014]

[Embodiments] Next, embodiments of the present invention will be described with reference to the drawings.

[0015] FIG. 1 is a plan view showing a first embodiment of the present invention.

[0016] This embodiment has a structure comprising, on substrate 1: a first metal wire 2, such as a power supply wire or a ground wire, that has a predetermined wire-width d1 (for example, 40 μm) that is wider than 5 μm and is formed in a predetermined pattern; a second metal wire 3, for transmitting electrical signals, that has a second wire-width d2 (for example 1 μm) that is narrower than 5 μm and is formed at a predetermined spacing along the first metal wire 2; and a dummy wire 4 that has a third wire-width d3 that is substantially equal to the wire-width d2 of the first metal wire 2 and is formed between the first metal wire 2 and the second metal wire 3, electrically isolated from the first and second metal wires 2 and 3. The metal wires 2 and 3 and the dummy wire 4 are formed of aluminum or an aluminum-based alloy.

[0017] By providing the dummy wire 4 in this manner, even if a lateral hillock occurs on, and extends from, the metal wire 2 having the wide wire-width, the growth of this lateral hillock will be stopped by the dummy wire 4, such that the metal wire 2 and the metal wire 3 will not short-circuit.

[0018] In this embodiment, because just one dummy wire 4 having approximately the same wire-width as the second metal wire 3 is added, and this is provided only in the region where the metal wires 2 and 3 are close to each other, the dummy wire 4 will present almost no hinderance to increased integration. Furthermore, because this is not covered with a passivation film, there is no stress migration impact.

[0019] FIG. 2 is a plan view showing a second embodiment of the present invention.

[0020] This embodiment is one in which the first metal wire 2 and the dummy wire 4a are electrically connected. In this embodiment, because the levels in the dummy wire 4a will be stable, there is an advantage in so much as the impact on the signals transmitted through the second metal wire 3 will be reduced.

[0021] In this embodiment, lateral hillocks grow large on the metal wire 2 having the wide wire-width, and thus, even though the dummy wire 4a is connected to the metal wire 2, there will be no problems in terms of operation or effect.

[0022] FIG. 3 is a plan view showing a third embodiment of the present invention.

[0023] In this embodiment, dummy wires 4b are formed on both sides of the first metal wire 2a having the wide wire-width.

[0024] In this embodiment, it suffices to simply form the dummy wire 4b on both sides of the first metal wire 2a, and therefore, as compared to the case in which a dummy wire 4, 4a is only provided in regions where the first metal wire 2 and the second metal wire 3 are close to each other, as in the first and second embodiments, there are advantages in that the number of design steps will be reduced and design oversights can be prevented.

[0025] Note that, in these embodiments, when there are a plurality of second metal wires and the wire-widths thereof differ, the wire-width of the dummy wire may be an intermediate wire-width between the minimum wire-width for the second metal wire and the wire-width of the first metal wire.

[0026]

[Effects of the Invention] As described above, the present invention has a structure in which a dummy wire is provided between a first metal wire having a wide wire-width and a second metal wire having a narrow wire-width, the wire-width of which is intermediate between the wire-widths of these metal wires, whereby lateral hillocks can be prevented from growing on the first metal wire, and the adverse impacts of lateral hillocks such as short circuits between the first and second metal wires can be eliminated, without hindering increased integration.

[Brief Description of Drawings]

[FIG. 1] This is a plan view showing a first embodiment of the present invention.

[FIG. 2] This is a plan view showing a second embodiment of the present invention.

[FIG. 3] This is a plan view showing a third embodiment of the present invention.

[Explanation of the Symbols]

1 substrate

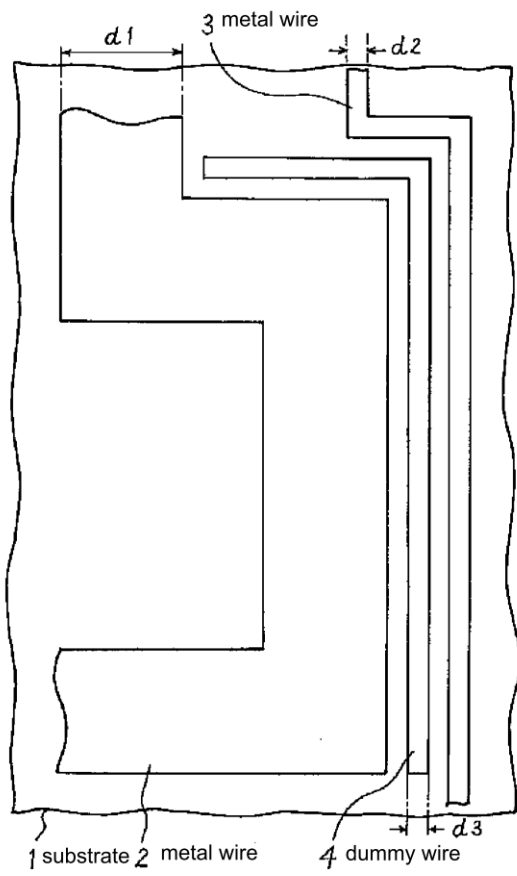
2, 2a, 3, 3a metal wire

4, 4a, 4b dummy wire

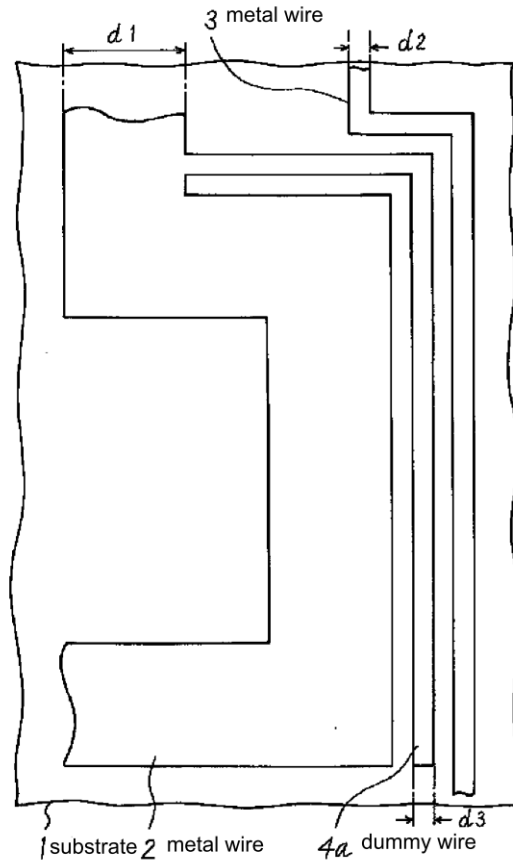
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[FIG. 1]



[FIG. 2]



(5)
[FIG. 3]

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