

Filed on behalf of: Invensas Corporation

Entered: November 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioners,

v.

INVENSAS CORPORATION,
Patent Owner.

Case IPR2018-01402
U.S. Patent No. 6,849,946

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Invensas Corporation (“Patent Owner” or “Invensas”) submits this preliminary response to the Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 6,849,946 (the “’946 patent”), filed by Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor LLC (“Petitioners” or “Samsung”).

The PTAB should deny institution since Petitioners failed to meet their burden to show “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims” (35 U.S.C. § 314(a)) due to a number of glaring deficiencies in the Petition and its supporting declaration. For example, Petitioners’ **only ground** suffers from a failure of proof of key limitations of the claims, and instead of relying on the references, relies on unsupported and conclusory assertions of Petitioners’ declarant that are driven by hindsight. Petitioners’ **only ground** fails to articulate sufficient motivation to combine. And Petitioners’ **only ground** fails to address fundamental incompatibilities between the references on which that ground is based and does not explain how predictable and reliable results of the claimed invention can be achieved. In short, Petitioners have failed to meet their burden in every ground since they failed to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim[.]” 35 U.S.C. § 312(a)(3). Moreover, Petitioners set forth substantially the same

arguments and prior art references already relied upon in a prior IPR petition denied by the Board. Petitioners attempt to thwart § 325(d) and fill gaps identified by the Board in the prior petition by relying on additional prior art that does not address the missing elements of the claimed invention. Petitioners' attempt to dress up the same prior art and arguments previously rejected by the Board in a prior IPR with additional art that fails to fill in the gaps should be rejected under § 325(d).

Due to these deficiencies and other reasons discussed herein, Petitioners cannot meet their burden of showing unpatentability and thus, institution should be denied.

Briefly, Petitioners' only ground suffers from a failure of proof. It depends on Takahashi (U.S. Patent No. 5,948,573, Ex. 1005) for disclosing the "dummy trenches" limitation required for all the challenged claims. But Petitioners fail to show that Takahashi includes any of the claimed "plurality of laterally spaced dummy trenches" or "dummy conductors in said laterally spaced dummy trenches." Petitioners point to Figures 4A-D and 1B in Takahashi, which they assert show dummy trenches. Pet. 17-20 (citing annotated versions of Figures 4A-D and 1B of Takahashi, Ex. 1005, with the alleged dummy trenches identified in gray). But Takahashi never describes those figures, and particularly the features identified by Petitioners in those figures, as showing anything called "dummy **trenches**." In fact, only "dummy **patterns**," not dummy trenches, are mentioned, which Petitioners

admit are not the same as the alleged dummy trenches. Pet. 17-18; Ex. 1005, 7:21-40. Petitioners' assertion that Takahashi discloses dummy trenches has no support other than conclusory statements from their declarant, Dr. Thomas. Pet. 17-20 (citing Declaration of Dr. Michael Thomas, Ex. 1002 ¶¶ 32, 34). But Dr. Thomas's declaration does nothing more than repeat the Petition's conclusory statements regarding Takahashi. Ex. 1002 ¶¶ 32-35. These are exactly the sort of unsupported, conclusory statements that the Board has determined do not establish a reasonable likelihood of unpatentability required to support institution. U.S. PATENT AND TRADEMARK OFFICE, TRIAL PRACTICE GUIDE UPDATE (Aug. 2018) ("Practice Guide Update") at 4–5 ("Expert testimony [] cannot take the place of a disclosure in a prior art reference, when that disclosure is required as part of the unpatentability analysis.").

In short, Petitioners' entire support for their argument that Takahashi discloses etching "dummy trenches"—a claim step that appears in ***every challenged claim***—is Dr. Thomas's conclusory and unsupported opinion. Petitioners' strategy is prohibited by 35 U.S.C. § 311(b), which mandates that *inter partes* review be requested only "on the basis of prior art consisting of patents or printed publications[,]” not mere conclusory expert testimony as explained in the Practice Guide Update. Nor does the other reference on which Petitioners rely disclose the missing dummy trenches and Petitioners do not even try to argue otherwise.

II. PERSON OF ORDINARY SKILL IN THE ART (“POSITA”)

Patent Owner does not believe it is necessary to address at this time Petitioners' proffered level of ordinary skill in the art for the limited purpose of this Preliminary Response and accepts it as sufficient for purposes of this Preliminary Response. If *inter partes* review is instituted, Patent Owner will address the level of ordinary skill in the art in its Patent Owner Response.

III. CLAIM CONSTRUCTION

Patent Owner also does not believe it is necessary to address claim construction for the limited purpose of this Preliminary Response since the identified deficiencies in the Petition discussed herein are not affected by particular claim constructions. If *inter partes* review is instituted, Patent Owner will address claim construction in its Patent Owner Response. As the '946 patent has since expired, the *Phillips* claim construction standard should apply.

In the parallel district court litigation in the U.S. District Court for the Eastern District of Texas, the Court construed the following terms from the '946 patent:

Claim Term	Court's Construction
“substantially planar” / “substantially coplanar”	plain and ordinary meaning
“trench”	plain and ordinary meaning
“dummy conductors”	“conductive structures that are not connected to any active or passive devices that function as an integrated circuit[.]”
“conductive lines”	plain and ordinary meaning

“plurality of laterally spaced dummy trenches”	plain and ordinary meaning
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See Claim Construction Opinion and Order at 4–12, *Invensas Corp. v. Samsung Elecs. Co., Ltd.*, No. 2:17-cv-00670-RWS-RSP (E.D. Tex. Oct. 26, 2018), ECF No. 193.

In the parallel district court litigation in the U.S. District Court for the District of Delaware, the Court construed the following terms from the '946 patent:

Claim Term	Court's Construction
“substantially planar” / “substantially coplanar”	“substantially flat” / “substantially at the same elevation”
“trench”	plain and ordinary meaning, provided that a “trench” does not require any particular shape, including “elongated,” nor any particular depth
“dummy conductors”	“conductive structures that are not connected to any active or passive devices that function as an integrated circuit”
“conductive lines”	“interconnects” Note: “Interconnect” or “interconnects” may be used interchangeably as the plural form of the singular term “interconnect.”
“plurality of laterally spaced dummy trenches”	“two or more dummy trenches arranged with spaces between their sides”

See generally Memorandum Opinion and Order, *Invensas Corp. v. Samsung Elecs. Co., Ltd. et al.*, No. 1:17-cv-01363-MN (D. Del. Nov. 16, 2018), ECF Nos. 66-67.

IV. PATENT OWNER'S INVENTION TO USE DUMMY TRENCHES TO ADDRESS DISHING AND EROSION ISSUES FOR SEMICONDUCTOR LAYERS

a. The '946 Patent (Ex. 1001)

The '946 patent relates to manufacturing interconnects in integrated circuits. Ex. 1001, 1:13. A process known as chemical-mechanical polishing ("CMP") is used to form a planarized layer during manufacturing of integrated circuit interconnects. *Id.* at 1:53-59. The '946 patent describes undesirable elevational disparities that may result during this process and lead to various problems, including depth-of-focus issues that make it difficult to print high resolution features. *Id.* at 1:32-52. In particular, the '946 patent describes two phenomena that lead to such disparities: (i) metal "dishing" and (ii) oxide erosion. Figure 4 of the '946 patent is reproduced below.

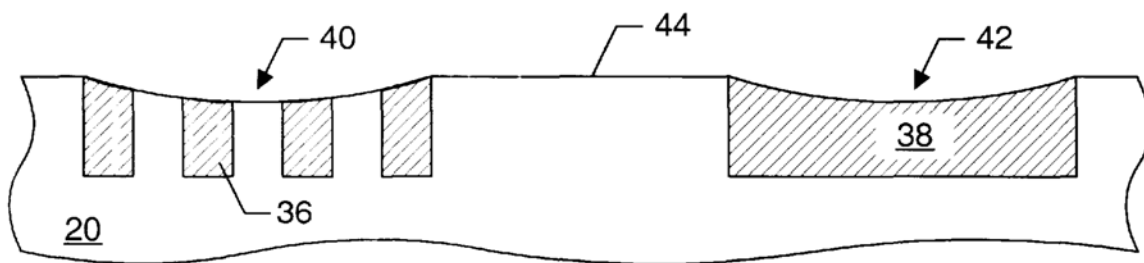


FIG. 4

According to the '946 patent, Figure 4 depicts a series of relatively narrow interconnects 36 formed in narrow trenches and a relatively wide interconnect 38 formed in a wide trench. *Id.* at 2:58-62. The narrow interconnects 36 electrically

connect underlying active devices and conductive elements of the semiconductor topography. *Id.* at 2:62-64.

Recessed area 42 depicts a localized thinning or “dishing” problem experienced by conventional metal CMP processes. *Id.* at 2:38-39, 3:3-4. The metal dishing causing recessed area 42 results from the polishing pad used in the CMP process flexing or conforming to initial deformities in the surface of the metal deposited to create wide interconnect 38. *Id.* at 3:4-24.

Recessed area 40 depicts a disparity known as oxide erosion. *Id.* at 3:26-28. Dielectric 20 may be composed of silicon oxide. *Id.* at 3:28-29. During the CMP process, a slurry is used to polish the metal of narrow interconnects 36. *Id.* at 3:29-32. First, a chemical component of this slurry reacts with the metal at a faster rate than with the silicon oxide, creating metal “steps” spaced below the surface of the oxide. *Id.* at 3:29-37. Then, the relatively small, elevated oxide regions are removed at a faster rate than the surrounding oxide by the polishing pad used in the CMP process. *Id.* at 3:37–44. This process results in recessed area 40. *Id.* at 3:25-44.

The '946 patent seeks to provide a substantially planar semiconductor topography by mitigating the problems of “metal dishing” and “oxide erosion.” *Id.* at 3:59-66. The '946 patent discloses “placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide interconnect and another region defined by a series of relatively narrow interconnect.” *Id.* at 4:1-5.

Figure 7 of the '946 patent is reproduced below.

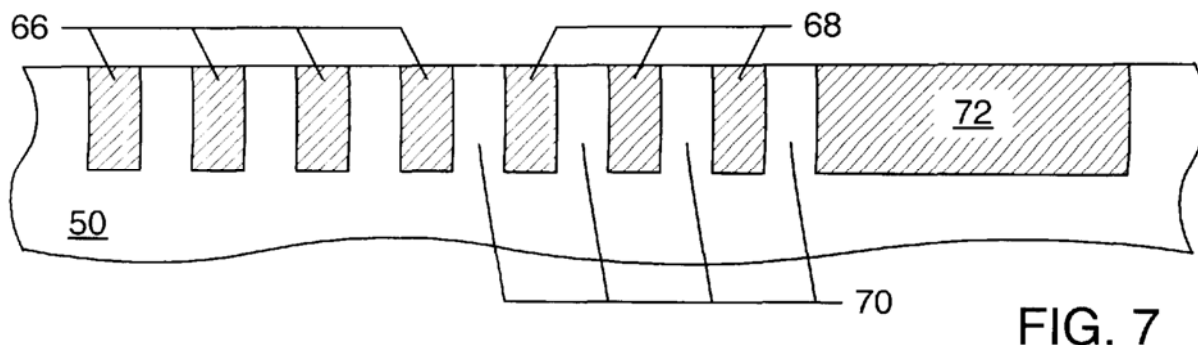


Figure 7 depicts a series of relatively narrow interconnects 66, a series of dummy conductors 68, and a relatively wide interconnect 72. *Id.* at 7:42–46. Dummy conductors 68 and interposing dielectric protrusions 70 “replace a relatively wide dielectric region absent of any conductive material,” such as area 44 of Figure 4. *Id.* at 5:31–34.

According to one embodiment, dummy conductors 68 are formed by etching dummy trenches into the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. *Id.* at 4:14-17. “The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively.” *Id.* at 4:20-23. Conductive material deposited on top of the dielectric layer is polished to form dummy conductors in the dummy trenches, which “serve no purpose except to improve the planarization of the interconnect level in which they reside.” *Id.* at 4:29-

42.

The '946 patent explains that dummy conductors 68 prevent metal dishing because the metal of the dummy conductors is softer than the surrounding dielectric. *Id.* at 5:34–45. Because the surface area of the dielectric protrusions between the dummy conductors is not sufficient to withstand the force of the polishing pad, the surface of the polishing pad remains substantially flat across the dummy conductors and wide interconnect during polishing. *Id.* Thus, the presence of the dummy conductors mitigates the flexing or contracting of the polishing pad during the CMP process that can lead to dishing. *Id.*

The '946 patent further explains that dummy conductors 68 also prevent oxide erosion. As before, the conductive material of the interconnects and dummy conductors may be polished more rapidly than the surrounding dielectric once the surface of the conductive material has been removed to the same elevational plane as the dielectric. *Id.* at 5:47-51. Once the dummy conductors 68 and narrow interconnects 66 are polished to a consistent level below the surrounding dielectric, the polish rate of the elevated dielectric protrusions becomes greater than the recessed dummy conductors and interconnect. *Id.* at 5:51-61. As polishing continues, the dielectric protrusions are “again made substantially coplanar with the dummy conductors and the interconnect.” *Id.* This cycle may be repeated until it is desirable to stop the polishing process. *Id.*

b. Illustrative Claim

Claim 16 is the only independent claim at issue. Claim 16 is representative of the challenged claims and reproduced below.

16. A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches,

wherein each of the second trenches is relatively narrow compared to the first trench and

wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches;

dummy conductors in said laterally spaced dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of second trenches and said first trench,

wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Ex. 1001, 10:23–40.

V. SUMMARY OF THE PROSECUTION HISTORY

U.S. Patent Application No. 09/779,123, which led to the '946 patent, was filed on February 7, 2001. It is a continuation of U.S. Application No. 09/143,723, which was filed on August 31, 1998, and to which the '946 patent claims priority.

U.S. Application No. 09/143,723 issued as U.S. Patent No. 6,232,231.¹ During prosecution of the '946 patent, the Examiner issued a non-final rejection based on U.S. Patent No. 6,093,631 to Jaso et al. ("Jaso"). After further correspondence between the Examiner and the patentee, the Examiner withdrew his objections based on Jaso and the patent ultimately issued on February 1, 2005. In the notice of allowance, the Examiner stated that "Jaso et al. at least neither teach nor suggest that the *second* trenches is a (*sic*) relatively narrow compared to the first trench and that polishing the conductive material by applying a liquid substantially *free of particulate matter* between an abrasive polishing surface and the conductive material. Therefore, the instant invention is neither anticipated nor rendered obvious over the prior art of record." Ex. 1004, p. 302 (emphasis in original).

VI. PREVIOUS BOARD PROCEEDINGS REGARDING THE '946 PATENT

The '946 patent was the subject of *Broadcom Ltd. v. Invensas Corp.*, IPR2017-00107 ("*Broadcom*"), a prior petition for *inter partes* review filed on October 18, 2016. The petitioner in *Broadcom* advanced five grounds for why it

¹ U.S. Patent No. 6,232,231 is the subject of a separate petition for *inter partes* review filed by Petitioners that relies on the same art as in this Petition. Case IPR2018-01401.

believed that the claims of the '946 patent were unpatentable. Ground 1 of *Broadcom* challenged claims 16-20 of the '946 patent as anticipated by Takahashi. See *Broadcom Ltd. v. Invensas Corp.*, IPR2017-00107, Paper 1 at 2 (P.T.A.B. Oct. 18, 2016). Takahashi is the same reference used in the only ground asserted here. Grounds 2-5 of *Broadcom* challenged additional claims and/or relied on references not at issue in the present Petition.

Broadcom was **denied** institution in its entirety because, among other things, Takahashi, the primary reference for Ground 1 of *Broadcom*, did not disclose the requirement in the challenged claims “wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches[.]” *Broadcom*, Paper 7 at 8-9 (P.T.A.B. Mar. 15, 2017).

The ground in the present Petition is largely duplicative of Ground 1 in *Broadcom*. Ground 1 in the present Petition challenges the same claims as in Ground 1 of *Broadcom* and relies on the same primary reference as in *Broadcom*, adding only a single additional reference, Japanese Patent Application 4-262535 (“Tonishi”) (Ex. 1007 (certified translated version)), with Petitioners arguing that Tonishi supplies what the Board found missing from Takahashi. Pet. 14-15 (arguing that Tonishi discloses narrow signal lines and wide power lines that address the required narrow trenches and wide trench the Board found missing from

Takahashi).²

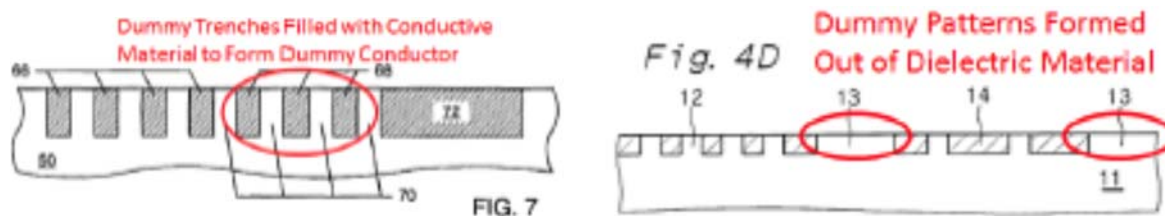
VII. BRIEF DISCUSSION OF THE REFERENCES

a. U.S. Patent No. 5,948,573 (“Takahashi”) (Ex. 1005)

Unlike the '946 patent that teaches the addition of a plurality of laterally spaced dummy trenches filled with conductive material to form dummy conductors

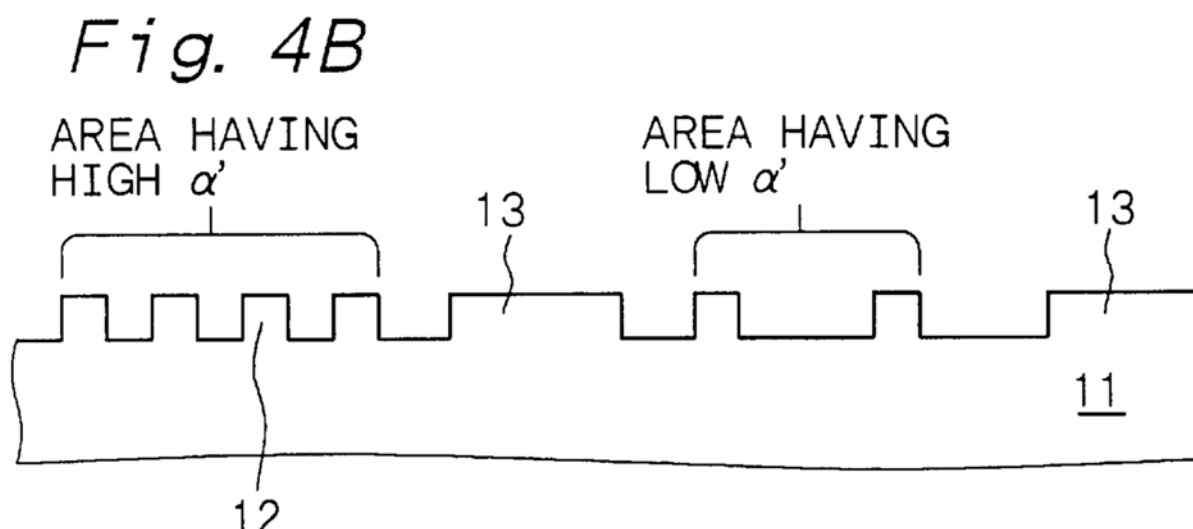
² While Samsung and Broadcom are not the same petitioner, the similarity of the only ground in the present Petition to Ground 1 of *Broadcom* raises many of the same concerns the Board expressed in *General Plastic*, particularly the adverse impact on efficiency and fundamental fairness when petitioners use the Board's prior decisions “as a roadmap, until a ground is found that results in the grant of review.” *Gen. Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2017-01357, Paper 19 at 15–19 (P.T.A.B. Sept. 6, 2017). Samsung also appears to have known about the Tonishi reference since at least November 16, 2017, when it was translated, but has provided no explanation for its delay in filing the present Petition. *See* Ex. 1007, at 1. For at least these reasons, the Board should use its discretion to deny institution of ground 1 of the present Petition. *See Shenzhen Silver Star Intelligent Tech. Co., Ltd. v. iRobot Corp.*, IPR2018-00761, Paper 15 at 7–15 (P.T.A.B. Sept. 5, 2018) (denying institution based on the *General Plastic* factors where the follow-on petitioner was not the same entity as the original petitioner).

to address planarization issues, Takahashi teaches its antithesis—the addition of dummy patterns formed out of dielectric material (*e.g.*, SiO₂).



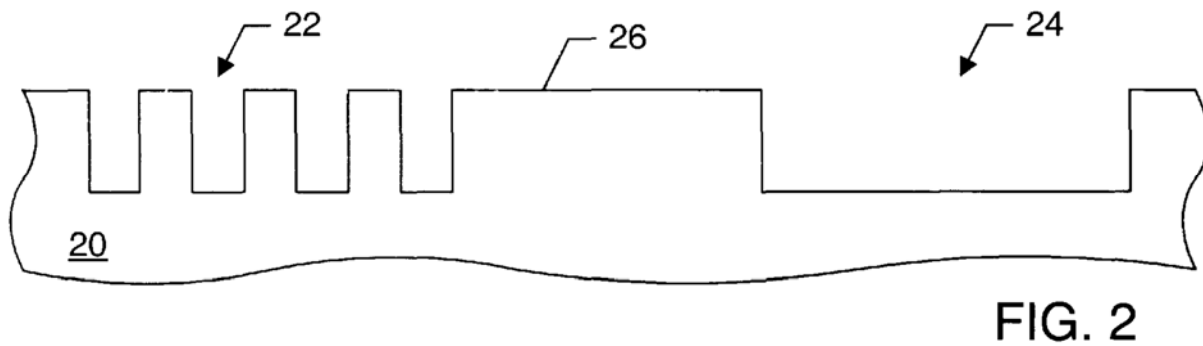
'946 Patent (Ex. 1001), Fig. 7 (annotated) Takahashi (Ex. 1005), Fig. 4D (annotated)

In particular, Takahashi discusses designing an integrated circuit by combining partial circuits, each of which is called a circuit block. Ex. 1005, 1:14-16. “A pattern constituting an integrated circuit generally belongs to one of [the] circuit blocks.” *Id.* at 1:16-18. Takahashi discloses adding what it calls “dummy patterns” to areas where there is no existing pattern. *Id.* at 7:21-44. As shown in Figure 4B of Takahashi, below, the dummy patterns 13 create areas where additional dielectric material 11 exists (or more accurately, is not etched away).



Takahashi does not disclose or suggest that “dummy pattern 13” consists of anything other than the raised area identified in Figure 4B above, and Takahashi does not disclose that “dummy pattern 13” includes any surrounding trenches or conductive wiring. *See, e.g.*, Ex. 1005 at Fig. 4B. Notably, Takahashi's own definition of the term “dummy pattern” contains no mention or suggestion that the dummy pattern includes a dummy trench or a dummy conductor in such a trench. *Id.* at 7:25-26 (defining “dummy pattern” as “a pattern which does not constitute any circuit of an integrated circuit.”). Instead, Takahashi's definition of “dummy pattern” confirms that the raised area 13 of Figure 4B is built up from dielectric material such as SiO₂ and is not connected to active circuitry.

In contrast, the '946 patent teaches the use of dummy trenches and dummy conductors that are formed by the opposite technique of **removing** (such as by etching) dielectric material to address dishing and erosion issues. Takahashi most closely resembles the conventional metal CMP processes that the invention in the '946 patent improved upon. For example, in Figure 2 below from the '946 patent, which illustrates a conventional prior art CMP process, the central expanse 26 resembles dummy pattern 13 from Takahashi's Figure 4B, above.



Notably in contrast, Takahashi does not disclose removing dielectric material, such as in area 26 above, to create dummy trenches. But this is exactly what the '946 patent claims cover. For this reason, Takahashi cannot achieve the results of the '946 patent.

Furthermore, as the Board recognized in the denial of institution in *Broadcom*, Takahashi fails to provide any information about the specific dimensions of the grooves and raised areas depicted in Figures 4A-4D or make any representation that the Figures are drawn to scale. The only lateral dimension taught by Takahashi is that there can be “space, e.g., of 5 μm between the pattern and the dummy pattern.” Ex. 1005, 7:39-40. Takahashi also explains that “[w]hen the above space cannot be provided, or when the dummy pattern to be provided is too small (smaller than a size about twice as large as a minimum design size), it is not necessary to provide such dummy pattern.” *Id.* at 7:40-44. These statements do not provide any information as to the dimensions or relative sizes of the structures of Figure 4, and “it is well

established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (internal citation omitted); *Neutrino Dev. Corp. v. Sonosite, Inc.*, 423 F. Supp. 2d 673, 677-78 (S.D. Tex. 2006) (holding that even arguments based on general proportions or relative size of features shown in a patent figure are improper where there is no explicit disclosure in the patent specification identifying the scale or dimensions) (citing *Hockerson-Halbertstadt*, 222 F.3d at 954, 956).

Accordingly, Takahashi teaches the opposite of the ’946 Patent—where the ’946 Patent teaches dummy conductors, Takahashi teaches dummy insulators (*e.g.*, dummy patterns). It is therefore not surprising that Takahashi does not mention “dummy trenches” or “dummy conductors” formed in such trenches.

b. Japanese Patent Application 4-262535 (“Tonishi”) (Ex. 1007)

Unlike the ’946 patent, Tonishi is not concerned with any planarity issues that can arise from etching or polishing processes during the fabrication of an integrated circuit. In fact, Tonishi never even mentions polishing, nor achieving a substantially planar semiconductor topography. There are at least two reasons for this. First, there is no dispute that Tonishi discloses the creation of metal wires for an integrated circuit using a subtractive process, not the damascene process that is the subject of

the '946 patent.³ See Pet. 31 (instead, acknowledging Tonishi solely describes a subtractive method). Using a subtractive process such as that disclosed in Tonishi would not have created dummy trenches via etching as the challenged claims require. Second, regardless of the process used to form the metal wires in Tonishi, Tonishi is focused on solving a problem that can arise during subsequent heat treatment processes: short circuiting of two adjacent wires due to lateral hillocks. Ex. 1007, ¶ 6. Neither Takahashi nor the '946 patent mention heat treatment, nor the problem of short circuiting or lateral hillocks. Furthermore, Petitioners do not point to anything in the record to show that the formation of lateral hillocks is a concern in the damascene process or that a person of ordinary skill in the art would

³ As Petitioners acknowledge, one of the differences between the subtractive process and the damascene process is that in the subtractive process, conductive material is deposited as a blanket layer and then those portions of the conductive material that are not part of an interconnect are etched away. Pet. 5. In contrast, for the damascene process, trenches are formed in a non-conductive material via etching, and then those trenches are filled with conductive material to form interconnects. *Id.* at 5-6.

have considered a reference that addresses lateral hillocks when considering how to mitigate metal dishing or oxide erosion during the damascene process.

To purportedly solve the problem of lateral hillocks, Tonishi suggests the addition of a single dummy wire between two adjacent wires. *Id.* at ¶¶ 11-12, 16-17. Because the dummy wire is interposed between the adjacent wires, any lateral hillocks from one of those wires will contact the dummy wire, and not the other adjacent wire. *Id.* at ¶ 17. While Tonishi does disclose that a dummy wire can be placed between a wide wire and a plurality of narrow wires, Tonishi is silent on how that dummy wire is formed and does not disclose dummy trenches at all. *Id.* at ¶¶ 11-12. In addition, Tonishi specifically teaches using a **single** dummy wire between a wide wire and a narrow wire, not a plurality of dummy wires as claimed.⁴ *Id.* at ¶ 18. Thus, Tonishi does not disclose and would not teach one of ordinary skill in the art to etch a plurality of dummy trenches between a wide trench and a series of narrow trenches as claimed by the '946 patent.

⁴ Separately, Tonishi discloses a single embodiment where a dummy wire is placed on either side of the wide wire, but again, as between the wide wire and any adjacent narrow wires on either side, there would only be a single dummy wire between the wide wire and each adjacent narrow wire. Ex. 1007, ¶ 24.

VIII. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1 DUE TO CRITICAL DEFICIENCIES AND OTHER REASONS

Petitioners failed their burden of demonstrating “with particularity . . . the evidence that supports the grounds for the challenge to each claim[.]” 35 U.S.C. § 312(a)(3). For the sole ground, Petitioners fail to meet their burden of proof to show the elements of the claims are in the prior art, individually or in combination, and instead rely in critical ways on their declarant’s hindsight-driven, unsupported and conclusory assertions. For the sole ground, Petitioners fail to articulate sufficient motivation to combine references. And for the sole ground, Petitioners fail to address fundamental incompatibilities between the references on which that ground is based and thus cannot show that predictable results can be obtained. The Board should therefore exercise its right to deny institution for the sole ground for all challenged claims.

a. Deficiencies In Ground 1 (Takahashi in view of Tonishi)

Claims 16-20 are challenged in ground 1 as obvious under 35 U.S.C. § 103 over Takahashi in view of Tonishi. At the threshold, Petitioners fail to show that Takahashi includes any of the claimed “plurality of laterally spaced dummy trenches” or “dummy conductors in said laterally spaced dummy trenches.” Tonishi does not disclose any trenches, whether dummy trenches or otherwise, so the dimensions disclosed in Tonishi regarding wires are simply irrelevant and do not

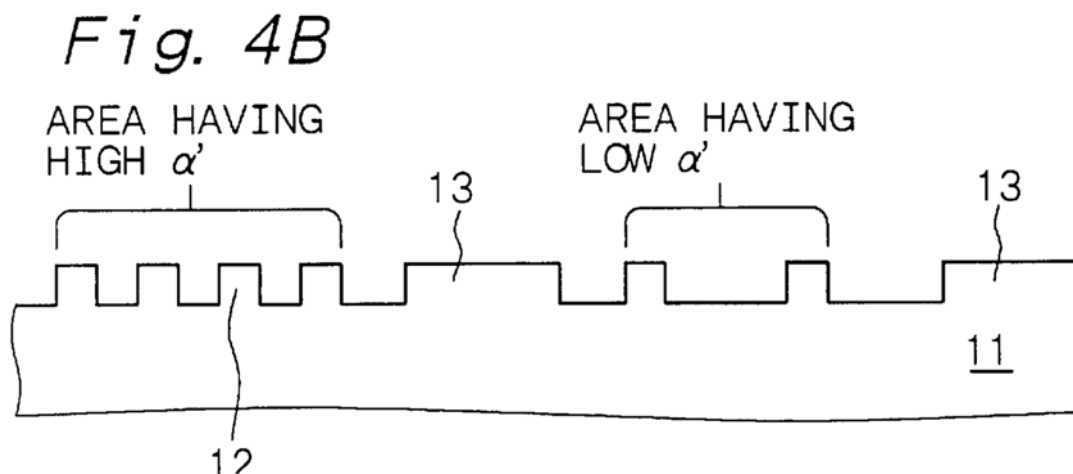
supply the required trench dimensions missing from Takahashi. As a result, Petitioners' arguments are essentially no different than the arguments the Board rejected in the *Broadcom* IPR. Furthermore, Petitioners' arguments regarding a motivation to combine Takahashi and Tonishi are based on conclusory statements regarding the broad field in which Takahashi and Tonishi lie and fail to address that they are two very different references that apply different techniques to address vastly different problems. Accordingly, as discussed in more detail below, Petitioners' ground 1 is deficient, and trial should not be instituted on this ground.

1. Petitioners fail to show that either Takahashi or Tonishi disclose the claimed “plurality of laterally spaced dummy trenches” or “dummy conductors in said laterally spaced dummy trenches”

Petitioners' argument starts with a false premise—that either reference on which Petitioners rely discloses the claimed “plurality of laterally spaced dummy trenches” or “dummy conductors in said laterally spaced dummy trenches.” Because Petitioners cannot show that either Takahashi or Tonishi disclose these required claim elements, there is no basis to conclude that the challenged claims are obvious in light of these references.

With respect to Takahashi, Petitioners point to nothing other than self-serving and conclusory statements in support of their argument that Takahashi discloses dummy trenches and corresponding dummy conductors, which is simply

insufficient. *See, e.g., AnyLogic N. Am., LLC v. TheBrain Techs., LP*, IPR2018-00546, Paper 10 at 18 (P.T.A.B. May 24, 2018) (denying institution and explaining that AnyLogic fails to “point to any evidence, apart from a conclusory statement by [its expert] that Duncan’s system necessarily operates in this manner[.]”); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01587, Paper 8 at 27 (P.T.A.B. Dec. 15, 2017) (informative) (denying institution and finding that the petitioner’s expert declaration “does not provide persuasive facts, data, or analysis to support [the] stated opinion[.]”); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1364 (Fed. Cir. 2016) (affirming the Board’s determination that the petitioner did not meet its burden of showing unpatentability where petitioner’s arguments and expert testimony were “conclusory”). As discussed above, Takahashi discloses only dummy **patterns**. *See, e.g.,* Ex. 1005, 16:9-43. Figure 4B, on which Petitioners rely, is illuminative on this point. As seen below, Figure 4B specifically identifies element 13 as a dummy pattern, but does not identify the lower portions on either side of the dummy pattern as dummy trenches.



See also *id.* at 16:9-43 (describing Figures 4A-4D). This is not surprising, as Takahashi specifically defines a “dummy pattern” as “a **pattern** which does not constitute any circuit of an integrated circuit.” *Id.* at 7:25-26 (emphasis added). Nor is the dummy pattern in Figure 4B formed of conductive material; the dummy pattern is instead made of a dielectric material such as SiO₂ and is formed by adding, not removing, that dielectric material. *Id.* at 16:18-28. Takahashi further specifically distinguishes dummy patterns from the spaces around the dummy pattern. See *id.* at 7:35-40 (“space, e.g., of 5 μm between the pattern and the dummy pattern[.]”).

Petitioners argue that those spaces are nonetheless dummy trenches because “the two spaces . . . are trenches that are not part of any integrated circuit[.]” Pet. 37.

But this assertion is based on nothing more than attorney argument.⁵ Takahashi nowhere discloses that the grooves on either side of the dummy pattern qualify as dummy features, let alone dummy trenches. Nothing in Takahashi suggests one way or the other to a POSITA whether they are dummy features or connected to the integrated circuit. While Takahashi does say that a “pattern constituting an integrated circuit generally belongs to one of circuit blocks,” the use of “generally”

⁵ While Petitioners appear to rely on the expert declaration for support, in particular paragraph 62, all the expert declaration does is cut-and-paste the exact same language from the Petition. *Compare* Pet. 37 with Ex. 1002, ¶ 62. This is not the only instance in which the expert's declaration consists of nothing more than unsupported attorney argument cut-and-pasted from the Petition. Almost every cite in the Petition to the expert's declaration is to a paragraph in the expert's declaration that simply repeats the exact same language found in the Petition itself. Such “[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” 37 C.F.R. § 42.65(a). The Federal Circuit has rejected expert testimony that merely parrots the Petitioner's language. *Harmonic Inc.*, 815 F.3d at 1363 (rejecting expert testimony that “add[s] nothing beyond the conclusory statements in [the] petition.”).

makes it clear that Takahashi explicitly allows for instances where the integrated circuit is not confined to circuit blocks. *Id.* at 1:16-18 (emphasis added). Thus, Petitioners establish nothing with their attempt to rely on their own annotated Figure 1B and its identification of the spaces or grooves as being outside a circuit block. Pet. 36-37. At a minimum, Takahashi fails to disclose that those spaces (or any other features) are not connected to the integrated circuit, nor that those spaces are “dummy trenches” in which “dummy conductors” are formed.

Petitioners do not point to any evidence for their assertion that the spaces are dummy trenches. Petitioners literally cite to nothing when they assert that “[t]hese two spaces (marked by [Petitioners’ own annotated] gray arrows) are dummy trenches.” Pet. 17. And the gray arrows referenced point back to Figure 4B, which, as discussed above, is not described or identified by Takahashi as including dummy trenches. Petitioners repeat this assertion again and again, pointing only to Figures 4A-4D and columns 7 and 16 of Takahashi, which as discussed above do not disclose dummy trenches. *See, e.g., id.* at 17-20, 34-38.

Petitioners further overstep when they mischaracterize the Board’s opinion in *Broadcom* by asserting that the Board “noted” that Takahashi’s “Figures 4A-4D depict placing intermediate-sized dummy trenches (gray) between a wide trench (red) and narrow trenches (green)[.]” Pet. 20. The Board did no such thing. Looking at the denial of institution in *Broadcom*, the Board specifically does not characterize

any of the trenches in Takahashi as being a dummy trench or not, but rather limits its opinion to confirming that Takahashi does not disclose any dimensional information regarding the features shown in Figure 4B. *Broadcom*, Paper 7, at 8-9.

With respect to Tonishi, Petitioners do not even attempt to argue that Tonishi discloses the claimed dummy trenches. Pet. 38-41. And while Petitioners do assert that Tonishi discloses a dummy conductor, they do not assert that any such dummy conductor is in a dummy trench as required by the claims. *See, e.g.*, Pet. 20-23, 38-41. Indeed, Tonishi does not even mention trenches as the claims require. Nor do Petitioners contest that Tonishi fails to disclose the other claim limitations, including “conductive lines in said series of second trenches and said first trench”

As neither Takahashi nor Tonishi disclose the claimed “plurality of laterally spaced dummy trenches” or “dummy conductors in said laterally spaced dummy trenches,” Petitioners cannot show that the combination of Takahashi and Tonishi includes all the required elements or makes the challenged claims of the '946 patent obvious, regardless of what attorney arguments Petitioners might make or conclusory statements Petitioners' expert might declare. “[B]ecause an *inter partes* review may only be requested ‘on the basis of prior art consisting of patents or printed publications,’ 35 U.S.C. § 311(b), expert testimony cannot take the place of disclosure from patents or printed publications.” Practice Guide Update at 5. Accordingly, for this reason alone, ground 1 of the Petition should be denied

institution.

2. Petitioners fail to show that Tonishi discloses the dimensional limitations that the Board found were missing in Takahashi

Even setting aside the lack of any disclosure in Takahashi (or for that matter Tonishi) of “dummy trenches” or “dummy conductors” in dummy trenches, Petitioners essentially attempt to repackage the rejected argument from the earlier *Broadcom* IPR that Takahashi discloses the limitation “wherein a lateral dimension of at least one of the laterally spaced dummy trenches is less than a lateral dimension of the first trench and greater than a lateral dimension of at least one of the series of second trenches” (“Dimensional Limitation”). While Petitioners are not so bold as to assert Takahashi explicitly discloses the Dimensional Limitation, they use hindsight to graft Tonishi, an unrelated reference, to Takahashi to supply the missing Dimensional Limitation simply because Tonishi discloses some relative dimensions, albeit not for trenches or conductors formed in such trenches.

As discussed above, Tonishi does not disclose any of the limitations of the independent claims. Tonishi at most mentions generic “metal wire forming processes” for the wires described therein. Ex. 1007, ¶ 6. And Petitioners concede that Tonishi only discloses at most subtractive etching, which does not create wires using trenches. Pet. 31. Accordingly, there is no disclosure in Tonishi of any process to create its wires in trenches as required by all of the challenged claims. More

specifically, there is no basis to conclude that the wire widths disclosed in Tonishi relate to the trenches disclosed in Takahashi given the distinction between the wires and trenches. And there would be no reason—other than hindsight—to apply the wire dimensions in Tonishi to ascribe dimensions to the trenches disclosed in Takahashi. Tonishi adds nothing new to the disclosures in Takahashi, and so Petitioners' argument that Takahashi, even combined with Tonishi, invalidates the challenged claims of the '946 patent, is substantively the same as the argument made in *Broadcom* regarding Takahashi, which the Board has already rejected.

Petitioners are not justified in their attempt to bootstrap their argument regarding finding the Dimensional Limitation in Takahashi by considering it with the knowledge of Tonishi. Petitioners acknowledge that "Takahashi is silent on whether its figures are drawn to scale," but attempt to get around that by arguing that "its figures must be viewed based on the knowledge of a POSA, as reflected by Tonishi." Pet. 27. But "it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue[,]" as Petitioners acknowledge is true for Takahashi. *Hockerson-Halberstadt*, 222 F.3d at 956. Petitioners try to overcome this clear instruction from the Federal Circuit by relying on *Paice LLC v. Ford Motor Co.* See Pet. 27-28 (citing 722 F. App'x 1015 (Fed. Cir. 2018) (nonprecedential)). But the facts in *Paice* were very different—unlike the figures in

Takahashi, in *Paice* the Federal Circuit explicitly found that “Figure 11 of Ibaraki provides some scale information[,]” as it “specifies 0 at the intersection of the x- and y- axes, both of which run continuously,” and “the parties’ experts both treated the scale of the axes as linear[.]”⁶ 722 F. App’x at 1022. Thus, *Paice* fails to support Petitioners’ attempt to impose a scale on Takahashi’s figures when no basis to do so exists.

3. Petitioners’ conclusory statements about the field of the references and the generic problems in the field cannot replace the analysis required to establish a motivation to combine

Petitioners’ arguments regarding the motivation to combine Takahashi and Tonishi are based on nothing more than generalities about Takahashi and Tonishi and the generic problems in the field, and are therefore insufficient to establish a motivation to combine.

⁶ Petitioners also misunderstand what *Paice* is referring to as “the understanding of a person of skill[.]” Pet. 27 (citing *Paice*, 722 F. App’x at 1022). Separate and apart from Ibaraki’s Figure 11 (which contained scale information), the Federal Circuit found additional support based on the expert’s opinion that “a person of skill would understand” the limitation was taught because “it would not make sense to a person of skill” otherwise. 722 F. App’x at 1022. Petitioners do not make this argument.

Petitioners make two arguments in support of a motivation to combine Takahashi and Tonishi: (1) “Tonishi discloses reasons and benefits for selecting various wire-widths in integrated circuits that are generally applicable to all integrated circuit designs, including the design disclosed in Takahashi[.]” and (2) a “POSA would have further been motivated to combine Takahashi with Tonishi because both references aim to improve manufacturing yield of semiconductors through the use of dummy features.” Pet. 25, 28. Neither argument provides a reason (supported by the reference) why a POSITA would be motivated to look to the other reference, and therefore the arguments do not hold up to any scrutiny.

With respect to the argument that both references are directed towards the field of “integrated circuit designs,” Petitioners’ argument boils down to the statement that “Tonishi’s teachings relating to the relative sizes of power and signals interconnects are applicable to any design.” Pet. 26 (emphasis added). But the Federal Circuit has previously rejected combining art simply because they “both fall[] within the same alleged field,” as “[s]uch short-cut logic would lead to the conclusion that any and all combinations of elements known in this broad field would automatically be obvious, without the need or any further analysis.” *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 Fed. App’x 971, 977 (Fed. Cir. 2017); see also *Westinghouse Air Brake Techs. Corp. v. Siemens Indus., Inc.*, IPR2017-00582, Paper 12, at 13 (P.T.A.B. July 19, 2017) (“Petitioner’s argument regarding the

similarity of architecture and capabilities in Curtis and Collins [] is unpersuasive because Petitioner does not explain what similarities would have provided a reason to combine those references in the claimed manner.”) Petitioners simply do not explain why—other than hindsight—a person of skill in the art would have been motivated to look to Tonishi, from the wide field of integrated circuit design, and to then combine it with Takahashi, especially given that Tonishi does not share any of the elements for which Petitioners rely on Takahashi.

Petitioners' mistake in failing to explain why there would be a specific motivation to combine Takahashi and Tonishi is magnified by the fact that the disclosures in Takahashi and Tonishi on which Petitioners rely are directed towards two entirely different techniques for fabricating integrated circuits. Petitioners assert that Takahashi discloses two separate techniques for fabricating integrated circuits: a subtractive method, which etches conductive material, and a damascene method, which etches dielectric material. Pet. 33. But these two methods are not interchangeable, as the art Petitioners rely on makes clear. *See, e.g.*, Ex. 1019, 1:15-22 (distinguishing between damascene and traditional metal etching). And besides, Petitioners do not explain how these techniques would be combined or used one for the other. Such an attempt to mix-and-match two alternative methods should be rejected. *See Westinghouse*, Paper 12, at 14 (rejecting attempt to combine disclosures in the same reference related to “two alternative technologies[]”).

Petitioners clearly recognize the differences between the two techniques, since Petitioners limit their reliance on Takahashi to the disclosure in Takahashi of what they assert is the damascene method, as exemplified in Figures 4A-4D. Pet. 34-38; *see also id.* 16 (“Figures 4A-D depict the use of dummy conductors for a damascene process”). Petitioners do not explain how a POSITA could combine Tonishi, a reference that discloses adding a dummy wire to a subtractive etch process, with Takahashi, a reference that discloses adding a dummy pattern to a process that Petitioners assert is a damascene process. To the extent that a person of skill in the art would be inclined to combine the disclosures in Tonishi (which Petitioners acknowledge solely describes the subtractive method, Pet. 31) with Takahashi, that combination would be with the subtractive method disclosures in Takahashi, not the purported damascene method disclosures in Takahashi on which Petitioners rely. Petitioners do not explain why a POSITA would want to replace the primary reference's purported damascene method with the subtractive method.

Petitioners' second argument regarding motivation to combine fares no better. Petitioners ignore that Takahashi and Tonishi are directed towards solving entirely different problems when it lumps them together under the generic objective of “increasing yield in high density integrated circuits.” Pet. 28-31. But as with Petitioners' conclusory and generic statement that Takahashi and Tonishi are both directed towards the design of integrated circuits, simply stating that both Takahashi

and Tonishi would help improve yield, without more, does not establish why a POSITA would be motivated to combine these specific references. Improving yield is a generic consideration applicable to all integrated circuit design and manufacturing. Ex. 1019, 1:15-17. But this is not enough. *See Securus*, 701 Fed. App'x at 976. Petitioners provide no basis for why a POSITA would be motivated to combine these two specific references as opposed to others from the entire field of integrated circuit design and manufacturing. What is completely missing from the Petition is an explanation of how Tonishi's disclosure of a way to reduce the problem of "hillocks," which occur during heat treatment processes, applies to the disclosures in Takahashi which purport to address dishing, which occurs during an entirely different process of etching and planarization not disclosed or addressed by Tonishi. *Compare* Ex. 1007, ¶¶ 6, 10 *with* Ex. 1005, 2:47-56. And nothing in Tonishi suggests that any teaching found therein would help a POSITA with the dishing problems addressed by Takahashi. Furthermore, Petitioners do not point to any evidence in either reference that "hillocks" are an issue with etching and/or planarization or anything else in Takahashi, nor that Takahashi was concerned with hillocks. Thus, there would be no motivation for a person of skill in the art to look to and apply any teaching in Tonishi to solve a problem that does not exist in Takahashi. "A motivation to combine the teachings of references cannot be based on the alleged existence of a problem that does not exist in the specific asserted

combination.” *Aruba Networks, Inc. v. XR Commc’ns LLC*, IPR2018-00701, Paper 10, at 10 (P.T.A.B. Aug. 27, 2018) (internal citation omitted). Nor can Petitioners rely on conclusory statements regarding the common field in which these references lie when the references themselves provide no support for such a combination. See, e.g., *Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 990 (Fed. Cir. 2016) (“[T]he Board correctly concluded that [the petitioner] did not articulate a sufficient motivation to combine. With respect to [certain challenged claims], [the petitioner] gave no reason for the motivation of a person of ordinary skill to combine [the two references] except that the references were directed to the same art or same techniques. . . .”).

In sum, Petitioners attempt to stitch together two references that address different problems, use different techniques to solve those problems, and together fail to fully disclose all elements of the challenged claims. Hindsight has driven Petitioners to their conclusions. This is far from the sort of “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness” that is required. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citation and internal quotations omitted).

4. Petitioners fail to show that a POSITA could predictably combine Takahashi with Tonishi

Petitioners also fail to sufficiently articulate how the combination of

Takahashi and Tonishi would successfully lead to the claimed invention. “Predictability” is the “touchstone of obviousness.” *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326 (Fed. Cir. 2009) (citing *KSR Int’l*, 550 U.S. 398). The concept of “predictable” is understood to mean “whether a person of ordinary skill in the art would, at the relevant time, have had a ‘reasonable expectation of success[.]’” *Institut Pasteur & Universite Pierre Et Marie Curie v. Focarino*, 738 F.3d 1337, 1344 (Fed. Cir. 2013) (citing cases). To show a reasonable expectation of success, a petitioner must “explain convincingly, with adequate specificity, how one would have achieved that result[.]” *Biodelivery Scis. Int’l, Inc. v. Monosol Rx, LLC*, IPR2015-00167, Paper 6 at 28 (P.T.A.B. May 20, 2015).

Instead of providing the required specificity, Petitioners assert in conclusory fashion that “a POSA would have known to use the dimensions disclosed by Tonishi in Takahashi because such a combination involves only the use of a known technique to improve a similar device with no unexpected results.” Pet. 24. Although Petitioners cite to their expert for support, Dr. Thomas’s declaration merely parrots the language in the Petition. *Compare* Ex. 1002, ¶ 41 *with* Pet. 23-25. Petitioners’ casual summation of the prior art does not explain with any specificity exactly how a POSITA would successfully modify Takahashi with the disclosures of Tonishi (which does not even disclose any trenches) to achieve the specific dummy trenches

and dummy conductors formed in the trenches claimed in the '946 patent.

The absence of evidence throughout the Petition on how Takahashi and Tonishi could fit together—particularly given the differences in their purposes, the technology and structures, let alone with unexplained modifications—is fatal to Petitioners' argument for why the result would be a predictable and reliable combination. Petitioners fail to address why or how a POSITA would modify the alleged damascene structures in Takahashi with the subtractive etching structures in Tonishi, why Tonishi's disclosure of a single dummy wire would result in adding a plurality of laterally spaced dummy trenches to Takahashi, or why Tonishi's proposed solution to hillocks would be applicable to the issues discussed in Takahashi regarding dishing.

Based on these facial deficiencies regarding a POSITA's motivation to combine Takahashi and Tonishi, as well as the predictability of that combination, Petitioners fail to meet their burden under 35 U.S.C. § 314(a) with respect to ground 1. Given the fatal flaws in Petitioners' arguments with respect to ground 1, institution of the Petition on ground 1, including with respect to challenged claims 16-20, should be denied.

IX. CONCLUSION

For the foregoing reasons, the Board should deny institution as to ground 1.

Respectfully submitted,

Dated: November 29, 2018

By: / Robert Steinberg /

Robert Steinberg (Reg. No. 33,144)

bob.steinberg@lw.com

Jonathan M. Strang (Reg. No. 61,724)

jonathan.strang@lw.com

Matthew J. Moore (Reg. No. 42,012)

matthew.moore@lw.com

Latham & Watkins LLP

555 Eleventh Street, NW, Ste. 1000

Washington, DC 20004-1304

Telephone: 202.637.2200

Fax: 202.637.2201

Counsel for Patent Owner

Invensas Corporation

CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 7,835 words, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

Respectfully submitted,

Dated: November 29, 2018

By: / Robert Steinberg /

Robert Steinberg (Reg. No. 33,144)

bob.steinberg@lw.com

Latham & Watkins LLP

555 Eleventh Street, NW, Ste. 1000

Washington, DC 20004-1304

Telephone: 202.637.2200

Fax: 202.637.2201

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 29th day of November, 2018, a true and correct copy of the foregoing **Patent Owner's Preliminary Response** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

Brian M. Berliner (Reg. No. 34,549)
bberliner@omm.com
Ryan Yagura (Reg. No. 47,191)
ryagura@omm.com
Nicholas Whilt (Reg. No. 72,081)
nwhilt@omm.com
O'Melveny & Myers LLP
400 South Hope Street, 18th Floor
Los Angeles, CA 90071
Telephone: 213.430.6000

John Kappos (Reg. No. 37,861)
jkappos@omm.com
O'Melveny & Myers LLP
610 Newport Center Drive, 17th Floor
Newport Beach, California 92660
Telephone: 949.823.6900

Mark Liang (Reg. No. L1031)
mliang@omm.com
O'Melveny & Myers LLP
2 Embarcadero Ctr., 28th Floor
San Francisco, California 94111
Telephone: 415.984.8700
INVENSASSAMSUNGTX17670OMM@omm.com

IPR2018-01402 (USP 6,849,946)

Patent Owner's Preliminary Response

By: / Robert Steinberg /

Robert Steinberg (Reg. No. 33,144)

bob.steinberg@lw.com

Latham & Watkins LLP

555 Eleventh Street, NW, Ste. 1000

Washington, DC 20004-1304

Telephone: 202.637.2200

Fax: 202.637.2201

Counsel for Patent Owner

Invensas Corporation