

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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INTEL CORPORATION  
Petitioner

v.

GODO KAISHA IP BRIDGE 1  
Patent Owner

**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 7,800,165**

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Intel Corporation (“Intel” or “Petitioner”) respectfully requests *inter partes* review (“IPR”) of claims 13–19 (the “Challenged Claims”) of U.S. Patent No. 7,800,165 (the “’165 patent”) (Ex. 1003).

## **I. INTRODUCTION**

The ’165 patent claims a semiconductor device with a semiconductor region, such as a “fin” in a three-dimensional field effect transistor. The purportedly novel characteristic of the invention is a resistivity in the side portion of the semiconductor region that is substantially equal to or smaller than the resistivity in the upper portion. As explained in this Petition, however, the claimed device would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of alleged invention in view of the prior art. The dependent claims add nothing more than structural features that were also well known in the prior art. The Challenged Claims should therefore be cancelled.

## **II. MANDATORY NOTICES**

### **A. 37 C.F.R. § 42.8(b)(1): Real Party-in-Interest**

Intel is the real party-in-interest for Petitioner.

### **B. 37 C.F.R. § 42.8(b)(2): Related Matters**

Godo Kaisha IP Bridge 1 (“IP Bridge”) has asserted the ’165 patent in *Godo Kaisha IP Bridge 1 v. Intel Corp.*, Case No. 2:17-cv-676 (E.D. Tex. Sept. 29, 2017). That matter may affect, or be affected by, decisions in this proceeding.

In addition, the Petitioner is concurrently filing a separate IPR petition challenging additional claims of the '165 patent.

**C. Counsel Information and Service Information**

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Intel concurrently submits a Power of Attorney, 37 C.F.R. § 42.10(b), and consents to electronic service directed to the following email address: Intel\_IPBRIDGE\_IPR@kirkland.com.

**III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103**

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. § 42.15(a)(1) for this Petition to Deposit Account No. 506092. Review of seven (7)

claims is requested, so no excess claim fee is required. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition to be charged to the above deposit account.

#### **IV. CERTIFICATION OF GROUNDS FOR STANDING**

Pursuant to Rule 42.104(a), Intel certifies that the '165 patent is available for IPR and that Intel is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds in this Petition. Intel certifies: (1) Intel is not the owner of the '165 patent; (2) Intel (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '165 patent; (3) Intel files this Petition within one year of the date Intel was served with a complaint asserting infringement of the '165 patent; (4) the estoppel provisions of 35 U.S.C. § 315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '165 patent was granted.

#### **V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED**

##### **A. 37 C.F.R. § 42.104(b)(1): Claims for Which IPR Is Requested**

Petitioner challenges claims 13–19 of the '165 patent.

##### **B. 37 C.F.R. § 42.104(b)(2): Grounds for Challenge**

The Challenged Claims are unpatentable based on the following:

1. U.S. Patent No. 7,494,862 (“Doyle ’862”) (Ex. 1005); effective filing date September 29, 2006, issued February 24, 2009, prior art under § 102(e).
2. U.S. Patent No. 7,323,389 (“Goktepli”) (Ex. 1006); filed July 27, 2005, issued January 29, 2008, prior art under § 102(e).

3. U.S. Patent Pub. No. 2004/0036126 (“Chau”) (Ex. 1008); filed August 23, 2002, published February 26, 2004, prior art under § 102(b).

Intel requests IPR on the following grounds:

Ground	Claims	Proposed Statutory Rejection
1	13–14, 16–19	Obvious under § 103 in view of the combination of Doyle ’862 with Chau
2	13–19	Obvious under § 103 in view of the combination of Goktepli with Chau

Ground 2 is not cumulative of Ground 1 because Doyle ’862 and Goktepli disclose different methods for uniformly doping a semiconductor device, such as a FinFET. Doyle ’862 discloses doping by vertical implantation into the upper region of the fin, and selectively modifying the upper region to prevent any additional implantation during subsequent angled implantation into the side regions of the fin. (*See* Section IX.A.) Goktepli, on the other hand, discloses doping by diffusion. A sacrificial doping layer is formed around the source-drain regions and source-drain extension regions, following which dopants diffuse into the upper and side regions of the fin simultaneously. (*See* Section IX.B.)

### **C. 37 C.F.R. § 42.104(b)(3): Claim Construction**

*See* Section VIII.



#### **D. 37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable**

A detailed explanation of how the Challenged Claims are unpatentable is provided below in Section X.

#### **E. 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge**

A table of exhibits is provided at the end of this Petition. The relevance of this evidence and the specific portions supporting the challenge is provided below in Section X. Intel also submits the Declaration of Dr. Stanley Shanfield (Ex. 1001) in support of this Petition under 37 C.F.R. § 1.68.

### **VI. BRIEF DESCRIPTION OF TECHNOLOGY**

The '165 patent's claimed invention is directed to three-dimensional transistor structures having a resistivity in a "side portion" that is substantially equal to or smaller than the resistivity of an "upper portion." (Ex. 1003 at 1:12–16.)

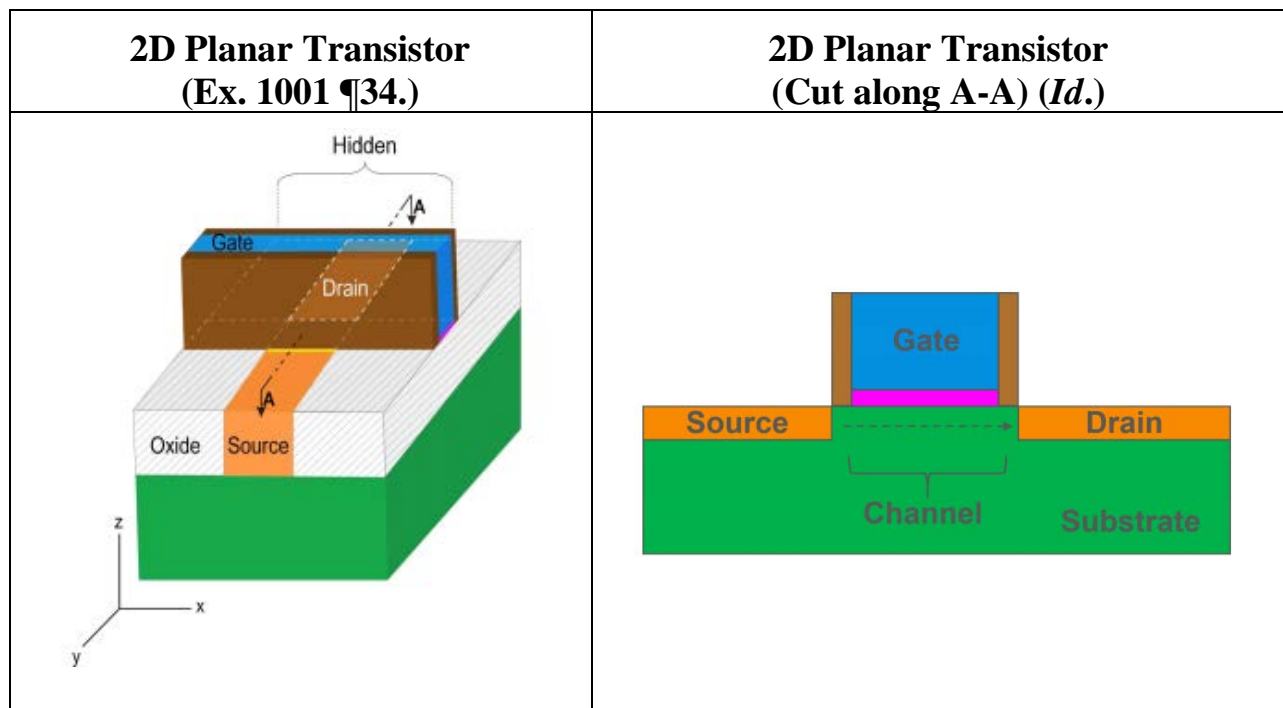
#### **A. Overview of Transistor Structures**

Integrated circuit devices—such as microprocessors and computer memory—typically include hundreds of millions of transistors. Transistors act as switches that, when turned "on," conduct electrical signals that can represent data. When many transistors are electrically connected, they can form complex logic that is used for computer data processing. (Ex. 1001 ¶33.)

##### **1. 2D Transistors**

Two-dimensional ("2D"), or "planar," transistors have been widely used since the 1960s. As shown in the figure below, 2D transistors typically have three

regions—a “**source**,” a “**drain**,” and a “**gate**.”<sup>1</sup> The **source** and **drain** regions are formed in a substrate—which can be formed of silicon—or in silicon on an insulator (“SOI”) sitting above the **substrate**. The region between the **source** and **drain** is the “channel.” When the channel region is turned “on,” current flows from the **source** to **drain** region. (Ex. 1001 ¶34.)



As shown above, the **gate** controls the flow of electrical current through the channel, between the **source** and **drain**. When a voltage is applied to the **gate**, the transistor turns “on,” allowing current to flow between the **source** and the **drain**.

<sup>1</sup> This is true of metal-oxide-semiconductor field-effect transistors (“MOSFETs”).

When the voltage is removed from the **gate**, the transistor turns “off,” impeding the flow of current between the **source** and the **drain**. (Ex. 1001 ¶35.)

## **2. 3D Transistors**

In 1975, the co-founder of Intel, Gordon E. Moore, set forth “Moore’s Law,” which predicts that the number of transistors in integrated circuits will double approximately every two years. For over four decades, Intel has developed new technologies that followed Dr. Moore’s prediction. One of the most significant of those technological advances was the development of three-dimensional (“3D”) transistor structures, which Intel was the first to commercialize. Such 3D transistors are called “Tri-Gate” transistors or “FinFETs” (for Fin Field Effect Transistors).<sup>2</sup> (Ex. 1001 ¶¶36–37.)

The benefit of a FinFET structure is that it allows transistors to be packed together more closely on a substrate. In a 2D, planar transistor, the **source**, **drain**, and channel regions are formed in a semiconductor **substrate**. The **gate** interacts with the channel primarily along a single surface. By contrast, in a 3D, FinFET

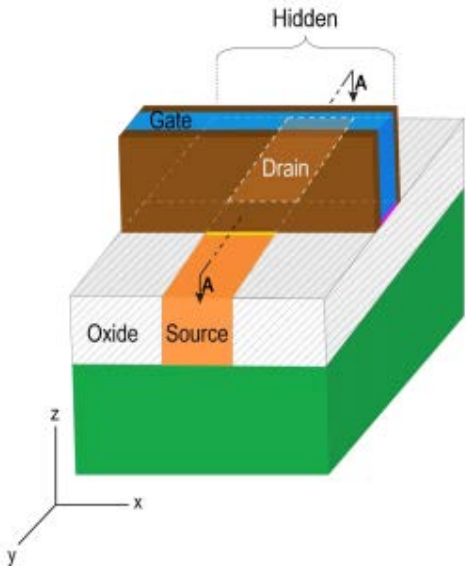
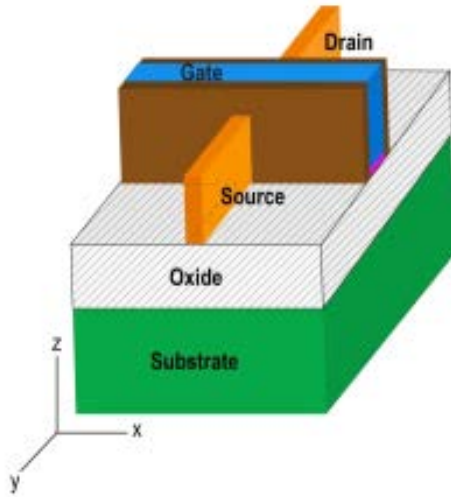
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<sup>2</sup> Although differences between Tri-Gate transistors and FinFETs exist, Petitioner will address both as “FinFETs” for purposes of this Petition. Petitioner reserves the right to address the distinction, should the Patent Owner raise an argument that requires so.

structure, the **source**, **drain**, and channel regions are formed on the surface of the **substrate** in a “**fin**” shape. The **gate** wraps around and interacts with the channel along three surfaces, *i.e.*, the upper and side surfaces of the **fin**, as illustrated below. (Ex. 1005 at 1:20–22 (“These three separate **gates** provide three separate channels for electrical signals to travel, thus effectively tripling<sup>3</sup> the conductivity as compared to a conventional planar transistor.”).) This structure yields improved performance, reduced current leakage, and reduced transistor size in the lateral (x-axis) dimension, due to the longer effective length of contact between the upper and side regions of the elevated **fin** and **gate**. (Ex. 1001 ¶37.)


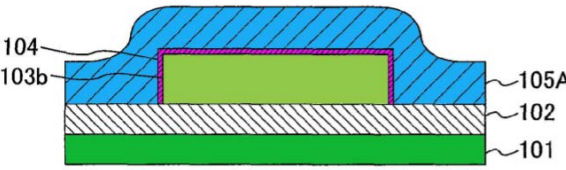
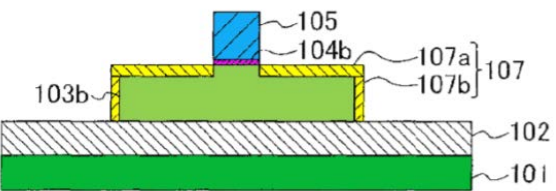
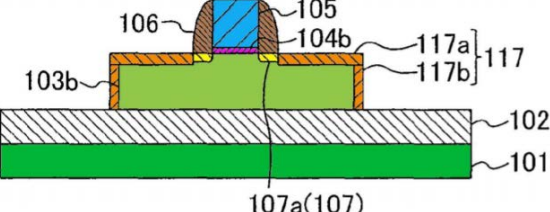
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<sup>3</sup> If the upper and side regions of the fin are not equal in length, the conductivity will be increased, but not necessarily tripled.

2D Planar Transistor (Ex. 1001 ¶37.)	3D FinFET ( <i>Id.</i> )
	

### 3. 3D Transistor Fabrication

The '165 patent's Admitted Prior Art ("APA") describes a known method for fabricating a FinFET. (Ex. 1003 at Figs. 16A–16D, 17A–17D.) First, a **fin 103b** is formed on a **substrate 101**. (*Id.* at Fig. 17A.) Second, a **gate insulating film 104** and a **polysilicon film 105a**, are formed on the **fin**. (*Id.* at Fig. 17B.) Third, the **gate insulating film 104** and **polysilicon film 105a** are etched away, leaving a gate comprised of a **gate insulating film 104** and a **gate electrode 105**. (*Id.* at Fig. 17C.) The **fin 103b** is implanted to form the **extension regions 107**. Finally, an insulating film is formed and then etched back to form insulative **sidewall spacers 106** before the exposed portions of **fin 103b** are ion implanted to form the **source/drain regions 117**. (*Id.* at Fig. 17D.) (Ex. 1001 ¶38.)

<p align="center"><b>APA Figure 17A</b> (Ex. 1003 at Fig. 17A (annotated))</p>	<p align="center"><b>APA Figure 17B</b> (Id. at Fig. 17B (annotated))</p>
	
<p align="center"><b>APA Figure 17C</b> (Id. at Fig. 17C (annotated))</p>	<p align="center"><b>APA Figure 17D</b> (Id. at Fig. 17D (annotated))</p>
	

The final, ion-implantation step referred to in the APA increases the electrical conductivity of the **source** and **drain portions** of the **fin**. As the APA notes, the **fin** is made of a semiconducting material, such as silicon. (Ex. 1003 at 2:18–20.) Ions—referred to as “impurities” or “dopants”—are implanted into **silicon fin**. Following implantation, the manufacturer anneals, or heats to a high temperature, the implanted ions to activate them, thereby forming “doped” or “impurity” regions within the semiconducting material. Higher implantation doses of dopants lead to higher conductivity and lower resistivity—because conductivity and resistivity are inversely related. (Ex. 1001 ¶39).

#### 4. PMOS and NMOS Transistor Types

There are two types of MOS transistors: PMOS and NMOS. Both types are typically used in “complementary pair” logic in integrated circuit design because they allow a logic state to be maintained with almost zero power consumption. This low-power feature enables more efficient products to be created. (Ex. 1001 ¶40.)

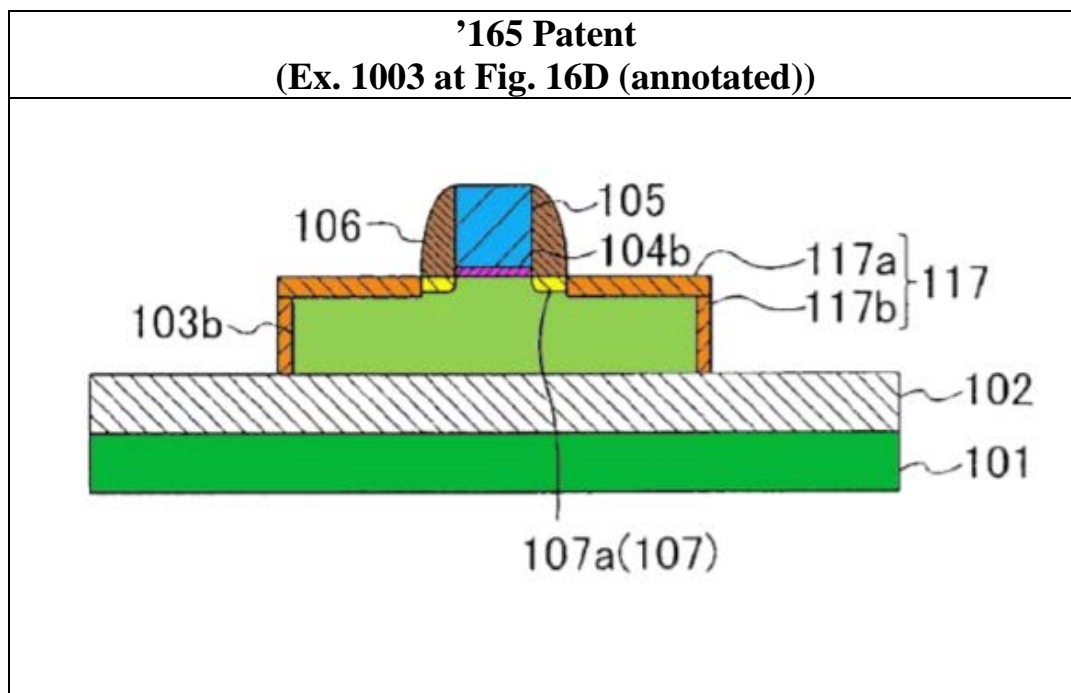
Two types of dopants are used to form the **source/drain regions** in PMOS and NMOS transistors: “N-type” and “P-type.” An “N-type” dopant has more electrons than the host lattice, resulting in a net negative charge. A “P-type” dopant has less electrons than the host lattice, resulting in a net positive charge. The impurity type used as a dopant determines the “conductivity type” of the impurity region in the **source/drain regions**. This, in conjunction with the conductivity type of the channel, determines the “conductivity type” of the overall transistor, *i.e.*, a PMOS or NMOS transistor. (Ex. 1001 ¶¶41, 42.)

“Bulk” doping is commonly used in FinFET manufacturing as a way to set the doping type of the channel region. First, a **fin** is “bulk” doped with the opposite dopant type as the overall transistor.<sup>4</sup> For example, to form a PMOS transistor, a **silicon fin** is created on the **substrate**, and then the **fin** is “bulk doped” with N-type impurities. A **gate structure** is formed over the channel region of the **fin**, followed

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<sup>4</sup> An already-doped **substrate** can be provided by the wafer manufacturer.

by doping the rest of the **fin** with P-type dopants, which forms the **extension regions** in alignment with the **gate** sidewalls. The **sidewall spacers** are formed, following which the exposed portions of the **fin** receive additional P-type dopants, forming the **source** and **drain regions**. (See, e.g., Ex. 1003 at Fig. 16D (showing **extension regions** 107).) The **extension regions** prevent so-called “short-channel effects,” which degrade the operating characteristics of the transistor. The implants are then annealed to activate all the implanted dopants. (Ex. 1001 ¶¶43, 44.)



All of the structures and concepts described above were well known in the art before the effective priority date of the '165 patent. (Ex. 1001 ¶45.)

## **5. Transistor Properties**

There are several ways to measure the resistivity of a doped region in a transistor, all of which were well-known before the '165 patent. For example, a



POSITA could have measured “the sheet resistance, the resistivity, or the spreading resistance” of the impurity region. (Ex. 1003 at 3:66–67.) Sheet resistance is a common measure of resistivity of thin films and is calculated as the resistivity divided by the thickness of the material. (*Id.* at 4:3–5.) Resistivity “is a specific resistance” that quantifies how strongly a material opposes the flow of electric current. (*Id.* at 4:4.) Spreading resistance is the resistance between any two points in or on a layer of material. Sheet resistance and spreading resistance are always proportional to resistivity. (*Id.* at 4:3–11; *see also* Schroder, Dieter K., *Semiconductor Material and Device Characterization* (3d Ed. 2006) (“Schroder”) (Ex. 1009) at 23, 43–44.) (Ex. 1001 ¶46.)

## **B. Overview of the ’165 Patent**

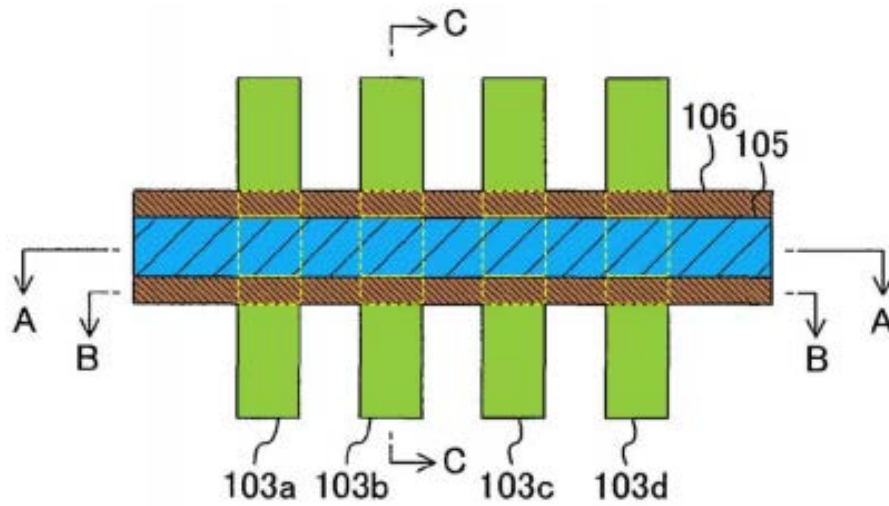
The ’165 patent issued from U.S. Patent Application No. 12/025,504, which was filed on February 4, 2008, as a continuation of PCT/JP2008/050253, filed on January 11, 2008, which claims priority to a Japanese patent application JP 2007-011572, filed on January 22, 2007. (Ex. 1003 at Cover.) (Ex. 1001 ¶47.)

The ’165 patent claims a semiconductor device with side and upper portions (*e.g.*, in a **fin**) in which the **side** portion has a resistivity that is equal to or smaller than the resistivity of the **upper** portion. (Ex. 1003 at 9:19–23.) Equal resistivity in, for example, the **source/drain regions** of a FinFET, allows for optimum operation of the transistor. (Ex. 1001 ¶¶48, 49.)

## **1. Admitted Prior Art (“APA”)**

The '165 patent admits that most of the claimed FinFET structures were well known in the prior art. Specifically, the APA discloses the following structural features of FinFETs, as illustrated below: a **plurality of semiconductor regions** (103a–103d), each having an **impurity region** formed in the upper surface (107a) and side surfaces (107b), a **gate dielectric** (104a–104d) formed on each of a **plurality of semiconductor regions**, a **gate electrode** (105) spanning across the **plurality of semiconductor regions**, insulative **sidewall spacer** (106), and **extension regions** (107). (Ex. 1003 at 1:36–2:5, Figs. 16A–D.) (Ex. 1001 ¶¶50–55.)

APA  
(Ex. 1003 at Fig. 16A (annotated))



APA  
(Id. at Fig. 16B (annotated))

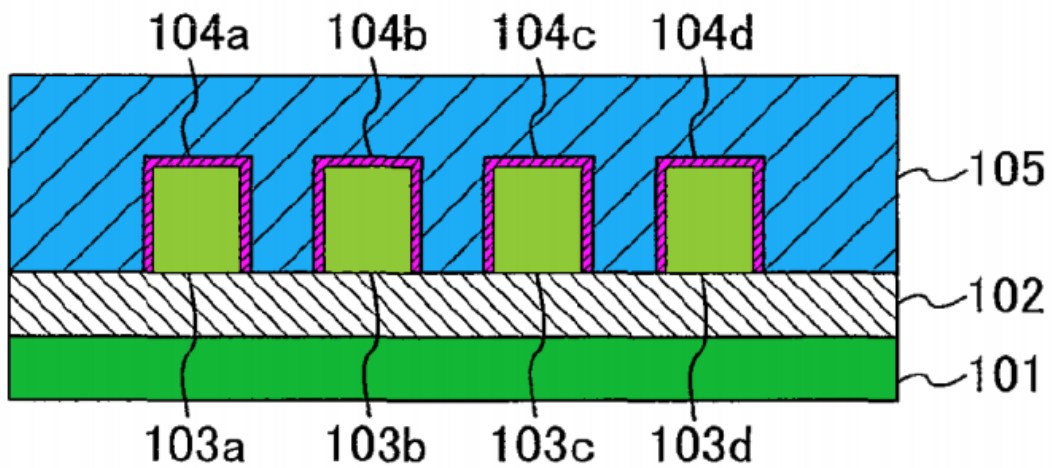


FIG. 16B  
PRIOR ART

APA  
(Ex. 1003 at Fig. 16C (annotated))

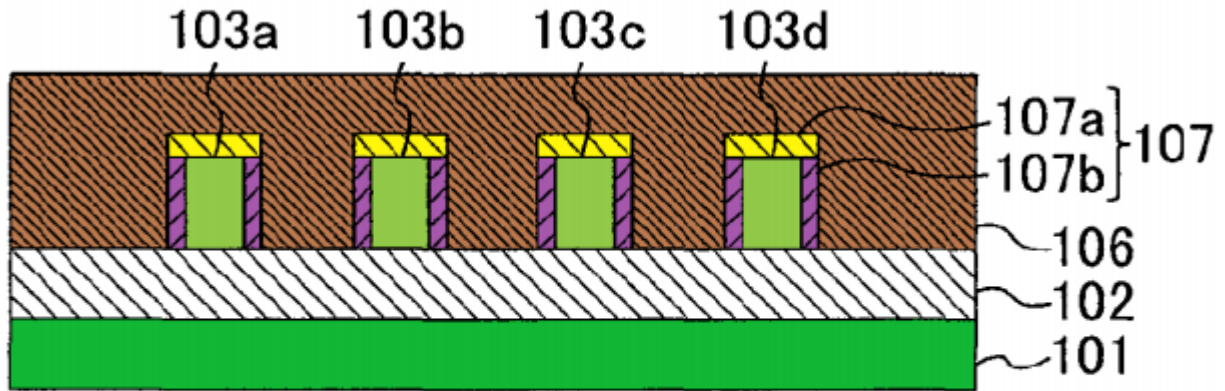
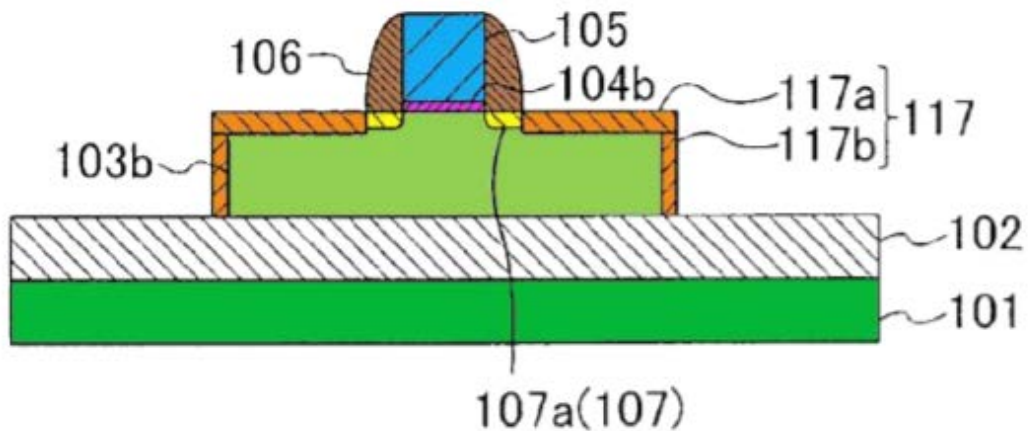


FIG. 16C  
PRIOR ART

APA  
(*Id.* at Fig. 16D (annotated))



The '165 patent likewise admits that the steps to manufacture a FinFET were known in the APA. (Ex. 1003 at 2:6–41, Figs. 17A–D; *see also* Section VI.A.3.) (Ex. 1001 ¶¶56, 57.)

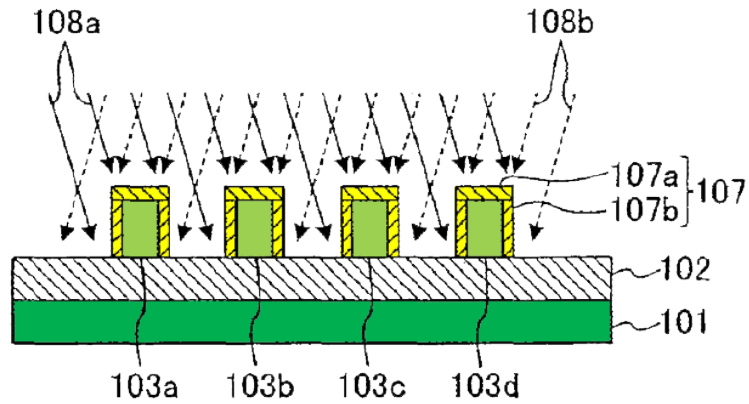
## 2. Alleged Problem

The '165 patent notes that prior-art doping techniques introduce impurities predominantly from *above* the **fin**, resulting in a greater amount and penetration of dopants at the *top* surface of the **fins** (107a) than on the *side* surfaces of the **fins** (107b). (Ex. 1003 at 3:19–64.) (Ex. 1001 ¶58.)

**APA**  
(Ex. 1003 at Fig. 18A (annotated))

**FIG. 18A**

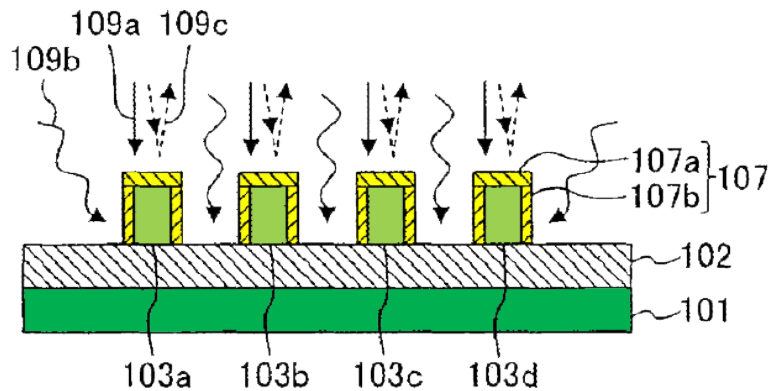
PRIOR ART



**APA**  
(*Id.* at Fig. 18B (annotated))

**FIG. 18B**

PRIOR ART



For example, Figure 18A shows ion implantation at two different angles, resulting in up to twice the dopants implanted in the top surface as in the side. (Ex. 1001 ¶¶58, 59.) Figure 18B similarly shows a plasma doping method described in the APA in which the top surface is doped by implanted ions 109a, adsorbed ions

109b, and desorbed ions 109c (which are desorbed by sputtering). The side surface is doped primarily by adsorbed ions 109b. As a result, the implantation dose of the top surface is approximately 25% higher than that of the side surface. (Ex. 1003 at 3:38–64.) Both prior-art approaches thus purportedly yield uneven distribution of dopants, with more on the top region as compared to the side regions. (Ex. 1001 ¶59.)

According to the '165 patent, uneven distribution is undesirable because the top region will become relatively more conductive. In other words, certain electrical resistance characteristics—"sheet resistance," "resistivity," and "spreading resistance"—will be lower in the top region than in the side regions, producing non-optimum current flow through the top regions of the **fins**, as compared to the side regions of the **fins**. (Ex. 1003 at 4:26–42; 3:57–4:42.) (Ex. 1001 ¶60.)

The '165 patent explains that such a disparity in resistivity in three regions (*i.e.*, the upper and side surfaces of the **fin**) results in "degradation in the transistor characteristics (e.g., drain current)." (Ex. 1003 at 12:39–40.) (Ex. 1001 ¶¶61, 62.)

### **3. Summary of Alleged Invention of the '165 Patent**

Representative claim 1 of the '165 patent recites:

1. A semiconductor device, comprising:  
[a] a **first semiconductor region** of a first conductivity type formed on a **substrate** and having an upper surface and a side surface;

- [b] a **first impurity region** of a second conductivity type formed in *an upper portion* of the **first semiconductor region** and made of a semiconductor; and
- [c] a **second impurity region** of a second conductivity type formed in *a side portion* of the **first semiconductor region** and made of a semiconductor, wherein
- [d] a resistivity of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.

The '165 patent's *only* alleged point of novelty is reflected in the final limitation, which claims impurity regions in the sides of the **fins** with a resistivity *equal to or smaller than* that in the top of the **fin**.

'165 Patent (Claimed Invention) (Ex. 1003 at Fig. 2E (annotated))	'165 Patent (APA) (Id. at Fig. 17D (annotated))

According to the '165 patent, this resistivity ratio leads to optimal transistor performance. (Ex. 1003 at 4:43–64). But it was already well known that non-uniform doping could lead to degraded transistor performance. (Ex. 1001 ¶¶63, 64.)



There was nothing novel or inventive about a uniformly-doped FinFET. Long before the '165 patent's priority date, a POSITA would have known that it was optimal to uniformly dope the top and side regions of **fins** in a FinFET to obtain the best FinFET performance. As more fully described herein, Doyle '862 in combination with Chau, or Goktepli in combination with Chau, renders obvious the allegedly novel features of the Challenged Claims. (*Id.* ¶64.)

### **C. Prosecution History**

The Applicant initially filed 33 claims, drawn to two groups: (1) a semiconductor device, and (2) a method of manufacturing a semiconductor device. The Examiner issued a restriction requirement, so Applicant elected to prosecute the claims drawn to the semiconductor device. (U.S. Patent No. 7,800,165 File History (Ex. 1004) at 260.) This is notable because the Applicant chose to focus prosecution on minor structural attributes that allegedly improved upon the prior art considered by the Examiner.<sup>5</sup> (Ex. 1001 ¶¶65, 66.)

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<sup>5</sup> This Petition relies on art that was **not** considered by the Examiner and that teaches not only the allegedly novel “uniform doping” aspect of the purported invention, but also the structural differences on which the Applicant relied during prosecution.

## **VII. LEVEL OF ORDINARY SKILL IN THE ART**

A POSITA at the time of the alleged invention would have had at least a B.S. degree in electrical engineering or materials science (or equivalent experience) and would have had two or three years of experience with integrated circuit processing, manufacturing, and device design. This was the typical level of experience of persons working with processes for manufacturing semiconductor device structures at the time of the alleged invention. (Ex. 1001 ¶¶67, 68.)

## **VIII. CLAIM CONSTRUCTION**

A claim in an IPR is currently given the broadest reasonable interpretation in light of the specification to one having ordinary skill in the art. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2133 (2016). However, the USPTO has proposed “to replace the broadest reasonable interpretation (‘BRI’) standard for construing unexpired patent claims and proposed claims in [IPR] trial proceedings with a standard that is the same as the standard applied in federal district courts and International Trade Commission (‘ITC’) proceedings.” *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 21,221 (May 9, 2018) (to be codified at 37 C.F.R. pt. 42). (Ex. 1001 ¶¶69.)

Federal district courts construe patent claims in accordance with the principles that the United States Court of Appeals for the Federal Circuit articulated in *Phillips*

*v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Under the *Philips* standard, claim terms are generally given their “ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1312–13. (Ex. 1001 ¶69.)

In the co-pending district court litigation, neither party has proposed constructions for any claim terms in the ’165 patent. Petitioner likewise does not propose any claim construction in this Petition for at least the reason that Petitioner believes the Challenged Claims are invalid under either claim-construction standard. If IP Bridge hereafter proposes constructions in the co-pending litigation, however, Petitioner reserves the right to request additional briefing in connection with this Petition.

## **IX. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES**

There is nothing novel or inventive in any of the Challenged Claims. Doping the surfaces of a semiconductor fin to ensure that the resistivity of the “side portion” is “substantially equal to or smaller than that of” the “upper portion” was well known before the priority date of the ’165 patent. (Ex. 1001 ¶70.)

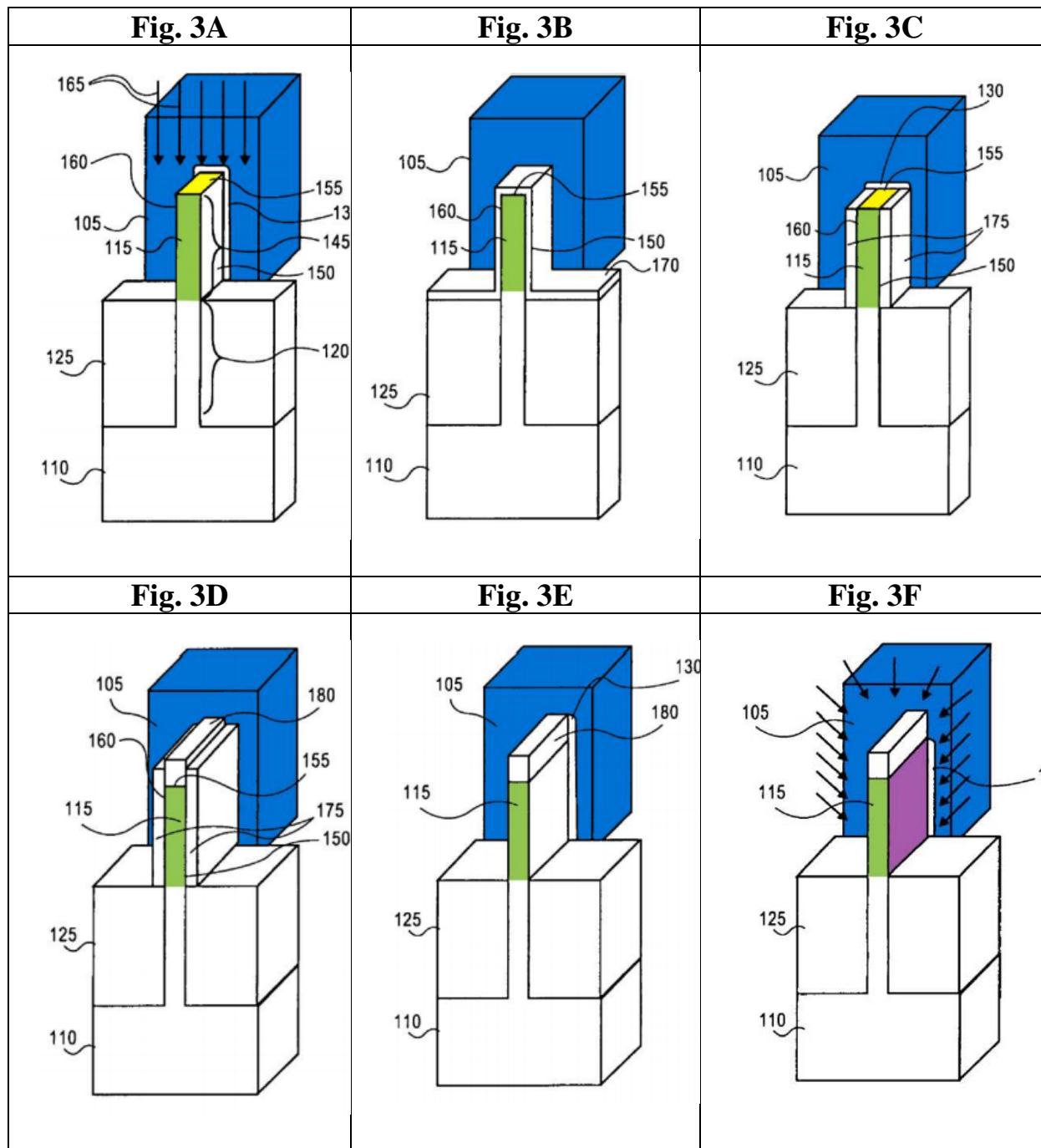
### **A. Overview of Doyle ’862**

Doyle ’862 was not considered during prosecution of the ’165 patent. It teaches a method for “uniform doping of non-planar transistor structures,” such as FinFETs. (Ex. 1005 at Title.) Using this method, ions can be implanted to a uniform

depth on the top and sides of the **fin**s, resulting in “a functional transistor, [with] current flowing, or ‘wrapping around’” in a “uniform [manner] which results in a more efficient transistor.” (*Id.* at 4:20–23.) (Ex. 1001 ¶¶71, 72.)

Figures 3A–3F illustrate Doyle ’862’s uniform doping process following formation of a **silicon fin** and **gate electrode**. In Figure 3A, a **first impurity region** is formed in the upper surface of the **silicon fin** via vertical implantation. A conformal layer 170 is then deposited on all sides of the **silicon fin** before being etched (or removed) from the upper surfaces (Figs. 3B, 3C). Next, the top surface is selectively modified, such as by re-oxidation (Fig. 3D). Then the conformal layer deposited on the sides of **silicon fin** is removed by isotropic etching (Figure 3E) before a **second impurity region** is formed in the side surfaces of the **silicon fin** via angled ion implantation, resulting in uniform doping. (Ex. 1005 at 3:9–31.) (Ex. 1001 ¶¶73–79.)

**Doyle '862**  
(Ex. 1005 Figures (annotated))



## B. Overview of Goktepli

Goktepli was not considered during prosecution of the '165 patent. It teaches a “Method of Forming a FinFET Structure,” (Ex. 1006 at Title), and discloses:

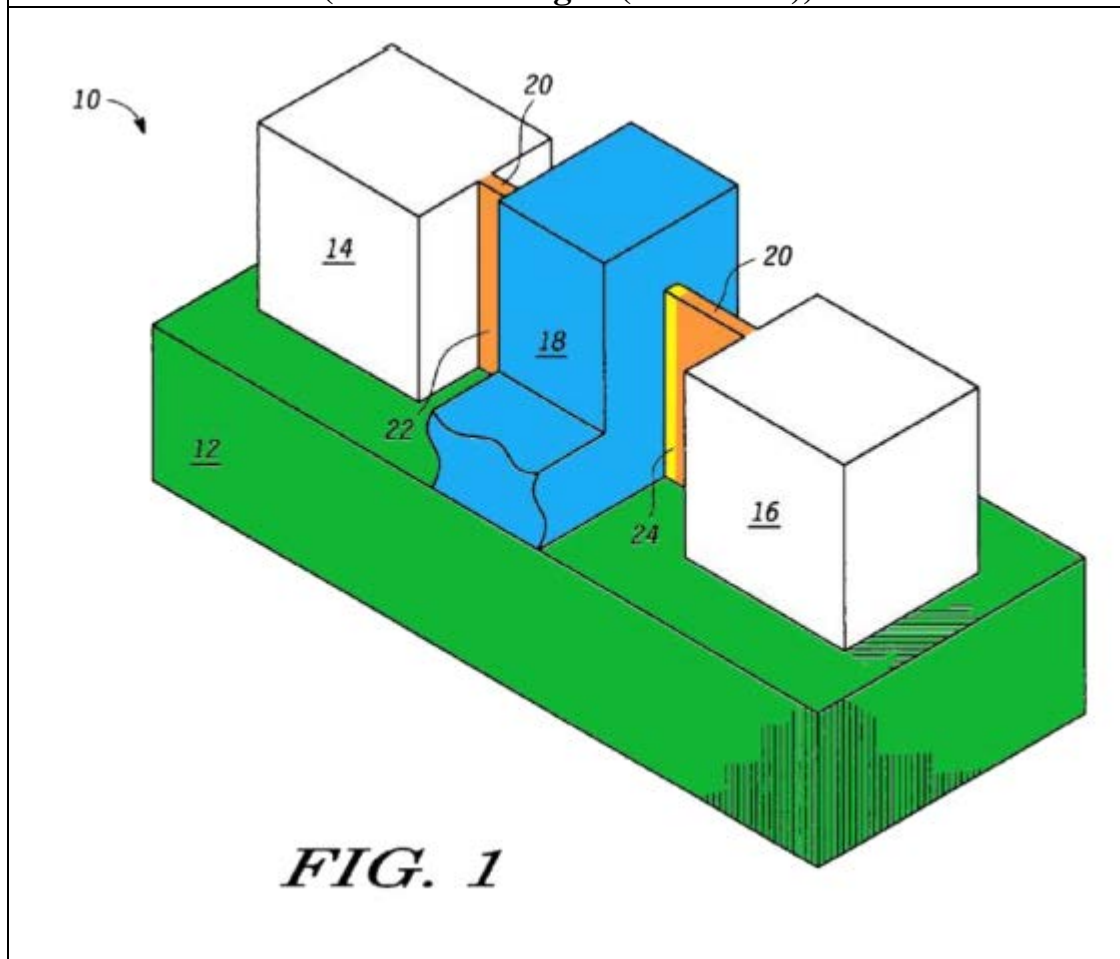
A semiconductor device (10) such as a FinFET transistor of small dimensions is formed in a process that permits *substantially uniform ion implanting* (32) of a source (14) electrode and a drain (16) electrode adjacent to an intervening **gate** (18) and channel (23) connected via **source/drain extensions** (22, 24) which form a **fin**.

(*Id.* at Abstract.) According to Goktepli, as transistors become smaller, they “have difficulty in maintaining high drive current with low leakage while not demonstrating short-channel effects such as leakage and threshold voltage stability.”

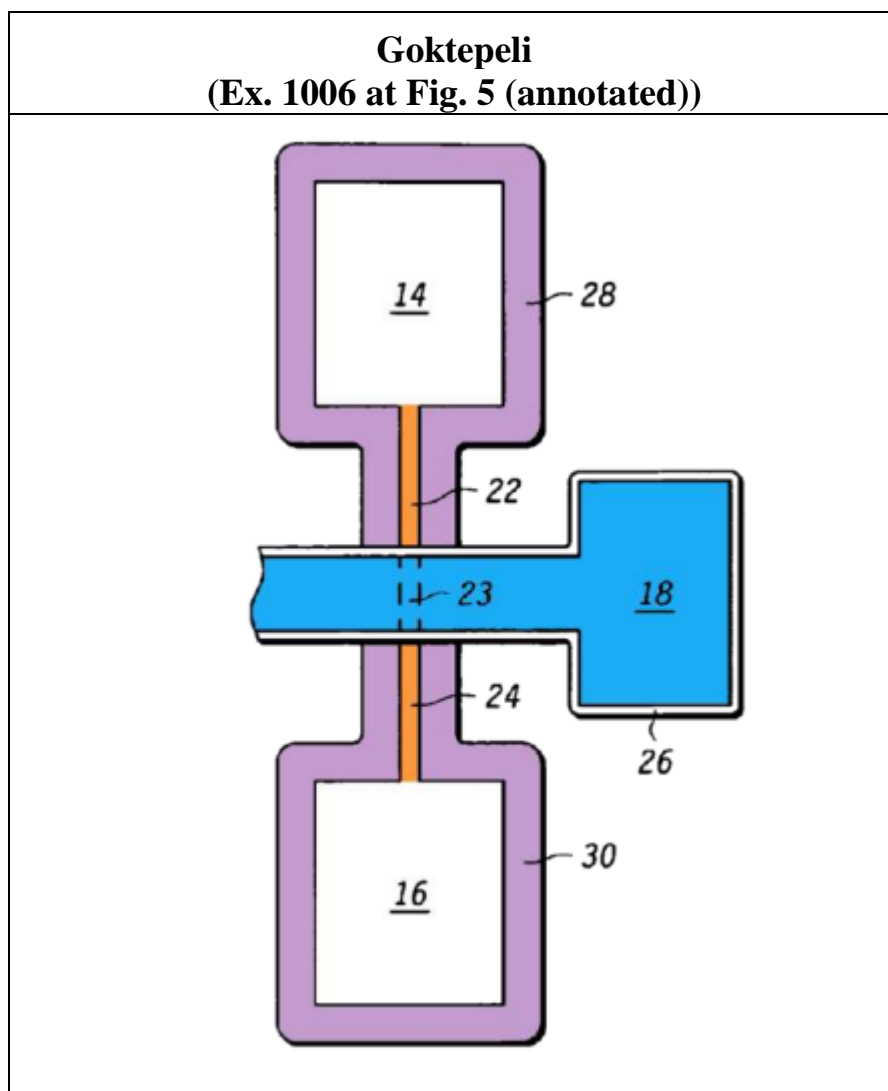
(*Id.* at 1:19–22.) Goktepli further identifies the specific problems associated with doping of the **source/drain regions** and **source/drain extension regions** by ion implantation: “ion implantation of the **source** and **drain regions** may cause significant damage to the **extension region** since is it [sic] thin and subject to full penetration by implanted ions.” (*Id.* at 1:63–65.) (Ex. 1001 ¶¶81, 82.)

Goktepli discloses a method for resolving these problems by doping the **source/drain regions** and **source/drain extension regions**. First, “a semiconductor device 10 comprising a **substrate** 12, a conformal layer on the **substrate** 12 which is patterned to form source/drain contact regions 14 and 16 and a **fin** 20 which forms **extension regions** 22 and 24, and a **gate feature** 18.” (Ex. 1006 at 3:12–16.) (Ex. 1001 ¶84.)

**Goktepel**  
**(Ex. 1006 at Fig. 1 (annotated))**



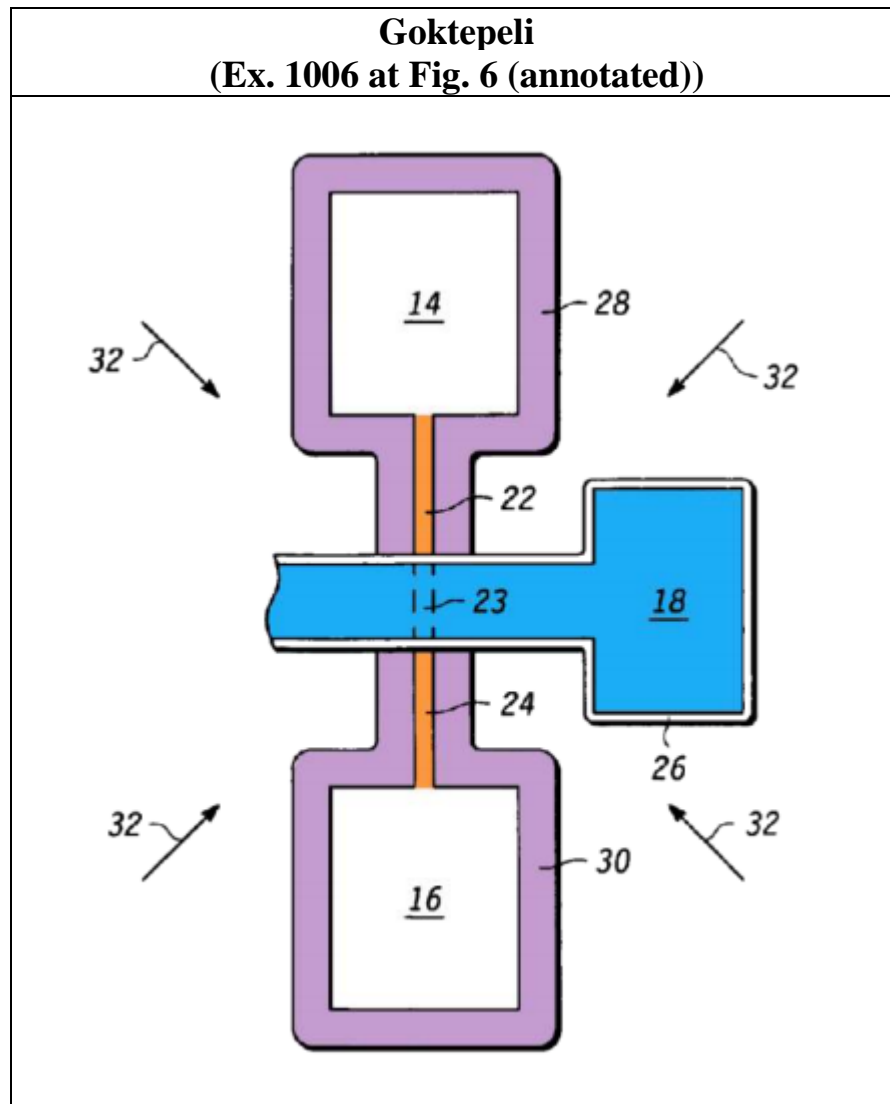
Second, following the formation of these elements, a dielectric material 26 is applied to “all exposed outside surfaces of the source/drain contact regions 14 and 16, the **extension regions** 22 and 24 and the **gate feature** 18.” (Ex. 1006 at 3:56–59.) The “**sacrificial doping layers** 28 and 30” are formed around source/drain contact regions and **source/drain extension regions**, such as by selective epitaxial growth. (*Id.* at 4:7–14.) (Ex. 1001 ¶85.)



Goktepel discloses several methods for doping the **source/drain regions** and **source/drain extension regions** via the **sacrificial doping layers** 28 and 30. It discloses in-situ doping. (Ex. 1006 at 4:28–31 (“As one form of implementing semiconductor device 10, **sacrificial doping layers** 28 and 30 are in-situ doped with source/drain dopants in the growth process to have a desired conductivity of predetermined strength.”).) It also discloses angled ion implantation 32, performed on the **sacrificial doping layers**. (*Id.* at 4:33–38 (“semiconductor device 10 is



exposed to angle implants 32 to place source/drain dopants into **sacrificial doping layers** 28 and 30”). (Ex. 1001 ¶¶86–88.)



Following doping either by diffusion or angled implantation, the dopants are annealed. This “heating of semiconductor device 10 causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and thoroughly diffuse into source/drain contact regions 14 and 16.” (Ex. 1006 at 4:57–60.) The **sacrificial doping layers** are then removed. (*Id.* at 5:12–15.) (Ex. 1001 ¶89.)

### C. Overview of Chau

Chau was not considered during prosecution of the '165 patent. It teaches “a tri-gate fully depleted substrate transistor and its methods of fabrication,” (Ex. 1008 ¶2), and explains:

The tri-gate transistor includes a **thin semiconductor body** formed on a[] **substrate**, the **substrate** can be an insulating **subst[r]ate** or a semiconductor **substrate**. A **gate dielectric** is formed on the top surface and the sidewalls of the **semiconductor body**. A **gate electrode** is formed on the **gate dielectric** on the top surface of the **semiconductor body** and is formed adjacent to the **gate dielectric** formed on the sidewalls of the **semiconductor body**. **Source** and **drain regions** are formed in the **semiconductor body** on opposite sides of the **gate electrode**.

(Ex. 1008 ¶16.) (Ex. 1001 ¶¶99, 100.) Importantly, Chau also notes that “[s]**ource region** 330 and **drain region** 332 can be formed of *uniform concentration* or can include subregions of different concentrations or doping profiles such as **tip regions** (e.g., **source/drain extensions**”).” (*Id.* ¶23.) (Ex. 1001 ¶¶101.) These structural features are shown in Figure 3 below.

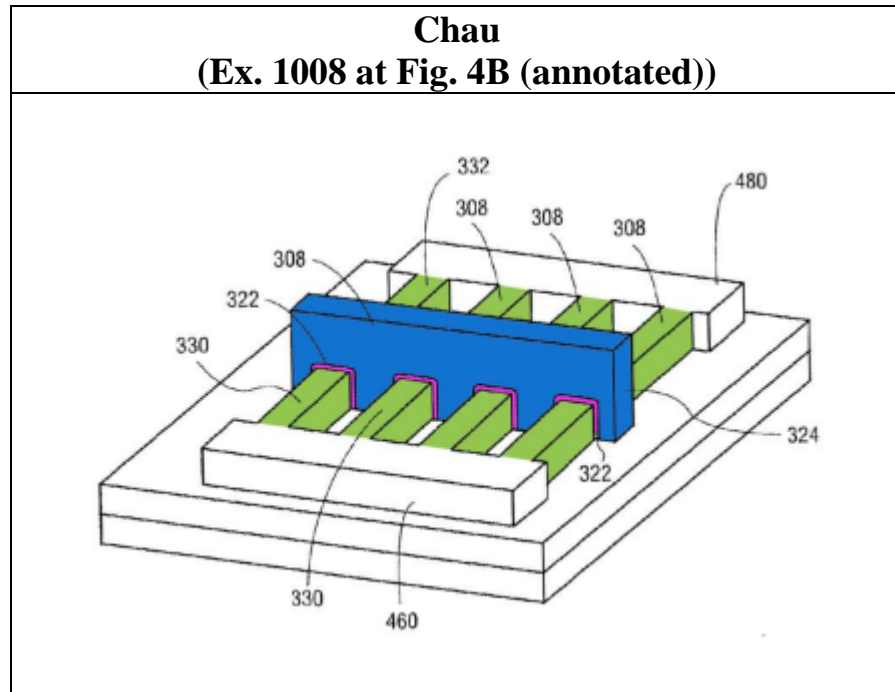
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Chau additionally teaches a tri-gate transistor with a **plurality of fins**, as illustrated in Figure 4B:

In order to fabricate the transistors with larger gate widths, transistor 300 can include an additional or multiple **semiconductor bodies** or **fingers** 308 as shown in FIG. 4B. Each **semiconductor body** 308 has a **gate dielectric layer** 322 formed on its top surface and sidewalls as shown in FIG. 4B. **Gate electrode** 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308. Each **semiconductor body** 308 also includes a **source region** 330 and a **drain region**

332 formed in the **semiconductor body** 308 on opposite sides of **gate electrode** 324 as shown in FIG. 4B.

(Ex. 1008 ¶31.) (Ex. 1001 ¶102.)



## **X. SPECIFIC GROUNDS FOR PETITION**

Intel demonstrates below how the prior art renders obvious each and every limitation of the Challenged Claims. Secondary considerations do not support a finding of nonobviousness. (Ex. 1001 ¶30.) Should IP Bridge submit alleged evidence relating to secondary considerations, Intel will respond.

**A. Ground 1: Claims 13–14, 16–19 Are Obvious in View of Doyle ’862 in Combination with Chau**

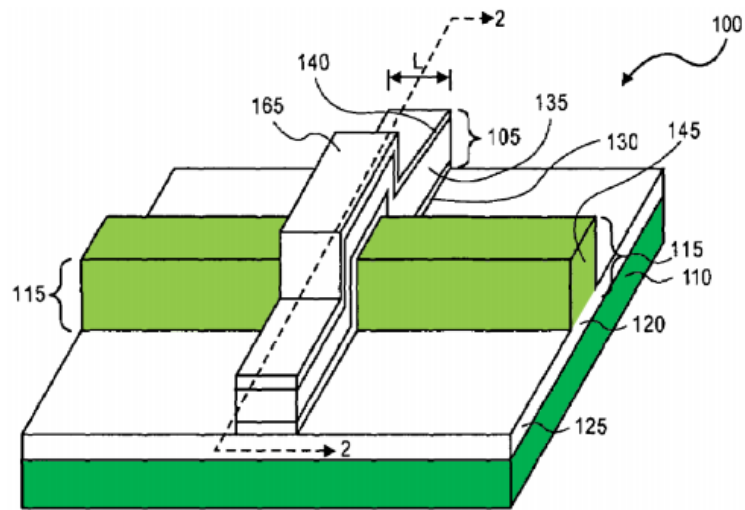
**1. Independent Claim 13**

*a. 13[preamble]–[a]: “A semiconductor device, comprising:*

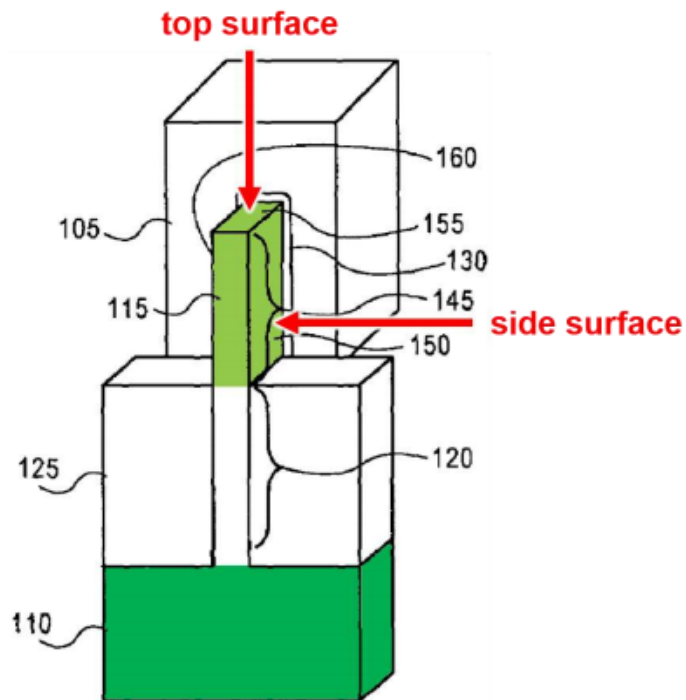
*a plurality of semiconductor regions of a first conductivity type formed on a substrate and each having an upper surface and a side surface”*

Doyle ’862 in combination with Chau renders obvious a plurality of semiconductor regions of a first conductivity type formed on a substrate, each having an upper and side surface. A single semiconductor region, *i.e.*, a silicon fin, is formed on a substrate, having an upper and a side surface, as illustrated in Figures 1 and 2. (Ex. 1005 at 1:12–14 (“thin semiconductor body (e.g., a silicon fin) formed on a substrate and having a top surface and two sidewall surfaces perpendicular to the top surface”); *see also id.* at 2:23–25 (“Silicon fin 115 is in a different plane relative to substrate 110”); *see also id.* at Fig. 1.) (Ex. 1001 ¶199.)

**Doyle '862**  
**(Ex. 1005 at Fig. 1 (annotated))**



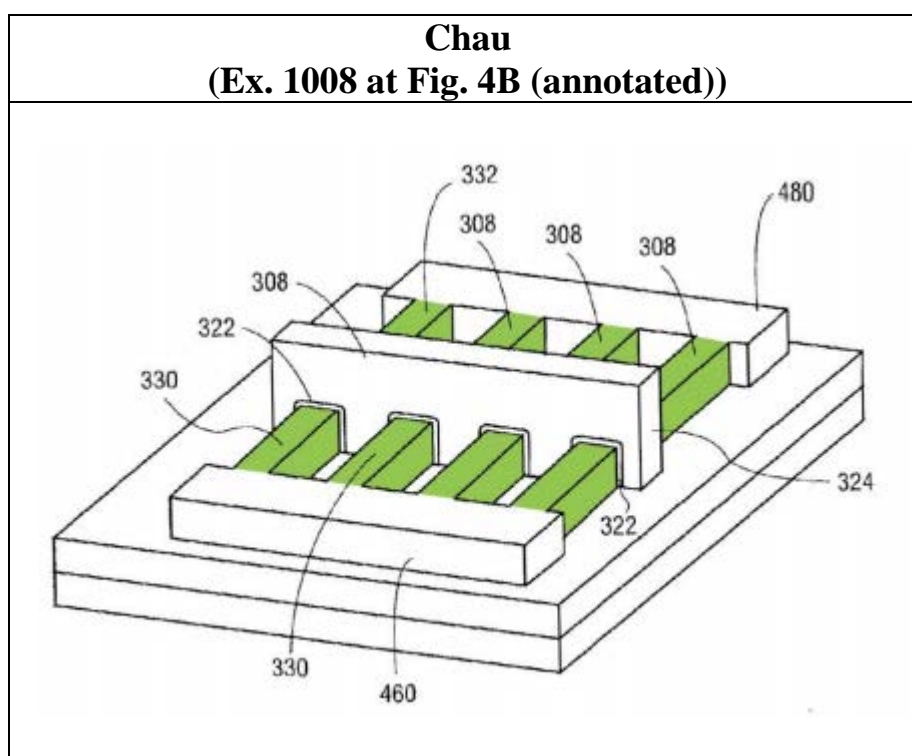
**Doyle '862**  
**(Id. at Fig. 2 (annotated))**



Doyle '862 renders obvious that the **fin** is of a first conductivity type. Later doping of the **source-drain regions** is with either P-type or N-type impurities. (Ex. 1005 at 3:2–6) (“For PMOS transistor devices, the **source** and **drain region** are typically doped with p-type impurities [and] NMOS transistor devices . . . are typically doped with n-type impurities.”).) A POSITA would have known that *before* doping the **source-drain regions** with P-type or N-type impurities, the **silicon fin** would first be bulk doped with the *opposite* impurity type to prevent electrical interaction between adjacent FETs. (*See* Section VI.A.4.) (Ex. 1001 ¶200.) The initial doping is of a first conductivity type.

Alternatively, Chau discloses that the **semiconductor region** is of a first conductivity type. Chau explains that “[w]hen channel region is doped it is typically doped to the opposite conductivity type of the **source region** 330 and the **drain region** 332.” (Ex. 1008 ¶24.) Thus, a POSITA reading Chau would have understood that the region of the **semiconductor fin** located between the **source** and **drain regions** is initially doped to a first conductivity type, where the **source** and **drain** are later doped to a second, or opposite conductivity type. (*Id.* at Claim 14 (“**single crystalline silicon body** is doped to a first conductivity type”).) (Ex. 1001 ¶201.) The initial doping of the **fin** ensures that the **source/drain regions** do not leak current into the the **fin** and **substrate**. (*See* Section VI.A.4.) (Ex. 1001 ¶201.)

Chau further discloses a **plurality of semiconductor regions**. Chau explains that “[i]n order to fabricate the transistors with larger gate widths, transistor 300 can include an **additional or multiple semiconductor bodies or fingers 308** as shown in Fig. 4B.” (Ex. 1008 ¶31.) Thus, Chau teaches a “**first semiconductor region**” or a “**plurality of semiconductor regions**,” each having an upper and side surface. (Ex. 1001 ¶202.)

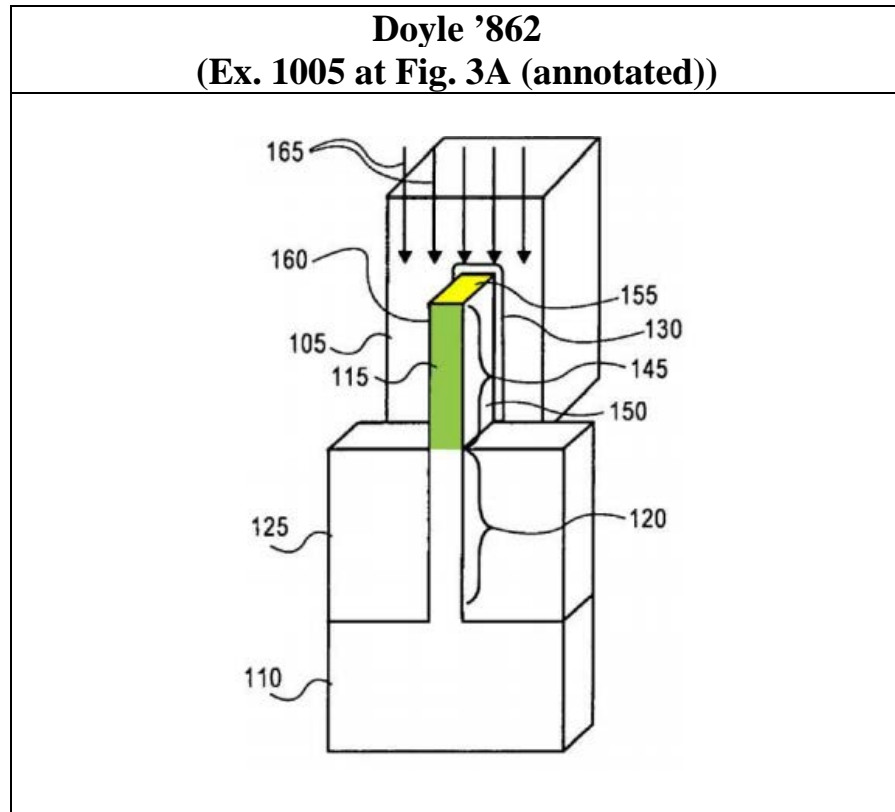


A POSITA would have been motivated to combine Doyle '862 with Chau.  
(See Section X.A.1.e.)



*b. 13[b]: “first impurity region of a second conductivity type formed in an upper portion of each of the plurality of semiconductor regions and made of a semiconductor;”*

Doyle '862 in combination with Chau renders obvious a **first impurity region** formed in an upper portion of each of the **silicon fins**. Doyle '862 discloses a **first impurity region** is formed in an upper portion of a **silicon fin** by implanting dopants through vertical implantation, as illustrated in Figure 3A. (Ex. 1005 at 3:12–15 (“In FIG. 3A, **top surface** 155 of **silicon fin** 115 is doped using a process, such as, for example, ionized implantation at 0°, i.e., vertical implantation.”); *id.* at Claim 1 (“selectively doping the top surface of the **silicon body**”).) (Ex. 1001 ¶203.)



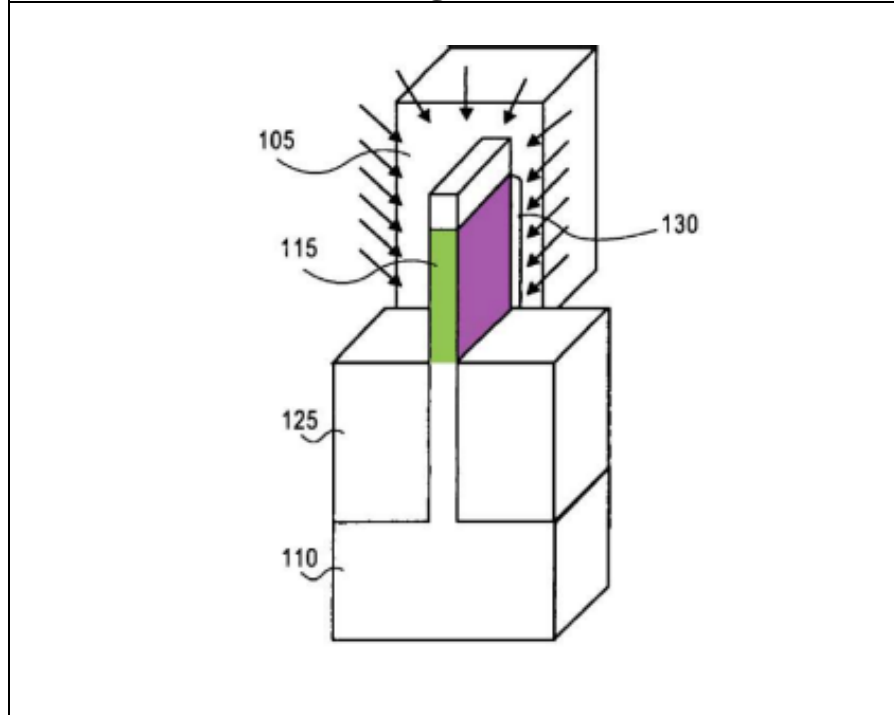
Doyle '862 renders obvious this **first impurity region** is of a second conductivity type and made of a semiconductor. (See Section X.A.1.c.)

As previously discussed, Chau discloses a **plurality of semiconductor regions**. (See Section X.A.1.a.) A POSITA would have found it obvious that each of the **plurality of semiconductor regions** disclosed by Chau would have a **first impurity region** as disclosed by Doyle '862. (Ex. 1001 ¶204.) This is because in order for a transistor with a **plurality of semiconductor regions** to turn “on” or “off,” each **fin** would need to have its own **source/drain regions**. (*Id.*)

*c. 13[c]: “a **second impurity region** of a second conductivity type formed in a side portion of each of the **plurality of semiconductor regions** and made of a semiconductor”*

Doyle '862 in combination with Chau renders obvious a **second impurity region** formed in the side portion of each of a **plurality of fins**, made of a semiconductor. Doyle '862 discloses that a **second impurity region** is formed in a side portion of the **silicon fin** though selective angled implantation or plasma-induced ion implantation. (Ex. 1005 at 3:65–67 (“[A]ngled ion implantation can be performed to selectively dope **sidewalls** 150 and 155, illustrated in FIG. 3F.”); *id.* at 4:2–3 (“Alternatively, plasma-induced ion implantation (PLAD) can be performed to selectively dope **sidewalls** 150 and 155.”); *id.* at Claim 1 (“doping the **first side surface** and the **second side surface** of the **silicon body**”).) (Ex. 1001 ¶205.)

**Doyle '862**  
(Ex. 1005 at Fig. 3F (annotated))



Doyle '862 renders obvious the **first** and **second impurity regions** are of a second conductivity type. “For PMOS transistor devices, the **source** and **drain region** are typically doped with p-type impurities, such as boron.” (Ex. 1005 at 3:2–4.) Doping a **source-drain region** with P-type dopants creates a P-type **source-drain region**. (Ex. 1001 ¶206.) As previously discussed, a POSITA would have known that the **fin** was initially lightly doped with ions of a first conductivity type, followed by doping of the **source-drain regions** with ions of a second conductivity type. (See Section X.A.1.a; *see also* Section VI.A.4.) (Ex. 1001 ¶206.)

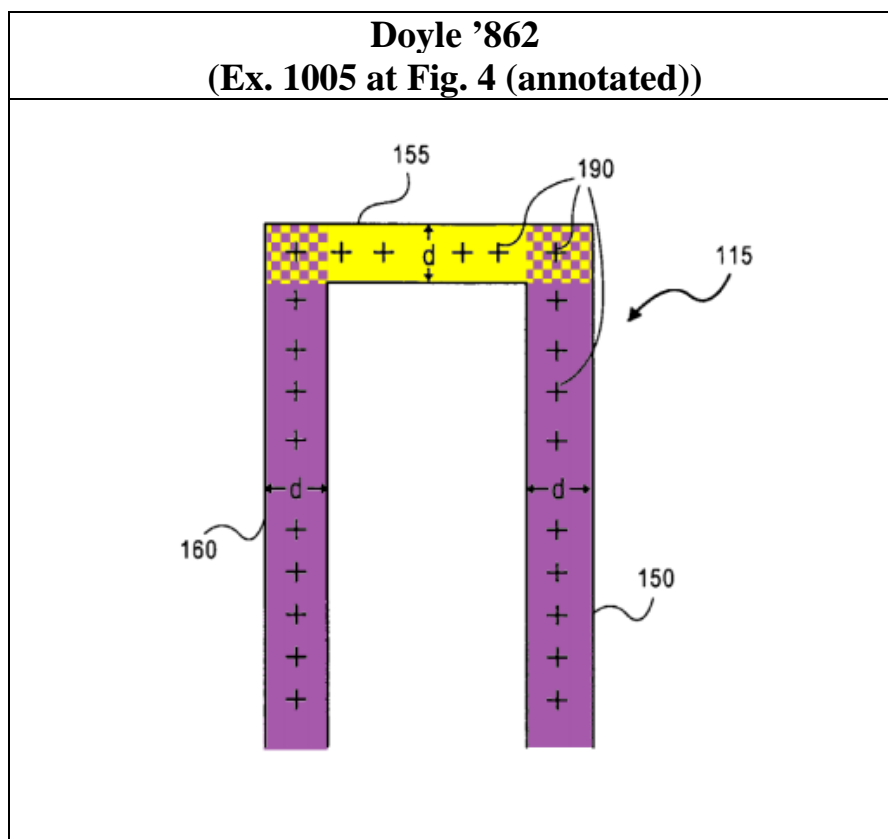
Doyle '862 further renders obvious that the **first** and **second impurity regions** are made of a semiconductor. Doyle '862 discloses that P-type and N-type

impurities are implanted in the **silicon fin**. (Ex. 1005 at 3:4–6). The purpose of doping with these impurities is to allow current to flow more freely within the semiconductor material. (See Section IX.A.3.) Thus, a POSITA would have known that the doped regions are made of a semiconductor. (Ex. 1001 ¶¶207, 208.)

As previously discussed, Chau discloses a **plurality of semiconductor regions**. (See Section X.A.1.a.) A POSITA would have found it obvious that each of the **plurality of semiconductor regions** disclosed by Chau would have a **second impurity region** as disclosed by Doyle '862. (Ex. 1001 ¶204.) This is because in order for a transistor with a **plurality of semiconductor regions** to turn “on” or “off,” each **fin** would need to have its own **source/drain regions**. (*Id.*)

*d. 13[d]: wherein a resistivity of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.*

Doyle '862 in combination with Chau renders obvious a resistivity of the **second impurity region** is substantially equal to the resistivity of the **first impurity region**. The **fin** can be uniformly doped on the upper and side regions, *i.e.*, the **first** and **second impurity regions**, respectively, as shown below in Figure 4. (Ex. 1005 at 4:13–15 (“**silicon fin** 115 can be *uniformly doped* on surfaces 150, 155 and 160, respectively”); *see also id.* at 4:21–23 (“once fabrication is completed to create a functional transistor, the current flowing, or ‘wrapping around,’ **silicon fin** 115 should be uniform which results in a more efficient transistor”).) (Ex. 1001 ¶209.)



A POSITA would have understood that Doyle '862 renders obvious a uniform resistivity in the **first** and **second impurity regions** because it discloses uniform doping to, and uniform current flowing through, the **silicon fin**. (Ex. 1001 ¶209.) A POSITA would have understood that uniform doping would create regions of uniform resistivity, because resistivity is a characteristic that measures the ability of current to flow through a region. (Ex. 1001 ¶210.) Alternatively, a POSITA would have understood that current could not flow uniformly through the **silicon fin** if the resistivity, or ability of a region to resist the flow of current, was not uniform. (*Id.*) Thus, Doyle '862's disclosure of uniform doping to the **source-drain regions** renders obvious uniform resistivity. (Ex. 1001 ¶¶209–11.)

*e. Motivation to Combine*

A POSITA would have been motivated to combine the teachings of Doyle '862 with Chau for a number of reasons. First, both Doyle '862 and Chau address the same problem of fabricating a transistor with optimal device performance. Doyle '862 discusses the difficulty of uniformly doping a FinFET with a **plurality of silicon fins**. (Ex. 1005 at 1:44–48 (“Additionally, when a **substrate** comprises a **plurality of silicon fins** on the same surface, one **silicon fin** can create a shadow on another **silicon fin** situated approximately perpendicular and approximately adjacent to one another in angled doping, which results in variable doping on the surfaces of the **silicon fins**.”).) (See Section IX.A.) Similarly, Chau discloses how to “increase device performance,” particularly by use of a “fully depleted silicon on insulator (SOI) transistor.” (Ex. 1008 ¶4.) A POSITA would have recognized that an SOI that is not fully depleted increases parasitic capacitance between the **source** and the **drain regions**. This leads to non-optimal transistor performance because a higher parasitic capacitance impedes the speed with which a transistor can switch “on” or “off.” Moreover, four of the same named inventors (Robert Chau, Brian Doyle, Jack Kavalieros, Suman Datta) are listed on each. (Ex. 1005 at Cover; Ex. 1008 at Cover.) (Ex. 1001 ¶¶213, 214.)

Second, a POSITA would have been motivated to apply the uniform doping method disclosed by Doyle '862 to the **plurality of fins** disclosed by Chau, to create

a FinFET with desirable characteristics in a larger gate width. The use of a **plurality of fins** was a known technique for improving a transistor device by creating a larger effective gate width—*i.e.*, the contact area between the gate and the **plurality of fins** is greater than the contact area between the gate and a single **fin**. Increasing the gate width results in the transistor being able to control higher current levels, allowing it to simultaneously provide the same output signal to multiple logic gate inputs. (Ex. 1001 ¶215.) This “fan out” feature in turn allows increased integrated circuit functionality. (Ex. 1001 ¶216.) An increased effective gate width also leads to a more compact layout for FinFET devices, permitting a higher density of devices within a given area. (Ex. 1001 ¶217.) The area savings translates directly into lower unit production cost of each integrated circuit. (*Id.*) A POSITA would thus have been motivated to make a FinFET device with desirable characteristics, by manufacturing a **plurality of** uniformly-doped **fins**. (Ex. 1001 ¶¶215–17.)

Third, a POSITA would have been motivated to combine prior art elements from Doyle '862 and Chau according to known methods to yield predictable results. Doyle '862 discloses a method for uniformly doping a single **fin** in a FinFET. (*See* Section IX.A.) Chau discloses a FinFET with a **plurality of silicon fins**. (*See* Section IX.C.) Chau further discloses that the **fins** have “**source region** 330 and **drain region** 332 [that] will have the same doping concentration and profile.” (Ex. 1008 ¶23.) Combining Chau’s disclosure of **fins** with doped **source** and **drain**



**regions** with the uniform doping method in Doyle '862 would yield the predictable result of a **plurality of** uniformly-doped **fins**. (Ex. 1001 ¶218.)

In addition, a POSITA would recognize that Doyle '862's method could be applied to a **plurality of fins**. First, vertical implantation can be effectively performed on a **plurality of fins** since vertical implantation implants only the upper surface of each **fin**. (See Section IX.A; Ex. 1001 ¶219.) Next, the conformal layer can be deposited by physical vapor deposition and then anisotropically etched (etched with little to no undercutting) by reactive ion etching on a **plurality of fins**. (Ex. 1005 at 3:37–42; *see also* Section IX.A; Ex. 1001 ¶¶220, 221.) The top surfaces of the **plurality of fins** can then be modified by re-oxidation. (See Section IX.A; Ex. 1001 ¶222.) Next, the spacers can be removed by isotropic etching from all **fins**. (See Section IX.A; Ex. 1001 ¶223.) Finally, the sidewalls can be selectively doped by plasma-induced ion implantation, which can be performed to evenly dope the sidewalls of a **plurality of fins**. (See Section IX.A; Ex. 1001. ¶224.) In this manner, applying Doyle '862's uniform doping method to a **plurality of silicon fins** would have yielded the predictable result of a transistor with the required gate width that has optimized electrical characteristics. (*Id.* ¶225.)

Fourth, combining Doyle '862 with Chau constitutes a simple substitution of one known element for another to obtain predictable results. Chau discloses **fins** with **source-drain regions**. (Ex. 1008 ¶23 (**fins** have “**source region** 330 and **drain**

**region** 332 [that] will have the same doping concentration and profile.”).) Doyle ’862’s disclosure of a uniformly-doped **fin** can be substituted into Chau’s disclosure of FinFET with a **plurality of fins** with doped **source-drain regions**. This simple substitution yields the predictable result of a FinFET with a **plurality of** uniformly-doped **silicon fins**. (Ex. 1001 ¶226.)

Fifth, it would have been obvious to try the uniform doping method disclosed in Doyle ’862 on a transistor with a **plurality of fins**, as disclosed by Chau. Doyle ’862 and Chau list four of the same inventors. (Ex. 1005 at Cover; *see also* Ex. 1008 at Cover.) As previously discussed, the common inventors addressed the same problem of optimizing transistor performance in a FinFET. A POSITA would have found it obvious to combine the inventions of a common group of inventors working to address the same problem. (Ex. 1001 ¶227.) Doyle ’862 expressly discloses the problem of uniformly doping a transistor with a **plurality of fins**. (Ex. 1005 at 1:44–49 (“Additionally, when a substrate comprises a **plurality of silicon fins** on the same surface, one silicon **fin** can create a shadow on another silicon **fin** situated approximately perpendicular and approximately adjacent to one another in angled doping, which results in variable doping on the surfaces of the silicon **fins**.”).) Chau expressly discloses a transistor with a **plurality of fins**. (Ex. 1008 ¶31 (“transistor 300 can include an additional or multiple semiconductor bodies or fingers 308 as shown in FIG. 4B”).) Thus, because a POSITA would have known

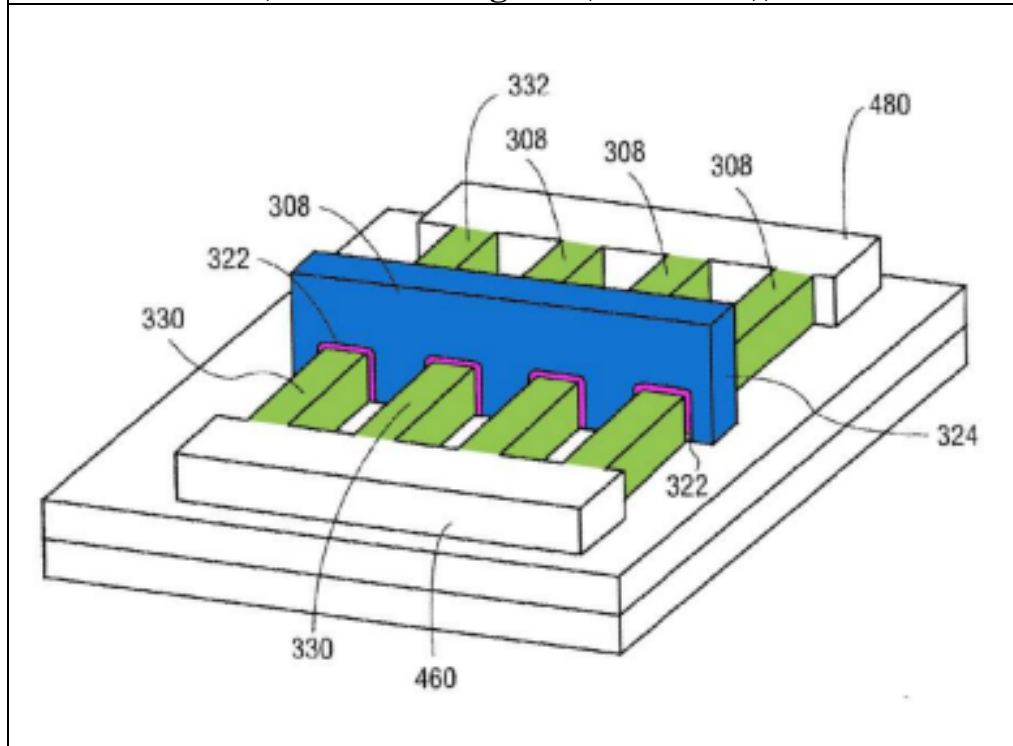
that the common inventors of Doyle '862 and Chau were addressing the same problem, it would have been obvious to try the uniform doping method of Doyle '862 on the FinFET with a **plurality of fins** disclosed by Chau. (*Id.* ¶227.)

## 2. Dependent Claim 14

*a. 14[a]: “The semiconductor device of claim 13, further comprising a **gate electrode** formed on each of the **plurality of semiconductor regions** with a **gate insulating film** interposed therebetween”*

As previously discussed, Doyle '862 in combination with Chau renders obvious claim 13. (See Section X.A.1.) Chau further discloses a **gate electrode** formed on each of a **plurality of fins**, with a **gate insulating film** interposed between. As shown in Figure 4B, Chau discloses a **plurality of fins**, where “[e]ach **semiconductor body** 308 has a **gate dielectric layer** 322 formed on its top surface and sidewalls . . . . **Gate electrode** 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308.” (Ex. 1008 ¶31; *see also id.* at Claim 19 (“a **gate dielectric** formed on the top surface and sidewalls of each of said **semiconductor bodies**; a **gate electrode** formed on the **gate dielectric** on the top surface of each of said **plurality of semiconductor bodies** and adjacent to said **gate dielectrics** formed on each of said first and second laterally opposite sidewalls of each of said **silicon bodies**”).) In other words, the **gate electrode** is formed on each of the **semiconductor regions**, with **gate insulating film** interposed therebetween. (Ex. 1001 ¶229.)

**Chau**  
(Ex. 1008 at Fig. 4B (annotated))



*a. 14[b]: “wherein the **gate electrode** extends across the **plurality of semiconductor regions** in a gate width direction.”*

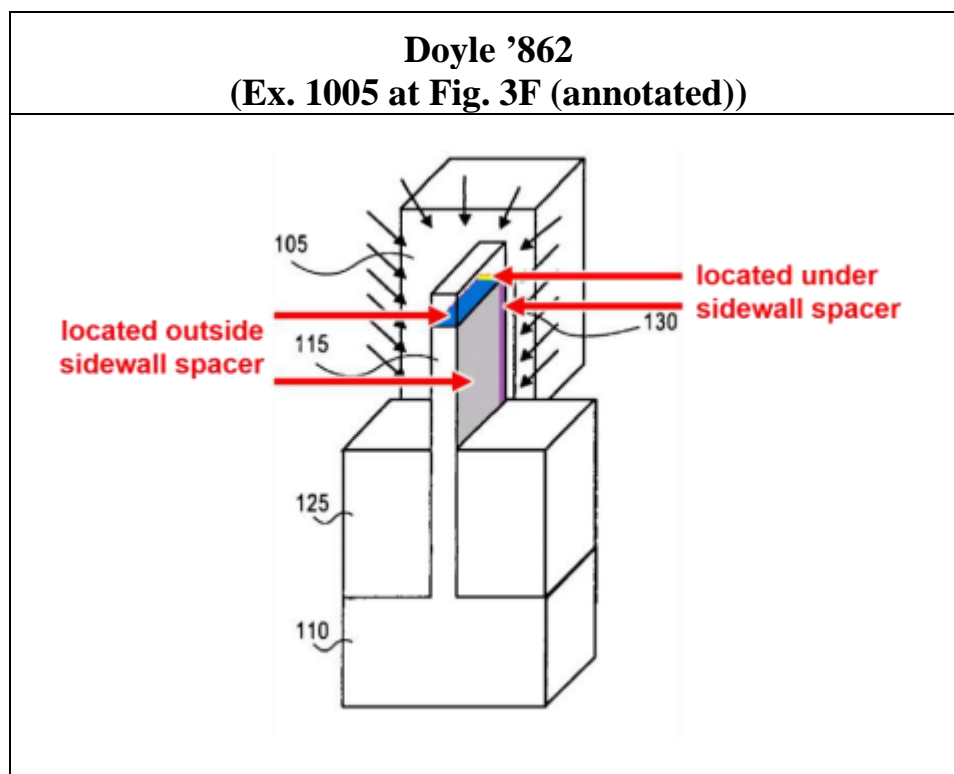
Chau discloses that the **gate electrode** 324 extends across the **plurality of fin-shaped semiconductor regions** in a gate width direction. Chau renders obvious that the gate width direction is the direction labeled in Figure 3 because it refers to gate width dimensions along that axis. (Ex. 1008 at Claim 20 (“gate width of said transistor is approximately the sum of the gate widths of each of said **semiconductor bodies** wherein the gate width of a **semiconductor body** is two times the height of the **semiconductor body** plus the distances between the laterally opposite sidewalls.”) (Ex. 1001 ¶230.)

[illegible]

Chau further discloses that the **gate electrode** extends across the **plurality of** **gate electrodes** in the gate width direction. (Ex. 1008 at Fig. 4B; *see also id.* ¶31 (“**Gate electrode** 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **conductor bodies** 308.”).) (Ex. 1001 ¶231.)



to form the **second impurity region**. (Ex. 1005 at 3:12–15, 3:67–4:2; *see also id.* at 3:56–58 (“In addition, re-oxidation does not affect the **gate structure** 105 because it is protected by a **spacer formation** formed on the gate sidewall (not shown.”).) Thus, Doyle ’862 discloses the **first** and **second impurity regions** are doped regions of the **fin** located beneath the **sidewall spacers**, which the ’165 patent refers to as **extension regions**. (Ex. 1001 ¶223.) These regions are shown in Figure 3F below.



Doyle ’862 further renders obvious that the **first** and **second impurity regions** are P-type. Doyle ’862 discloses that for a “PMOS transistor device[], the **source** and **drain region** are typically doped with p-type impurities, such as boron.” (Ex. 1005 at 3:2–4.) As previously discussed, a POSITA would have known that the doping of the **extension regions** would be of the same type as the doping of the

**source-drain regions**, in order to minimize short channel effects. (See Section VI.A.4.) Thus, Doyle '862 renders obvious P-type **extension regions**. (Ex. 1001 ¶234.)

#### **4. Dependent Claim 16**

- a. 16: “The semiconductor device of claim 14, wherein the **first impurity region** and the **second impurity region** are a P-type **source-drain region**.”*

As previously discussed, Doyle '862 in combination with Chau, renders obvious claim 14. (See Section X.A.2.) As previously discussed, Doyle '862 renders obvious **first** and **second impurity regions** in the **source-drain region**. (See Section X.A.1.)

Doyle '862 further discloses the **source-drain regions** can be P-type. (Ex. 1005 at 3:2–4 (“For PMOS transistor devices, the **source** and **drain region** are typically doped with p-type impurities.”).) (Ex. 1001 ¶236.)

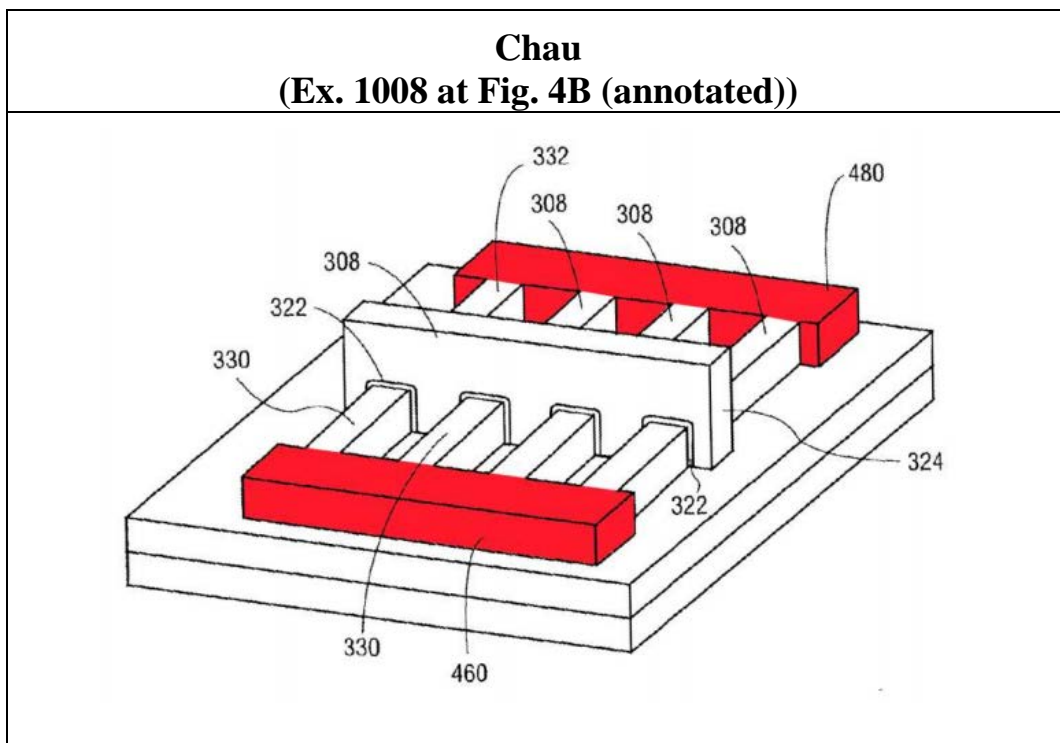
#### **5. Dependent Claim 17**

- a. 17: “The semiconductor device of claim 13, further comprising a **third semiconductor region** connecting together end portions of the **plurality of semiconductor regions** on each side of the **semiconductor regions** in a gate length direction.”*

As previously discussed, Doyle '862 in combination with Chau renders obvious claim 13. (See Section X.A.1.) Chau further discloses a **third semiconductor region** connecting together end portions of the **fins**, i.e., a **landing pad**. Specifically, Chau describes “**source regions** 330 and **drain regions** 332 of



the **semiconductor bodies** 308 are electrically coupled together by the semiconductor material . . . to form a **source landing pad** 460 and a **drain landing pad** 480 as shown in FIG. 4B.” (Ex. 1008 ¶31; *see also id.* at Claim 22 (“each of said **source regions** are coupled together and each of said **drain regions** are coupled together”).) Such **landing pads** electrically couple the ends of a **plurality of fins** in a gate length direction as shown below in Figure 4B. (Ex. 1001 ¶238.)



## 6. Independent Claims 18 and 19

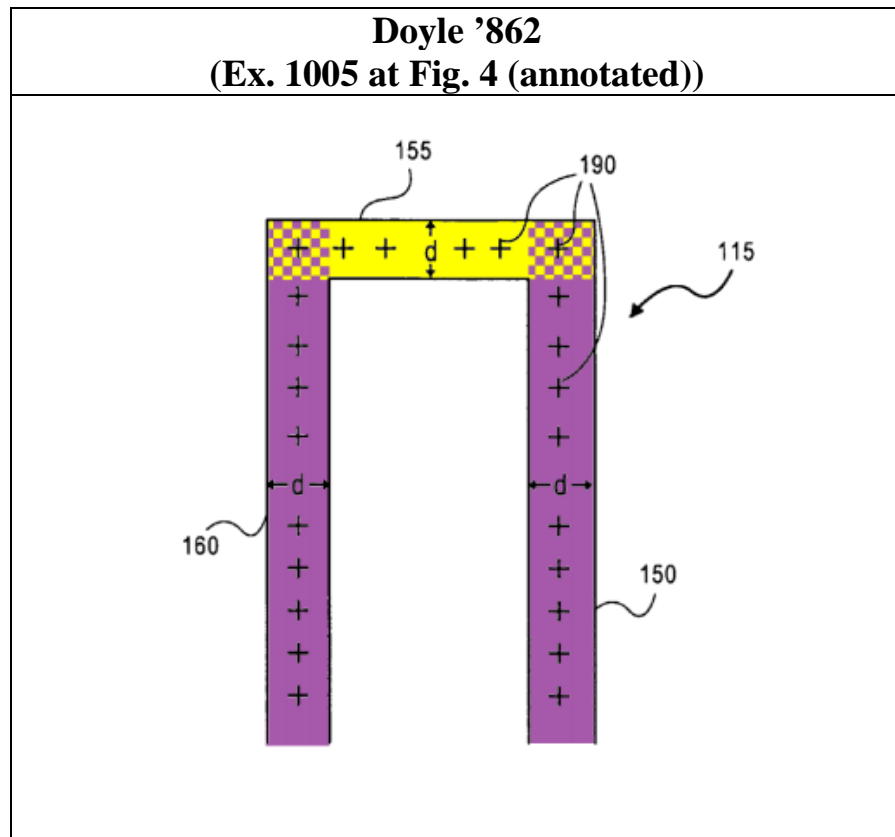
- a. 18, 19[preamble]–18, 19[c]: “A semiconductor device, comprising:  
*a first semiconductor region of a first conductivity type formed on a substrate and having an upper surface and a side surface;*  
*a first impurity region of a second conductivity type formed in an upper portion of the first semiconductor region and made of a semiconductor; and*  
*a second impurity region of a second conductivity type formed in a side portion of the first semiconductor region and made of a semiconductor”*

As previously discussed, Doyle '862 discloses a **first semiconductor region**, *i.e.*, a **silicon fin**, of a first conductivity type formed on a **substrate** having an upper and side surface. (See Section X.A.1.a.) Doyle '862 further discloses a **first impurity region** formed in an upper portion of a **silicon fin** made of a semiconductor. (See Section X.A.1.b.) Doyle '862 further discloses a **second impurity region** is formed in a side portion of the **silicon fin** made of a semiconductor. (See Section X.A.1.c.) (Ex. 1001 ¶¶239, 240.)

- b. 18[d]: “[wherein] a sheet resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.”

Doyle '862 renders obvious that the sheet resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. As previously discussed, Doyle '862 discloses a uniform resistivity in the **first** and **second impurity regions**. (See Section X.A.1.d.) A POSITA would have known

that, for a constant thickness, sheet resistance is directly proportional to resistivity. (See Section VI.A.5; *see also* Ex. 1009 at 1; Ex. 1001 ¶241.) Doyle '862 discloses that the thickness of the impurity region is constant, and this is confirmed in Figure 4. (Ex. 1005 at 4:16–18 (“As can be seen, **silicon fin** 115 is uniformly doped by ions 190 to a depth  $d$  below surfaces 150, 155 and 160.”).)



As previously discussed, sheet resistance measures resistivity as a function of the thickness of the material. (See Section VI.A.5.) Because the resistivity and thickness of the upper and side impurity regions is uniform, a POSITA would have known that the sheet resistance in the upper and side impurity regions is substantially equal. (Ex. 1001 ¶242.)

- c. 19[d]: “[wherein] a spreading resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.”

Doyle '862 renders obvious that the spreading resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. As previously discussed, Doyle '862 discloses a uniform resistivity in the **first** and **second impurity regions**. (See Section X.A.1.d.) Spreading resistance is the measure of resistance between any two points in or on a layer of material, and it is always directly proportional to resistivity. (See Section VI.A.5.) Thus, if the resistivity of the upper and side impurity regions is substantially equal, and the concentration of implanted ions is uniform (as disclosed by Doyle '862 (Ex. 1005 at 4:16–18)), a POSITA would have known that the spreading resistance in the upper and side regions is likewise substantially equal. (Ex. 1001 ¶¶233, 234.)

## **B. Ground 2: Claims 13–19 Are Obvious in View of Goktepelı in Combination with Chau**

### **1. Independent Claim 13**

- a. 13[preamble]–[a]: “A semiconductor device, comprising:  
*a plurality of semiconductor region of a first conductivity type formed on a **substrate** and each having an upper surface and a side surface;*”

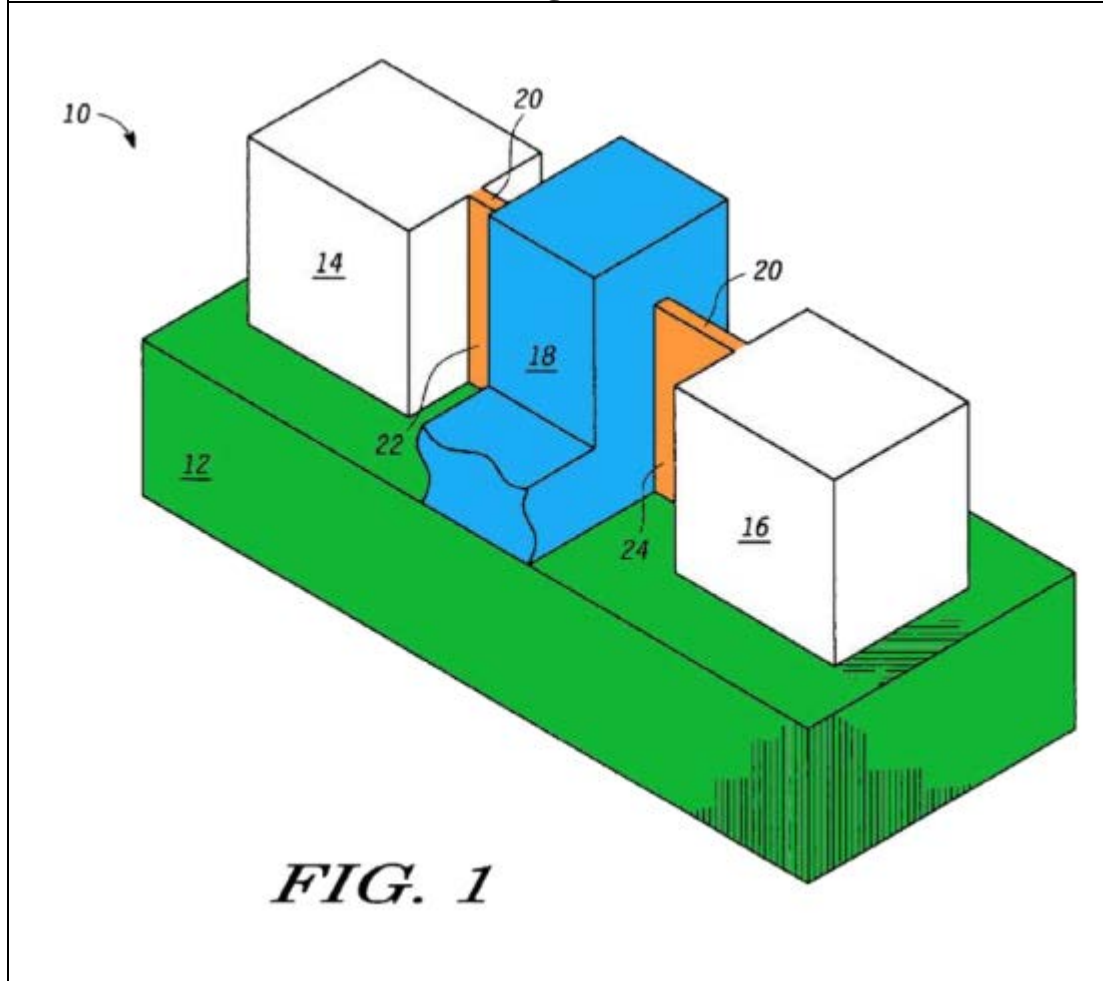
Goktepelı discloses a single **first semiconductor region** (i.e., a **silicon fin**) formed on a **substrate**. Goktepelı discloses a “semiconductor device 10 comprising a **substrate** 12, a conformal layer on the **substrate** 12 which is patterned to form

source/drain contact regions 14 and 16 and a **fin** 20 which forms **extension regions** 22 and 24, and a **gate feature** 18.” (Ex. 1006 at 3:12–16.) Goktepli further renders obvious that the **first semiconductor region**—*i.e.*, the **silicon fin**—has an upper and a side surface by referring to the region as a “**fin**.” (Ex. 1006 at 3:15–16 (“a **fin** 20 which forms **extension regions** 22 and 24,<sup>6</sup> and a **gate feature** 18.”); *see also id.* at Fig. 1.) (Ex. 1001 ¶246.)

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<sup>6</sup> Goktepli appears to refer to the entirety of regions 22 and 24 as the “**extension region**,” whereas the ’165 patent limits “**extension region**” to the doped portion of the **fin** located beneath a **sidewall spacer**. For purposes of this Petition, the definition in the ’165 patent is used, and the “thin **source/drain regions**” 20 that Goktepli refers to as **extension regions** 22 and 24 are the same **source/drain regions** referred to by the ’165 patent. (Ex. 1001 ¶153.)

**Goktepli**  
(Ex. 1006 at Fig. 1 (annotated))



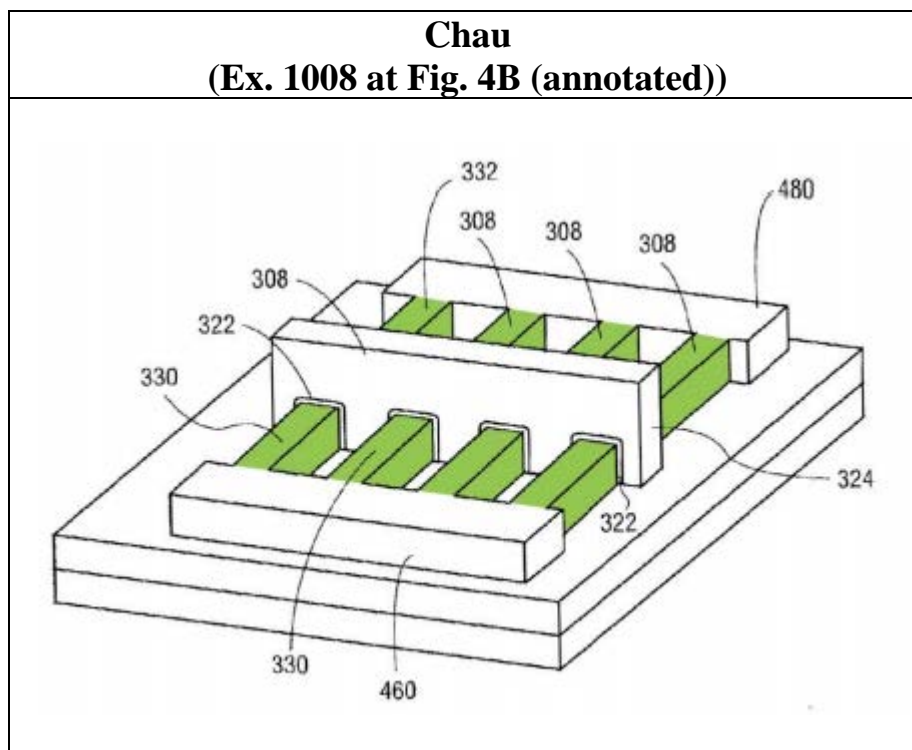
Alternatively, Chau discloses a **fin** with an upper and side surface that is formed on a **substrate**. (Ex. 1008 at Abstract (“a **semiconductor body** having a top surface and laterally opposite sidewalls formed on a **substrate**”); *see also id.* ¶16 (“The tri-gate transistor includes a thin **semiconductor body** formed on a[] **substrate**, the **subst[r]ate** can be an insulating **substrate** or a semiconductor **substrate**.”).) (Ex. 1001 ¶247.)

Goktepli renders obvious that the **first semiconductor region**—*i.e.*, the **silicon fin**—is of a first conductivity type, either N-type or P-type, and the later doping of the **silicon fin** to form the **source-drain regions** is of a second conductivity type. Goktepli discloses doping of the source-drain contact regions (Ex. 1006 at 4:57–60 (“The heating of semiconductor device 10 causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and thoroughly diffuse into source/drain contact regions 14 and 16.”).) A POSITA would have known that the dopants could be P-type or N-type. (*See* Section VI.A.4.) As previously discussed, *before* doping with P-type or N-type impurities, the **silicon fin** would first be lightly doped with the *opposite* impurity type, to prevent electrical interaction between adjacent FETs. (*Id.*) The initial doping creates the claimed **first semiconductor region** of a first conductivity type. (Ex. 1001 ¶249.)

Alternatively, Chau renders obvious that the **semiconductor region** is of a first conductivity type. Chau explains that “[w]hen channel region is doped it is typically doped to the opposite conductivity type of the **source region** 330 and the **drain region** 332.” (Ex. 1008 ¶24.) Thus, a POSITA reading Chau would have understood that the region of the **semiconductor fin** located between the **source** and **drain regions** is initially doped to a first conductivity type, where the **source** and **drain** are later doped to a second, or opposite conductivity type. (Ex. 1008 at Claim 14 (“**single crystalline silicon body** is doped to a first conductivity type”).) (Ex.

1001 ¶250.) The initial doping of the **fin** ensures that the **source/drain regions** do not leak current into the the **fin** and **substrate**. (See Section VI.A.4.) (Ex. 1001 ¶250.)

Finally, Chau discloses a **plurality of semiconductor regions**. Chau explains that “[i]n order to fabricate the transistors with larger gate widths, transistor 300 can include an **additional or multiple semiconductor bodies or fingers 308** as shown in Fig. 4B.” (Ex. 1008 ¶31.) Figure 4B shows the **plurality of semiconductor regions**. Thus, Chau teaches a “**first semiconductor region**” or a “**plurality of semiconductor regions**,” each having an upper and side surface. (Ex. 1001 ¶251.)



A POSITA would have been motivated to combine Goktepli with Chau. (See Section X.B.1.e.)

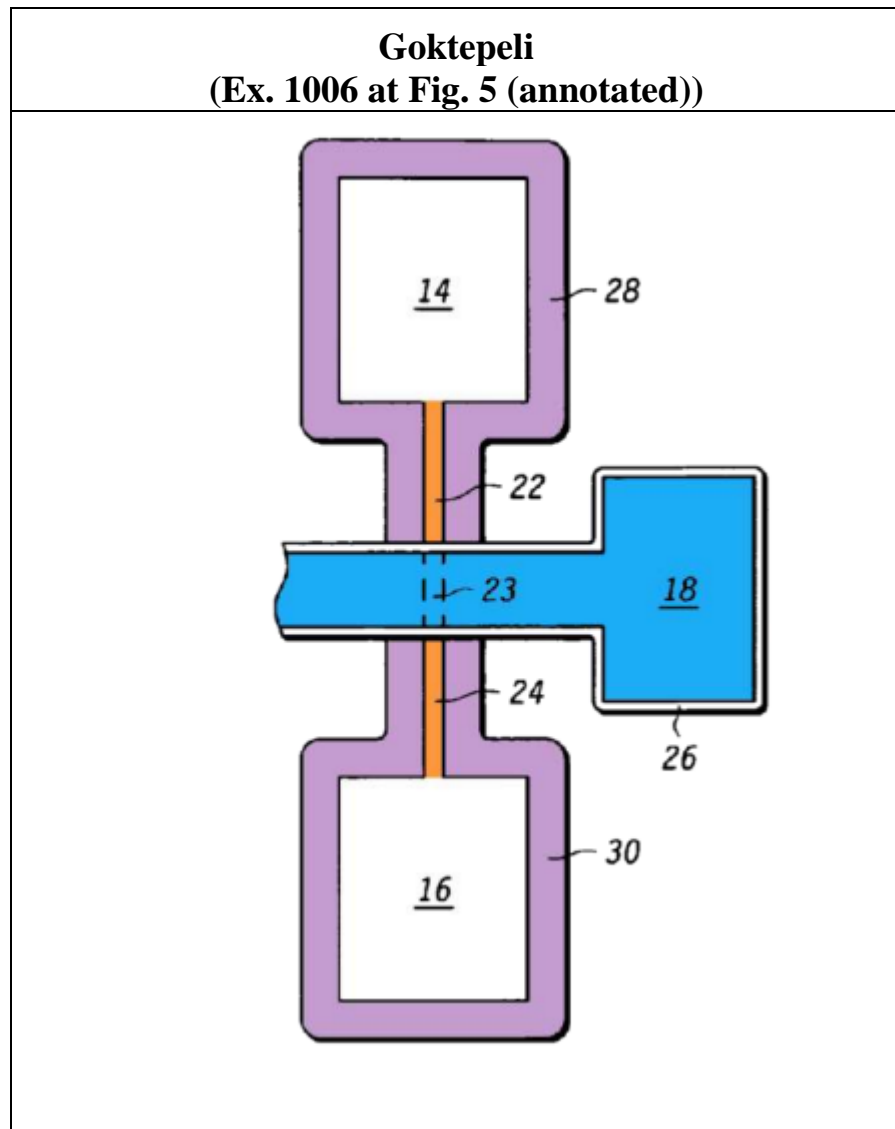


*b. 13[b]: “a **first impurity region** of a second conductivity type formed in an upper portion of each of the plurality of **semiconductor regions** and made of a semiconductor”*

Goktepli renders obvious a **first impurity region** formed in an upper portion in a single **silicon fin** through diffusion from a **sacrificial doping layer**. (Ex. 1006 at 2:63–66 (“The problems associated with doping of the **source/drain extensions** and **source/drain regions** can be overcome by providing a thick amorphous, polycrystalline, or crystalline **sacrificial doping layer**.”).) Goktepli discloses that the **sacrificial doping layer** can be “in-situ doped with source/drain dopants in the growth process to have a desired conductivity of predetermined strength.” (Ex. 1006 at 4:29–31.) Goktepli discloses that an alternative doping method can be used where “angle[d] ion implantation is performed rather than the use of in-situ doping.” (*Id.* at 4:36–38.) A POSITA would have realized that using either method to dope the **source/drain regions** and **source/drain extension regions** of the **fin** would dope the upper portion of the **fin** because the **sacrificial doping layer** is formed directly over the top of the **fin**. (Ex. 1006 at 2:67–3:3 (“The **sacrificial doping layer** is selectively or unselectively grown on the vertical device which functions as the dopant source to dope the thin **source/drain regions**, **source/drain extensions**, or the **gate** through solid-phase diffusion of the dopants from the pre-doped **sacrificial doping layer**.”); *see also id.* at 4:9–11 (“**Sacrificial doping layer** 30 forms around

source/drain contact region 16 and **extension region 24.**"); *see also id.* at Fig. 5.)

(Ex. 1001 ¶252.)



Goktepli renders obvious the **first impurity region** is of a second conductivity type and made of a semiconductor. (See Section X.B.1.c.)

As previously discussed, Chau discloses a **plurality of semiconductor regions**. (See Section X.B.1.a.) A POSITA would have found it obvious that each of the **plurality of semiconductor regions** disclosed by Chau would have a **first**

**impurity region** as disclosed by Goktepli. (Ex. 1001 ¶253.) This is because in order for a transistor with a **plurality of semiconductor regions** to turn “on” or “off,” each **fin** would need to have its own **source/drain region**. (*Id.*)

*c. 13[c]: “a **second impurity region** of a second conductivity type formed in a side portion of each of the plurality of **semiconductor regions** and made of a semiconductor”*

Goktepli renders obvious that a **second impurity region** formed in a side portion of the **silicon fin** through diffusion from a **sacrificial doping layer**. A POSITA would have realized that the same **sacrificial doping layer** that is formed on the upper part of the **fin** in the **source/drain regions**, and **source/drain extension regions**, is also formed on the side of the **fin**. (*See* Section X.B.1.a.) (Ex. 1001 ¶254.)

Goktepli renders obvious the **first** and **second impurity regions** are of a second conductivity type. Goktepli discloses doping of the **source-drain regions**. (Ex. 1006 at 4:57–60 (“The heating of semiconductor device 10 causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and thoroughly diffuse into source-drain contact regions 14 and 16.”).) A POSITA would have known that the dopants could be P-type or N-type. (*See* Section VI.A.4.) As previously discussed, *before* doping with P-type or N-type impurities, the **silicon fin** would first be lightly doped with the *opposite* impurity type, to prevent electrical interaction between adjacent FETs. (*See* Section VI.A.4.) The doping of the **source-**

**drain regions** creates the claimed **first** and **second impurity regions** of a second conductivity type. (Ex. 1001 ¶255.)

Alternatively, Chau renders obvious that the **first** and **second impurity regions** are of a first conductivity type. Chau explains that “[w]hen channel region is doped it is typically doped to the opposite conductivity type of the **source region** 330 and the **drain region** 332.” (Ex. 1008 ¶24.) Thus, a POSITA reading Chau would have understood that the region of the **semiconductor fin** located between the **source** and **drain regions** is initially doped to a first conductivity type, where the **source** and **drain** are later doped to a second, or opposite conductivity type. (Ex. 1008 at Claim 14 (“**single crystalline silicon body** is doped to a first conductivity type”).) (Ex. 1001 ¶256.) The initial doping of the **fin** ensures that the **source/drain regions** do not leak current into the the **fin** and **substrate**. (*See* Section VI.A.4.) (Ex. 1001 ¶256.)

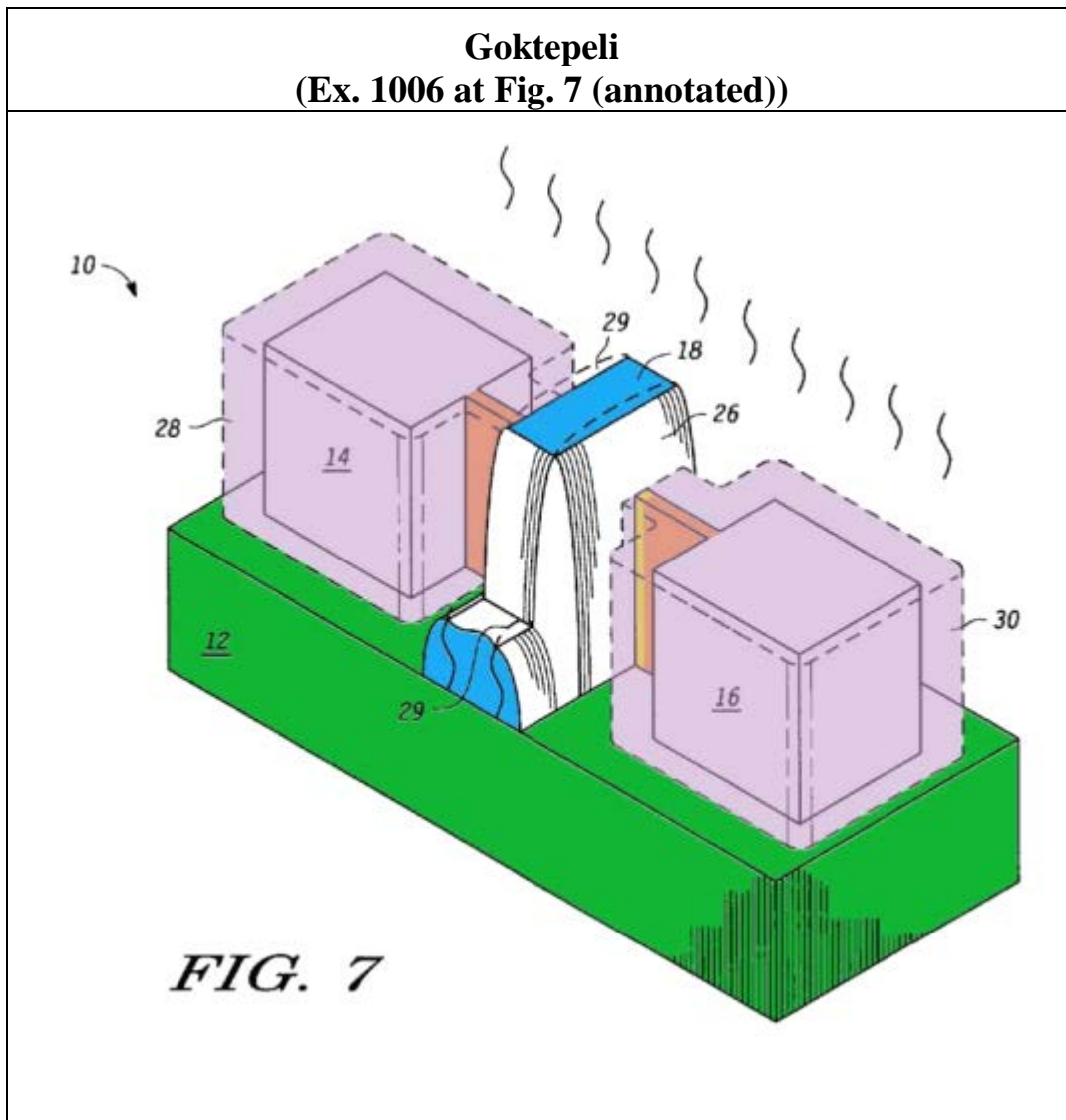
Either of Goktepli or Chau renders obvious that the **first** and **second impurity regions** are made of a semiconductor. Both disclose that the **source-drain regions** are doped. (Ex. 1006 at 3:2–3; *see also* Ex. 1008 ¶24.) The purpose of doping the **source-drain regions** with these impurities is to allow current to flow more freely within the semiconductor material. (*See* Section IX.A.4.) Thus, a POSITA would have known that the doped regions would be made of a semiconductor. (Ex. 1001 ¶257.)

As previously discussed, Chau discloses a **plurality of semiconductor regions**. (See Section X.B.1.a.) A POSITA would have found it obvious that each of the **plurality of semiconductor regions** disclosed by Chau would have a **second impurity region** as disclosed by Goktepli. (Ex. 1001 ¶258.) This is because in order for a transistor with a **plurality of semiconductor regions** to turn “on” or “off,” each **fin** would need to have its own **source/drain regions**. (Ex. 1001 ¶¶258, 259.)

*d. 13[d]: “[wherein] a resistivity of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.”*

Goktepli renders obvious that in a single **fin**, the resistivity of the **second impurity region** is substantially equal to the resistivity of the **first impurity region**. A POSITA would have realized the diffusion doping method disclosed by Goktepli would have uniformly doped the **source/drain regions** and **source/drain extension regions** in a **plurality of semiconductor regions**. (Ex. 1006 at 2:67–3:5 (“The **sacrificial doping layer** is selectively or unselectively grown on the vertical device which functions as a dopant source to dope the thin **source/drain regions**, **source/drain extensions**, or the **gate** through solid-phase diffusion of the dopants from the pre-doped **sacrificial doping layer**.”); *see also id.* at Fig. 7.) (Ex. 1001 ¶260.) The **sacrificial doping layer** is then heated, which “causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and

thoroughly diffuse into source/drain contact regions 14 and 16.” (Ex. 1006 at 4:57–60.) (Ex. 1001 ¶260.)



Because Goktepel discloses that the **source/drain regions** and **source/drain extension regions** receive dopants “evenly and thoroughly,” a POSITA would have known that the resistivity of the upper and side regions of the **fin** would be substantially equal. (Ex. 1001 ¶260.) A POSITA would have known that resistivity is dependent on the concentration and penetration depth of dopant. (See Section

VI.A.4.) A POSITA would have realized that Goktepelı discloses an even concentration and penetration depth of dopant, since the doping by diffusion is even across all contact surfaces, and Goktepelı discloses that formation of the **sacrificial doping layer** can be unselective. (Ex. 1006 at 2:67–3:5.) (Ex. 1001 ¶260.) Thus, Goktepelı renders obvious a resistivity of the side region of the **fin** substantially equal to that of the top, both in the **source/drain region**, or in the **source/drain extension region**. (Ex. 1001 ¶260.) A POSITA would have further found it obvious that each of the **plurality of fins** disclosed by Chau would have the same resistivity relationship, in order for a FinFET with a **plurality of fins** to have optimal performance. (Ex. 1001 ¶¶260, 261.)

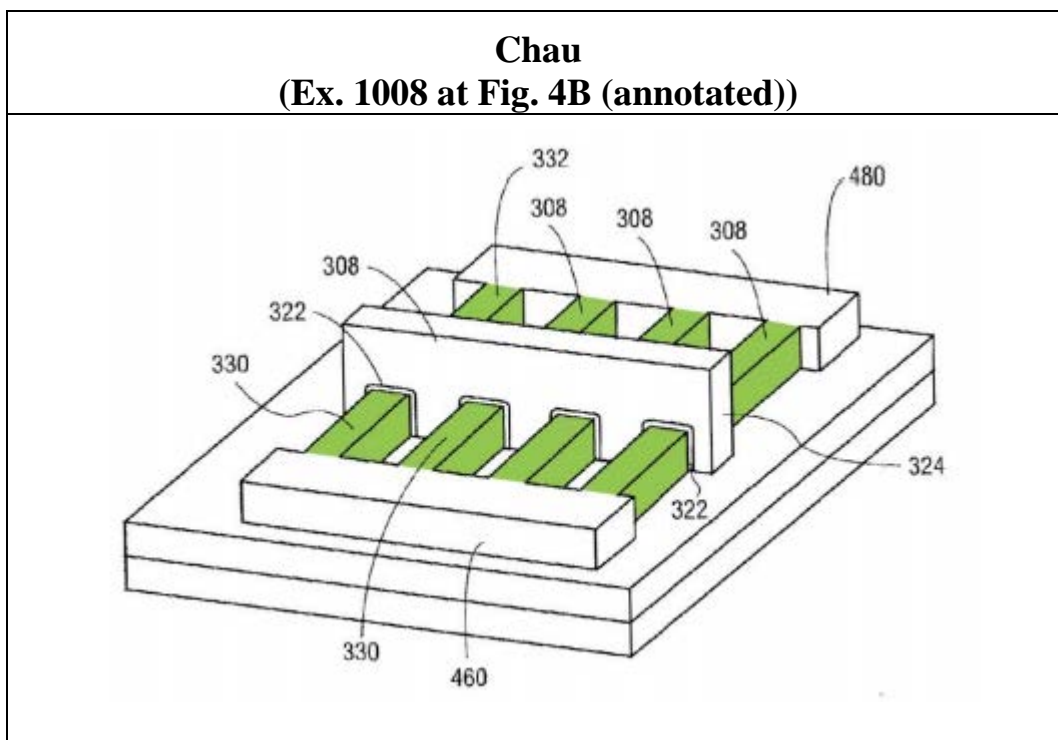
*e. Motivation to Combine*

A POSITA would have been motivated to combine the teachings of Goktepelı and Chau for a number of reasons. First, Goktepelı and Chau both address the same problem of fabricating a transistor with optimal device performance. Goktepelı discloses the use of “[d]oped selective epitaxy . . . to thicken the **source/drain extension regions**.” (Ex. 1006 at 40–42.) Goktepelı further discloses that doping by diffusion is used to “evenly and thoroughly diffuse dopants into the **source/drain regions**.” (*Id.* at 4:59–60.) Chau addresses how to “increase device performance,” particularly by use of a “fully depleted silicon on insulator (SOI) transistor.” (Ex. 1008 ¶4.) A POSITA would have recognized that a fully depleted SOI lowers

parasitic capacitance between the **source** and the **drain regions**. (Ex. 1001 ¶262.)

This leads to optimal transistor performance because with lower parasitic capacitance, the transistor can switch between “on” and “off” states more quickly, allowing logic circuits using it to execute arithmetic operations more quickly. (Ex. 1001 ¶262.)

Specifically, Chau discloses structural features of a tri-gate transistor. Chau discloses a tri-gate transistor with “**multiple semiconductor bodies**,” as shown in Figure 4B. (Ex. 1008 ¶31.) Chau discloses that the purpose of having a transistor with **multiple fins** is to “fabricate the transistors with larger gate widths.” (*Id.* ¶263.)



Goktepli discloses that **source/drain regions** and the **source/drain extension regions** are doped by diffusion to “evenly and thoroughly diffuse



[dopants] into the source/drain contact regions.” (Ex. 1006 at 4:59–60.) A POSITA would have realized that diffusion at a uniform temperature would create uniformly doped **source/drain regions**. (Ex. 1001 ¶264.) Uniform doping on the sides and top of the FinFET **fins** allows optimal doping at every point along the device width, so the entire device can operate with minimal short channel effects. (*Id.*) Thus, a POSITA would have been motivated to combine Goktepli and Chau in order to create a transistor with a **plurality of fins** with minimal short channel effects. (*Id.*)

Second, a POSITA would have been motivated to apply the doping method disclosed in Goktepli, to the disclosure of a **plurality of fins** in Chau, to create a FinFET with a larger gate width that has desirable transistor characteristics. As Chau discloses, a FinFET with a **plurality of fins** can be used to “fabricate . . . transistors with larger gate widths.” (Ex. 1008 ¶31.) This is because the “gate width of transistor 300 is equal to the sum of the three gate width[s] created from **semiconductor body** 308 of transistor 300.” (*Id.*) In a transistor with a **plurality of fins**, the effective gate width is the sum of the three gate width[s] from each of the individual **fin[s]**. Increasing the gate width results in the transistor being able to control higher current levels, allowing it to simultaneously provide the same output signal to multiple logic gate inputs. (Ex. 1001 ¶265.) This “fan out” feature in turn allows increased integrated circuit functionality. (Ex. 1001 ¶266.) An increased effective gate width also leads to a more compact layout for FinFET devices,

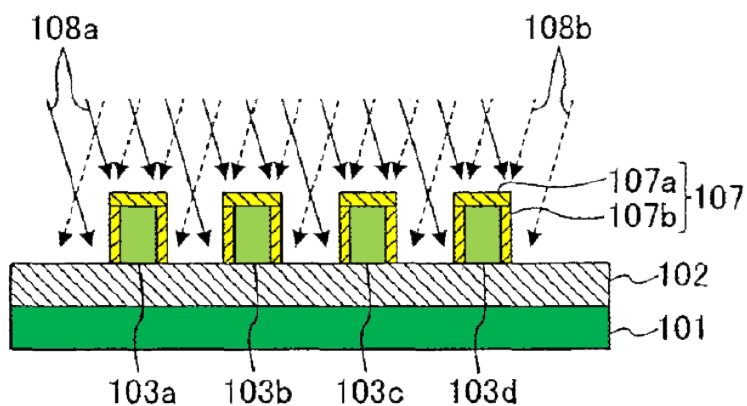
permitting a higher density of devices within a given area. (Ex. 1001 ¶266.) The area savings translates directly into lower unit production cost of each integrated circuit. (Ex. 1001 ¶267.) A POSITA would thus have been motivated to make a FinFET device with desirable characteristics, by manufacturing a **plurality of** uniformly-doped **fins**. (Ex. 1001 ¶¶265–67.)

Third, a POSITA would have been motivated to combine prior art elements from Goktepelı and Chau according to known methods to yield predictable results. Goktepelı discloses one method of uniform doping of **source/drain regions** and **source/drain extension regions**. (Ex. 1006 at 4:57–60.) Goktepelı additionally discloses that the benefit of using its doping method is to prevent “significant damage to the **extension region** since it is thin and subject to full penetration by implanted ions.” (*Id.* at 1:63–65.) Chau discloses the use of a **plurality of fins** to increase the effective gate width of a transistor. A POSITA would have known that each of the **plurality of fins** could have been doped using a number of doping methods, such as implantation, angled implantation, plasma doping, or epitaxial deposition. (*See, e.g.*, Ex. 1006 at 1:63–65 (discussing in “Background of the Invention” that ion implantation can cause significant damage); Ex. 1003 at 3:19–37 (APA discusses the problems with known methods of doping, such as angled ion implantation and plasma doping).) (Ex. 1001 ¶268.)

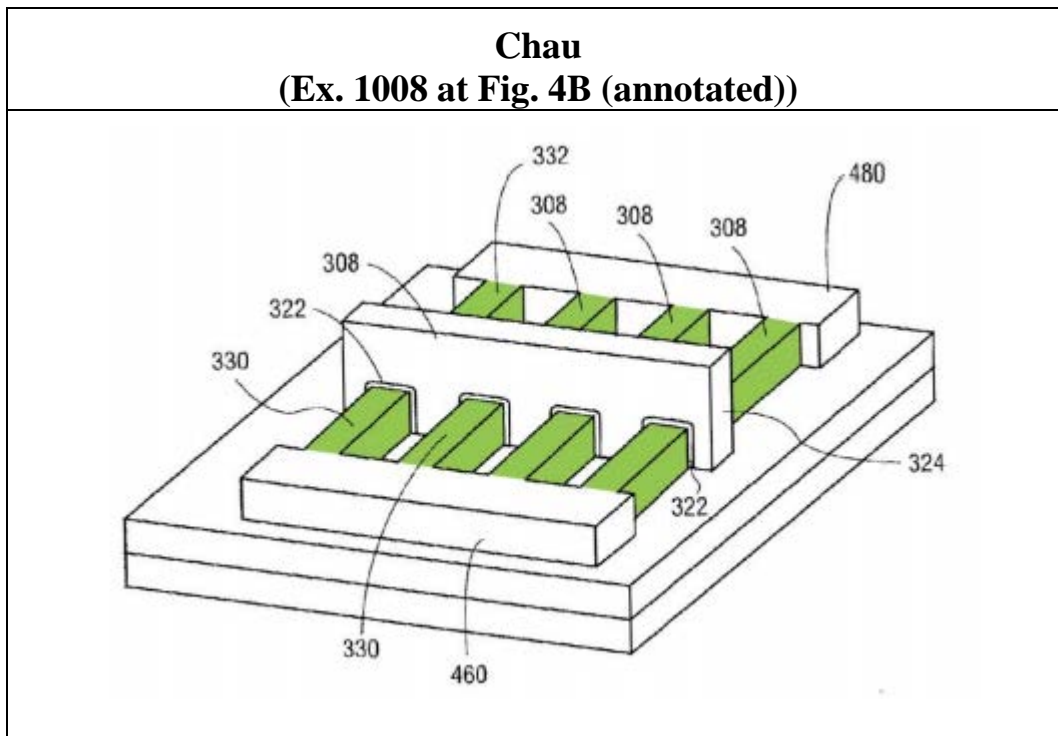
**'165 Patent (APA)**  
**(Ex. 1003 at Fig. 18A (annotated))**

**FIG. 18A**

PRIOR ART



The use of the doping method disclosed by Goktepli with Chau's disclosure of a **plurality of fins** is a combination of known methods to yield predictable results. Applying Goktepli to the **plurality of fins** disclosed in Chau (shown below in Figure 4B), yields the predictable result of a **plurality of uniformly doped fins**, *i.e.*, a uniformly doped transistor with a larger effective gate width and faster switching speed. (Ex. 1001 ¶269.)



Fourth, it would have been obvious to try the doping method disclosed by Goktepel, with the disclosure of a **plurality of fins** disclosed by Chau. As previously discussed, the uniform doping method disclosed by Goktepel results in optimal transistor performance, because a uniformly-doped **fin** has faster switching speed and is less likely to leak current. As previously discussed, the **plurality of fins** disclosed by Chau has the benefit of a larger effective gate width, resulting in the benefits of increased transistor density. Doping using ion implantation requires angled implants to achieve uniformity on the sides and top of an individual **fin**, and a **plurality of fins** can cause “shadowing” of the implant because the **fin** nearest the implantation ion beam creates a “shadow,” blocking some of dopant from reaching bottom portions of more distant **fins**. (Ex. 1001 ¶213.) Similarly, a plasma implant

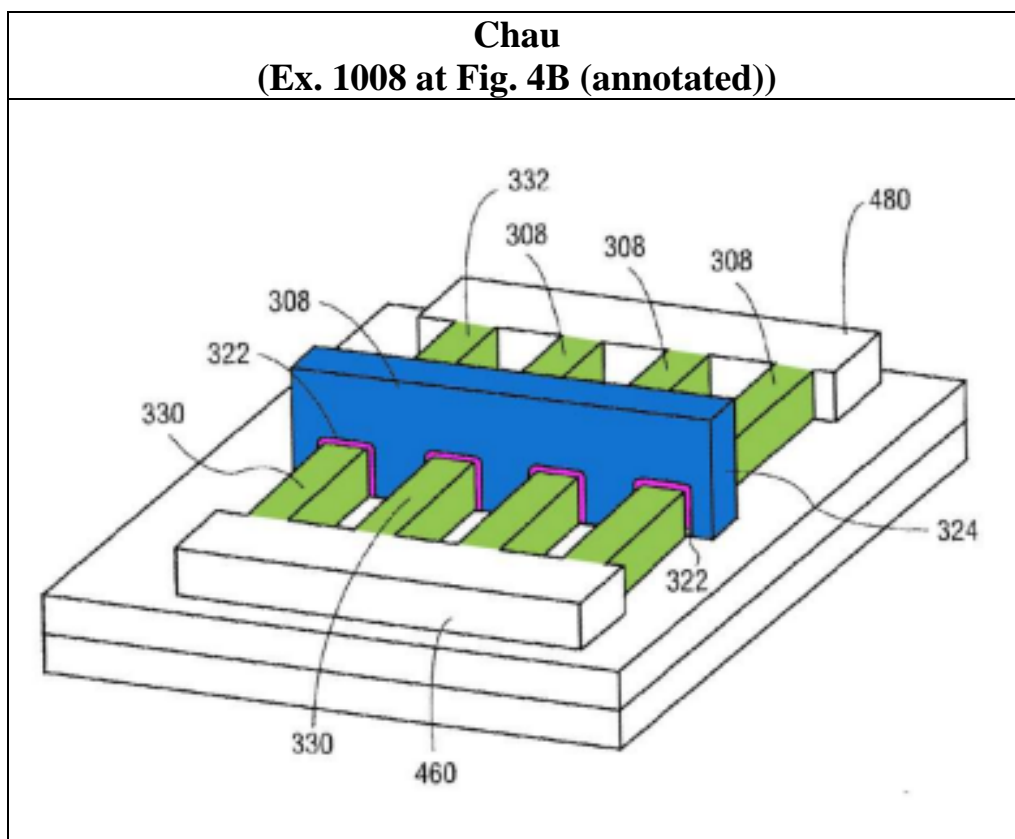
delivers less dopant to the bottom of tightly spaced **fin**s because the rate of delivery per unit surface area is reduced deeper into the gaps. (Ex. 1001 ¶270.) Goktepli, in contrast, uses a uniformly doped **sacrificial doping layer**, providing the same amount of dopant per unit surface area when temperature-cycled, regardless of where the **sacrificial doping layer** is deposited in the spaces between the **fin**s. (*Id.*) Therefore, a POSITA would recognize that Goktepli's method, of all possible methods known at the time, would provide the highest doping uniformity on a **plurality of fin**s in tightly spaced FinFETs, thus rendering Goktepli obvious to try in combination with Chau. (*Id.*)

## 2. Dependent Claim 14

- a. 14[a]: “The semiconductor device of claim 13, further comprising a **gate electrode** formed on each of the **plurality of semiconductor regions** with a **gate insulating film** interposed therebetween,*

As previously discussed, Goktepli in combination with Chau renders obvious claim 13. (See Section X.B.1.) Chau further discloses a **gate electrode** formed on each of a **plurality of fin**s, with a **gate insulating film** interposed between. Figure 4B illustrates the **plurality of fin**s, where “[e]ach **semiconductor body** 308 has a **gate dielectric layer** 322 formed on its top surface and sidewalls . . . . **Gate electrode** 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308.” (Ex. 1008 ¶31; see also *id.* at Claim 19 (“a **gate dielectric** formed on the top surface and sidewalls of each of said **semiconductor**

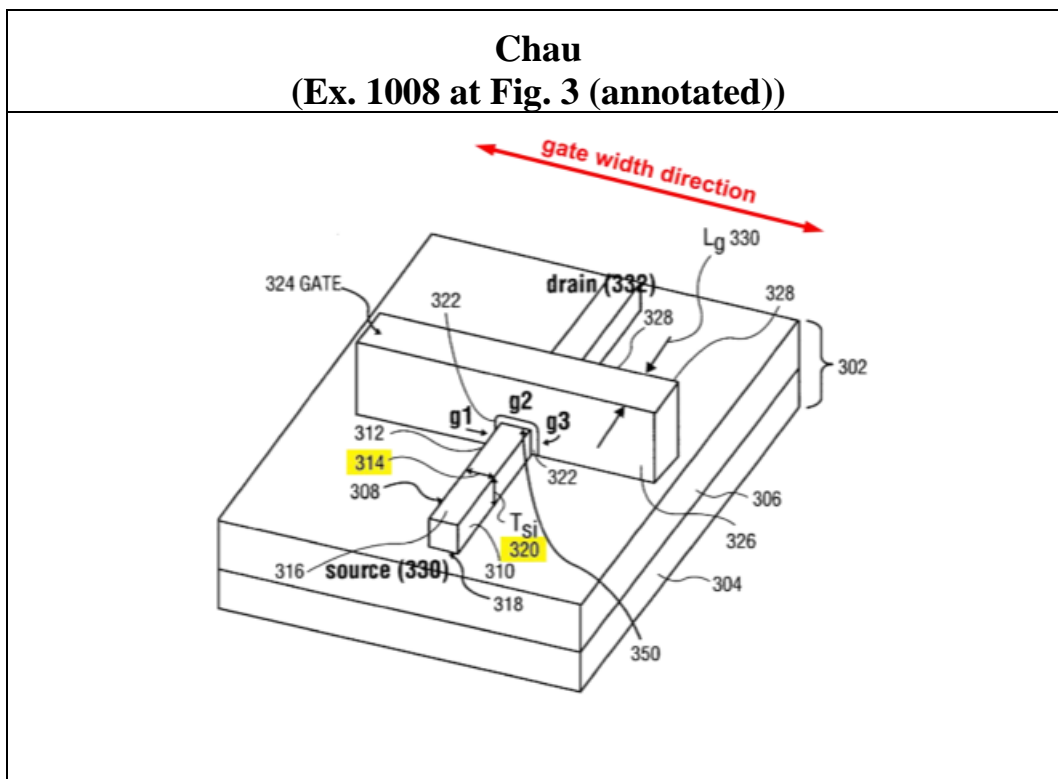
bodies; a gate electrode formed on the gate dielectric on the top surface of each of said plurality of semiconductor bodies and adjacent to said gate dielectrics formed on each of said first and second laterally opposite sidewalls of each of said silicon bodies”).) In other words, the gate electrode is formed on each of the semiconductor regions, with gate insulating film interposed therebetween. (Ex. 1001 ¶272.)



***b. 14[b]: “wherein the gate electrode extends across the plurality of semiconductor regions in a gate width direction.”***

Chau discloses that the **gate electrode 324** extends across the **plurality of fin-shaped semiconductor regions** in a gate width direction. Chau renders obvious that the gate width direction is the direction labeled in Figure 3 because it refers to

gate width dimensions along that axis. (Ex. 1008 at Claim 20 (“gate width of said transistor is approximately the sum of the gate widths of each of said **semiconductor bodies** wherein the gate width of a **semiconductor body** is two times the height of the **semiconductor body** plus the distances between the laterally opposite sidewalls.”) (Ex. 1001 ¶273.)



Chau further discloses that the **gate electrode** extends across the **plurality of fins**, in the gate width direction. (Ex. 1008 at Fig. 4B; *see also id.* ¶31 (“**Gate electrode** 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308.”).) (Ex. 1001 ¶274.)



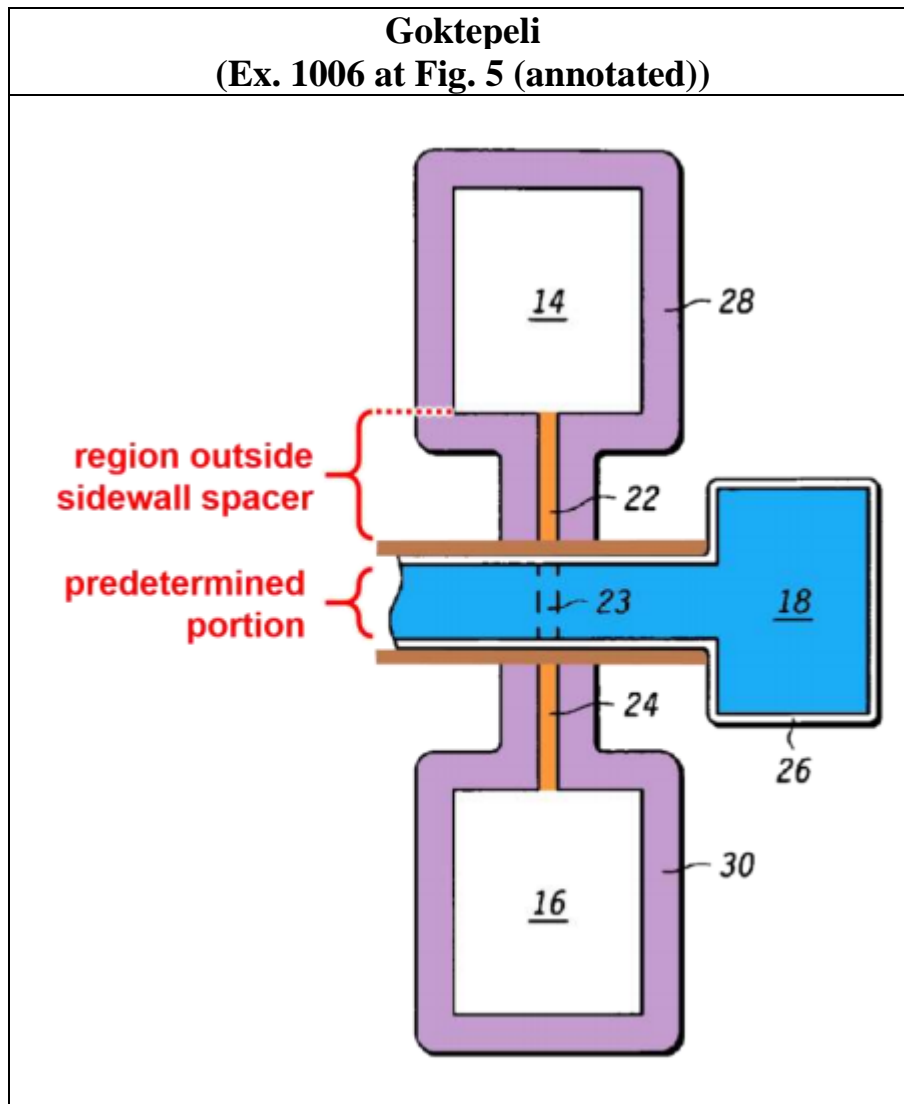


**gate feature** prior to forming the first and second **sacrificial doping layers**.”); *see also id.* at Claim 6 (“The method of claim 1 further comprising forming a **sidewall spacer** adjacent to the **gate feature** prior to the step of forming the first and second **sacrificial doping layers**.”).) A POSITA would have known that in the alternative embodiment using a **sidewall spacer**, the **sacrificial doping layer** would have been formed adjacent to the **sidewall spacer**. (Ex. 1001 ¶276.) This is because the original embodiment discloses the **sacrificial doping layer** is formed adjacent to the **gate feature**. (Ex. 1006 at 6:2–7 (“A first **sacrificial doping layer** is formed on the first side of the **semiconductor fin** between the first source/drain contact region *and the gate feature* and a second **sacrificial doping layer** on the first side of the **semiconductor fin** between the second source/drain contact *and the gate feature*.”).) (Ex. 1001 ¶¶276, 277.)

Goktepli renders obvious **extension regions** that are P-type. Goktepli discloses that for doping by diffusion, dopants diffuse into the **fin** through the surfaces in direct contact. (Ex. 1006 at 4:57–60 (“The heating of semiconductor device 10 causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and thoroughly diffuse into source/drain contact regions 14 and 16.”).) A POSITA would have known dopants from the **sacrificial doping layer** would diffuse into the portion of the **fin** located beneath the **sidewall spacer**, even though the **sacrificial doping layer** was not in direct contact with the **fin**

beneath the **sidewall spacer**. (Ex. 1001 ¶277.) In other words, a POSITA would have known that diffusion of the dopants would not be limited to the portion of the **fin** outside the **sidewall spacer**. (*Id.*) This is because diffusion involves the movement of dopants to a region of lower density, and absent any constraints in the recipient region, the dopants will disperse freely from the point of contact. In this case, those dopants will move freely from the contact point adjacent to the **sidewall spacer**, into the **fin** beneath the **sidewall spacer**. (*Id.*)

Moreover, since the doping of the **fin** outside the **sidewall spacer**, *i.e.*, in the **source-drain region**, is of the second conductivity type, the dopants of the same second conductivity type would diffuse underneath the **sidewall spacer**. Thus, Goktepli renders obvious **first** and **second impurity regions** of a second conductivity type underneath the **sidewall spacer** through its disclosure of diffusion from a **sacrificial doping layer** formed adjacent to the **sidewall spacer**, as shown below in Figure 5. (Ex. 1001 ¶278.)



#### 4. Dependent Claim 16

- a. 16: “The semiconductor device of claim 14, wherein the **first impurity region** and the **second impurity region** are a P-type **source-drain region**.”

As previously discussed, Goktepel in combination with Chau renders obvious claim 14. (See Section X.B.2.) Goktepel further renders obvious that the **first** and **second impurity regions** are a P-type **source-drain region**. Goktepel discloses **first** and **second impurity regions**, i.e., **source-drain regions**. (Ex. 1006 at 2:67–

3:3 (“The **sacrificial doping layer** is selectively or unselectively grown on the vertical device which functions as a dopant source to dope the thin **source/drain regions**, **source/drain extensions**, or the **gate** through solid-phase diffusion of the dopants from the pre-doped **sacrificial doping layer**.”); *see also id.* at 4:57–60 (“The heating of semiconductor device 10 causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to evenly and thoroughly diffuse into source/drain contact regions 14 and 16.”).)

Goktepli further renders obvious that the **source/drain region** is P-type. As previously discussed, a POSITA would have known that to form a PMOS transistor, the **source/drain regions** would have been implanted with P-type dopants. (*See* Section VI.A.4.) Thus, because Goktepli discloses a **source/drain region**, and because a POSITA would have known to implant the **source/drain region** with P-type dopants to form a PMOS transistor, Goktepli renders obvious a P-type **source/drain region**. (Ex. 1001 ¶280.)

## **5. Dependent Claim 17**

- a. 17: “The semiconductor device of claim 13, further comprising a **third semiconductor region** connecting together end portions of the **plurality of semiconductor regions** on each side of the semiconductor regions in a gate length direction.”*

As previously discussed, Goktepli in combination with Chau renders obvious claim 13. (*See* Section X.B.1.) Chau further discloses a **third semiconductor region**, *i.e.*, a **landing pad**. Specifically, Chau describes “**source regions** 330 and



## 6. Independent Claims 18 and 19

- a. 18, 19[preamble]–18, 19[c]: “A semiconductor device, comprising:
- a first semiconductor region of a first conductivity type formed on a substrate and having an upper surface and a side surface;*
- a first impurity region of a second conductivity type formed in an upper portion of the first semiconductor region and made of a semiconductor; and*
- a second impurity region of a second conductivity type formed in a side portion of the first semiconductor region and made of a semiconductor”*

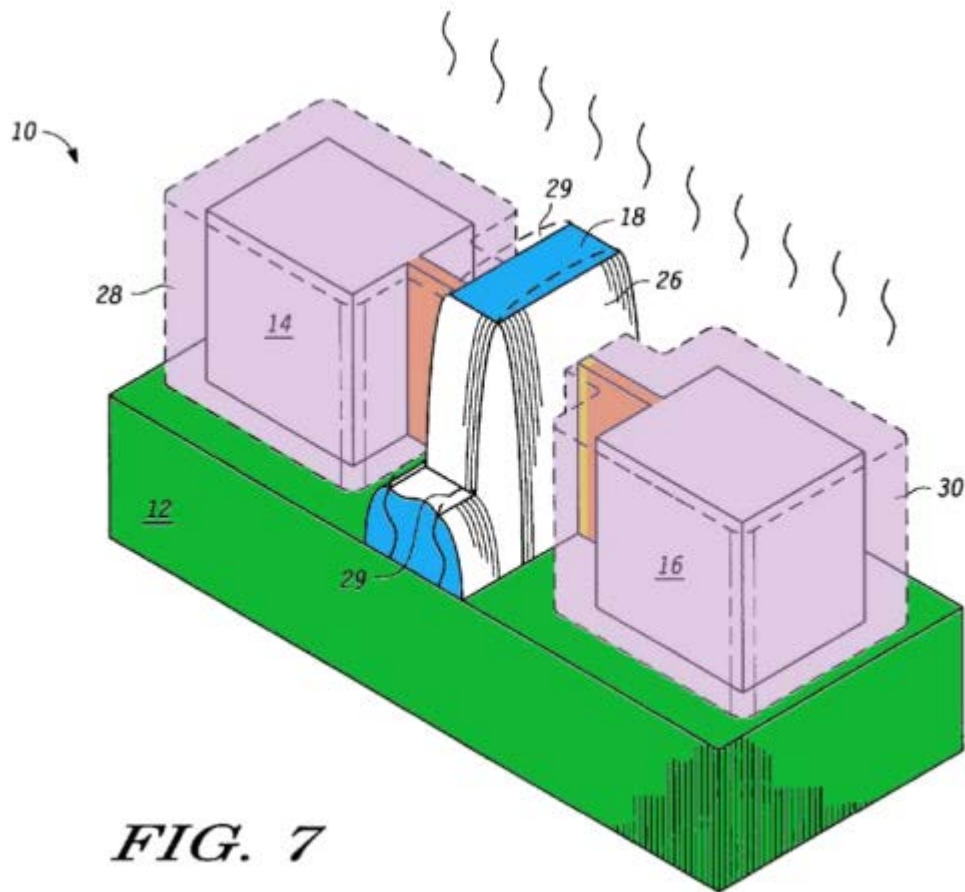
As previously discussed, Goktepli discloses a **first semiconductor region**, *i.e.*, a **silicon fin**, of a first conductivity type formed on a **substrate** having an upper and side surface. (See Section X.B.1.a.) Goktepli further discloses a **first impurity region** formed in an upper portion of a **silicon fin** made of a semiconductor. (See Section X.B.1.b.) Goktepli further discloses a **second impurity region** is formed in a side portion of the **silicon fin** made of a semiconductor. (See Section X.B.1.c.) (Ex. 1001 ¶¶283, 284.)

- b. 18[d]: “[wherein] a sheet resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.”

Goktepli renders obvious that the sheet resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. As previously discussed, Goktepli discloses a uniform resistivity in the **first** and **second impurity regions**. (See Section X.B.1.d.) A POSITA would have known

that, for a constant thickness, sheet resistance is directly proportional to resistivity. (See Section VI.A.5; *see also* Ex. 1009 at 1; Ex. 1001 ¶285.) Goktepli renders obvious a uniform thickness in the **source/drain regions** and **source-drain extension regions**. (Ex. 1006 at 2:67–3:5 (“The **sacrificial doping layer** is selectively or unselectively grown on the vertical device which functions as a dopant source to dope the thin **source/drain regions**, **source/drain extensions**, or the **gate** through solid-phase diffusion of the dopants from the pre-doped **sacrificial doping layer**.”); (*see also id.* at 4:57–60 (heading the **sacrificial doping layer** “causes some of the source/drain dopants present in **sacrificial doping layers** 28 and 30 to *evenly and thoroughly* diffuse into source/drain contact regions 14 and 16.”); *see also id.* at Fig. 7.) (Ex. 1001 ¶286.)

**Goktepli**  
**(Ex. 1006 at Fig. 7 (annotated))**



Because Goktepli renders obvious a uniform thickness in the **source/drain regions** and **source-drain extension regions**, and because as previously discussed Goktepli discloses a uniform resistivity in the **source/drain regions**, a POSITA would have known that the sheet resistance in the upper and side regions of the **source/drain regions** is substantially equal. (Ex. 1001 ¶¶285, 286.)



*c. 19[d]: “[wherein] a spreading resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**.”*

Goktepli renders obvious that the spreading resistance of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. As previously discussed, Goktepli discloses a uniform resistivity in the **first** and **second impurity regions**. (See Section X.B.1.d.) Spreading resistance is the measure of resistance between any two points in or on a layer of material, and it is always directly proportional to resistivity. (See Section VI.A.5.) Thus, if the resistivity of the upper and side impurity regions is substantially equal, and the concentration of implanted ions is uniform (as disclosed by Goktepli (Ex. 1006 at 4:57–60)), a POSITA would have understood that the spreading resistance in the upper and side regions is likewise substantially equal. (Ex. 1001 ¶¶287, 288.)

## **XI. CONCLUSION**

The Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Dated: July 31, 2018

Respectfully Submitted,

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**CERTIFICATE OF COMPLIANCE REGARDING WORD COUNT**

This Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling **13,513** words. Counsel has relied upon the word count feature provided by Microsoft Word.

Dated: July 31, 2018

Respectfully Submitted,

/s/ Gregory S. Arovas

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**Table of Exhibits for U.S. Patent 7,800,165 Petition for *Inter Partes* Review**

<b>Exhibit</b>	<b>Description</b>
1001	Declaration of Stanley Shanfield
1002	Curriculum Vitae of Stanley Shanfield
1003	U.S. Patent No. 7,800,165
1004	U.S. Patent No. 7,800,165 File History
1005	U.S. Patent No. 7,494,862 (“Doyle ’862”)
1006	U.S. Patent No. 7,323,389 (“Goktepli”)
1007	U.S. Patent No. 7,449,373 (“Doyle ’373”)
1008	U.S. Patent Publication No. 2004/0036126 (“Chau”)
1009	Schroder, Dieter K., Semiconductor Material and Device Characterization (3d Ed. 2006) (“Schroder”)

## **CERTIFICATE OF SERVICE**

I hereby certify that on July 31, 2018, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,800,165
- Certificate of Compliance Regarding Word Count
- List of Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 7,800,165 (Exs. 1001–1009)

to be served via Express Mail on the following attorney of record as listed on

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