# UNITED STATES PATENT AND TRADEMARK OFFICE

# **BEFORE THE PATENT TRIAL AND APPEAL BOARD**

INTEL CORPORATION Petitioner

v.

GODO KAISHA IP BRIDGE 1 Patent Owner

**DECLARATION OF STANLEY SHANFIELD, PH.D.** 

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IX.

I, Dr. Stanley Shanfield, declare as follows:

1. My name is Stanley Shanfield.

2. I am an expert in the fields of integrated circuit design, processing, manufacturing, and structures, among other fields. I have over 35 years of experience as a practicing engineer in the field of semiconductor fabrication.

3. My academic training was at the University of California, Irvine, where I received my Bachelor of Science degree in 1977, in Physics. I received my Doctor of Philosophy degree from the Massachusetts Institute of Technology in 1981, with a dissertation on high field superconductors. During my doctoral program at the Massachusetts Institute of Technology, I received a four-year scholarship from the Energy Research and Development Administration, from the Department of Energy.

4. Upon completing my Doctor of Philosophy, I worked until 1984 at Spire Corporation as a Staff Scientist, then later as a Senior Staff Scientist. There, I developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. I also built, operated, and characterized an ion-assisted deposition system for making coatings for semiconductors.

5. In 1985, I joined Raytheon Corporation, where I began as Section Manager, Semiconductors and Integrated Circuits. My work involved developing processes for fabricating high power, high frequency multi-function integrated circuits. In 1992, I became Research Laboratory Manager, where I led a 90employee team, in high performance semiconductor devices and circuits, including measurement, assembly, and wafer fabrication. I was directly involved in the design, fabrication, and measurement of state-of-the-art complementary metaloxide semiconductor ("CMOS") devices of the time, primarily for digital and mixed signal applications. As part of that activity, I developed implant and annealing schedules to optimize lightly doped drain ("LDD") transistor performance, and evaluated various self-aligned gate and source-drain fabrication I led research work that established fabrication processes for two schemes. versions of CMOS FinFET devices used in custom digital and mixed signal integrated circuit ("IC") designs on silicon-on-insulator ("SOI"). These devices utilized a combination of optical and electron-beam lithography, and required multiple angle ion-implantation. At least one version of this process was used in a customized chip set for Raytheon products. In 1996, I became Manager, Semiconductor Operations. In this capacity, I was involved with all aspects of CMOS-based IC fabrication, including the use of production ion implantation and rapid thermal annealing equipment, metallization and dielectric deposition tools, plasma etching equipment, stepper-based photolithography processes, chemomechanical polishing stations, chip singulation methods, etc. I was also responsible for a custom silicon application-specific integrated circuit ("ASIC") design and development group and the associated layout and simulation facilities.

6. Following 14 years at Raytheon, I transitioned to AXSUN Technologies, where I eventually became Vice President, Operations. I designed a complete facility for semiconductor processing, including establishing a fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material. I also raised \$36 million in funding.

7. In 2001, I transitioned to Clarendon Photonics, where I was the Director, Packaging & Integration. Clarendon Photonics began as a 30 person startup company, where we invented and productized new, low cost semiconductor processing and packaging technology. I helped establish assembly and packaging processes.

8. In 2003, I transitioned to the Draper Laboratory at the Massachusetts Institute of Technology ("Draper"), where I have held the position of Division Leader in the Advanced Hardware Development group, and am a Distinguished Member of Technical Staff, and Technical Director. In my time at Draper, I have been responsible for in-house device and module fabrication, and have been involved in CMOS foundry implementation for multiple ASIC designs, including the testing of advanced TSMC processes incorporating FinFET structures.

9. I have been a member of many professional societies and electrical engineering industry groups over the years, such as the Institute of Electrical and

Electronic Engineers (IEEE) and the American Physical Society (APS).

10. I have received a number of academic awards and honors over the years, including awards and honors for the best Draper patent and most successful Draper development project.

11. I have also authored or co-authored over 25 technical papers covering aspects of semiconductor devices, such as hot electron effects in FETs and high frequency transistor design.

12. I am a named inventor or co-inventor on more than nine (9) patents covering aspects of semiconductor devices, such as thin film deposition methods, transistor optimization, and advanced semiconductor processing.

13. Through the course of my educational and professional activities, I am familiar with the state of the field of semiconductor technologies from the late 1990s through at least 2010.

14. A copy of my curriculum vitae (including a list of selected publications, and the patents on which I am a named inventor) is attached as Exhibit 1002.

15. I have been retained as an expert witness in the field of semiconductor device fabrication and design on behalf of Intel Corporation ("Intel") for the above-captioned Petition for *Inter Partes* Review ("IPR") of U.S. Patent No. 7,800,165 (the "165 patent") (Ex. 1003). I am working as an independent

consultant and am being compensated for my time in connection with this IPR at my standard consulting rate of \$385 per hour. My compensation is not affected by the outcome of this matter.

16. I am not currently, and have not at any time in the past, been an employee of Intel.

17. I have no financial interest in Intel. I similarly have no financial interest in the '165 patent, and have had no contact with the named inventors of the '165 patent.

18. I have been asked to provide my opinions regarding whether claims 1-19 (the "Challenged Claims") of the '165 patent are invalid as obvious to a person having ordinary skill in the art at the time of the alleged invention.

19. In preparing this Declaration, I have reviewed the specification, claims, and file history of the '165 patent. I understand that, for purposes of determining whether a publication will qualify as prior art, the earliest date that the '165 patent could be entitled to is January 22, 2007. Even under that earliest priority date, the cited references are prior art and invalidate the '165 patent.

20. In forming the opinions expressed in my Declaration, I relied upon my education and experience in the relevant field of the art, and I have considered the viewpoint of a person having ordinary skill in the relevant art as of the priority date of the '165 patent. In my opinion, a person of ordinary skill in the art for the '165

patent would have found the '165 patent invalid. My opinions are based, at least in part, on my review of the following references:

- U.S. Patent No. 7,494,862 ("Doyle '862") (attached as Ex. 1005)
- U.S. Patent No. 7,323,389 ("Goktepeli") (attached as Ex. 1006)
- U.S. Patent No. 7,449,373 ("Doyle '373") (attached as Ex. 1007)
- U.S. Patent Pub. No. 2004/0036126 ("Chau") (attached as Ex. 1008)

21. I have reviewed the above references and any other publication cited in this declaration.

# I. UNDERSTANDING OF PATENT LAW

22. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

# A. Claim Construction

23. My understanding of claim construction standards is stated in paragraph 69.

## B. Obviousness

24. I have been informed and understand that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

25. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

26. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

 whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;

- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

27. I understand that one of ordinary skill in the art has ordinary creativity, and is not an automaton.

28. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

29. I understand that prior art to the '165 patent includes patents and printed publications in the relevant art that predate the priority date of the '165 patent.

30. I understand that certain factors-often called "secondary

considerations"—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

#### II. SUMMARY OF OPINIONS

31. In my opinion, from the perspective of a person of ordinary skill in the art as of the priority date of the '165 patent, every limitation of the structures described in the Challenged Claims of the '165 patent are disclosed or rendered obvious by the prior art.

# **III. BRIEF DESCRIPTION OF TECHNOLOGY**

32. The '165 patent generally relates to characteristics of a threedimensional semiconductor field-effect transistor. Specifically, the '165 patent claims a semiconductor region with a resistivity in the side portion "substantially equal to or smaller than that" of the top region. '165 patent at Claim 1.

# A. Overview of Transistor Structures

33. Transistors form the basis for integrated devices, such as microprocessors and computer memory. Each individual transistor can act as a switch, turning on to transmit electrical signals. These electrical signals represent data. For example, a transistor that is "on" might represent the binary number "1," and a transistor that is "off" might represent the binary number "0." By turning the transistor "on" or "off," the transistor can communicate data. When electrically connected together, transistors can form electrical circuits. Together, they can perform complex data processing.

#### 1. <u>2D Transistors</u>

34. A planar transistor is a transistor whose components are all formed in the same plane, i.e., within the plane of the **substrate**. As shown in the figures below, planar transistors typically contain three primary parts: (1) a "gate," (2) a "**source**," and (3) a "drain."<sup>1</sup> The gate, source, and drain of a transistor are collectively called its "terminals" or "electrodes." In a planar transistor, the source

<sup>1</sup> Throughout my declaration, I have color-coded structural features for ease of identification.

and the **drain** terminals are formed within the same plane as the silicon **substrate**. The region of the transistor between **source** and the **drain** is known as the "channel" region or "conducting channel." The **gate insulating film** and **gate** typically sit atop the channel region, above the plane of the **substrate**. The diagram below shows the **source**, **drain**, and conducting channel all within the same plane as the **substrate**, hence why these transistors are referred to as two-dimensional, or planar transistors. The figure to the left shows a three-dimensional view of a planar transistor. The figure to the right is a section cut through the three-dimensional view, cut along line A-A.



35. When an appropriate voltage is applied to the **gate** structure shown in the figures above, the voltage causes the channel region to become more

electrically conductive, allowing the current to flow between the **source** and the **drain regions**. In this state, the transistor turns "on." Conversely, when the voltage is removed from the **gate**, the channel region becomes less electrically conductive, impeding the flow of electricity between the **source** and the **drain**, and the transistor turns "off." In other words, the application or removal of voltage to the **gate** can control (or "gate") the flow of electricity between the **source** and the **drain regions** to turn the transistor on or off. In modern day computing devices, these turn on/off events can occur at several billion times per second.

#### 2. <u>3D Transistors</u>

36. The development and commercialization of new technologies drives the need for more and smaller transistors. In 1975, Gordon E. Moore, the cofounder of Intel, set forth Moore's Law. Moore's Law predicts that the number of transistors in integrated circuits doubles approximately every two years. For over four decades, Intel has consistently developed and commercialized new technologies utilizing the so-called "tick-tock" product development cycle that have enabled Dr. Moore's prediction to become a reality.

37. One of the most significant technological advances in this progression was the transition from planar (2D) transistors to three-dimensional (3D) transistor structures. Indeed, Intel itself was the first to commercialize these 3D transistors,

or FinFETs.<sup>2</sup> In a two-dimensional (planar) transistor structure, the **gate** interacts with the channel primarily along a single surface, because the **source region**, **drain region**, and channel regions are formed in the surface of the semiconductor **substrate**. But in a three-dimensional (or FinFET) transistor structure, the **source** and **drain regions** are formed on top of the surface of the semiconductor **substrate**, in a fin shape. In this way, the regions are elevated from the plane of the **substrate**. The **gate** is then formed around three sides of the fin, thereby increasing the interaction area because the **gate** is in contact with three sides of the fin. For example, in the Background of Invention section, Doyle '862 discloses that "three separate gates provide three separate channels for electrical signals to travel, thus effectively tripling<sup>3</sup> the conductivity as compared to a conventional

- <sup>2</sup> FinFET is the generic industry term for a three-dimensional transistor; Intel refers to three-dimensional transistors as Tri-Gate transistors. For the purposes of my declaration, I use the terms interchangeably. If the Patent Owner raises an argument that requires addressing the distinction, I will at that point further address the distinction.
- <sup>3</sup> Although Doyle '862 states that the conductivity will be tripled, this will only hold true if the upper and side regions are approximately equal in length. If the

planar transistor." Doyle '862 at 1:20-22 (Ex. 1005). As a result, the lateral dimension of the transistor along the x-direction shrinks down even further as compared to the planar transistor, but the area of interaction between the **gate** and the underlying channel is still high, allowing the transistors to perform reliably.



## 3. <u>3D Transistor Fabrication</u>

38. The FinFET fabrication method disclosed in the Admitted Prior Art ("APA") of the '165 patent is consistent with my understanding as a person of ordinary skill in the art. '165 patent at 1:36-2:41, Figs. 16A-D, 17A-D (Ex. 1003).

upper and side regions of the fin are not equal in length, the conductivity will be increased, but not necessarily tripled. A fin is formed on a substrate made of semiconducting material, such as silicon. A silicon fin is formed on the semiconductor substrate, for example, by etching, or removing, portions of a flat silicon substrate to form vertically standing fins. Then, a gate insulating film and a polysilicon film are formed on the fin and etched away to leave a gate structure. The entire exposed portion of the fin is lightly doped. Finally, sidewall spacers are formed on the sides of the gate structure, and the remaining exposed portions of fin are ion-implanted to form the source/drain regions. The portions of the fin located underneath the sidewall spacers that received only the initial doping are referred to as extension regions. Figures 17A-D of the '165 patent (which are expressly labeled as Admitted Prior art in the '165 patent) depict these steps.



39. Ion implantation is performed to increase the electrical conductivity of certain portions of a semiconductor region, such as the **source** and **drain regions** in a **fin**. During ion implantation, a manufacturer implants specific atoms—called "dopants" or "impurities"—into portions of the **fin** that the manufacturer wants to be more conductive. Once the dopants are driven into the **fin**, the manufacturer then anneals those dopants by heating them to a high temperature. This heating step activates the dopants. Once activated, the dopants form regions which carry current, i.e., current flowing through the **fin** will flow through the **source** and **drain regions**.

<sup>&</sup>lt;sup>4</sup> All annotations and emphases added unless otherwise noted.

A larger number of implanted ions renders a region more conductive, in other words, less resistant. Conductivity and resistivity are inversely proportional—a region with a higher conductivity or better ability to carry current, will have a lower resistivity, or ability to oppose the flow of current, as discussed below in paragraph 45.

### 4. <u>PMOS and NMOS Transistor Types</u>

40. There are two transistor types that can be fabricated: p-type metaloxide-semiconductor logic ("PMOS") and n-type metal-oxide-semiconductor logic ("NMOS"). The existence of these two transistor types allows "complementary pair" logic to exist in integrated circuit design. With "complementary pair" logic, a transistor can maintain a logic state with nearly zero power consumption. The benefits of low power consumption are more readily seen in circuit designs containing large numbers of logic gates, where the low power feature can be used to obtain benefits.

41. The two types of impurities used as dopants in the fabrication of NMOS and PMOS transistors are "n-type" and "p-type," respectively. The type the dopant is named is based on the type of charge carriers that are present. N-type dopants, such as phosphorus, have more valence electrons than the host lattice. When activated, an n-type dopant displaces a silicon atom in the silicon crystal lattice, bonding with other neighboring silicon atoms. The extra valence electron

remains free and generate a current. P-type dopants, such as boron, have less valence atoms. When placed in the silicon lattice, the p-type dopant has an absence of electrons to form bonds with the lattice, resulting in a "hole," or a positively charged element.

42. The type of impurity used during doping determines the "conductivity type" of an impurity region, such as the impurity regions that form the **source** and **drain regions**, and the impurity regions that form the channel region. For example, a **source** and **drain region** doped with p-type impurities would have a p-type conductivity type, a net positive charge, and be called a PMOS transistor. A **source** and **drain region** doped with n-type impurities would have an n-type conductivity type, a net negative charge, and be called an NMOS transistor. NMOS and PMOS transistors would be used in pairs to create the complementary logic previously discussed.

43. Leakage current can be a problem in FinFETs, where current intended to flow through the **source** and **drain regions** "leaks" through the **fin** and into the **substrate**. Such leakage is undesirable because it is inefficient, leads to unpredictable transistor performance, and can have unintended effects on adjacent transistors once the current travels through the **substrate**.

44. One common method for addressing the problem of leakage current, as well as setting the doping type of the channel region, is "bulk" doping. Bulk

doping refers to an initial light doping of the entire semiconductor region to the opposite type as the final transistor type. For example, to form an NMOS FinFET, before the source and drain regions are doped with n-type dopants, the entire fin is first doped with p-type dopant. Conversely, to form a PMOS FinFET, the entire fin is first implanted with n-type dopant before the source and drain regions are doped with p-type dopants. After initial bulk doping of the entire fin, the manufacturer deposits a gate structure that surrounds three sides of the fin in a specific region of the fin. The gate structure includes three parts: a gate oxide (sometimes called a "gate dielectric"), a gate electrode, and a sidewall spacer on each side of the gate electrode. Before forming the sidewall spacer, the exposed portions of the fin are lightly doped with the same dopant type that will later be used in the source and drain regions. Then, after the sidewall spacer is formed, the source and drain regions are doped (in the portions of the fin not covered by the sidewall spacers). The portions of the fin that are initially bulk doped, then covered by the sidewall spacers, are referred to as extension regions.



45. All of the structures and concepts described up above were wellknown in the art by January 22, 2007.

# 5. <u>Transistor Properties</u>

46. The properties of a doped region can be characterized in several ways. First, resistivity is a material property that measures how strongly a material opposes the flow of electric current. Second, sheet resistance is calculated by dividing the resistivity by the thickness of the material. Third and finally, spreading resistance is the measure of resistance between any two points in or on a layer of material. A person of ordinary skill in the art would know that all three properties are related to each other and proportional. Schroder at 23, 43-44 (Ex. 1009). In other words, a certain ratio in the resistivity between two regions would translate to the same ratio in the sheet resistance and spreading resistance between two regions, if the variables for both regions (such as for example, the thickness of both regions) remained constant.

#### **B.** Overview of the '165 Patent

47. U.S. Patent Application No. 12/025,504 was filed on February 4, 2008, as a continuation application of PCT/JP2008/050253, filed on January 11, 2008, which claims priority to Japanese patent application JP 2007-011572, filed on January 22, 2007. The '165 patent issued from the '504 application.

48. The '165 patent attributes its purportedly inventive aspect to doping the side portions of a **fin** with more (or at least the same amount of) dopants as compared to the top portion of the **fin**. Specifically, the '165 patent states that "[a]ccording to the present invention, it is possible to obtain a semiconductor device including an impurity region in a side portion of a **fin-shaped semiconductor region**, the impurity region having an implantation dose substantially equal to or greater than that in an upper portion of the **fin-shaped semiconductor region**." '165 patent at 9:18-23 (Ex. 1003).

49. According to the '165 patent, doping the side portions of **fins** substantially equal to the top is important because such doping allows for faster flow of charges on all three sides of the **fin**, and therefore increased transistor performance. '165 patent at 9:23-28 ("In other words, it is possible to obtain a semiconductor device including an impurity region having a low sheet resistance in

a side portion of the fin-shaped semiconductor region. Therefore, it is possible to prevent the degradation in the characteristics of a three-dimensional device such as a fin-shaped FET.") (Ex. 1003). However, as described above, this, along with all other claimed structural features, was well known to one of ordinary skill in the art in January 2007.

#### 1. <u>Admitted Prior Art ("APA")</u>

50. The '165 patent contains a "Background Art" section that describes FinFETs and known methods of fabrication, all of which were known to a person of ordinary skill in the art as of the priority date. For example, Figures 16A-D depict a "structure of a conventional fin-shaped FET." '165 patent at 1:36-37, Figs. 16A-D (Ex. 1003). Figures 17A-D show, "step by step, a conventional method for producing a semiconductor device." *Id.* at 2:6-8, Figs. 17A-D. Further confirming that a person of ordinary skill in the art was familiar with FinFETS and their known methods of fabrication, Figures 16A-D, 17A-D, and 18A-B are each expressly labeled "PRIOR ART." *Id.* at Figs. 16A-D, 17A-D, 18A-B.

51. Figures 16A-D show many structural features, all of which were well known in the art at the time of the priority date. *Id.* at Figs. 16A-D.



52. Figure 16A shows a plan view of a FinFET, along with proposed cross-sections A-A (shown in Figure 16B), B-B (shown in Figure 16C), and C-C (shown in Figure 16D). The plan view shows **source** and **drain regions** 103a-d formed in each of a plurality of **fins**, as well as the **sidewall spacers** 106 running along the sides of the **gate electrode** 105. '165 patent at Fig. 16A (Ex. 1003).

53. Figure 16B, which corresponds to the section view cut along line A-A, shows the **gate dielectric** 104a-104d formed around each of the **fins** 103a-103d, interposed between the **gate electrode** and the **fin**. *Id*. at Fig. 16B, 1:36-2:5.

54. Figure 16C, which corresponds to the section view cut along line B-B,

i.e., directly through the **sidewall spacers** 106. The portions of the **fin** under the **sidewall spacers** 106 are the doped **extension regions** 107a and 107b. '165 patent at Fig. 16C (Ex. 1003); *id.* at 1:36-2:5.

55. Figure 16D, which corresponds to the view cut along line C-C, along the length of a fin. This view shows the gate electrode 105, surrounded by the sidewall spacers 106 over the doped extension regions 107a and doped source/drain regions 117a/117b. *Id.* at Fig. 16D, 1:36-2:5.

56. Figures 17A-17D, also all labeled as "prior art," show cross-sectional views cut along the line C-C to illustrate the typical and admittedly well-known manufacturing steps for a FinFET structure. Specifically, the '165 patent states that "FIG. 17A to FIG. 17D are cross-sectional views, showing, step by step, a conventional method for producing a semiconductor device." *Id.* at 2:6-9. The corresponding three-dimensional views of the fabrication steps described in Figures 17A-17D are shown in the right column.



57. As shown in Figure 17A, fabrication begins with the formation and

doping of the fin 103b. Then, a gate insulating film 104b and gate electrode 105 are provided over the doped fin 103b. Then, as shown in Figure 17C, a first doping is carried out to form region 107. After the first doping, a sidewall spacer 106 is deposited, and a second doping is carried out. In this step, the regions outside the sidewall spacer 106 form the source-drain regions 117. In contrast, the '165 patent calls the region below the sidewall spacer 106 an "extension region 107." This final structure is shown in Figure 17D. '165 patent at 2:6-53 (Ex. 1003).

#### 2. <u>Alleged Problem</u>

58. The '165 patent points to the problem of undesirable transistor characteristics resulting from uneven doping of **fins**. The patent further points to Figures 18A and 18B to attempt to identify the basis for the undesirable characteristic of uneven doping in the **fins**. The figures specifically show that with for example, angled implantation, the tops of the **fins** may receive more dopants than the sides of the **fins**.



59. Figure 18A illustrates that angled implantation from two angles results in more dopant deposited on the upper surface of the fin, due to the top surface being exposed during both implantation steps. Figure 18B shows a plasma doping method, where implantation occurs by vertical implantation in the top surface, adsorbed ions on the top and surface, and then desorption of the adsorbed

ions on the top surface (by sputtering). The '165 patent states that with the plasma doping method, the implantation dose of the top surface is approximately 25% higher than that of the side.

60. The '165 patent states that a higher resistivity in the side region than the top region is undesirable in the **source-drain region**, because the presence of localized flow fails to obtain desirable transistor characteristics. '165 patent at 3:58-4:42 (Ex. 1003). Further, because sheet resistance and spreading resistance are proportional to resistivity, the undesirable characteristics resulting from nonuniform resistivity apply equally to non-uniform sheet resistance and spreading resistance.

61. The '165 patent further explains that localized current flow in either the upper or side surfaces of the fin will result in "degradation in the transistor characteristics (e.g., drain current)." *Id.* at 12:39-40.

62. Doyle also explains that "uneven doping of the silicon fin results in a change in resistance of the [subthreshold] current," whereas low off-leakage current is desirable. Doyle '862 at 1:29-32, 1:53-54 (Ex. 1005).

3. <u>Summary of Alleged Invention of the '165 Patent</u>

63. The '165 patent contains 19 claims, four of which are independent. The independent claims (claims 1, 13, 18, and 19) are all directed to a uniformly doped FinFET. Claim 1 measures the resistivity characteristic, claim 13 points to a FinFET with a **plurality of fins**, claim 18 measures the sheet resistance characteristic, and claim 19 measures the spreading resistance characteristic. '165 patent at Claims 1, 13, 18, and 19 (Ex. 1003). The remaining dependent claims all add structural features. These structural features are all found in the prior art and were well known to a person of ordinary skill in the art at the priority date.

64. Despite the '165 patent claiming a "substantially equal" resistivity in the upper and side regions of a semiconductor region, it was well known in the art that uniform doping could lead to optimal transistor performance. This ratio of resistivity between the top and side **fins** is the *only* alleged point of novelty, but there was nothing novel or inventive about the idea. A person of ordinary skill in the art knew well before the priority date that this doping pattern would lead to optimal transistor performance.

## C. Prosecution History

65. The PTO issued two office actions during the prosecution of the application that led to the '165 patent. U.S. Patent No. 7,800,165 File History ("165 patent file history") at 255-59, 263-68 (Ex. 1004). The first required applicant to elect either the claims drawn to a semiconductor device or the claims drawn to a method of manufacturing a semiconductor device, as the claims were in different classes and subclasses. Applicant elected the claims drawn to a semiconductor device.

66. The second office action rejected the original claims under 35 U.S.C. section 103(a) based on U.S. Patent No. 7,238,601 to Mathew et al. ("Mathew"), which teaches a FinFET where a silicide layer forms the top and side regions of the fin. '165 patent file history at 263-68 (Ex. 1004). Applicant overcame the 103(a) rejection simply by noting that Mathew disclosed regions with silicide, rather than an impurity region, and by amending the claims. *Id.* at 285-96. The amended claims recited that the first semiconductor region was "of a first conductivity type," and the first and second impurity regions were "of a second conductivity type" and "made of a semiconductor." *Id.* Applicant also noted that even if the disclosed regions were made of a metal and a p- or n- type semiconductor region. *Id.* The new claims were then allowed. *Id.* at 309-13.

#### IV. LEVEL OF ORDINARY SKILL IN THE ART

67. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

68. In my opinion, a person of ordinary skill in the art at the time of the alleged invention would have a B.S. degree in electrical engineering or computer

science (or equivalent experience) and three years of experience with integrated circuit processing, manufacturing, and device design. Based on my experience in the industry at this time, this was the typical level of experience of persons working in semiconductor fabrication at the time of the alleged invention. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

#### V. CLAIM CONSTRUCTION

69. I understand that claims in an unexpired patent are given their broadest reasonable interpretation in view of the patent specification and the understandings of one having ordinary skill in the relevant art. Additionally, any claim term lacking a definition in the specification is also to be given a broad interpretation. I also understand that the USPTO has proposed replacing the broadest reasonable interpretation standard with the same standard applied in federal district courts and International Trade Commission proceedings, i.e., applying their "ordinary and customary meaning." My opinion does not change regardless of which standard is applied.

## VI. OVERVIEW OF THE PRIMARY PRIOR ART REFERENCES

70. Uniform doping of **fins** in a FinFET was well known before the priority date of the '165 patent. This concept was not novel or inventive. Similarly, the other minor structural features added in the dependent claims were

likewise well known at the priority date.

# A. Overview of Doyle '862

71. Doyle '862 was filed on September 29, 2006 and issued on February 24, 2009. Doyle '862 at Cover (Ex. 1005). I have been informed that it is prior art to the '165 patent under 35 U.S.C. § 102(e). I also understand that Doyle '862 was not considered during the prosecution of the '165 patent.

72. Doyle '862 teaches a method for creating uniformly doped **fins** in a FinFET. Doyle '862 specifically discloses that uniform doping results "in a more efficient transistor," due to even current flowing in the upper and side regions of a **fin**. Doyle '862 at 4:22-23 (Ex. 1005).

73. Doyle '862's uniform doping process begins after a **gate electrode** has been formed on a **silicon fin**. In Figure 3A, the upper surface of the **silicon fin** is doped using, "for example, ionized implantation at  $0^{\circ}$ , i.e., vertical implantation." *Id.* at 3:14-15. At this stage, only the upper surface is doped by implanting ions to a depth d below the surface. *Id.* at 3:17-19, 3:21-22. This creates the **first impurity region**.


74. Next, a conformal layer 170 (for example, made of silicon nitride) is deposited on the **silicon fin**, by, for example, physical vapor deposition. Doyle '862 at 3:25-36, Fig. 3B (Ex. 1005).



75. The conformal layer 170 is then etched away, leaving behind spacers 175 on the sides of the **silicon fin**. This etching can be, for example, by reactive ion etching. Note that these "spacers" are not the "**sidewall spacers**" referred to in the claim language of the '165 patent. The '165 patent claim language refers to spacers formed on the side of the **gate electrode**, not the **fin**. *Id*. at 3:37-42, Fig. 3C.



76. The top surface of the **silicon fin** is then selectively modified, by for example, re-oxidation. Such re-oxidation forms a "mask" on the top surface of the **silicon fin**. The re-oxidation does not affect the **silicon fin**, since the **fin** is protected by the spacers formed in the previous step. Doyle '862 at 3:43-60, Fig. 3D (Ex. 1005).



77. Following re-oxidation, the spacers are removed by isotropic etching.For example, phosphoric acid can remove the spacers. Doyle '862 at 3:61-64, Fig. 3E (Ex. 1005).



78. Finally, following removal of the spacers, the sides of the **fins** are selectively doped. Doping can be by angled implantation (at an angle greater than  $0^{\circ}$ ), or by plasma-induced ion implantation (PLAD). PLAD refers to the process whereby a **substrate** is placed in a plasma field, and the dopants accelerate to and penetrate the surface of a region due to their charges. After implantation of the side regions of the **fin**, the oxide mask 180 can be removed. Doyle '862 at 3:65-4:12 (Ex. 1005).

79. In this way, Doyle masks the top of the **fin** while implanting the sides of the **fin**, resulting in the same doping level on the sides of the **fin** as on the top of the **fin**.



#### **B.** Overview of Goktepeli

80. Goktepeli was filed on July 27, 2005 and issued on January 29, 2008. Goktepeli at Cover (Ex. 1006). I have been informed that it is prior art to the '165 patent under 35 U.S.C. § 102(e). I also understand that Goktepeli was not considered during the prosecution of the '165 patent.

81. Goktepeli identifies problems associated with smaller transistor sizes. Specifically, Goktepeli states that transistors "have difficulty in maintaining high drive current with low leakage while not demonstrating short-channel effects such as leakage and threshold voltage stability." Goktepeli at 1:18-22 (Ex. 1006). Leakage was a particular problem in transistors of smaller gate length because, for a given operating voltage, these transistors are increasingly subject to the generation of "hot electrons" caused by high electric fields in the semiconductor, and these electrons manifest as leakage current.

82. Goktepeli additionally identifies that ion implantation in the source/drain regions and source/drain extension regions can damage the extension region. Goktepeli at 1:63-65 (Ex. 1006). Goktepeli discloses that because the extension region is thin, it is subject to full penetration by implanted ions. *Id.* at 1:64-65. The full penetration in turn can create a polycrystalline extension region, rather than a single crystalline region. *Id.* at 1:65-2:2. A structure of this composition degrades carrier mobility and reduces drive current. *Id.* 

83. Goktepeli proposes doping the **source/drain regions** and **source/drain extension regions** by doping from a **sacrificial doping layer**.

84. Goktepeli first discloses elements of a FinFET that were commonly known at the time, such as "a **substrate** 12, a conformal layer on the **substrate** 12 which is patterned to form source/drain contact regions 14 and 16 and a **fin** 20 which forms **extension regions** 22 and 24, and a **gate feature** 18." *Id.* at 3:12-16. These structural features are shown in Figure 1:



85. Next, Goktepeli discloses sacrificial doping layers 28 and 30 formed around the source/drain contact regions and extension regions. Goktepeli at 4:7-14 (Ex. 1006). Goktepeli further discloses that the sacrificial doping layer can be grown by selective epitaxial growth, which allows growth only on exposed surfaces (i.e., those not covered by the gate feature 18). *Id.* at 4:11-14. The growth, from the view looking down on the FinFET, is shown in Figure 5:



86. Goktepeli discloses that doping via the the sacrificial doping layer in the source/drain regions and source/drain extension regions can use one of two methods: in-situ doping or angled ion implantation. Goktepeli at 4:28-31, 4:33-38 (Ex. 1006).

87. In-situ doping refers to the process of doping as the material is grown. In other words, the epitaxial layer has dopant atoms introduced during its growth. Thus, an already-doped doped **sacrificial doping layer** is formed. The dopants, already present in the **sacrificial doping layer**, then diffuse into the surfaces in contact with the sacrificial doping layer.

88. Angled ion implantation, as previously discussed, involves accelerating dopants towards a surface, where the dopants are driven into a region—in this case, the **sacrificial doping layer**. Once dopants are implanted in the **sacrificial doping layer**, the dopants diffuse into the surfaces in contact with the **sacrificial doping layer**.

89. Regardless of whether in-situ doping or angled ion implantation doping of the sacrificial doping layer is performed, after the dopants diffuse into the source/drain regions and source/drain extension regions via the sacrificial doping layer, the dopants are annealed. Annealing is the process of heating dopants in a semiconductor region.

#### C. Overview of Doyle '373

90. Doyle '373 was filed on March 31, 2006 and issued on November 11, 2008. Doyle '373 at Cover (Ex. 1007). I have been informed that it is prior art to the '165 patent under 35 U.S.C. § 102(e). I also understand that Doyle '373 was not considered during the prosecution of the '165 patent.

91. Doyle '373 teaches a "method of ion implanting for tri-gate devices." Doyle '373 at Title (Ex. 1007). Specifically, Doyle '373's method of ion implantation is directed towards the formation of three regions in a tri-gate transistor, or FinFET. 92. First, Doyle '373 discloses the doping of the main source and drain regions. Doyle '373 at 3:39-40 (Ex. 1007). The main source and drain regions that Doyle '373 refers to are the uncovered portions of the fin, i.e., the portions not covered by the gate structure. *Id.* This is consistent with what a POSITA would have understood the main source and drain regions to be.

93. Second, Doyle '373 discloses the doping of the **tip implant regions**. Doyle '373 teaches that the **tip implant regions** are "shallow, **extension source** and **drain regions** to, for example, reduce punchthrough." *Id.* at 1:11-13. A POSITA would have understood that the terms **tip implant regions** and **extension regions** refer to the same region for several reasons. Doyle '373 discloses that the purpose of the **tip implant regions** is to reduce punchthrough. *Id.* The purpose of an **extension region** is likewise to reduce punchthrough, i.e., reduce short channel effects. Moreover, in a separate application, the same named inventors on the Doyle '373 patent referred to the terms interchangeably. *See* Chau ¶ 23 (referring to "**tip regions** (e.g., **source/drain extensions**)") (Ex. 1008). This explicit disclosure that the terms refer to the same region confirms the disclosure in Doyle '373.

94. Third, Doyle '373 discloses the doping of the halo region. Doyle '373 discloses that the halo region is located underneath the **gate structure**. Specifically, Doyle '373 discloses that "[i]t is the channel region which receives

the halo implant." Doyle '373 at 3:42-43 (Ex. 1007); *see also id.* at 1:13-17, Claim 1.

95. Doyle '373 discloses one embodiment in the form of implanting the halo region, then implanting the **tip region**, and then forming **spacers** on the sides of the **gate structure**. Doyle '373 discloses that the halo implants may be performed first. *Id.* at 4:46-48 ("[T]he halo implants may be performed before the **tip implants**.") Doyle '373 then discloses that after the halo and **tip implants** are performed, "**spacers** are formed on the sides of the **gate structure** 27." *Id.* at 3:47-49. The doping of the **tip implant region** corresponds to the doping of the **first** and **second impurity regions**.



96. The '165 patent shows an allegedly inventive step in the doping of **extension regions**, i.e., the **first** and **second impurity regions**.



97. For the doping of all three regions (main source-drain regions, tip implant regions, and halo regions), Doyle '373 discloses that the best angle at which to perform angled ion implantation is 50-55°. Doyle '373 at 4:10-12 (Ex. 1007). Doyle '373 discloses that such an angle has the best tradeoff between depth of the implant, and concentration of the implant. In other words, performing angled implantation at this angle yields the most uniformly doped regions on the top and the side of the fin. Doyle '373 confirms that this angle is optimal through its disclosure that the transistor has more than a 30% increase in performance than a fin undergoing vertical implantation. *Id.* at 4:13-15.

98. Doyle '373 confirms that like the implantation for the **tip implant regions**, the halo implant should be performed at 50-55°. First, "[t]wo implantations [labeled 30 and 31] are done from one side of the **gate structure** 

27." Doyle '373 at 4:31-33 (Ex. 1007). Second, "[t]wo other implants are done from the other side of the **gate structure**," as shown in Figure 5 labeled 32 and 33. *Id.* at 4:33–36. The third and fourth implantation steps 32 and 33 are performed after the wafer is rotated around a certain angle. *Id.* at 4:38–40. Doyle '373 discloses that the rotation can be  $10^{\circ}$ -45° with a tilt, and recommends the tilt used is again,  $50^{\circ}$ -55°. *Id.* at 4:40–43.



# **D.** Overview of Chau

99. Chau was filed on August 23, 2002 and published on February 26,2004. Chau at Cover (Ex. 1008). I have been informed that it is prior art to the

'165 patent under 35 U.S.C. § 102(b). I also understand that Chau was not considered during the prosecution of the '165 patent.

100. Chau teaches a method for fabricating a fully depleted substrate transistor. Chau ¶ 2 (Ex. 1008). A fully depleted substrate transistor uses a channel depleted of charge when no voltage is applied to the **gate** (i.e., normally off). Charge (for carrying current from **source** to **drain**) is induced in the channel only when the **gate** is biased, a situation that allows for higher switching speed than non-depleted devices.

101. Chau further discloses that the transistor can have uniform source/drain regions. Specifically, Chau discloses that source/drain regions can be formed of "uniform concentration or can include subregions of different concentrations or doping profiles such as **tip regions** (e.g., **source/drain extensions**)." *Id.* ¶ 23. A uniform source/drain region has one level of doping, i.e., one resistivity in the source/drain region. Or a source/drain region can include source/drain extension, which are pockets of lightly-doped regions formed to minimize short channel effects.

102. Chau further discloses a number of structural features in a tri-gate transistor. For example, Chau discloses a tri-gate transistor with a **plurality of fins**. *Id*. ¶ 31. Chau further discloses that each of the **fins** has a **gate electrode** formed on top of a **gate dielectric film** on each of the **fins**. *Id*. Finally, Chau

discloses that in a configuration with a **plurality of fins**, each fin has a **source/drain region**. Chau ¶ 23 (Ex. 1008). These features are shown in Figure 4B:



# VII. SPECIFIC GROUNDS FOR PETITION FOR CLAIMS 1-12

# A. Ground 1: Doyle '862 in Combination with Doyle '373

103. It is my opinion that Doyle '862 in combination with Doyle '373 renders obvious claims 1-11 of the '165 patent.

#### 1. <u>Independent Claim 1</u>

104. Doyle '862 discloses the [preamble] and element [a] of claim 1. A **substrate**, also referred to as a wafer, is a surface on which a FinFET is formed.

Doyle '862 teaches that a "**substrate** 110 can be composed of a single crystal semiconductor material, which can be, for example, silicon or germanium." Doyle '862 at 2:27-29 (Ex. 1005). Doyle '862 further teaches that "**Silicon fin** 115 includes buried section 120." *Id.* at 2:30-31. As seen in Figure 1, fin 115 refers to the entire fin—both the portion formed above the surface of the **substrate**, as well as the portion buried in the **substrate**. Figures 1 and 2 show the fin has both an upper and a side surface, as shown by the portion not buried in the **substrate**.



105. As previously discussed, bulk doping was a common method for addressing the problem of leakage current in FinFETs. In order to bulk dope, the

entire **fin** was first implanted with the opposite type dopant as the final transistor type.<sup>5</sup> For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**. The initial doping further serves to create a functioning transistor with "on" and "off" states.

106. Doyle '862 discloses element [b] of claim 1. As previously discussed, Doyle '862 discloses a uniform doping method. The upper surface of the fin is doped in the first step, and Doyle '862 suggests vertical implantation. Doyle '862 at 3:12-15 (Ex. 1005). Implantation is the process where ions are accelerated into the surface of a fin, and depending on certain variables (such as speed and angle) will penetrate a certain distance into the surface of the fin. Following implantation, the semiconductor containing the ions is annealed, or heated, to a high temperature to activate the ions. Once the dopant is annealed, a doped region of the fin is formed. Vertical implantation refers to implantation 0° from vertical, such that the ions approach the fin perpendicular to the upper surface. The vertical implantation is represented by the arrows labeled 165 in Figure 3A.

<sup>&</sup>lt;sup>5</sup> Often the **substrate** itself has already received bulk doping as part of the wafer manufacturing process.



107. Doyle '862 discloses element [c] of claim 1. The last step of the uniform doping method disclosed by Doyle calls for "selectively dop[ing] sidewalls 150 and 155," or the sides of the **fins**. Doyle '862 at 3:66-67 (Ex. 1005). Doyle '862 teaches that such doping can be done by angled ion implantation, or plasma-induced ion implantation (PLAD). *Id.* at 3:67-4:3, *see also id.* at Claim 10. Angled ion implantation is the same process as described in the preceding paragraph, except the dopants are accelerated toward the **fin** at an angle, as shown by the arrows in Figure 3F. PLAD, as Doyle '862 describes, requires a **substrate** be placed in a plasma field in the presence of dopant atoms. The dopant atoms accelerate towards the surface of the **fin** as a result of proper charges on the dopant atoms and the **fin**. *Id.* at 4:5-8. This angled implantation is represented by the

arrows shown in Figure 3F.



108. Doyle '862 further renders obvious that the **first** and **second impurity regions** are of a second conductivity type. As previously discussed, a POSITA would have known that the **fin** would first be doped to a first conductivity type. The **first** and **second impurity regions** would then be doped to a second conductivity type, of the same type as the overall transistor. For example, Doyle '862 discloses that for PMOS devices, the **source** and **drain regions** are doped with p-type impurities. Doyle '862 at 3:2-4 (Ex. 1005). Doping with dopants of a second impurity type forms impurity regions that are of a second conductivity type.

109. Doyle '862 further renders obvious that the impurity regions are made of a semiconductor. A semiconductor is a material (for example, silicon) that can be doped to transform into one of two distinct types of conductors: n-type and ptype. If the regions were not made of a semiconductor, current would not be able to flow through them.

110. In order to achieve optimal transistor performance, a person of ordinary skill in the art would have known that the top and sides of a **fin** should be doped uniformly using the same dopant type. Doping uniformly with the same dopant type on the top and side of the **fin** creates uniform current flow. This minimizes unwanted effects, such as sub-threshold leakage current and results in optimal transistor performance. For example, for a PMOS transistor device, the **source/drain regions** would be uniformly doped on all sides with p-type dopants.

111. Doyle '862 discloses limitation 1[d], that the resistivity of the second impurity region is substantially equal to or smaller than that of the first impurity region. Doyle '862 discloses that after the doping steps are completed, "the current flowing, or 'wrapping around,' silicon fin 115 should be uniform which results in a more efficient transistor." Doyle '862 at 4:21-23 (Ex. 1005). A POSITA would have understood this to mean that because the current is uniform in the fin, the resistivity of the fin is uniform. In other words, the resistivity of the doped upper portion of the fin is equal to the resistivity on each side of the fin, because resistivity is a characteristic that controls current flow.

112. Resistivity is a product of the depth and concentration of the implant.Doyle '862 discloses a uniform depth to which the dopants are implanted into the

top and sides of the **fin**. As shown in Figure 4, the dopants are implanted to a depth "d" on all three sides of the **fin**. Doyle '862 at Fig. 4 (Ex. 1005). Doyle '862 discloses that the ions in the top surface can be implanted to a depth "from about 20 angstroms (Å) to about 200 Å." *Id*. at 3:23-24. Doyle '862 then discloses that the ions in the side surfaces can be doped "from about 10 Å to about 100 Å." *Id*. at 4:9. Concentration of ions can be controlled by changing certain parameters during doping processes. With implantation, for example, changing acceleration voltage and ion beam current affects the concentration of the implanted dopants. Thus, by changing the depth, and concentration of implants, a POSITA can achieve the same resistivity on the upper and side surfaces of a **fin**, such that the resistivity is substantially the same in each.

113. Non-uniform doping of the **source-drain regions** creates undesirable transistor characteristics. A single FinFET can be viewed as three MOSFETs connected in parallel, a "top" horizontally oriented FET, and a "left" and "right" FET on each side of the **fin**. Each of these MOSFETs will perform optimally, with minimal short-channel effects, when they have the same doping profile<sup>6</sup> in the **source-drain** contact **region**. If any of the parallel FETs are not doped optimally,

<sup>6</sup> This profile measures doping versus depth from the respective horizontal or vertical surface and, doping versus distance from the edge of the gate.

they degrade the overall operation of the FinFET.

# 2. Dependent Claims 2-4

114. Because claims 2, 3, and 4 all depend from claim 1, I will address them together in this section.

115. Claims 2, 3, and 4 all depend from claim 1. As described above, Doyle '862 renders obvious each and every limitation of claim 1.

116. Doyle '862 renders obvious claim 2, that the width of impurity region in the side surface is substantially equal to or greater than the width of the impurity region in the upper surface, where the width is measured perpendicular to the face. A width along a direction perpendicular to a surface is a depth. This is because a surface spans in two directions (for example, along x and y axes), and therefore the only direction that can be perpendicular to that surface is along the third remaining axis (for example, the z axis). Thus, for a side surface of the **first semiconductor region**, a width along a direction perpendicular to the surface refers to the depth. Similarly, a width along a direction perpendicular to the upper surface refers to a depth below the upper surface.

117. Doyle '862 discloses impurity regions with the same depth on the top and side of the fin. Figure 4 refers to the depth on the top and side surfaces using the same variable - "d." Doyle '862 at Fig. 4 (Ex. 1005). And Doyle '862 refers to the depth of all three surfaces expressly using the same variable: "As can be seen, silicon fin 115 is uniformly doped by ions 190 to a depth d below surfaces 150, 155 and 160." Doyle '862 at 4:16-18 (Ex. 1005). Doyle '862 therefore discloses the same depth impurity region on all three exposed sides of the fin - the top and sides.



118. Doyle '862 also provides dimensions for the depth of dopant in each of the surfaces. Doyle '862 states that the "depth d of the dopants in top surface 155 can be from about 20 angstroms (Å) to about 200 Å." Doyle '862 at 3:22-24 (Ex. 1005). Doyle '862 also states that the "depth d of the dopants in sidewalls 150 and 155 can be from about 10 Å to about 100 Å." *Id.* at 4:8-9. Thus, the depth in the top surface could be 20 Å, and the depth in the side surface could be

50 Å, as disclosed by Doyle '862. The results would be that the depth of the side surface would be greater than that of the top surface.

119. Doyle '862 renders obvious claim 3, that the **first semiconductor region** is a **fin** shape. A POSITA would understand a "**fin**" shape as being a substantially rectangular shape, and indeed, such shapes were the basis for the label "FinFET." Doyle '862 discloses such a **fin** shape by disclosing two sets of perpendicular walls. Doyle '862 at 2:54-58 (Ex. 1005) (disclosing a top surface, with two perpendicular sidewall surfaces); *see also id.* at Fig. 1 (depicting what a person of ordinary skill in the art would have identified as a "**fin**" shape).



120. Doyle '862 renders obvious claim 4, that the first semiconductor

**region** is formed on an insulating layer on the **substrate**. Doyle '862 discloses a silicon on insulator **substrate**. Doyle '862 at 2:22-23 (Ex. 1005); *see also id.* at Fig. 1. A silicon on insulator **substrate** refers to a **substrate** that has an insulating layer formed on it, that then has a **fin** formed on top of the insulating layer. The purpose of the insulating layer is to prevent any leakage current from the bottom of the **fin** flowing into the **substrate**. Such leakage current has the undesired effect of affecting nearby transistors formed on the same **substrate**. Therefore, an insulating layer helps to prevent this leakage and keep the current within the intended path.



#### 3. Dependent Claim 5

121. Claim 5 depends from claim 1. As described above, Doyle '862 renders obvious each and every limitation of claim 1.

122. Doyle '862 renders obvious element [a] of claim 5. Doyle '862 discloses a **gate insulating film**, formed on a side surface of the **first semiconductor region**. The purpose of a **gate insulating film** is to electrically isolate the **gate electrode** from the underlying **source/drain regions**, and prevent current flow from the gate into the **source/drain regions**. As a result, the **gate can** control the large **source/drain** current underneath it while requiring almost no power (where power is equal to current times voltage). Because the purpose of the **gate insulating film** is to provide an insulating layer between the **gate electrode** and the **fin**, and because the **gate electrode** wraps around the **fin** on three sides, the **gate insulating film** necessarily is formed on the side of the **fin**. Figure 2 of Doyle '862 confirms this configuration.



123. Doyle '373 likewise renders obvious a **gate insulating film**, formed on a side surface of the **first semiconductor region**. Doyle '373 discloses that a **gate structure** wraps around the **fin**. Doyle '373 at 3:36-37 (Ex. 1007). Figure 3 indeed shows such a **gate structure** wrapping around the **fin**.



124. Doyle '373 renders obvious that the **gate structure** has a **gate insulating film** formed between it and the fin. A POSITA would have known that in order to insulate the **gate structure** from the current passing through the fin, a **gate insulating film** would have to be formed therebetween.

125. In semiconductor manufacturing, the structural elements of a transistor are precisely determined prior to fabrication, in order to ensure that a final transistor meets a customer's specifications. This includes for example, the exact location, and dimensions of a **gate insulating film** on a **fin**, and the size and position of the **gate electrode**, formed over the **gate insulating film**. Without knowing the exact placement of the **gate insulating film** on the **fin**, a transistor cannot meet customer specifications. The **gate insulating film** is therefore formed on the **fin** in a predetermined portion of the **fin**.

126. Doyle '862 discloses element 5[b], that a gate electrode is formed on

the **gate insulating film**. Because the purpose of the **gate insulating film** is to insulate the **fin** from the **gate electrode**, the **gate electrode** must be formed on top of the insulating film in order for the film to be effective. Figure 2 of Doyle '862 further confirms that the **gate insulating film** 130 is formed between the **fin** 115 and **gate electrode** 105.



127. Doyle '862 renders obvious element 5[c], that the first and second impurity regions are formed in another portion of the fin other than the predetermined region. As previously mentioned, the gate insulating film, and gate electrode on gate insulating film, are formed in a predetermined region on

the fin, according to customer specifications. Because the portion of the fin covered by the gate insulating film and gate electrode form the channel region, the portions of the fin not covered by the gate insulating film and gate electrode comprise the source and drain regions of the fin. Doyle '862 discloses that the source and drain regions are doped to uniform resistivity. The source and drain regions are in the portions of the fin, outside the predetermined portion covered by the gate insulating film and the gate electrode. I have annotated Figure 2 of Doyle '862 to demonstrate the portions of the fin, located outside the predetermined region (i.e., where the gate insulating film and gate electrode are formed). The arrows are annotated to demonstrate the first and second impurity regions located within the source and drain regions.



128. Doyle '373 likewise renders obvious first and second impurity regions formed outside of the predetermined portion. A POSITA would have known that extension regions, or tip implant regions, as Doyle '373 calls out, refer to the regions located beneath the sidewall spacers. Sidewall spacers are formed on the sides of the gate structure. Because the extension regions are located below the sidewall spacers, which are next to the gate structure, Doyle '373 renders obvious that the uniformly-doped extension regions are not formed in the predetermined region where the gate structure is located.

129. A POSITA would have been motivated to combine Doyle '862 with Doyle '373 for several reasons. First, both address the same problem. Doyle '862 notes the problems associated with nonuniform doping of the silicon fin in FinFETs. For example, Doyle '862 states that "uneven doping of the silicon fin results in a change in resistance of the current." Doyle '862 at 1:53-54 (Ex. 1005). Doyle '373 notes that among the fabrication challenges for tri-gate transistors is the "difficulty of *optimizing* the **tip** and halo implantation profiles in this three-dimensional structure." Doyle '373 at 1:63-67 (Ex. 1007). Thus, both Doyle '862 and Doyle '373 address the same problem of nonuniform doping—Doyle '862 in the **source-drain regions**, and Doyle '373 in the **extension regions**.

130. Nearly the same group of inventors addressed the problems contemplated by both pieces of prior art. Doyle '862 lists named inventors as Brian Doyle, Robert Chau, Suman Datta, and Jack Kavalieros. Doyle '862 at cover (Ex. 1005). Doyle '373 lists as inventors Brian S. Doyle, Suman Datta, Jack T. Kavalieros, and Amlan Majumdar. Doyle '373 at cover (Ex. 1007). Thus, three of the same inventors are listed on both.

131. Both pieces of prior art further have the same assignee: Intel Corporation. Doyle '862 at cover (Ex. 1005); Doyle '373 at cover (Ex. 1007).

132. A POSITA would have known that a transistor with optimal characteristics would have uniform doping in the **source-drain regions**. **Source-drain regions** with nonuniform doping have less desirable characteristics than **source-drain regions** with uniform doping. The FinFET can be considered three FETs in parallel: one "FET" results from current flowing on the top surface of the

fin, while the other two "FETs" result from current flow on the two sides of the fin. If the source-drain region of the FET in the upper region ("top FET") of the fin is more heavily doped than the source-drain regions in the two sides of the fin ("side FETs"), the top FET will turn "off" or "on" at a difference gate voltage than the two side FETs. This results in the combination of the three FETs in parallel not switching "off" or "on" as quickly as FETs with identical source-drain doping. Thus, uniform doping of the source-drain regions leads to optimal device behavior.

133. A POSITA would further have known that uniform doping of the extension regions leads to optimal transistor performance. The purpose of doping the extension regions is to minimize the channel length underneath the gate electrode, which both increases the operation speed and, because of the region of lower doping, minimizes short channel effects. Short channel effects become important when gate length is reduced, since reduced gate length without extension regions leads to disproportionately high electric fields at the gate edges, generating excessive source-drain current. The excess current is undesirable, as it causes excessive heating and wastes power.

134. Fabrication of transistors includes the steps of doping the sourcedrain regions and the extension regions. A POSITA would have known that doping of each of these regions could be performed by any number of doping
methods, including implantation or diffusion. Utilizing the methods for doping the **source-drain regions** and the **extension regions** proposed by Doyle '862 and Doyle '373, respectively, is a simple substitution of known methods. Such a substitution yields the predictable result of a transistor with uniformly-doped **source-drain regions** and **extension regions**, which for reasons previously discussed would lead to optimal transistor characteristics.

135. Combining the methods disclosed by Doyle '862 and Doyle '373 would have been obvious to a POSITA. Because a POSITA would have known that uniform doping leads to optimal transistor characteristics for the reasons previously discussed, it would have been obvious to a POSITA to use methods for doping both the **source-drain regions** and **extension regions** that would lead to uniformly-doped regions. Also as previously discussed, a POSITA would have found it obvious to combine the two pieces of prior art because of the common inventors on each, and the common assignee, and the fact that both prior art address the same problem.

### 4. <u>Dependent Claim 7</u>

136. Claim 7 depends from claim 5, which depends from claim 1. As discussed above and below, Doyle '862 in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

137. Doyle '373 discloses the remaining elements of claim 7, that the

extension regions are P-type. As previously discussed, Doyle '373 refers to extension regions as tip implant regions. Doyle '373 further discloses that the tip implant regions are doped with dopants of the opposite conductivity type as the halo, or channel implant. Doyle '373 at 4:16-17 (Ex. 1007). A POSITA would have understood that the halo region is added to each end of the channel to create a more abrupt transition from the channel region doping to the opposite type sourcedrain doping. This abrupt transition further enhances the ability of the extension region to reduce short channel effects. Because a POSITA would further understand that the purpose of the extension regions is to shorten the channel length, a POSITA would have understood that the extension regions would be of the same conductivity type as the source-drain regions. Thus, for a PMOS FinFET, a POSITA would have understood that the source-drain regions, and extension regions, would both be p-type.

#### 5. Dependent Claim 8

138. Claim 8 depends from claim 5, which depends from claim 1. As discussed above and below, Doyle '862 in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

139. Doyle '862 discloses the further limitation of claim 8[a], that a sidewall spacer is formed on a side surface of the gate electrode. Doyle '862 specifically states that the gate structure is "protected by a spacer formation

formed on the **gate** sidewall (not shown)." Doyle '862 at 3:56-58 (Ex. 1005). For reference, the Admitted Prior Art of the '165 patent confirms that the **sidewall spacer** disclosed by the '165 patent is located on the sidewall of the **gate structure**, precisely where Doyle '862 discloses.



140. Doyle '862 discloses limitations 8[b] and 8[c]. As previously discussed, Doyle '862 discloses a uniform doping method, which involves two separate doping steps, for the upper and side surfaces. First, the upper surface is doped by vertical implantation. Second, the side surfaces are selectively doped, such as by angled implantation or PLAD. Doyle '862 therefore discloses the formation of a **third impurity region** formed in an upper portion of a **fin** (i.e., the doped region in the upper surface formed by vertical implantation), and the formation of a **fourth impurity region** formed in a side portion of the **fin** (i.e., the

doped region in the side surface formed by selective doping, such as angled implantation or PLAD). These regions are annotated in the figure below.



141. Doyle '862 discloses limitation 8[d], that the first and second impurity regions are formed in the fin under the sidewall spacer and provided in the other portion of the first semiconductor region. Doyle '862 discloses a sidewall spacer, although it does not show the location of the sidewall spacer in its figures. Doyle '862 at 3:56-58 (Ex. 1005). Specifically, Doyle '862 explains that "re-oxidation does not affect the gate structure 105 because it is protected by a spacer formation formed on the gate sidewall (not shown)." *Id.* Thus, although

the figures in Doyle '862 do not show a **sidewall spacer**, Doyle '862 nevertheless expressly discloses that one would be formed on the side surface of the **gate** electrode. Given that the purpose of a **sidewall spacer** is to protect the doped extension region on each side of the **gate electrode** from doping performed to the source/drain regions, this is unsurprising, and is not considered to be part of Doyle '862's novel invention of a uniform doping method.

142. Doyle '373 likewise discloses limitation 8[d]. As previously discussed, Doyle '373 discloses a method for doping the extension regions, and a POSITA would have known that the extension regions are located outside the gate electrode, since they are located beneath the spacers formed on the side of the gate electrode.

143. Doyle '862 renders obvious limitation 8[e]. A POSITA would have known that the **third** and **fourth impurity regions** referred to in claim 8 refer to the upper and side portions of the **fin** in the **source/drain regions**. Limitation 8[e] states that the **third** and **fourth impurity regions** are formed in the **fin**, and imposes two further limitations: that they are located "outside of the insulative **sidewall spacer**" and are "in the other portion" of the **fin**. With regard to the former, a POSITA would have realized that the **fin** portions located outside the insulative **sidewall spacer**, i.e., not underneath the **sidewall spacer**, could only refer to the **source/drain regions**, or the channel region (the portion of the **fin**  located underneath the **gate insulating film** and **gate electrode**). The second limitation further narrows where a POSITA would have understood the **third** and **fourth impurity regions** to be. Claim 8 depends from claim 5, which sets forth that the "predetermined portion" is where the **gate insulating film** is formed. A POSITA would have understood that the "other" portion means outside the "predetermined portion" of the **gate insulating film**. Therefore, because claim 8 states that the **third** and **fourth impurity regions** are not the **extension regions**, and are not located underneath the **gate insulating film** in the "predetermined portion," they must be in the **source/drain regions**. And as previously discussed, Doyle '862 discloses a method for doping the **source/drain regions**.



# 6. <u>Dependent Claim 9</u>

144. Claim 9 depends from claim 8, which depends from claims 5 and 1. As discussed above and below, Doyle '862 in combination with Doyle '373 renders obvious each and every limitation of claims 1, 5, and 8.

145. Doyle '862 renders obvious the additional limitation of claim 9, that the **third** and **fourth impurity regions** referred to in claim 8 are p-type **sourcedrain regions**. As previously discussed, a POSITA would have known that the **third** and **fourth impurity regions** refer to the **source/drain regions**. Doyle '862 discloses a method for doping **source/drain regions**.

146. Doyle '862 further discloses a PMOS transistor device. Doyle '862 at

3:2-4 (Ex. 1005). Doyle '862 then discloses that for a PMOS transistor device, the "**source** and **drain region** are typically doped with p-type impurities, such as boron." *Id*. Doyle '862 therefore discloses that the **third** and **fourth impurity regions**, located in the **source/drain regions**, are a p-type **source/drain region**.

#### 7. <u>Dependent Claim 10</u>

147. Claim 10 depends from claim 5, which depends from claim 1. As discussed above, Doyle '862 in combination with Doyle '373 renders obvious each and every limitation of claims 5 and 1.

148. Doyle '862 discloses the additional limitations of element 10[b], that the first and second impurity regions are formed outside the sidewall spacer and not underneath the gate electrode. As previously discussed, Doyle '862 discloses a method for doping the source-drain regions. The source-drain regions are located outside the gate electrode. Doyle '862 discloses that doping of the source-drain regions occurs on either side of the gate. Doyle '862 at 4:23-36 (Ex. 1005). Doyle '862 further discloses that the sidewall spacer is formed on the side of the gate electrode, and thus the extension region located beneath the sidewall spacer is likewise not under the gate.



### 8. <u>Dependent Claim 11</u>

149. Claim 11 depends from claim 5, which depends from claim 1. As previously discussed, Doyle '862 in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

150. Doyle '862 renders obvious claim 11, that the **first impurity region** and the **second impurity region** are a p-type **source-drain region**. A PMOS transistor device is so named because the **source** and **drain regions** of a PMOS transistor device are doped with p-type dopants, such as boron, for example. Doyle '862 discloses so. Doyle '862 at 3:2-4 (Ex. 1005) ("For PMOS transistor devices, the **source** and **drain region** are typically doped with P-type impurities.").

Since Doyle '862 discloses that the **first** and **second impurity region** comprise the **source drain regions**, and Doyle '862 discloses that the **source drain regions** contain p-type impurities, Doyle '862 therefore discloses that the **first** and **second impurity regions** are P-type **source drain regions**. These regions are annotated below in Doyle '862 Figure 2.



# B. Ground 2: Goktepeli in Combination with Doyle '373

151. It is my opinion that Goktepeli in combination with Doyle '373 renders obvious claims 1 and 3-12 of the '165 patent.

### 1. Independent Claim 1

152. Goktepeli discloses the [preamble] and element [a] for claim 1. Goktepeli discloses a fin formed on a substrate. "Illustrated in FIG. 1 is a semiconductor device 10 comprising a **substrate** 12, a **conformal layer** on the **substrate** 12 which is pattered to form source/drain contact regions 14 and 16 and a **fin** 20 which forms **extension regions** 22 and 24, and a **gate feature** 18." Goktepeli at 3:12-16 (Ex. 1006). These features are shown in the annotated Figure 1 below.



153. Goktepeli appears to refer to the entirety of regions 22 and 24 as the "extension regions." On the other hand, the '165 patent refers to the extension region as the portion of the fin located beneath a sidewall spacer. Because the

**sidewall spacer** is formed adjacent to the **gate electrode**, the majority of regions 22 and 24 would have been viewed as a **source/drain region**, whereas the portions of the **fin** under the **sidewall spacer** adjacent to the **gate electrode** would be referred to as the **extension regions**. For the purpose of this petition, the definition from the '165 patent is used, and the "thin **source/drain regions**" 20 are the same **source/drain regions** referred to by the '165 patent.

154. Goktepeli discloses that the **first semiconductor region** is a "fin." *See, e.g.*, Goktepeli at 21-22 (Ex. 1006). A POSITA would have known that a **fin** is a rectangular shape with an upper and side surface. Figure 1 confirms.



155. As previously discussed, bulk doping was a common method for addressing the problem of leakage current in FinFETs. In order to bulk dope, the entire **fin** was first implanted with the opposite type dopant as the final transistor type.<sup>7</sup> For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The

Often the substrate itself has already received bulk doping as part of the wafer manufacturing process.

purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**.

156. Goktepeli further renders obvious that the **first** and **second impurity regions** are of a second conductivity type. As previously discussed, a POSITA would have known that the **fin** would first be doped to a first conductivity type. The **first** and **second impurity regions** would then be doped to a second conductivity type, of the same type as the overall transistor. For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**. Doping with dopants of a second impurity type forms impurity regions that are of a second conductivity type.

157. Goktepeli discloses element [b] of claim 1. Goktepeli discloses a uniform doping method, by forming a sacrificial doping layer over the sourcedrain extensions and source/drain regions. Goktepeli at 4:29-31 (Ex. 1006). Goktepeli discloses that the formation of the sacrificial doping layer can be on "exposed semiconductor surfaces." *Id.* at 4:13-14. Since the upper region of the fin is exposed, a POSITA would have known that the sacrificial doping layer would have been formed over the upper portion of the **fin**, leading to doping of the upper portion of the **fin** (either by diffusion or by angled ion implantation of the **sacrificial doping layer**). Figure 7 confirms that the **sacrificial doping layer** is formed over the upper region of the **source-drain extensions** and **source/drain regions**.



158. Goktepeli discloses element [c] of claim 1. Goktepeli discloses a uniform doping method, by forming a sacrificial doping layer over the sourcedrain extensions and source/drain regions. Goktepeli at 4:29-31 (Ex. 1006). Goktepeli discloses that the formation of the **sacrificial doping layer** can be on "exposed semiconductor surfaces." *Id.* at 4:13-14. Since the side region of the fin is exposed, a POSITA would have known that the **sacrificial doping layer** would have been formed over the side portion of the fin, leading to doping of the side portion of the fin (either by diffusion or by angled ion implantation of the **sacrificial doping layer**). Figure 7 confirms that the **sacrificial doping layer** is formed over the side region of the **source-drain extensions** and **source/drain regions**.



159. Goktepeli further renders obvious that the impurity regions are made of a semiconductor. A semiconductor is a material (for example, silicon) that can be doped to transform into one of two distinct types of conductors: n-type and ptype. If the regions were not made of a semiconductor, current would not be able to flow through them.

160. In order to achieve optimal transistor performance, a person of ordinary skill in the art would have known that the top and sides of a **fin** should be doped uniformly using the same dopant type. Doping uniformly with the same

dopant type on the top and side of the **fin** creates uniform current flow. This minimizes unwanted effects, such as sub-threshold leakage current and results in optimal transistor performance. For example, for a PMOS transistor device, the **source/drain regions** would be uniformly doped on all sides with p-type dopants.

161. Goktepeli discloses limitation 1[d], that the resistivity of the second **impurity region** is substantially equal to or smaller than that of the **first impurity** region. Goktepeli discloses that the sacrificial doping layer is formed over the upper and side regions of the source-drain extensions and source/drain regions, following which the dopants diffuse into the source-drain extensions and source/drain regions. Goktepeli at 2:67-3:5, 4:57-60 (Ex. 1006). Goktepeli specifically discloses that the dopants diffuse into the regions "evenly and thoroughly," *id.* at 4:59-60, which a POSITA would have understood to mean uniformly in the upper and side regions. Resistivity is a product of the depth and concentration of the implant. Doping by diffusion distributes dopants to a uniform depth across all surfaces, with a uniform concentration across all surfaces. Thus, Goktepeli's disclosure of doping by diffusion renders obvious a uniform resistivity of the first and second impurity regions.

162. Non-uniform doping of the **source-drain regions** creates undesirable transistor characteristics. A single FinFET can be viewed as three MOSFETs connected in parallel, a "top" horizontally oriented FET, and a "left" and "right"

FET on each side of the **fin**. Each of these MOSFETs will perform optimally, with minimal short-channel effects, when they have the same doping profile<sup>8</sup> in the **source-drain** contact **region**. If any of the parallel FETs are not doped optimally, they degrade the overall operation of the FinFET.

#### 2. Dependent Claims 3-4

163. Because claims 3 and 4 depend from claim 1, I will address them together in this section.

164. Claims 3 and 4 depend from claim 1. As described above, Goktepeli renders obvious each and every limitation of claim 1.

165. Goktepeli renders obvious claim 3, that the **first semiconductor region** is a **fin** shape. A POSITA would understand a "**fin**" shape as being a substantially rectangular shape, and indeed, such shapes are depicted in the figures. *See, e.g.*, Goktepeli at Fig. 1 (Ex. 1006). In addition, Goktepeli refers to the region as a "**fin**." *See, e.g.*, *id.* at 2:46-47.

166. Goktepeli renders obvious claim 4, that the **first semiconductor region** is formed on an insulating layer on the **substrate**. A silicon on insulator **substrate** refers to a **substrate** that has an insulating layer formed on it, that then

<sup>8</sup> This profile measures doping versus depth from the respective horizontal or vertical surface and, doping versus distance from the edge of the gate.

has a **fin** formed on top of the insulating layer. The purpose of the insulating layer is to prevent any leakage current from the bottom of the **fin** flowing into the **substrate**. Such leakage current has the undesired effect of affecting nearby transistors formed on the same **substrate**. Therefore, an insulating layer helps to prevent this leakage and keep the current within the intended path. Such a configuration was well known in the prior art, and indeed, even Goktepeli references this well-known feature. Goktepeli at 1:35 ("SOI (silicon on insulator)") (Ex. 1006); *id.* at 3:43-45 ("silicon-on-insulator (SOI)").

#### 3. <u>Dependent Claim 5</u>

167. Claim 5 depends from claim 1. As described above, Goktepeli renders obvious each and every limitation of claim 1.

168. Goktepeli further renders obvious element [a] of claim 5. Goktepeli discloses that a **gate dielectric** is formed between a **gate feature** and the **semiconductor fin**. Goktepeli at 6:14-16 (Ex. 1006). Goktepeli further discloses that the **gate feature** wraps around the **semiconductor fin**. *Id*. at 1:57-59. A POSITA would have understood that the **gate feature** wrapping around the **semiconductor fin** would have been formed on the upper and side regions of the **semiconductor fin**. Moreover, a POSITA would have realized that the **gate dielectric** is an insulating film, because the purpose of the **gate dielectric** is to insulate the **fin** from the **gate feature**.

169. Doyle '373 likewise renders obvious a **gate insulating film**, formed on a side surface of the **first semiconductor region**. Doyle '373 discloses that a **gate structure** wraps around the **fin**. Doyle '373 at 3:36-37 (Ex. 1007). Figure 3 indeed shows such a **gate structure** wrapping around the **fin**.



170. Doyle '373 renders obvious that the **gate structure** has a **gate insulating film** formed between it and the **fin**. A POSITA would have known that in order to insulate the **gate structure** from the current passing through the **fin**, a **gate insulating film** would have to be formed therebetween.

171. In semiconductor manufacturing, the structural elements of a transistor are precisely determined prior to fabrication, in order to ensure that a final transistor meets a customer's specifications. This includes for example, the exact location, and dimensions of a **gate insulating film** on a fin, and the size and position of the **gate electrode**, formed over the **gate insulating film**. Without

knowing the exact placement of the **gate insulating film** on the **fin**, a transistor cannot meet customer specifications. The **gate insulating film** is therefore formed on the **fin** in a predetermined portion of the **fin**.

172. Goktepeli discloses element 5[b], that a **gate electrode** is formed on the **gate insulating film**. Because the purpose of the **gate insulating film** is to insulate the **fin** from the **gate electrode**, the **gate electrode** must be formed on top of the insulating film in order for the film to be effective. Indeed, Goktepeli discloses that a **gate dielectric** is formed between a **gate feature** and the **semiconductor fin**. Goktepeli at 6:14-16 (Ex. 1006).

173. Goktepeli renders obvious element 5[c], that the first and second impurity regions are formed in another portion of the fin other than the predetermined region. As previously mentioned, the gate insulating film, and gate electrode on gate insulating film, are formed in a predetermined region on the fin, according to customer specifications. Because the portion of the fin covered by the gate insulating film and gate electrode form the channel region, the portions of the fin not covered by the gate insulating film and gate electrode comprise the source and drain regions of the fin. The predetermined portion under the gate electrode forming the channel region is labeled below in Figure 5.



174. Doyle '373 likewise renders obvious first and second impurity regions formed outside of the predetermined portion. A POSITA would have known that extension regions, or tip implant regions, as Doyle '373 calls out, refer to the regions located beneath the sidewall spacers. Sidewall spacers are formed on the sides of the gate structure. Because the extension regions are located below the sidewall spacers, which are next to the gate structure, Doyle '373 renders obvious that the uniformly-doped extension regions are not formed

in the predetermined region where the **gate structure** is located.

175. A POSITA would have been motivated to combine Goktepeli with Doyle '373 for several reasons. First, both address the same problem of fabricating challenges associated with FinFETs. Goktepeli discloses that thicker silicon is needed in the **source/drain extensions** and **source/drain regions** in order to reduce parasitic resistance. Goktepeli at 2:38-40 (Ex. 1006). Goktepeli further discloses that high dose ion implantation can damage the thin silicon in these regions. *Id.* at 2:46-55. Doyle '373 notes that among the fabrication challenges for tri-gate transistors is the "difficulty of *optimizing* the **tip** and halo implantation profiles in this three-dimensional structure." Doyle '373 at 1:63-67 (Ex. 1007). Thus, both Goktepeli and Doyle '373 address the same problem of fabricating a transistor with optimal device performance.

176. A POSITA would have been motivated to apply Goktepeli to Doyle '373, to create a FinFET with desirable characteristics. A POSITA would have known that a transistor with optimal characteristics would have uniform doping in both the **source-drain regions**. **Source-drain regions** with nonuniform doping have less desirable characteristics than **source-drain regions** with uniform doping. This is because a non-uniformly doped **source-drain region** turns "on" and "off" at a slower speed. In order for a region to turn "on," current must flow through the upper and side regions. The FinFET can be understood as a combination of three planar FETs connected in parallel: the "top FET," and the two "side FETs." If, for example, the **source-drain regions** of the top FET are more heavily doped than the **source-drain regions** of the side FETs, the top FET will turn "off" before the two side FETs turn "off," i.e., the combination of the three FETs making up the FinFET will not be entirely shut "off" with a gate voltage that would normally hold the device in the "off" state. The situation is equivalent to the overall FinFET switching "off" more slowly, and could result in leakage current between the source and drain. Thus, uniform doping of the **source-drain regions** leads to optimal device behavior.

177. A POSITA would further have known that uniform doping of the extension regions leads to optimal transistor performance. The purpose of doping the extension regions is to minimize the channel length underneath the gate electrode, which both increases the operation speed and, because of the region of lower doping, minimizes short channel effects. Short channel effects become important when gate length is reduced, since reduced gate length without extension regions leads to disproportionately high electric fields at the gate edges, generating excessive source-drain current. The excess current is undesirable, as it causes excessive heating and wastes power.

178. Fabrication of transistors includes the steps of doping the sourcedrain regions and the extension regions. A POSITA would have known that doping of each of these regions could be performed by any number of doping methods, including implantation or diffusion. Utilizing the methods for doping the **source-drain regions** and the **extension regions** proposed by Goktepeli and Doyle '373, respectively, is a simple substitution of known methods. Such a substitution yields the predictable result of a transistor with uniformly-doped **source-drain regions** and **extension regions**, which for reasons previously discussed would lead to optimal transistor characteristics.

179. Combining the methods disclosed by Goktepeli and Doyle '373 would have been obvious to a POSITA. Because a POSITA would have known that uniform doping leads to optimal transistor characteristics for the reasons previously discussed, it would have been obvious to a POSITA to use methods for doping both the **source-drain regions** and **extension regions** that would lead to uniformly-doped regions. Also as previously discussed, a POSITA would have found it obvious to combine the two pieces of prior art because of the common inventors on each, and the common assignee, and the fact that both prior art address the same problem.

#### 4. <u>Dependent Claim 7</u>

180. Claim 7 depends from claim 5, which depends from claim 1. As discussed above and below, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

181. Doyle '373 discloses the remaining elements of claim 7, that the extension regions are P-type. As previously discussed, Doyle '373 refers to extension regions as tip implant regions. Doyle '373 further discloses that the tip implant regions are doped with dopants of the opposite conductivity type as the halo, or channel implant. Doyle '373 at 4:16-17 (Ex. 1007). A POSITA would have understood that the halo region is added to each end of the channel to create a more abrupt transition from the channel region doping to the opposite type sourcedrain doping. This abrupt transition further enhances the ability of the extension region to reduce short channel effects. Because a POSITA would further understand that the purpose of the extension regions is to shorten the channel length, a POSITA would have understood that the extension regions would be of the same conductivity type as the source-drain regions. Thus, for a PMOS FinFET, a POSITA would have understood that the source-drain regions, and extension regions, would both be p-type.

### 5. <u>Dependent Claim 8</u>

182. Claim 8 depends from claim 5, which depends from claim 1. As discussed above and below, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

183. Goktepeli discloses the further limitation of claim 8[a], that a **sidewall spacer** is formed on a side surface of the **gate electrode**. Goktepeli discloses "a

sidewall spacer is formed adjacent to the gate feature prior to forming the first and second sacrificial doping layers." Goktepeli at 6:16-18 (Ex. 1006). Goktepeli also claims a sidewall spacer in a dependent claim: "The method of claim 1 further comprising forming a sidewall spacer adjacent to the gate feature prior to the step of forming the first and second sacrificial doping layers." *Id.* at Claim 6. For reference, the Admitted Prior Art of the '165 patent confirms that the sidewall spacer disclosed by the '165 patent is located on the sidewall of the gate structure, precisely where Doyle '862 discloses.



184. Goktepeli discloses limitations 8[b] and 8[c]. As previously discussed, Goktepeli discloses a uniform doping method, by diffusion of dopants from the **sacrificial doping layer** into the **source/drain regions**. Goktepeli at 2:67-3:3, 4:57-60 (Ex. 1006). Also as previously discussed, Goktepeli discloses

that diffusion occurs in the upper and side regions of the fin. The doped upper and side regions of the fin in the source/drain regions disclose the **third** and **fourth impurity regions**.

185. Goktepeli discloses limitation 8[d], that the **first** and **second impurity regions** are formed in the **fin** under the **sidewall spacer** and provided in the other portion of the **first semiconductor region**. As previously discussed, Goktepeli discloses a **sidewall spacer**, formed adjacent to the **gate feature**. Goktepeli at 6:16-18 (Ex. 1006). A POSITA would have known that the **sacrificial doping layer** would be formed over the **sidewall spacer** (not in direct contact with the **extension regions**), and over the remainder of the exposed **fin** (in direct contact with the **source-drain regions**). The portion of the **sacrificial doping layer** formed in contact with the **source-drain regions** would be formed adjacent to the portion of the fin comprising the **extension region**.

186. When the dopants diffuse from the sacrificial doping layer into the fin, some of the dopants would diffuse into the extension region, because the sacrificial doping layer is formed adjacent to the extension region. The basic principle behind diffusion is that dopants will disperse to regions of less dopant concentration. Before diffusion begins, all regions of the fin are of equal lesser concentration than the sacrificial doping layer. Thus, when diffusion occurs, the dopants will travel into the entire fin accessible from the contact point of the

sacrificial doping layer with the source-drain regions, i.e., dopants will diffuse underneath the sidewall spacer into the extension region. These regions are illustrated on Figure 5 below.



187. Doyle '373 likewise discloses limitation 8[d]. As previously discussed, Doyle '373 discloses a method for doping the extension regions, and a POSITA would have known that the extension regions are located outside the gate electrode, since they are located beneath the spacers formed on the side of

the gate electrode.

188. Goktepeli renders obvious limitation 8[e]. A POSITA would have known that the **third** and **fourth impurity regions** referred to in claim 8 refer to the upper and side portions of the fin in the source/drain regions. Limitation 8[e] states that the third and fourth impurity regions are formed in the fin, and imposes two further limitations: that they are located "outside of the insulative sidewall spacer" and are "in the other portion" of the fin. With regard to the former, a POSITA would have realized that the fin portions located outside the insulative sidewall spacer, i.e., not underneath the sidewall spacer, could only refer to the source/drain regions, or the channel region (the portion of the fin located underneath the gate insulating film and gate electrode). The second limitation further narrows where a POSITA would have understood the third and fourth impurity regions to be. Claim 8 depends from claim 5, which sets forth that the "predetermined portion" is where the gate insulating film is formed. A POSITA would have understood that the "other" portion means outside the "predetermined portion" of the gate insulating film. Therefore, because claim 8 states that the third and fourth impurity regions are not the extension regions, and are not located underneath the gate insulating film in the "predetermined portion," they must be in the source/drain regions. And as previously discussed, Goktepeli discloses a method for doping the source/drain regions.



# 6. <u>Dependent Claim 9</u>

189. Claim 9 depends from claim 8, which depends from claims 5 and 1. As discussed above, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 1, 5, and 8.

190. Goktepeli renders obvious the additional limitation of claim 9, that the **third** and **fourth impurity regions** referred to in claim 8 are p-type **source-drain regions**. As previously discussed, a POSITA would have known that the **third** and **fourth impurity regions** refer to the **source/drain regions**. Goktepeli discloses a

method for doping source/drain regions.

191. A POSITA would have known that a transistor could be fabricated as one of two types: PMOS or NMOS. In a PMOS transistor, the **source/drain regions** are doped with p-type dopants. Goktepeli therefore discloses that the **third** and **fourth impurity regions**, located in the **source/drain regions**, are a ptype **source/drain region**.

#### 7. <u>Dependent Claim 10</u>

192. Claim 10 depends from claim 5, which depends from claim 1. As discussed above, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 5 and 1.

193. Goktepeli discloses the additional limitations of element 10[b], that the **first** and **second impurity regions** are formed outside the **sidewall spacer** and not underneath the **gate electrode**. As previously discussed, Goktepeli discloses a method for doping the **source-drain regions**. The **source-drain regions** are located outside the **gate electrode**. Goktepeli further discloses that the **sidewall spacer** is formed on the side of the **gate electrode**, and thus the **extension region** located beneath the **sidewall spacer** is likewise not under the **gate**.



# 8. <u>Dependent Claim 11</u>

194. Claim 11 depends from claim 5, which depends from claim 1. As previously discussed, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

195. Goktepeli renders obvious claim 11, that the first impurity region and the second impurity region are a p-type source-drain region. A PMOS transistor device is so named because the source and drain regions of a PMOS transistor device are doped with p-type dopants, such as boron, for example. Since Goktepeli discloses that the first and second impurity region comprise the source **drain regions**, and a POSITA would have known that the **source drain regions** contain p-type impurities, Goktepeli therefore renders obvious that the **first** and **second impurity regions** are p-type **source drain regions**.

### 9. Dependent Claim 12

196. Claim 12 depends from claim 5, which depends from claim 1. As previously discussed, Goktepeli in combination with Doyle '373 renders obvious each and every limitation of claims 1 and 5.

197. Goktepeli discloses the additional limitation of claim 12, that the height of the **fin** is greater than the width. A POSITA would have known that the gate width direction is the direction along which the gate spans. This is because the surfaces of the **fin** that are in contact with the gate feature are referred to in sum as the "gate width" of the transistor. Thus, the gate width dimensions are those that run parallel to the gate width direction. Goktepeli discloses that the height is greater than the width, measured in the gate width direction as shown, in Figure 1. For example Goktepeli specifically discloses that the height is five times the width. Goktepeli at 3:21-23 (Ex. 1006).



### **VIII. SPECIFIC GROUNDS FOR PETITION FOR CLAIMS 13-19**

### A. Ground 1: Doyle '862 in Combination with Chau

198. It is my opinion that Doyle '862 in combination with Chau renders obvious claims 13-19 of the '165 patent.

### 1. <u>Independent Claim 13</u>

199. Doyle '862 discloses the [preamble] and element [a] of claim 1. A **substrate**, also referred to as a wafer, is a surface on which a FinFET is formed. Doyle '862 teaches that a "**substrate** 110 can be composed of a single crystal
semiconductor material, which can be, for example, silicon or germanium." Doyle '862 at 2:27-29 (Ex. 1005). Doyle '862 further teaches that "Silicon fin 115 includes buried section 120." *Id.* at 2:30-31. As seen in Figure 1, fin 115 refers to the entire fin—both the portion formed above the surface of the substrate, as well as the portion buried in the substrate. Figures 1 and 2 show the fin has both an upper and a side surface, as shown by the portion not buried in the substrate.



200. As previously discussed, bulk doping was a common method for addressing the problem of leakage current in FinFETs. In order to bulk dope, the

entire **fin** was first implanted with the opposite type dopant as the final transistor type.<sup>9</sup> For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**.

201. Chau likewise discloses that the **fin** is of a first conductivity type. Chau discloses that the channel region and **source/drain regions** are doped with dopants of opposite conductivity types. This is done to prevent the electrical state of a nearby FET from affecting the threshold voltage (i.e., "backgating"). If opposite doping was not used, the electrical state of nearby FETs would cause changes in the device threshold voltage.

202. Chau further discloses that a **plurality of fins** can be used to "fabricate the transistors with larger gate widths." Chau ¶ 31 (Ex. 1008). A transistor with a larger gate width is desirable because it increases the effective gate width, allowing more transistors to be packed together on a single wafer. Figure 4B in Chau confirms such a configuration contains a **plurality of fins**, each

<sup>9</sup> Often the **substrate** itself has already received bulk doping as part of the wafer manufacturing process.



having an upper surface and a side surface:

203. Doyle '862 discloses element [b] of claim 13. As previously discussed, Doyle '862 discloses a uniform doping method. The upper surface of the **fin** is doped in the first step, and Doyle '862 suggests vertical implantation. Doyle '862 at 3:12-15 (Ex. 1005). Implantation is the process where ions are accelerated into the surface of a **fin**, and depending on certain variables (such as speed and angle) will penetrate a certain distance into the surface of the **fin**. Following implantation, the semiconductor containing the ions is annealed, or heated, to a high temperature to activate the ions. Once the dopant is annealed, a doped region of the **fin** is formed. Vertical implantation refers to implantation 0° from vertical, such that the ions approach the **fin** perpendicular to the upper surface. The vertical implantation is represented by the arrows labeled 165 in

Figure 3A.



204. Chau renders obvious that the impurity region disclosed by Doyle '862 is formed in each of a **plurality of fins**. The purpose of impurity regions is to carry current. Thus, each **fin** must have its own doped regions, i.e., **source/drain regions**. Without these regions in each **fin**, the **fins** would not each provide current, thus negating the benefits of a larger effective gate width in a FinFET with a **plurality of fins**.

205. Doyle '862 discloses element [c] of claim 13. The last step of the uniform doping method disclosed by Doyle '862 calls for "selectively doping sidewalls 150 and 155," or the sides of the **fins**. Doyle '862 at 3:66-67 (Ex. 1005). Doyle '862 teaches that such doping can be done by angled ion implantation, or

plasma-induced ion implantation (PLAD). *Id.* at 3:67-4:3, *see also id.* at Claim 10. Angled ion implantation is the same process as described in the preceding paragraph, except the dopants are accelerated toward the **fin** at an angle, as shown by the arrows in Figure 3F. PLAD, as Doyle '862 describes, requires a **substrate** be placed in a plasma field in the presence of dopant atoms. The dopant atoms accelerate towards the surface of the **fin** as a result of proper charges on the dopant atoms and the **fin**. *Id.* at 4:5-8. This angled implantation is represented by the arrows shown in Figure 3F.





**regions** are of a second conductivity type. As previously discussed, a POSITA would have known that the **fin** would first be doped to a first conductivity type. The **first** and **second impurity regions** would then be doped to a second conductivity type, of the same type as the overall transistor. For example, Doyle '862 discloses that for PMOS devices, the **source** and **drain regions** are doped with p-type impurities. Doyle '862 at 3:2-4 (Ex. 1005). Doping with dopants of a second impurity type forms impurity regions that are of a second conductivity type.

207. Doyle '862 further renders obvious that the impurity regions are made of a semiconductor. A semiconductor is a material (for example, silicon) that can be doped to transform into one of two distinct types of conductors: n-type and ptype. If the regions were not made of a semiconductor, current would not be able to flow through them.

208. In order to achieve optimal transistor performance, a person of ordinary skill in the art would have known that the top and sides of a **fin** should be doped uniformly using the same dopant type. Doping uniformly with the same dopant type on the top and side of the **fin** creates uniform current flow. This minimizes unwanted effects, such as sub-threshold leakage current and results in optimal transistor performance. For example, for a PMOS transistor device, the **source/drain regions** would be uniformly doped on all sides with p-type dopants.

209. Doyle '862 in combination with Chau renders obvious limitation

13[d], that the resistivity of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. Doyle '862 discloses that after the doping steps are completed, "the current flowing, or 'wrapping around,' **silicon fin** 115 should be uniform which results in a more efficient transistor." Doyle '862 at 4:21-23 (Ex. 1005). A POSITA would have understood this to mean that because the current is uniform in the **fin**, the resistivity of the **fin** is uniform. In other words, the resistivity of the doped upper portion of the **fin** is equal to the resistivity on each side of the **fin**, because resistivity is a characteristic that controls current flow.

210. Resistivity is a product of the depth and concentration of the implant. Doyle '862 discloses a uniform depth to which the dopants are implanted into the top and sides of the fin. As shown in Figure 4, the dopants are implanted to a depth "d" on all three sides of the fin. Doyle '862 at Fig. 4 (Ex. 1005).

211. Doyle '862 further discloses that the ions in the top surface can be implanted to a depth "from about 20 angstroms (Å) to about 200 Å." *Id.* at 3:23-24. Doyle '862 then discloses that the ions in the side surfaces can be doped "from about 10 Å to about 100 Å." *Id.* at 4:9. Concentration of ions can be controlled by changing certain parameters during doping processes. With implantation, for example, changing acceleration voltage and ion beam current affects the concentration of the implanted dopants. Thus, by changing the depth, and

concentration of implants, a POSITA can achieve the same resistivity on the upper and side surfaces of a **fin**, such that the resistivity is substantially the same in each.

212. Non-uniform doping of the **source-drain regions** creates undesirable transistor characteristics. A single FinFET can be viewed as three MOSFETs connected in parallel, a "top" horizontally oriented FET, and a "left" and "right" FET on each side of the **fin**. Each of these MOSFETs will perform optimally, with minimal short-channel effects, when they have the same doping profile<sup>10</sup> in the **source-drain** contact **region**. If any of the parallel FETs are not doped optimally, they degrade the overall operation of the FinFET.

213. There are numerous reasons why a POSITA would have been motivated to combine Doyle '862 with Chau. Both Doyle '862 and Chau address the same problem. That problem is how to fabricate a transistor with optimal device performance. Doyle '862 discloses the problems associated with nonuniform doping: "[t]he uneven doping of the **silicon fin** results in a change in resistance of the current." Doyle '862 at 1:52-53 (Ex. 1005). Doyle '862 further discloses that uniform doping with a **plurality of fins** can be difficult with angled ion implantation due to the shadowing effect of adjacent **fins**. *Id*. at 1:44-48. Chau

<sup>10</sup> This profile measures doping versus depth from the respective horizontal or vertical surface and, doping versus distance from the edge of the gate.

also discloses the problems associated with nonuniform doping: fabricating a transistor that does not operate in a fully depleted manner leads to non-ideal subthreshold slope and higher leakage of the device in the off state. Chau ¶ 17 (Ex. 1008). A transistor operating in a fully depleted manner lowers parasitic capacitance, which allows it to switch more quickly between the "on" and "off" states. This in turn allows logic circuits to execute arithmetic operations more quickly.

214. Nearly the same group of inventors addressed the problems contemplated by both pieces of prior art. Doyle '862 lists named inventors as Brian Doyle, Robert Chau, Suman Datta, and Jack Kavalieros. Doyle '862 at cover (Ex. 1005). Chau lists named inventors as Robert S. Chau, Brian S. Doyle, Jack Kavalieros, Douglas Barlage, and Suman Datta. Chau at cover (Ex. 1008). Thus, four of the same inventors are listed on both.

215. A POSITA would have been motivated to try different doping methods on a **plurality of fins**, in order to obtain a uniformly doped transistor with a **plurality of fins**. Such a transistor would have a larger effective gate width, because the effective gate width is the sum of the individual gate width of each fin. The benefit of having an increased gate width is that a transistor can control higher current levels. This in turn allows it to provide the same output signal (i.e., transmit whether it is in the on or off state), to multiple logic gate inputs.

216. The configuration of a transistor providing the same output signal to multiple logic gate inputs is referred to a "fan out" feature. The feature is so named, because the signal is transmitted from the transistor to multiple outputs, so the signal "fans out." The benefit of having a fan out feature is that it increases integrated circuit functionality. In certain types of logic circuitry, the state of a particular gate (e.g., the state of the output transistor) must become input to multiple new gates. For example, a memory sector must simultaneously report its status as "busy" or "ready for request" to multiple arithmetic processing units operating independently, each of which will eventually need to access this memory.

217. Another benefit of have a larger effective gate width is that it allows for more compact configuration of FinFET devices than a configuration with multiple separate FETs. This in turn leads to a lower unit production cost due to the area savings.

218. Applying the known uniform doping method disclosed by Doyle '862, to the **plurality of fins** disclosed by Chau, would have yielded the predictable result of a uniformly-doped **plurality of fins** in a FinFET. Doyle '862 discloses a method for uniformly doping a **source/drain region** in a since **fin**. Chau discloses a **plurality of fins**, where each has a **source/drain region**. Thus, combining the two would have yielded the predictable result of a **plurality of fins**, each with a

uniformly-doped source/drain region.

219. A POSITA would have understood that the method disclosed in Doyle '862 could be performed on a **plurality of fins**, as disclosed by Chau. The first step disclosed in Doyle '862 is the doping of the top surface of the **silicon fin** by, for example, vertical implantation. Doyle '862 at 3:12-14 (Ex. 1005). Vertical implantation is a type of ionized implantation where dopant atoms are ionized and isolated, accelerated, formed onto a beam, and targeted onto a **substrate**. *Id.* at 3:15-17. Due to being accelerated at and targeted onto a **substrate**, the ions penetrate the surface to a certain depth d. *Id.* at 3:17-19. Vertical implantation can be performed on a **plurality of fins**, since none of the **fins** would interfere with the vertical doping of an adjacent **fin**.

220. The second step disclosed in Doyle '862 is the conformal layer being deposited on the **silicon fin**. Doyle '862 discloses that deposition can be for example, by physical vapor deposition, atomic layer deposition, chemical vapor deposition, low pressure CVD, plasma-enhanced CVD or any other suitable process. Doyle '862 at 3:32-36 (Ex. 1005). A POSITA would know that any of these processes could be performed on a **plurality of fins**, since none of these processes would be affected by the presence of an adjacent fin.

221. The third step disclosed in Doyle '862 is the anisotropic etching to

remove the conformal layer and leave spacers on the sides of the **silicon fin**. Doyle '862 discloses that this can be done by, for example, reactive ion etching. Doyle '862 at 3:41-42 (Ex. 1005). A POSITA would have known that reactive ion etching could be performed on each of a **plurality of fins**, since reactive ion etching would not be unduly affected by the presence of adjacent **fins**.

222. The fourth step disclosed in Doyle '862 is the selective modification of the top surface of the **silicon fin**, such as by re-oxidation. Doyle '862 at 3:43-44 (Ex. 1005). Doyle '862 discloses that the re-oxidation can be by, for example, thermal oxidation, plasma oxidation or implantation of an oxygen species followed by annealing. *Id.* at 3:45-47. The purpose of the re-oxidation is to form a "mask" on the top surface of the **fin**, which protects the top surface of the **fin** from later implantation. *Id.* at 3:54-56. A POSITA would have known that re-oxidation could be performed on each of a **plurality of fins**, since the exemplar processes of thermal oxidation, plasma oxidation, or implantation of an oxygen species followed by annealing would not be affected by the presence of adjacent **fins**.

223. The fifth step disclosed in Doyle '862 is the removal of spacers by isotropic etching. For example, Doyle discloses that a chemical could be used, such as phosphoric acid, to etch in all directions, which would cause undercutting. Doyle '862 at 3:61-64 (Ex. 1005). A POSITA would have known that isotropic etching could be performed on each of the **plurality of fins**, since the process of

isotropic wet etching on each of the **fins** would not be unduly affected by the presence of adjacent **fins**.

224. The sixth step disclosed in Doyle '862 is the selective doping of sidewalls. Doyle '862 discloses that this can be done by angled ion implantation, or by plasma-induced ion implantation (PLAD). Doyle '862 at 3:65-4:3 (Ex. 1005). PLAD involves a **substrate** placed in a plasma field, and due to charges on the dopant atoms and the **substrate**, the dopant atoms accelerate into the **substrate** (here, the **fin**) and thereby penetrate the surface of the **substrate**. *Id.* at 4:5-8. A POSITA would have known that selective doping could be performed on each of the sidewalls of a **plurality of fins** because PLAD, for example, can be performed without adjacent **fins** impeding the atoms' ability to penetrate the surfaces of the **fins**.

225. A POSITA would know that Doyle '862 could be performed on a single fin. And because of the steps enumerated above, and their ability to be performed on each of a **plurality of fins** without the presence of adjacent fins impeding any of the steps, the expected result would be a **plurality of fins**, each uniformly doped.

226. In fact, combining Doyle '862 with Chau was simply substituting one known method for another to obtain predictable results. A POSITA would have known that each of the **plurality of fins** disclosed by Chau would have had its own

**source/drain region** that had to be created by doping. Chau ¶ 23 (Ex. 1008). And Doyle '862 discloses a method for doping a **source/drain region**. Thus, combining the two is a simple substitution of known elements to yield the predictable result of a **plurality of fins**, each with its own uniformly-doped **source/drain region**.

227. Moreover, a POSITA would have found it obvious to try the uniform doping method disclosed by Doyle '862, on a **plurality of fins** disclosed by Chau. Doyle '862 discloses a method for uniformly doping one **fin**. And as previously discussed, a POSITA would have known that each of the steps disclosed by Doyle '862 could be performed on each of a **plurality of fins**. Doyle '862 and Chau additionally have four common inventors, addressing the same problem of how to fabricate a transistor with optimal characteristics.

#### 2. <u>Independent Claim 14</u>

228. Claim 14 depends from claim 13. As described above, Doyle '862 in combination with Chau discloses every limitation of claim 13.

229. Chau discloses the limitation 14[a]. Chau discloses that "[g]ate electrode 324 is formed on and adjacent to each gate dielectric 322 on each of the semiconductor bodies 308." Chau ¶ 31 (Ex. 1008). Figure 4B from Chau confirms that Chau discloses this limitation:



230. Chau discloses limitation 14[b] that the **gate electrode** extends across the **plurality of fins** in a gate width direction. A POSITA would have known that the gate width direction is the direction labeled in Figure 3. For example, the labels "g1," "g2," and "g3" refer to gate width dimensions. Chau ¶ 16 (Ex. 1008) ("The gate 'width' of a transistor is equal to the sum of each of the three sides of the semiconductor body."). These dimensions are in the plane of the gate width direction.



231. Chau discloses that the **gate electrode** extends across the **plurality of fins** in the aforementioned gate width direction. Chau ¶ 31 (Ex. 1008) ("Gate electrode 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308."). Chau's disclosure is confirmed by Figure 4B:



## 3. Dependent Claim 15

232. Claim 15 depends from claim 14. As described above, Doyle '862 in combination with Chau discloses every limitation of claim 14.

233. Doyle '862 renders obvious the additional limitation of claim 15, that a first and second impurity region are a p-type extension region. As previously discussed, Doyle '862 describes manufacturing steps that creates doped regions underneath a sidewall spacer. And Doyle expressly acknowledges the presence of a sidewall spacer, formed on the side of a gate electrode. Doyle at 3:56-58 (Ex. 1006). Thus, Doyle '862 discloses a first and second impurity region by its disclosure of an extension region. As previously discussed, the vertical and angled implantation steps used to form the first and second impurity regions,



respectively, can be performed where a **sidewall spacer** is used.

234. Doyle '862 renders obvious that the **extension regions** are p-type. A POSITA would have known that the **extension regions** would be doped with the same type impurity as the overall transistor type, i.e., the **source-drain region** dopant type. This is because the purpose of the **extension region** is to minimize short channel effects, i.e., to decrease the width of the channel. If the **extension region** was doped to the same type as the **source-drain region**, then the effective length of the channel would increase, which would be undesirable. Thus, the **extension regions** would be doped with the same type impurity as the **source-drain region** in order to minimize short channel effects.

## 4. <u>Dependent Claim 16</u>

235. Claim 16 depends from claim 14. As described above, Doyle '862 in

combination with Chau discloses every limitation of claim 14.

236. Doyle '862 discloses the further limitation of claim 16, that the **first** and **second impurity regions** are p-type **source-drain regions**. As previously discussed, Doyle '862 discloses a method for uniform doping of the **source-drain regions**. Doyle '862 further discloses that a PMOS transistor device has a **source** and **drain region** doped with p-type impurities, such as boron. Doyle '862 at 3:2-4 (Ex. 1005). Therefore, Doyle renders obvious a **first** and **second impurity region** in the **source-drain region** that is p-type.

## 5. <u>Dependent Claim 17</u>

237. Claim 17 depends from claim 13. As described above, Doyle '862 in combination with Chau renders obvious each and every limitation of claim 13.

238. Chau further discloses the additional limitation of claim 17, that a third semiconductor region connects together the end portions of the plurality of fins in a gate length direction. Chau refers to the third semiconductor region as a source-drain landing pad. Chau ¶ 31 (Ex. 1008) ("source regions 330 and drain regions 332 of the semiconductor bodies 308 are electrically coupled together by the semiconductor material . . . to form a source landing pad 460 and a drain landing pad 480 as shown in FIG. 4B.").



# 6. <u>Independent Claims 18 and 19</u>

239. Because claims 18 and 19 of the '165 patent are nearly identical, I will address them together in this section. The only difference between claims 18 and 19 is in the final limitation. And the additional difference between claims 18 and 19 and previously-discussed claim 13 is that claim 13 applies to a **plurality of fins**, rather than a single **fin**.

Claim 13	Claim 18	Claim 19
13[preamble]-13[a]:	18[preamble]-18[a]:	19[preamble]-19[a]:
A semiconductor	A semiconductor	A semiconductor
device, comprising:	device, comprising:	device, comprising:
a [ <mark>plurality of</mark> ]	a first semiconductor	a first semiconductor
semiconductor region[ <mark>s</mark> ]	region of a first	region of a first
of a first conductivity	conductivity type	conductivity type
type formed on a	formed on a substrate	formed on a substrate
substrate and [ <mark>each</mark> ]	and having an upper	and having an upper

Claim 13	Claim 18	Claim 19
having an upper surface	surface and a	surface and a
and a side surface;	side surface;	side surface;
13[b]:	18[b]:	19[b]:
a first impurity region of a second	a first impurity region of a second	a first impurity region of a second
conductivity type	conductivity type	conductivity type
formed in an upper	formed in an upper	formed in an upper
portion of [ <mark>each of the</mark>	portion of the first	portion of the first
plurality of	semiconductor region	semiconductor region
<mark>semiconductor</mark>	and made of a	and made of a
regions] and made of a	semiconductor; and	semiconductor; and
semiconductor; and		
13[c]:	18[c]:	19[c]:
a second impurity	a second impurity	a second impurity
region of a second	region of a second	region of a second
conductivity type	conductivity type	conductivity type
formed in a side portion	formed in a side portion	formed in a side portion
of [ <mark>each of the</mark>	of the first	of the first
plurality of	semiconductor region	semiconductor region
semiconductor	and made of a	and made of a
regions] and made of a	semiconductor, wherein	semiconductor, wherein
semiconductor, wherein	4.05.11	4.05.17
13[d]:	18[d]:	19[d]:
a <mark>resistivity</mark> of the	a <mark>sheet resistance</mark> of the	a <mark>spreading resistance</mark>
second impurity region	second impurity region	of the second impurity
is substantially equal to	is substantially equal to	region is substantially
or smaller than that of	or smaller than that of	equal to or smaller than
the first impurity	the first impurity	that of the first
region.	region.	impurity region.

240. As previously discussed, Doyle '862 discloses the limitations of elements 13[preamble]-13[c] for a single fin.

241. Doyle '862 discloses the additional limitation of element 18[d], that the *sheet resistance* of the **second impurity region** is substantially equal to or smaller than that of the **first impurity region**. It is well known that sheet resistance is directly proportional to resistivity. Schroder at 1 (Ex. 1009). The sheet resistance of a region is calculated as resistivity divided by thickness. Thus, if two regions have the same resistivity, and the same thickness, they will have the same sheet resistance.

242. As previously discussed in claim 13, Doyle '862 discloses that the resistivity of the **first** and **second impurity regions** is equal. Doyle '862 further discloses that the thickness of the **first** and **second impurity regions** is equal. Doyle '862 at 4:16-18 (Ex. 1005) (disclosing all faces are doped "to a depth d"). Thus, the sheet resistance of the **first** and **second impurity regions** is equal.



243. Doyle '862 renders obvious limitation 19[d], that the spreading resistance of the **first** and **second impurity regions** is equal. Spreading resistance is a way of comparing the resistance between any two points in or on a layer of material. Schroder at 43-44 (Ex. 1009). Spreading resistance is calculated as resistivity, divided by the circumference of a tip end of a probe, with certain correction factors taken into account. '165 patent at 4:6-19 (Ex. 1003). In other words, the spreading resistance of an impurity region is equal to resistivity of that region multiplied by a geometric factor. That geometric factor is always the same for the same shape of impurity layer (for example, the constant for a rectangular box region will always be constant) measured with the same probes. Therefore, for the same geometry, as occurs in the top and side layers of the **fin** disclosed in

Doyle, impurity regions with the same or lower resistivity (as is described by Doyle) will have the same or lower spreading resistance. Like sheet resistance, spreading resistance is always directly proportional to resistivity. If the resistivity of a region at two points is equal, i.e., the concentration of ions at those two points is equal, then the spreading resistance will be equal.

244. As previously discussed in claim 13, Doyle '862 renders obvious that the resistivity in the **first** and **second impurity regions** is equal. Doyle '862 further discloses that the "silicon body [has] uniform doping." Doyle '862 at cover (Ex. 1005). Because Doyle '862 discloses an equal resistivity, and uniform doping, a POSITA would have realized that the spreading resistance of the **first** and **second impurity regions** is equal.

#### **B.** Ground 2: Goktepeli in Combination with Chau

245. It is my opinion that Goktepeli in combination with Chau renders obvious claims 13-19 of the '165 patent.

#### 1. Independent Claim 13

246. Goktepeli discloses the [preamble] and element [a] for claim 13. Goktepeli discloses a fin formed on a substrate. "Illustrated in FIG. 1 is a semiconductor device 10 comprising a substrate 12, a conformal layer on the substrate 12 which is patterned to form source/drain contact regions 14 and 16 and a fin 20 which forms extension regions 22 and 24, and a gate feature 18."

Goktepeli at 3:12-16 (Ex. 1006). These features are shown in the annotated Figure 1 below.



247. Chau likewise discloses a fin formed on a substrate. Chau specifically discloses "a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate." Chau at Abstract (Ex. 1008); *see also id.* ¶ 16.

248. As previously discussed, bulk doping was a common method for addressing the problem of leakage current in FinFETs. In order to bulk dope, the entire fin was first implanted with the opposite type dopant as the final transistor type.<sup>11</sup> For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**.

249. Goktepeli further renders obvious that the **first** and **second impurity regions** are of a second conductivity type. As previously discussed, a POSITA would have known that the **fin** would first be doped to a first conductivity type. The **first** and **second impurity regions** would then be doped to a second conductivity type, of the same type as the overall transistor. For example, for an NMOS FinFET, the entire **fin** is first implanted with a p-type dopant. Thus, the **silicon fin** is formed of a first conductivity type. The purpose of the initial doping is to prevent current leakage from **source/drain regions** formed later in the process. Any such current leakage could leak into the **substrate** and affect nearby FinFETs formed on the same **substrate**. Doping with dopants of a second impurity type forms impurity regions that are of a second conductivity type.

250. Chau likewise discloses that the fin is of a first conductivity type. Chau discloses that the channel region and source/drain regions are doped with

<sup>&</sup>lt;sup>11</sup> Often the **substrate** itself has already received bulk doping as part of the wafer manufacturing process.

dopants of opposite conductivity types. This is done in order to ensure that the flow of current in the channel region can be turned "on" and "off." If the channel region was doped with the same conductivity type dopants as the **source/drain regions**, the transistor would not have such performance.

251. Chau further discloses that a **plurality of fins** can be used to "fabricate the transistors with larger gate widths." *Id.* ¶ 31. A transistor with a larger gate width is desirable because it increases the effective gate width, allowing more transistors to be packed together on a single wafer. Figure 4B in Chau confirms such a configuration contains a **plurality of fins**, each having an upper surface and a side surface:



252. Goktepeli discloses element [b] of claim 13. Goktepeli discloses a uniform doping method, by forming a sacrificial doping layer over the source-

drain extensions and source/drain regions. Goktepeli at 4:29-31 (Ex. 1006). Goktepeli discloses that the formation of the sacrificial doping layer can be on "exposed semiconductor surfaces." *Id.* at 4:13-14. Since the upper region of the fin is exposed, a POSITA would have known that the sacrificial doping layer would have been formed over the upper portion of the fin, leading to doping of the upper portion of the fin (either by diffusion or by angled ion implantation of the sacrificial doping layer). Figure 7 confirms that the sacrificial doping layer is formed over the upper region of the source-drain extensions and source/drain regions.



253. Chau renders obvious that the impurity region disclosed by Goktepeli

is formed in each of a **plurality of fins**. The purpose of impurity regions is to attract and hold the flow of current, so that applying a voltage to the gate turns an individual **fin** "on" or "off." Thus, each **fin** must have its own doped regions, i.e., **source/drain regions**. Without these regions in each **fin**, the **fins** would not turn on or off uniformly, thus negating the benefits of a larger effective gate width in a FinFET with a **plurality of fins**.

254. Goktepeli discloses element [c] of claim 13. Goktepeli discloses a uniform doping method, by forming a sacrificial doping layer over the sourcedrain extensions and source/drain regions. Goktepeli at 4:29-31 (Ex. 1006). Goktepeli discloses that the formation of the sacrificial doping layer can be on "exposed semiconductor surfaces." *Id.* at 4:13-14. Since the side region of the fin is exposed, a POSITA would have known that the sacrificial doping layer would have been formed over the side portion of the fin, leading to doping of the side portion of the fin (either by diffusion or by angled ion implantation of the sacrificial doping layer). Figure 7 confirms that the sacrificial doping layer is formed over the side region of the source-drain extensions and source/drain regions.



255. Goktepeli renders obvious that the **first** and **second impurity regions** are of a second conductivity type. A POSITA would have known that a transistor could be fabricated as one of two types: PMOS or NMOS. For example, in a PMOS transistor, the **source-drain regions** are doped with p-type dopants. As previously discussed, a POSITA would have known that before doping with p-type dopants, the fin would first be bulk doped with dopants of the opposite conductivity type, in order to create a contrast in the conductivity type of the **source-drain regions**. The initial bulk doping creates a region of the first conductivity type, and the later doping of the **source-drain regions** creates the

region of a second conductivity type.

256. Chau likewise renders obvious that the **first** and **second impurity regions** are of a second conductivity type. Chau explains that the channel region, i.e., the portion of the **fin** located beneath the gate, is doped to the opposite type as the **source-drain regions**. A POSITA would have understood that the purpose of doping a channel region to the opposite type as the **source-drain regions** is to create a more abrupt transition from the channel region doping to the opposite type source-drain doping. This abrupt transition further enhances the ability of the **extension region** to reduce short channel effects.

257. Either of Goktepeli or Chau further render obvious that the impurity regions are made of a semiconductor. A semiconductor is a material (for example, silicon) that can be doped to transform into one of two distinct types of conductors: n-type and p-type. If the regions were not made of a semiconductor, current would not be able to flow through them.

258. In order to achieve optimal transistor performance, a person of ordinary skill in the art would have known that the top and sides of a **fin** should be doped uniformly using the same dopant type. Doping uniformly with the same dopant type on the top and side of the **fin** creates uniform current flow. This minimizes unwanted effects, such as sub-threshold leakage current and results in optimal transistor performance. For example, for a PMOS transistor device, the

source/drain regions would be uniformly doped on all sides with p-type dopants.

259. Chau renders obvious that the impurity region disclosed by Goktepeli is formed in each of a **plurality of fins**. The purpose of impurity regions is to carry current. Thus, each **fin** must have its own doped regions, i.e., **source/drain regions**. Without these regions in each **fin**, the **fins** would not supply current, thus negating the benefits of a larger effective gate width in a FinFET with a **plurality of fins**.

260. Goktepeli discloses limitation 1[d], that the resistivity of the second **impurity region** is substantially equal to or smaller than that of the **first impurity** region. Goktepeli discloses that the sacrificial doping layer is formed over the upper and side regions of the source-drain extensions and source/drain regions, following which the dopants diffuse into the source-drain extensions and source/drain regions. Goktepeli at 2:67-3:5, 4:57-60 (Ex. 1006). Goktepeli specifically discloses that the dopants diffuse into the regions "evenly and thoroughly," id. at 4:59-60, which a POSITA would have understood to mean uniformly in the upper and side regions. Resistivity is a product of the depth and concentration of the implant. Doping by diffusion distributes dopants to a uniform depth across all surfaces, with a uniform concentration across all surfaces. Thus, Goktepeli's disclosure of doping by diffusion renders obvious a uniform resistivity of the first and second impurity regions.

261. Non-uniform doping of the **source-drain regions** creates undesirable transistor characteristics. A single FinFET can be viewed as three MOSFETs connected in parallel, a "top" horizontally oriented FET, and a "left" and "right" FET on each side of the **fin**. Each of these MOSFETs will perform optimally, with minimal short-channel effects, when they have the same doping profile<sup>12</sup> in the **source-drain** contact **region**. If any of the parallel FETs are not doped optimally, they degrade the overall operation of the FinFET.

262. There are numerous reasons why a POSITA would have been motivated to combine Goktepeli with Chau. Both Goktepeli and Chau address the same problem of how to fabricate a transistor with optimal device performance. Goktepeli discusses the problem of the conflicting needs for thinner silicon for the channel to reduce transistor gate length, and thicker silicon in the **source/drain extensions** and **source/drain regions** in order to reduce parasitic resistance. Goktepeli at 2:36-40 (Ex. 1006). Thicker silicon is needed in the **source/drain extensions** and **source/drain regions** because implanting with ions in these regions can lead to dose loss (the regions are not thick enough to stop the ions), and can cause excessive crystal damage. *Id.* at 2:49-55. Chau also discloses the

<sup>12</sup> This profile measures doping versus depth from the respective horizontal or vertical surface and, doping versus distance from the edge of the gate.

problems associated with nonuniform doping: fabricating a transistor that does not operate in a fully depleted manner leads to unideal subthreshold slope and higher leakage of the device in the off state. Chau ¶ 17 (Ex. 1008). A transistor operating in a fully depleted manner lowers parasitic capacitance, which allows it to switch more quickly between the "on" and "off" states. This in turn allows logic circuits to execute arithmetic operations more quickly.

263. Chau discloses a FinFET with a **plurality of fins**, or "**multiple semiconductor bodies**," as shown in Figure 4B. Chau ¶ 31 (Ex. 1008). The benefit of having such a **plurality of fins** is that a transistor has a larger effective gate width, since the gate width is the sum of the gate width of each of the individual **fins**.

264. Goktepeli discloses that doping by diffusion creates uniformly-doped regions in the **source/drain regions** and the **source/drain extension regions**. Goktepeli at 4:59-60 (Ex. 1006). If doping by diffusion occurs at a constant temperature, then dopants will spread uniformly. This allows for the top FET and the two side FETs that make up a FinFET to all operate with the same optimized source-drain doping.

265. A POSITA would have been motivated to try different doping methods on a **plurality of fins**, in order to obtain a uniformly doped transistor with a **plurality of fins**. Goktepeli discloses one such method for uniform doping.

Such a transistor would have a larger effective gate width, because the effective gate width is the sum of the individual gate width of each fin. The benefit of having an increased gate width is that a transistor can control higher current levels. This in turn allows it to provide the same output signal (i.e., transmit whether it is in the on or off state), to multiple logic gate inputs.

266. The configuration of a transistor providing the same output signal to multiple logic gate inputs is referred to a "fan out" feature. The feature is so named, because the signal is transmitted from the transistor to multiple outputs, so the signal "fans out." The benefit of having a fan out feature is that it increases integrated circuit functionality. In certain types of logic circuitry, the state of a particular gate (e.g., the state of the output transistor) must become input to multiple new gates. For example, a memory sector must simultaneously report its status as "busy" or "ready for request" to multiple arithmetic processing units operating independently, each which will eventually need to access this memory.

267. Another benefit of having a larger effective gate width is that it allows for more compact configuration of FinFET devices than a configuration with multiple separate FETs. This in turn leads to a lower unit production cost due to the area savings.

268. Applying the known uniform doping method disclosed by Goktepeli, to the **plurality of fins** disclosed by Chau, would have yielded the predictable
result of a uniformly-doped **plurality of fins** in a FinFET. Goktepeli discloses a method for uniformly doping a **source/drain region** in a since **fin**. Chau discloses a **plurality of fins**, where each has a **source/drain region**. Thus, combining the two would have yielded the predictable result of a **plurality of fins**, each with a uniformly-doped **source/drain region**.

269. In fact, combining Goktepeli with Chau was simply substituting one known method for another to obtain predictable results. A POSITA would have known that each of the **plurality of fins** disclosed by Chau would have had its own **source/drain region** that had to be created by doping. Chau ¶ 23 (Ex. 1008). And Goktepeli discloses a method for doping a **source/drain region**. Thus, combining the two is a simple substitution of known elements to yield the predictable result of a **plurality of fins**, each with its own uniformly-doped **source/drain region**.

270. Moreover, a POSITA would have found it obvious to try the uniform doping method disclosed by Goktepeli, on a **plurality of fins** disclosed by Chau. Doyle '862 discloses a method for uniformly doping one **fin**. Chau discloses the benefit of a **plurality of fins** is a larger effective gate width. Doping a **plurality of fins** with a plasma implant is not ideal because less implant reaches the bottom portions of tightly-spaced **fins**. In contrast, Goktepeli's disclosure of doping by diffusion via a **sacrificial doping layer** provides uniform doping across all surfaces of the **fin**.

#### 2. <u>Independent Claim 14</u>

271. Claim 14 depends from claim 13. As described above, Goktepeli in combination with Chau discloses every limitation of claim 13.

272. Chau discloses the limitation 14[a]. Chau discloses that "[g]ate electrode 324 is formed on and adjacent to each gate dielectric 322 on each of the semiconductor bodies 308." Chau ¶ 31 (Ex. 1008). Figure 4B from Chau confirms that Chau discloses this limitation:



273. Chau discloses limitation 14[b] that the **gate electrode** extends across the **plurality of fins** in a gate width direction. A POSITA would have known that the gate width direction is the direction labeled in Figure 3. For example, the labels "g1," "g2," and "g3" refer to gate width dimensions. Chau ¶ 16 (Ex. 1008) ("The gate 'width' of a transistor is equal to the sum of each of the three sides of

the semiconductor body."). These dimensions are in the plane of the gate width direction.



274. Chau discloses that the **gate electrode** extends across the **plurality of fins** in the aforementioned gate width direction. Chau ¶ 31 (Ex. 1008) ("Gate electrode 324 is formed on and adjacent to each **gate dielectric** 322 on each of the **semiconductor bodies** 308."). Chau's disclosure is confirmed by Figure 4B:



## 3. Dependent Claim 15

275. Claim 15 depends from claim 14, which depends from claim 13. As described above, Goktepeli in combination with Chau discloses every limitation of claims 14 and 13.

276. Goktepeli renders obvious the additional limitation of claim 15, that a first and second impurity region are a p-type extension region. Goktepeli discloses a sidewall spacer, formed adjacent to the gate feature. Goktepeli at 6:16-18 (Ex. 1006). A POSITA would have known that the sacrificial doping layer would be formed over the sidewall spacer (not in direct contact with the extension regions), and over the remainder of the exposed fin (in direct contact with the source-drain regions). The portion of the sacrificial doping layer

formed in contact with the **source-drain regions** would be formed adjacent to the portion of the fin comprising the **extension region**.

277. When the dopants diffuse from the sacrificial doping layer into the fin, some of the dopants would diffuse into the extension region, because the sacrificial doping layer is formed adjacent to the extension region. The basic principle behind diffusion is that dopants will disperse to regions of less dopant concentration. Before diffusion begins, all regions of the fin are of equal lesser concentration than the sacrificial doping layer. Thus, when diffusion occurs, the dopants will travel into the entire fin accessible from the contact point of the sacrificial doping layer with the source-drain regions, i.e., dopants will diffuse underneath the sidewall spacer into the extension region.

278. Goktepeli renders obvious that the **extension regions** are p-type. A POSITA would have known that the **extension regions** would be doped with the same type impurity as the overall transistor type, i.e., the **source-drain region** dopant type. This is because the purpose of the **extension region** is to minimize short channel effects, i.e., to decrease the width of the channel. If the **extension region** was doped to the same type as the **source-drain region**, then the effective length of the channel would increase, which would be undesirable. Thus, the **extension regions** would be doped with the same type impurity as the **source-drain region** in order to minimize short channel effects.

#### 4. Dependent Claim 16

279. Claim 16 depends from claim 14, which depends from claim 13. As described above, Goktepeli in combination with Chau discloses every limitation of claims 14 and 13.

280. Goktepeli discloses the further limitation of claim 16, that the first and second impurity regions are p-type source-drain regions. A POSITA would have known that a transistor could be one of two types: PMOS or NMOS. For a PMOS transistor, a POSITA would have known that the source-drain regions would be doped with p-type dopants. As previously discussed, Goktepeli discloses a method for uniform doping of the source-drain regions. Thus, a POSITA would have known that Goktepeli's method of doping source-drain regions could be performed with p-type dopants, for a PMOS transistor.

### 5. Dependent Claim 17

281. Claim 17 depends from claim 13. As described above, Goktepeli in combination with Chau renders obvious each and every limitation of claim 13.

282. Chau further discloses the additional limitation of claim 17, that a **third semiconductor region** connects together the end portions of the **plurality of fins** in a gate length direction. Chau refers to the **third semiconductor region** as a **source-drain landing pad**. Chau ¶ 31 (Ex. 1008) ("**source regions** 330 and **drain regions** 332 of the semiconductor bodies 308 are electrically coupled together by

the semiconductor material . . . to form a **source landing pad** 460 and a **drain landing pad** 480 as shown in FIG. 4B.").



# 6. <u>Independent Claims 18 and 19</u>

283. Because claims 18 and 19 of the '165 patent are nearly identical, I will address them together in this section. The only difference between claims 18 and 19 is in the final limitation. And the additional difference between claims 18 and 19 and previously-discussed claim 13 is that claim 13 applies to a **plurality of fins**, rather than a single **fin**.

Claim 13	Claim 18	Claim 19
13[preamble]-13[a]:	18[preamble]-18[a]:	19[preamble]-19[a]:
A semiconductor device, comprising:	A semiconductor device, comprising:	A semiconductor device, comprising:
a [ <mark>plurality of</mark> ]	a first semiconductor	a first semiconductor

Claim 13	Claim 18	Claim 19
semiconductor region[ <b>s</b> ] of a first conductivity type formed on a substrate and [ <b>each</b> ] having an upper surface and a side surface;	region of a first conductivity type formed on a substrate and having an upper surface and a side surface;	region of a first conductivity type formed on a substrate and having an upper surface and a side surface;
13[b]:	18[b]:	19[b]:
a first impurity region of a second conductivity type formed in an upper portion of [each of the plurality of semiconductor regions] and made of a semiconductor: and	a first impurity region of a second conductivity type formed in an upper portion of the first semiconductor region and made of a semiconductor; and	a first impurity region of a second conductivity type formed in an upper portion of the first semiconductor region and made of a semiconductor; and
13[c]:	18[c]:	19[c]:
a second impurity region of a second conductivity type formed in a side portion of [ <b>each of the</b> <b>plurality of</b> <b>semiconductor</b> <b>regions</b> ] and made of a semiconductor, wherein	a second impurity region of a second conductivity type formed in a side portion of the first semiconductor region and made of a semiconductor, wherein	a second impurity region of a second conductivity type formed in a side portion of the first semiconductor region and made of a semiconductor, wherein
13[d]:	18[d]:	19[d]:
a <i>resistivity</i> of the second impurity region is substantially equal to or smaller than that of the first impurity region.	a <b>sheet resistance</b> of the second impurity region is substantially equal to or smaller than that of the first impurity region.	a <i>spreading resistance</i> of the second impurity region is substantially equal to or smaller than that of the first impurity region.

284. As previously discussed, Goktepeli discloses the limitations of elements 13[preamble]-13[c] for a single fin.

285. Goktepeli discloses the additional limitation of element 18[d], that the *sheet resistance* of the second impurity region is substantially equal to or smaller than that of the first impurity region. It is well known that sheet resistance is directly proportional to resistivity. Schroder at 1 (Ex. 1009). The sheet resistance of a region is calculated as resistivity divided by thickness. Thus, if two regions have the same resistivity, and the same thickness, they will have the same sheet resistance.

286. As previously discussed in claim 13, Goktepeli renders obvious that the resistivity of the **first** and **second impurity regions** is equal. Goktepeli further renders obvious that the thickness of the **first** and **second impurity regions** is equal, since a POSITA would have known that doping by diffusion would create regions of uniform thickness. Thus, the sheet resistance of the **first** and **second impurity regions** is equal.

287. Goktepeli renders obvious the additional limitation of element 19[d], that the spreading resistance of the **first** and **second impurity regions** is equal. Spreading resistance is a way of comparing the resistance between any two points in or on a layer of material. Schroder at 43-44 (Ex. 1009). Spreading resistance is calculated as resistivity, divided by the circumference of a tip end of a probe, with

certain correction factors taken into account. '165 patent at 4:6-19 (Ex. 1003). In other words, the spreading resistance of an impurity region is equal to resistivity of that region multiplied by a geometric factor. That geometric factor is always the same for the same shape of impurity layer (for example, the constant for a rectangular box region will always be constant) measured with the same probes. Therefore, for the same geometry, as occurs in the top and side layers of the **fin** disclosed in Goktepeli, impurity regions with the same or lower resistivity will have the same or lower spreading resistance. Like sheet resistance, spreading resistance is always directly proportional to resistivity. If the resistivity of a region at two points is equal, i.e., the concentration of ions at those two points is equal, then the spreading resistance will be equal.

288. As previously discussed in claim 13, Goktepeli renders obvious that the resistivity in the **first** and **second impurity regions** is equal. Goktepeli further discloses that the "silicon body [has] uniform doping." Goktepeli at cover (Ex. 1006). Because Goktepeli discloses an equal resistivity, and uniform doping, a POSITA would have realized that the spreading resistance of the **first** and **second impurity regions** is equal.

#### IX. CONCLUSION

289. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art as of the priority date of the '165 patent, every limitation of

the structures described in the Challenged Claims of the '165 patent are disclosed or rendered obvious by the prior art.

290. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: July 31, 2018

Respectfully submitted,

tanley Darfield ey Shanfield, Ph.D. Stanley Shanfield, Ph.D.