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(54) **METHOD OF ION IMPLANTING FOR TRI-GATE DEVICES**

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257/E29.275; 257/E21.618; 257/E21.633

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438/202; 257/412, E21.345, E21.442, E27.112,
257/E29.275, E21.618, E21.633

See application file for complete search history.

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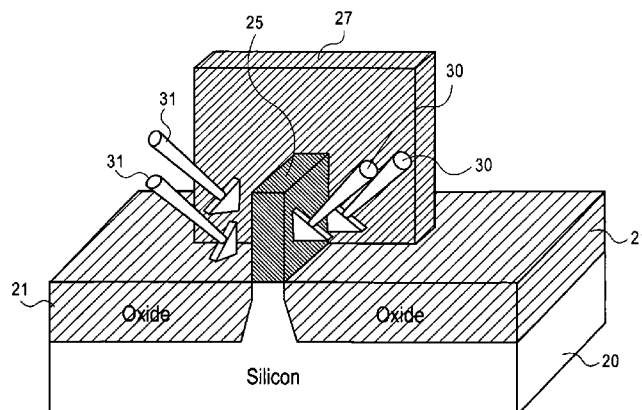
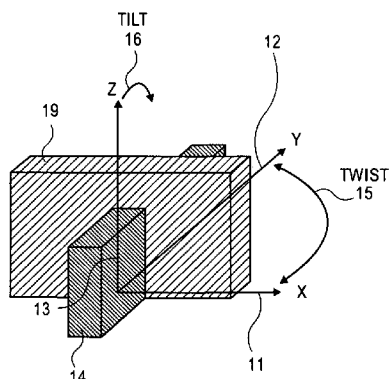
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(57) **ABSTRACT**

A method for ion implanting a tip source and drain region and halo region for a tri-gate field-effect transistor is described. A silicon body is implanted, in one embodiment, from six different angles to obtain ideal regions.

19 Claims, 3 Drawing Sheets



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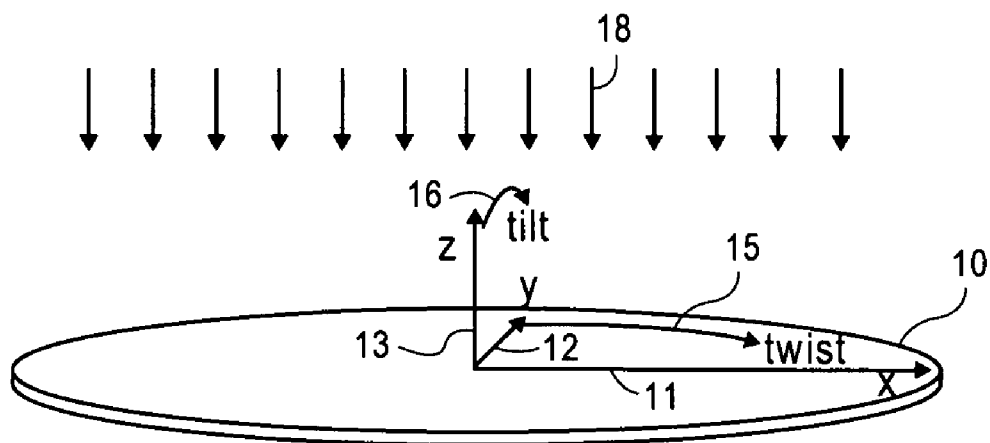


FIG. 1

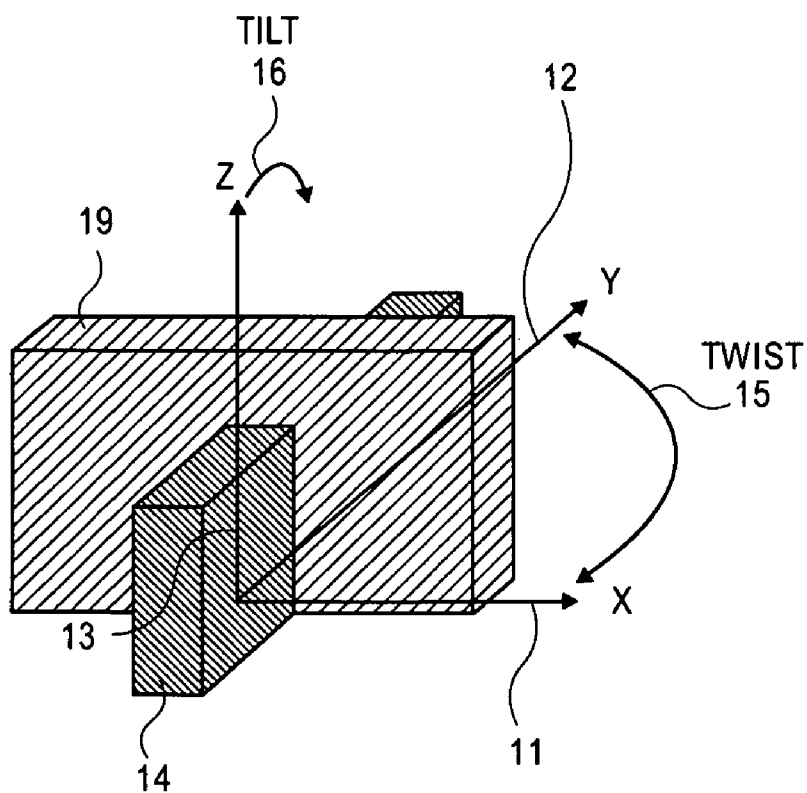


FIG. 2

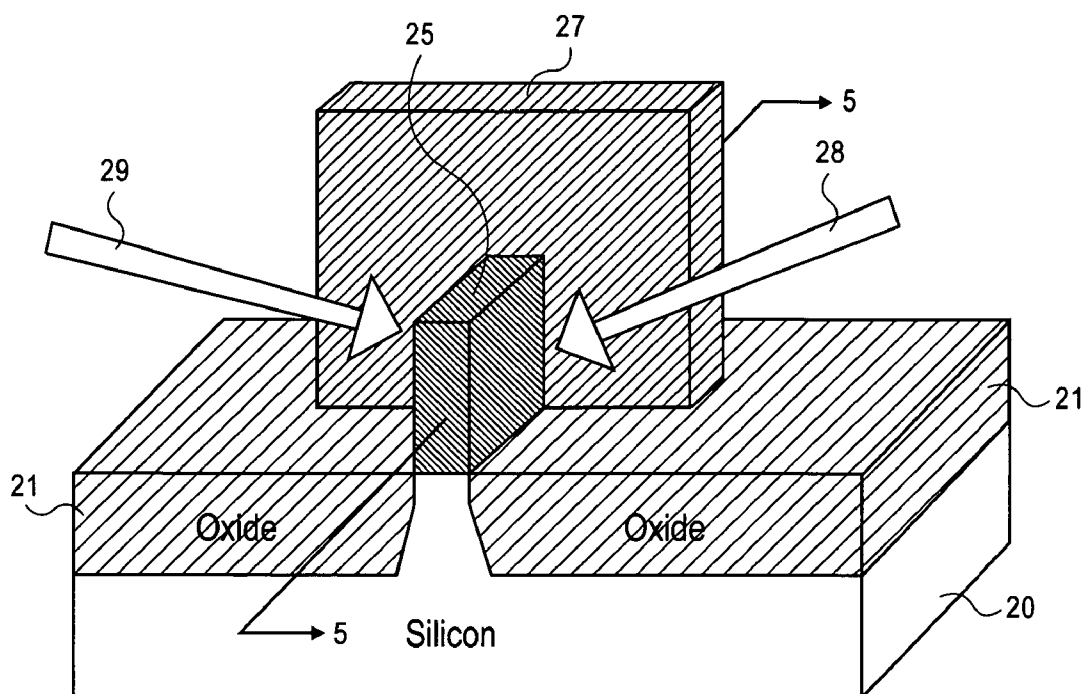


FIG. 3

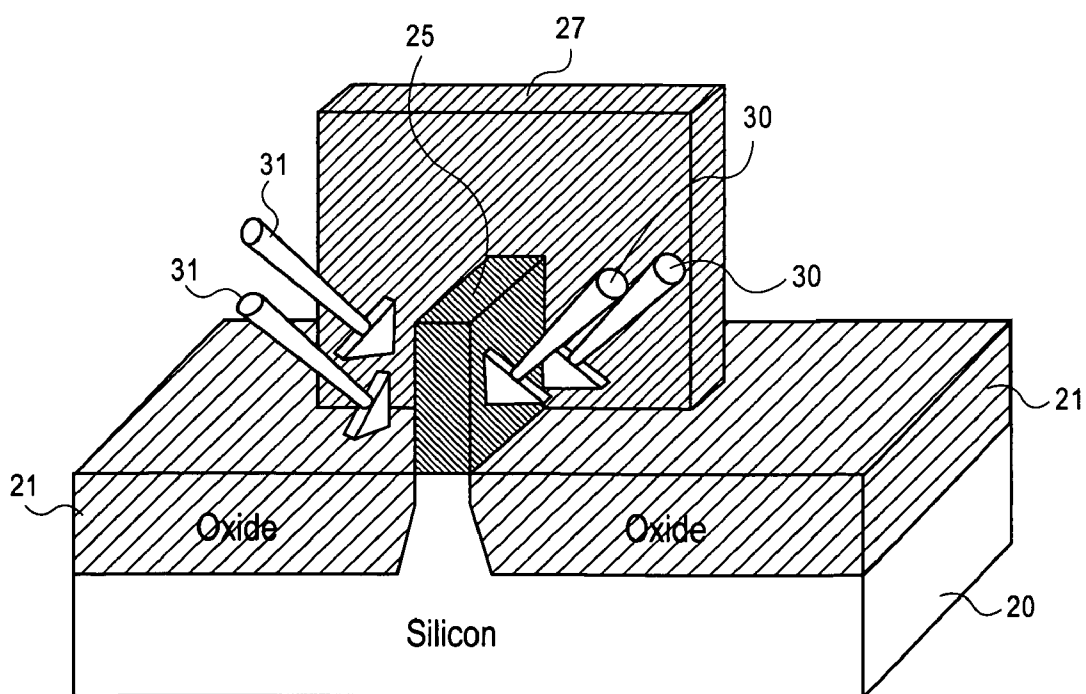


FIG. 4

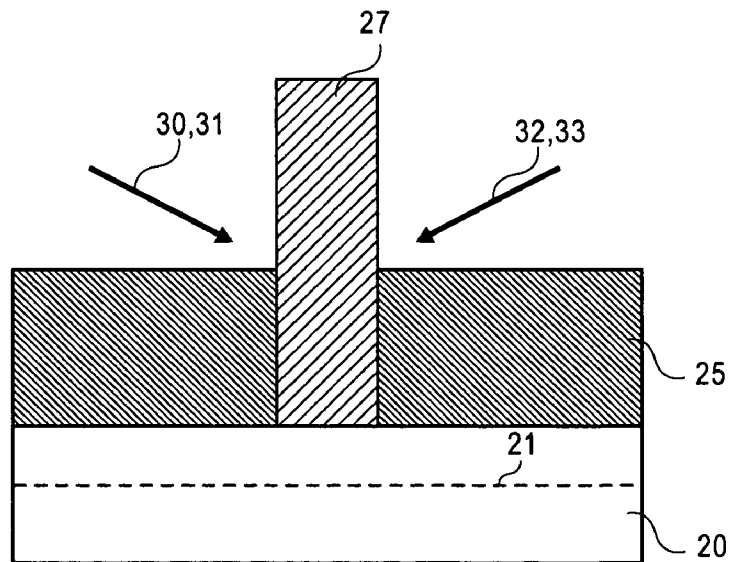


FIG. 5

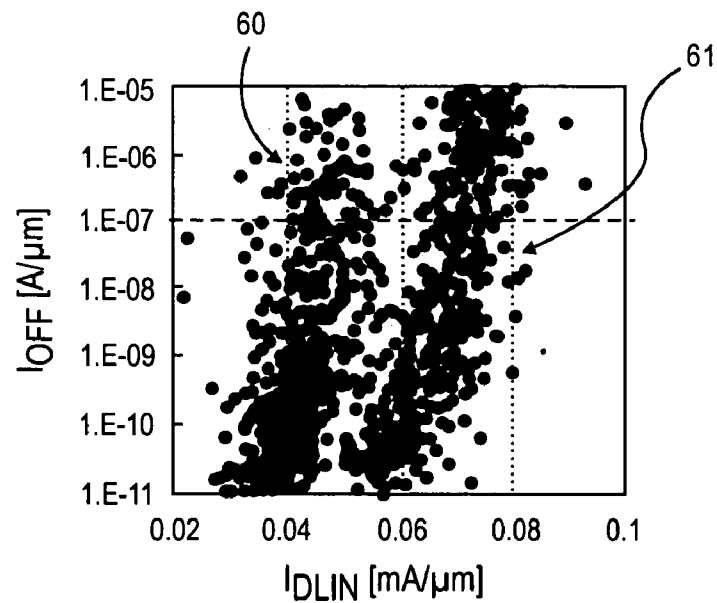


FIG. 6

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METHOD OF ION IMPLANTING FOR TRI-GATE DEVICES

FIELD OF THE INVENTION

The invention relates to tip and halo implants in field-effect devices.

PRIOR ART AND RELATED ART

It is well known to implant the source and drain regions of field-effect transistors with a shallow, extension source and drain regions to, for example, reduce punchthrough. It is also well known to implant doping under the gates of field-effect transistors, generally after the formation of the shallow, extension source and drain regions and before the formation of side spacers. This implantation is used to form doped halos, in some applications, to adjust the threshold voltage and to combat short channel effects. This implantation may provide compensation for variations in critical dimensions of the gate. See for instance U.S. Pat. No. 6,020,244 and U.S. Publication 2004/0061187.

Sometimes dual halo implants are used to provide dual thresholds for both NMOS and PMOS transistors. Examples of this are shown in U.S. Publications 2003/0203579 and 2003/0122197. In other cases, particularly for tri-gate devices, dual implants are used at different angles to assure the implantation of halos, both for the top transistor and sidewall transistors. See "A Dual Halo Implant for Improved Short Channel Effect in 3-Dimensional Tri-Gate Transistors," U.S. Ser. No. 11/321,128, filed Dec. 28, 2005, assigned to the assignee of the present application.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a wafer being ion implanted. This figure is used to show tilt and twist angles.

FIG. 2 is a perspective view of a semiconductor body or fin and a tri-gate structure. This figure is used to show the axes orientation adopted for purposes of explanation in this patent.

FIG. 3 is a perspective view of a tri-gate transistor during its fabrication and more particularly during an implantation step used to implant the tip source and drain regions.

FIG. 4 illustrates the structure of FIG. 3 in another ion implantation process, for implanting halo regions.

FIG. 5 illustrates the structure of FIG. 3 in a cross-sectional view, taken generally through the sectional line 5-5 of FIG. 3.

FIG. 6 is a graph illustrating the improved performance obtained for the angled tip implant over a vertical implant.

DETAILED DESCRIPTION

A method for providing tip source/drain and halo implants particularly suited for a tri-gate transistor is described. In the following description, numerous specific details are set forth such as dose levels, in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known processes needed to carry out ion implantation, such as dopant activation, are not described in detail in order to not unnecessarily obscure the present invention.

There are numerous performance advantages to tri-gate transistors which justifies the increased complexity needed in their fabrication. Among the fabrication challenges is the difficulty of optimizing the tip and halo implantation profiles in this three-dimensional structure.

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As an example, currently, multiple energy implants are proposed to target the shallow and deep portions of the device source/drain regions and channel regions. In the case of the tip implant of the body or fin, implanting vertically dopes the top of the fin. This vertical implant does not effectively implant the sidewalls which may have a 50 nm or deeper depth. Deep and shallow implants can be used. The consequences of the deep implants include a resultant spread or lateral "straggle" which severely limits the precision with which the dopant can be introduced and creating devices with different effective lengths.

Another difficulty stems from the fact that a first type dopant is needed for the tip implant and a second type dopant is needed for the halo implant. Consequently, the introduction of the halo dopant can counter-dope the tip region.

Tri-gate transistors may be looked at as constituting a top transistor, similar to a conventional planar transistor, and two side wall transistors. Usually, a single angled halo implant is used from opposite directions to, for instance, adjust the threshold voltage of the transistors and to control the short channel effects. If this implantation is targeted deep (nearly vertical) in order to control the side transistors and lower plane of the tri-gate transistor, which is most susceptible to short channel effect, the threshold voltage of the top transistor is too low. On the other hand, if the halo implant is at a shallow angle and relatively low energy, the bottom of the transistor is lightly doped, making the transistor susceptible to subsurface punchthrough (e.g. source to drain tunneling). Moreover, the source/drain extension regions are counter doped, leading to a high external resistance.

In the description which follows, ion implantation occurs at different angles relative to the devices being fabricated. Some conventions are needed in this patent to explain the angles at which the implantation occurs.

In FIG. 1, a wafer 10 is illustrated being ion implanted as shown by the ion beam 18. Typically in an ion implanter the beam is fixed relative to the implanter. The wafer is mounted on a movable platform and can be moved to desired angles for implantation. In FIG. 1, the wafer is shown on an X-axis 11 and Y-axis 12, both of which are in the plane of the wafer. The wafer 10 is also shown to have a Z-axis 13 normal to the plane of the wafer. For the discussion below, "twist" refers to rotation of the wafer (or a substrate) in the plane of the wafer as indicated by the arrow 15. "Tilt" refers to tilting the wafer in any direction as indicated by arrow 16 in the YZ plane. With a combination of twisting and tilting, ions can be implanted at any desired angle into devices fabricated on the wafer 10.

In FIG. 2, a single semiconductor fin 14 is illustrated with a transverse gate structure 19. The fin 14 may be formed on a bulk silicon substrate by masking some regions and then epitaxially growing fins on the exposed silicon. Alternatively, the fin may be etched in a bulk silicon. Moreover, a silicon-on-insulator (SOI) substrate may be used where the fins are etched in a thin monocrystalline film. For purposes of explanation in this patent, it is assumed that the fin 14 is disposed along the Y-axis 12, the gate structure 19 is disposed along the X-axis 11, and that the fin 14 extends upward along the Z-axis 13.

The structure of FIG. 2 may be disposed on the wafer 10 of FIG. 1. The twisting and tilting that occurs in an ion implanter is shown as twist 15 and tilt 16 in FIG. 2. Consequently, by way of example, the fin 15 may be twisted in the XY plane so that the fin is at acute angle to the Y-axis, and then it may be tilted, as shown by the arrow 16 in FIG. 2. For the description below, it is assumed that the tilting occurs in only a single plane. This is often the case since the table upon which the

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wafer is mounted is effectively hinged for the described embodiment, along the X-axis.

It will be apparent to one skilled in the art that the orientation of the fin **14** along the axes shown in FIG. **2** is arbitrary. The fin **14** could just as well extend along the X-axis, and the gate structure **19** along the Y-axis. If this is the case, the twisting and tilting, described below, will need to be adjusted to accommodate this different orientation of the fin **14**. Additionally, if for instance, the table on which the wafer is mounted tilts in all directions, as it would if it is gimbaled, then the twisting described below determines the plane in which the tilting occurs.

In FIGS. **3**, **4** and **5** below, ion implantation is shown occurring into a semiconductor body or fin **25**. Rather than showing a wafer or substrate, twisted and turned, a substrate is shown in a normal position and the ion beam at an angle. The angle of the beam is described by the twisting and tilting discussed above relative to the X, Y and Z-axes shown in FIG. **2**.

In FIG. **3**, a monocrystalline silicon substrate **20**, which is a portion of the wafer **10** of FIG. **1**, is illustrated. A monocrystalline silicon body or fin **25** is formed on the substrate **20**. Where a bulk substrate **20** is used, the fin **25** can be formed by epitaxial growth between the oxide members **21**. The fin **25** may also be formed by etching a substrate leaving a fin in place. The fin **25** may also be formed on a silicon-oxide-insulator (SOI) substrate, as mentioned.

A tri-gate structure **27** is formed on at least three sides of the fin **25** as part of, for instance, a replacement gate process. At the point in processing shown in FIGS. **3-5**, the structure **27** may be a dummy gate, of for instance, polysilicon, which is subsequently removed and replaced with a high-k dielectric and a metal gate with a targeted work function.

The relationship of the gate structure **27** of FIG. **3** and the fin **25** is illustrated in FIG. **5**, a cross-sectional, elevation view taken through the section line **5-5** of FIG. **3**. In this view, it can be seen that the gate structure **27** wraps around the fin **25**. When a field-effect transistor is fabricated from the structure of FIGS. **3-5**, the source and drain regions are formed in the portion of the fin **25** not covered by the gate structure **27**. The portion of the fin **25** covered by the gate structure **27** becomes the channel region of the transistor. It is the channel region which receives the halo implant, and the exposed portions of the fin **25** which receive the tip implant.

In one embodiment, both the tip implant and halo implant are done at the stage in transistor fabrication shown in FIGS. **3-5**. After these implants, spacers are formed on the sides of the gate structure **27**. Then, the main source and drain regions are implanted in alignment with the spacer. Following this, a dielectric such as an interlayer dielectric (ILD) is formed surrounding the gate structure **27**. This allows the gate structure **27** to be etched, leaving exposed, the channel region of the fin **25**. Then, the final high-k dielectric and metal gate are formed in the replacement gate process. Other embodiments, where, for instance, the spacers are formed after the halo implant are discussed later.

The tip implant for the lightly doped source and drain regions is done with the ion beam being generally parallel to the sides of the gate structure **27** and at an acute angle to a normal extending from the XY plane. This angle is obtained by twisting the wafer $\pm 90^\circ$ and then tilting the wafer to the acute angle. The ion implantation that occurs with the twist of $+90^\circ$ and the tilt of the acute angle is shown by beam **28** in FIG. **3**. The implantation that occurs with the twist of -90° and a tilt to the acute angle is shown by beam **29** in FIG. **3**.

At first it may seem that a tilt of 45° is ideal. The problem that occurs, however, is that if 45° is selected, the top surface

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of the fin **25** receives twice the dose since it is implanted first by the beam **28** at the $+90^\circ$ angle, and then again by the beam **29** in the -90° angle. Thus, the top receives more dopant than the sides.

An acute angle of 60° ensures that both the top and sides get the same dopant concentration. However, this results in a shallower doping of the top since the angle of incident for the top surface is 60° , whereas the angle of incident for the sides of the fin is 30° .

An angle of between 50° - 55° tilt has been found to provide the best trade-off between the depth of the implant and the concentration of the implant. As will be shown later, in conjunction with FIG. **6**, implanting in this manner provides a better than 30% increase in performance, when compared to a vertical implant into the fin **25**.

The dopant for the tip implant is of an opposite conductivity type to the halo implant. The tip implant may be phosphorous or arsenic for an n-channel transistor, or boron for a p-channel transistor. A typical implant dose may be $5E14$ - $5E15$ atoms/cm². In some processes, it may be possible to implant the fin with a single ion implantation step from a single side of the fin (i.e. either $+90^\circ$ or -90°). An angle between 45° - 60° is used in one embodiment.

FIG. **4** illustrates the halo implant. For the n-channel transistor, a p-type dopant such as boron is used. For a p-channel transistor, an n-type dopant such as phosphorous or arsenic is used. As mentioned earlier, it is necessary to get the dopant along both the sides and top of the fin **25** under the gate structure **27**. This assures that both the top and the side "transistors" formed by the tri-gate, turn-on at the same time.

The halo implant is done in four steps. Two implantations are done from one side of the gate structure **27** as shown by beams **30** and **31** of FIG. **4**. Two other implants are done from the other side of the gate structure as best seen in FIG. **5**, as shown by the beam **32** and **33**. The first two implants are done by first twisting the wafer by a 180° and then implanting at an additional twist $\pm$ a first acute angle (θ_1) from the 180° twist with a tilt of a second acute angle (θ_2). The third and fourth implants are done at $\pm\theta_1$. That is, the fin is twisted $\pm\theta_1$ from the position shown in FIG. **2**. Again, a tilt angle of θ_2 is used for the third and fourth implants. θ_1 of 10° - 45° with a tilt (θ_2) of, again, 50° - 55° is used. In a typical field-effect transistor a dose of $1E12$ - $1E13$ atoms/cm² may be typical. The selection of θ_2 is, for the most part, based on the same rationale used for the selection of the tilt angle for the tip implant.

While in the above description the tip implants are performed before the halo implants, the halo implants may be performed before the tip implants. A number of other alternate orders of the steps may be used. First, it should be appreciated that since the tip implant is done at an angle, it may be done after the spacers are formed. Thus, the halo implants may be done first (without spacers) followed by forming the spacers, and then the tip implants. Alternatively, the tip implants may be first, followed by forming spacers, and then the halo implants.

In FIG. **6**, the data point group **60** represents one measure of performance for vertical implantation, whereas the group **61** shows the performance for the tip implants at the tilt angle of 50° - 55° , as described earlier. As can be seen, the ratio of the off current to the current before saturation is much improved by the angled implant, as shown by the grouping **61**. There is an approximately 30% increase in performance, as mentioned earlier.

Thus, with angled implants as described above, better performance is achieved, as well as improving short channel characteristics associated with a halo implant.

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What is claimed is:

1. A method for fabricating a semiconductor device comprising:

ion implanting, a semiconductor fin disposed on a substrate, which fin is initially disposed along a Y-axis, extends above the substrate along a Z-axis, and has a gate structure transversing the fin along a X-axis, with ions of a first conductivity type to form spaced-apart tip source and drain regions in the fin along the Y-axis; and ion implanting the semiconductor fin generally under the gate structure, with ions of a second conductivity type to form halo regions generally between the spaced-apart tip source and drain regions, the halo ion implanting occurring with the wafer twisted in the XY plane at a first acute angle, and tilted at a second acute angle in the YZ plane.

2. The method defined by claim 1, wherein the first acute angle is between approximately 10°-45°.

3. The method defined by claim 2, wherein the second acute angle is approximately 50°-55°.

4. The method defined by claim 3, wherein the halo implantation also occurs at the first and second acute angles after the substrate has been twisted approximately 180° so as to implant under the gate structure from the opposite side.

5. The method defined by claim 4, wherein the second acute angle is approximately 50°-55°.

6. The method defined by claim 5, wherein the first acute angle is approximately 10°-45°.

7. The method defined by claim 6, wherein the fin comprises a monocrystalline silicon.

8. The method defined by claim 7, wherein the fin is implanted by the halo ion implantation to a dose of 1E12-1E13 atoms.

9. The method defined by claim 1, wherein the halo ion implantation occurs before the tip ion implantation.

10. A method of fabricating a semiconductor device comprising:

performing one of the following steps before the other:
ion implanting a semiconductor fin disposed on a substrate, which fin is initially disposed on a Y-axis,

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extends above the substrate on a Z-axis, and has a gate structure transversing the fin on a X-axis, with ions of a first conductivity type to form spaced-apart tip source and drain regions in the fin along the Y-axis, the tip ion implanting occurring with the wafer twisted by approximately 90° and tilted at a first angle in the YZ plane; and

ion implanting the semiconductor fin generally under the gate structure, with ions of a second conductivity type to form halo regions, generally between the spaced-apart tip source and drain regions, the halo ion implanting occurring with the wafer twisted in the XY plane at plus and minus a second acute angle, and tilted at a third acute angle in the YZ plane.

11. The method defined by claim 10, wherein the halo implantation also occurs at plus and minus the second acute angle after the substrate has been twisted approximately 180° so as to implant under the gate structure from the opposite side.

12. The method defined by claim 10, wherein the first acute angle is between approximately 50°-55°.

13. The method defined by claim 12, wherein the second acute angle is approximately between 10°-45°.

14. The method defined by claim 13, wherein the third acute angle is approximately between 50°-55°.

15. The method defined by claim 11, wherein the first and third acute angle is approximately between 50°-55° and the second acute angle is approximately between 10°-45°.

16. The method defined by claim 10, including forming spacers on the gate structure before the tip and halo implantations.

17. The method defined by claim 10, including forming spacers between the two implantation steps of claim 10.

18. The method defined by claim 10, wherein the substrate is a bulk silicon substrate.

19. The method defined by claim 10, wherein the substrate is a silicon-on-insulator (SOI) substrate.

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