# SEMICONDUCTOR MATERIAL AND DEVICE CHARACTERIZATION

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## Third Edition

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# CONTENTS

# PREFACE TO THIRD EDITION

Semiconductor characterization has continued its relentless advance since the publication of the second edition. New techniques have been developed, others have been refined. In the second edition preface I mentioned that techniques such as scanning probe, total-reflection X-ray fluorescence and contactless lifetime/diffusion length measurements had become routine. In the intervening years, probe techniques have further expanded, charge-based techniques have become routine, as has transmission electron microscopy through the use of focused ion beam sample preparation. Line width measurements have become more difficult since lines have become very narrow and the traditional SEM and electrical measurements have been augmented by optical techniques like scatterometry and spectroscopic ellipsometry. In addition to new measurement techniques, the interpretation of existing techniques has changed. For example, the high leakage currents of thin oxides make it necessary to alter existing techniques/theories for many MOS-based techniques.

I have rewritten parts of each chapter and added two new chapters, deleted some outdated material, clarified some obscure/confusing parts that have been pointed out to me. I have redone most of the figures, deleted some outdated ones or replaced them with more recent data. The third edition is further enhanced through additional problems and review questions at the end of each chapter and examples throughout the book, to make it a more attractive textbook. I have added 260 new references to bring the book as up-to-date as possible. I have also changed the symbol for sheet resistance from $\rho_s$ to $R_{sh}$, to bring it in line with more accepted use.

I list the main additional or expanded material here briefly by chapter. There are many other smaller changes throughout the book.

*Chapter 1*

New sheet resistance explanation; new 4-point probe derivation; use of 4-point probe for shallow junctions and high sheet resistance sample; added the *Carrier Illumination* method.

*Chapter 2*
Contactless $C-V$ added; integral capacitance augmented; series capacitance added/augmented; free carrier absorption augmented; new lateral profiling section; added Appendix 2—equivalent circuit derivations.

*Chapter 3*
Augmented circular contact resistance section; added considerations of parasitic resistance in TLM method; expanded barrier height section by adding BEEM; added Appendix dealing with parasitic resistance effects.

*Chapter 4*
Added section of pseudo MOSFETs for silicon-on-insulator characterization; added several MOSFET effective channel length measurement methods and deleted some of the older methods.

*Chapter 5*
Added Laplace DLTS; added a section to the time constant extraction portion in Appendix 5.2.

*Chapter 6*
Expanded the section on oxide thickness measurements; added considerations for the effect of leaky gate oxides on conductance and charge pumping; added the $DC$-$IV$ method; expanded the section on gate oxide leakage currents; added Appendix 6.2 considering the effects of wafer chuck parasitic capacitance and leakage current.

*Chapter 7*
Clarified the optical lifetime section; added *Quasi-steady-state Photoconductance*; augmented the free carrier absorption and diode current lifetime method; added leaky oxide current considerations to the pulsed MOS capacitor technique.

*Chapter 8*
Added the effects of gate depletion, channel location, gate current, interface traps, and inversion charge frequency response to the extraction of the effective mobility. I also added a section on contactless mobility measurements.

*Chapter 9*
This chapter is new and introduces charge-based measurement and Kelvin probes. I have also included probe-based measurements here and expanded these by including scanning capacitance, scanning Kelvin force, scanning spreading resistance, and ballistic electron emission microscopy.

*Chapter 10*
Expanded confocal optical microscopy, photoluminescence, and line width measurement.

*Chapter 11*
Made some small changes.

*Chapter 12*
This is a new chapter, dealing with *Failure Analysis and Reliability*. I have taken some sections from other chapters in the second edition and expanded them. I introduce failure times and distribution functions here, then discuss electromigration; hot carriers; gate oxide integrity; negative bias temperature instability; stress induced leakage current; electrostatic discharge that are of concern for device reliability. The rest of this chapter deals with the more common failure analysis techniques: quiescent drain current; mechanical probes; emission microscopy; fluorescent microthermography; infrared thermography; voltage contrast; laser voltage probe; liquid crystals; optical beam induced resistance change and noise.

Several people have supplied experimental data and several concepts were clarified by discussions with experts in the semiconductor industry. I acknowledge their contributions in the figure captions. Tom Shaffner from the National Institute of Standards and Technology has continued to be an excellent source of knowledge and a good friend and Steve Kilgore from Freescale Semiconductor has helped with electromigration concepts. The recent book *Handbook of Silicon Semiconductor Metrology*, edited by Alain Diebold, is an excellent companion volume as it gives many of the practical details of semiconductor metrology missing here. I thank executive editor G. Telecki, R. Witmer and M. Yanuzzi from John Wiley & Sons for editorial assistance in bringing this edition to print.

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# 1

# RESISTIVITY

## 1.1 INTRODUCTION

The *resistivity* $\rho$ of a semiconductor is important for starting material as well as for semiconductor devices. Although carefully controlled during crystal growth, it is not truly uniform in the grown ingot due to variability during growth and segregation coefficients less than unity for the common dopant atoms. The resistivity of epitaxially grown layers is generally very uniform. Resistivity is important for devices because it contributes to the device series resistance, capacitance, threshold voltage, hot carrier degradation of MOS devices, latch up of CMOS circuits, and other parameters. The wafers resistivity is usually modified locally during device processing by diffusion and ion implantation, for example.

The resistivity depends on the free electron and hole densities $n$ and $p$, and the electron and hole mobilities $\mu_n$ and $\mu_p$ according to the relationship

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \tag{1.1}$$

$\rho$ can be calculated from the measured carrier densities and mobilities. For extrinsic materials in which the majority carrier density is much higher than the minority carrier density, it is generally sufficient to know the majority carrier density and the majority carrier mobility. The carrier densities and mobilities are generally not known, however. Hence we must look for alternative measurement techniques, ranging from *contactless*, through *temporary contact* to *permanent contact* techniques.

*Semiconductor Material and Device Characterization, Third Edition*, by Dieter K. Schroder

## 1.2 TWO-POINT VERSUS FOUR-POINT PROBE

The *four-point probe* is commonly used to measure the semiconductor resistivity. It is an absolute measurement without recourse to calibrated standards and is sometimes used to provide standards for other resistivity measurements. Two-point probe methods would appear to be easier to implement, because only two probes need to be manipulated. But the interpretation of the measured data is more difficult. Consider the two-point probe or two-contact arrangement of Fig. 1.1(a). Each contact serves as a current *and* as a voltage probe. We wish to determine the resistance of the device under test (DUT). The total resistance $R_T$ is given by

$$R_T = V/I = 2R_W + 2R_C + R_{DUT} \tag{1.2}$$

where $R_W$ is the wire or probe resistance, $R_C$ the contact resistance, and $R_{DUT}$ the resistance of the device under test. Clearly it is impossible to determine $R_{DUT}$ with this measurement arrangement. The remedy is the four-point probe or four-contact arrangement in Fig. 1.1(b). The current path is identical to that in Fig. 1.1(a). However, the voltage is now measured with two additional contacts. Although the voltage path contains $R_W$ and $R_C$ as well, the current flowing through the voltage path is very low due to the high input impedance of the voltmeter (around $10^{12}$ ohms or higher). Hence, the voltage drops across $R_W$ and $R_C$ are negligibly small and can be neglected and the measured voltage is essentially the voltage drop across the DUT. By using four rather than two probes, we have eliminated parasitic voltage drops, even though the voltage probes contact the device on the same contact pads as the current probes. Such four contact measurements are frequently referred to as *Kelvin measurements*, after Lord Kelvin.

An example of the effect of two versus four contacts is shown in Fig. 1.2. The drain current–gate voltage characteristics of a metal-oxide-semiconductor field-effect transistor were measured with one contact on source and drain (no Kelvin), one contact on source and two contacts on drain (Kelvin-Drain), two contacts on source and one on drain (Kelvin-Source), and two contacts on source and drain (Full Kelvin). It is quite obvious that eliminating contact and probe resistances in the "Full Kelvin" has a significant effect on the measured current. The probe, contact, and spreading resistances of a two-point probe arrangement on a semiconductor are illustrated in Fig. 1.3.

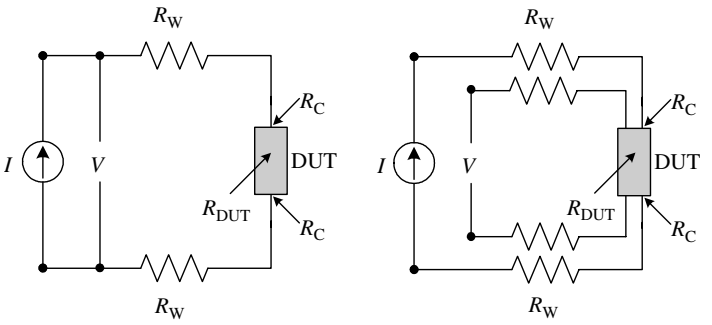



**Fig. 1.1** Two-terminal and four-terminal resistance measurement arrangements.

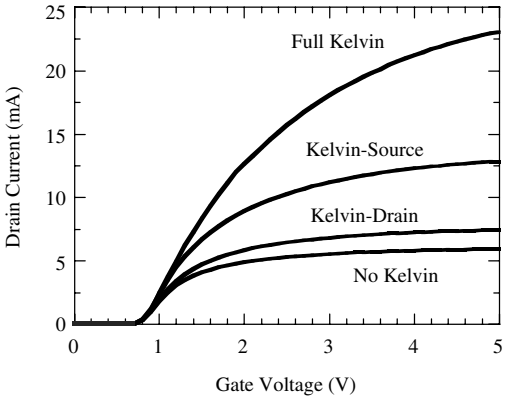



**Fig. 1.2** Effect of contact resistance on MOSFET drain current. Data courtesy of J. Wang, Arizona State University.

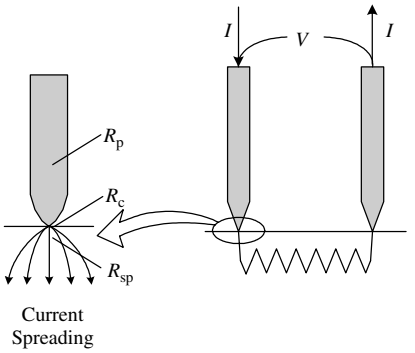



**Fig. 1.3** Two-point probe arrangement showing the probe resistance $R_p$, the contact resistance $R_c$, and the spreading resistance $R_{sp}$.

The four-point probe was originally proposed by Wenner[1] in 1916 to measure the earth's resistivity. The four-point probe measurement technique is referred to in Geophysics as *Wenner's method*. Valdes adopted it for semiconductor wafer resistivity measurements in 1954.[2] The probes are generally collinear, *i.e.*, arranged in-line with equal probe spacing, but other probe configurations are possible.[3]

---

**Exercise 1.1**

*Problem:* This exercise deals with data presentation. Frequently non-linear behavior is encountered in presenting data of semiconductor materials or devices, where one parameter may be proportional to another parameter to some power, *e.g.*, $y = Kx^b$, where both the prefactor $K$ and exponent $b$ are constant. One parameter may vary exponentially with another parameter, *e.g.*, $I = I_o \exp(\beta V)$. What is the best way to present the information to be able to extract "$b$" and "$\beta$"?

*Solution:* Consider the relationship $y = Kx^b = 8x^5$. Plots of $y$ versus $x$ on a linear scale, shown in Fig. E1.1(a) and (b), do not allow "$b$" do be determined, regardless what scale is used because the curves are non-linear. However, when the same data are plotted on a log-log plot as in (c), "$b$" is simply the slope of such a plot. In this case the slope is 5, because

$$\log(y) = \log(Kx^b) = \log(K) + \log(x^b) = \log(K) + b\log(x)$$

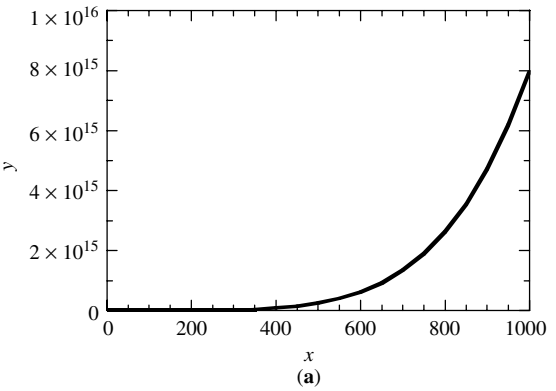
and the slope $m$ is

$$m = \frac{d[\log(y)]}{d[\log(x)]} = b = 5$$

If the data are plotted as in (d), which is also a log-log plot, the data must first be converted to "log" before the slope is taken. When that is done, the slope is again $m = 5$.

Let us now consider the relationship $y = y_o \exp(\beta x) = 10^{-14}\exp(40x)$. Obviously, a linear-linear plot, shown in (e), allows neither $y_o$ nor $\beta$ to be extracted. When, however, the data are plotted on a semilog plot, as in (f), we have

$$\ln(y) = \ln(y_o) + \beta x \Rightarrow \log(y) = \log(y_o) + \beta x/\ln(10)$$



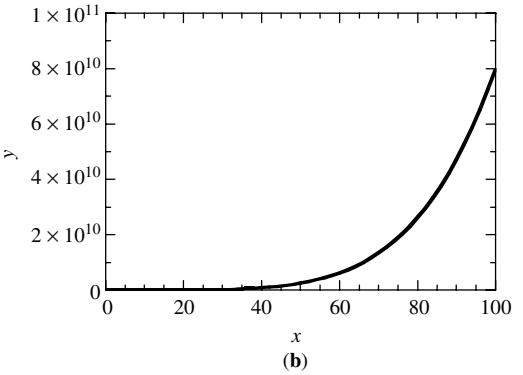
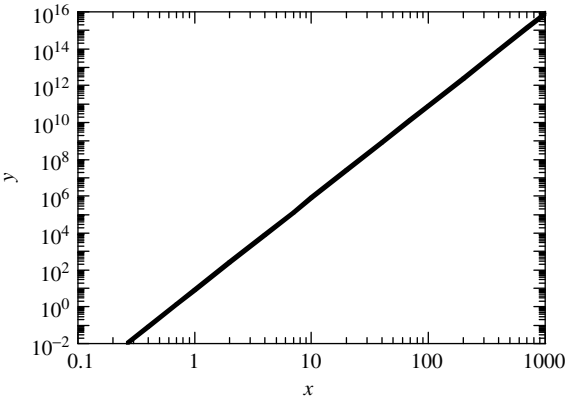
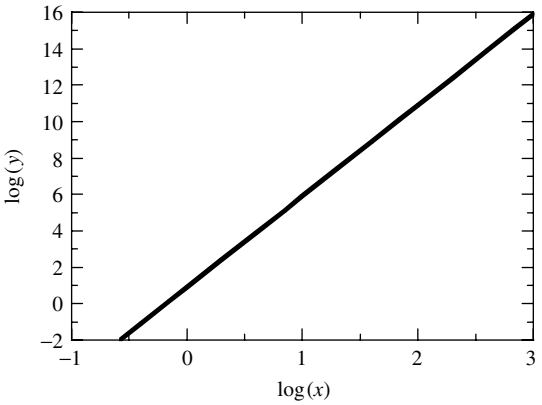



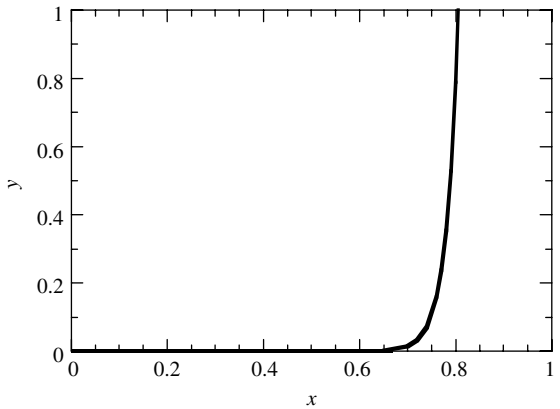

**Fig. E1.1**




(**c**)




(**d**)




(**e**)

**Fig. E1.1** (*continued*)

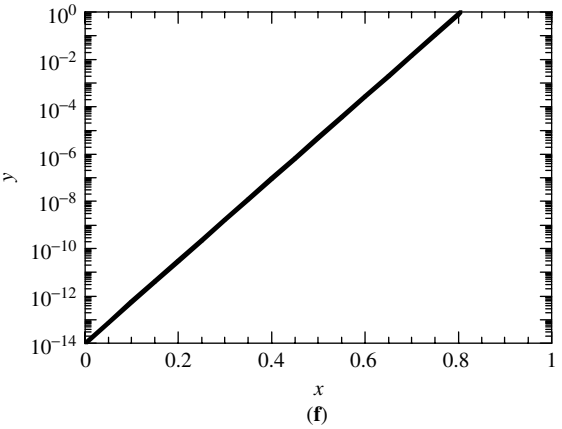



**Fig. E1.1** (*continued*)

The slope $m$ is

$$m = \frac{d[\log(y)]}{dx} = \frac{\beta}{\ln(10)} = \frac{\beta}{2.3036} = \frac{14}{2.3036 \times 0.8}$$

and the intercept at $x = 0$ is $y_o = 10^{-14}$.

---

To derive the four-point probe resistivity expression, we start with the sample geometry in Fig. 1.4(a). The electric field $\mathscr{E}$ is related to the current density $J$, the resistivity $\rho$, and the voltage $V$ through the relationship[2]

$$\mathscr{E} = J\rho = -\frac{dV}{dr};\ J = \frac{I}{2\pi r^2} \tag{1.3}$$

The voltage at point $P$ at a distance $r$ from the probe, is then

$$\int_0^V dV = -\frac{I\rho}{2\pi}\int_0^r \frac{dr}{r^2} \Rightarrow V = \frac{I\rho}{2\pi r} \tag{1.4}$$

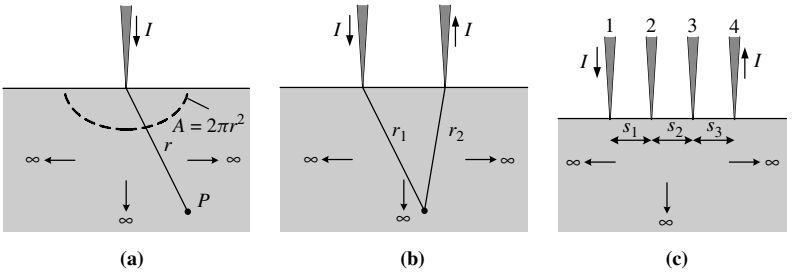



**Fig. 1.4** (a) one-point probe, (b) two-point, and (c) collinear four-point probe showing current flow and voltage measurement.

For the configuration in Fig. 1.4(b), the voltage is

$$V = \frac{I\rho}{2\pi r_1} - \frac{I\rho}{2\pi r_2} = \frac{I\rho}{2\pi}\left(\frac{1}{r_1} - \frac{1}{r_2}\right) \tag{1.5}$$

where $r_1$ and $r_2$ are the distances from probes 1 and 2, respectively. The minus sign accounts for current leaving through probe 2. For probe spacings $s_1$, $s_2$, and $s_3$, as in Fig. 1.4(c), the voltage at probe 2 is

$$V_2 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3}\right) \tag{1.6}$$

and at probe 3 it is

$$V_3 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1 + s_2} - \frac{1}{s_3}\right) \tag{1.7}$$

The total measured voltage $V = V_{23} = V_2 - V_3$ becomes

$$V = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3} - \frac{1}{s_1 + s_2} + \frac{1}{s_3}\right) \tag{1.8}$$

The resistivity $\rho$ is given by

$$\rho = \frac{2\pi}{(1/s_1 - 1/(s_1 + s_2) - 1/(s_1 + s_2) + 1/s_3)}\frac{V}{I} \tag{1.9}$$

usually expressed in units of ohm · cm, with $V$ measured in volts, $I$ in amperes, and $s$ in cm. The current is usually such that the resulting voltage is approximately 10 mV. For most four-point probes the probe spacings are equal. With $s = s_1 = s_2 = s_3$, Eq. (1.9) reduces to

$$\rho = 2\pi s\frac{V}{I} \tag{1.10}$$

Typical probe radii are 30 to 500 μm and probe spacings range from 0.5 to 1.5 mm. The spacings vary for different sample diameter and thickness.[4] For $s = 0.1588$ cm, $2\pi s$ is unity, and $\rho$ becomes simply $\rho = V/I$. Smaller probe spacings allow measurements closer to wafer edges, an important consideration during wafer mapping. Probes to measure metal films should not be mixed with probes to measure semiconductors. For some applications, *e.g.* magnetic tunnel junctions, polymer films, and semiconductor defects, microscopic four-point probes with probe spacings of 1.5 μm have been used.[5]

Semiconductor wafers are not semi-infinite in extent in either the lateral or the vertical dimension and Eq. (1.10) must be corrected for finite geometries. For an arbitrarily shaped sample the resistivity is given by

$$\boxed{\rho = 2\pi s F\frac{V}{I}} \tag{1.11}$$

where $F$ corrects for probe location near sample edges, for sample thickness, sample diameter, probe placement, and sample temperature. It is usually a product of several

independent correction factors. For samples thicker than the probe spacing, the simple, independent correction factors contained in $F$ of Eq. (1.11) are no longer adequate due to interactions between thickness and edge effects. Fortunately the samples are generally thinner than the probe spacings, and the correction factors can be independently calculated.

### 1.2.1 Correction Factors

Four-point probe correction factors have been calculated by the method of images,[2,6] complex variable theory,[7] the method of Corbino sources,[8] Poisson's equation,[9] Green's functions,[10] and conformal mapping.[11–12] We will give the most appropriate factors here and refer the reader to others where appropriate.

The following correction factors are for *collinear* or *in-line probes* with equal probe spacing, $s$. We write $F$ as a product of three separate correction factors

$$F = F_1 F_2 F_3 \tag{1.12}$$

Each of these factors can be further subdivided. $F_1$ corrects for sample thickness, $F_2$ for lateral sample dimensions, and $F_3$ for placement of the probes relative to the sample edges. Other correction factors are discussed later in the chapter.

Sample thickness must be corrected for most measurements since semiconductor wafers are not infinitely thick. A detailed derivation of thickness correction factors is given by Weller.[13] Sample thicknesses are usually on the order of the probe spacing or less introducing the correction factor[14]

$$F_{11} = \frac{t/s}{2\ln\{[\sinh(t/s)]/[\sinh(t/2s)]\}} \tag{1.13}$$

for a *non-conducting* bottom wafer surface boundary, where $t$ is the wafer or layer thickness. If the sample consists of a semiconducting layer on a semiconductor substrate, it is important that the layer be electrically isolated from the substrate. The simplest way to do this is for the two regions to be of opposite conductivity, *i.e.*, $n$-layer on a $p$-substrate or $p$-layer on an $n$-substrate. The space-charge region is usually sufficiently insulating to confine the current to the layer.

For a *conducting* bottom surface the correction factor becomes

$$F_{12} = \frac{t/s}{2\ln\{[\cosh(t/s)]/[\cosh(t/2s)]\}} \tag{1.14}$$

$F_{11}$ and $F_{12}$ are plotted in Fig. 1.5. Conducting bottom boundaries are difficult to achieve. Even a metal deposited on the wafer back surface does not ensure a conducting contact. There is always a contact resistance. Most four-point probe measurements are made with insulating bottom boundaries.

For thin samples Eq. (1.13) reduces to

$$F_{11} = \frac{t/s}{2\ln(2)} \tag{1.15}$$

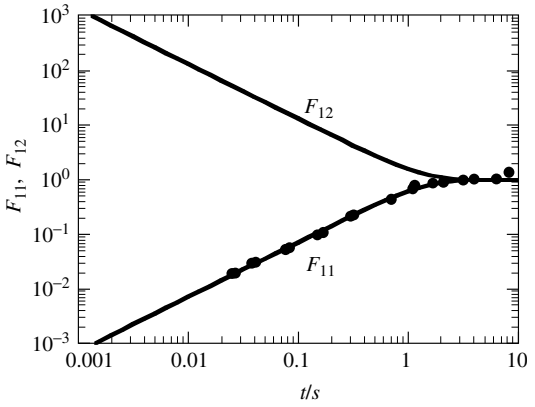



**Fig. 1.5** Wafer thickness correction factors versus normalized wafer thickness; $t$ is the wafer thickness, $s$ the probe spacing. The data points are taken from ref. 15.

using the approximation $\sinh(x) \approx x$ for $x \ll 1$. Eq. (1.15) is valid for $t \leq s/2$. For very thin samples that satisfy the conditions for $F_2$ and $F_3$ to be approximately unity, we find from Eqs. (1.11), (1.12), and (1.15)

$$\boxed{\rho = \frac{\pi}{\ln(2)} t \frac{V}{I} = 4.532 t \frac{V}{I}} \tag{1.16}$$

Thin layers are often characterized by their *sheet resistance* $R_{sh}$ expressed in units of ohms per square. The sheet resistance of uniformly doped samples is given by

$$\boxed{R_{sh} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \frac{V}{I} = 4.532 \frac{V}{I}} \tag{1.17}$$

subject to the constraint $t \leq s/2$. The sheet resistance characterizes thin semiconductor sheets or layers, such as diffused or ion-implanted layers, epitaxial films, polycrystalline layers, and metallic conductors.

The sheet resistance is a measure of the resistivity averaged over the sample thickness. The sheet resistance is the inverse of the sheet conductance $G_{sh}$. For *uniformly-doped* samples we find

$$R_{sh} = \frac{1}{G_{sh}} = \frac{1}{\sigma t} \tag{1.18}$$

where $\sigma$ is the conductivity and $t$ the sample thickness. For *non uniformly-doped* samples

$$R_{sh} = \frac{1}{\displaystyle\int_0^t [1/\rho(x)]\, dx} = \frac{1}{\displaystyle\int_0^t \sigma(x)\, dx} = \frac{1}{\displaystyle q \int_0^t [n(x)\mu_n(x) + p(x)\mu_p(x)]\, dx} \tag{1.19}$$

**Exercise 1.2**

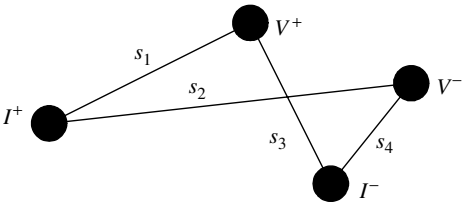



**Fig. E1.2**

*Problem:* Is there another way to derive the sheet resistance expression?

*Solution:* Consider a sample of thickness $t$ and resistivity $\rho$. The four probes are arranged as in Fig. E1.2. Current $I$ is injected at probe $I^+$ and spreads out cylindrically symmetric. By symmetry and current conservation, the current density at distance $r$ from the probe is

$$J = \frac{I}{2\pi r t}$$

The electric field is

$$\mathscr{E} = J\rho = \frac{I\rho}{2\pi r t} = -\frac{dV}{dr}$$

Integrating this expression gives the voltage drop between probes $V^+$ and $V^-$, located at distances $s_1$ and $s_2$ from $I^+$ as

$$\int_{V_{s1}}^{V_{s2}} dV = -\frac{I\rho}{2\pi t}\int_{s_1}^{s_2}\frac{dr}{r} \Rightarrow V_{s1} - V_{s2} = V_{12} = \frac{I\rho}{2\pi t}\ln\left(\frac{s_2}{s_1}\right)$$

By the principle of superposition, the voltage drop due to current injected at $I^-$ is

$$V_{34} = -\frac{I\rho}{2\pi t}\ln\left(\frac{s_3}{s_4}\right)$$

leading to

$$V = V_{12} - V_{34} = \frac{I\rho}{2\pi t}\ln\left(\frac{s_2 s_3}{s_1 s_4}\right)$$

For a collinear arrangement with $s_1 = s_4 = s$ and $s_2 = s_3 = 2s$

$$\rho = \frac{\pi t}{\ln(2)}\frac{V}{I}; R_{sh} = \frac{\pi}{\ln(2)}\frac{V}{I}$$

**Exercise 1.3**

*Problem:* What does *sheet resistance* mean and why does it have such strange units?

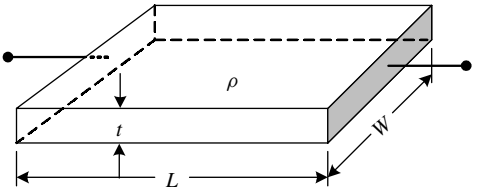



**Fig. E1.3**

*Solution:* To understand the concept of sheet resistance, consider the sample in Fig. E1.3. The resistance between the two ends is given by

$$R = \rho \frac{L}{A} = \rho \frac{L}{Wt} = \frac{\rho}{t} \frac{L}{W} \text{ ohms}$$

Since $L/W$ has no units, $\rho/t$ should have units of ohms. But $\rho/t$ is not the sample resistance. To distinguish between $R$ and $\rho/t$, the ratio $\rho/t$ is given the units of ohms/square and is named sheet resistance, $R_{sh}$. Hence the sample resistance can be written as

$$R = R_{sh} \frac{L}{W} \text{ ohms}$$

The sample is sometimes divided into squares, as in Fig. E1.4. The resistance is then given as

$$R = R_{sh} \text{ (ohms/square)} \times \text{Number of squares} = 5R_{sh} \text{ ohms}$$

Looking at it this way, the "square" cancels.

The sheet resistance of a semiconductor sample is commonly used to characterize ion implanted and diffused layers, metal films, etc. The depth variation of the dopant atoms need not be known, as is evident from Eq. (1.19). The sheet resistance can be thought of as the depth integral of the dopant atom density in the sample, regardless of its vertical spatial doping density variation. A few sheet resistances are plotted in Fig. E1.5 versus sample thickness as a function of sample resistivity. Also shown are typical values for Al, Cu and heavily-doped Si.

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**Exercise 1.4**

*Problem:* For the carrier density profiles in Fig. E1.6, do the sheet resistances of the three layers differ?

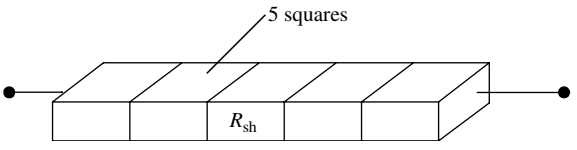


**Fig. E1.4**

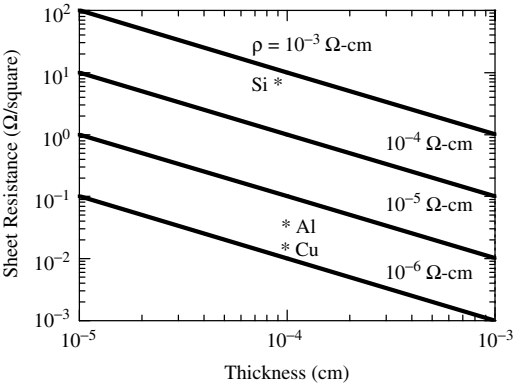


**Fig. E1.5**

*Solution:* Eq. (1.19) shows the sheet resistance to be inversely proportional to the conductivity-thickness product. For constant mobility, $R_{sh}$ is inversely proportional to the area under the curves in Fig. E1.6. Since the three areas are equal, this implies that $R_{sh}$ is the same for all three cases. In other words, it does not matter what the carrier distribution is, only the integrated distribution matters for $R_{sh}$.

---

Four-point probe measurements are subject to further sample size correction factors. For circular wafers of diameter $D$, the correction factor $F_2$ in Eq. (1.12) is given by[16]

$$F_2 = \frac{\ln(2)}{\ln(2) + \ln\{[(D/s)^2 + 3]/[(D/s)^2 - 3]\}} \tag{1.20}$$

$F_2$ is plotted in Fig. 1.6 for circular wafers. The sample must have a diameter $D \geq 40$ s for $F_2$ to be unity. For a probe spacing of 0.1588 cm, this implies that the wafer must be at least 6.5 cm in diameter. Also shown in Fig. 1.6 is the correction factor for rectangular samples.[6]

The correction factor 4.532 in Eq. (1.17) is for collinear probes with the current flowing into probe 1, out of probe 4, and with the voltage sensed across probes 2 and 3. For the current applied to and the voltage sensed across other probes, different correction factors obtain.[17] For probes *perpendicular* to and a distance $d$ from a *non-conducting boundary*, the correction factors, for infinitely thick samples, are shown in Fig. 1.7.[2] It is obvious from the figures that as long as the probe distance from the wafer boundary is at least

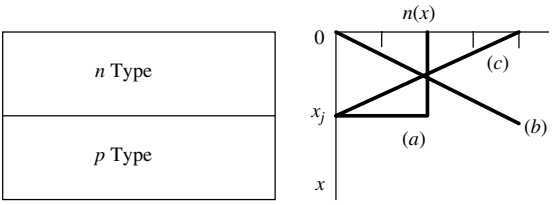


**Fig. E1.6**

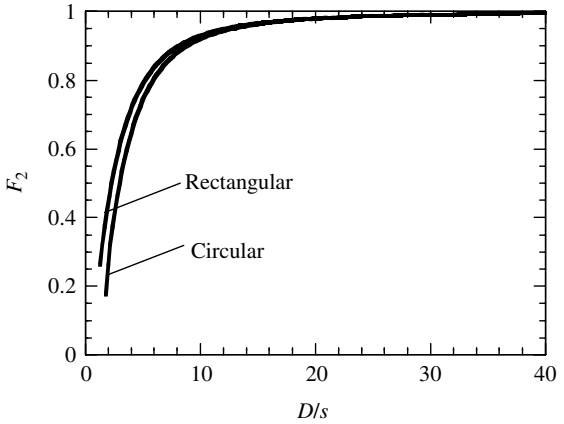


**Fig. 1.6** Wafer diameter correction factors versus normalized wafer diameter. For circular wafers: $D$ = wafer diameter; for rectangular samples: $D$ = sample width, $s$ = probe spacing.

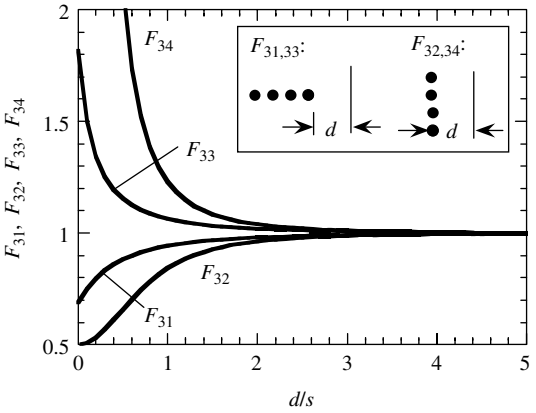


**Fig. 1.7** Boundary proximity correction factors versus normalized distance $d$ ($s$ = probe spacing) from the boundary. $F_{31}$ and $F_{32}$ are for non-conducting boundaries, $F_{33}$ and $F_{34}$ are for conducting boundaries.

three to four probe spacings, the correction factors $F_{31}$ to $F_{34}$ reduce to unity. For most four-point probe measurements this condition is easily satisfied. Correction factors $F_{31}$ to $F_{34}$ only become important for small samples in which the probe is, of necessity, close to the sample boundary.

Other corrections must be applied when the probe is not centered even in a wafer of substantial diameter.[16] For rectangular samples it has been found that the sensitivity of the geometrical correction factor to positional error is minimized by orienting the probe with its electrodes within about 10% of the center.[11] For square arrays the error is minimized by orienting the probe array with its electrodes equidistant from the midpoints of the sides. There is also an angular dependence of the placement of a square array on the rectangular

sample.[9, 11] We should mention that if the probe spacings are not exactly identical, there is a further small correction.[18]

The key to high precision four-point probe measurements, including reduced geometric effects associated with proximity of the probe to a non-conducting boundary, is the use of two measurement configurations at each probe location.[19–21] This technique is known as the "dual configuration" or as the "configuration switched" method. The first configuration is usually with current into probe 1 and out of probe 4 and with the voltage sensed across probes 2 and 3. The second measurement is made with current driven through probes 1 and 3 and voltage measured across probes 2 and 4. The advantages are: (i) the probe no longer needs to be in a high symmetry orientation (being perpendicular or parallel to the wafer radius of a circular wafer or to the length or width of a rectangular sample), (ii) the lateral dimensions of the specimen do not have to be known since the geometric correction factor results directly from the two measurements, and (iii) the two measurements self-correct for the actual probe spacings.

The sheet resistance in the dual configuration is given by[21]

$$R_{sh} = -14.696 + 25.173(R_a/R_b) - 7.872(R_a/R_b)^2 \tag{1.21}$$

where

$$R_a = \frac{V_{f23}/I_{f14} + V_{r23}/I_{r14}}{2};\ R_b = \frac{V_{f24}/I_{f13} + V_{r24}/I_{r13}}{2} \tag{1.22}$$

$V_{f23}/I_{f14}$ is the voltage/current across terminals 2,3 and 1,4 with the current in the forward direction and $V_{r23}/I_{r14}$ with the current in the reverse direction.

The resistivity of semiconductor ingots, measured with the four-point probe, is given by

$$\rho = 2\pi s \frac{V}{I} \tag{1.23}$$

only if the ingot diameter $D$ satisfies the relationship $D \geq 10$ s.[10, 22, 23]

### 1.2.2 Resistivity of Arbitrarily Shaped Samples

The collinear probe configuration is the most common four-point probe arrangement. Arrangement of the points in a square has the advantage of occupying a smaller area since the spacing between points is only s or $2^{1/2}$s, whereas in a collinear configuration the spacing between the outer two probes is 3s. The square arrangement is more commonly used, not as an array of four mechanical probes, but rather as contacts to square semiconductor samples.

The theoretical foundation of measurements on irregularly shaped samples is based on conformal mapping developed by van der Pauw.[24, 26] He showed how the specific resistivity of a flat sample of arbitrary shape can be measured without knowing the current pattern, if the following conditions are met: (1) the contacts are at the circumference of the sample, (2) the contacts are sufficiently small, (3) the sample is uniformly thick, and (4) the surface of the sample is singly connected, *i.e.*, the sample does not contain any isolated holes.

Consider the flat sample of a conducting material of arbitrary shape, with contacts 1, 2, 3, and 4 along the periphery as shown in Fig. 1.8 to satisfy the conditions above. The resistance $R_{12,34}$ is defined as

$$R_{12,34} = \frac{V_{34}}{I_{12}} \tag{1.24}$$

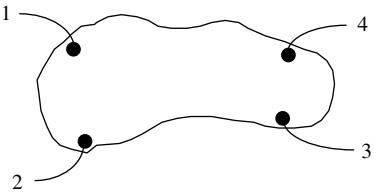


**Fig. 1.8** Arbitrarily shaped sample with four contacts.

where the current $I_{12}$ enters the sample through contact 1 and leaves through contact 2 and $V_{34} = V_3 - V_4$ is the voltage difference between the contacts 3 and 4. $R_{23,41}$ is defined similarly.

The resistivity is given by[24]

$$\rho = \frac{\pi}{\ln(2)} t \frac{(R_{12,34} + R_{23,41})}{2} F \tag{1.25}$$

where $F$ is a function only of the ratio $R_r = R_{12,34}/R_{23,41}$, satisfying the relation

$$\frac{R_r - 1}{R_r + 1} = \frac{F}{\ln(2)} \operatorname{ar\,cosh}\left(\frac{\exp[\ln(2)/F]}{2}\right) \tag{1.26}$$

The dependence of $F$ on $R_r$ is shown in Fig. 1.9.

For a *symmetrical* sample such as the circle or the square in Fig. 1.10, $R_r = 1$ and $F = 1$. This allows Eq. (1.25) to be simplified to

$$\boxed{\rho = \frac{\pi}{\ln(2)} t R_{12,34} = 4.532 t R_{12,34}} \tag{1.27}$$

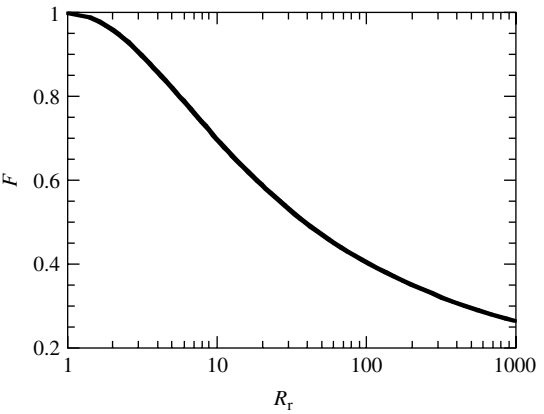


**Fig. 1.9** The van der Pauw correction factor $F$ versus $R_r$.

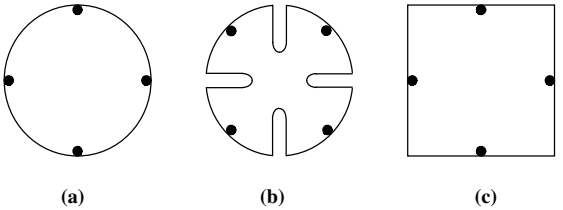


**Fig. 1.10** Typical symmetrical circular and square sample geometries.

The sheet resistance becomes

$$R_{sh} = \frac{\pi R_{12,34}}{\ln(2)} = 4.532 R_{12,34} \tag{1.28}$$

similar to the four-point probe expression in Eq. (1.17).

The van der Pauw equations are based on the assumption of negligibly small contacts located on the sample periphery. Real contacts have finite dimensions and may not be exactly on the periphery of the sample. The influence of non-ideal peripheral contacts is shown in Fig. 1.11. The correction factor $C$ is plotted as a function of the ratio of contact size to sample side length $d/l$. $C$ is defined as

$$\rho = C t R_{12,34}; \; R_{sh} = C R_{12,34} \tag{1.29}$$

Figure 1.11 shows that corner contacts introduce less error than contacts placed in the center of the sample sides. However, if the contact length is less than about 10% of the side length, the correction is negligible for either contact placement.

The error introduced by non-ideal contacts can be eliminated by the cloverleaf configuration of Fig. 1.10(b). Such configurations make sample preparation more complicated and are undesirable, so square samples are generally used. One of the advantages of the van der Pauw structure is the small sample size compared with the area required for four-point probe measurements. For simple processing it is preferable to use the circular or

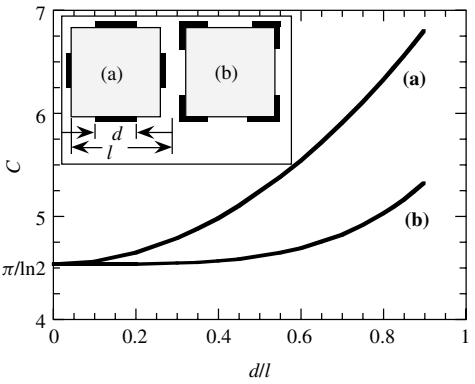


**Fig. 1.11** Correction factor $C$ versus $d/l$ for contacts at the center and at the corners of the square. Data after ref. 25.

square sample geometries shown in Fig. 1.10. For such structures it is not always possible to align the contacts exactly.

Geometries other than those in Fig. 1.10 are also used. One of these is the *Greek cross* in Fig. 1.12. Using photolithographic techniques, it is possible to make such structures very small and place many of them on a wafer for uniformity characterization. The sheet resistance of the shaded area is determined in such measurements. For structures with $L = W$, the contacts should be placed so that $d \leq L/6$ from the edge of the cross, where $d$ is the distance of the contact from the edge.[27] Surface leakage can introduce errors if $L$ is too large.[28] A variety of cross sheet resistor structures have been investigated and their performance compares well with conventional bridge-type structures.[29] The measured voltages in cross and van der Pauw structures are lower than those in conventional bridge structures.

The cross and the bridge structures are combined in the cross-bridge structure in Fig. 1.13, allowing the *sheet resistance* and the *line width* to be determined. The sheet resistance, determined in the shaded cross area, is

$$R_{sh} = \frac{\pi}{\ln(2)} \frac{V_{34}}{I_{12}} \tag{1.30}$$

where $V_{34} = V_3 - V_4$ and $I_{12}$ is the current flowing into contact $I_1$ and out of contact $I_2$.

The left part of Fig. 1.13 is a bridge resistor to determine the line width $W$. We mention the line width measurement feature only briefly here. Line width measurements are more fully discussed in Chapter 10. The voltage along the bridge resistor is

$$V_{45} = \frac{R_{sh} L I_{26}}{W} \tag{1.31}$$

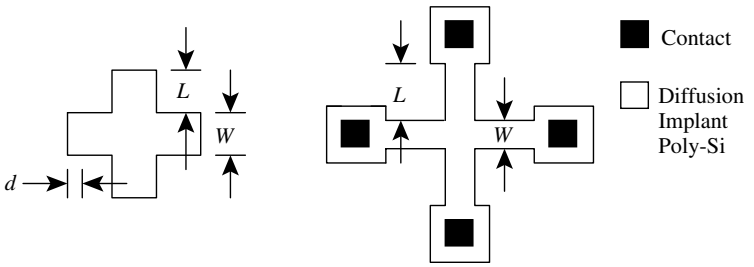


**Fig. 1.12** A Greek cross sheet resistance test structure. $d$ = distance of contact from edge.

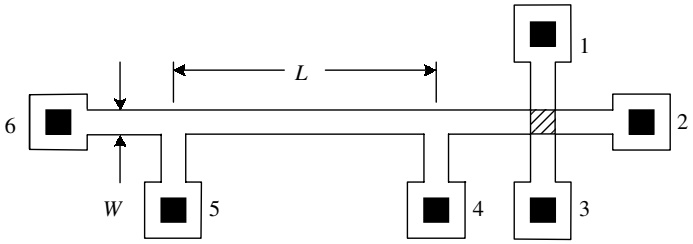


**Fig. 1.13** A cross bridge sheet resistance and line width test structure.

where $V_{45} = V_4 - V_5$ and $I_{26}$ is the current flowing from contact 2 to contact 6. From Eq. (1.31) the line width is

$$\boxed{W = \frac{R_{sh} L I_{26}}{V_{45}}} \tag{1.32}$$

with $R_{sh}$ determined from the cross structure and Eq. (1.30). A key assumption in this measurement is that the sheet resistance be identical for the entire test structure.

Since the bridge structure in Fig. 1.13 is suitable for resistance measurements, it can be used to characterize "dishing" during chemical-mechanical polishing of semiconductor wafers, where soft metal lines tend polish thinner in the central portion than at the edges leading to non-uniform thickness. This is particularly important for soft metals such as copper. With the resistance inversely proportional to metal thickness, resistance measurements can be used to determine the amount of dishing.[30]

### 1.2.3 Measurement Circuits

Four-point probe measurement circuits are given in various ASTM Standards. For example, ASTM F84[18] and F76[31] give detailed circuit diagrams. Today's equipment is supplied with computers to provide the current stimulus, measure the voltage and apply appropriate correction factors as well as provide the signals for the probe station stepping for wafer mapping.

### 1.2.4 Measurement Errors and Precautions

For four-point probe measurements to be successful a number of precautions must be taken and appropriate correction factors must be applied to the measured data.

*Sample Size:* As mentioned earlier, a number of corrections must be applied, depending on the location of the probe as well as sample thickness and size. For those cases where the wafer is uniformly doped in the lateral direction and its diameter is appreciably larger than the probe spacing, the wafer thickness is the chief correction. If the wafer or the layer to be measured is appreciably thinner than the probe spacing, the calculated resistivity varies directly with thickness. It is therefore very important to determine the thickness accurately for resistivity determination. For sheet resistance measurements the thickness need not be known.

*Minority/Majority Carrier Injection:* It is often stated that metal-semiconductor contacts do not inject minority carriers. That is not strictly true. Metal-semiconductor contacts do inject minority carriers, but their injection efficiency is low. However, under high current conditions it may not be negligible. Minority carrier injection causes *conductivity modulation* because increased minority carrier density leads to increased majority carrier density (to maintain charge neutrality) and subsequent enhanced conductivity. To reduce minority carrier injection, the surface should have a high recombination rate for minority carriers. This is best achieved by using lapped surfaces. For a highly polished wafer it may not be possible to achieve the necessary high surface recombination. Injected minority carriers will have decayed by recombination and cause very little error for voltage probes 3–4 minority carrier diffusion lengths from the injecting current probe. However, for high lifetime material the diffusion length may be longer than the probe spacing, and the measured resistivity will be in error. Another possible source of error is the *probe pressure-induced band gap narrowing* leading to enhanced minority carrier injection.

Minority carrier injection may be important for high resistivity materials. For silicon this applies for $\rho \geq 100$ ohm · cm. An error of less than 2% is introduced by minority carrier injection if the voltage across the two voltage-sensing probes is held to less than 100 mV for 1 mm probe spacings for samples with lapped surfaces. If the current density exceeds the value $J = qnv$, where $n \approx N_D$ for $n$-type samples and $v$ is the thermal velocity, excess *majority* carriers can be injected into the sample, causing the resistivity to change. Majority carrier injection is usually of little concern if the four-point probe voltage does not exceed 10 mV.

*Probe Spacing:* A mechanical four-point probe exhibits small random probe spacing variations. Such variations give erroneous values of resistivity or sheet resistance, especially when evaluating uniformly doped wafers. In such cases it is very important to know whether any non-uniformities are due to the wafer, due to process variations, or due to measurement errors. An example is the evaluation of ion-implanted layers. It is known that ion-implanted layers can have sheet resistance uniformities better than 1%. For small probe spacing variations the correction factor[18]

$$F_S \approx 1 + 1.082(1 - s_2/s_m) \tag{1.33}$$

must be applied, where $s_2$ is the spacing between the inner two probes and $s_m$ is the mean value of the probe spacings. Errors due to probe wander can be reduced by averaging several independent readings.

*Current:* Additional sources of error are the current amplitude and surface leakage current. The current can affect the measured resistivity in two ways: by an apparent resistivity increase produced by wafer heating and by an apparent resistivity decrease due to minority and/or majority carrier injection. The suggested four-point probe measurement current for silicon wafers is shown in Fig. 1.14 as a function of resistivity and sheet resistance.[18] The data were obtained by measuring the four-point probe resistivity as a function of current for a given sample. Such resistivity-current curves show typically a flat region bounded by non-linearities at both low and high currents. The flat region gives the appropriate current. Surface leakage is reduced or eliminated by enclosing the probe in a shielded enclosure held at a potential equal to the inner probe potential.

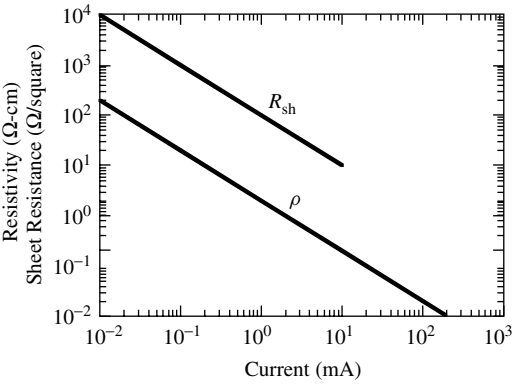


**Fig. 1.14** Recommended four-point probe current versus Si sheet resistance and resistivity.

*Temperature:* It is important that the sample temperature be uniform in order not to introduce thermoelectric voltages. Temperature gradients can be caused by ambient effects but are more likely due to sample heating by the probe current. Current heating is most likely to occur in low resistivity samples where high currents are required to obtain readily measurable voltages.

Even if temperature variations are not caused by the measurement apparatus and there are no temperature gradients, there may still be temperature variations due to temperature fluctuations in the measurement room. Since semiconductors have relatively large temperature coefficients of resistivity, errors are easily introduced by failing to compensate for such temperature variations ($n$- and $p$-Si[18] and for $n$- and $p$-Ge).[32] For resistivities of 10 ohm · cm or higher, the Si coefficient is on the order of 1%/°C. Temperature corrections are made by using the correction factor[18]

$$F_T = 1 - C_T(T - 23) \tag{1.34}$$

where $C_T$ is the temperature coefficient of resistivity and $T$ is the temperature in °C.

*Surface Preparation:* Proper surface preparation is important for high sheet resistance Si measurements. For example, positive charge on the surface of a $p$-type layer on an $n$-type wafer, leads to a surface charge-induced space-charge region leaving only a portion of the layer in its neutral state. This, of course, increases the thickness-dependent sheet resistance. Similarly, a positive surface charge on an $n$-type implanted layer, leads to surface accumulation and a sheet resistance reduction. An example of this effect is shown in Fig. 1.15. Wafers dipped into boiling water or into $H_2SO_4$ or $H_2O_2$ exhibit stabilized surfaces while those etched in HF exhibit a time-dependent sheet resistance.[33]

*High Resistivity, High Sheet Resistance Materials:* Materials of very high resistivity are more difficult to measure by four-point probe or van der Pauw methods. Moderately doped wafers can become highly resistive at low temperatures and are similarly difficult

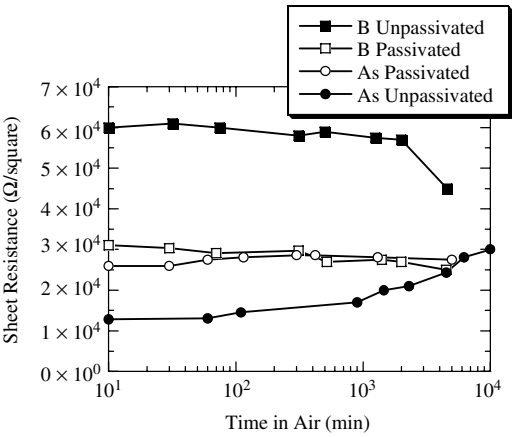


**Fig. 1.15** Sheet resistance versus time in room temperature air. $B$ implant: $8 \times 10^{11}$ cm$^{-2}$, 70 keV through 59 nm oxide into $n$-Si substrate, annealed 1050°C, 15 s; As implant: $8 \times 10^{11}$ cm$^{-2}$ into bare $p$-Si substrate, annealed 1000°C, 30 min. Both passivated in boiling water for 10 min. After ref. 33.

to measure. Special measurement precautions must be observed. Thin semiconductor films usually have high sheet resistance. These include lightly doped layers, polycrystalline Si films, amorphous Si films, silicon-on-insulator, *etc*. It is possible to make four-point probe measurements with sheet resistances up to about $10^{10}-10^{11}$ ohms/square, provided one uses a stable low current as low as picoamperes. A further consideration is penetration of the probes through shallow implanted layers. One solution to this problem is to use mercury four-point probes instead of metal "needles".

A measurement for high-resistivity bulk wafers relies on providing the wafer with a large contact on one side and a small contact on the other side. A current is passed through the contacts and the voltage is measured. This arrangement, by itself, can suffer from surface leakage currents. By surrounding the small contact with a guard ring and holding the guard ring at the same or nearly the same potential as the small contact, surface currents are essentially suppressed.[34] It is of course necessary to ensure that the contacts are ohmic or as close to ohmic as possible so that the bulk resistivity and not the contact resistance is measured.

Two-terminal measurements are notorious for being complicated by contact effects and the true sample resistivity is not easy to determine as indicated by Eq. (1.2). Conventional van der Pauw measurements suitable for moderate or low resistivity materials are suspect for high resistance samples unless care is taken to eliminate current leakage paths and sample loading by the voltmeter. One approach around this problem is the "guarded" approach using high input impedance, unity gain amplifiers between each probe on the sample, and the external circuitry.[35] The unity gain amplifiers drive the shields on the leads between the amplifier and the sample, thereby effectively eliminating the stray capacitance in the leads. This reduces leakage currents and the system time constant. Measurements of resistances up to $10^{12}$ ohms have been made with such a system. The "guarded" approach can also be automated.[36]

## 1.3 WAFER MAPPING

Wafer mapping, originally developed to characterize ion implantation uniformity, has become a powerful process monitoring tool. Manual wafer mapping originated in the 1970s.[37] Today, highly automated systems are used. During wafer mapping the sheet resistance or some other parameter proportional to ion implant dose is measured at many locations across a sample. The data are then converted to two-dimensional or three-dimensional contour maps. Contour maps are a more powerful display of process uniformity than displaying the same data in tabular form. A well-designed contour map gives instant information about ion implant uniformity, flow patterns during diffusion, epitaxial reactor non-uniformities, *etc*. If desired, line scans along one line across the sample can also be displayed to show the uniformity along that line.

The most common sheet resistance wafer mapping techniques are: four-point probe sheet resistance, modulated photoreflectance, and optical densitometry.[38] Of these, the configuration-switched four-point probe method is commonly used. It allows for rapid comparison between samples and has been used for ion implantation, diffusion, poly-Si films, and metal uniformity characterization.[39] Example wafer maps are shown in Fig. 1.16.

### 1.3.1 Double Implant

Precaution needs to be taken to measure the sheet resistance of low-dose, single implanted layers by the four-point probe technique, because (1) it is difficult to make good electrical

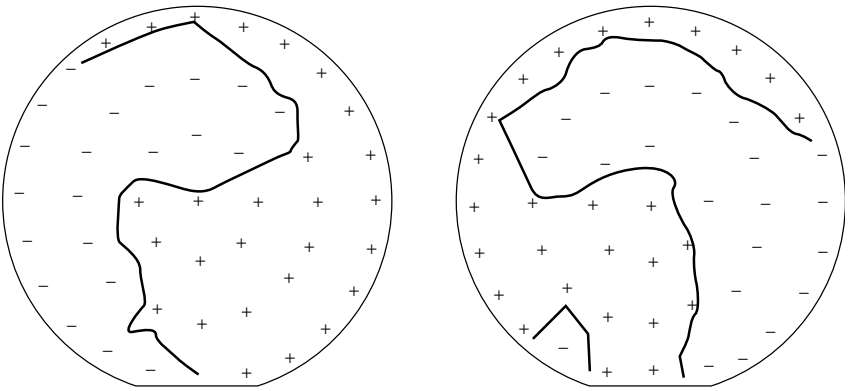

**Fig. 1.16** Four-point probe contour maps; (a) boron, $10^{15}$ cm$^{-2}$, 40 keV, $R_{sh}$(average) = 98.5 ohms/square; (a) arsenic, $10^{15}$ cm$^{-2}$, 80 keV, $R_{sh}$(average) = 98.7 ohms/square; 1% intervals. 200 mm diameter Si wafers. Data courtesy of Marylou Meloni, Varian Ion Implant Systems.

contact from the probe to the semiconductor, (2) low doses give low carrier densities and low conductivity, and (3) the surface leakage current can be comparable to the measurement current. The conventional four-point probe method can be used provided the starting wafers are of high resistivity, and they are oxidized before the implant to stabilize the surface resistance and to prevent ion channeling. The wafer is implanted and annealed, the oxide is stripped, and the surface is stabilized in a hot sulfuric acid and hydrogen peroxide solution (piranha etch).

A modified four-point probe method, the *double implant technique*, is sometimes used for sheet resistance measurements of such layers.[20, 40] It is implemented as follows: A $p$-type ($n$-type) impurity is implanted into an $n$-type ($p$-type) substrate at a dose $\Phi_1$ and energy $E_1$. For example, boron is implanted at a dose of $\Phi_1 = 10^{14}$ cm$^{-2}$ and energy $E_1 = 120$ keV. The wafer is annealed to activate the implanted ions electrically. The sheet resistance $R_{sh1}$ is measured and the data are stored. Next the desired low-dose impurity is implanted at dose $\Phi_2$ and energy $E_2$, with $\Phi_2 < \Phi_1$. $E_2$ should be less than $E_1$ to prevent penetration through the first implant layer. The first implant energy is typically at least 10–20% higher, and the first implant dose is at least two orders of magnitude higher than the second implant. The second implant conditions might be $\Phi_2 = 10^{11}$ cm$^{-2}$ and $E_2 = 100$ keV. The sheet resistance $R_{sh2}$ after the second implant is measured and compared to $R_{sh1}$ *without* annealing the second implant.

The second sheet resistance measurement relies on the implant damage of the second implant being proportional to the implant dose. This is true for low implant doses. Implanted, but not activated ions, do not contribute to electrical conduction. Furthermore, due to implant damage, the mobility is reduced making $R_{sh2} > R_{sh1}$. The impurity atomic mass of the first implant should be approximately the same mass as the second implant. It has also been found that (111)-oriented Si wafers are preferred over (100)-oriented wafers to reduce channeling effects. The double-implant method allows measurements immediately after the second implant. Implant doses as low as $10^{10}$ cm$^{-2}$ can be measured by this technique. Test wafers can be annealed and reused, provided the anneal temperature is kept sufficiently low to prevent impurity redistribution. The method is also applicable for electrically inactive species, such as oxygen, argon, or nitrogen implants. A more detailed discussion is given in Smith et al.[40]

The double-implant technique suffers from several problems. Any sheet resistance nonuniformities resulting from the first implant and its activation cycle alter the low-dose measurement. Additionally, since this method derives its low-dose sensitivity from ion-implant *damage*, it is sensitive to post-implant relaxation, where implant damage anneals itself over a period of hours to days following the implant. If the measurement is made immediately after the second implant, damage relaxation has little effect. However, if the measurement is made several hours or days after the implant, damage relaxation can reduce the measured resistance by 10–20% for the types of implant doses and energies typical for low-dose implants. The measurement stability is improved by a 200°C, dry $N_2$ anneal for 45 min before making the measurement.[40]

### 1.3.2 Modulated Photoreflectance

Modulated photoreflectance is the modulation of the optical reflectance of a sample in response to waves generated when a semiconductor sample is subjected to periodic heat stimuli. In the *modulated photoreflectance* or *thermal wave* method an $Ar^+$ ion laser beam, incident on the semiconductor sample, is modulated at a frequency of 0.1 to 10 MHz, creating transient thermal waves near the surface that propagate at different speeds in damaged and crystalline regions. Hence, signals from regions with various damages differ, leading to a measure of crystal damage. The thermal wave diffusion length at a 1 MHz modulation frequency is 2 to 3 μm.[41] The small temperature variations cause small volume changes of the wafer near the surface and the surface expands slightly.[42] These changes include both thermoelastic and optical effects,[43] and they are detected with a second laser—the probe beam—by measuring the reflectivity change. The apparatus is illustrated in Fig. 1.17. Both pump and probe laser beams are focused to approximately 1 μm diameter spots, allowing measurements not only on uniformly implanted wafers but also on patterned wafers.

Modulated photoreflectance is commonly used to determine the implant dose of ion implanted wafers. Conversion from thermal wave signal to implant dose requires calibrated standards with known implant doses. The ability to determine ion-implant doses by thermal waves depends on the conversion of the single crystal substrate to a partially

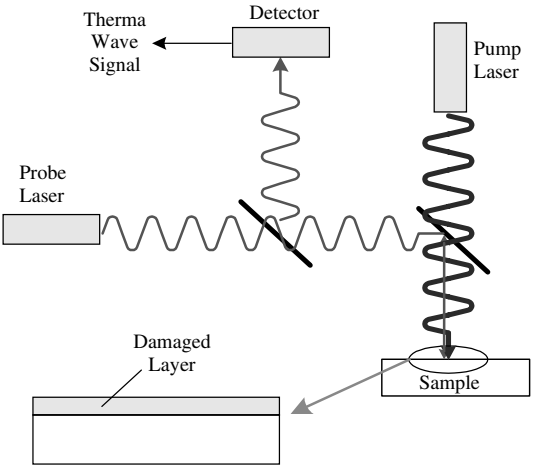


**Fig. 1.17** Schematic diagram of the modulated photoreflectance apparatus.

disordered layer by the implant process. The thermal wave-induced thermoelastic and optical effects are changed in proportion to the number of implanted ions. Modulated photoreflectance implant monitoring is subject to post-implant damage relaxation. However, the laser detection scheme accelerates the damage relaxation process, and the sample stabilizes within a few minutes.

The technique is contactless and non-destructive and has been used to measure implant doses from $10^{11}$ to $10^{15}$ $cm^{-2}$.[44] Measurements can be made on bare and on oxidized wafers. The ability to characterize oxidized samples has the advantage of allowing measurements of implants through an oxide. The technique can discriminate between implant species since the lattice damage increases with implant atom size and the thermal wave signal depends on the lattice damage. It has been used for ion implantation monitoring, wafer polish damage, and reactive and plasma etch damage studies. Its chief strength lies in the ability to detect low-dose implants contactless and to display the information as contour maps. Example contour maps are shown in Fig. 1.18.

### 1.3.3 Carrier Illumination (CI)

Somewhat similar to modulated photoreflectance is *carrier illumination*, to determine junction depth. Optical characterization of activated shallow junctions requires high contrast between the active implant and the underlying layer. The index of refraction of the doped layer is slightly higher than the underlying silicon by virtue of its higher conductivity. However, this is insufficient to enable measurement using conventional methods. In carrier illumination, a focused laser ($\lambda = 830$ nm) injects excess carriers into the semiconductor, forming a dc excess carrier distribution and a $\lambda = 980$ nm probe beam measures the reflectance.[45] The carrier distribution is deduced from the reflected signal. The carrier density in the substrate is flat, and falls rapidly at the junction edge. This creates a steep gradient in the index of refraction at the edge of the doping profile. The index of refraction change $\Delta n$ relates to the excess carrier density $\Delta N$ as

$$\Delta n = \frac{q^2 \Delta N}{2K_s \varepsilon_o m^* \omega^2} \tag{1.35}$$

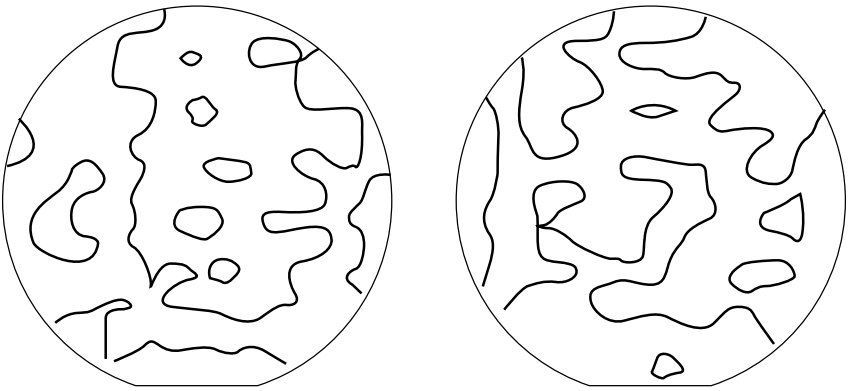

**Fig. 1.18** Modulated photoreflectance contour maps; (a) boron, $6.5 \times 10^{12}$ $cm^{-2}$, 70 keV, 648 TW units; (a) boron, $5 \times 10^{12}$ $cm^{-2}$, 30 keV, 600 TW units; 0.5% intervals. 200 mm diameter Si wafers. Data courtesy of Marylou Meloni, Varian Ion Implant Systems.

where $\omega$ is the radial frequency of the light. Light is reflected from this distribution and interference with a reference leads to an interference signal correlating directly to the junction depth. By slowly modulating the laser generating the excess carriers, thereby maintaining the static distribution conditions, it is possible to use sensitive phase-locked methods to obtain a reflection signal with several orders of magnitude gain over a dc measurement.

The method works best for layers with active doping densities in excess of $10^{19}$ cm$^{-3}$ to avoid high-level injection conditions in the active implanted region. High depth resolution is achieved because of the high index of refraction of the semiconductor. The measurement wavelength in silicon is about 270 nm, and a full $2\pi$ phase shift occurs in 135 nm. With a noise-limited phase resolution better than 0.5°, the depth resolution is about 0.2 nm. In addition to junction depth measurements, CI has been shown to be sensitive to the active dopant density and the profile abruptness and can also measure the thickness of the amorphous depth after a pre-amorphizing implant, making the CI method very sensitive for monitoring as-implanted low-dose ion implants.[46]

### 1.3.4 Optical Densitometry

In *optical densitometry* the doping density is determined by a technique entirely different from any of the methods discussed in this chapter. The method was developed for ion implantation uniformity and dose monitoring and does not use semiconductor wafers. A transparent substrate, typically glass, is coated with a thin film consisting of a polymer carrier and an implant sensitive radiochromic dye. During implant, the dye molecule undergoes heterolytic cleavage, resulting in positive ions with a peak light absorption at a wavelength of 600 nm.[47] When this polymer-coated glass wafer is ion implanted, the film darkens. The amount of darkening depends on the implant energy, dose, and species.

The optical densitometer, using a sensitive microdensitometer, detects the transparency of the entire wafer before and after implant and compares the final-to-initial difference in optical transparency with internal calibration tables. The optical transparency is measured over the entire implanted wafer and then displayed as a contour map. Calibration curves of optical density as a function of implant dose have been developed for implant doses from $10^{11}$ to $10^{13}$ cm$^{-2}$.

The method requires no implantation activation anneal and the results can be displayed within a few minutes of the implantation. The optical density is measured with about 1 mm resolution and lends itself well to ion doses as low $10^{11}$ cm$^{-2}$. As discussed earlier in this chapter, the doping density of low-dose implants is not easy to measure electrically, and this optical method is a viable alternate technique. It is also very stable. Table 1.1 compares three mapping techniques.[38]

## 1.4 RESISTIVITY PROFILING

A four-point probe measures the sheet resistance. The resistivity is obtained by multiplying by the sample thickness with the correct resistivity obtained only for *uniformly*-doped substrates. For non-uniformly doped samples, the sheet resistance measurement averages the resistivity over the sample thickness according to Eq. (1.19). The resistivity *profile* of a non-uniformly doped layer cannot be determined from a single sheet resistance measurement. Furthermore it is usually the dopant density profile that is desired, not the resistivity profile.

**TABLE 1.1 Mapping Techniques for Ion Implantation Uniformity Measurements.**

| | Four-Point Probe | Double Implant | Spreading Resistance | Modulated Photoreflectance | Optical Densitometry |
|---|---|---|---|---|---|
| Type | Electrical | Electrical | Electrical | Optical | Optical |
| Measurement | Sheet Resistance | Crystal Damage | Spreading Resistance | Crystal Damage | Polymer Damage |
| Resolution ($\mu$m) | 3000 | 3000 | 5 | 1 | 3000 |
| Species | Active | Active, Inactive | Active | Inactive | Inactive |
| Dose Range ($cm^{-2}$) | $10^{12}-10^{15}$ | $10^{11}-10^{14}$ | $10^{11}-10^{15}$ | $10^{11}-10^{15}$ | $10^{11}-10^{13}$ |
| Results | Direct | Calibration | Calibration | Calibration | Calibration |
| Relaxation | Minor | Serious | Minor | Serious | Serious |
| Requires | Anneal | Initial Implant | Anneal | | Measure before and after |

Suitable techniques for determining dopant density profiles include the differential Hall effect, spreading resistance, capacitance-voltage, MOSFET threshold voltage, and secondary ion mass spectrometry. We will discuss the first two methods in this chapter and defer discussion of the others to Chapter 2.

### 1.4.1 Differential Hall Effect (DHE)

To determine a resistivity or dopant density depth profile, depth information must be provided. It is possible to measure the resistivity profile of a non-uniformly doped sample by measuring the resistivity, removing a thin layer of the sample, measuring the resistivity, removing, measuring, *etc*. The *differential Hall effect* is such a measurement procedure. The sheet resistance of a layer of thickness $(t - x)$ is given by

$$R_{sh} = \frac{1}{q\int_x^t [n(x)\mu_n(x) + p(x)\mu_p(x)]\,dx} \tag{1.36}$$

where $x$ is the coordinate from the surface into the sample as illustrated in Fig. 1.19. If the sample is a thin layer, it must be separated from the substrate by an insulating layer to confine the four-point probe current to the layer. For example, an $n$-type implant into a $p$-substrate is suitable, with the space-charge region of the resulting np junction acting as an "insulating" boundary. An $n$-type implant into an $n$-substrate is not suitable as the measuring current is no longer confined to the $n$-layer.

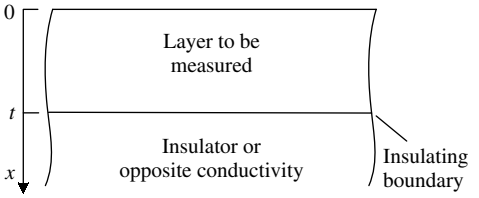


**Fig. 1.19** Sample geometry with measurement proceeding from the surface into the sample.

The sheet resistance of a uniformly doped layer with constant carrier densities and mobilities is

$$R_{sh} = \frac{1}{q(n\mu_n + p\mu_p)t} \tag{1.37}$$

The sheet resistance is a meaningful descriptor not only for uniformly doped layers but also for non-uniformly doped layers, where both carrier densities and mobilities are depth dependent. In Eq. (1.36) $R_{sh}$ represents an averaged value over the sample thickness $(t - x)$. Obviously, for $x = 0$, the sheet resistance is given by Eq. (1.19).

The sheet resistance is measured by the Hall effect or with a four-point probe as a function of depth by incremental layer removal. A plot of $1/R_{sh}(x)$ versus $x$ leads to the sample conductivity $\sigma(x)$ according to the equation[48]

$$\frac{d[1/R_{sh}(x)]}{dx} = -q[n(x)\mu_n(x) + p(x)\mu_p(x)] = -\sigma(x) \tag{1.38}$$

Equation (1.38) is derived from (1.36) using Leibniz's theorem

$$\frac{d}{dc}\int_{a(c)}^{b(c)} f(x,c)\,dx = \int_{a(c)}^{b(c)} \frac{\partial}{\partial c}[f(x,c)]\,dx + f(b,c)\frac{\partial b}{\partial c} - f(a,c)\frac{\partial a}{\partial c} \tag{1.39}$$

The resistivity is determined from Eq. (1.38) and from the identity $\rho(x) = 1/\sigma(x)$ as

$$\rho(x) = -\frac{1}{d[1/R_{sh}(x)]/dx} = \frac{R_{sh}^2(x)}{dR_{sh}(x)/dx} = \frac{R_{sh}(x)}{d[\ln(R_{sh}(x))]/dx} \tag{1.40}$$

The dopant density determined by this method is illustrated in Exercise 1.5. Dopant density profiles determined by DHE, spreading resistance profiling, and secondary ion mass spectrometry are shown in Fig. 1.20.

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**Exercise 1.5**

*Problem:* Given the sheet resistance versus depth plot of an $n$-Si layer on a $p$-Si substrate in Fig. E1.7(a), determine the resistivity and the doping density as a function of depth.

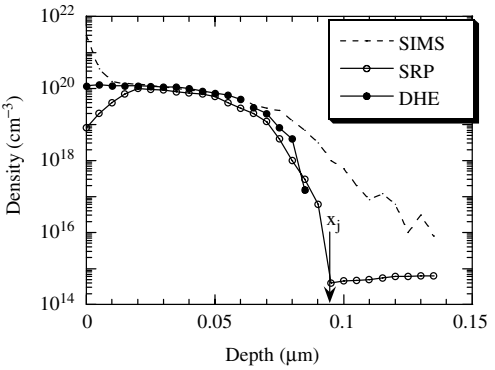
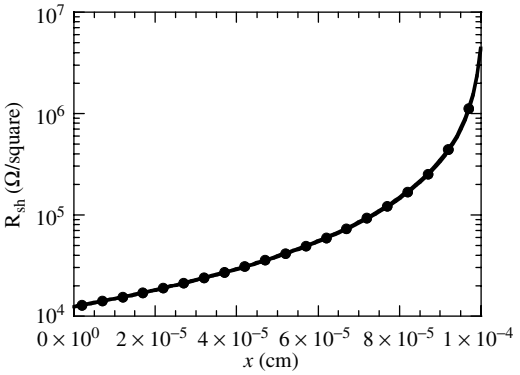
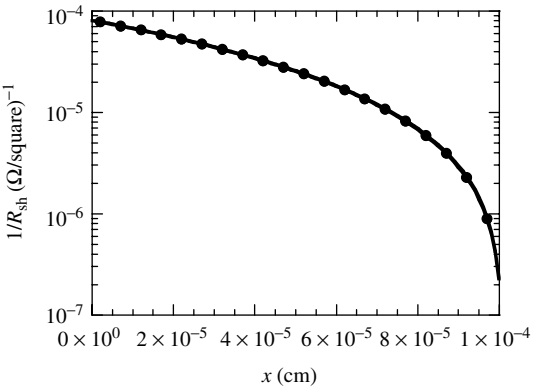


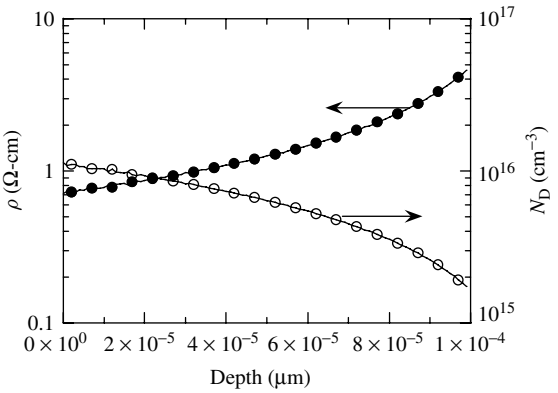

**Fig. 1.20** Dopant density profiles determined by DHE, spreading resistance profiling, and secondary ion mass spectrometry. Data after ref. 49. Reprinted from the Jan. 1993 edition of *Solid State Technology*.




(**a**)




(**b**)




(**c**)

**Fig. E1.7**

*Solution:* Determine the slope of this plot as a function of $x$. Then determine $\rho(x)$ versus $x$ using Eq. (1.40). Remember, in problems where the data are given in terms of "log" as in the figure above, you need to use the conversion "$\ln(10)\ln(x) = \log(x)$". The resistivity and doping density data so derived are shown in Figs. E1.7(b) and (c). Conversion of "$\rho$ to $N_D$" used a mobility of 800 $cm^2/V \cdot s$.

---

A word of caution regarding sheet resistance measurements of thin layers is in order here. Surface charges can induce space-charge regions at the sample surface. If that happens, then the neutral layer that governs the sheet resistance is thinner than the physical layer, introducing an error into the measurement. It is generally not a problem for Si, but can be a problem for GaAs, where surface charge-induced space-charge regions are very common. Corrections need to be applied then.[50–51]

Repeated removal of well-controlled thin layers from a heavily-doped semiconductor is difficult to do by chemical etching. It can, however, be done with *anodic oxidation*. During anodic oxidation a semiconductor is immersed in a suitable electrolyte in an anodization cell. A current is passed from an electrode to the semiconductor sample through the electrolyte, causing an oxide to grow at room temperature. The oxide grows by consuming a portion of the semiconductor. By subsequently etching the oxide, that portion of the semiconductor consumed during the oxidation is removed as well. This can be done very reproducibly.

Two anodization methods are possible. In the *constant voltage* method, the anodization current is allowed to fall from an initial to a final predetermined value. In the *constant current* method, the voltage is allowed to rise until a preset value is attained. The oxide thickness is directly proportional to the net forming voltage in the constant current anodization method, where the net forming voltage is the final cell voltage minus the initial cell voltage.

A variety of anodization solutions have been used. The non-aqueous solutions *N*-methylacetamide, tetrahydrofurfuryl alcohol and ethylene glycol are suitable for silicon.[52] Ethylene glycol containing 0.04N $KNO_3$ and 1–5% water produces uniform, reproducible oxides at current densities of 2 to 10 $mA/cm^2$. For the ethylene glycol mixture 2.2 Å of Si are removed per volt.[52] A forming voltage of 100 V removes 220 Å of Si. Ge[53], InSb[54], and GaAs[55] have all been anodically oxidized.

The laborious nature of the differential conductivity profiling technique limits its applicability if the entire process is done manually. The measurement time can be substantially reduced by automating the method. Computer-controlled experimental methods have been developed in which the sample is anodized, etched and then the resistivity and the mobility are measured *in situ*.[49, 56–57]

### 1.4.2 Spreading Resistance Profiling (SRP)

The *spreading resistance probe* technique has been in use since the 1960s. Although originally used for lateral resistivity variation determination, it is mainly used today to generate resistivity and dopant density *depth profiles*. It has very high dynamic range ($10^{12}$–$10^{21}$ $cm^{-3}$) and is capable of profiling very shallow junctions into the nm regime. Substantial progress has been made in data collection and treatment. The latter relates to improved sample preparation and probe conditioning procedures, specialized constrained cubic spline smoothing schemes, universally applicable Schumann-Gardner-based correction factors with appropriate radius calibration procedures, and the development of

physically based Poisson schemes for the correction of the carrier diffusion (spilling) phenomenon. Reproducibility is sometimes mentioned as an SRP problem. Reproducibility of 10% can be obtained routinely by "qualified" SRP systems, provided qualification procedures are rigorously implemented.[58]

The spreading resistance concept is illustrated in Fig. 1.21. The instrument consists of two carefully aligned probes that are stepped along the beveled semiconductor surface. The resistance between the probes is given by

$$R = 2R_p + 2R_c + 2R_{sp} \tag{1.41}$$

where $R_p$ is the probe resistance, $R_c$ the contact resistance and $R_{sp}$ the spreading resistance. The resistance is measured at each location.[59]

The sample is prepared by mounting it on a bevel block with melted wax. Bevel angles less than 1° can be readily prepared. The bevel block is inserted into a well-fitting cylinder, and the sample is lapped using a diamond paste or other polishing compound. Sample preparation is very important for successful SRP measurements.[60–61] Next the sample is positioned in the measurement apparatus with the bevel edge perpendicular to the probe stepping direction. It is very useful to provide the sample with an insulating (oxide or nitride) coating. The oxide provides a sharp corner at the bevel and also clearly defines the start of the beveled surface because the spreading resistance of the insulator is very high. Spreading resistance measurements should be made in the dark to avoid photoconductance effects and are primarily used for silicon.

A good discussion of sample preparation is given by Clarysse et al.[58] The bevel angle should be measured with a well-calibrated profilometer. In the absence of a top oxide, the measurement should be started at least 10–20 points before the bevel edge. The actual starting point can then be determined from a micrograph (dark field illumination, magnification 500×). The error on the starting point should not be larger than a few points (maximum 3). Typically, the raw resistance profile shows a transition at the starting point position. The probe imprints must be visible to be able to count them and to determine the starting point. The bevel edge must be sharp enough to reduce the uncertainty of the starting point as much as possible. Good bevel surfaces require a 0.1 or 0.05 μm, high-quality, diamond paste. The rotating glass plate, used for polishing the bevel, should have a peak-to-peak roughness of 0.13 μm. The probe separation must be below 30–40 μm. Typically, 100–150 data points are used for sub micrometer implants or epitaxial layers. For sub-100 nm structures, one should try to obtain 20–25 data points.

To understand spreading resistance, consider a metallic probe contacting a semiconductor surface as in Fig. 1.22. The current $I$ flows from the probe of diameter $2r$ into a

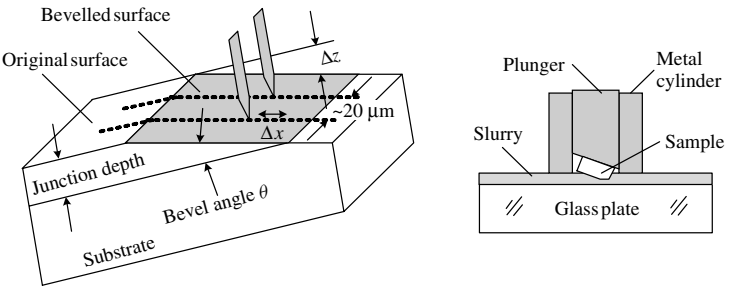



**Fig. 1.21** Spreading resistance bevel block and the beveled sample with probes and the probe path shown by the dashed line.

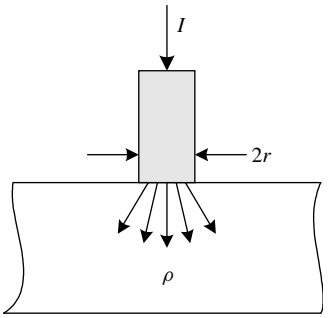



**Fig. 1.22** A cylindrical contact of diameter $2r$ to a semiconductor. The arrows represent the current flow.

semiconductor of resistivity $\rho$. The current is concentrated at the probe tip and *spreads* out radially from the tip. Hence the name *spreading resistance*. For a non-indenting, cylindrical contact with a planar, circular interface and a highly conductive probe, the spreading resistance for a semi-infinite sample is[62]

$$R_{sp} = \frac{\rho}{4r} \text{ ohms} \tag{1.42a}$$

For a hemispherical, indenting probe tip of radius $r$, the spreading resistance is

$$R_{sp} = \frac{\rho}{2\pi r} \text{ ohms} \tag{1.42b}$$

Equation (1.42a) has been verified by comparing spreading resistance with four-point probe measurements. The spreading resistance can be expressed as[63]

$$R_{meas} = R_{cont} + R_{spread} = R_{cont} + \frac{\rho}{2r}C \tag{1.43}$$

where $C$ is a correction factor that depends on sample resistivity, probe radius, current distribution and probe spacing. It should be noted that the radius $r$ is not necessarily the physical radius. The contact resistance also depends on wafer resistivity and probe pressure and on the surface state density. These surface states dominate the Schottky barrier height of the metal/semiconductor contact. The surface state density and energy distribution are expected to be different for polished and beveled surfaces. High surface state densities induce Fermi level pinning.[64] On beveled SRP $p$-type material the contact is expected to be surrounded by a depleted region while $n$-type material has an inversion layer near the surface.

A weight of approximately 5 g is applied and the probes have to be conditioned to form an area of small microcontacts, believed to be necessary to break through the thin native oxide on the bevel surface. Despite the relatively low weight very high local pressures result. Assuming a 1 μm radius, a straightforward division by the contact area leads to an estimate of the contact pressure of approximately 16 GPa.

About 80% of the potential drop due to current spreading occurs within a distance of about five times the contact radius. The probe penetration is about 10 nm for probe loads of 10 to 12 g.[65] The relationship between SRP measured resistance and Si resistivity is

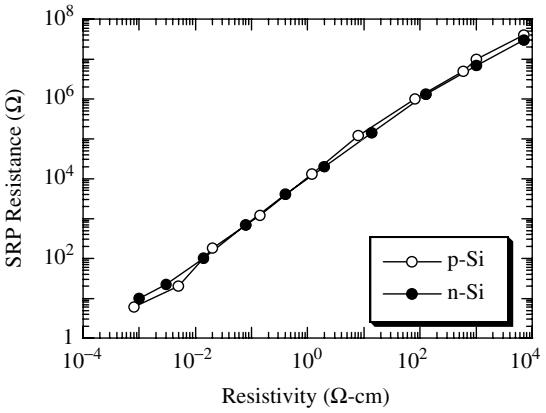



**Fig. 1.23** Calibration curves for conventional SRP measurements. After ref. 63.

shown in Fig. 1.23.[63] For a contact radius of 1 μm, Eq. (1.42a) predicts $R_{sp} \approx 2500\rho$. The fact that the spreading resistance is about $10^4$ times higher than $\rho$ is the reason that $R_{sp}$ dominates over $R_p$ and $R_c$ in Eq. (1.41). However, if the metal-semiconductor barrier height is significant, then the measured resistance does include a non-negligible contact resistance, as in GaAs, for example.

The tungsten-osmium alloy probes, are mounted in gravity-loaded probe arms. The probe tips are shaped so that they can be positioned very close together, often with less than 20 μm spacing. The probe arms are supported by a kinematic bearing system with five contacts giving the arms only one degree of freedom, which is a rotation around the horizontal axis. This virtually eliminates lateral probe motion during contact to the sample minimizing probe wear and damage to the semiconductor. The probes deform only slightly elastically upon contacting the semiconductor, thus making very reproducible contacts. The probes are "conditioned" using the "Gorey-Schneider technique"[63] for the contact area of the probe to consist of a large number of microscopic protrusions to penetrate the thin oxide layer on silicon surfaces. An example SRP plot and the resulting dopant density profile is shown in Fig. 1.24.

The conversion of spreading resistance data to a carrier density profile and subsequently to a doping density profile is a complicated task that involves data smoothing to reduce measurement noise, a deconvolution algorithm, and a correct model for the contact.[67] An important aspect of SRP is the fact that spreading resistance measures a carrier distribution along a *beveled* surface. It has often been assumed that this profile is identical to the vertical carrier profile. Furthermore, the vertical *carrier* profile is often assumed to be identical to the vertical *doping* profile. This is not true for shallow junctions where the redistribution of mobile carriers, referred to as carrier spilling, distorts the measured SR profiles. For example, electrons from the highly doped $n^+$ layer in an $n^+p$ junction spill into the lowly $p$-doped substrate. Hence, an SRP plot, that is expected to show a resistance maximum at the metallurgical junction due to the space-charge region with few carriers, may not show such a maximum at all.[67] The actual plot suggests the absence of a junction leading to the conclusion that the junction may be an $n^+n$ junction. Carrier spilling accounts for SRP determined junction depths being usually less than those measured by SIMS.[68]

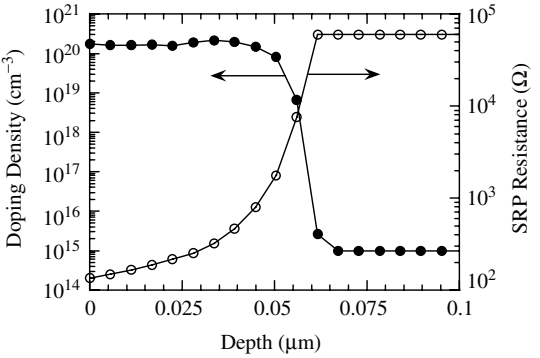



**Fig. 1.24** High-resolution spreading resistance and dopant density profiles. Data courtesy of S. Weinzierl, Solid State Measurements, Inc.

The voltage between the probes during measurement is kept at around 5 mV to reduce the effect of contact resistance. The probe-semiconductor contact is a metal-semiconductor contact with the non-linear current–voltage characteristic

$$I = I_0(e^{qV/kT} - 1) \approx I_0 qV/kT \tag{1.44}$$

for voltages less than $kT/q \approx 25$ mV.

The spreading resistance profiling technique is a comparative technique. Calibration curves are generated for a particular set of probes at a particular time using samples of known resistivity. Such calibration samples are commercially available for silicon. Comparison of the spreading resistance data to the calibration samples is necessary and sufficient for uniformly doped samples. For samples containing pn or high-low junctions, additional corrections are necessary. These multilayer corrections have evolved over the years where today very sophisticated correction schemes are used.[67–72] A different approach calculates the spreading resistance profile from an assumed doping profile.[73] The calculated profile is then compared to the measured profile and adjusted until they agree.

The bevel angle $\theta$ is typically $1^\circ$–$5^\circ$ for junction depths of 1–2 μm and $\theta \leq 0.5^\circ$ for junction depths less than 0.5 μm. The equivalent depth, $\Delta z$, for each $\Delta x$ step along the surface beveled at angle $\theta$, is

$$\Delta z = \Delta x \sin(\theta) \tag{1.45}$$

For a step of 5 μm and an angle of $1^\circ$, the equivalent step height or measurement resolution is 0.87 nm. A plot of dopant density profiles determined by differential Hall effect, spreading resistance profiling, and secondary ion mass spectrometry (SIMS) is shown in Fig. 1.20. Note the good agreement between DHE and SRP for this sample. SIMS profiling is discussed in Chapter 2. The small SRP angles are determined by measuring a small slit of light that is reflected from the beveled and the unbeveled surfaces so that two images are detected. When the slit is rotated, the two images rotate also, and the rotation angle is measured and related to the bevel angle.[74] Surface profilometers can also be used for angle determination.[61]

Limitations in SRP profiling for very shallow junctions arise due to the large sampling volume induced by the large contact and probe spacing necessitating correction

factors which can be as large as 2000. Moreover, additional correction factors have been identified to correct for carrier spilling, surface damage, microcontact distribution, and three-dimensional current flow. Unfortunately, all these corrections become increasingly important for very shallow profiles and scale with probe radius and probe separation. Probe penetration and bevel roughness also limit the depth resolution. In order to cope with the limited thickness of the layers, very shallow bevels are required.[75]

Almost all spreading resistance measurements are made with two probes, but three-probe arrangements have been used.[69] In the three-probe configuration one probe serves as the common point to both voltage and current circuits and is the only probe contributing to the measured resistance. The three-probe system is more difficult to keep aligned. Since probe alignment parallel to the bevel intersection with the top surface is crucial for depth profiling, the three-point spreading resistance probe is rarely used. *Micro spreading resistance*, known as *scanning spreading resistance microscopy* is discussed in Chapter 9.

## 1.5 CONTACTLESS METHODS

Contactless resistivity measurement techniques have become popular in line with the general trend toward other contactless semiconductor measurements. Contactless resistivity measurement methods fall into two broad categories: electrical and non-electrical measurements. Commercial equipment is available for both. Electrical contactless measurement techniques fall into several categories. (1) the sample is placed into a microwave circuit and perturbs the transmission or reflection characteristics of a waveguide or cavity[76], (2) the sample is capacitively coupled to the measuring apparatus[77], and (3) the sample is inductively coupled to the apparatus.[78–79]

### 1.5.1 Eddy Current

To be a viable commercial instrument, the apparatus should be simple with no special sample requirements. This rules out special sample configurations to fit microwave cavities, for example, and led to a variation of the inductively coupled approach. The eddy current measurement technique is based on the parallel resonant tank circuit of Fig. 1.25. The quality factor $Q$ of such a circuit is reduced when a conducting material is brought close to the coil due to the power absorbed by the conducting material. An implementation of this concept is shown in Fig. 1.25(a), where the LC circuit is replaced by dual coils on ferrite cores separated to provide a gap for the wafer that is coupled to the circuit via the high permeability ferrite cores. The oscillating magnetic field sets up eddy currents in the semiconductor leading to Joule heating of the material.

The absorbed power $P_a$ is[80]

$$P_a = K(V_T/n)^2 \int_0^t \sigma(x)\,dx \tag{1.46}$$

where $K$ is a constant involving the coupling parameters of the core, $V_T$ the rms primary rf voltage, $n$ the number of primary turns of the coil, $\sigma$ the semiconductor conductivity, and $t$ the thickness. With power given by $P_a = V_T I_T$, where $I_T$ is the in-phase drive current

$$I_T = \frac{KV_T}{n^2} \int_0^t \sigma(x)\,dx = \frac{KV_T}{n^2} \frac{1}{R_{sh}} \tag{1.47}$$

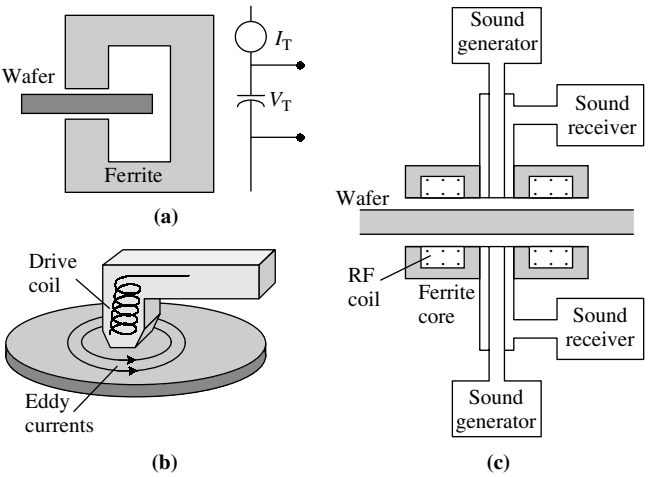



**Fig. 1.25** (a) Schematic eddy current experimental arrangement, (b) practical implementation after Johnson[81], and (c) schematic showing the eddy current coils and the thickness sound generator.

If $V_T$ is held constant through a feedback circuit, the current is proportional to the sample conductivity-thickness product, or it is inversely proportional to the sample sheet resistance. A more recent implementation is shown in Fig. 1.25(b).[81] Eddy current and other contactless techniques are discussed further in Chapter 7 in reference to lifetime measurements.

When an alternating current is induced in a conductor, the current is not uniformly distributed, but is displaced toward the surface. For high frequencies most of the current is concentrated in a layer near the surface known as the *skin depth*. Equation (1.46) is valid provided the sample is thinner than the skin depth $\delta$ given by

$$\delta = \sqrt{\rho/\pi f \mu_o} = 5.03 \times 10^3 \sqrt{\rho/f} \text{ cm} \tag{1.48}$$

where $\rho$ is the resistivity ($\Omega \cdot$ cm), $f$ the frequency (Hz), and $\mu_o$ the permeability of free space ($4\pi \times 10^{-9}$ H/cm). Equation (1.48) is plotted in Fig. 1.26 as a function of frequency. Comparison of four-point probe and eddy current wafer maps are shown in Fig. 1.27 for Al and Ti layers. Note the excellent agreement in the contours and the average sheet resistances.

To determine the wafer resistivity, its thickness must be known. In contactless measurements provision must be made to measure the wafer thickness without contact. Two methods are used: differential capacitance probe and ultrasound.[82] In the ultrasound method sound waves are reflected from the upper and lower wafer surfaces located between the two probes shown in Fig. 1.25(c). The phase shift of the reflected sound caused by the impedance variation of the air gap is detected by the sonic receiver. The phase shift is proportional to the distance from each probe to each surface. With known probe spacing, the wafer thickness can be determined.

One system to determine sample thickness by capacitance measurements is illustrated in Fig. 1.28.[83] Two capacitive probes of area $A$ are separated by a distance $s$. The semiconductor wafer is held between the two capacitance probes. Each probe forms one plate of the capacitor, the wafer the other. The capacitance is $C_1 = \varepsilon_o A/d_1$ between the upper

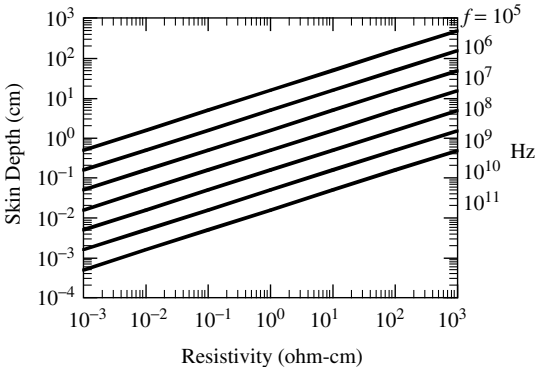



**Fig. 1.26** Skin depth versus resistivity as a function of frequency.

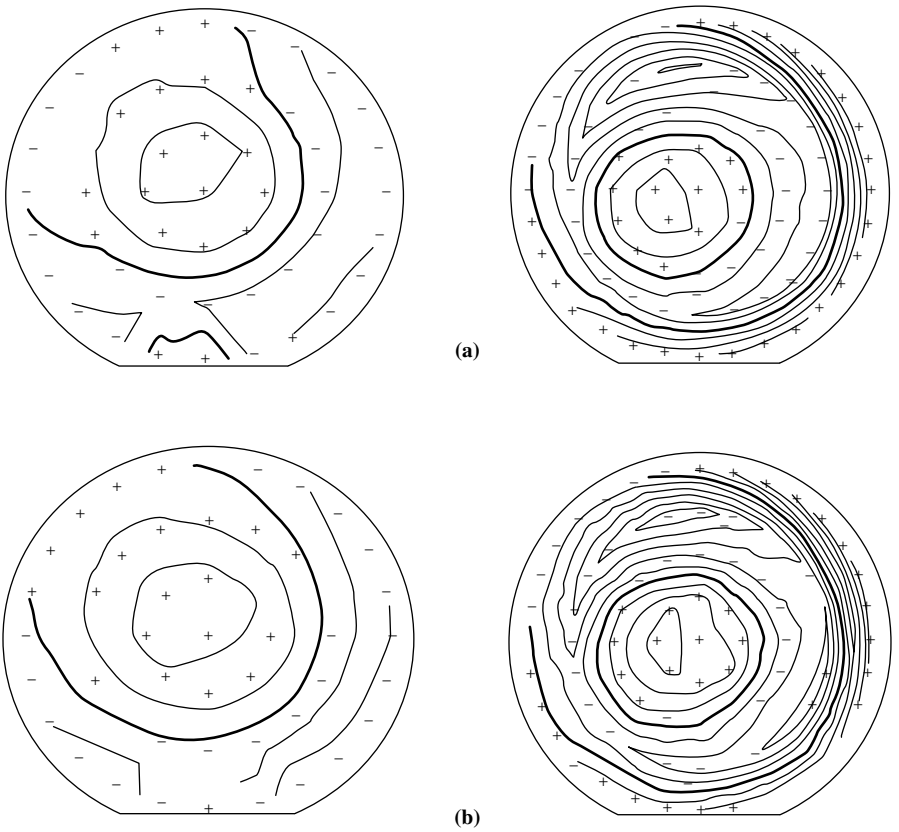



**Fig. 1.27** (a) Four-point probe and (b) eddy current contour maps. *Left*: 1 μm aluminum layer, $R_{sh,av}$(4 pt) = $3.023 \times 10^{-2}$ ohms/square, $R_{sh,av}$(eddy) = $3.023 \times 10^{-2}$ ohms/square, *right*: 20 nm titanium layer, $R_{sh,av}$(4 pt) = 62.90 ohms/square, $R_{sh,av}$(eddy) = 62.56 ohms/square. Data courtesy of W.H. Johnson, KLA-Tencor.

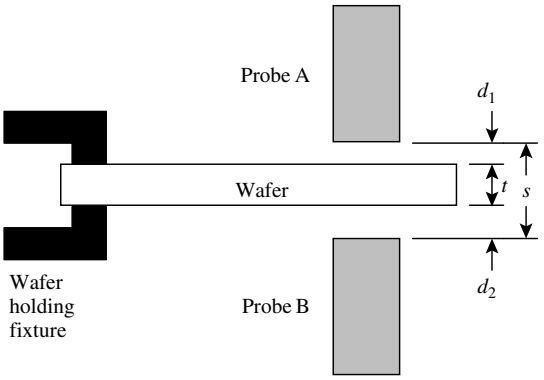



**Fig. 1.28** Capacitive wafer thickness and flatness measurement system.

probe and the wafer and $C_2 = \varepsilon_o A/d_2$ between the lower probe and the wafer. From Fig. 1.28, the thickness $t$ is

$$t = s - (d_1 + d_2) = s - \varepsilon_o A(C_1^{-1} + C_2^{-1}) \tag{1.49}$$

To determine $t$ we only need to know the probe separation $s$ and the capacitances $C_1$ and $C_2$.

The wafer thickness measurement is independent of the vertical wafer position in the gap. As the wafer moves in the vertical direction, both $d_1$ and $d_2$ change by equal and opposite amounts leaving the thickness reading unchanged. The median surface is determined by $d_1 + d_2$. By measuring the capacitance at many points on the wafer, the thickness and shape of the entire wafer can be determined. Bow and warpage, due to stress in the wafer, are determined from the median surface reading allowing the stress to be determined.[84] The flatness obtained by this capacitive technique is a function of only the wafer, not the mechanical support used in the instrument.

Resistivity measurements based on the eddy current technique are useful for uniformly-doped wafers. The technique has also found use for the measurement of highly conductive layers on less conductive substrates. The sheet resistance of the layer should be at least a hundred times lower than the sheet resistance of the substrate to measure the layer and not the substrate. This rules out measurements of diffused or ion-implanted layers on conducting substrates, which generally do not satisfy this rule. For example, sheet resistances of diffused or ion-implanted layers are typically 10 to 100 ohms/square, and the sheet resistance of a 10 ohm · cm, 650 μm thick Si wafer is 154 ohms/square. However, the sheet resistance of implanted or epitaxial layers on semi-insulating substrates (*e.g.*, GaAs) or of metal layers on semiconductor substrates can be measured. The sheet resistance of a 5000 Å Al layer is typically 0.06 to 0.1 ohms/square, making such layers 2000 times less resistive than the Si substrate. The layer *thickness* is determined from a sheet resistance measurement according to

$$t = R_{sh}/\rho \tag{1.50}$$

The layer resistivity must be determined from an independent measurement. Contactless resistance measurements are routinely used to determine sheet resistances and thicknesses of conducting layers.

Eddy current measurements require calibrated standards. Radial resistivity variations or other $\rho$ non-uniformities under the transducer are averaged and may be different from that of other $\rho$ or $R_{sh}$ measurement techniques. The measurement frequency should be such that the skin depth is at least five times the sample thickness to be measured.

## 1.6 CONDUCTIVITY TYPE

The semiconductor *conductivity type* can be determined by wafer flat location, thermal emf, rectification, optically, and Hall effect. The Hall effect is discussed in Chapter 2. The simplest method utilizes the shape of the wafer flats for those wafers following a standard pattern. Silicon wafers are usually circular. They may have characteristic flats, illustrated in Fig. 1.29, provided for alignment and identification purposes. The primary flat (usually along the $\langle 110 \rangle$ direction) and secondary flats identify the conductivity type and orientation. Wafers of diameter $\leq$150 mm usually have the standard flats of Fig. 1.29. Larger wafers usually do not have flats; instead they are provided with notches that do not provide conductivity type information.

In the *hot* or *thermoelectric probe* method the conductivity type is determined by the sign of the thermal emf or Seebeck voltage generated by a temperature gradient. Two probes contact the sample surface: one is hot the other is cold as illustrated in Fig. 1.30(a). Thermal gradients generate currents in a semiconductor; the majority carrier currents for $n$ and $p$-type materials are[85]

$$J_n = -qn\mu_n \mathcal{P}_n \, dT/dx; \; J_p = -qp\mu_p \mathcal{P}_p \, dT/dx \tag{1.51}$$

where $\mathcal{P}_n < 0$ and $\mathcal{P}_p > 0$ are the *differential thermoelectric power*.

Consider the experimental arrangement of Fig. 1.30(a). The right probe is hot, the left probe is cold. $dT/dx > 0$ and the electron current in an $n$-type sample flows from left to right. The thermoelectric power can be thought of as a current generator. Some of the

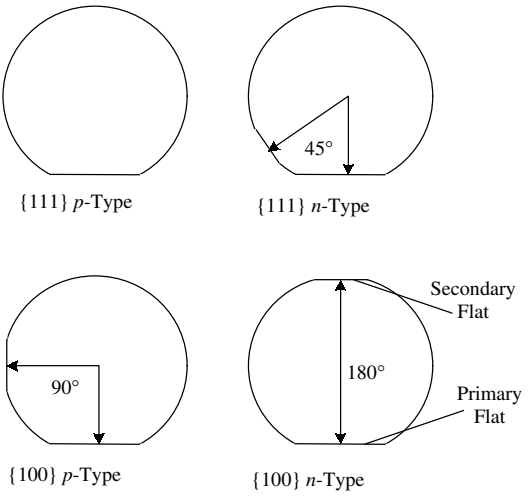



**Fig. 1.29** Identifying flats on silicon wafers.

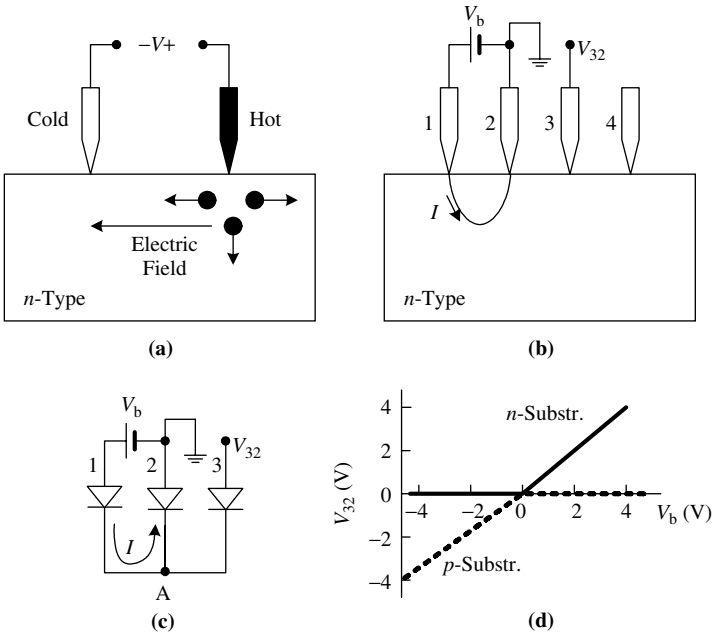



**Fig. 1.30** Conductivity type measurements. (a) Hot probe; (b) rectifying probe, (c) equivalent circuit for (b), and (d) experimental data adapted from ref. 88.

current flows through the voltmeter causing the hot probe to develop a positive potential with respect to the cold probe.[86–87] There is a simple alternative view. Electrons diffuse from the hot to the cold region setting up an electric field that opposes the diffusion. The electric field produces a potential detected by the voltmeter with the hot probe positive with respect to the cold probe. Analogous reasoning leads to the opposite potential for $p$-type samples.

Hot probes are effective over the $10^{-3}$ to $10^{3}$ ohm-cm resistivity range. The voltmeter tends to indicate $n$-type for high resistivity material even if the sample is weakly $p$-type because the method actually determines the $n\mu_n$ or the $p\mu_p$ product. With $\mu_n > \mu_p$ intrinsic or high resistivity material is measured $n$-type if $n \approx p$. In semiconductors with $n_i > n$ or $n_i > p$ at room temperature (narrow band gap semiconductors, for example), it may be necessary to cool one of the probes and let the room temperature probe be the "hot" probe.

In the *rectification* method, the sign of the conductivity is determined by the polarity of a rectified ac signal at a point contact to the semiconductor.[86–87] When two probes are used, one should be rectifying and the other should be ohmic. Current flows through a rectifying contact to $n$-type material if the metal is positive and for $p$-type if it is negative. Rectifying and ohmic contacts are difficult to implement with two-point contacts. Fortunately four-point probes can be used with appropriate connections. A dc voltage is applied and current flows between probes 1 and 2, and the resulting potential is measured between probes 3 and 2 in Fig. 1.30(b). For an $n$-substrate with positive $V_b$, the probe 1 metal-semiconductor diode is forward biased and probe 2 diode is reverse biased. Hence the current $I$ is the leakage current of the reverse-biased diode and diode 1 in Fig. 1.30(c)

has very low forward bias. The voltage at point A is

$$V_A = V_b + V_{D1} \approx V_b \tag{1.52}$$

The voltage is measured with a high-input impedance voltmeter with very low current between points A and 3. Hence, there is negligible voltage drop across diode 3 and $V_{32} \approx V_A$.

$$V_{32} \approx V_A \approx V_b \tag{1.53}$$

For $p$-substrates and the same bias arrangement as in Fig. 1.30(c) diode 1 is reverse and diode 2 forward biased. Consequently,

$$V_{32} \approx V_A \approx 0 \tag{1.54}$$

Equations (1.53) and (1.54) show how this probe arrangement can be used for semiconductor *type* determination. The voltage dependence is shown in Fig. 1.30(d). For thin semiconductor films, *e.g.*, silicon-on-insulator or polysilicon films, the metallic needle probes have been replaced with mercury probes.[88] This method of conductivity type measurement is built into some commercial four-point probe instruments.

In the *optical* method, an incident modulated laser beam creates a time-varying surface photovoltage (SPV) in the sample, detected with a non-vibrating, optically transparent Kelvin probe held up to several cm from the sample surface. The principle is the surface photovoltage method discussed in Section 7.4.5. The SPV is negative for $p$-type and positive for $n$-type semiconductors.

## 1.7 STRENGTHS AND WEAKNESSES

*Four-Point Probe:* The weakness of the four-point probe technique is the surface damage it produces and the metal it deposits on the sample. The damage is not very severe but sufficient not to make measurements on wafers to be used for device fabrication. The probe also samples a relatively large volume of the wafer, preventing high-resolution measurements. The method's strength lies in its established use and the fact that it is an absolute measurement without recourse to calibrated standards. It has been used for many years in the semiconductor industry and is well understood. With the advent of wafer mapping, the four-point probe has become a very powerful process-monitoring tool. This is where its major strength lies today.

*Differential Hall Effect:* The weakness of this method is its tediousness. The layer removal by anodic oxidation is well controlled, but it is also slow, limiting the method to relatively few data points per profile when done manually. That restriction is lifted when the technique is automated. The sheet resistance can be measured by four-point probe or Hall effect. Repeated four-point probe measurements on the same area create damage, rendering the measurements questionable. That problem does not exist for Hall samples. The method is destructive. The method's strength lies in its inexpensive equipment when using "home assembled" equipment. For those dopant profiles that cannot be profiled by capacitance-voltage measurements, only secondary ion mass spectrometry and spreading resistance methods are the alternatives. Equipment for those measurements is significantly more expensive, leaving anodic oxidation/four-point probe as a viable, inexpensive alternative.

*Spreading Resistance:* The weakness of the spreading resistance profiling technique is the necessity of a skilled operator to obtain reliable profiles. The system must be periodically calibrated against known standards, and the probes must be periodically reconditioned. It does not work well for semiconductors other than Si and Ge. The sample preparation is not trivial, and the measurement is destructive. The conversion of the measured spreading resistance data to doping density profiles depends very much on the algorithm. Several algorithms are in use, and others are being developed. The strengths of SRP lie in the ability to profile practically any combination of layers with very high resolution and no depth limitation and no doping density limitations. Very high resistivity material must be carefully measured and interpreted. The equipment is commercially available and it is used extensively. Hence there is a large background of knowledge related to this method, which has been in use over the past 40 years.

*Contactless Techniques:* The weakness of the eddy current technique is its inability to determine the sheet resistance of thin diffused or ion-implanted layers. In order to detect such sheet resistances, it is necessary for the sheet resistance of the layer to be on the order of a hundred times lower than the sheet resistance of the substrate. This is only attainable when the sheet consists of a metal on a semiconductor or a highly doped layer on an insulating substrate. The eddy current technique is often used to measure the sheet resistance of metal layers on semiconductor substrates to determine their thickness. The strength of the eddy current method lies in its non-contacting nature and the availability of commercial equipment. This is ideal for measuring the resistivity of semiconductor wafers and the layer thickness.

*Optical Techniques:* The weakness of optical techniques is that the measurements are qualitative with quantitative doping measurements requiring calibrated standards. Profiling is generally not possible, and only average values are obtained. The optical densitometry and modulated photoreflectance techniques have become commercially available methods. They are mainly used for wafer mapping of ion-implanted wafers. Their strength lies in their ability to measure the implants non-destructively, with small spot size, and rapidly and in displaying the information in the form of contour plots. The modulated photoreflectance technique is able to measure through an oxide and is routinely used for ion implantation monitoring. Disadvantages are possible laser drift and post-implant damage relaxation. Disadvantages of optical densitometry are the Al backing plate that must be affixed to the wafer rear surface before implantation and removed for optical sensing and the film's UV sensitivity. Without the backing plate the optical sensors in the ion implanter will register a loading error.

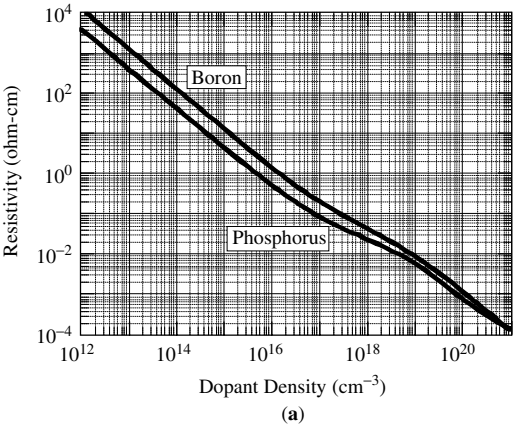
## APPENDIX 1.1

### Resistivity as a Function of Doping Density

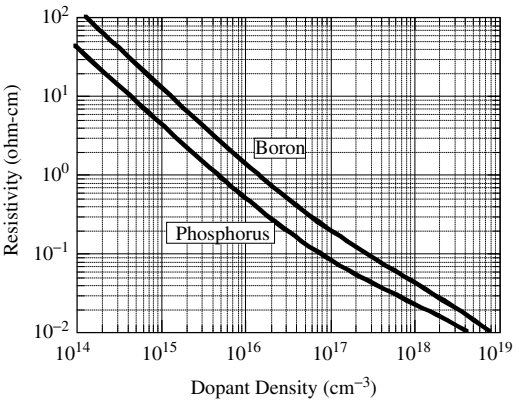
Figures A1.1(a) and (b) show the resistivity for boron- and phosphorus-doped Si. For boron-doped Si, the boron density is related to the resistivity by[89]

$$N_B = \frac{1.33 \times 10^{16}}{\rho} + \frac{1.082 \times 10^{17}}{\rho[1 + (54.56\rho)^{1.105}]} \ [\text{cm}^{-3}]$$

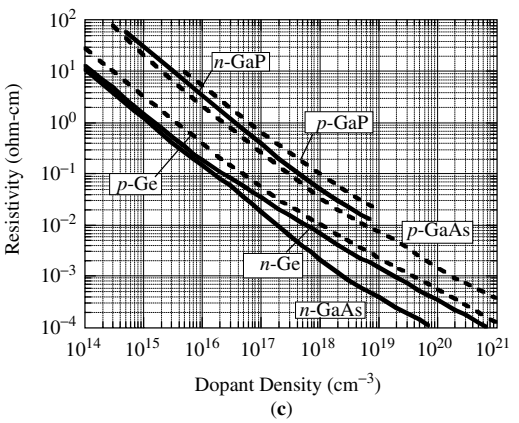
$$\rho = \frac{1.305 \times 10^{16}}{N_B} + \frac{1.133 \times 10^{17}}{N_B[1 + (2.58 \times 10^{-19} N_B)^{-0.737}]} \ [\Omega\text{-cm}] \qquad \text{(A1.1)}$$




(**a**)




(**b**)




(**c**)

**Fig. A1.1** (a) and (b) Doping density versus resistivity for *p*-type (boron-doped) and *n*-type (phosphorus-doped) silicon at 23°C. Data from ASTM F723; (c) for Ge, GaAs, and GaP. Data from Ref. 95 and 96.

For phosphorus-doped Si, the phosphorus density is related to the resistivity by[89]

$$N_P = \frac{6.242 \times 10^{18} 10^Z}{\rho} \text{ [cm}^{-3}\text{]}, \text{ where } Z = \frac{A_0 + A_1 x + A_2 x^2 + A_3 x^3}{1 + B_1 x + B_2 x^2 + B_3 x^3} \qquad \text{(A1.2a)}$$

where $x = \log_{10}(\rho)$, $A_0 = -3.1083$, $A_1 = -3.2626$, $A_2 = -1.2196$, $A_3 = -0.13923$, $B_1 = 1.0265$, $B_2 = 0.38755$, and $B_3 = 0.041833$. The resistivity is

$$\rho = \frac{6.242 \times 10^{18} 10^Z}{N_P} \text{ [}\Omega\text{-cm]}, \text{ where } Z = \frac{C_0 + C_1 y + C_2 y^2 + C_3 y^3}{1 + D_1 y + D_2 y^2 + D_3 y^3} \qquad \text{(A1.2b)}$$

and $y = \log_{10}(N_P) - 16$, $C_0 = -3.0769$, $C_1 = 2.2108$, $C_2 = -0.62272$, $C_3 = 0.057501$, $D_1 = -0.68157$, $D_2 = 0.19833$, and $D_3 = -0.018376$.

Resistivity plots for Ge, GaAs, and GaP are shown in Fig. A1.1(c).

## APPENDIX 1.2

### Intrinsic Carrier Density

The intrinsic carrier density $n_i$ for Si has been described by a number of equations over the years. The most recent and most accurate expressions are[90–91]

$$n_i = 5.29 \times 10^{19} (T/300)^{2.54} \exp(-6726/T) \qquad \text{(A2.1a)}$$

$$n_i = 2.91 \times 10^{15} T^{1.6} \exp(-E_G(T)/2kT) \qquad \text{(A2.1b)}$$

where the temperature-dependent band gap is given by[92]

$$E_G(T) = 1.17 + 1.059 \times 10^{-5} T - 6.05 \times 10^{-7} T^2 \quad (0 \le T \le 190\ K) \qquad \text{(A2.2a)}$$

$$E_G(T) = 1.1785 - 9.025 \times 10^{-5} T - 3.05 \times 10^{-7} T^2 \quad (150 \le T \le 300\ K) \qquad \text{(A2.2b)}$$

$T$ is in Kelvin. $n_i$ and $E_G$ are plotted in Figs. A2.1 and A2.2. Eq. (A2.1a) is based on experiments over the 78–340 K temperature range.[92] Equation (A2.1a) has been rewritten

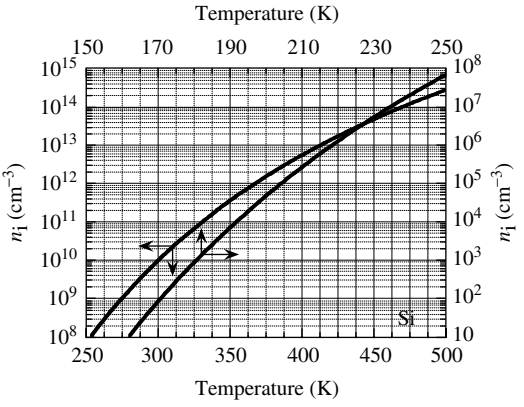



**Fig. A2.1** Silicon intrinsic carrier density versus temperature.

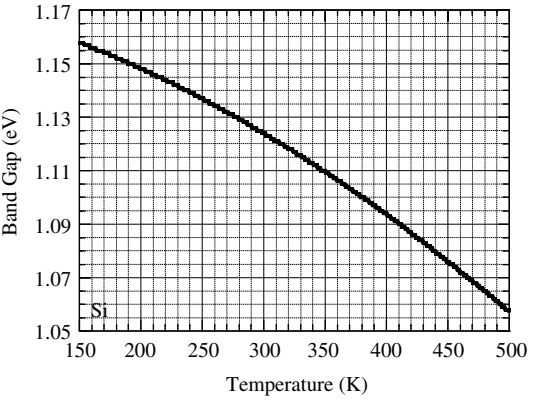



**Fig. A2.2** Silicon band gap versus temperature.

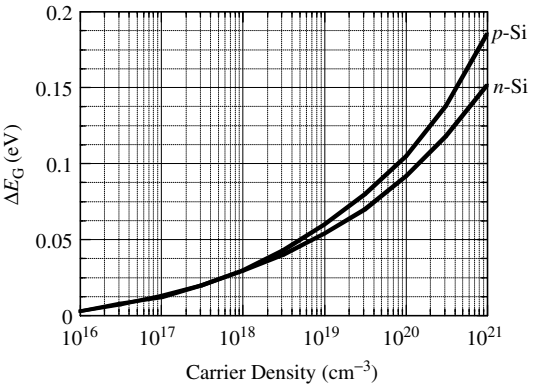



**Fig. A2.3** Silicon band gap narrowing versus carrier density.

as Eq. (A2.1b) by Trupke et al.[91] At $T = 300$ K, $n_i = 9.7 \times 10^9$ cm$^{-3}$. This is slightly lower than the earlier value by Sproul and Green[93] due to band gap narrowing. Band gap narrowing is expressed by

$$n_{i,eff} = n_i \ \exp(\Delta E_G / kT) \tag{A2.3}$$

where the band gap narrowing energy, $\Delta E_G$, is shown in Fig. A2.3.[94]

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## PROBLEMS

**1.1** The function $y = x^n$ is plotted in Fig. P1.1. Determine $n$.

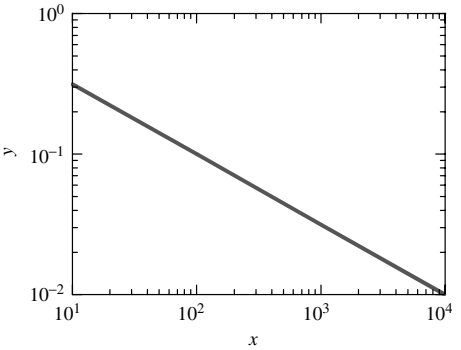



**Fig. P1.1**

**1.2** Determine $y_o$ and $x_1$ in the equation $y = y_o \exp((x/x_1) - 1)$ plotted in Fig. P1.2.

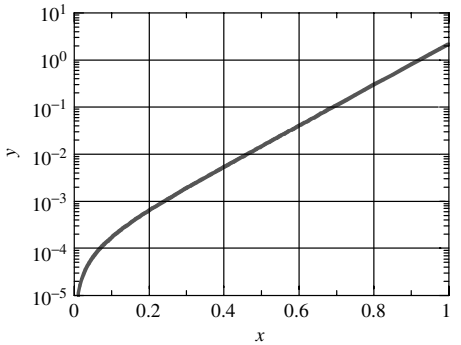



**Fig. P1.2**

**1.3** Plot the $\log(y) - x$ data of Fig. P1.3(a) on the $x - y$ figure in Fig. P1.3(b). Write numeric values on the $y$ axis of Fig. P1.3(b).

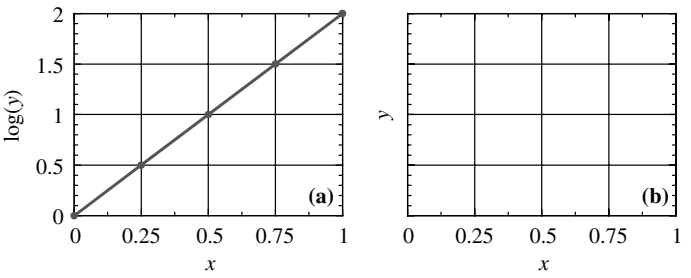



**Fig. P1.3**

**1.4** Derive an expression for the resistivity of a semiconductor sample infinite in extent laterally and vertically measured with a *square* four-point probe with the probes spaced a distance $s$ shown in Fig. P1.4. Current $I$ enters probe 1 and leaves probe 4; voltage $V$ is measured between probes 2 and 3.

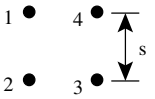



**Fig. P1.4**

**1.5** Derive an expression for the resistivity of a semiconductor sample infinite in extent laterally and vertically measured with a four-point probe with the probes spaced as shown in Fig. P1.5. Current $I$ enters probe 1 and leaves probe 4; voltage $V$ is measured between probes 2 and 3.

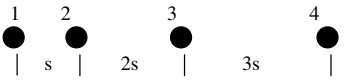



**Fig. P1.5**

**1.6** Consider an $n$-type wafer containing small $n^+$ regions. A four-point probe is placed on this wafer so that probe 1 of a conventional *in-line* four-point probe, is placed on one of those $n^+$ regions. The other three probes are on the $n$-portion of the wafer. In this four-point probe, current enters probe 1 and leaves probe 4; the voltage is measured across probes 2 and 3. There are no $n^+$ regions between probes 2 and 4. Is the correct sheet resistance measured in this case?

**1.7** The resistance of the semiconductor sample in Fig. P1.7 is measured between the two contacts as a function of wafer thickness $t$. The results are:

| $t$ (μm) | 200 | 400 | 600 | 800 | 1000 |
|---|---|---|---|---|---|
| $R$ (Ω) | 318.3 | 623.9 | 929.5 | 1235.1 | 1540.7 |

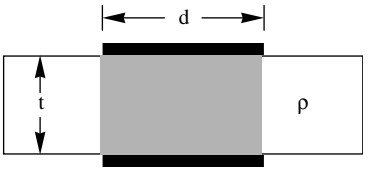



**Fig. P1.7**

Determine the resistivity $\rho$ in $\Omega \cdot$ cm and the specific contact resistance $\rho_c$ in $\Omega \cdot \text{cm}^2$ for $d = 0.01$ cm. Assume the current is confined to the area of the contact, shown by the shaded region. The contact is circular with the contact resistance given by $R_c = \rho_c / A$, where A is the contact area.

**1.8** From the $I-V$ curve in Fig. P1.8 determine the conductance $g = dI/dV$ at $I = 10^{-7}$ A.

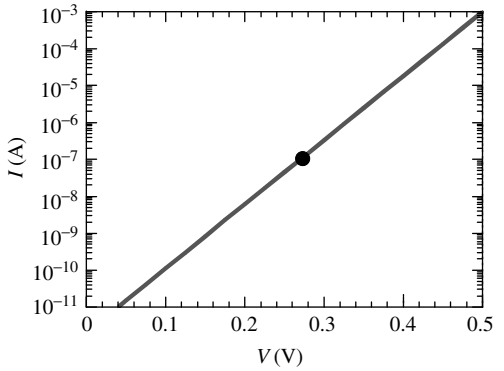
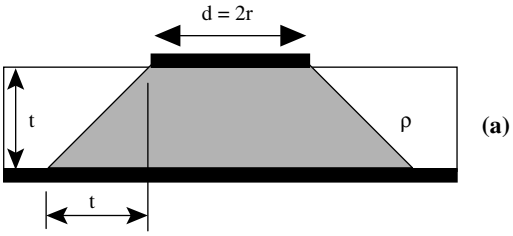
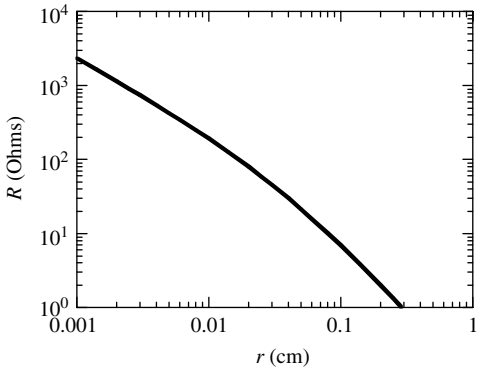



**Fig. P1.8**

**1.9** The resistance $R$ of a semiconductor sample in Fig. P1.9(a) is measured between the two contacts as a function of circular contact of radius $r = d/2$. $R$ is shown as a function of $r$ and $1/r$ in P1.9(b) and (c). Derive an expression for the resistance in terms of the resistivity $\rho$, radius $r$ and thickness $t$. Neglect contact resistance and assume the current follows the shaded region. Determine the resistivity $\rho$ (in $\Omega \cdot$ cm) for $t = 400$ μm.




**(a)**




**(b)**

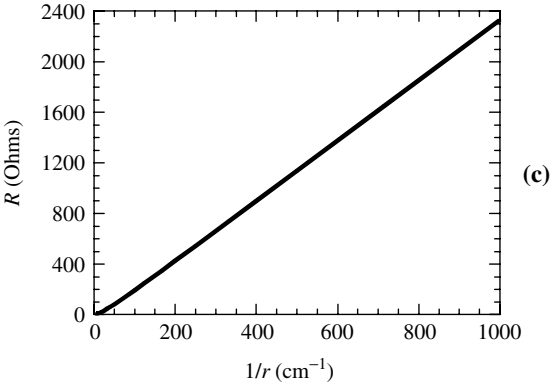



**Fig. P1.9** (*continued*)

**1.10** The conducting region in Fig. P1.10 of thickness $t = 0.1$ μm and resistivity $\rho = 0.1\ \Omega \cdot \text{cm}$, is deposited on an insulating substrate. $L = 1$ mm, $W = 100$ μm. Determine the resistance between contacts A and B.

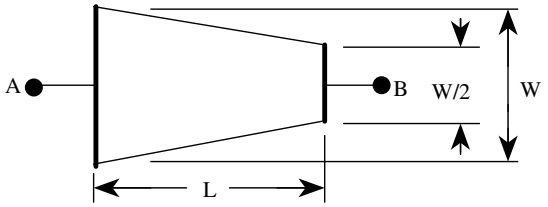



**Fig. P1.10**

**1.11** The semiconductor structure in Fig. P1.11 has thickness $t$, inside and outside radii $r_1$ and $r_2$, and resistivity $\rho$. Determine the resistance $R$ (in Ω) between the inner ring and the outer ring, *i.e.*, for the doughnut-shaped sample, for $\rho = 15\ \Omega \cdot \text{cm}$, $t = 500$ μm and $r_2/r_1 = 100$. Current flows radially as indicated by the bold arrows. *Hint*: $R = \rho L/A$ becomes $dR = \rho dr/A(r)$.

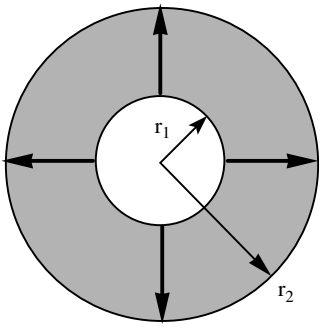



**Fig. P1.11**

**1.12** The sheet resistance is measured in an anodic oxidation experiment. The results are shown in Fig. P1.12. Determine and plot the *resistivity*, $\rho$ (in $\Omega \cdot$ cm), and the *carrier density*, $n$ (in cm$^{-3}$), versus $x$ for this sample. To determine $n(x)$, use $\mu_n = 1180$ cm$^2$/V $\cdot$ s.

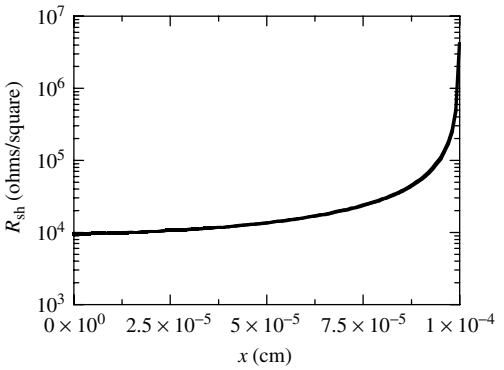



**Fig. P1.12**

**1.13** The semiconductor structure in Fig. P1.13 consists of two films of width $W = 20$ μm, lengths $L_1 = 150$ μm and $L_2 = 100$ μm, thicknesses $t_1 = 0.6$ μm and $t_2 = 0.3$ μm, and resistivities $\rho_1 = 10$ ohm-cm and $\rho_2 = 1$ ohm-cm. Determine the sheet resistance of each film (in ohms/square) and the resistance between points A and B (in ohms). The dark regions at points A (not seen) and B are ideal ohmic contacts with zero resistance. The boundary between the two films has zero resistance.

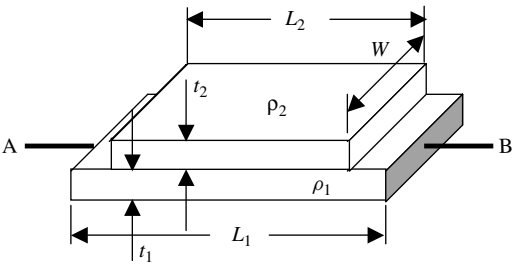



**Fig. P1.13**

**1.14** The resistivity of a semiconductor layer of thickness $t$ varies according to $\rho = \rho_o(1 - kx/t)$, where $k$ is a constant. $L$ is the sample length, $W$ is the sample width and $x$ is the dimension along the sample thickness. Derive an expression for the *sheet resistance* of this sample.

**1.15** For the $n$-type layers on a $p$-type substrate in Fig. P1.15:

**(a)** determine $R_{sh}$

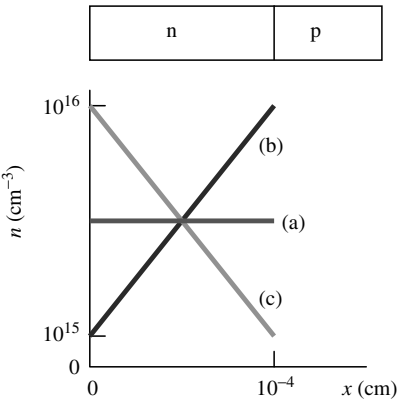



**Fig. P1.15**

**(b)** calculate and plot: $\sigma$ versus $x$ (linear-linear plot), $\rho$ versus $x$ (linear-linear plot), $R_{sh}$ versus $x$ (log-linear plot), and $1/R_{sh}$ versus $x$ (log-linear plot) for the three cases. Use $\mu_n = 1250$ cm$^2$/V $\cdot$ s.

**1.16** An arbitrarily shaped van der Pauw sample of thickness $t = 500$ μm was measured. The measured resistances were: $R_{12,34} = 74\ \Omega$ and $R_{23,41} = 6\ \Omega$. Determine the *resistivity* and *sheet resistance* of this sample.

**1.17** An arbitrarily shaped van der Pauw sample of thickness $t = 350$ μm was measured. The measured resistances were: $R_{12,34} = 59\ \Omega$ and $R_{23,41} = 11\ \Omega$. Determine the *resistivity* and *sheet resistance* of this sample.

**1.18** An arbitrarily shaped, uniformly doped van der Pauw sample has a thickness of 500 μm. The measured resistances are $R_{12,34} = 90\ \Omega$ and $R_{23,41} = 9\ \Omega$. Determine the *resistivity* and the *sheet resistance* of this sample.

**1.19** In the cross bridge test structure in Fig. 1.13, consisting of a uniformly-doped layer on an insulating substrate, the following parameters are determined: $V_{34} = 58$ mV, $I_{12} = 1$ mA, $V_{45} = 1.75$ V, $I_{26} = 0.1$ mA. An independent measurement has given the resistivity of the film as $\rho = 0.0184\ \Omega \cdot$ cm and $L = 500$ μm. Determine the film sheet resistance $R_{sh}$ (in Ω/square), the film thickness $t$ (in μm), and the line width $W$ (in μm).

**1.20** The doping profile $N_D(x)$ of an ion implanted layer is given by

$$N_D(x) = \frac{\phi}{\Delta R_p \sqrt{2\pi}} \exp\left[-0.5\left(\frac{x - R_p}{\Delta R_p}\right)^2\right],$$

where $\phi$ is the implant dose, $R_p$ is the range, and $\Delta R_p$ the straggle. Determine the sheet resistance for an arsenic layer implanted ($E = 100$ keV) into $p$-type Si doped to $N_A = 10^{15}$ cm$^{-3}$. Use $\phi = 10^{15}$ cm$^{-2}$, $R_p = 577$ Å, $\Delta R_p = 204$ Å, and $\mu_n = 100$ cm$^2$/V $\cdot$ s. Assume $N_D(x) = n(x)$.

*Hint*: First you have to find the junction depth.

**1.21** The doping profile $N_D(x)$ of an ion-implanted layer is given by

$$N_D(x) = \frac{\phi}{\Delta R_p \sqrt{2\pi}} \exp\left[-0.5\left(\frac{x - R_p}{\Delta R_p}\right)^2\right],$$

where $\phi$ is the implant dose, $R_p$ the range, and $\Delta R_p$ the straggle. Determine the sheet resistance for an $n$-type dopant layer (arsenic) implanted at an energy of 60 keV into a $p$-type Si wafer doped to $N_A = 10^{16}$ cm$^{-3}$. Use $\phi = 5 \times 10^{15}$ cm$^{-2}$, $R_p = 368$ Å, $\Delta R_p = 133$ Å, and $\mu_n = 50$ cm$^2$/V · s. Assume $N_D(x) = n(x)$.

*Hint*: At the junction depth $x_j$: $N_A = N_D$.

**1.22** **(a)** In a cross bridge test structure in Fig. 1.13 of a semiconductor layer on an insulating substrate, the following parameters are determined: $V_{34} = 18$ mV, $I_{12} = 1$ mA, $V_{45} = 1.6$ V, $I_{26} = 1$ mA. An independent measurement has given the resistivity of the film as $\rho = 4 \times 10^{-3}$ Ω · cm and $L = 1$ mm. Determine the film sheet resistance $R_{sh}$ (Ω/square), the film thickness $t$ (μm), and the line width $W$ (μm).

**(b)** In one particular cross bridge test structure, the leg between contacts $V_4$ and $V_5$ is overetched. For this particular structure $V_{45} = 3.02$ V for $I_{26} = 1$ mA; it is known that half of the length $L$ has a reduced $W$, *i.e.*, $W'$, due to a fault during pattern etching. Determine the width $W'$.

**1.23** In a cross bridge test structure in Fig. 1.13 consisting of a uniformly-doped layer on an insulating substrate, measurements give: $V_{34} = 58$ mV, $I_{12} = 1$ mA, $V_{45} = 1.75$ V, $I_{26} = 0.1$ mA. An independent measurement has given $\rho = 1.84 \times 10^{-2}$ Ω · cm and $L = 500$ μm.

**(a)** Determine the film sheet resistance $R_{sh}$ (in Ω/square), the film thickness $t$ (in μm), and the line width $W$ (in μm).
It is usually assumed that the sheet resistance $R_{sh}$, measured in region A in Fig. P1.23, is the same in the entire structure. Suppose that is not the case. What effect will that have on the line width measurement?

**(b)** Determine the widths $W$(a) and $W$(b) in Fig. P1.23 that are calculated if the sheet resistance in the cross hatched region is $R_{sh1}$ and in the white region it is $R_{sh}$ (as determined in (i)), where $R_{sh} = 0.5R_{sh1}$, but you assumed it was $R_{sh}$ everywhere. Give your answer as $W$(a)/$W$ and $W$(b)/$W$, where $W$ is the width for uniform sheet resistance.

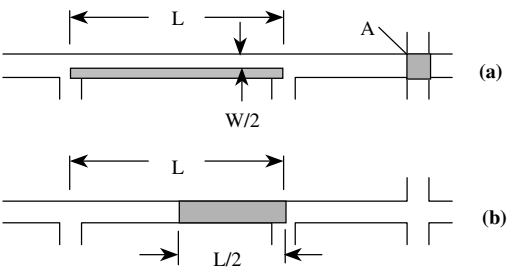



**Fig. P1.23**

**1.24** Consider a $p$-type semiconductor cross bridge test structure on an insulating substrate. The layer, of thickness $t$, is non-uniformly doped according to $N_A = 10^{19}\exp(-kx)$, where $k$ is a constant and $x$ is the dimension along the sample thickness. Determine $R_{sh}$, $V_{34}$ and $V_{45}$. Use $I_{12} = I_{26} = 1$ mA, $\mu_p = 100$ cm$^2$/V $\cdot$ s, $t = 1$ μm, $k = 10^5$ cm$^{-1}$, $L = 500$ μm, and $W = 10$ μm. Neglect the electron contribution to the layer resistivity and assume $N_A = p$.

**1.25** **(a)** In the cross bridge test structure in Fig. P1.25, consisting of a uniformly doped layer on an insulating substrate, measurements give: $V_{34} = 11$ mV, $I_{12} = 0.5$ mA, $V_{45} = 50$ mV, $I_{26} = 1$ μA. The resistivity of the film is $\rho = 5 \times 10^{-3}$ Ω $\cdot$ cm and $L = 100$ μm. Determine the film *sheet resistance* $R_{sh}$ (in Ω/square), the film *thickness* $t$ (in μm), and the *line width* $W$ (in μm).

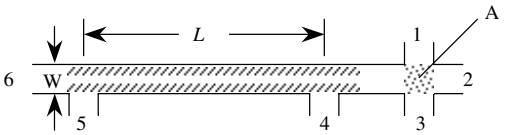



**Fig. P1.25**

**(b)** It is usually assumed that the resistivity in the "$L$" region is uniform. Suppose that is not the case. Determine the *effective line width* $W_{eff}$ if the resistivity in the shaded "$L$" region varies linearly from $5 \times 10^{-3}$ Ω $\cdot$ cm at terminal 5 to $10^{-2}$ Ω $\cdot$ cm at terminal 4. The resistivity in region "A", $I_{12}$, $I_{26}$ and the physical width $W$ are the same as in (a).

**1.26** A sample with doped regions as shown in Fig. P1.26 is characterized by a spreading resistance probe. The minimum lateral step (along the beveled direction) that the probe can be moved is 2 μm. Determine the maximum bevel angle $\theta$ (in degrees) to ensure a minimum of 20 measurement points per doped region?

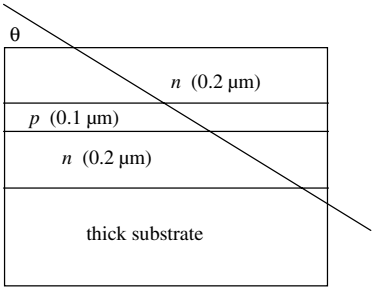



**Fig. P1.26**

**1.27** Draw the spreading resistance plots, $R_{sp}$ versus depth, for a $p^+n$ and an $n^+n$ junction on the same plot. The $n$-substrates are the same and the resistivity of the $n^+$ region is the same that of the $p^+$ region. These are *qualitative curves*, without numerical values.

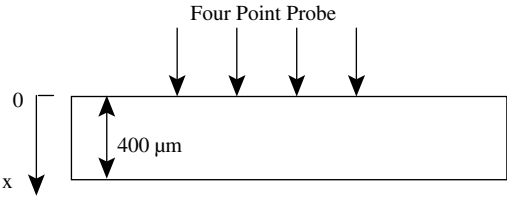



**Fig. P1.28**

**1.28** Determine the sheet resistance $R_{sh}$ for a Si wafer of thickness $t = 400$ μm, shown in Fig. P1.28, for:

**(a)** $N_A(x) = N_A(0)\exp(-x/L)$; $N_D = 0$, *i.e.*, no donors.

**(b)** $N_A(x) = N_A(0)\exp(-x/L)$; $N_D = 10^{16}$ cm$^{-3}$, *i.e.*, uniformly doped with donors.

*Use* $p(x) - n(x) - N_A(x) + N_D(x) = 0$, $p(x)n(x) = n_i^2$, $n_i = 10^{10}$ cm$^{-3}$, $N_A(0) = 10^{17}$ cm$^{-3}$, $L = 5$ μm,

$$\mu_p(x) = 54.3 + \frac{406.9}{1 + \left(\dfrac{N_A(x) + N_D}{2.35 \times 10^{17}}\right)^{0.88}}; \mu_n(x) = 92 + \frac{1268}{1 + \left(\dfrac{N_A(x) + N_D}{1.3 \times 10^{17}}\right)^{0.91}}.$$

The sheet resistance is measured on the top surface. Assume the pn junction in (b) is an insulating boundary. Neglect the width of the pn junction space-charge region. Assume that the four-point probe spacing $s$ is much larger than the wafer thickness $t$.

**1.29** Consider the sample in Fig. P1.29(a). Give a value for the sheet resistance $R_{sh}$. To convert from $N_A$ to $\rho$, use Fig. A1.1. Then positive charge of density $10^{12}$ cm$^{-2}$ is deposited on the upper surface, as in (b), and the charge remains there. This charge sheet does not change the measurement condition, *i.e.*, no surface current flows, but it does change the sample configuration, by causing the $p$-layer to be partially depleted and this depleted region can be considered an insulating region. Give a value for the new sheet resistance $R_{sh}$.

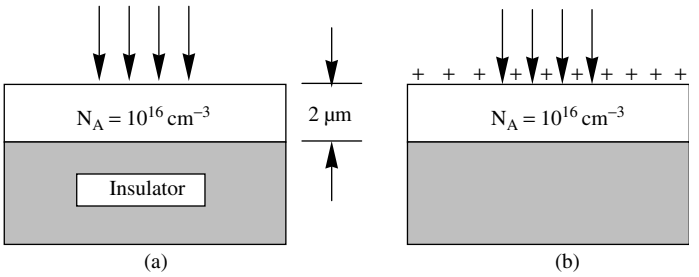



**Fig. P1.29**

**1.30** The hot probe is used to determine the semiconductor *type*, *i.e.* $n$-type or $p$-type. For the arrangement in Fig. P1.30, determine the conductivity type and draw the band diagram. The sample is uniformly doped and in the dark, *i.e.*, it is not illuminated.

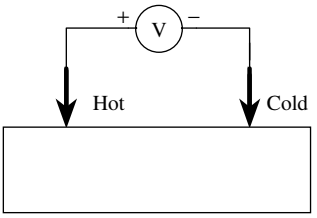



**Fig. P1.30**

*Hint:* The electron current density is $J_n = n\mu_n \, dE_F/dx - qn\mu_n P_n \, dT/dx$, where $P_n < 0$ is the differential thermoelectric power.

## REVIEW QUESTIONS

- What is the best way to plot power law data?
- What is the best way to plot exponential data?
- Why is a four-point probe better than a two-point probe?
- Why is resistivity inversely proportional to doping density?
- What is an important application of wafer mapping?
- What is sheet resistance and why does it have such strange units?
- Why is sheet resistance commonly used to describe thin films?
- What are *van der Pauw* measurements?
- What is the main advantage of *Eddy current* measurements?
- What are advantages and disadvantages of the *modulated photoreflectance* (therma wave) technique?
- What is *carrier illumination* and what material parameters does it provide?
- How is *spreading resistance* profiling implemented?
- How can *conductivity type* be determined?