

Filed on behalf of Institute of Microelectronics, Chinese Academy of Sciences
By: David C. Radulescu, Ph.D., Reg. No. 36,250

RADULESCU LLP

Empire State Building
350 Fifth Avenue, Suite 6910
New York, NY 10118
Tel: 646-502-5950
david@radip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

INSTITUTE OF MICROELECTRONICS, CHINESE ACADEMY OF
SCIENCES,
Patent Owner.

Inter Partes Review No. 2018-01574
U.S. Patent No. 9,070,719B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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I. INTRODUCTION

Patent Owner Institute of Microelectronics, Chinese Academy of Sciences (“IMECAS” or “Patent Owner”) submits this Preliminary Response to the Petition for *Inter Partes* Review (the “Petition”) filed by Intel Corporation (“Petitioner”) regarding U.S. Patent No. 9,070,719 (the “’719 Patent”). IMECAS respectfully requests that the Board deny the Petition for at least the following reasons.

First, a petition for *inter partes* review must identify how the challenged claims are to be construed and how they read on the prior art under the proper construction. The Petition here fails to do either. Petitioner takes no claim construction position on any claim term, but alleges that the prior art falls within the scope of the challenged claims under some unstated claim construction. The failure to construe the challenged claims should result in a denial of the Petition outright.

Second, the Petition fails to show a reasonable likelihood of prevailing on any ground, because every ground suffers from a failure of proof for certain limitations. Notably, the Petition fails to analyze how any cited prior art discloses two claim terms—“inter-device” and “of respective devices”—in what Petitioner alleges to be the “key” claim limitation. Indeed, aside from section headings, the only place in the Petition that mentions these claim terms is the section introducing the ’719 Patent. Petitioner does not allege that these terms are not limiting or offer

any justification for ignoring them from the claim language. Petitioner's failure to analyze or even acknowledge these terms dooms all grounds of the Petition.

Third, despite Petitioner's claims to the contrary, the prior art references fail to disclose performing inter-device electrical isolation *after* forming dielectric spacers, which is alleged to be the "point of novelty" of the '719 Patent by Petitioner. Petitioner misinterprets and mischaracterizes the cited prior art, which in fact discloses the conventional process that caused the very problems that the '719 Patent aimed to solve.

Fourth, Petitioner's motivation to combine arguments rely on unsupported and conclusory assertions of its expert that are driven by hindsight, rather than relying on specific disclosures in the prior art references. Essentially, Petitioner proposes that any two references in the field of SRAM technology can be combined in an obviousness analysis. In particular, Petitioner erroneously asserts that techniques used in older "planar" semiconductor manufacturing technology could be lifted and inserted into next-generation FinFET technology. The Petition fails to address fundamental incompatibilities between the planar references and the FinFET references in its proposed combinations and does not explain how predictable and reliable results of the proposed combination can be achieved.

Due to these glaring deficiencies in the Petition and the supporting declaration, Petitioner cannot meet its burden of showing unpatentability, and institution should be denied.

II. THE '719 PATENT

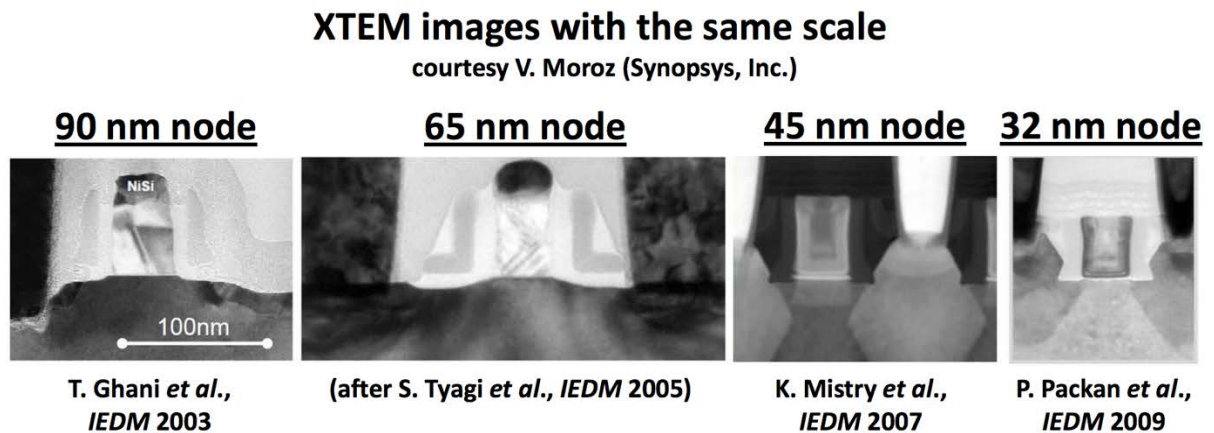
A. Technology Background

A Field Effect Transistor (“FET”) is a transistor that uses an electric field to control the electrical conductivity through a channel formed between a “source” and a “drain.” A FET “gate” opens and closes the channel by either permitting or blocking the flow of charge carriers (e.g., electrons or holes) between the source and the drain. For decades, scientists have strived to reduce the size of transistors in accordance with Moore’s Law—a projection that the number of transistors in an integrated circuit doubles about every 18 months. Ex. 2002 at 1.

With each generation after the 130nm node¹ (e.g., 90 nm, 65 nm, 45 nm, 32 nm), different challenges appeared and different solutions were sought, and, as a result, each generation had substantially different designs. *See* Ex. 1037 at 2197

¹ A “node” is a reference to a particular generation of semiconductor manufacturing process and is specified by a size—e.g., 130 nm—that at one time referred to the length of a gate in that particular generation of technology, but has since lost that meaning.

(“The 90-nm SRAM cell was a ‘tall’ architecture with significant diffusion corner rounding. The 65-nm cell added the ‘wide’ cell to eliminate diffusion corners, the 45-nm cell added double patterning to eliminate poly rounding, and the 32- and 22-nm cells refined the basic ‘wide’ design with patterning and polish improvements.”). The following figure illustrates the evolution of device structure with each generation.



Ex. 2003 at 6 (sources for figures: Ex. 2004 at 11.6.2; Ex. 2005 at 2; Ex. 1021 at 248; Ex. 2006 at 28.4.2).

As the technology advanced to 22nm node, performance of the two-dimensional/planar transistor was severely affected by short-channel effects, which refer to large current leakage between the source and drain when carrier flow should have been turned off. Ex. 2007 at 21. In 1998, a research team led by professors at the University of California, Berkeley introduced double-gate three-dimensional/non-planar FETs, later known as “FinFETs” (fin field-effect

transistors), to improve short-channel effects immunities. Ex. 2008 at 15.7.1; Ex. 2009 at 880. A FinFET structure has a three-dimensional fin instead of a planar active region, thereby allowing current flow to be controlled from not only the top surface but also the side surfaces of the fin. The FinFet structure is generally considered to have superior electrostatics than two-dimensional/planar devices. Ex. 2010 at 12.1.1. However, the transition from planar to FinFET technology involves more than simply replacing planar active regions with three-dimensional fins in existing two-dimensional designs; additional steps must be taken to address challenges specific to FinFET manufacturing. *Id.* at 12.1.1 (“For instance, *it is not easy to build by a conventional process narrow fins* with good fin width (D_{fin}) uniformity. Conformality of thin film deposition or ion implantation (I/I) along the fin height is also *a stringent requirement*. In spacer formation, *unlike for a planar FET*, significant over-etching is necessary to remove spacer material from the fins.”) (emphasis added), Figs. 5-6 (shown below), 12.1.2 (“*New doping techniques* such as plasma doping or solid-phase doping *will be necessary* to realize conformal doping into the FinFET.”) (emphasis added); Ex. 2011 at 1:28-39 (“[T]he introduction of *non-planar transistors* has introduced its own *particular problems*, such as, for example, corner effects, the difficulty of fabricating fins with high aspect ratios, floating body effects related to a fin built on an SOI substrate, and self-heating for non-planar transistors built on an SOI

substrate, *to name just a few*. In addition to the above-mentioned problems sometimes associated with non-planar transistors, one particular issue concerns fringe effects associated with unwanted capacitance between the gate electrode and the fin in a non-planar transistor built on a bulk silicon substrate.”) (emphasis added).

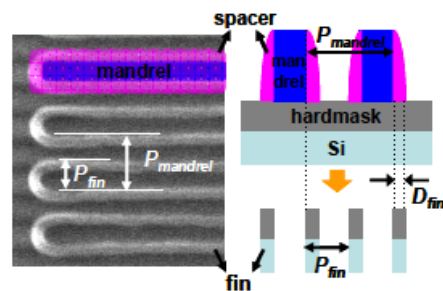


Fig. 5: The schematic of the SIT process. First, spacers are formed around mandrels. After mandrels are removed, Si is etched using spacers as a mask and then, fins are formed. The spacer width defines D_{fin} . P_{fin} is a half of $P_{mandrel}$ because two fins are formed per one mandrel. Thus D_{fin} and P_{fin} can exceed lithographic limitation. Unnecessary fins or parts of a fin can be removed by adding fin cutting processes (Fig. 19).

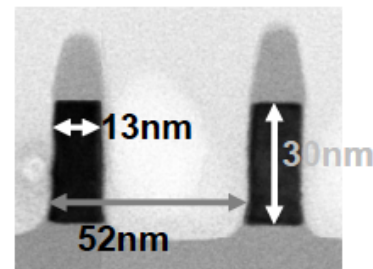


Fig. 6: Fins formed by the SIT process. Design rules used here are equivalent to 32 nm node. In this work, the surface orientation of the channel on the fin is (110) and current direction is $\langle 110 \rangle$.

Accordingly, since the first FinFETs were introduced, researchers proposed numerous changes in both the design and manufacturing process to overcome various manufacturing difficulties and to improve the performance of FinFETs. Such changes included reduced fin width to suppress drain-induced barrier lowering (DIBL), the use of spacer lithography to control critical dimension (CD) and achieve uniformity in fin width, the use of bulk semiconductor substrate to lower production cost and improve thermal conduction, the smoothening of fin

sidewalls to improve carrier mobilities, and the integration of metal gate and high-k gate dielectric to reduce equivalent gate-oxide thickness (EOT). *See, e.g.*, Ex. 2012 at 489; Ex. 2014, Fig. 2; Ex. 2013 at 10.4.3; Ex. 2015 at 27.5.2. By 2002, FinFETs with gate length down to 10 nm were achieved. Ex. 2016. Nearly ten years later, Petitioner Intel Corporation announced that it would bring relatively large (22 nm) FinFETs into commercial production, despite having had decades of experience in the manufacture of planar transistors. Ex. 1033.

Patent Owner IMECAS is a premier research institution in China that has been at the forefront of FinFET research since 2001 and has contributed to many of the necessary advances in FinFET technology. *See, e.g.*, Exs. 2017, 2018. In particular, the Integrated Circuit Advanced Process Center at IMECAS focuses on developing FinFET devices of 10 nm nodes and beyond. IMECAS' FinFET research is frequently published and cited in peer reviewed journals, and its intellectual property has been recognized as the highest quality FinFET patent portfolio in the world, surpassing a long list of the entrenched semiconductor giants including IBM, Intel, Samsung, Micron, AMD and Global Foundries. Ex. 2019 at 17 (graphically illustrating IMECAS as having the highest "Portfolio Quality Score").

B. The Claimed Invention of the '719 Patent

At the time of the invention of the '719 Patent, the conventional process for

making FinFET devices was often susceptible to defects as their size was reduced. The inventors of the '719 Patent discovered that one major cause of defects related to the dielectric spacer between the gate electrodes. Specifically, under the conventional process, a gate line was cut into several gate electrodes with very small breaks in between, and spacer material was then deposited onto each gate electrode to form gate spacers. The inventors of the '719 Patent discovered that, because the devices were so densely packed and the breaks between adjacent electrodes were so small, dielectric material that enters these breaks could cause voids, which would result in shorts in the devices and cause complications in subsequent processes. Ex. 1001 at 5:10-28.

To solve this problem, the inventors of the '719 Patent came up with a novel way to prevent spacer material from entering into the spaces between gate electrodes—by depositing spacer material onto the gate line before cutting the gate line into independent gate electrodes. Ex. 1001 at 7:38-67. This way, the spaces between adjacent gate electrodes would not impact the profile of the dielectric spacer, and voids may be avoided. *Id.* Accordingly, this invention allowed smaller devices to be made with reduced shorting defects.

The '719 Patent issued with two independent claims, claims 1 and 8, with only claim 1 being at issue in the Petition. Claim 1 is copied below for the convenience of the Board:

1. A method for manufacturing a semiconductor device structure,
comprising:
 - 1[a]** forming a fin in a first direction on a semiconductor substrate;
 - 1[b]** forming a gate line in a second direction, the second direction crossing
the first direction on the semiconductor substrate, and the gate line
intersecting the fin with a gate dielectric layer sandwiched between the
gate line and the fin;
 - 1[c]** forming a dielectric spacer surrounding the gate line; and
 - 1[d]** performing inter-device electrical isolation at a predetermined position
after forming the dielectric spacer, wherein isolated portions of the gate
line form independent gate electrodes of respective devices.

III. CLAIM CONSTRUCTION

For *inter partes* review petitions filed before November 13, 2018,
challenged claims in an unexpired patent are given the broadest reasonable
interpretation in light of the specification of the patent in which they appear. 37
C.F.R. § 42.100(b) (2016) (amended 2018); *Cuozzo Speed Techs., LLC v. Lee*, 136
S. Ct. 2131 (2016).

A. “a dielectric spacer surrounding the gate line”

The broadest reasonable interpretation of “a dielectric spacer surrounding
the gate line” is “a dielectric spacer enclosing the gate line on all side surfaces.”

This construction is supported by the plain language of the claims and by the specification of the '719 Patent. The word “surround” means “to enclose on all sides.” Ex. 2020 at 1258. The specification is explicit that the dielectric spacer encloses the gate line on all side surfaces, including the ends. Ex. 1001 at 5:3-10 (“In FIG. 8, for sake of simplification, no spacer is shown at the uppermost and lowermost sides. However, it should be noted that there are also spacers 207 formed at the positions if some gate electrodes 204 terminate at those positions”), 6:18-21 (“the dielectric spacer layer 1005 is formed on opposite lateral outer sides of the respective gate lines 1004 in the horizontal direction of the figure, *besides those formed at the ends of the gate lines 1004 in the vertical direction of the gate line.*”) (emphasis added).

Accordingly, the broadest reasonable interpretation of “forming a dielectric spacer surrounding the gate line” is “forming a dielectric spacer enclosing the gate line on all side surfaces.”

B. Reservation of Rights

Because there are sufficient reasons to deny institution, as explained herein, the Board need not address the construction of any other claim term at this time. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795 (Fed. Cir. 1999) (“only those terms need be construed that are in controversy, and only to the extent

necessary to resolve the controversy.”). IMECAS reserves the right to present further arguments on claim construction if necessary.

IV. THE BOARD SHOULD DENY INSTITUTION BECAUSE THE PETITION IS DEFICIENT ON ITS FACE

A. Petitioner Fails to Offer Any Construction of Claim Terms

No *inter partes* review can be instituted here because Petitioner fails to construe critical claim terms and fails to demonstrate how the challenged claims read on the prior art under the proper construction.

A petition for *inter partes* review must identify “[h]ow the challenged claim is to be construed” as well as “how the *construed* claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4) (emphasis added); *Jiawei Tech. v. Richmond*, IPR2014-00937, Paper 22 at 8 (P.T.A.B. Dec. 16, 2014) (“It is Petitioner’s burden to explain how the challenged claims are to be construed and how they read on the prior art.”). At a minimum, Petitioner must state whether the claim terms are to be construed as having their plain and ordinary meaning under the broadest reasonable interpretation standard. *SharkNinja Operating LLC v. Flexible Techs., Inc.*, IPR2018-00903, Paper 8 at 8-9 (P.T.A.B. Oct. 17, 2018) (citing Office Trial Practice Guide, 77 Fed. Reg. 48,756, 48,764 (Aug. 14, 2012)). Where a party believes that a specific claim term has meaning other than its plain meaning, the party must identify “a proposed construction of the particular term and where the disclosure supports that meaning.” *Id.*

Nowhere in the Petition does Petitioner take any position regarding the construction of any claim term in the '719 Patent. Specifically, Petitioner does not recite any claim construction standard or state whether the claim terms should be accorded their plain meaning. Nor does Petitioner provide any proposed construction of any term, let alone an explanation of how the specification supports any proposed construction. Therefore, the Petition fails to meet the requirements of 37 C.F.R. § 42.104(b)(3). As result of its failure to construe any challenged claim, Petitioner also fails to meet the requirements of 37 C.F.R. § 42.104(b)(4), under which "Petitioner must explain how to apply the art to the *construed* claim in a meaningful way." *SharkNinja*, Paper 8 at 8-9 (emphasis added). The Petition ought to be denied on the basis of these failures. *Id.* at 23.

B. The Petition Fails to Establish a Likelihood of Prevailing on Any Ground

The Board should deny institution because Petitioner fails to meet its burden to show a reasonable likelihood of prevailing on any ground due to a number of glaring deficiencies in the Petition and its supporting declaration. Notably, Petitioner fails to show that any prior art discloses limitations 1[c] and 1[d], which are required by every challenged claim. Further, Petitioner's motivation to combine arguments are driven by impermissible hindsight, rather than specific disclosures in the prior art references.

1. Ground 1 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Liaw Anticipates Claims 1-2 and 6

Petitioner asserts in Ground 1 that Liaw, which fails to disclose limitations 1[c] (“forming a dielectric spacer surrounding the gate line”) and 1[d] (“performing inter-device electrical isolation at a predetermined position after forming the dielectric spacer, wherein isolated portions of the gate line form independent gate electrodes of respective devices”), can somehow anticipate claim 1 and its dependent claims. The Petition not only fails to address or analyze particular claim terms, but also mischaracterizes Liaw’s teachings. Despite Petitioner’s misreading of Liaw, the reference teaches nothing more than the conventional process that would result in the very problems the ’719 Patent sought to solve.

i Liaw Fails to Disclose Limitation 1[c] (“forming a dielectric spacer surrounding the gate line”)

Liaw fails to disclose that the permanent spacers—which Petitioner alleges are the “dielectric spacer”—surround the gate line on all side surfaces, including the ends, as required by limitation 1[c]. Liaw only states that “[t]he permanent spacers may be formed on opposing sides of the gate electrode 309” (Ex. 1003 at 7:27-29), but does not teach or show in any figure that the permanent spacers are formed on the ends of the gate line. As such, Liaw does not disclose that

permanent spacers are formed on *all* sides of gate electrode 309, and fails to meet the “surround” requirement of claim limitation 1[c].

Nowhere does Liaw disclose that the permanent spacers are formed on the ends of the gate line. Petitioner’s heavy reliance on Liaw’s disclosed process for making the permanent spacers in attempt to meet the “surround” requirement of limitation 1[c] is misplaced. Pet. at 33. Liaw teaches that the permanent spacers are formed by “blanket depositing a spacer layer [] on the previously formed structure,” which “are then patterned, such as by anisotropically etching to remove the spacer layer from the horizontal surfaces of the structure.” *Id.* (citing Ex. 1003 at 7:29-38). Petitioner argues that this disclosure *necessarily* teaches that dielectric spacer is formed on *all* side surfaces of the gate line, including the ends. Pet. at 33; Ex. 1002 ¶ 223. But this is demonstrably false according to Liaw itself.

Liaw discloses forming another set of spacers—first spacers 211—using the exact same manufacturing process, which are explicitly shown as not covering the ends of the structure on which the spacer material is deposited. Ex. 1003, Fig. 2C (annotated and shown below), 3:61-4:6 (“The first spacers 211 may be formed by blanket depositing a spacer layer (illustrated in Figs. 2B and 2C by the dashed line 210) over the previously formed structure. ... The first spacers 211 are then patterned, such as by anisotropically etching and removing the spacer layer 210 from the horizontal surfaces of the structure.”).

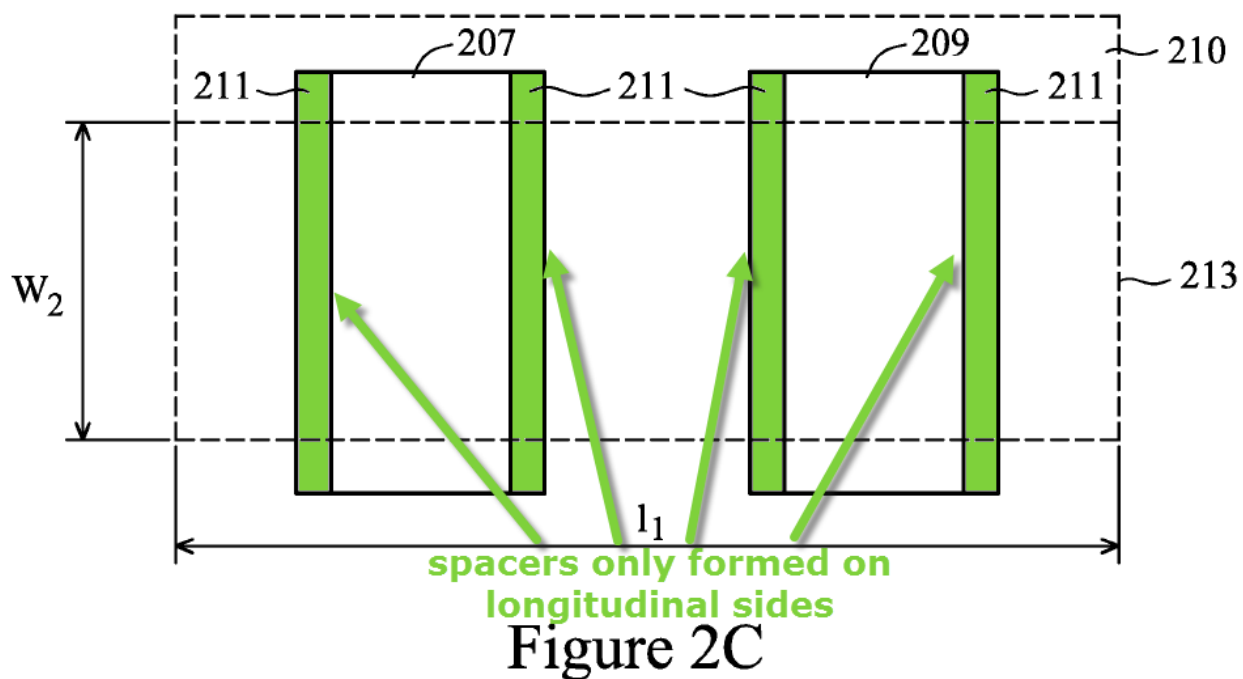


Figure 2C clearly shows that first spacers 211 only extend along the length, but not the ends, of structures 207 and 209. *Id.*, Fig. 2C. As such, the described manufacturing process used to make the permanent spacers in Liaw results in spacers that only extend along the gate length direction and do not cover the ends of the gate.

Petitioner thus fails to establish a reasonable likelihood that Liaw meets limitation 1[c] either expressly or inherently.

- ii **Liaw Fails to Disclose Limitation 1[d]**
 (“performing inter-device electrical isolation at a predetermined position after forming the dielectric spacer, wherein isolated portions of the gate line form independent gate electrodes of respective devices”)

**(1) Petitioner Fails to Show that Liaw Discloses
“Inter-Device Electrical Isolation” and
“Independent Gate Electrodes of Respective
Devices”**

As a separate and independent ground for denial of institution, Petitioner’s Ground 1 allegations entirely fail to address the claims’ requirements that the “electrical isolation” must be “inter-device” and that the “independent gate electrodes” must be “of respective devices.” Pet. at 34-37. In arguing that Liaw meets limitation 1[d], Petitioner merely states, in relevant part, “Liaw taught electrical isolation of the gate line at a predetermined position to form independent gate electrodes,” deleting the terms “inter-device” and “of respective devices” from the claim language. *Compare* Pet. at 34 *with* Ex. 1001, cl. 1. Similarly, Petitioner’s expert provides no evidence or basis to support his opinion that Liaw discloses “*inter-device* electrical isolation” and “independent gate electrodes *of respective devices*.” *See* Ex. 1002 ¶¶ 230-231. His opinion that Liaw discloses these claims terms is entitled to no weight. *Intel Corp. v. VLSI Tech. LLC*, IPR2018-01038, Paper 18 at 21 (P.T.A.B. Dec. 4, 2018) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”) (citing 37 C.F.R. § 42.65(a)). As discussed previously, Petitioner offers no claim construction position that those phrases are not limiting. Nor does Petitioner provide any other justification for reading the

phrases out of the challenged claims. Petitioner instead withholds its theory of how the cited prior art allegedly discloses these claims terms and deprives Patent Owner of the ability to fully defend against Petitioner's invalidity challenges. This is not allowed under the rules. 37 C.F.R. § 42.104(b)(4). Petitioner's failure to address or even acknowledge the "inter-device" and "of respective devices" limitations dooms all of the grounds that read limitation 1[d] on Liaw.

**(2) Petitioner Fails to Show that Liaw
Discloses Performing Electrical Isolation
After Forming Dielectric Spacers**

Liaw also does not disclose "performing inter-device electrical isolation at a predetermined position *after* forming the dielectric spacer" of limitation 1[d], which is alleged by Petitioner to be the "point of novelty" of the '719 Patent. Petitioner's basis for contending otherwise is that the paragraph in Liaw discussing the formation of permanent spacers merely precedes the paragraph discussing gate separation, which reads more into the reference than its explicit disclosures. Pet. at 36-37. Critically, nothing in Liaw indicates that the formation of permanent spacers in fact takes place before gate separation. Indeed, Liaw does not disclose any advantage of separating the gate electrodes after forming permanent spacers.

Other than an explicit disclosure that forming permanent spacers is one of the last steps in the manufacturing process—which directly contradicts Petitioner's characterization—Liaw is in fact silent on the order in which spacer formation and

electrical isolation must take place. Liaw teaches, “The memory device 100 may be completed through the formation of permanent spacers (not shown), source/drain regions (not shown), and silicide contacts (not shown).” Ex. 1003 at 7:25-27. Specifically, according to Liaw, permanent spacers may be formed on opposite sides of the gate electrode 309 (*id.* at 7:27-38); then, the gate electrode 309 and permanent spacers are used as masks to implant the source/drain regions (*id.* at 7:46-47); and lastly, Liaw teaches forming electrical connections between transistors using the source/drain regions (*id.* at 8:18-61). As such, Liaw discloses the following steps which take place sequentially: (1) forming gate electrode 309, (2) forming permanent spacers along the gate electrode 309; (3) implanting source/drain regions; and (4) forming electrical connections using the source/drain regions. Liaw does not explicitly disclose how gate patterning fits into the above sequence. By definition, gate patterning must take place after step (1), gate formation, but Liaw is silent on whether gate patterning takes place before or after step (2), the formation of permanent spacers, and Liaw discloses no reason of choosing to do it either before or after. *See generally id.* at 8:5-17. Moreover, Liaw’s disclosure that “The memory device 100 may be *completed* through the formation of permanent spacers [], source/drain regions [], and silicide contacts” suggests that these are the last steps in the manufacturing process—i.e., after gate patterning is completed. *Id.* at 7:25-27 (emphasis added). Accordingly, in light of

the above, Petitioner's attempt to rely on the order in which text is arranged in the reference runs counter to the express disclosure.

Lacking support from the express disclosure of the reference, Petitioner resorts to crafty annotations of its figures to mislead the Board into believing that Liaw teaches cutting gate electrodes after spacer formation. Pet. at 35-36. Specifically, the "[s]idewall spacer" added by Petitioner in annotated Figure 3J (Pet. at 36) is not part of Liaw's disclosure. *Compare* Pet. at 33 *with* Ex. 1003, Fig. 3J. Similarly, in its annotated Figure 3K, Petitioner only added sidewall spacers to the long sides of the gate electrodes but not the ends, in attempt to advance its argument that cutting of the gate electrodes took place after spacers were placed along the gate electrodes. *Compare* Pet. at 35 *with* Ex. 1003, Fig. 3K (comparison shown below). Again, the added sidewall spacer in annotated Figure 3K is not part of Liaw's disclosure. Liaw is explicit that permanent spacers are "not shown" in any figure. Ex. 1003 at 7:25-27. Thus, Petitioner's assertion that Liaw discloses "performing inter-device electrical isolation at a predetermined position *after* forming the dielectric spacer" does not find support in the figures of Liaw.

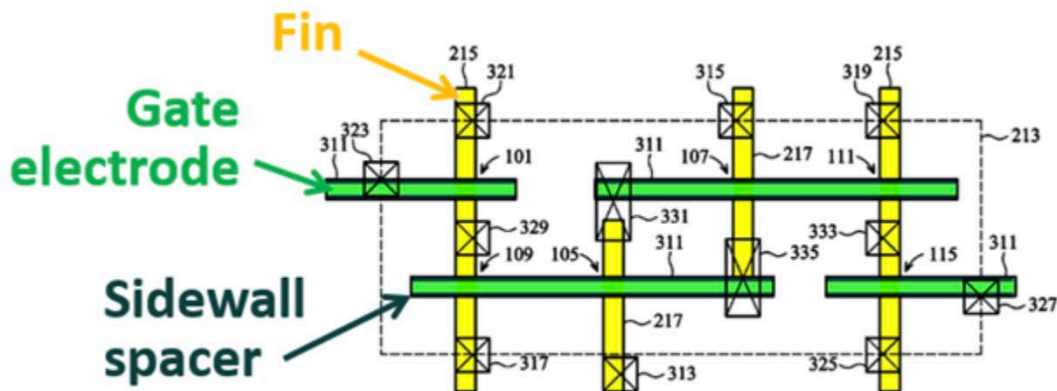


Figure 3K

Petitioner's Annotated 3K (with added "sidewall spacer")

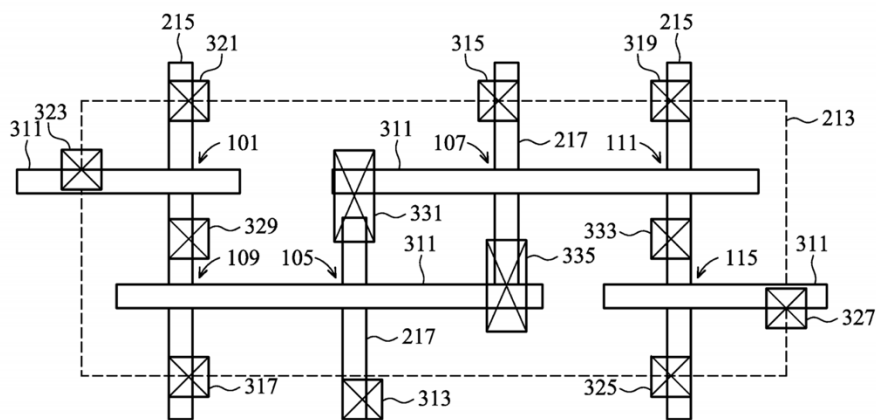


Figure 3K

Actual Figure 3K from Liaw

Petitioner's reliance on Liaw's reference to "gate electrode 309" is equally unjustified and contradicted by Liaw's explicit disclosure. Specifically, Petitioner and its expert argue that Petitioner's position regarding the timing of the cutting of the gates in Liaw is supported by Liaw's supposed use of different designations for "uncut gate" and "separated gate electrodes." Pet. at 37. According to Petitioner,

Liaw refers to the “uncut gate” as 309 (in Figure 3J) and the “separated gate electrodes” as 311 (in Figure 3K). Relying on Liaw’s teaching that permanent spacers are placed along “gate electrode 309” (which can only be uncut according to Petitioner), Petitioner concludes that the spacers may only be formed on the uncut gate, and that spacer formation must therefore happen before gate cutting. *Id.*; Ex. 1002 ¶¶ 230-231. This argument is clearly contradicted by the disclosure of Liaw. Liaw explicitly states that element 311 denotes the dielectric, not any gate electrode, in the embodiment illustrated in Figures 3A-3M. Ex. 1003 at 6:66-7:3 (“FIGS. 3G-3H illustrate a cross-sectional view and plan view, respectively, of the patterning of the gate electrode layer 303 and the gate dielectric layer 301 (see FIGS. 3A-3E) into a gate electrode 309 and *gate dielectric 311*”) (emphasis added), 7:11-13 (“FIGS. 3I-3J illustrate the removal of the second spacers 307 from *the gate dielectric 311* and gate electrode 309”) (emphasis added), 7:21-24 (“any suitable removal process may alternatively be utilized to remove the second spacers 307 while maintaining the gate electrode 309 and *gate dielectric 311*”) (emphasis added), 2:22-23 (Figs. 3A-3M illustrate the same embodiment). Thus, Petitioner’s alleged distinction between uncut gate and separated gate electrodes on the basis of numerical designations is demonstrably false.

Accordingly, Petitioner fails to establish a reasonable likelihood that Liaw discloses both limitations 1[c] and 1[d]. Petitioner’s assertions that Liaw

anticipates claims 2 and 6 of the '719 Patent, both of which are dependent on claim 1, must fail as well. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1576 (Fed. Cir. 1987) (“Because [independent] claim 1 is not invalid, the presence of all its limitations in [dependent] claim 6 preserves the latter’s validity.”).

2. Ground 2 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Liaw Combined with Kim Renders Obvious Claim 7

Ground 2 of the Petition (regarding claim 7) suffers from at least the same deficiencies as Ground 1 with respect to limitations 1[c] and 1[d]. In Ground 2, Petitioner asserts that the combination of Liaw and Kim renders obvious claim 7, which is dependent on claim 1. Petitioner does not assert that Kim discloses any limitation of claim 1, but cites Kim solely in attempt to meet limitations that are unique to claim 7. Pet. at 39-43. As a result, the addition of Kim does not remedy Liaw’s deficiency of failing to disclose limitations 1[c] and 1[d], and Petitioner has failed to show a reasonable likelihood of prevailing on Ground 2.

3. Ground 3 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Okuno Combined with Liaw Renders Obvious Claims 1-3 and 6

In Ground 3, Petitioner claims that Okuno discloses all limitations of claim 1 other than 1[a], and argues that a person of ordinary skill in the art would have been motivated to incorporate fins as taught by Liaw into Okuno’s two-dimensional FET design. Pet. at 43-54. However, Petitioner fails to show that

Okuno discloses limitations 1[c] and 1[d], or that a person of ordinary skill in the art would have been motivated to combine Okuno and Liaw with a reasonable expectation of success.

**i Petitioner Fails to Show that Element 27 of
Okuno Meets Limitation 1[c]**

With respect to limitation 1[c], Petitioner points to element 27 of Okuno as the alleged “dielectric spacer surrounding the gate line.” Pet. at 49 (citing Ex. 1005 ¶ [0026]). To the contrary, element 27 is an extension region within the substrate *below* the gate line, and therefore does not cover any side surface of the gate line. Petitioner fails to show that element 27 meets limitation 1[c]: “forming a dielectric spacer surrounding the gate line.”

**(1) Element 27 is an Extension Region
Within the Substrate**

Element 27 of Okuno does not meet the “dielectric spacer surrounding the gate line” limitation. Petitioner’s cited paragraph from Okuno discloses that element 27 is formed by extension implantation: “Next, *extension implantation is performed*, as the gate electrode 25 still remains continuous, *so as to form sidewall spacers* [] 27, and source/drain implantation is performed to form source/drain regions 28, as illustrated in FIG. 6C.” Ex. 1005 ¶ [0026] (emphasis added); *see also* ¶ [0010]. The process of “extension implantation” does not introduce new materials or create new structure. Rather, “extension implantation” refers to the

process of implanting impurities into an existing substrate to define source drain extension regions within the substrate *beneath* the gate. *See* Ex. 2021 at 12:55-60 (“A first drain extension implantation process 420 is performed in FIG. 5B ... to implant As or other n-type dopant species in *drain extension regions* 422a of the substrate 408 adjacent to and defining a channel region 416 beneath the gate 404.”) (emphasis added), Fig. 5B (“extension regions” annotated in blue and shown below).

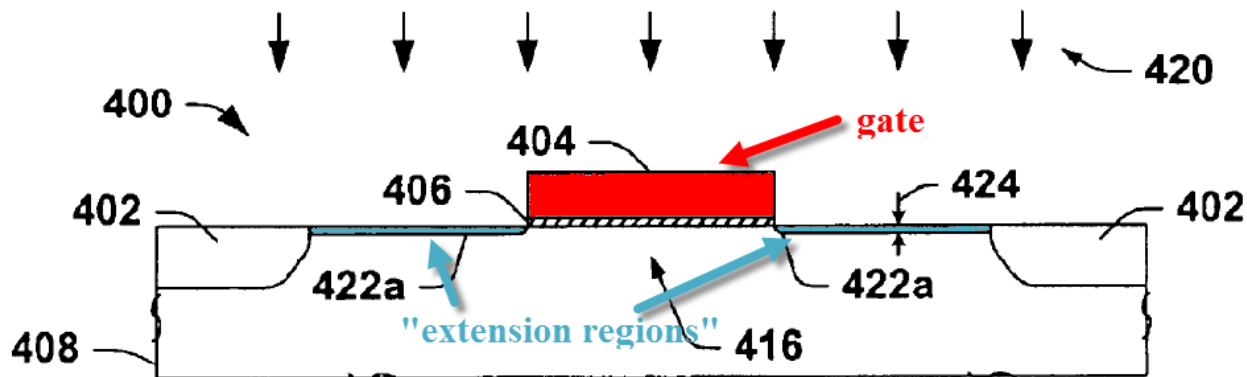
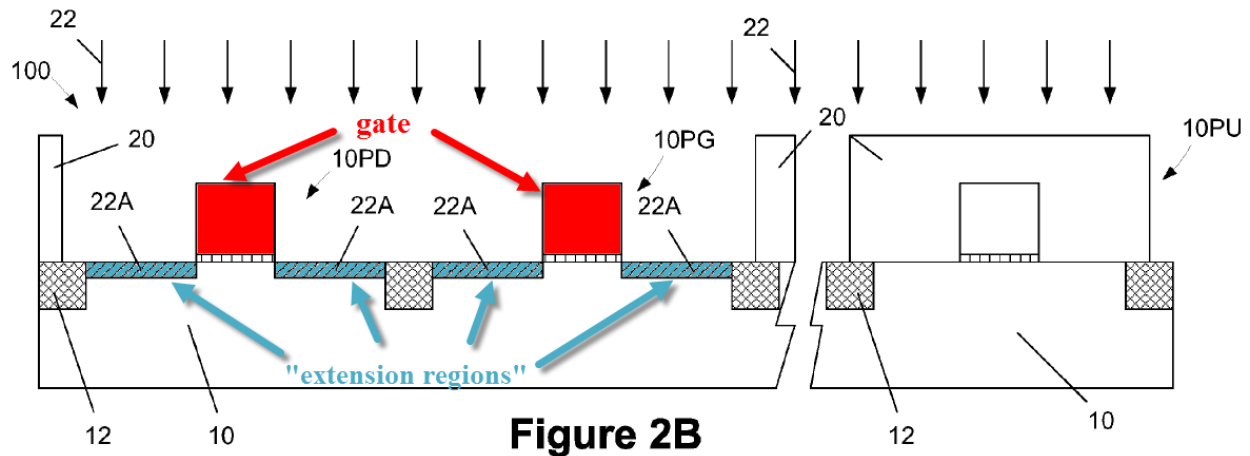


FIG. 5B

See also Ex. 2022 ¶ [0025] (“Next, as shown in FIG. 2B, an extension ion implant process 22 is performed on the exposed pull-down transistor 10PD and pass gate transistor 10PG to define *extension implant regions* 22A in the substrate 10 for both of the transistors 10PD, 10PG”) (emphasis added), Fig. 2B (“extension regions” annotated in blue and shown below).



Since element 27, Petitioner’s alleged “dielectric spacer,” is formed by extension implantation, it can only be an extension region within the existing substrate *below* gate 25, rather than a distinct structure created to surround the side surfaces of gate 25.

The remaining disclosure of Okuno cited in the Petition is consistent with the teaching that element 27 is formed by extension implantation. Paragraph [0033] of Okuno states, “extension implantation [is] performed . . . so as to dispose the sidewalls 27 formed, for example, of a CVD oxide film having a thickness of 30 to 80 nm.” Ex. 1005 ¶ [0033]; Pet. at 49. This disclosure confirms that element 27 is formed by extension implantation, and teaches that the region within the substrate—later to be defined as the extension region—may be formed of a CVD oxide film. Okuno provides no additional disclosure regarding where the oxide film that forms element 27 is deposited. Nor do the figures in Okuno show any cross section of the design to allow for Petitioner’s position that element 27

extends from the substrate along side surfaces of gate 25 so as to surround the gate line as required by the claims of the '719 patent. Ex. 1005.

Therefore, Okuno's explicit disclosure shows that element 27 is an extension region within the substrate below the gate line, and cannot possibly meet the limitation "dielectric spacer surrounding the gate line."

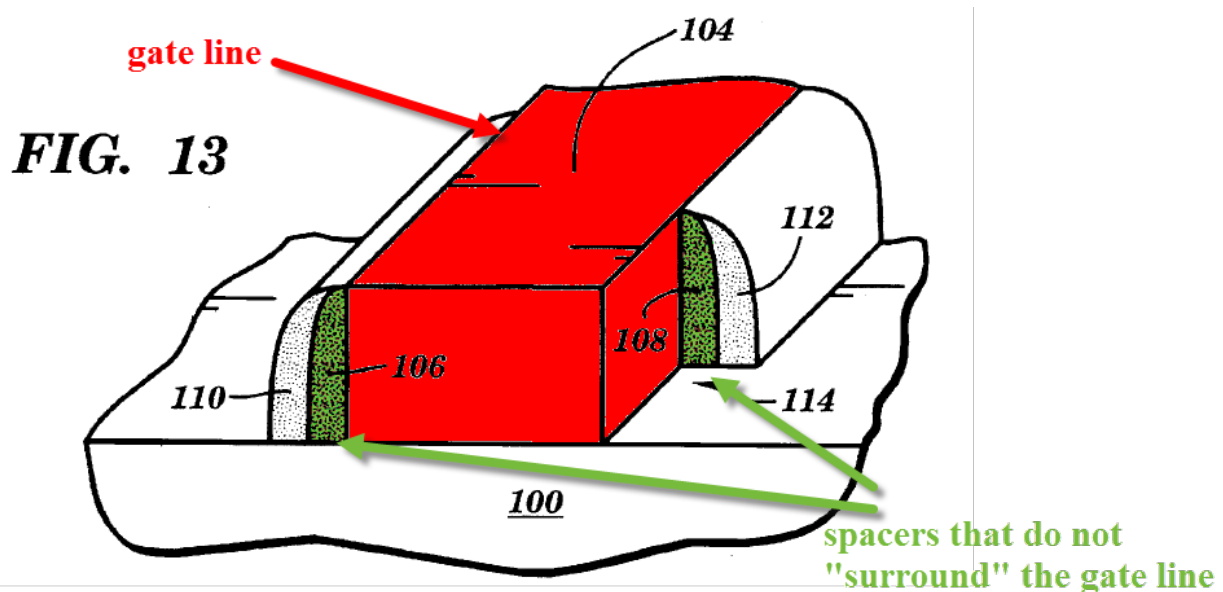
**(2) Element 27 of Okuno Does Not
"Surround" the Gate Line**

Even assuming *arguendo* that element 27 extends from the substrate along side surfaces of gate 25, it still falls short of meeting the limitation "dielectric spacer surrounding the gate line" under the proper claim construction, because Okuno does not disclose that element 27 encloses the gate 25 on all side surfaces.

Indeed, Okuno explicitly discloses that element 27 is not formed at the ends of gate 25. Ex. 1005 ¶ [0028] ("Unlike the conventional method, the sidewalls 27 are provided *only* in the longitudinal direction of the gate (i.e. along the gate length direction)") (emphasis added). Because element 27 is only formed along the gate length direction, it does not enclose the gate line on all side surfaces.

The assertion by Petitioner's expert that element 27 is necessarily formed on "all sides of the gate line, both lateral sides and the end faces" due to the "conventional CVD technique" can be easily rejected. *See* Ex. 1002 ¶ 266. First, no amount of hand-waving by Petitioner's expert can detract from the explicit

disclosure of Okuno that sidewalls 27 do not extent to the end faces as explained above. Moreover, in contrast to Petitioner's expert's assertion, conventional CVD technique does not necessarily lead to coverage on all sides of a gate. For example, a prior art patent discloses using conventional CVD techniques to form spacer 108 from oxide- or nitride-type material. Ex. 2023 at 1:29-52, 9:41-43. As shown in Figure 13 of the same patent, spacer 108 not only fails to cover ends of the gate, but also leaves parts of a longitudinal side surface of the gate exposed. *Id.* at 9:53-62, Fig. 13 (annotated and shown below with spacers that do not "surround" the gate line). Consequently, a person of ordinary skill in the art would not understand Okuno's reference of the CVD oxide film to override the explicit disclosure that element 27 is only formed along the gate length direction.

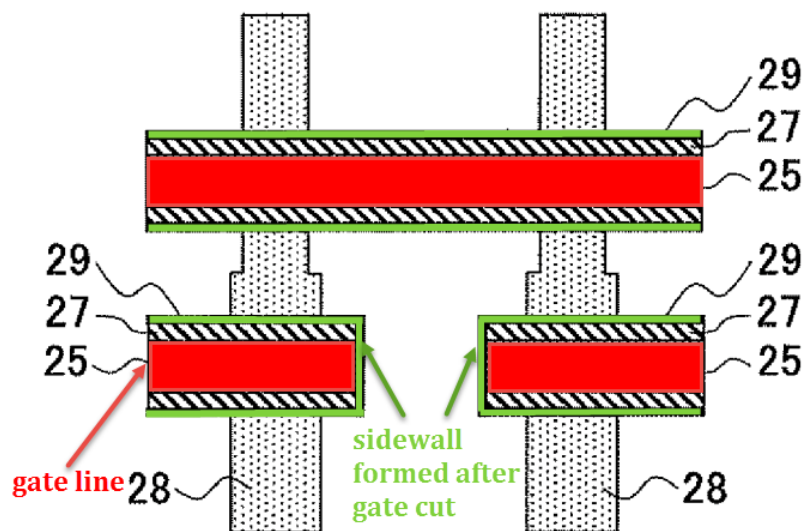


As such, Petitioner fails to show that element 27 meets the limitation “dielectric spacer surrounding the gate line.”

ii Okuno Fails to Meet Limitation 1[d]

At best, only element 29 of Okuno can possibly meet the limitation “dielectric spacer surrounding the gate line.” Ex. 1005 ¶ [0036]. However, Okuno discloses forming sidewalls 29 *after* gate 25 has been cut, thereby failing to meet limitation 1[d]. Okuno teaches that, in order to prevent silicide corrosion of the gate edges 25a, which are exposed after gate 25 has been cut, thin sidewalls 29 can be formed to cover the exposed gate edges 25a. *Id.* ¶¶ [0035], [0036]. By definition, the formation of sidewalls 29 must take place *after* gate 25 has been cut in order to cover gate edges 25a to protect them from silicide corrosion, because gate edges 25a are only formed and exposed as result of cutting of the gate 25. Figure 7E of Okuno shows sidewalls 29 being disposed on the ends of gate 25, confirming that sidewalls 29 are formed after gate 25 has been cut into separate gate electrodes. *Id.* Fig. 7E (annotated and shown below). Therefore, Okuno teaches forming dielectric spacers *after* performing the alleged electrical isolation of the gate electrodes, which is the conventional process that the claimed invention of the ’719 Patent distinguishes from.

FIG.7E



In addition, just like Grounds 1 and 2, Petitioner and its expert’s discussion of Ground 3 is devoid of any explanation of how the claim terms “inter-device” and “of respective devices” in limitation 1[d] read on the cited prior art. Pet. at 52-54; Ex. 1002 ¶¶ 275-281. Given the lack of any claim construction position regarding these terms, Petitioner’s failure to disclose its theory of how the cited prior art meets these terms deprives Patent Owner of the ability to fully defend against Petitioner’s invalidity challenges and invites the Board to assume that these terms are met under some unstated construction. This omission alone warrants non-institution with respect to Ground 3. *See* Section IV.B.1.ii(1) *supra*.

As discussed previously, Petitioner fails to show that Liaw discloses limitations 1[c] and 1[d]. Consequently, the addition of Liaw does not remedy Okuno's deficiency with respect to those limitations, and Petitioner thus fails to show that the combination of Okuno and Liaw discloses all limitations of the challenged claims.

iii Petitioner Fails to Show that A Person of Ordinary Skill in the Art Would be Motivated to Combine Okuno with Liaw

Petitioner's arguments regarding the motivation to combine Okuno and Liaw are based on nothing more than generalities about the references and the generic problems in the field, and are insufficient to establish a motivation to combine. *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017). Petitioner makes two arguments in support of a motivation to combine Okuno and Liaw: (1) "both relate to the formation of six-transistor cell or '6T' cell SRAMs in semiconductor device fabrication"; and (2) both "had the same imperative to make SRAMs smaller." Pet. at 43. Neither argument provides a sufficient reason that is supported by the reference as to why a person of ordinary skill in the art would be motivated to look to the other reference.

As to the **first argument**, Petitioner essentially proposes that a person of ordinary skill in the art would be motivated to combine *any* references in the SRAM field, regardless of the specific designs taught therein, including whether

the designs are two- or three-dimensional.² The Federal Circuit has previously rejected combining prior art simply because they “both fall[] within the same alleged field,” as “[s]uch short-cut logic would lead to the conclusion that any and all combinations of elements known in this broad field would automatically be obvious, without the need or any further analysis.” *Securus*, 701 F. App’x at 977. Petitioner fails to explain why, other than hindsight, a person of ordinary skill in the art would have been motivated to look to the two-dimensional structure of Okuno from the wide field of SRAM cell design, and to then combine it with the three-dimensional structure of Liaw. As Liaw itself appreciates, the conventional methods of manufacturing both two dimensional/planar and three-dimensional/FinFET devices, such as “standard lithographic techniques” are “untenable as a primary manufacturing technology for FinFETs.” Ex. 1003 at 1:24-34. Indeed, Petitioner itself took over a decade to replace two-dimensional/planar transistors with three-dimensional FinFET transistors in its own products. Ex. 1033. Petitioner’s suggestion that one is motivated to simply

² The 6T cell layout is the standard and conventional layout for SRAM memory cells. *See* Ex. 1006 ¶ [0004] (“One representative construction for a conventional SRAM memory cell, which is frequently referred to as a 6T cell, consists of six transistors.”).

substitute planar active regions with three-dimensional fins in any two-dimensional device does not hold up to the required scrutiny.

Petitioner's **second argument** regarding motivation to combine fares no better. Petitioner ignores that Okuno and Liaw are directed towards solving entirely different problems when it lumps them together under the generic objective of "size reduction." Pet. at 59-60. Like Petitioner's conclusory and generic statement that Okuno and Liaw are both directed towards SRAM devices, simply stating that both Okuno and Liaw would make transistors smaller, without more, does not establish why a person of ordinary skill in the art would be motivated to combine these specific references. Size reduction is a generic consideration applicable to all transistor design and manufacturing. Ex. 2002 at 1. This is not enough. *Securus*, 701 F. App'x at 976. Petitioner provides no basis for why a person of ordinary skill in the art would be motivated to combine these two specific references as opposed to others from the entire field of transistor design and manufacturing. What is completely missing from the Petition is an explanation of how Okuno's disclosure of a way to eliminate asymmetrical impurity characteristics in two-dimensional devices (Ex. 1005 ¶ [0027]) applies to the disclosures in Liaw which purport to address the problems with conventional lithography during the manufacture of three-dimensional devices (Ex. 1003, Abstract). Nothing in Liaw suggests that any teaching found therein would help a

person of ordinary skill in the art with problems associated with asymmetrical impurity characteristics. Nor does Petitioner point to any evidence in either reference that conventional lithography would be problematic for two-dimensional devices. Thus, there would be no motivation for a person of ordinary skill in the art to look to and apply any teaching in Liaw to solve a problem that does not exist in Okuno. Petitioner cannot rely on conclusory and generic statements regarding the common field in which the references lie when the references themselves provide no support for such a combination. *Microsoft Corp. v. Enfish, LLC*, 662 F. App'x 981, 990 (Fed. Cir. 2016).

**iv Petitioner Fails to Show A Reasonable
Expectation of Success When Combining
Okuno and Liaw**

Petitioner also fails to articulate how the combination of Okuno and Liaw would successfully lead to the claimed invention. To show a reasonable expectation of success, a petition must “explain convincingly, with adequate specificity, how one would have achieved that result.” *Biodelivery Scis. Int’l, Inc. v. Monosol Rx, LLC*, IPR2015-00167, Paper 6 at 28 (P.T.A.B. May 20, 2015).

The Petition is entirely devoid of any explanation of how a person of ordinary skill in the art would have achieved the combination of Okuno and Liaw. Petitioner’s expert generically asserts—in portions of his testimony not cited by Petitioner—that “compatible techniques were used for planar and fin-based

designs.” Ex. 1002 ¶ 173. In support, Dr. Thompson provides examples of both Petitioner and Patent Owner having applied certain unrelated two-dimensional techniques to three-dimensional processes, which have no bearing on how a person of ordinary skill in the art would have achieved the specific combination of Okuno and Liaw. *Id.* ¶¶ 175-177. Essentially, Petitioner’s argument boils down to the proposition that a person of ordinary skill in the art would expect to successfully convert any two-dimensional SRAM design into a three-dimensional design, simply because Petitioner and Patent Owner had specific instances of success in the past. This proposition runs counter to Liaw’s explicit teaching that conventional techniques are “untenable” in the three-dimensional context and is entirely driven by hindsight bias. Ex. 1003 at 1:24-34; *see also* Ex. 2010 at 12.1.1. Petitioner’s casual summation of the prior art does not explain with any specificity how a person of ordinary skill in the art would successfully replace the planar active regions in Okuno with three-dimensional fins to achieve the claimed invention of the ’719 Patent. The absence of evidence throughout the Petition on how the disclosure of Okuno could work with Liaw’s fins—given the differences in the purposes, technology, and structures of the two references—is fatal to Petitioner’s argument for why the combination would yield predictable and reliable results.

Petitioner fails to establish a reasonable likelihood that the combination of Okuno and Liaw renders claim 1 obvious. Petitioner's assertions that the combination of Okuno and Liaw renders obvious dependent claims 2, 3, and 6 must fail as well. *Panduit*, 810 F.2d at 1576 (Fed. Cir. 1987). The Petition fails to establish a likelihood of prevailing as to Ground 3.

4. Ground 4 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Okuno Combined with Liaw and Kim Renders Obvious Claim 7

Ground 4 of the Petition (regarding claim 7) suffers from at least the same deficiencies as Ground 3. In Ground 4, Petitioner asserts that the combination of Okuno, Liaw, and Kim renders obvious claim 7, which is dependent on claim 1. Petitioner does not assert that Kim discloses any limitation of claim 1, but cites Kim solely in attempt to meet limitations that are unique to claim 7. Pet. at 56-57. As a result, the addition of Kim does not remedy the deficiencies identified in Ground 3, and Petitioner has thus failed to show a reasonable likelihood of prevailing on Ground 4.

5. Ground 5 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Mandelman Combined with Liaw Renders Obvious Claims 1-3 and 6

In Ground 5, Petitioner claims that Mandelman discloses all limitations of claim 1 other than 1[a], and argues that a skilled person would have been

motivated to incorporate fins as taught by Liaw into Mandelman's two-dimensional FET design. Pet. at 57-66. However, Petitioner fails to show that Mandelman discloses limitations 1[c] and 1[d], or that a person of ordinary skill in the art would have been motivated to combine Mandelman and Liaw with a reasonable expectation of success.

i Mandelman Fails to Disclose Limitation 1[c]

Mandelman fails to teach forming dielectric spacer surrounding the gate line, because it only discloses forming spacers along the two longitudinal sides of each conductor line, but not at the ends. Specifically, Mandelman discloses, "sidewall spacers 42, 44 are formed on the sidewalls 37*a, b* of conductor line 36, sidewall spacers 46, 48 are formed on the sidewalls 39*a, b* of conductor line 38, and sidewall spacers 50, 52 are formed on the sidewalls 41*a, b* of conductor line 40." Ex. 1006 ¶ [0029], Fig. 2 (annotated and shown below). Mandelman does not disclose forming spacers on any other sides of the conductor lines, namely the ends. *See* Ex. 1006.

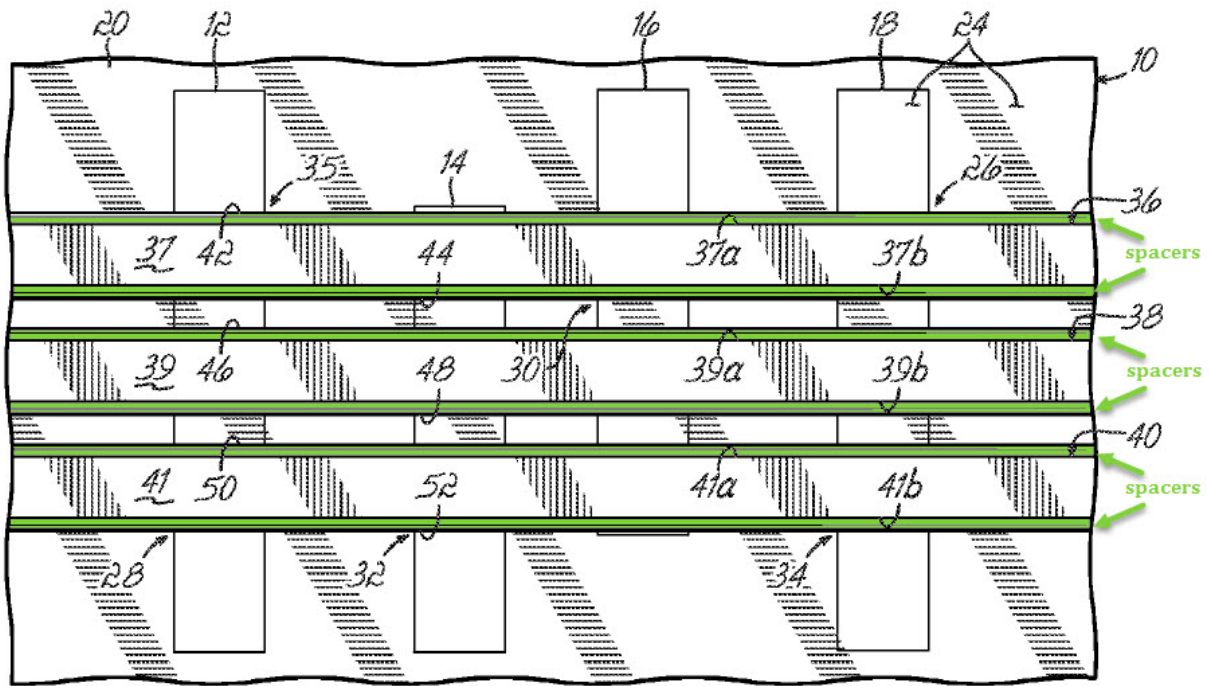


FIG. 2

Just like Grounds 1 and 3, Petitioner's reliance on Mandelman's disclosed manufacturing process of the sidewall spacers is insufficient to establish that the sidewall spacers are actually formed at the ends of the gate line as required by limitation 1[c]. *See* Pet. at 62-63 (citing Ex. 1002 ¶¶ 316-318). As discussed previously in connection with Ground 1, spacers formed by blanket deposition followed by anisotropic etching (such as reactive ion etching) do not necessarily extend along all side surfaces of the gate. *See* Ex. 1006 ¶ [0029]; *see supra* Section IV.B.1.i. Accordingly, Petitioner fails to show that Mandelman discloses limitation 1[c].

ii Mandelman Fails to Disclose Limitation 1[d]

Like Grounds 1 to 4, Petitioner’s Ground 5 obviousness allegations fail to analyze whether the claim elements “inter-device electrical isolation” and “independent gate electrodes of respective devices” are actually disclosed in the prior art. Petitioner states, without explanation, that Figure 4 of Mandelman “depict[s] electrical isolation of gate lines into respective devices.” Pet. at 65-66. In support, Petitioner does not point to any disclosure in Mandelman, but solely cites expert testimony. *Id.* However, the cited paragraphs in Dr. Thompson’s declaration only relate to how Mandelman teaches “electrical isolation,” and contain no opinion as to why the gates, once electrically isolated, become “respective devices.” Ex. 1002 ¶ 325. Although Dr. Thompson conclusorily states that “Mandelman taught performing inter-device electrical isolation,” his declaration offers no explanation for how the “inter-device” limitation is actually met. Short of any analysis of how Mandelman actually discloses these limitations, Dr. Thompson’s conclusory statement cannot adequately support Petitioner’s assertion that Mandelman discloses the “inter-device” and “of respective devices” limitations. *VLSI Tech.*, IPR2018-01038, Paper 18 at 21. Given the lack of any claim construction position regarding these terms, Petitioner’s failure to disclose its theory of how the cited prior art meet these terms deprives Patent Owner of the ability to fully defend against Petitioner’s invalidity challenges and invites the

Board to assume that these terms are met under some unstated construction.. This omission alone warrants non-institution with respect to Ground 5. *See* Sections IV.B.1.ii(1), IV.B.3.ii *supra*.

iii Petitioner Fails to Show that A Person of Ordinary Skill in the Art Would be Motivated to Combine Mandelman with Liaw

Like Ground 3, Petitioner's arguments regarding the motivation to combine Mandelman and Liaw are based on nothing more than generalities about the references and the generic problems in the field, and are insufficient to establish a motivation to combine. *Securus*, 701 F. App'x at 977. As in Ground 3, Petitioner only makes two arguments in support of a motivation to combine Mandelman and Liaw: (1) "both relate to forming SRAM transistors in semiconductor device fabrication"; and (2) both "had the same imperative to make SRAMs smaller." Pet. at 57. Neither argument provides a sufficient reason that is supported by the reference as to why a person of ordinary skill in the art would be motivated to look to the other reference.

As to the **first argument**, Petitioner once again proposes that a person of ordinary skill in the art would be motivated to combine *any* references in the SRAM field, regardless of the specific designs taught therein, including whether the designs are two- or three-dimensional. As discussed previously in connection

with Ground 3, this argument must be rejected under Federal Circuit precedent.

Securus, 701 F. App'x at 977.

Petitioner's failure to identify a specific motivation to combine Mandelman and Liaw is magnified by the fact that the disclosures in Mandelman and Liaw are directed towards two entirely different FET designs. On the one hand, Liaw discloses a method of manufacturing three-dimensional FinFET devices, which involves *electrically isolating* the gate electrodes to form transistors and *using metal local interconnects* to establish electrical connections between different transistors. Ex. 1003 at 8:5-17, 8:47-61. Mandelman, on the other hand, discloses a two-dimensional/planar FET design which *eliminates metal local interconnects* by using a *conducting* silicide layer to *electrically connect* different transistors. Ex. 1006 ¶¶ [0034]-[0045]. Petitioner does not explain how a person of ordinary skill in the art could combine Mandelman, a reference that discloses *electrically connecting* gate electrodes to *eliminate* metal interconnects, with Liaw, a reference that discloses *electrically isolating* gate electrodes while *adding* metal interconnects. Petitioner's attempt to mix and match two fundamentally incompatible designs should be rejected.

Petitioner's **second argument** regarding motivation to combine fares no better. As in Ground 3, Petitioner ignores that Mandelman and Liaw are directed towards solving entirely different problems when it lumps them together under the

generic objective of “shrinking transistors.” Pet. at 59-60. Simply stating that both Mandelman and Liaw would make transistors smaller, without more, does not establish why a person of ordinary skill in the art would be motivated to combine these specific references, because shrinking transistors is a generic consideration applicable to all transistor design and manufacturing. Ex. 2002 at 1. This is not enough. *Securus*, 701 F. App’x at 976. Petitioner provides no basis for why a person of ordinary skill in the art would be motivated to combine these two specific references as opposed to others from the entire field of transistor design and manufacturing. The Petition completely fails to provide an explanation of how Mandelman’s disclosure of a way to eliminate metal interconnects in two-dimensional devices applies to the disclosures in Liaw which purport to address the problems with conventional lithography during the manufacture of three-dimensional devices. Nothing in Liaw suggests that any teaching found therein would help a person of ordinary skill in the art with problems associated with metal interconnects. Nor does Petitioner point to any evidence in either reference that conventional lithography would be problematic for two-dimensional devices. Thus, there would be no motivation for a person of ordinary skill in the art to look and apply any teaching in Liaw to solve a problem that does not exist in Mandelman. Petitioner cannot rely on conclusory and generic statements regarding the common field in which the references lie when the references

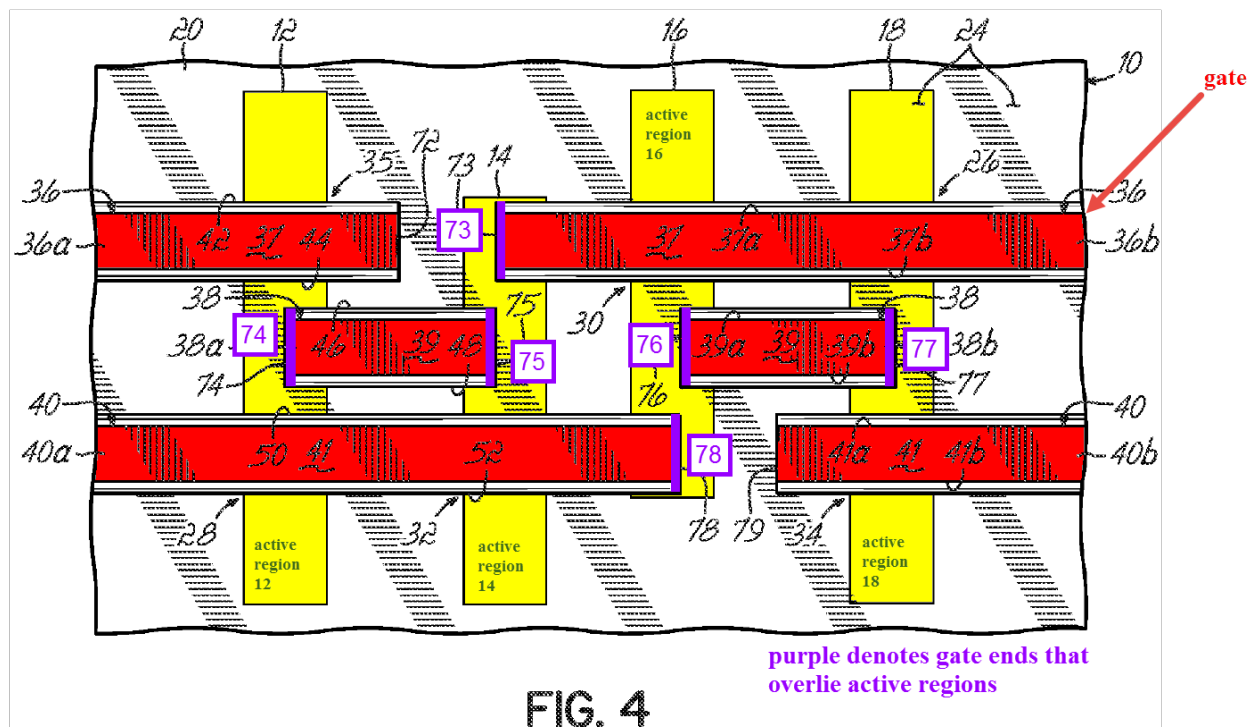
themselves provide no support for such a combination. *Enfish*, 662 F. App'x at 990.

**iv Petitioner Fails to Show A Reasonable
Expectation of Success When Combining
Mandelman and Liaw**

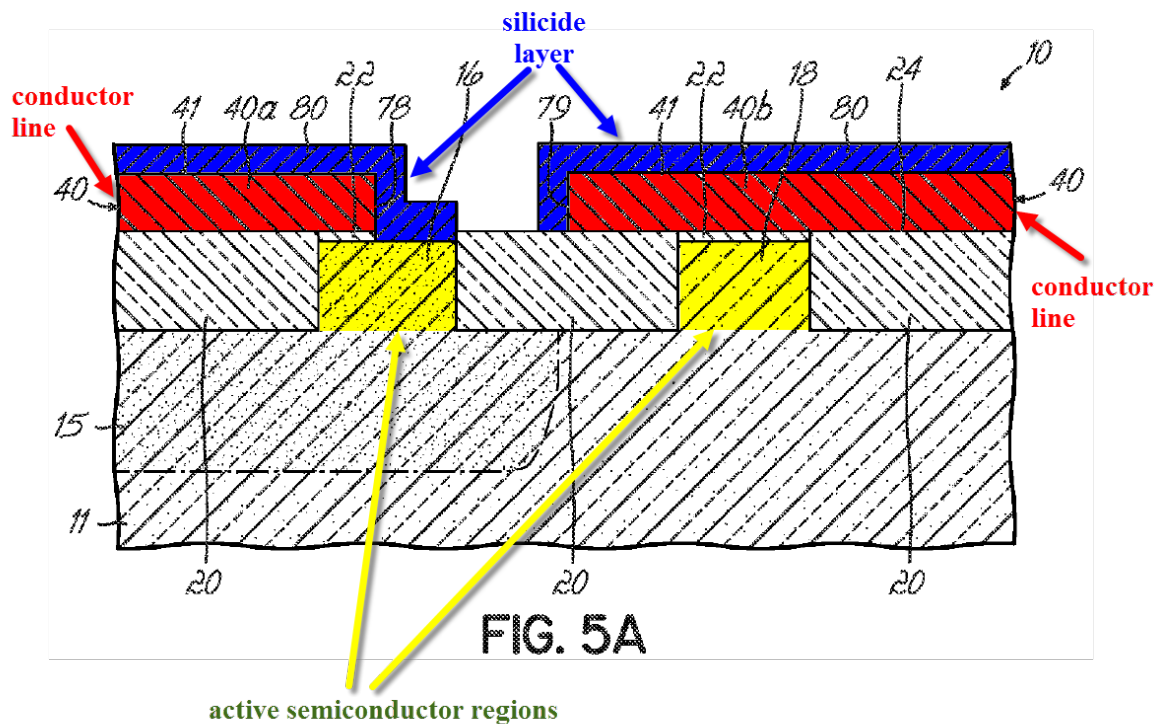
Petitioner also fails to sufficiently articulate how the combination of Mandelman and Liaw would successfully lead to the claimed invention. Instead of providing the required specificity, Petitioner asserts in conclusory fashion that “[t]he compatibility between planar and FinFET fabrication techniques was known in the state of the art.” Pet. at 40. Although Petitioner cites its expert for support, Dr. Thompson’s declaration only points to Patent Owner and Petitioner’s past success in applying particular (and different) two-dimensional techniques to three-dimensional devices, which is irrelevant to how a person of ordinary skill in the art would successfully modify Mandelman with the disclosures of Liaw to achieve the claimed invention in the ’719 Patent. Ex. 1002 ¶¶ 173-178, 203; *see also* Section IV.B.3.iv *supra*.

Petitioner fails to address how a person of ordinary skill in the art would incorporate the fins of Liaw into Mandelman. To achieve electrical connection (as opposed to isolation) between gate electrodes, Mandelman specifically requires that the subject gate cut must take place directly above an active region. In particular, as shown in Figure 4 of Mandelman, gate end 74 overlies active region

12; gate ends 73 and 75 overlie active region 14; gate ends 76 and 78 overlie active region 16; and gate end 77 overlies active region 18. Ex. 1006, Fig. 4 (annotated and shown below); *see, e.g., id.* ¶ [0034] (“One segment 40 a of the conductor line 40 has an exposed substantially vertical surface on a sidewall 78 overlying the active semiconductor region 16.”).



Mandelman also requires that the silicide layer be deposited on the exposed top portions of the active regions. *Id.* ¶ [0036] (“a silicide layer 80 is formed on the top surface 24 of the active semiconductor regions 12, 14, 16, 18 not covered by the conductor lines 36, 38, 40”), Fig. 5A (annotated and shown below).



Accordingly, Mandelman requires that gate cut and silicide layer deposition must both take place on top of the active regions. This is necessary to establish electrical connections between the gate electrodes using the silicide layer. *See, e.g., id.* ¶ [0038] (“The sidewall 73 of the gate conductor structure defined by segment 36*b* is electrically coupled with the sidewall 75 of the segment 38*a* of the conductor line 38 by electrically connective bridges defined by respective portions of the silicide layer 80 on sidewalls 73, 75 and by the portion of the silicide layer 80 on the active semiconductor region 14 between the sidewalls 73, 75.”); *see also id.* ¶ [0039].

Mandelman's design is achievable in the planar/two-dimensional context where active regions have sufficient width. In contrast, fins in three-dimensional FinFET devices must have considerably smaller width to minimize short-channel effects. Ex. 2012 at 489; *compare* Ex. 1003 at 4:2-4 (spacers 211 from which fins are formed have thickness "between about 10 Å and about 700 Å, such as about 30 Å" (i.e. between about 1 nm to 70 nm, such as 3 nm)), 4:45-48 *with* Ex. 1006 ¶ [0008] ("the conventional photolithography tools can only resolve line widths of about 90 nm"), ¶ [0024] ("Active semiconductor regions 12, 14, 16, 18 ... are fabricated by standard processes"). Therefore, if applied to the three-dimensional FinFET context, Mandelman's design would necessarily involve both cutting the gate and forming a silicide layer on top of a very narrow top surface of a thin fin structure. Petitioner and its expert provide no explanation as to how that is expected to be achievable—especially in view of both Liaw and Mandelman's comments on the limitations of the standard lithographic process to scale down far enough to allow such resolution. Ex. 1003 at 1:24-34; Ex. 1006 ¶ [0008]; *see also* Ex. 2010 at 12.1.1. The absence of evidence throughout the Petition on how the disclosure of Mandelman could work together with Liaw's fins—given the differences in the purposes, technology, and structures of the two references—is fatal to Petitioner's argument for why the combination would yield predictable and reliable results.

In sum, Petitioner attempts to stitch together two inapposite references that address different problems, use different techniques to solve those problems, and together fail to fully disclose all elements of the challenged claims. Hindsight has driven Petitioner to its conclusion. Accordingly, Petitioner fails to show that the combination of Mandelman and Liaw renders claim 1 obvious. Petitioner's assertions that the combination of Mandelman and Liaw renders obvious dependent claims 2, 3, and 6 must fail as well. *Panduit*, 810 F.2d at 1576 (Fed. Cir. 1987).

6. Ground 6 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Mandelman Combined with Liaw and Kim Renders Obvious Claim 7

Ground 6 of the Petition (regarding claim 7) suffers from at least the same deficiencies as Ground 5. In Ground 6, Petitioner asserts that the combination of Mandelman, Liaw, and Kim renders obvious claim 7, which is dependent on claim 1. Petitioner does not assert that Kim discloses the limitations 1[c] and 1[d] which are missing from Liaw and Mandelman, but cites Kim solely in attempt to meet limitations that are unique to claim 7. Pet. at 56-57. As a result, the addition of Kim does not remedy Liaw and Mandelman's deficiency of failing to disclose limitations 1[c] and 1[d], and Petitioner has thus failed to show a reasonable likelihood of prevailing on Ground 6.

7. Ground 7 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Okuno Combined with Chang Renders Obvious Claims 1-3 and 6

Ground 7 of the Petition suffers from at least the same deficiencies as Ground 3. In Ground 7, Petitioner asserts that the combination of Okuno and Chang renders claims 1-3 and 6 of the '719 Patent obvious. Petitioner does not contend that Chang discloses limitations 1[c] or 1[d], but relies solely on the teachings of Okuno in attempt to meet that limitation. Pet. at 79-81. As discussed in Section IV.B.3, Petitioner fails to show that Okuno discloses both limitations 1[c] and 1[d]. As a result, the addition of Chang does not remedy Okuno's deficiency, and Petitioner has thus failed to show that the combination of Okuno and Liaw discloses all limitations of the challenged claims.

Further, Petitioner fails to show that a person of ordinary skill in the art would have been motivated to combine Okuno and Chang with a reasonable expectation of success.

i Petitioner Fails to Show A Person of Ordinary Skill in the Art Would be Motivated to Combine Mandelman with Liaw

Like Grounds 3 and 5, Petitioner's arguments regarding the motivation to combine Okuno and Chang are based on nothing more than generalities about the references and the generic problems in the field, and are insufficient to establish a motivation to combine. *Securus*, 701 F. App'x at 977. As in Grounds 3 and 5,

Petitioner only makes two arguments in support of a motivation to combine Okuno and Chang: (1) “both relate to semiconductor device fabrication of SRAMs”; and (2) both “shared the objective of making circuits smaller.” Pet. at 57. Neither argument provides a sufficient reason that is supported by the reference as to why a person of ordinary skill in the art would be motivated to look to the other reference.

As to the **first argument**, Petitioner once again proposes that a person of ordinary skill in the art would be motivated to combine *any* references in the SRAM field, regardless of the specific designs taught therein, including whether the designs are two- or three-dimensional. As discussed previously in connection with Grounds 3 and 5, this argument must be rejected under Federal Circuit precedent. *Securus*, 701 F. App’x at 977.

Regarding the **second argument**, Petitioner fails to explain why—other than hindsight—a person of skill in the art would have been motivated to incorporate three-dimensional structure of Chang into Okuno to achieve size reduction, when Chang expressly discourages the use of three-dimensional structures. Specifically, Chang teaches separating planar active regions (referred to by Chang as “patterned diffusion regions”) by “isolation regions 314.” Ex. 1004 at 3:11-19, Fig. 3B (annotated and shown below).

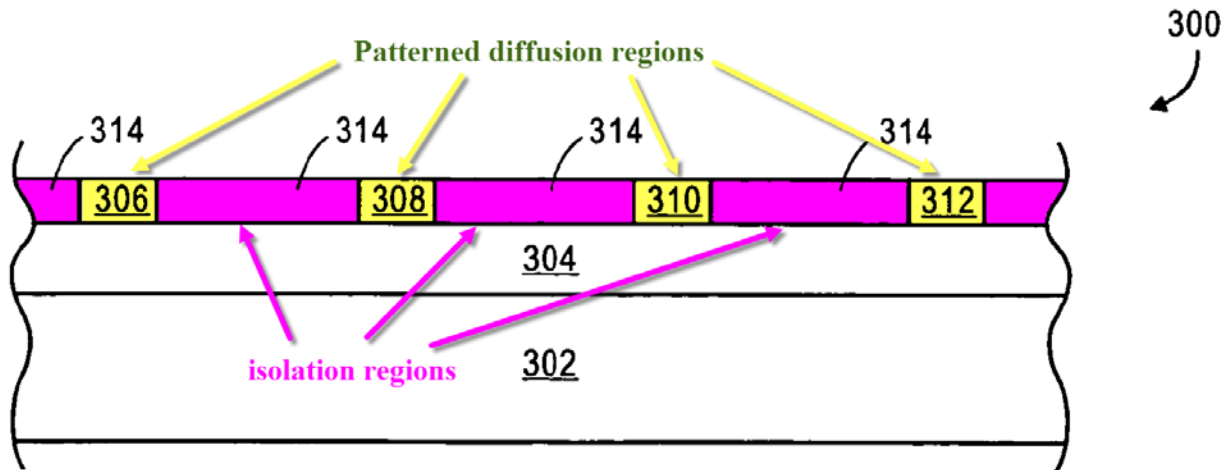


FIG. 3B

Chang also teaches that when isolation regions 314 are not present, the active regions become three-dimensional “tri-gate” structures—which Petitioner alleges to be fins (Pet. at 74)—and “the substrate surface would not be planar.” Ex. 1004 at 3:25-30. However, according to Chang, the planarity of the substrate surface is preferred. *Id.* at 3:17-21 (“the isolation regions 314 may improve planarity of the substrate surface and may be advantageous.”). In other words, Chang recommends planar active regions (separated by isolation regions) over three-dimensional tri-gate structures (without isolation regions) to achieve planarity of the substrate. A person of ordinary skill in the art would not be motivated to incorporate a three-dimensional structure into Okuno with this teaching. *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (“[A] reference must be considered for all it taught, disclosures that diverged and taught away from the invention at

hand as well as disclosures that pointed towards and taught the invention at hand. ... [E]ven if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding whether a skilled artisan would be motivated to combine that reference with another reference.”) (internal quotations omitted); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 n.15 (Fed. Cir. 2016) (*en banc*). Given Chang’s express preference for planar active regions over three-dimensional tri-gate structures, the basis for Petitioner’s alleged motivation to import the three-dimensional structures of Chang into Okuno can only be impermissible hindsight. *Merck Sharp & Dohme B.V. v. Warner Chilcott Co., LLC*, 711 F. App’x 633, 637 (Fed. Cir. 2017) (“The district court’s reliance on hindsight is further underscored by the prior art’s criticism of the one-compartment solution. PCT ’015 expressly states that one compartment rings are undesirable because it is difficult to control the release rates for both compounds.”).

Further, as in Grounds 3 and 5, Petitioner ignores that Okuno and Chang are directed towards solving entirely different problems when it lumps them together under the generic objective of size reduction. Pet. at 74-75. Like Petitioner’s conclusory and generic statement that Okuno and Chang are both directed towards SRAM devices, simply stating that both Okuno and Chang would make circuits smaller, without more, does not establish why a person of ordinary skill in the art would be motivated to combine these specific references. Size reduction is a

generic consideration applicable to all transistor design and manufacturing. Ex. 2002 at 1. This is not enough. *Securus*, 701 F. App'x at 976. Petitioner provides no basis for why a person of ordinary skill in the art would be motivated to combine these two specific references as opposed to others from the entire field of transistor design and manufacturing. Petitioner fails to address how Okuno's disclosure of a way to eliminate asymmetrical impurity characteristics (Ex. 1005 ¶ [0027]) applies to the disclosures in Chang which purport to reduce the occurrence of gate electrode/diffusion region misalignment (Ex. 1004 at 1:33-47). Nothing in Chang suggests that any teaching found therein would help a person of ordinary skill in the art with problems associated with asymmetrical impurity characteristics. Nor does Petitioner point to any evidence in either reference that gate electrode/diffusion region misalignment was an issue with the method disclosed in Okuno. Thus, there would be no motivation for a person of ordinary skill in the art to look and apply any teaching in Liaw to solve a problem that does not exist in Okuno. Petitioner cannot rely on conclusory and generic statements regarding the common field in which the references lie when the references themselves provide no support for such a combination. *Enfish*, 662 F. App'x at 990.

**ii Petitioner Fails to Show A Reasonable
Expectation of Success When Combining
Okuno and Chang**

Petitioner also fails to sufficiently articulate how the combination of Mandelman and Liaw would successfully lead to the claimed invention. Like Ground 3, Petitioner’s discussion of Ground 7 is entirely devoid of any explanation of how a person of ordinary skill in the art would have achieved the combination of Okuno and Chang. The only basis for Petitioner’s alleged reasonable expectation of success is uncited expert testimony regarding the general compatibility between two- and three-dimensional techniques. Ex. 1002 ¶¶ 173-178. As discussed previously, this testimony is irrelevant to whether a person of ordinary skill in the art would have a reasonable expectation of success in combining Okuno and Chang specifically. *See* Sections IV.B.3.iv, IV.B.5.iv *supra*. The absence of evidence throughout the Petition on how the disclosure of Okuno could work with Chang’s “fins”—especially given Chang’s explicit preference for two-dimensional designs—is fatal to Petitioner’s argument for why the combination would yield predictable and reliable results.

Petitioner fails to establish a reasonable likelihood that the combination of Okuno and Chang renders claim 1 obvious. Petitioner’s assertions that the combination of Okuno and Chang renders obvious dependent claims 2, 3, and 6 must fail as well. *Panduit*, 810 F.2d at 1576 (Fed. Cir. 1987).

8. Ground 8 Must Fail Because Petitioner Does Not Establish a Reasonable Likelihood that Okuno Combined with Chang and Kim Renders Obvious Claim 7

Ground 8 of the Petition suffers from at least the same deficiencies as Ground 7 with respect to limitations 1[c] and 1[d]. In Ground 8, Petitioner asserts that the combination of Okuno, Chang, and Kim renders obvious claim 7, which is dependent on claim 1. Petitioner does not assert that Kim discloses limitations 1[c] or 1[d], but cites Kim solely in attempt to meet limitations that are unique to claim 7. Pet. at 56-57. As a result, the addition of Kim does not remedy Okuno and Chang's deficiency with respect to limitations 1[c] and 1[d], and Petitioner has thus failed to show a reasonable likelihood of prevailing on Ground 8.

C. The Petition Exceeds the Word Limit

Throughout its Petition, Petitioner uses atypical citation formats in order to exceed the 14,000-word limit imposed under 37 C.F.R. § 42.24(a)(i). Specifically, Petitioner omits a space between the paragraph symbol and the paragraph number (e.g. "¶26"). *See generally* Pet. As such, Petitioner manages to make two words appear to be a single word to word count software. The Petition includes a certification stating that the word count of the Petition is 13,935. *See* Pet. (Certificate of Word Count Under 37 C.F.R. § 42.24(d)). Because 320 non-standard citations appear in the Petition, the Petition is over the word limit by about 250 words. Petitioner has not filed a motion to waive the word count

pursuant to 37 C.F.R. § 42.24(a)(2), but has instead exceeded the word limit without attempting to obtain authorization.

The Board has disapproved of this particular formatting trick of omitting the space after the paragraph symbol to exceed the word limit. *EMC Corp. v. Intellectual Ventures I, LLC*, IPR2017-00429, Paper 11 at 28-29 (P.T.A.B. July 5, 2017). The Board should exercise its discretion here to deny the Petition or to impose another appropriate remedy to the Petition's violation of the word limit.

V. CONCLUSION

For the foregoing reasons, the Board should deny the Petition.

Dated: January 28, 2019

Respectfully submitted,

/David C. Radulescu/

David C. Radulescu, Ph.D. (Reg. No. 36,250)

david@radip.com

Etai Lahav (*pro hac vice*)

etai@radip.com

Jonathan A. Auerbach (Reg. No. 59,193)

jonathan@radip.com

RADULESCU LLP

The Empire State Building

350 Fifth Avenue, Ste. 6910

New York, NY 10118

Phone: (646) 502-5950

Facsimile: (646) 502-5959

**Attorneys for Patent Owner
Institute of Microelectronics,
Chinese Academy of Sciences**

CERTIFICATION UNDER 37 C.F.R. §42.24

The undersigned certifies that the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE PURSUANT TO 37 C.F.R. § 42.107(a)** complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 10,882 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

Dated: January 28, 2019

/David C. Radulescu/
David C. Radulescu, Ph.D.
(Reg. No. 36,250)
david@radip.com
RADULESCU LLP
The Empire State Building
350 Fifth Avenue, Ste. 6910
New York, NY 10118
Phone: (646) 502-5950
Facsimile: (646) 502-5959

**Attorneys for Patent Owner
Institute of Microelectronics,
Chinese Academy of Sciences**

CERTIFICATE OF SERVICE

I hereby certify that on January 28, 2019, a copy of the foregoing:

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

were served via email to counsel of record for Petitioner at the following:

Jonathan McFarland
PERKINS COIE
1201 Third Avenue, Suite 4900
Seattle, WA 98101-3099
Phone: (206) 359-8000
Facsimile: (206) 359-9000
Email: Intel-IMECAS-Service-IPR@perkinscoie.com

Dated: January 28, 2019

/David C. Radulescu/
David C. Radulescu, Ph.D.
(Reg. No. 36,250)
david@radip.com
RADULESCU LLP
The Empire State Building
350 Fifth Avenue, Ste. 6910
New York, NY 10118
Phone: (646) 502-5950
Facsimile: (646) 502-5959

**Attorneys for Patent Owner
Institute of Microelectronics,
Chinese Academy of Sciences**