

## TITLE OF THE INVENTION

### METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

#### 5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of, and claims the benefit of priority under 35 U.S.C. § 120 from U.S. Serial No. 14/754,111, filed June 29, 2015, which is a division of U.S. Serial No. 14/197,070, filed March 4, 2014, which is a division of U.S. Serial No. 13/341,273, filed December 30, 2011, which is a continuation of U.S. Serial No. 12/954,740,  
10 filed November 26, 2010, now Patent No. 8,153,505, which is a continuation of U.S. Serial No. 12/720,368 filed March 9, 2010, now Patent No. 7,871,898, which is a continuation of U.S. Serial No. 11/980,664 filed October 31, 2007, now Patent No. 7,807,549, which is a continuation of U.S. Serial No. 10/913,441 filed August 9, 2004, now Patent No. 7,387,944, which is a continuation of U.S. Serial No. 09/505,283, filed February 16, 2000, now Patent  
15 No. 6,902,987, the entire contents of each of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to bonding of materials at room temperature and, in particular, to bonding of processed semiconductor materials, such as integrated circuit or  
20 device substrates, having activated surfaces to achieve high bonding strength adequate for subsequent fabrication and/or a desired application.

### 2. Background of the Invention

Direct room temperature bonding generally produces weak van der Waals or  
25 hydrogen bonding. Annealing is typically required to convert the weak bond to a stronger chemical bond such as a covalent bond. Other wafer bonding techniques including anodic and fusion typically require the application of voltage, pressure and/or annealing at elevated temperature to achieve a sufficient bond strength for subsequent fabrication and/or the desired application. The need to apply voltage, pressure or heat has significantly limited  
30 wafer bonding applications because these parameters can damage the materials being wafer bonded, give rise to internal stress and introduce undesirable changes in the devices or materials being bonded. Achieving a strong bond at low temperatures is also critical for

bonding of thermally mismatched or thermally sensitive wafers including processed device wafers.

Ultra high vacuum (UHV) bonding is one of the approaches to achieve a low or room temperature strong bond. However, the bonding wafers still have to be pre-annealed at high temperatures, for instance  $>600^{\circ}\text{C}$  for silicon and  $500^{\circ}\text{C}$  for GaAs, before cooling down to low or room temperature for bonding. Furthermore, the UHV approach does not generally work on commonly used materials, for example, in  $\text{SiO}_2$ . It is further also expensive and inefficient.

Adhesive layers can also be used to bond device wafers to a variety of substrates and to transfer device layers at low temperatures. However, thermal and chemical instability, interface bubbles, stress and the inhomogeneous nature of adhesive layers prevent its wide application. It is thus highly desirable to achieve a strong bond at room temperature by bonding wafers in ambient without any adhesive, external pressure or applied electric field.

Low vacuum bonding has been explored as a more convenient alternative to UHV bonding but a bonding energy comparable to the bulk silicon fracture energy using bonded bare silicon wafer pairs has only been achieved after annealing at  $\sim 150^{\circ}\text{C}$ . For oxide covered silicon wafer pairs annealing at  $\sim 300^{\circ}\text{C}$  is required to obtain a high bond energy. It has not been possible to obtain high bonding energies in bonded material using low vacuum bonding at room temperature.

A gas plasma treatment prior to bonding in ambient is known to enhance the bonding energy of bonded silicon pairs at low or room temperature. See, for example, G.L. Sun, Q.-Y. Tong, et al., *J. de Physique*, 49(C4), 79 (1988); G.G. Goetz, *Proc. of 1st Symp. on Semicond. Wafer Bonding: Science, Technol. and Applications*, The Electrochem. Soc., 92-7, 65 (1992); S. Farrens et al., *J. Electroch. Soc.*, 142, 3950 (1995) and Amirfeiz et al, *Abstracts of 5th Symp. on Semi. Wafer Bonding: Science, Tech. and Appl.*, The Electrochemical Society, 99-2, Abstract No. 963 (1999). Although these treatments have increased the bond energy obtainable at low or room temperature, they have only been demonstrated with planar silicon wafers or with silicon wafers using a plasma process that results in oxide being grown on the wafers during the plasma process. Moreover, these treatments have only been used to increase the bond energy by charging or damaging the surface. Furthermore, these treatments have not been used or shown to be applicable to deposited dielectrics or other materials.

Obtaining low or room temperature bonding with a method that is not only applicable to planar silicon and grown oxide surfaces but further to deposited materials and non-planar

surfaces with planarized deposited materials will allow generic materials, including processed semiconductor wafers, to be bonded with minimal damage for manufacturing purposes. Such a method based on etching and chemical bonding is described herein.

5

## SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for bonding materials at low or room temperature.

It is another object of the invention to bond materials by cleaning and activating the bonding surfaces to promote chemical bond formation at about room temperature.

10

It is a further object of the invention to provide a bonding method to bond any solid state material such as processed device or integrated circuit wafers or thermally sensitive or mis-matched materials at or about room temperature.

15

It is further object of the invention to provide a bonding method to bond processed device or integrated circuit wafers of different types of devices or different technologies, and transfer a layer of devices or circuits at or about room temperature.

It is another object of the invention to enable a direct wafer bonding method that does not require annealing to achieve a required bond strength.

20

It is a further object of the invention to provide a method whereby diverse materials including those with non-planar surfaces and deposited materials can be planarized and bonded.

These and other objects are achieved by a method of bonding having steps of forming first and second bonding surfaces, etching the first and second bonding surfaces, and

25

bonding together at room temperature the first and second bonding surfaces after said etching step. The etching may include etching the first and second bonding surfaces such that respective surface roughnesses of the first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching. The surface roughness may be in a range of 0.1 to 3.0 nm.

30

The bonding surfaces may be the surface of a deposited insulating material, such as silicon oxide, silicon nitride or a dielectric polymer. The bonding surface may also be the surface of a silicon wafer. Silicon wafers, using either the surface of the wafer or a deposited material on the wafer, may be bonded together. The wafers may have devices or integrated circuits formed therein. The devices and circuits in the wafers bonded together may be

interconnected. The wafers may have a non-planar surface or an irregular surface topology upon which a material is deposited to form the bonding surfaces.

Forming at least one of the bonding surfaces may include depositing a polishable material on a non-planar surface. Depositing said polishable material may include depositing one of silicon oxide, silicon nitride or a dielectric polymer. The bonding surfaces may be polished using a method such as chemical-mechanical polishing. The surfaces may also be etched prior to the polishing.

The etching step may also include activating the first and second bonding surfaces and forming selected bonding groups on the first and second bonding surfaces. Bonding groups may also be formed capable of forming chemical bonds at approximately room temperature, and chemical bonds may be formed between the bonding surfaces allowing bonded groups to diffuse or dissociate away from an interface of the bonding surfaces. The chemical bonds can increase the bonding strength between the bonding surfaces by diffusing or dissociating away said bonding groups.

After said etching step, the bonding surfaces may be immersed in a solution to form bonding surfaces terminated with desired species. The species may comprise at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group. Also, a monolayer of one of a desired atom and a desired molecule may be formed on the bonding surface. Terminating the surface may include rinsing said bonding materials in an ammonia-based solution after said slightly etching. The ammonia-based solution may be ammonium hydroxide or ammonium fluoride.

The method may also include exposing the bonding surfaces to one of an oxygen, argon,  $\text{NH}_3$  and  $\text{CF}_4$  RIE plasma process. Silicon dioxide may be deposited as to form the bonding surfaces, and etched using the RIE process.

The etching process may create a defective or damaged zone proximate to the bonding surfaces. The defective or damaged zone can facilitate the removal of bonding by-products through diffusion or dissociation.

The method may also include steps of forming first and second bonding surfaces, etching the bonding surfaces, terminating the bonding surfaces with a species allowing formation of chemical bonds at about room temperature, and bonding the bonding surfaces at about room temperature, or may include steps of forming the bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm, removing material from the bonding surfaces while maintaining said surface roughness, and directly bonding the bonding surfaces at room



temperature with a bonding strength of at least  $500 \text{ mJ/m}^2$ , at least  $1000 \text{ mJ/m}^2$ , or at least  $2000 \text{ mJ/m}^2$ .

5 The objects of the invention may also be achieved by a bonded device having a first material having a first etched bonding surface, and a second material having a second etched bonding surface directly bonded to the first bonding surface at room temperature having a bonding strength of at least  $500$  to  $2000 \text{ mJ/m}^2$ . The bonding surfaces may be being activated and terminated with a desired bonding species, and the desired species may include a monolayer of one of a desired atom and a desired molecule on said bonding surface or at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group. The bonding  
10 surfaces may each have a defective region located proximate to said first and second bonding surfaces, respectively.

The first material may include a surface of a first semiconductor wafer having devices formed therein, and the second material may include a surface of a second semiconductor wafer having devices formed therein. Devices in the wafers may be interconnected, and the  
15 wafers may be of different technologies. The wafers may also have an integrated circuit formed therein, and devices or circuits in the wafers may be interconnected.

One of said first and second wafers may be a device region after removing a substantial portion of a substrate of said one of said first and second wafers. The wafers may have an irregular surface topology.

20 The first material may include a first wafer containing electrical devices and having a first non-planar surface, and the first bonding surface may include a polished and etched deposited oxide layer on said first non-planar surface. The second material may include a second wafer containing electrical devices and having a second non-planar surface, and the second bonding surface may include a polished, planarized and slightly etched deposited  
25 oxide layer on the second non-planar surface.

The first material may include a first wafer containing electrical devices and having a first surface with irregular topology, and the first bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the first surface. The second material may include a second wafer containing electrical devices and having a second surface with  
30 irregular topology, and the second bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the second surface.

The bonded device according to the invention may also include a first material having a first etched and activated bonding surface terminated with a first desired bonding species,

and a second material having a second etched and activated bonding surface terminated with a second desired bonding species bonded to the first bonding surface at room temperature.

### BRIEF DESCRIPTION OF THE DRAWINGS

5 A more complete appreciation of the invention and many of the attendant advantages thereof are readily obtained as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart of the method according to the invention;

10 FIG. 2 is a flow chart of an example of the method according to the invention;

FIGS. 3A-3E are diagrams illustrating a first embodiment of a method according to the invention;

FIGS. 4A-4E are diagrams illustrating bonding according to the invention using silicon oxide;

15 FIGS. 5A-5E are diagrams illustrating bonding according to the invention using silicon;

FIGS. 6A and 6B are graphs of room temperature bonding energy versus storage time;

FIG. 7 is a diagram of a bonding fixture used in the invention; and

FIG. 8 is a fluorine concentration profile by SIMS (Secondary Ion Mass Spectroscopy) near the bonding interface of deposited oxide covered silicon wafers that were  
20 very slight etched by diluted HF before bonding.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. 1 and 3A-3E, a first embodiment of the method according to the  
25 invention will be described. Wafer 30, preferably a processed semiconductor device wafer and more preferably a processed silicon device wafer, contains a device layer 31 with processed devices. Device layer 31 may contain a number of layers and include surface regions of wafer 30. The surface topography of layer 31 is typically nonplanar. Layer 31 may also represent a processed integrated circuit containing any number of layers such as  
30 active devices, interconnection, insulation, etc.

The integrated circuit may be fully processed, or partially processed where the remaining processing is performed after the bonding process. The processing after the

bonding may include full or partial substrate removal or via formation between the bonded wafers for interconnection.

On layer 31 a bonding layer 32 is formed (step 1, FIG. 1). Bonding layer 32 may be any solid state material or mixed materials which can be deposited or formed at low temperatures and can be polished to a sufficiently smooth surface. Layer 32 may be an insulator, such as SiO<sub>2</sub>, silicon nitride, amorphous silicon formed using chemical vapor deposition (CVD) or plasma-enhanced CVD (PECVD), sputtering or by evaporation. Other materials such as polymers, semiconductors or sintered materials may also be used. Layer 32 should have thickness greater than the surface topography of layer 31.

The surface 33 of layer 32 is planarized and smoothed, as shown in step 2 of FIG. 1 and in FIG. 3B. It is noted that the roughness/planarity of surface 33 is exaggerated in FIG. 3A for illustrative purposes. This step may be accomplished using chemical-mechanical polishing. Surface 33 is preferably polished to a roughness of about no more than about 3 nm and preferably no more than about 0.1 nm and be substantially planar. The surface roughness values are typically given as root-mean square (RMS) values. Also, the surface roughness may be given as mean values which are nearly the same as the RMS values. After polishing surface 33 is cleaned and dried to remove any residue from the polishing step. Polished surface 33 is preferably then rinsed with a solution.

The bonding surface may also be etched prior to polishing to improve the planarity and/or surface roughness. The etching can be effective to remove high spots on the bonding surface by selective etching of the high spots using, for example, standard photolithographic techniques. For example, a layer of silicon nitride can be embedded within a silicon dioxide bonding layer 32 that can serve as an etch stop when using a solution containing HF. The etch stop material may be used to improve uniformity, reproducibility, and manufacturability.

FIG. 3B illustrates layer 32 having upper surface 34 after the polishing/planarization and cleaning steps. Surface 34 then undergoes an activation process (step 3, FIG. 1). This activation process is an etching process and preferably a very slight etch (VSE) process. The term VSE means that the root-mean-square micro-roughness (RMS) of the very slightly etched surface remains at approximately the unetched value, typically < 0.5 nm and preferably in the range of 0.1 nm to 3 nm. The optimum amount of material removed depends upon the material and the method used for removal. Typical amounts removed vary from Angstroms to a few nanometers. It is also possible to remove more material. VSE also includes the breaking of bonds on the treated surfaces and can occur without significant

removal of material. The VSE is distinct from simple modification of the surface by, for example, charging the surface with electronic charge or damaging the surface layer. In a first example of the method according to the invention, the VSE process consists of a gas or mixed gas (such as oxygen, argon, nitrogen,  $\text{CF}_4$ ,  $\text{NH}_3$ ) plasma process at a specified power level for a specified time (FIG. 3C). The power and duration of the plasma process will vary depending upon the materials used to obtain the desired bond energy. Examples are given below, but in general, the power and duration will be determined empirically.

The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used. Data and examples are given below in both the RIE and plasma modes.

The VSE process etches the surface very slightly via physical sputtering and/or chemical reaction and preferably is controlled to not degrade the surface roughness of the bonding surfaces. The surface roughness may even be improved depending upon the VSE and materials etched. Almost any gas or gas mixture that will not etch surface 34 excessively can be used for the room temperature bonding method according to the invention.

The VSE serves to clean the surface and break bonds of the oxide on the wafer surface. The VSE process can thus enhance the surface activation significantly. A desired bonding species can be used to terminate on surface 34 during the VSE by proper design of the VSE. Alternatively, a post-VSE treatment that activates and terminates the surface with a desired terminating species during the post-VSE process may be used.

The desired species further preferably forms a temporary bond to the surface 34 atomic layer, effectively terminating the atomic layer, until a subsequent time that this surface can be brought together with a surface terminated by the same or another bonding species 36 as shown in FIG. 3D. Desired species on the surfaces will further preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between surfaces 34 and 36 at low or room temperature that is enhanced by diffusion or dissociation and diffusion of the reacted desired species away from the bonding interface.

The post-VSE process preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species. The immersion is preferably performed immediately after the VSE process. The post-VSE process may be performed in the same apparatus in which the VSE process is conducted. This is done most readily if both VSE and post-VSE processes are

either dry, i.e., plasma, RIE, ICP, sputtering, etc., or wet, i.e., solution immersion. A desired species preferably consists of a monolayer or a few monolayers of atoms or molecules.

5 The post-VSE process may also consist of a plasma, RIE, or other dry process whereby appropriate gas chemistries are introduced to result in termination of the surface with the desired species. The post-VSE process may also be a second VSE process. The termination process may also include a cleaning process where surface contaminants are removed without VSE. In this case, a post-cleaning process similar to the post-VSE processes described above then results in a desired surface termination.

10 The post-VSE or post-cleaning process may or may not be needed to terminate surfaces with desired species if the activated surface bonds by the cleaning or VSE process are subsequently sufficiently weakly surface reconstructed and can remain sufficiently clean before bonding such that subsequent bonding with a similar surface can form a chemical bond.

15 The wafers are optionally rinsed then dried. Two wafers are bonded by aligning them (if necessary) and bringing them together to form a bonding interface. As shown in FIG. 3D, a second wafer 35 has been processed in the manner shown in FIG. 3C to prepare bonding surface 36. The two wafers are brought together by, for example, commercially available wafer bonding equipment (not shown) to initiate bonding interface 37 (FIG. 3E).

20 A spontaneous bond then typically occurs at some location in the bonding interface and propagates across the wafer. As the initial bond begins to propagate, a chemical reaction such as polymerization that results in chemical bonds takes place between species used to terminate surfaces 34 and 36 when the surfaces are in sufficient proximity. The bonding energy is defined as the specific surface energy of one of the separated surfaces at the bonding interface that is partially debonded by inserting a wedge. The by-products of the reaction then diffuse away from the bonding interface to the wafer edge or are absorbed by the wafers, typically in the surrounding materials. The by-products may also be converted to other by-products that diffuse away or are absorbed by the wafers. The amount of covalent and/or ionic bonding may be increased by removal of converted species resulting in further increase in bond strength.

30 FIGS. 4A-4E show surface conditions and the bonding propagation to form covalent bonds in the case of a planar Si wafer covered with silicon oxide. On Si wafer 40 an SiO<sub>2</sub> layer 41 is formed, which has been polished and planarized. Surface 42 of layer 41 is subjected to the VSE process to produce an activated surface (FIG. 4A). On a second wafer

44 a second SiO<sub>2</sub> layer 45 is formed, and surface 46 is subjected to a VSE process to activate surface 46 (FIG. 4B). Desired species are terminated on surface 46 and are shown as lines 43 in FIG. 4C. Either or both of a VSE and post-VSE processes are used to properly terminate surface 46. While not shown, surface 42 may also be terminated using a post-VSE process.

5 Wafer 44 is brought together with wafer 40 (FIG. 4D) and bonds 46 begin to form. The bonding propagates and by-products are removed (indicated as arrows 47) and chemical bonds (such as covalent) are formed, as shown in FIG. 4E.

The bonding immediately after the RIE process may use a special bonding fixture allowing immediate in situ bonding of the etched wafers. A diagram of the fixture is shown  
10 in FIG. 7. In plasma chamber 75 are two wafers to be bonded 70 disposed on RF electrodes 76 and 77. A plasma is formed in zone 79 by the application of RF power to the electrodes via moveable vacuum RF power feedthrough 74 and by the introduction of an appropriate gas or gas mixture through gas feedthrough 73. Element 71 is a vacuum feedthrough for mechanical actuator (not shown) to retract retractable spacer 72. Chamber 75 is pumped  
15 down to a desired vacuum level via pumps (not shown) and chamber inlet 78. In the case where a post-VSE process or post cleaning process is also a dry process, as discussed above, the VSE and post-VSE or post-cleaning may be conducted in chamber 75.

After the plasma treatment to conduct the VSE process, the mechanical spacers 72 are retracted by the mechanical actuator and the wafers 70 are moved into contact with to begin  
20 the bonding process. The bonded wafers are then moved from the chamber into ambient or into another vacuum chamber (not shown) and stored for a desired period to allow the bonding to propagate by a wafer handling system (not shown).

The materials of the bonding layers preferably have an open structure so that the by-products of the polymerization reaction can be easily removed. The bonding species on the  
25 opposing bonding surfaces must be able to react at room temperature to form a strong or chemical bond. The bond energy is sufficiently high to virtually eliminate slippage between wafers after subsequent heat treatments associated with a subsequent processing or operation when wafers have different thermal expansion coefficients. Lack of slippage is manifest by a lack of wafer bowing upon inspection after the subsequent processing or operation.

30 In order to achieve the high bonding energies, it is preferable for at least one of the wafers to be as thin as possible because a thin wafer allows compliance to accommodate a lack of perfect surface planarization and smoothness. Thinning to thickness of about 10 mils to 10 microns is effective.

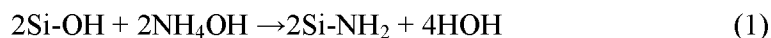
The bonded wafers are preferably stored at ambient or at low or room temperature after bonding to allow removal of species or converted species for a specified period of time depending upon the materials and species used. Twenty four hours is usually preferable. The storage time is dependent upon the type of plasma process used. Chemical bonds may be  
5 obtained more quickly, in a matter of minutes, when certain plasma processes such as an Ar plasma are used. For example, 585 mJ/m<sup>2</sup> bonds were obtained immediately after bonding and over 800 mJ/m<sup>2</sup> were observed after 8 hours for deposited oxides etched by an Ar plasma followed by NH<sub>4</sub>OH dip.

Annealing the bonded wafers during bonding may increase the bonding strength. The  
10 annealing temperature should be below 200°C and may be typically in the range of 75-100°C. Storing the bonded wafers under vacuum may facilitate the removal of residual gasses from the bonding surfaces, but is not always necessary.

All of the processes above may be carried out at or near room temperature. The wafers are bonded with sufficient strength to allow subsequent processing operations  
15 (lapping, polishing, substrate removal, chemical etching, lithography, masking, etc.). Bonding energies of approximately 500-2000 mJ/m<sup>2</sup> or more can be achieved (see FIG. 6A).

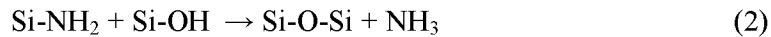
At this point (FIG. 3E) it is possible to remove a part or all of the substrate of wafer 35 by, for instance, lapping and etch back. The layer of devices of wafer 35 is thus transferred onto wafer 30. The devices from the two layers may be interconnected.  
20 Additional device or circuit layers may be bonded and interconnected to form a multilayer structure. Different types of wafers, devices or circuits may be bonded, as well as different technologies (i.e. CMOS and bipolar or III-V HBT and Si CMOS). Other elements or materials such as thermal spreaders, surrogate substrates, antennas, wiring layers, a pre-formed multi-layer interconnects, etc. may be bonded to produce different types of circuits or  
25 systems, as desired.

In an example, shown in FIG. 2, PECVD SiO<sub>2</sub> is deposited on a Si wafer containing devices. Surface 34, after the plasma (such as argon, oxygen or CF<sub>4</sub>) treatment, is mainly terminated by Si-OH groups due to the availability of moisture in the plasma system and in air. After the plasma treatment, the wafers are immediately immersed in solution such as  
30 ammonium hydroxide (NH<sub>4</sub>OH), NH<sub>4</sub>F or HF for a period such as between 10 and 120 seconds. After immersing the wafers in the NH<sub>4</sub>OH solution, many Si-OH groups are replaced by Si-NH<sub>2</sub> groups according to the following substitution reaction:



Alternatively, many Si-F groups are terminating on the PECVD SiO<sub>2</sub> surface after an NH<sub>4</sub>F or HF immersion.

The hydrogen bonded Si-NH<sub>2</sub>:Si-OH groups or Si-NH<sub>2</sub>:Si-NH<sub>2</sub> groups across the bonding surfaces can polymerize at room temperature in forming Si-O-Si or Si-N-N-Si (or Si-N-Si) covalent bonds:



Alternatively, the HF or NH<sub>4</sub>F dipped oxide surfaces are terminated by Si-F groups in addition to Si-OH groups. Since HF or NH<sub>4</sub>F solution etches silicon oxide strongly, their concentrations must be controlled to an adequately low level, and the immersion time must be sufficiently short. This is an example of a post-VSE process being a second VSE process. The covalent bonds across the bonding interface are formed due to the polymerization reaction between hydrogen bonded Si-HF or Si-OH groups:

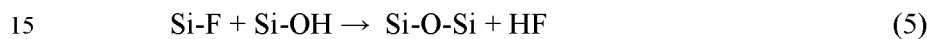
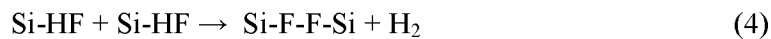


FIG. 8 shows the fluorine concentration profile of bonded thermal oxide covered silicon wafers that were dipped in 0.05% HF before room temperature bonding. A fluorine concentration peak is clearly seen at the bonding interface. This provides evidence of the chemical process described above where the desired species are located at the bonding interface.

Since reaction (2) is reversible only at relatively high temperatures of ~500EC, the formed siloxane bonds should not be attacked by NH<sub>3</sub> at lower temperatures. It is known that H<sub>2</sub> molecules are small and diffuse about 50 times quicker than water molecules in oxide. The existence of a damaged layer near the surface of an adequate thickness i.e. a few nm, will facilitate the diffusion or dissolution of NH<sub>3</sub>, and HF and hydrogen in reactions (2), (3), (4) and/or (5) in this layer and enhancement of the chemical bond. The three reactions result in a higher bonding energy of SiO<sub>2</sub>/SiO<sub>2</sub> bonded pairs at room temperature after a period of storage time to allow NH<sub>3</sub> or H<sub>2</sub> to diffuse away.

In the example of FIG. 2, the plasma treatment may create a damaged or defective area in the oxide layer near the bonding surface. The zone extends for a few monolayers. The damaged or defective area aids in the removal of bonding by-products. Efficient



removal of the bonding by-products improves the bonding strength since the by-products can interfere with the bonding process by preventing high-strength bond from forming.

Many different surfaces of materials may be smoothed and/or planarized, followed by a cleaning process, to prepare for bonding according to the invention. These materials can be room temperature bonded by mating surfaces with sufficient planarity, surface smoothness, and passivation that includes cleaning, and/or VSE, activation and termination. Amorphous and sintered materials, non-planar integrated circuits, and silicon wafers are examples of such materials. Single crystalline semiconductor or insulating surfaces, such as  $\text{SiO}_2$  or Si surfaces, can also be provided with the desired surface roughness, planarity and cleanliness. Keeping the surfaces in high or ultra-high vacuum simplifies obtaining surfaces sufficiently free of contamination and atomic reconstruction to achieve the strong bonding according to the invention. Other semiconductor or insulator materials such as InP, GaAs, SiC, sapphire, etc., may also be used. Also, since PECVD  $\text{SiO}_2$  may be deposited on many types of materials at low temperatures, many different combinations of materials may be bonded according to the invention at room temperature. Other materials may also be deposited as long as appropriate processes and chemical reactions are available for the VSE, surface activation, and termination.

For example, the method may also be used with silicon nitride as the bonding material. Silicon nitride may be bonded to silicon nitride, or to silicon dioxide and silicon. Silicon oxide may also be bonded to silicon. Other types of dielectric materials may be bonded together including aluminum nitride and diamond-like carbon.

The method may be applied to planar wafers having no devices or circuits and one wafer with devices and circuits. The planar wafer may be coated with a bonding layer, such as PECVD oxide or amorphous silicon, and then processed as described above to bond the two wafers. The planar wafer may not need to be coated with a bonding layer if it has sufficient smoothness and planarity and the proper bonding material.

As can be appreciated, the bonding process may be repeated with any number of wafers, materials or functional elements. For example, two device or IC wafers may be joined, followed by removing one of the exposed substrates to transfer a layer or more of devices, or just the active regions of an IC.

The bonding according to the invention may be applied to joining different types of materials. For example, a silicon wafer can be bonded to another silicon wafer, or bond to an oxidized silicon wafer. The bare silicon wafer and the oxide covered wafer are immersed in

HF, NH<sub>4</sub>F and/or NH<sub>4</sub>OH and bonded after drying. The time for the immersion should be less than about twenty minutes for the silicon wafer covered with the thin oxide since the NH<sub>4</sub>OH solution etches silicon oxide. Since HF and NH<sub>4</sub>F etches oxides strongly, very diluted solutions, preferably in 0.01-0.2% range should be used for dipping of the silicon wafers.

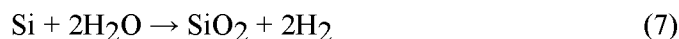
5 After drying the silicon wafer and the oxide-covered wafer are bonded in ambient at room temperature. Reactions (2), (3), (4) and/or (5) take place at the bonding interface between the two wafers. The plasma-treated wafers may also be immersed in deionized water instead of the NH<sub>4</sub>OH solution.

10 The silicon bonding may be conducted with a bare silicon wafer, i.e. having a native oxide or a silicon wafer having an oxide layer formed on its surface as described above. During the oxygen plasma treatment, the native oxide which if formed on the bare silicon wafer is sputter etched, and the oxide layer formed on the silicon surface is etched. The final surface is an activated (native or formed) oxide. When rinsed in deionized water, the activated oxide surface is mainly terminated with Si-OH groups. Since oxide growth in  
15 oxygen plasma has been found to have less water than in normal native oxide layers, the water from the original bonding bridge and generated by the following polymerization reaction (6) can be absorbed into the plasma oxide readily.



FIGS. 5A-5E illustrate bonding two silicon wafers. Wafers 50 and 52 have respective  
20 surfaces 51 and 53 with native oxides (not shown) subjected to a VSE process (FIGS. 5A and 5B). Surface 53 in FIG. 5C is shown terminated with a desired species 54. The two wafers are brought together and bonds 55 begin to form (FIG. 5D). The bonding propagates and bonding by-products, in this case H<sub>2</sub> gas, are removed. The by-products being removed are shown as arrows 56 in FIG. 5E.

25 In addition to removal of the water from the bonding interface by dissolving into the plasma activated oxide of the oxidized silicon wafer, the water can also diffuse through the thin oxide layer on the bare silicon wafer to react with silicon. As the silicon surface underneath the oxide has a damaged or defective zone, extending for a few monolayers, the water molecules that diffuse through the oxide layer and reach the damaged or defective zone  
30 can be converted to hydrogen at room temperature and be removed readily:



The reverse reaction of (6) is thus avoided and the room temperature bonding energy increases enormously due to the formation of covalent Si-O-Si bonds.

If a relatively thick (~5 nm) oxide layer is formed, it will take a long period of time for the water molecules to diffuse through this thick layer. On the other hand, if after the plasma treatment a thin oxide layer is left or a too narrow defective zone is formed, water that can reach the silicon surface may not react sufficiently with the silicon and convert to hydrogen. In both cases the bonding energy enhancement will be limited. The preferred oxygen plasma treatment thus leaves a minimum plasma oxide thickness (e.g., about 0.1-1.0 nm) and a reasonably thick defective zone (e.g., about 0.1-0.3 nm) on the silicon surface.

In a second embodiment, the VSE process uses wet chemicals. For example, an InP wafer having a deposited silicon oxide layer, as in the first embodiment, and a device layer are bonded to a AlN substrate having a deposited oxide layer. After smoothing and planarizing the InP wafer bonding surface and the AlN wafer bonding surface, both wafers are cleaned in an standard RCA cleaning solution. The wafers are very slightly etched using a dilute HF aqueous solution with an HF concentration preferably in the range of 0.01 to 0.2%. About a few tenths of a nm is removed and the surface smoothness is not degraded as determined by AFM (atomic force microscope) measurements. Without deionized water rinse, the wafers are spin dried and bonded in ambient air at room temperature. The resulting bonding energy has been measured to reach ~700 mJ/m<sup>2</sup> after storage in air. After annealing this bonded pair at 75°C the bonding energy of 1500 mJ/m<sup>2</sup> was obtained. The bonding energy has been measured to reach silicon bulk fracture energy (about 2500 mJ/m<sup>2</sup>) after annealing at 100°C. If the wafers are rinsed with deionized water after the HF dip, the bonding energy at 100°C is reduced to 200 mJ/m<sup>2</sup>, that is about one tenth of that obtained without the rinse. This illustrates the preference of F to OH as a terminating species.

In a third embodiment the VSE process consists of 0.1% HF etching followed by 5 min dip in 0.02% HN<sub>4</sub>F solution of thermally oxidized silicon wafers at room temperature after a standard cleaning process. Without rinsing in deionized water, the wafers are bonded after spin drying at room temperature. The bonding energy of the bonded pairs reaches ~1700 mJ/m<sup>2</sup> after 100°C annealing. If the wafers are rinsed in de-ionized water after the HF etching before bonding, the bonding energy of bonded pairs is only 400 mJ/m<sup>2</sup>, again illustrating the preference of F to OH as a terminating species. Dilute NH<sub>4</sub>F is used in the VSE process to etch silicon oxide covered wafers in a fourth embodiment. The concentration

of the  $\text{NH}_4\text{F}$  should be below 0.02% to obtain the desired bonding. The bonding energy of  $\sim 600 \text{ mJ/m}^2$  can be achieved at room temperature after storage.

A fifth embodiment of the invention is used to bond Si surfaces having a native oxide of about 1 nm in thickness. In the fifth embodiment, after cleaning the Si surface by a standard RCA1 cleaning process, a VSE process using 5 min etching in 70%  $\text{HNO}_3$  + diluted HF (preferably 0.01 to 0.02%) is performed. Wafers are pulled out of the solution vertically with a basically hydrophobic surface. Without rinsing in water, the wafers were bonded at room temperature in air. In this process covalent bonding occurs at room temperature with measured bonding energies typically about  $600 \text{ mJ/m}^2$ . This bonding energy is significantly increased to  $1300 \text{ mJ/m}^2$  after annealing at  $75^\circ\text{C}$  and reaches the fracture energy of bulk silicon (about  $2500 \text{ mJ/m}^2$ ) at a temperature of  $100^\circ\text{C}$ .

Instead of 70%  $\text{HNO}_3$ , diluted  $\text{HNO}_3$  with water can be used in the solution to achieve similar results. According to AMF measurements and high resolution transmission electron microscopy measurement results, the silicon is etched in the dilute  $\text{HNO}_3$  VSE process at a rate of 0.1-0.15 nm/min and a new thick oxide 2.5-3.5 nm in thickness is formed.

As further embodiments, the VSE process may consist of a dry etch that has chemical and/or physical components. For a bare Si surface, chemical etching may result from  $\text{SF}_4/\text{H}_2$  gas mixture while physical etching may result from Ar etch. For a silicon oxide surface, chemical etching may use  $\text{CF}_4$  while physical etching may use oxygen or argon gas. It is also possible to use a thermally stable polymer material for the bonding materials and bond two polymer surfaces together. Examples are polyimides or spin-on materials.

The mechanisms governing the increased bond energy at low or room temperature are similar. A very slight etching (VSE) of the bonding wafers by plasma to clean and activate the surfaces, and improve removal of by-products of interface polymerization to prevent the undesirable reverse reaction and rinse in appropriate solution to terminate the surface with desired species to facilitate room temperature covalent bonding. The oxide covered wafer bonding case is similar except that a different surface termination is preferred. In bare silicon wafer bonding, the highly reactive surface layers of oxide and silicon to allow water adsorption and conversion to hydrogen should be formed. The highly reactive layers can be a plasma thin oxide layer and a damaged silicon surface layer. The oxide on the silicon wafer will also have some damage. Not only  $\text{O}_2$  plasma but also plasma of other gases (such as Ar,  $\text{CF}_4$ ) are adequate. Because during and after VSE the silicon surface is readily to react with

moisture to form an oxide layer, and the underlying damaged silicon layer is created by VSE. Since the VSE and by-products removal methods are rather general in nature, this approach can be implemented by many means and apply to many materials.

## 5 EXAMPLE 1

In a first example, three inch <100>, 1-10 ohm-cm, boron doped silicon wafers were used. PECVD oxide was deposited on some of the silicon wafers. For comparison, thermal oxidized silicon wafers were also studied. The PECVD oxide thickness was 0.5 μm and 0.3 μm on the front side and the back side of the wafers, respectively. Oxide is deposited on both  
10 sides of the wafer to minimize wafer bow during polishing and improve planarization. A soft polish was performed to remove about 30 nm of the oxide and to smooth the front oxide surface originally having a root mean square of the micro-roughness (RMS) of ~0.56 nm to a final ~0.18 nm. A modified RCA1 solution was used to clean the wafer surfaces followed by spin-drying.

15 Two wafers were loaded into the plasma system, both wafers are placed on the RF electrode and treated in plasma in RIE mode. For comparison, some wafers were treated in plasma mode in which the wafers were put on the grounded electrode. An oxygen plasma was used with a nominal flow rate of 16 scc/m. The RF power was 20-400 W (typically 80 W) at 13.56 MHz and the vacuum level was 100 mTorr. The oxide covered wafers were  
20 treated in plasma for times between 15 seconds to 5 minutes. The plasma treated silicon wafers were then dipped in an appropriate solution or rinse with de-ionized water followed by spin-drying and room temperature bonding in air. Some of the plasma treated wafers were also directly bonded in air without rinse or dipping.

The bonding energy was measured by inserting a wedge into the interface to measure  
25 the crack length according to the equation:

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4 (E_1 t_{w1}^3 + E_2 t_{w2}^3)}$$

E and tw are the Young's modulus and thickness for wafers one and two and tb is the  
30 thickness of a wedge inserted between the two wafers that results in a wafer separation of length L from the edge of the wafers.

The room temperature bonding energy as a function of storage time of bonded plasma treated oxide covered silicon wafers is shown in FIG. 6A. This figure shows measured room temperature bonding energy versus storage time for 4 different cases as shown. The results can be summarized as follows: (1) for dipped and bonded RIE plasma treated oxide wafers, the room temperature bonding energy increases with storage time and reaches a stable value after ~20 h in air or at low vacuum; (2) RIE mode results in higher bonding energies than plasma mode; (3) too short a plasma exposure time or too low a plasma power provides a small or negligible increase in bond energy; (4) NH<sub>4</sub>OH dip after plasma treatment shows a much higher increase in bonding energy than water rinse; (5) direct bonding in air after plasma treatment without dipping or rinse shows an almost constant bonding energy with time. The bonding energy of the directly bonded wafer pairs immediately after room temperature bonding is slightly higher than the de-ionized water rinsed or NH<sub>4</sub>OH dipped wafer pairs.

FIG. 6B shows room temperature bonding of Si and AlN wafers with PECVD oxide deposited layers. After about 100 h of storage time a bonding energy of over 2000 mJ/m<sup>2</sup> were observed.

Comparing different bonding materials, the bonding energy as a function of storage time of O<sub>2</sub> plasma treated thermally oxidized silicon wafer pairs is similar to wafers with PECVD oxide, although the values of the room temperature bonding energy are somewhat lower.

After ~24 h storage in air at room temperature, the bonding energy as high as ~1000 mJ/m<sup>2</sup> was reached in the RIE mode plasma treated and NH<sub>4</sub>OH dipped PECVD oxide covered wafer pairs. Since the maximum bonding energy of a van der Waals bonded silicon oxide covered wafer pairs is about 200 mJ/m<sup>2</sup>, a large portion of the bonding energy is attributed to the formation of covalent bonds at the bonding interface at room temperature according to the above equation.

### EXAMPLES 2-3

The above process was applied to bond processed InP wafers (600 μm thick) to AlN wafers (380 μm thick), or to bond processed Si (380 μm thick) and InP 600 μm thick) wafers, as second and third examples. The processed InP device wafers are covered with PECVD oxide and planarized and smoothed by chemical-mechanical polishing CMP. A PECVD oxide layer is also deposited on the AlN wafers and is planarized and smoothed to improve

the RMS surface roughness. The processed Si and processed InP wafers are deposited with PECVD oxide and planarized and smoothed using CMP. After VSE similar to the example 1 bonding at room temperature, the bonded wafers are left in ambient air at room temperature.

After 24 hours storage at room temperature, bonding energy of  $1000 \text{ mJ/m}^2$  and  $1100 \text{ mJ/m}^2$  were achieved for the InP/Si and InP/AlN bonded pairs, respectively. For processed Si (380  $\mu\text{m}$  thick) /oxide covered AlN (280  $\mu\text{m}$  thick) wafer pairs, the bonding energy at room temperature as high as  $2500 \text{ mJ/m}^2$  has been achieved. These room temperature bonded plasma treated wafer pairs have sufficient bonding strength to sustain subsequent substrate lapping and etching and other typical semiconductor fabrication processes before or after substrate removal.

The InP substrate in the room temperature bonded InP/AlN pairs was lapped with 1900#  $\text{Al}_2\text{O}_3$  powder from initial 600  $\mu\text{m}$  thick to  $\sim 50 \mu\text{m}$  thick followed by etching in an  $\text{HCl}/\text{H}_3\text{PO}_4$  solution to leave about a 2.0  $\mu\text{m}$  thick InP device layer on the AlN or Si wafer. The water and etching solution did not penetrate into the bonding interface.

Surfaces are sputter etched by energetic particles such as radicals, ions, photons and electrons in the plasma or RIE mode. For example, the  $\text{O}_2$  plasma under conditions that bring about the desired VSE is sputter-etching about 2  $\text{\AA}/\text{min}$  of PECVD oxide as measured by a reflectance spectrometry. For thermal oxide the sputter etching rate is about 0.5  $\text{\AA}/\text{min}$ . The thickness of oxide before and after plasma treatment was measured by a reflectance spectrometry and averaged from 98 measured points on each wafer. The etching by  $\text{O}_2$  plasma has not only cleaned the surface by oxidation and sputtering but also broken bonds of the oxide on the wafer surfaces.

However, the surface roughness of plasma treated oxide surfaces must not be degraded by the etching process. AFM measurements show that compared with the initial surface roughness, the RMS of the  $\text{O}_2$  plasma treated oxide wafers was  $\sim 2 \text{\AA}$  and did not change noticeably. On the other hand, if the etching is not sufficiently strong, the bonding energy enhancement effect is also small. Keeping other conditions unchanged when the  $\text{O}_2$  plasma treatment was performed with plasma mode rather than RIE mode, the etching of oxide surfaces is negligible and the oxide thickness does not change. The final room temperature bonding energy is only  $385 \text{ mJ/m}^2$  compared to  $1000 \text{ mJ/m}^2$  of RIE treated wafers (see FIG. 6A).

Other gas plasma has shown a similar effect.  $\text{CF}_4/\text{O}_2$  RIE was used to remove  $\sim 4 \text{ nm}$  of PECVD oxide from the wafer surfaces prior to bonding. The bonding energy of room

temperature bonded PECVD oxide covered silicon wafers was also enhanced significantly in this manner and exceeds  $1000 \text{ mJ/m}^2$  after sufficient storage time (see also FIG. 6A).

5 An argon plasma has also been used for the VSE with a nominal flow rate of 16 scc/m. The RF power was typically 60 W at 13.56 MHz and the vacuum level was 100 mTorr. The oxide covered silicon wafers were treated in plasma in RIE mode for times between 30 seconds to 2 minutes. The plasma treated silicon wafers were then dipped in an  $\text{NH}_4\text{OH}$  solution followed by spin-drying and room temperature bonding in air. The bonding energy reached  $\sim 800 \text{ mJ/m}^2$  at room temperature after only 8 h storage in air.

10 Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

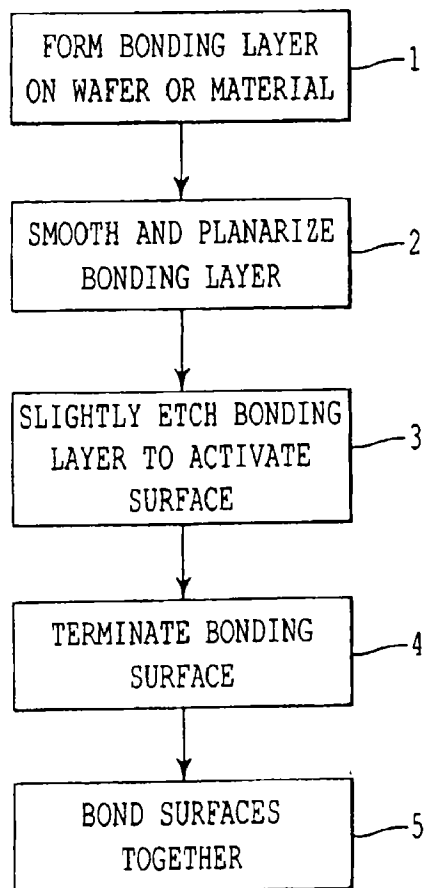


CLAIMS:

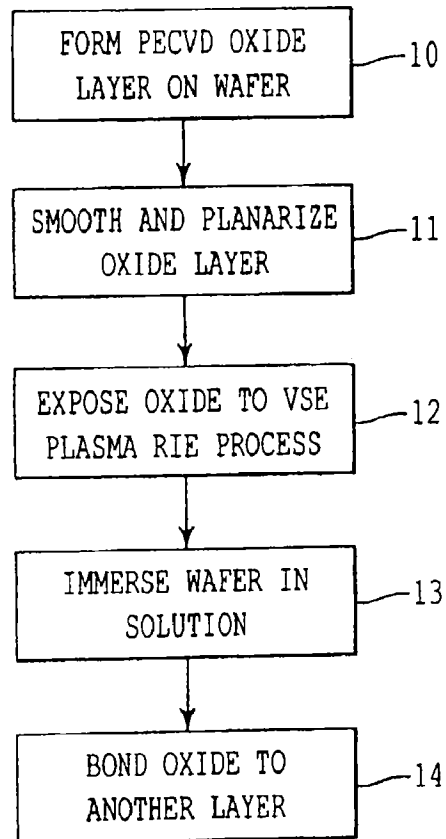
1. A bonding method, comprising:  
forming first and second bonding surfaces;  
etching said first and second bonding surfaces; and  
bonding together at room temperature said first and second bonding surfaces after  
said etching step.

## ABSTRACT OF THE INVENTION

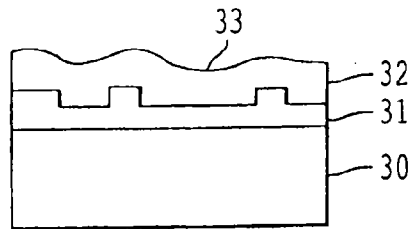
A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO<sub>2</sub>. The surfaces to be bonded are polished to a high degree of smoothness and planarity. VSE may use reactive ion etching or wet etching to slightly etch the surfaces being bonded. The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces.



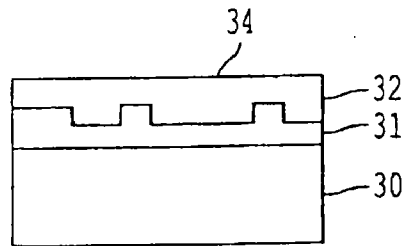
*FIG. 1*



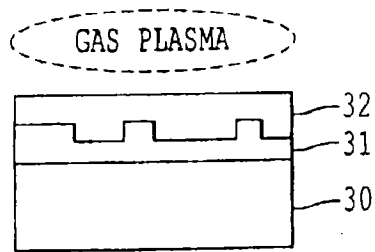
*FIG. 2*



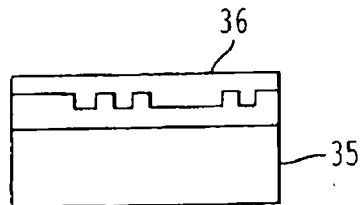
*FIG. 3A*



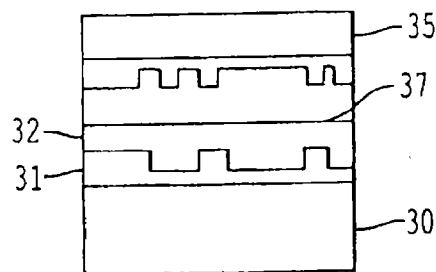
*FIG. 3B*



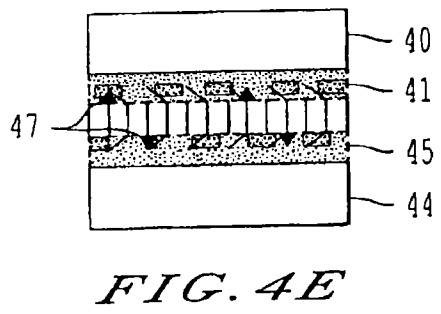
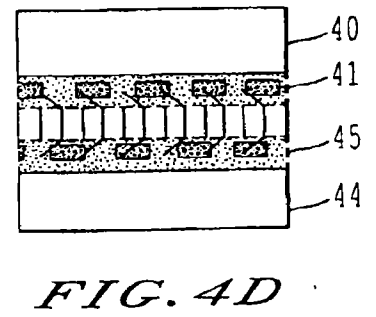
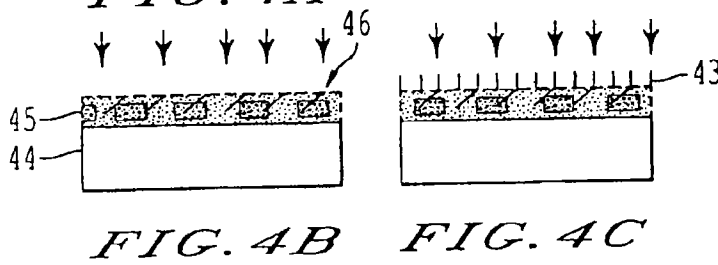
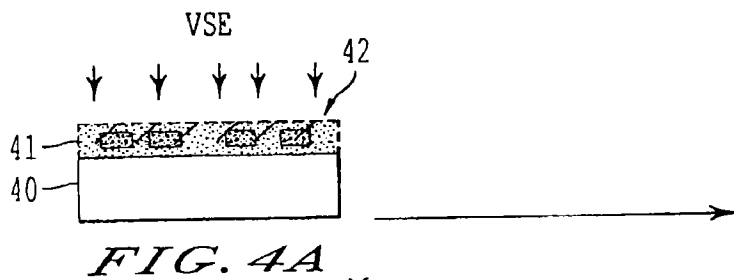
*FIG. 3C*

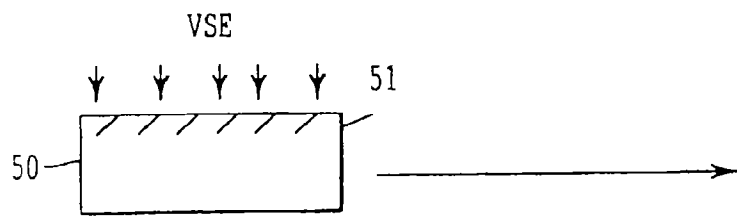


*FIG. 3D*

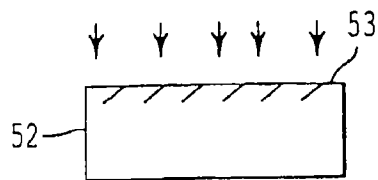


*FIG. 3E*

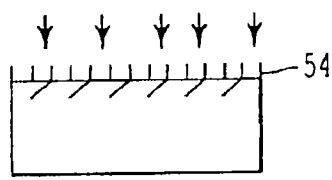




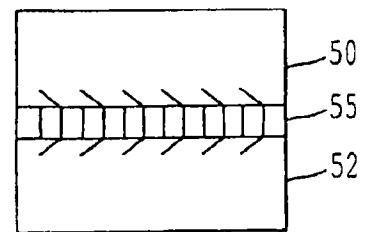
*FIG. 5A*



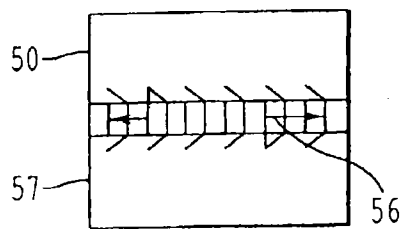
*FIG. 5B*



*FIG. 5C*



*FIG. 5D*



*FIG. 5E*

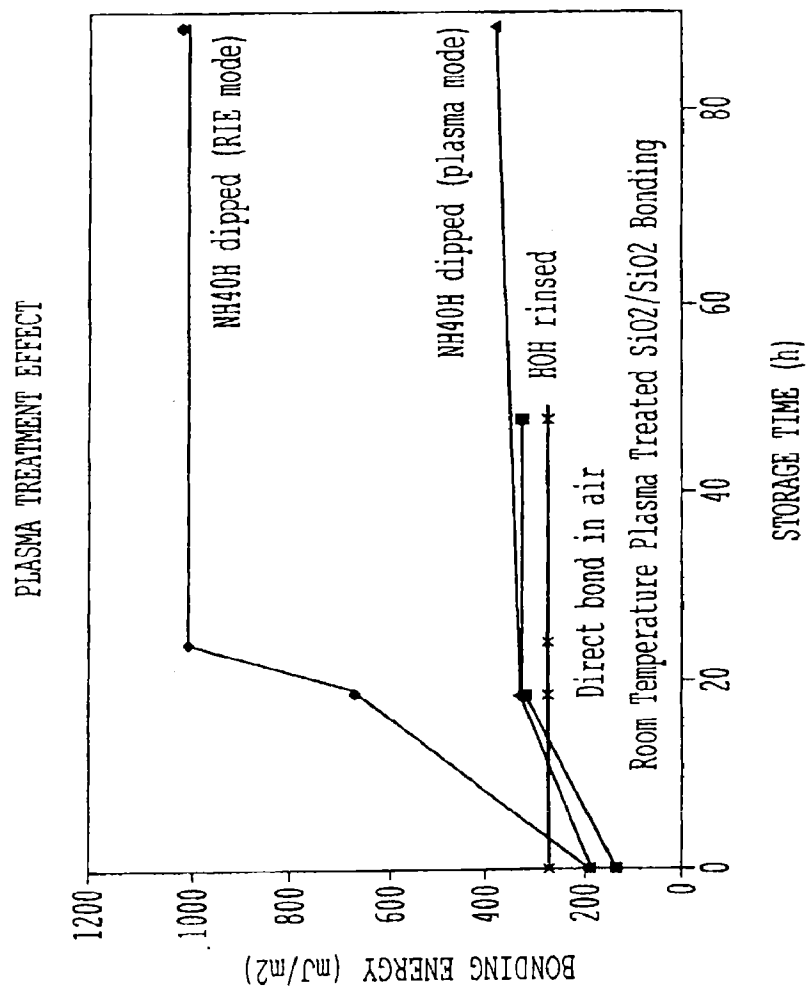


FIG. 6A



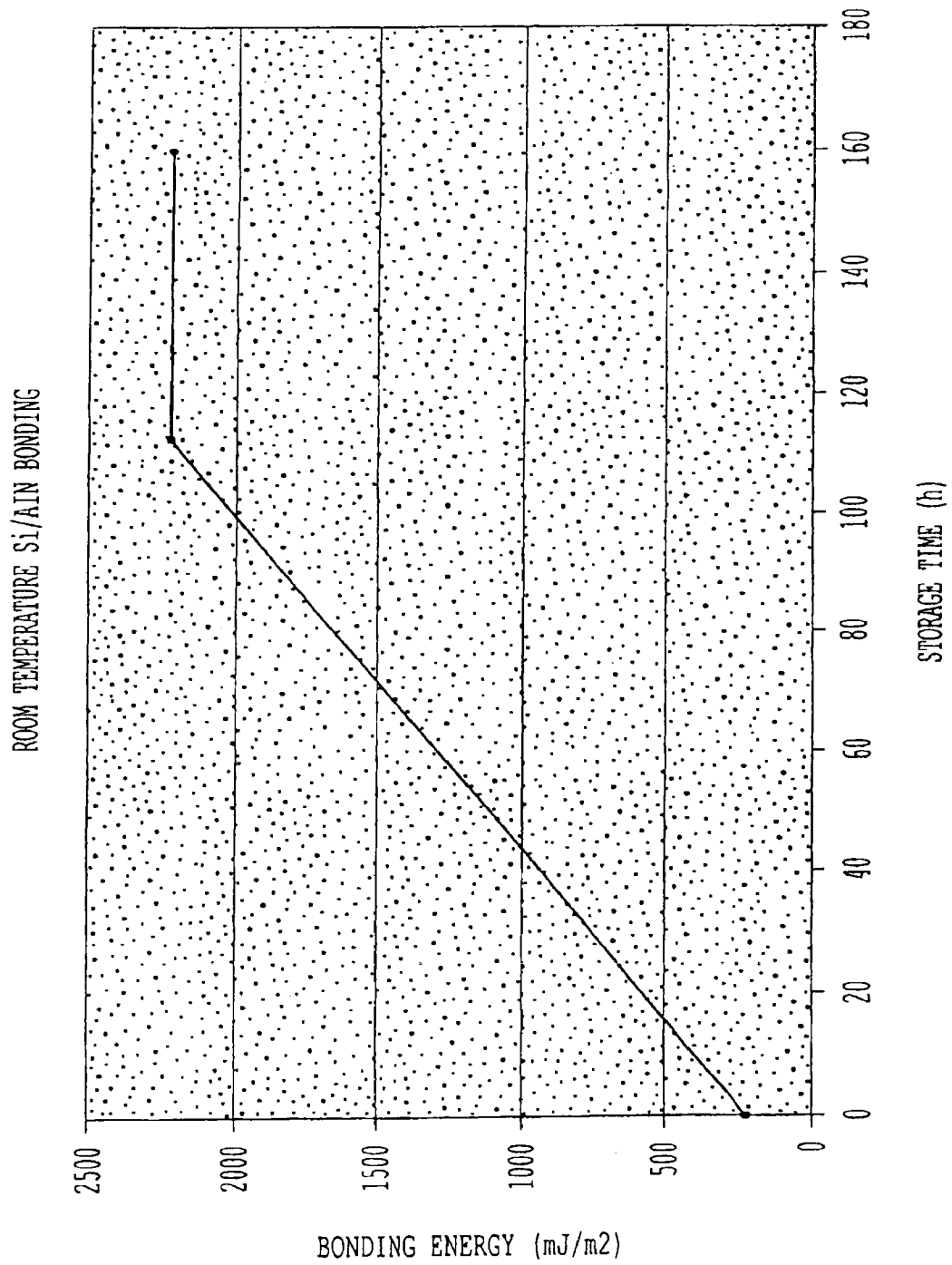
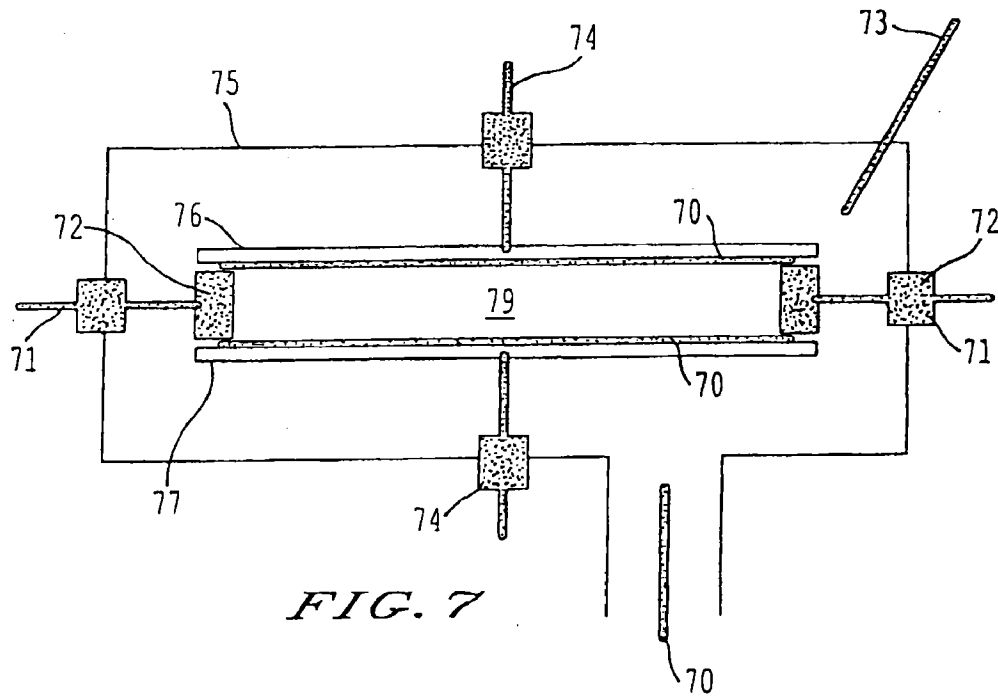
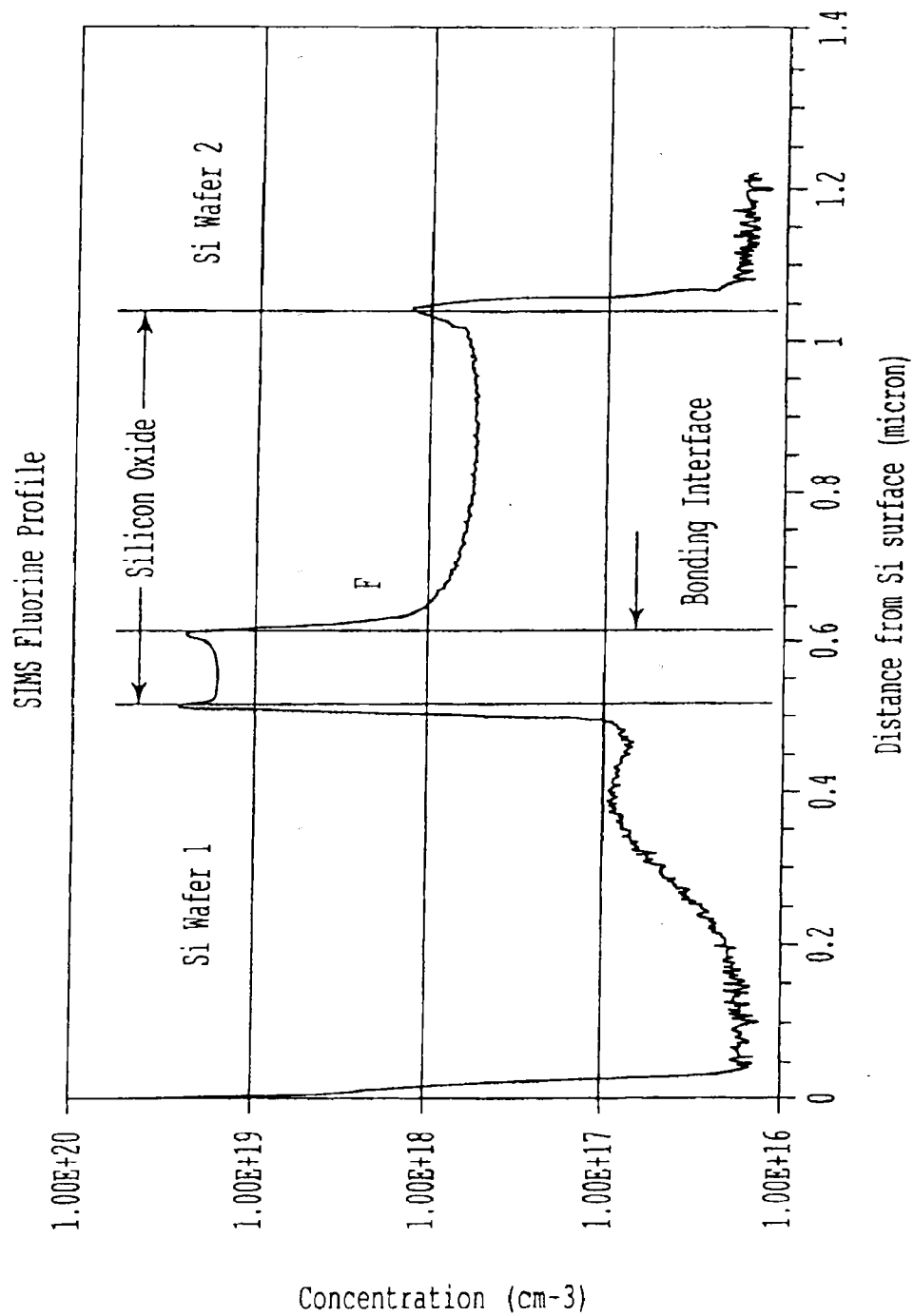


FIG. 6B





*FIG. 8*

**SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY  
OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)**

<b>Title of Invention</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
This statement is directed to:			
<input type="checkbox"/> The attached application,			
OR			
<input checked="" type="checkbox"/> United States application or PCT international application number <u>14/197,070</u> filed on <u>03/04/2014</u> .			
<b>LEGAL NAME of inventor to whom this substitute statement applies:</b>			
(E.g., Given Name (first and middle (if any)) and Family Name or Surname)			
Qin-Yi TONG			
Residence (except for a deceased or legally incapacitated inventor):			
City	State	Country	
Mailing Address (except for a deceased or legally incapacitated inventor):			
City	State	Zip	Country
I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.			
The above-identified application was made or authorized to be made by me.			
I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.			
Relationship to the inventor to whom this substitute statement applies:			
<input type="checkbox"/> Legal Representative (for deceased or legally incapacitated inventor only),			
<input type="checkbox"/> Assignee,			
<input type="checkbox"/> Person to whom the inventor is under an obligation to assign,			
<input type="checkbox"/> Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or			
<input checked="" type="checkbox"/> Joint Inventor.			

## SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☒ Inventor is deceased,  
☐ Inventor is under legal incapacity,  
☐ Inventor cannot be found or reached after diligent effort, or  
☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.


OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

### PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Paul M. ENQUIST  
Name:

4/16/14  
Date (Optional):

Signature: 

### APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer:

Applicant Name:

Title of Person Executing  
This Substitute Statement:

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

Residence of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

Cary  
City

North Carolina  
State

United States  
Country

Mailing Address of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

308 Frenchman's Bluff Drive

4715 Carlton Crossing Drive

Cary  
City

Purhan

North Carolina  
State

27713  
~~27613~~  
Zip

United States  
Country

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)

Title of  
Invention

METHOD FOR LOW TEMPERATURE BONDING AND BONDED  
STRUCTURE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number  
14/197,070 Filed on MARCH 4, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the  
application.

I hereby acknowledge that any willful false statement made in this declaration is punishable  
under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Gaius Gillman FOUNTAIN, Jr.

Date (Optional): 4-16-2014

Signature:

*Gaius Gillman Fountain Jr.*

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.  
Use an additional declaration form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN  
APPLICATION DATA SHEET (37 CFR 1.76)**

<b>Title of Invention</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
-------------------------------	--

As a below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number  
14/197,070 Filed on MARCH 4, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

**LEGAL NAME OF INVENTOR**

Inventor: Paul M. ENQUIST

Date (Optional): 4/16/14

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.  
Use an additional declaration form for each additional inventor.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

**Secrecy Order 37 CFR 5.2:**

<input type="checkbox"/>	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

**Inventor Information:**

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Qin-Yi		Tong		
Residence Information (Select One) <input checked="" type="radio"/> US Residency <input type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					
City	Durham	State/Province	NC	Country of Residence	US

**Mailing Address of Inventor:**

Address 1	3511 Meadowrun Drive				
Address 2					
City	Durham	State/Province	NC		
Postal Code	27707	Country	US		

Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Gaius	Gillman	Fountain	Jr.	
Residence Information (Select One) <input checked="" type="radio"/> US Residency <input type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					
City	Youngsville	State/Province	NC	Country of Residence	US

**Mailing Address of Inventor:**

Address 1	4068 Hugh Davis Road				
Address 2					
City	Youngsville	State/Province	NC		
Postal Code	27596	Country	US		

Inventor	3				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Paul	M.	Enquist		
Residence Information (Select One) <input checked="" type="radio"/> US Residency <input type="radio"/> Non US Residency <input type="radio"/> Active US Military Service					



<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		

City	Cary	State/Province	NC	Country of Residence	US
------	------	----------------	----	----------------------	----

**Mailing Address of Inventor:**

Address 1	4715 Carlton Crossing Drive				
Address 2					
City	Durham	State/Province	NC		
Postal Code	27713	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the <b>Add</b> button.					

**Correspondence Information:**

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
<input type="checkbox"/> An Address is being provided for the correspondence information of this application.			
Customer Number	135980		
Email Address	efiling@knobbe.com	Add Email	Remove Email

**Application Information:**

Title of the Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
Attorney Docket Number	TSSRA.012C1	Small Entity Status Claimed	<input type="checkbox"/>
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	9	Suggested Figure for Publication (if any)	

**Filing By Reference:**

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

**Publication Information:**

<input type="checkbox"/> Request Early Publication (Fee required at time of Request 37 CFR 1.219)
<input type="checkbox"/> <b>Request Not to Publish.</b> I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application <b>has not and will not</b> be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		

## Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	<input checked="" type="radio"/> Customer Number	<input type="radio"/> US Patent Practitioner	<input type="radio"/> Limited Recognition (37 CFR 11.9)
Customer Number	135980		

## Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78. When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending				Remove
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
	Continuation of		14/754111	2015-06-29	
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/754111	Division of	14/197070	2014-03-04	9082627	2015-07-14
Prior Application Status	Abandoned				Remove
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
14/197070	Division of		13/341273	2011-12-30	
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/341273	Continuation of	12/954740	2010-11-26	8153505	2012-04-10
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/954740	Continuation of	12/720368	2010-03-09	7871898	2011-01-18

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number		TSSRA.012C1	
		Application Number			
Title of Invention		METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/720368	Continuation of	11/980664	2007-10-31	7807549	2010-10-05
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/980664	Continuation of	10/913441	2004-08-09	7387944	2008-06-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10/913441	Continuation of	09/505283	2000-02-16	6902987	2005-06-07
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the <b>Add</b> button.					

## Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)<sup>i</sup> the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country <sup>i</sup>	Filing Date (YYYY-MM-DD)	Access Code <sup>i</sup> (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the <b>Add</b> button.			

## Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p>NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
---

<b>Application Data Sheet 37 CFR 1.76</b>	Attorney Docket Number TSSRA.012C1	
	Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE	

## Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

**NOTE:** This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

### 1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

**A. Priority Document Exchange (PDX)** - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

**B. Search Results from U.S. Application to EPO** - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

### 2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

**NOTE:** Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		

## Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

<b>Applicant</b>	1	<a href="#">Remove</a>
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p> <p style="text-align: right;"><a href="#">Clear</a></p>		
<input checked="" type="radio"/> Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
<div style="border: 1px solid black; height: 20px; width: 100%;"></div>		
Name of the Deceased or Legally Incapacitated Inventor: <div style="border: 1px solid black; height: 20px; width: 100%;"></div>		
If the Applicant is an Organization check here. <input checked="" type="checkbox"/>		
Organization Name	ZIPTRONIX, INC.	
<b>Mailing Address Information For Applicant:</b>		
Address 1	800 Perimeter Park Drive	
Address 2	Suite B	
City	Morrisville	State/Province NC
Country	US	Postal Code 27560
Phone Number		Fax Number
Email Address		
Additional Applicant Data may be generated within this form by selecting the Add button. <a href="#">Add</a>		

## Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		

<b>Assignee</b>	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				<input type="button" value="Remove"/>
If the Assignee or Non-Applicant Assignee is an Organization check here.				<input type="checkbox"/>
Prefix	Given Name	Middle Name	Family Name	Suffix
<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
<b>Mailing Address Information For Assignee including Non-Applicant Assignee:</b>				
Address 1		<input type="text"/>		
Address 2		<input type="text"/>		
City	<input type="text"/>	State/Province	<input type="text"/>	
Country <sup>i</sup>	<input type="text"/>	Postal Code	<input type="text"/>	
Phone Number	<input type="text"/>	Fax Number	<input type="text"/>	
Email Address	<input type="text"/>			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				<input type="button" value="Add"/>

**Signature:**

**NOTE:** This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

<b>Signature</b>	/Paul Stellman/		Date (YYYY-MM-DD)	2015-12-02
First Name	Paul	Last Name	Stellman	Registration Number
				68287
Additional Signature may be generated within this form by selecting the Add button.				<input type="button" value="Add"/>

<b>Application Data Sheet 37 CFR 1.76</b>		Attorney Docket Number	TSSRA.012C1
		Application Number	
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

## Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>				
<b>Filing Date:</b>				
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE			
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong			
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan			
<b>Attorney Docket Number:</b>	TSSRA.012C1			
Filed as Large Entity				
<b>Filing Fees for    Utility under 35 USC 111(a)</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1600</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24246561
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Tony Do
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	02-DEC-2015
<b>Filing Date:</b>	
<b>Time Stamp:</b>	20:20:34
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	20724
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2015-12-02_Specification_TSSRA-012C1.pdf	153218 4914a5a4834012191f2fc21c18937e08afb3406	yes	22
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	20	
	Claims		21	21	
	Abstract		22	22	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	2015-12-02_Drawings_TSSRA-012C1.pdf	110488 f44fa9e5ba76ee9796d7b3048803c1b9491ff0bc	no	9
Warnings:					
Information:					
3	Oath or Declaration filed	2015-12-02_Declaration_TSSRA-012C1.pdf	142370 cea2c9f3edf38cff13712c00f26b1f18dcb141dc	no	4
Warnings:					
Information:					
4	Application Data Sheet	2015-12-02_ADS_TSSRA-012C1.pdf	1823736 b7289574b97f38928edf98b24674de618ebd1170	no	9
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	35336 ae119501813900e06fc97377e21470c2f7262405	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2265148		

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875	Application or Docket Number <b>14/957,501</b>	Filing Date <b>12/02/2015</b>	<input type="checkbox"/> To be Mailed
---	---	----------------------------------	---------------------------------------

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

**APPLICATION AS AMENDED – PART II**

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	12/02/2015	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 33	Minus	** 33	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$420 =	0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))						
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

\* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

\*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE  
/KIMBERLY PANNELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor	:	Tong et al.
App. No.	:	14,957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Unknown
Art Unit	:	Unknown
Conf. No.	:	1033

**PRELIMINARY AMENDMENT****Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Prior to examination on the merits, Applicant submits the following amendments.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 6 of this paper.

**AMENDMENTS TO THE CLAIMS**

Please cancel Claim 1 without prejudice or disclaimer. Please add new Claims 2-34.

1. (Canceled)
2. (New) A bonding method, comprising:
  - forming a planarized insulating material on a semiconductor wafer;
  - etching the planarized insulating material in a reaction space;
  - terminating the planarized insulating material with a nitrogen-containing speciesby at least one of:
  - a nitrogen-containing plasma during the etching, and
  - a nitrogen-containing solution after the etching;bringing a first material into direct contact with the terminated and planarized insulating material outside the reaction space; and
  - forming a chemical bond between the terminated and planarized insulating material and the first material.
3. (New) The method of Claim 2, wherein the etching the planarized insulating material is conducted in a vacuum chamber, the reaction space comprising the vacuum chamber.
4. (New) The method of Claim 2, wherein the etching the planarized insulating material is conducted in a plasma chamber, the reaction space comprising the plasma chamber.
5. (New) The method of Claim 2, wherein the etching and the terminating comprise exposing the planarized insulating material to the plasma etching process in a plasma chamber, the reaction space comprising the plasma chamber.
6. (New) The method of Claim 5, wherein the exposing the planarized insulating material to the plasma etching process comprises exposing the planarized insulating material to a reactive ion etching process.
7. (New) The method of Claim 5, wherein the exposing the planarized insulating material to the plasma etching process in the plasma chamber comprises using nitrogen gas.
8. (New) The method of Claim 2, wherein the terminating comprises exposing the planarized insulating material to a nitrogen-containing solution after the etching.
9. (New) The method of Claim 8, wherein the nitrogen-containing solution comprises an ammonia-based solution.



10. (New) The method of Claim 2, wherein the first material comprises a second planarized insulating material on a second semiconductor wafer.

11. (New) The method of Claim 10, wherein the first material comprises silicon oxide.

12. (New) The method of Claim 2, wherein the bringing into direct contact comprises bringing into direct contact the terminated planarized insulating material and a silicon material having a native oxide, the first material comprising the silicon material.

13. (New) The method of Claim 2, further comprising, after the terminating, rinsing the insulating material.

14. (New) The method of Claim 13, wherein the rinsing comprises immersing the insulating material in deionized water.

15. (New) The method of Claim 2, wherein the bringing into direct contact is performed at room temperature.

16. (New) The method of Claim 2, wherein the bringing into direct contact is conducted in air.

17. (New) The method of Claim 2, wherein the forming the planarized insulating material comprises forming silicon oxide on the semiconductor wafer.

18. (New) The method of Claim 2, further comprising forming a bond between the planarized insulating material and the first material with a strength of at least  $500 \text{ mJ/m}^2$  without annealing at more than about  $200^\circ \text{ C}$ .

19. (New) The method of Claim 2, further comprising forming a bond between the planarized insulating material and the first material with a strength of at least  $2000 \text{ mJ/m}^2$  without annealing at more than about  $200^\circ \text{ C}$ .

20. (New) The method of Claim 2, further comprising annealing the planarized insulating material and the first material at a temperature of no more than about  $200^\circ \text{ C}$  after the bringing into direct contact.

21. (New) The method of Claim 2, wherein the planarized insulating material has a surface roughness between about 0.5 and 1.5 nm after the etching and before the bringing into direct contact.

22. (New) A bonded structure comprising:

a first semiconductor material comprising a planarized insulating material having a first bonding surface; and

a second material having a second bonding surface,

wherein the first bonding surface is an etched surface terminated with a nitrogen-containing species, and

wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive.

23. (New) The structure of Claim 22, further comprising at least one integrated circuit in the first semiconductor material.

24. (New) The structure of Claim 22, wherein the second material comprises silicon.

25. (New) The structure of Claim 22, wherein the chemical bond has a strength of at least 500 mJ/m<sup>2</sup>.

26. (New) The structure of Claim 22, wherein the chemical bond has a strength of at least 2000 mJ/m<sup>2</sup>.

27. (New) The structure of Claim 22, wherein the planarized insulating material comprises silicon oxide.

28. (New) The structure of Claim 22, wherein the second bonding surface comprises an etched surface.

29. (New) The structure of Claim 28, wherein the etched surface of the second bonding surface is terminated with a nitrogen-containing species.

30. (New) The structure of Claim 22, wherein the first bonding surface is terminated with a nitrogen-containing species by at least one of a nitrogen-containing plasma during etching and a nitrogen-containing solution after etching.

31. (New) The structure of Claim 22, wherein the chemical bond is a covalent bond.

32. (New) A bonding method, comprising:

forming a planarized insulating material on a semiconductor wafer;

etching the planarized insulating material;

terminating the planarized insulating material with a nitrogen-containing species by at least one of:

a nitrogen-containing plasma during the etching, and

a nitrogen-containing solution after the etching;

bringing a first material into direct contact with the terminated and planarized insulating material; and

forming a chemical bond between the terminated and planarized insulating material and the first material.

33. (New) A bonding method, comprising:

forming a planarized insulating material on a processed semiconductor wafer;

exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas;

terminating the planarized insulating material with a species;

bringing into direct contact the terminated and planarized insulating material and a first material outside of said plasma chamber; and

forming a chemical bond between the terminated and planarized insulating material and the first material.

34. (New) The bonding method of Claim 33, wherein the species comprises nitrogen.

**REMARKS**

Prior to examination on the merits, Applicant has canceled Claim 1 without prejudice or disclaimer. Claims 2-34 are new claims. Support for new Claims 2-34 may be found throughout the Application as filed. No new matter is added. Applicant respectfully requests entry and examination of the claims submitted herewith.

No Disclaimers or Disavowals

Although the present communication may include alterations to the application or claims, Applicant is not conceding in this application that previously pending claims are not patentable. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: December 3, 2015

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22188136  
120315

Electronic Patent Application Fee Transmittal				
Application Number:		14957501		
Filing Date:				
Title of Invention:		METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
First Named Inventor/Applicant Name:		Qin-Yi Tong		
Filer:		Paul Steven Stellman/Jonathan Pan		
Attorney Docket Number:		TSSRA.012C1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	13	80	1040
Independent claims in excess of 3	1201	1	420	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Post-Allowance-and-Post-Issuance:</b>				
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>1460</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24253209
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Heather OBrien
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	03-DEC-2015
<b>Filing Date:</b>	
<b>Time Stamp:</b>	15:53:18
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1460
RAM confirmation Number	2422
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

<b>File Listing:</b>					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2015-12-03_PreliminaryAmendment_TSSRA-012C1.pdf	107322 a2c9f923b2adf98105eff4d03e2417adf6d52c09	yes	6
	<b>Multipart Description/PDF files in .zip description</b>				
	<b>Document Description</b>		<b>Start</b>	<b>End</b>	
	Preliminary Amendment		1	1	
	Claims		2	5	
	Applicant Arguments/Remarks Made in an Amendment		6	6	
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (SB06)	fee-info.pdf	32396 637f62ff6fba759d3c2d23967261295925de4465	no	2
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			139718		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



## POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

135,980

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or  
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

--

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

### SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Paul Davis

Title

Senior Vice President, General Counsel and Secretary, ZIPTRONIX, INC.

**NOTE:** Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24256974
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Gustavo Lopez
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	03-DEC-2015
<b>Filing Date:</b>	
<b>Time Stamp:</b>	17:06:12
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2015-12-03_Rescission_TSSRA-012C1.pdf	64176 19939a07b84e1caab1b12103ad553ad090e373dd	no	1

### Warnings:

Information:

2		2015-12-03_POA_TSSRA-012C1.pdf	246826 0d2e2770c5b94734e48a1aaa16ce4c0d0e6df777	yes	2
	<b>Multipart Description/PDF files in .zip description</b>				
	<b>Document Description</b>		<b>Start</b>	<b>End</b>	
	Transmittal Letter		1	1	
	Power of Attorney		2	2	
<b>Warnings:</b>					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			311002		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  <b>If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</b></p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  <b>If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</b></p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  <b>If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</b></p>					

Please Direct All Correspondence to Customer Number 135,980

---

**RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART**

Inventor	:	Tong et al.
App. No	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Unknown
Art Unit	:	Unknown
Conf #	:	1033

---

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

The claims of the present application are different and possibly broader in scope than the claims pursued in the parent application(s). To the extent any prior amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant hereby rescinds and retracts such disclaimer. Accordingly, the references previously considered in the parent application(s) may need to be re-visited.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Knobbe, Martens, Olson & Bear, LLP

Respectfully submitted,

Dated: December 3, 2015

/Paul Stellman/

Paul Stellman

Registration No. 68,287

Attorney of Record

Customer No. 135,980

(415) 954-4114

22195876//120315

## TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/957,501
Filing Date	December 2, 2015
First Named Inventor	Tong et al.
Title	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	TSSRA.012C1

### SIGNATURE of Applicant or Patent Practitioner

Signature	/Paul Stellman/	Date (Optional)	December 3, 2015
Name	Paul Stellman	Registration Number	68,287
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

**NOTE:** This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



\*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Document code: WFEE

United States Patent and Trademark Office  
Sales Receipt for Accounting Date: 12/11/2015

VVAN11	SALE	#00000036	Mailroom Dt: 12/03/2015	111410	14957501
		01	FC : 1051	140.00	DA



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1

**CONFIRMATION NO. 1033**

135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614



Date Mailed: 12/15/2015

**NOTICE OF ACCEPTANCE OF AUTHORIZATION TO PERMIT  
ACCESS TO APPLICATION VIA PRIORITY DOCUMENT EXCHANGE**

This is in response to the applicant's authorization to permit access to the application-as-filed by participating offices under 37 CFR 1.14(h)(1) submitted on 12/02/2015.

The authorization to permit access to the application under 37 CFR 1.14(h)(1) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/fhadera/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1

**CONFIRMATION NO. 1033**

135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614



Date Mailed: 12/15/2015

**NOTICE OF ACCEPTANCE OF AUTHORIZATION  
TO PERMIT ACCESS TO SEARCH RESULTS**

This is in response to the applicant's authorization to permit access to the search results from the instant application under 37 CFR 1.14(h)(2) submitted on 12/02/2015.

The authorization to permit access to the search results under 37 CFR 1.14(h)(2) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/fhadera/



<b>PATENT APPLICATION FEE DETERMINATION RECORD</b> Substitute for Form PTO-875						Application or Docket Number 14/957,501			
<b>APPLICATION AS FILED - PART I</b>									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(j))	33      minus 20 =	*				x    80    =	1040		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4      minus 3 =	*				x    420   =	420		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	3060		
<b>APPLICATION AS AMENDED - PART II</b>									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus    **	=	x      =	x      =	=		
	Independent (37 CFR 1.16(h))	*	Minus    ***	=	x      =	x      =	=		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus    **	=	x      =	x      =	=		
	Independent (37 CFR 1.16(h))	*	Minus    ***	=	x      =	x      =	=		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1

**CONFIRMATION NO. 1033**

**INFORMAL NOTICE**



135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

Date Mailed: 12/15/2015

**INFORMATIONAL NOTICE TO APPLICANT**

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):  
Qin-Yi Tong
- The substitute statement is signed by a person who is not identified as the applicant under 37 CFR 1.46 in an application data sheet (ADS). Only an applicant under 37 CFR 1.43, 1.45 or 1.46 may execute a substitute statement. See 37 CFR 1.64(a). An application data sheet in compliance with 37 CFR 1.76 identifying the person (i.e., assignee, obligated assignee, or person who otherwise shows sufficient proprietary interest) executing the substitute statement as the applicant, or an inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to the inventor for whom the substitute statement was provided, is required.  
Qin-Yi Tong

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/fhadera/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/957,501	12/02/2015		3200	TSSRA.012C1	33	4

CONFIRMATION NO. 1033

FILING RECEIPT



0000000079347932

135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

Date Mailed: 12/15/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Qin-Yi Tong, Durham, NC;  
Gaius Gillman Fountain JR., Youngsville, NC;  
Paul M. Enquist, Cary, NC;

**Applicant(s)**

ZIPTRONIX, INC., Morrisville, NC;

**Power of Attorney:** The patent practitioners associated with Customer Number 135980

**Domestic Priority data as claimed by applicant**

This application is a CON of 14/754,111 06/29/2015  
which is a DIV of 14/197,070 03/04/2014 PAT 9082627  
which is a DIV of 13/341,273 12/30/2011 ABN  
which is a CON of 12/954,740 11/26/2010 PAT 8153505  
which is a CON of 12/720,368 03/09/2010 PAT 7871898  
which is a CON of 11/980,664 10/31/2007 PAT 7807549  
which is a CON of 10/913,441 08/09/2004 PAT 7387944  
which is a CON of 09/505,283 02/16/2000 PAT 6902987

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

**Permission to Access Application via Priority Document Exchange:** Yes

**Permission to Access Search Results:** Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted:** 12/11/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/957,501**

**Projected Publication Date:** 03/24/2016

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

**Preliminary Class**

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

**LICENSE FOR FOREIGN FILING UNDER**  
**Title 35, United States Code, Section 184**  
**Title 37, Code of Federal Regulations, 5.11 & 5.15**

**GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

---

***SelectUSA***

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 1 OF 5	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number <i>Number - Kind Code (if known)</i> Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	4,700,466	10-20-1987	Nakagawa et al.	
	2	4,983,251	01-08-1991	Haisma et al.	
	3	5,427,638	06-27-1995	Goetz et al.	
	4	5,451,547	09-19-1995	Himi et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document <i>Country Code-Number-Kind Code</i> Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	5	CA 2 399 282 A1	08-23-2001	Ziptronix, Inc.		
	6	JP H08-195334	07-30-1996	Canon Inc.		T
	7	TW 389965B	05-11-2000	San Fu Chemical Co. Ltd.		T

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	8	ABE et al., "Bonded SOI wafers with various substrates for IC fabrication," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 32-42.	
	9	AMIRFEIZ et al., "Formation of silicon structures by plasma-activated wafer bonding," Journal of The Electrochemical Society, 2000, Vol. 147, No. 7, pp. 2693-2698.	
	10	ARNOLD, Emil, "Silicon-on-insulator devices for high voltage and power IC applications," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 161-175.	
	11	BEITMAN et al., "Bonded SOI in a bipolar IC without trench isolation," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 144-151.	
	12	BOOTH et al., "Full three dimensional microcircuit integration techniques using wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 293-302.	
	13	BRUGGER et al., "High-precision aligned silicon wafer bonding for a micromachined AFM sensor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 363-372.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 2 OF 5	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	14	CHA et al., "Design considerations for wafer bonding of dissimilar materials," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 257-266.	
	15	CHRISTEL et al., "Silicon fusion bonding: An important tool for the design of micromechanical silicon devices," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 327-339.	
	16	CIARLO, D., "High - and low - temperature bonding techniques for microstructures," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 313-326.	
	17	DESMOND et al., "The effects of process-induced defects on the chemical selectivity of highly-doped boron etchstops," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 423-432.	
	18	EDA et al., "Quartz crystal on silicon technique using direct bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 373-381.	
	19	ESASHI, "Complex micromechanical structures by low temperature bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 348-362.	
	20	FARRENS et al., "Analysis of bond characteristics in Si direct-bonded materials," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 81-95.	
	21	FARRENS et al., "Chemical free room temperature wafer to wafer direct bonding," J. Electrochem. Soc., The Electrochemical Society, Inc., November 1995, Vol. 142, No. 11. pp. 3949-3955.	
	22	FARRENS et al., "Chemical free wafer bonding of silicon to glass and sapphire," Electrochemical Society Proceedings Volume 95-7, 1995, pp. 72-77.	
	23	FEIJÓO et al, "BE-SOI with etch stop layers grown by RTCVD," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 267-279.	
	24	FEINDT et al., "A complementary bipolar process on bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 189-196.	
	25	First Office Action (English translation) mailed October 6, 2015, issued in Japanese Patent Application No. 2012-107053, 7 pages.	
	26	FOLTA et al., "Low-temperature wafer bonding of surfaces using a reactive sputtered oxide," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 107-113.	
	27	GAN, Qing, "Surface activation enhanced low temperature silicon wafer bonding," Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, Department of Mechanical Engineering and Materials Science, Duke University, August 4, 2000, 192 pages.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 3 OF 5	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	28	GAROFALINI, Stephen H., "Atomistic structure and dynamic behavior of silica surfaces," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 57-70.	
	29	GASSEL et al., "SIMOX and wafer bonding: Combination of competitors complements one another," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 433-442.	
	30	GÖSELE et al., "SEMICONDUCTOR WAFER BONDING: A flexible approach to materials combinations in microelectronics; micromechanics and optoelectronics," IEEE, 1997, pp. 23-32.	
	31	GÖSELE et al., "Silicon layer transfer by wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 395-409.	
	32	HARENDT et al., "Bonded-wafer SOI smart power circuits in automotive applications," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 129-143.	
	33	HORNING et al., "Wafer-to-wafer bond characterization by defect decoration etching," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 199-206.	
	34	HUGHES, Donald L., "Silicon-silicon direct wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 17-31.	
	35	IYER et al., "Ultra thin silicon-on insulator using epitaxial etch stops," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 3-16.	
	36	JIAO et al., "Silicon direct bonding at low temperature near the boiling point of water," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 280-282.	
	37	KAWAI et al., "Structure of the interface of a bonded wafer," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 216-224.	
	38	LING et al., "Influence of bonding temperature on the electrical properties of Si/SiO <sub>2</sub> interfaces in bonded silicon-on-insulator-wafers" Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 453-462.	
	39	LJUNGBERG et al., "Buried silicide layers in silicon using wafer bonding with cobalt as interfacial layer," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 249-256.	
	40	LJUNGBERG et al., "Spontaneity of hydrophobic Si-Si bonding and properties of the bonded interfaces," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 473-482.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 4 OF 5	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	41	MACARY et al, "Influence of the wafer cleaning on the electrical properties of Si-Si bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 463-472.	
	42	MCLACHLAN et al., "A bonded wafer bipolar process in manufacturing," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 43-54.	
	43	MITANI et al, "Investigation of the N-type inversion layer induced at the bottom of P-type active silicon layers in bonded SOI wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 443-452.	
	44	MUMOLA et al., "Plasma-thinned silicon-on-insulator bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 410-422.	
	45	NAKANISHI et al., "Studies on SiO <sub>2</sub> -SiO <sub>2</sub> bonding with hydrofluoric acid --- room temperature and low stress bonding technique for MEMS ---" 1998 IEEE, pp. 609-614.	
	46	NISHIZAWA et al., "An advanced dielectric isolation structure for SOI-CMOS/BiCMOS VLSIs," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 176-188.	
	47	REICHE et al., "Characterization of interfaces of directly bonded silicon wafers: A comparative study of secondary ion mass spectroscopy multiple internal reflection spectroscopy, and transmission electron microscopy," Jpn. J. Appl. Phys., Vol. 35 (1996), pp. 2102-2107, Part 1, No. 4A, April 1996.	
	48	REICHE et al., "The effect of a plasma pretreatment on the Si/Si bonding behaviour," Electrochemical Society Proceedings, 1998, Vol. 97-36, pp. 437-444.	
	49	ROBB et al., "High temperature lateral dopant diffusion in WSi <sub>2</sub> , TiSi <sub>2</sub> and TiN films," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society, Proceedings Vol. 93-29 (1993), pp. 230-239.	
	50	ROBERDS et al., "Low temperature, in situ, plasma activated wafer bonding," Electrochemical Society Proceedings, 1997, Vol. 97-36, pp. 598-606.	
	51	ROBERDS et al., "Low temperature silicon direct bonding," Department of Mechanical, Aeronautical, and Materials Engineering, University of California, Davis, 1997, pp. 240-248.	
	52	ROUSE et al, "Application of 150 mm bonded wafer technology to a power asic process," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 283-292.	
	53	SAITOH et al., "Characterization of directly bonded silicon-on-insulator structures using spectroscopic ellipsometry," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 207-215.	
	54	SAKAKIBARA et al., "A wafer bonded - SOI bipolar transistor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 152-160.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 5 OF 5	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	55	SHAJII et al., "A backside contact technology for a wafer-bonded liquid shear-stress sensor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 340-347.	
	56	SÖDERBÄRG et al., "Formation of heat sinks using bonding and etch back technique in combination with diamond deposition," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 382-391.	
	57	SOORIAKUMAR et al., "Thermal mismatch strain in anodically bonded silicon and glass," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 225-229.	
	58	STANLEY, Timothy, "Revenue sensitivity to yield and starting wafer cost in SOI SRAM production," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 303-309.	
	59	SUGA, T., "Room-temperature bonding on metals and ceramics," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 71-80.	
	60	TONG et al., "A "smarter-cut" approach to low temperature silicon layer transfer," Appl. Phys. Lett. January 5, 1998, Vol. 72, No. 1, pp. 49-51.	
	61	TONG et al., "Hydrophobic silicon wafer bonding," Appl. Phys. Lett., January 31, 1994, Vol. 64, No. 5, pp. 625-627.	
	62	TONG et al., "Low temperature InP layer transfer," Electronics Letters, February 18, 1999, Vol. 35, No. 4, pp. 341-342.	
	63	TONG et al., "Low temperature wafer direct bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 96-106.	
	64	TONG et al., "Wafer bonding and layer splitting for microsystems**," Advanced Materials, 1999, Vol. 11, No. 17, pp. 1409-1425.	
	65	WELDON et al., "Physics and chemistry of silicon wafer bonding investigated by infrared absorption spectroscopy," Journal of Vacuum Science & Technology B, July/August 1996, Vol. 14, No. 4, pp. 3095-3106.	
	66	YALLUP, Kevin, "Analog CMOS circuits on thick film SOI," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 117-128.	

22415270  
010716

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

(12)

(21) 2 399 282

(22) 15.02.2001

(51) Int. Cl. 7: **H01L 21/48**

(85) 05.08.2002

(86) PCT/US01/03683

(87) WO01/061743

(30) 09/505,283 US 16.02.2000

(71) ZIPTRONIX, INC.,  
Herbert 147  
Cornwallis Road 3040, RESEARCH TRIANGLE  
PARK, XX (US).

(72) TONG, QIN-YI (US).  
FOUNTAIN, GAIUS GILLMAN JR. (US).  
ENQUIST, PAUL M. (US).

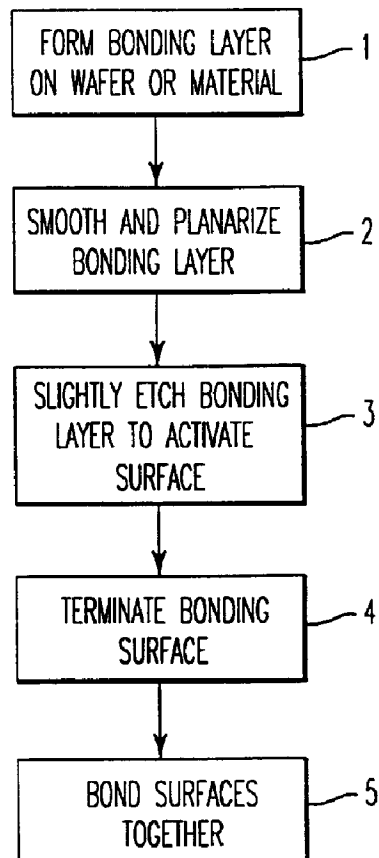
(74) OGILVY RENAULT

(54) PROCEDE DE LIAISON BASSE TEMPERATURE ET STRUCTURE LIEE

(54) METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

(57)

A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO<sub>2</sub>. The surfaces to be bonded are polished to a high degree of smoothness and planarity (2). VSE may use reactive ion etching or wet etching to slightly etch the surfaces being bonded (3). The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces (4).

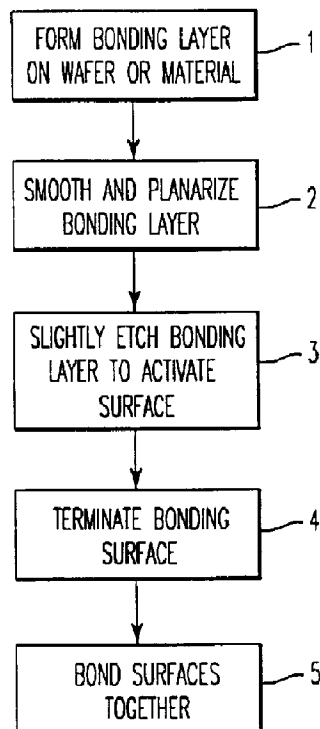




(86) Date de dépôt PCT/PCT Filing Date: 2001/02/15  
(87) Date publication PCT/PCT Publication Date: 2001/08/23  
(85) Entrée phase nationale/National Entry: 2002/08/05  
(86) N° demande PCT/PCT Application No.: US 2001/003683  
(87) N° publication PCT/PCT Publication No.: 2001/061743  
(30) Priorité/Priority: 2000/02/16 (09/505,283) US

(51) Cl.Int.<sup>7</sup>/Int.Cl.<sup>7</sup> H01L 21/48  
(71) Demandeur/Applicant:  
ZIPTRONIX, INC., US  
(72) Inventeurs/Inventors:  
TONG, QIN-YI, US;  
FOUNTAIN, GAIUS GILLMAN JR., US;  
ENQUIST, PAUL M., US  
(74) Agent: OGILVY RENAULT

(54) Titre : PROCEDE DE LIAISON BASSE TEMPERATURE ET STRUCTURE LIEE  
(54) Title: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE



(57) **Abrégé/Abstract:**

A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO<sub>2</sub>. The surfaces to be bonded are



(57) **Abrégé(suite)/Abstract(continued):**

polished to a high degree of smoothness and planarity (2). VSE may use reactive ion etching or wet etching to slightly etch the surfaces being bonded (3). The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces (4).

## (12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
23 August 2001 (23.08.2001)

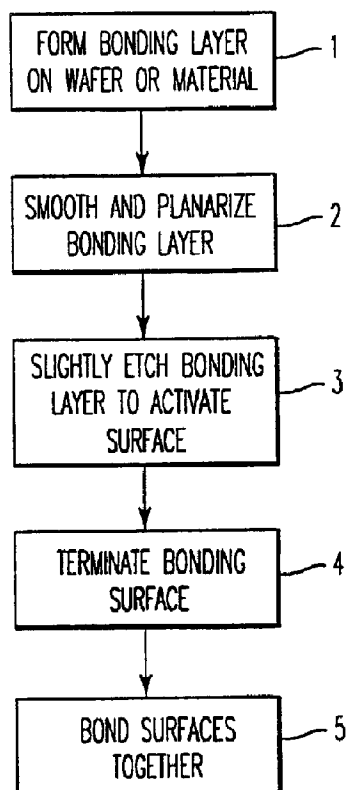
PCT

(10) International Publication Number  
**WO 01/61743 A1**

- (51) International Patent Classification<sup>7</sup>: **H01L 21/48**
- (21) International Application Number: **PCT/US01/03683**
- (22) International Filing Date: 15 February 2001 (15.02.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
09/505,283 16 February 2000 (16.02.2000) US
- (71) Applicant: **RESEARCH TRIANGLE INSTITUTE**  
[US/US]: 3040 Cornwallis Road, Research Triangle Park,  
NC 27709 (US).
- (72) Inventors: **TONG, Qin-Yi**, 3511 Meadowrun Drive,  
Durham, NC 27707 (US). **FOUNTAIN, Gaius, Gillman**,
- Jr.; 4068 Hugh Davis Road, Youngsville, NC 27596 (US).  
**ENQUIST, Paul, M.**; 308 Frenchmans Bluff Drive, Cary,  
NC 27513 (US).
- (74) Agents: **KUESTERS, Eckhard, H.** et al.; Oblon, Spivak,  
McClelland, Maier & Neustadt, P.C., 4th floor, 1755 Jef-  
ferson Davis Highway, Arlington, VA 22202 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU,  
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ,  
DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR,  
HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR,  
LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ,  
NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM,  
TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM,  
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian  
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European

[Continued on next page]

(54) Title: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE



(57) Abstract: A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO<sub>2</sub>. The surfaces to be bonded are polished to a high degree of smoothness and planarity (2). VSE may use reactive ion etching or wet etching to slightly etch the surfaces being bonded (3). The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces (4).

WO 01/61743 A1

## Method For Low Temperature Bonding And Bonded Structure

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to bonding of materials at room temperature and, in particular, to bonding of processed semiconductor materials, such as integrated circuit or device substrates, having activated surfaces to achieve high bonding strength adequate for subsequent fabrication and/or a desired application.

#### 2. Background of the Invention

Direct room temperature bonding generally produces weak van der Waals or hydrogen bonding. Annealing is typically required to convert the weak bond to a stronger chemical bond such as a covalent bond. Other wafer bonding techniques including anodic and fusion typically require the application of voltage, pressure and/or annealing at elevated temperature to achieve a sufficient bond strength for subsequent fabrication and/or the desired application. The need to apply voltage, pressure or heat has significantly limited wafer bonding applications because these parameters can damage the materials being wafer bonded, give rise to internal stress and introduce undesirable changes in the devices or materials being bonded. Achieving a strong bond at low temperatures is also critical for bonding of thermally mismatched or thermally sensitive wafers including processed device wafers.

Ultra high vacuum (UHV) bonding is one of the approaches to achieve a low or room temperature strong bond. However, the bonding wafers still have to be pre-annealed at high temperatures, for instance  $>600^{\circ}\text{C}$  for silicon and  $500^{\circ}\text{C}$  for GaAs, before cooling down to low or room temperature for bonding. Furthermore, the UHV approach does not generally work on commonly used materials, for example, in  $\text{SiO}_2$ . It is further also expensive and inefficient.

Adhesive layers can also be used to bond device wafers to a variety of substrates and to transfer device layers at low temperatures. However, thermal and chemical instability, interface bubbles, stress and the inhomogeneous nature of adhesive layers prevent its wide application. It is thus highly desirable to achieve a strong bond at room temperature by bonding wafers in ambient without any adhesive, external pressure or applied electric field.

Low vacuum bonding has been explored as a more convenient alternative to UHV bonding but a bonding energy comparable to the bulk silicon fracture energy using bonded



bare silicon wafer pairs has only be achieved after annealing at  $\sim 150^{\circ}\text{C}$ . For oxide covered silicon wafer pairs annealing at  $\sim 300^{\circ}\text{C}$  is required to obtain a high bond energy. It has not been possible to obtain high bonding energies in bonded material using low vacuum bonding at room temperature.

A gas plasma treatment prior to bonding in ambient is known to enhance the bonding energy of bonded silicon pairs at low or room temperature. See, for example, G.L. Sun, Q.-Y. Tong, et al., J. de Physique, 49(C4), 79 (1988); G.G. Goetz, Proc.of 1st Intl. Symp. on Semicond. Wafer Bonding: Science, Technol. and Applications, The Electrochem. Soc., 92-7, 65 (1992); S. Farrens et al., J. Electroch. Soc., 142,3950 (1995) and Amirffeiz et al, Abstracts of 5th Intl. Symp. on Semi. Wafer Bonding: Science, Tech. and Appl., The Electrochemical Society, 99-2, Abstract No. 963 (1999). Although these treatments have increased the bond energy obtainable at low or room temperature, they have only been demonstrated with planar silicon wafers or with silicon wafers using a plasma process that results in oxide being grown on the wafers during the plasma process. Moreover, these treatments have only been used to increase the bond energy by charging or damaging the surface. Furthermore, these treatments have not been used or shown to be applicable to deposited dielectrics or other materials.

Obtaining low or room temperature bonding with a method that is not only applicable to planar silicon and grown oxide surfaces but further to deposited materials and non-planar surfaces with planarized deposited materials will allow generic materials, including processed semiconductor wafers, to be bonded with minimal damage for manufacturing purposes. Such a method based on etching and chemical bonding is described herein.

#### SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for bonding materials at low or room temperature.

It is another object of the invention to bond materials by cleaning and activating the bonding surfaces to promote chemical bond formation at about room temperature.

It is a further object of the invention to provide a bonding method to bond any solid state material such as processed device or integrated circuit wafers or thermally sensitive or mis-matched materials at or about room temperature.

It is further object of the invention to provide a bonding method to bond processed

device or integrated circuit wafers of different types of devices or different technologies, and transfer a layer of devices or circuits at or about room temperature.

It is another object of the invention to enable a direct wafer bonding method that does not require annealing to achieve a required bond strength.

It is a further object of the invention to provide a method whereby diverse materials including those with non-planar surfaces and deposited materials can be planarized and bonded.

These and other objects are achieved by a method of bonding having steps of forming first and second bonding surfaces, etching the first and second bonding surfaces, and bonding together at room temperature the first and second bonding surfaces after said etching step. The etching may include etching the first and second bonding surfaces such that respective surface roughnesses of the first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching. The surface roughness may be in a range of 0.1 to 3.0 nm.

The bonding surfaces may be the surface of a deposited insulating material, such as silicon oxide, silicon nitride or a dielectric polymer. The bonding surface may also be the surface of a silicon wafer. Silicon wafers, using either the surface of the wafer or a deposited material on the wafer, may be bonded together. The wafers may have devices or integrated circuits formed therein. The devices and circuits in the wafers bonded together may be interconnected. The wafers may have a non-planar surface or an irregular surface topology upon which a material is deposited to form the bonding surfaces.

Forming at least one of the bonding surfaces may include depositing a polishable material on a non-planar surface. Depositing said polishable material may include depositing one of silicon oxide, silicon nitride or a dielectric polymer. The bonding surfaces may be polished using a method such as chemical-mechanical polishing. The surfaces may also be etched prior to the polishing.

The etching step may also include activating the first and second bonding surfaces and forming selected bonding groups on the first and second bonding surfaces. Bonding groups may also be formed capable of forming chemical bonds at approximately room temperature, and chemical bonds may be formed between the bonding surfaces allowing bonded groups to diffuse or dissociate away from an interface of the bonding surfaces. The chemical bonds can

increase the bonding strength between the bonding surfaces by diffusing or dissociating away said bonding groups.

After said etching step, the bonding surfaces may be immersed in a solution to form bonding surfaces terminated with desired species. The species may comprise at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group. Also, a monolayer of one of a desired atom and a desired molecule may be formed on the bonding surface. Terminating the surface may include rinsing said bonding materials in an ammonia-based solution after said slightly etching. The ammonia-based solution may be ammonium hydroxide or ammonium fluoride.

The method may also include exposing the bonding surfaces to one of an oxygen, argon,  $\text{NH}_3$  and  $\text{CF}_4$  RIE plasma process. Silicon dioxide may be deposited as to form the bonding surfaces, and etched using the RIE process.

The etching process may create a defective or damaged zone proximate to the bonding surfaces. The defective or damaged zone can facilitate the removal of bonding by-products through diffusion or dissociation.

The method may also include steps of forming first and second bonding surfaces, etching the bonding surfaces, terminating the bonding surfaces with a species allowing formation of chemical bonds at about room temperature, and bonding the bonding surfaces at about room temperature, or may include steps of forming the bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm, removing material from the bonding surfaces while maintaining said surface roughness, and directly bonding the bonding surfaces at room temperature with a bonding strength of at least  $500 \text{ mJ/m}^2$ , at least  $1000 \text{ mJ/m}^2$ , or at least  $2000 \text{ mJ/m}^2$ .

The objects of the invention may also be achieved by a bonded device having a first material having a first etched bonding surface, and a second material having a second etched bonding surface directly bonded to the first bonding surface at room temperature having a bonding strength of at least 500 to  $2000 \text{ mJ/m}^2$ . The bonding surfaces may be being activated and terminated with a desired bonding species, and the desired species may include a monolayer of one of a desired atom and a desired molecule on said bonding surface or at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group. The bonding surfaces may each have a defective region located proximate to said first and second bonding

surfaces, respectively.

The first material may include a surface of a first semiconductor wafer having devices formed therein, and the second material may include a surface of a second semiconductor wafer having devices formed therein. Devices in the wafers may be interconnected, and the wafers may be of different technologies. The wafers may also have an integrated circuit formed therein, and devices or circuits in the wafers may be interconnected.

One of said first and second wafers may be a device region after removing a substantial portion of a substrate of said one of said first and second wafers. The wafers may have an irregular surface topology.

The first material may include a first wafer containing electrical devices and having a first non-planar surface, and the first bonding surface may include a polished and etched deposited oxide layer on said first non-planar surface. The second material may include a second wafer containing electrical devices and having a second non-planar surface, and the second bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the second non-planar surface.

The first material may include a first wafer containing electrical devices and having a first surface with irregular topology, and the first bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the first surface. The second material may include a second wafer containing electrical devices and having a second surface with irregular topology, and the second bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the second surface.

The bonded device according to the invention may also include a first material having a first etched and activated bonding surface terminated with a first desired bonding species, and a second material having a second etched and activated bonding surface terminated with a second desired bonding species bonded to the first bonding surface at room temperature.

#### BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof are readily obtained as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart of the method according to the invention;

FIG. 2 is a flow chart of an example of the method according to the invention;

FIGS. 3A-3E are diagrams illustrating a first embodiment of a method according to the invention;

FIG. 4 is a diagram illustrating bonding according to the invention using silicon oxide;

FIG. 5 is a diagram illustrating bonding according to the invention using silicon;

FIGS. 6A and 6B are graphs of room temperature bonding energy versus storage time;

FIG. 7 is a diagram of a bonding fixture used in the invention; and

FIG. 8 is a fluorine concentration profile by SIMS (Secondary Ion Mass Spectroscopy) near the bonding interface of deposited oxide covered silicon wafers that were very slight etched by diluted HF before bonding.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. 1 and 3A-3E, a first embodiment of the method according to the invention will be described. Wafer 30, preferably a processed semiconductor device wafer and more preferably a processed silicon device wafer, contains a device layer 31 with processed devices. Device layer 31 may contain a number of layers and include surface regions of wafer 30. The surface topography of layer 31 is typically nonplanar. Layer 31 may also represent a processed integrated circuit containing any number of layers such as active devices, interconnection, insulation, etc.

The integrated circuit may be fully processed, or partially processed where the remaining processing is performed after the bonding process. The processing after the bonding may include full or partial substrate removal or via formation between the bonded wafers for interconnection.

On layer 31 a bonding layer 32 is formed (step 1, FIG. 1). Bonding layer 32 may be any solid state material or mixed materials which can be deposited or formed at low temperatures and can be polished to a sufficiently smooth surface. Layer 32 may be an insulator, such as SiO<sub>2</sub>, silicon nitride, amorphous silicon formed using chemical vapor deposition (CVD) or plasma-enhanced CVD (PECVD), sputtering or by evaporation. Other materials such as polymers, semiconductors or sintered materials may also be used. Layer 32

should have thickness greater than the surface topography of layer 31.

The surface 33 of layer 32 is planarized and smoothed, as shown in step 2 of FIG. 1 and in FIG. 3B. It is noted that the roughness/planarity of surface 33 is exaggerated in FIG. 3A for illustrative purposes. This step may be accomplished using chemical-mechanical polishing. Surface 33 is preferably polished to a roughness of about no more than about 3 nm and preferably no more than about 0.1 nm and be substantially planar. The surface roughness values are typically given as root-mean square (RMS) values. Also, the surface roughness may be given as mean values which are nearly the same as the RMS values. After polishing surface 33 is cleaned and dried to remove any residue from the polishing step. Polished surface 33 is preferably then rinsed with a solution.

The bonding surface may also be etched prior to polishing to improve the planarity and/or surface roughness. The etching can be effective to remove high spots on the bonding surface by selective etching of the high spots using, for example, standard photolithographic techniques. For example, a layer of silicon nitride can be embedded within a silicon dioxide bonding layer 32 that can serve as an etch stop when using a solution containing HF. The etch stop material may be used to improve uniformity, reproducibility, and manufacturability.

FIG. 3B illustrates layer 32 having upper surface 34 after the polishing/planarization and cleaning steps. Surface 34 then undergoes an activation process (step 3, FIG. 1). This activation process is an etching process and preferably a very slight etch (VSE) process. The term VSE means that the root-mean-square micro-roughness (RMS) of the very slightly etched surface remains at approximately the unetched value, typically  $< 0.5$  nm and preferably in the range of 0.1 nm to 3 nm. The optimum amount of material removed depends upon the material and the method used for removal. Typical amounts removed vary from Angstroms to a few nanometers. It is also possible to remove more material. VSE also includes the breaking of bonds on the treated surfaces and can occur without significant removal of material. The VSE is distinct from simple modification of the surface by, for example, charging the surface with electronic charge or damaging the surface layer. In a first example of the method according to the invention, the VSE process consists of a gas or mixed gas (such as oxygen, argon, nitrogen,  $\text{CF}_4$ ,  $\text{NH}_3$ ) plasma process at a specified power level for a specified time (FIG. 3C). The power and duration of the plasma process will vary depending upon the materials used to obtain the desired bond energy. Examples are given

below, but in general, the power and duration will be determined empirically.

The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used. Data and examples are given below in both the RIE and plasma modes.

The VSE process etches the surface very slightly via physical sputtering and/or chemical reaction and preferably is controlled to not degrade the surface roughness of the bonding surfaces. The surface roughness may even be improved depending upon the VSE and materials etched. Almost any gas or gas mixture that will not etch surface 34 excessively can be used for the room temperature bonding method according to the invention.

The VSE serves to clean the surface and break bonds of the oxide on the wafer surface. The VSE process can thus enhance the surface activation significantly. A desired bonding species can be used to terminate on surface 34 during the VSE by proper design of the VSE. Alternatively, a post-VSE treatment that activates and terminates the surface with a desired terminating species during the post-VSE process may be used.

The desired species further preferably forms a temporary bond to the surface 34 atomic layer, effectively terminating the atomic layer, until a subsequent time that this surface can be brought together with a surface terminated by the same or another bonding species 36 as shown in FIG. 3D. Desired species on the surfaces will further preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between surfaces 34 and 36 at low or room temperature that is enhanced by diffusion or dissociation and diffusion of the reacted desired species away from the bonding interface.

The post-VSE process preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species. The immersion is preferably performed immediately after the VSE process. The post-VSE process may be performed in the same apparatus in which the VSE process is conducted. This is done most readily if both VSE and post-VSE processes are either dry, i.e., plasma, RIE, ICP, sputtering, etc. or wet, i.e., solution immersion. A desired species preferably consists of a monolayer or a few monolayers of atoms or molecules.

The post-VSE process may also consist of a plasma, RIE, or other dry process whereby appropriate gas chemistries are introduced to result in termination of the surface

with the desired species. The post-VSE process may also be a second VSE process. The termination process may also include a cleaning process where surface contaminants are removed without VSE. In this case, a post-cleaning process similar to the post-VSE processes described above then results in a desired surface termination.

The post-VSE or post-cleaning process may or may not be needed to terminate surfaces with desired species if the activated surface bonds by the cleaning or VSE process are subsequently sufficiently weakly surface reconstructed and can remain sufficiently clean before bonding such that subsequent bonding with a similar surface can form a chemical bond.

The wafers are optionally rinsed then dried. Two wafers are bonded by aligning them (if necessary) and bringing them together to form a bonding interface. As shown in FIG. 3D, a second wafer 35 has been processed in the manner shown in FIG. 3C to prepare bonding surface 36. The two wafers are brought together by, for example, commercially available wafer bonding equipment (not shown) to initiate bonding interface 37 (FIG. 3E).

A spontaneous bond then typically occurs at some location in the bonding interface and propagates across the wafer. As the initial bond begins to propagate, a chemical reaction such as polymerization that results in chemical bonds takes place between species used to terminate surfaces 34 and 36 when the surfaces are in sufficient proximity. The bonding energy is defined as the specific surface energy of one of the separated surfaces at the bonding interface that is partially debonded by inserting a wedge. The by-products of the reaction then diffuse away from the bonding interface to the wafer edge or are absorbed by the wafers, typically in the surrounding materials. The by-products may also be converted to other by-products that diffuse away or are absorbed by the wafers. The amount of covalent and/or ionic bonding may be increased by removal of converted species resulting in further increase in bond strength.

FIGS. 4A-4E show surface conditions and the bonding propagation to form covalent bonds in the case of a planar Si wafer covered with silicon oxide. On Si wafer 40 an  $\text{SiO}_2$  layer 41 is formed, which has been polished and planarized. Surface 42 of layer 41 is subjected to the VSE process to produce an activated surface (FIG. 4A). On a second wafer 44 a second  $\text{SiO}_2$  layer 45 is formed, and surface 46 is subjected to a VSE process to activate surface 46 (FIG. 4B). Desired species are terminated on surface 46 and are shown as lines 43



in FIG. 4C. Either or both of a VSE and post-VSE processes are used to properly terminate surface 46. While not shown, surface 42 may also be terminated using a post-VSE process. Wafer 44 is brought together with wafer 40 (FIG. 4D) and bonds 46 begin to form. the bonding propagates and by-products are removed (indicated as arrows 47) and chemical bonds (such as covalent) are formed, as shown in FIG. 4E.

The bonding immediately after the RIE process may use a special bonding fixture allowing immediate in situ bonding of the etched wafers. A diagram of the fixture is shown in FIG. 7. In plasma chamber 75 are two wafers to be bonded 70 disposed on RF electrodes 76 and 77. A plasma is formed in zone 79 by the application of RF power to the electrodes via moveable vacuum RF power feedthrough 74 and by the introduction of an appropriate gas or gas mixture through gas feedthrough 73. Element 71 is a vacuum feedthrough for mechanical actuator (not shown) to retract retractable spacer 72. Chamber 75 is pumped down to a desired vacuum level via pumps (not shown) and chamber inlet 78. In the case where a post-VSE process or post cleaning process is also a dry process, as discussed above, the VSE and post-VSE or post-cleaning may be conducted in chamber 75.

After the plasma treatment to conduct the VSE process, the mechanical spacers 72 are retracted by the mechanical actuator and the wafers 70 are moved into contact with to begin the bonding process. The bonded wafers are then moved from the chamber into ambient or into another vacuum chamber (not shown) and stored for a desired period to allow the bonding to propagate by a wafer handling system (not shown).

The materials of the bonding layers preferably have an open structure so that the by-products of the polymerization reaction can be easily removed. The bonding species on the opposing bonding surfaces must be able to react at room temperature to form a strong or chemical bond. The bond energy is sufficiently high to virtually eliminate slippage between wafers after subsequent heat treatments associated with a subsequent processing or operation when wafers have different thermal expansion coefficients. Lack of slippage is manifest by a lack of wafer bowing upon inspection after the subsequent processing or operation.

In order to achieve the high bonding energies, it is preferable for at least one of the wafers to be as thin as possible because a thin wafer allows compliance to accommodate a lack of perfect surface planarization and smoothness. Thinning to thickness of about 10 mils to 10 microns is effective.

The bonded wafers are preferably stored at ambient or at low or room temperature after bonding to allow removal of species or converted species for a specified period of time depending upon the materials and species used. Twenty four hours is usually preferable. The storage time is dependent upon the type of plasma process used. Chemical bonds may be obtained more quickly, in a matter of minutes, when certain plasma processes such as an Ar plasma are used. For example, 585 mJ/m<sup>2</sup> bonds were obtained immediately after bonding and over 800 mJ/m<sup>2</sup> were observed after 8 hours for deposited oxides etched by an Ar plasma followed by NH<sub>4</sub>OH dip.

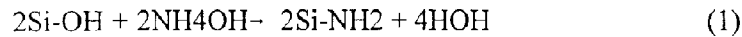
Annealing the bonded wafers during bonding may increase the bonding strength. The annealing temperature should be below 200° C and may be typically in the range of 75-100° C. Storing the bonded wafers under vacuum may facilitate the removal of residual gasses from the bonding surfaces, but is not always necessary.

All of the processes above may be carried out at or near room temperature. The wafers are bonded with sufficient strength to allow subsequent processing operations (lapping, polishing, substrate removal, chemical etching, lithography, masking, etc.). Bonding energies of approximately 500-2000 mJ/m<sup>2</sup> or more can be achieved (see FIG. 6A).

At this point (FIG. 3E) it is possible to remove a part or all of the substrate of wafer 35 by, for instance, lapping and etch back. The layer of devices of wafer 35 is thus transferred onto wafer 30. The devices from the two layers may be interconnected. Additional device or circuit layers may be bonded and interconnected to form a multilayer structure. Different types of wafers, devices or circuits may be bonded, as well as different technologies (i.e. CMOS and bipolar or III-V HBT and Si CMOS). Other elements or materials such as thermal spreaders, surrogate substrates, antennas, wiring layers, a pre-formed multi-layer interconnects, etc. may be bonded to produce different types of circuits or systems, as desired.

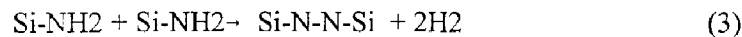
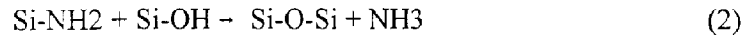
In an example, shown in FIG.2, PECVD SiO<sub>2</sub> is deposited on a Si wafer containing devices. Surface 34, after the plasma (such as argon, oxygen or CF<sub>4</sub>) treatment, is mainly terminated by Si-OH groups due to the availability of moisture in the plasma system and in air. After the plasma treatment, the wafers are immediately immersed in solution such as ammonium hydroxide (NH<sub>4</sub>OH), NH<sub>4</sub>F or HF for a period such as between 10 and 120 seconds. After immersing the wafers in the NH<sub>4</sub>OH solution, many Si-OH groups are

replaced by Si-NH<sub>2</sub> groups according to the following substitution reaction:



Alternatively, many Si-F groups are terminating on the PECVD SiO<sub>2</sub> surface after an NH<sub>4</sub>F or HF immersion.

The hydrogen bonded Si-NH<sub>2</sub>:Si-OH groups or Si-NH<sub>2</sub>:Si-NH<sub>2</sub> groups across the bonding surfaces can polymerize at room temperature in forming Si-O-Si or Si-N-N-Si (or Si-N-Si) covalent bonds:



Alternatively, the HF or NH<sub>4</sub>F dipped oxide surfaces are terminated by Si-F groups in addition to Si-OH groups. Since HF or NH<sub>4</sub>F solution etches silicon oxide strongly, their concentrations must be controlled to an adequately low level, and the immersion time must be sufficiently short. This is an example of a post-VSE process being a second VSE process. The covalent bonds across the bonding interface are formed due to the polymerization reaction between hydrogen bonded Si-HF or Si-OH groups:

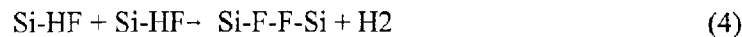


FIG. 8 shows the fluorine concentration profile of bonded thermal oxide covered silicon wafers that were dipped in 0.05% HF before room temperature bonding. A fluorine concentration peak is clearly seen at the bonding interface. This provides evidence of the chemical process described above where the desired species are located at the bonding interface.

Since reaction (2) is reversible only at relatively high temperatures of ~500° C, the formed siloxane bonds should not be attacked by NH<sub>3</sub> at lower temperatures. It is known that H<sub>2</sub> molecules are small and diffuse about 50 times quicker than water molecules in oxide. The existence of a damaged layer near the surface of an adequate thickness i.e. a few nm, will facilitate the diffusion or dissolution of NH<sub>3</sub>, and HF and hydrogen in reactions (2), (3), (4) and/or (5) in this layer and enhancement of the chemical bond. The three reactions result in a higher bonding energy of SiO<sub>2</sub>/SiO<sub>2</sub> bonded pairs at room temperature after a period of storage time to allow NH<sub>3</sub> or H<sub>2</sub> to diffuse away.

In the example of FIG. 2, the plasma treatment may create a damaged or defective

area in the oxide layer near the bonding surface. The zone extends for a few monolayers. The damaged or defective area aids in the removal of bonding by-products. Efficient removal of the bonding by-products improves the bonding strength since the by-products can interfere with the bonding process by preventing high-strength bond from forming..

Many different surfaces of materials may be smoothed and/or planarized, followed by a cleaning process, to prepare for bonding according to the invention. These materials can be room temperature bonded by mating surfaces with sufficient planarity, surface smoothness, and passivation that includes cleaning, and/or VSE, activation and termination. Amorphous and sintered materials, non-planar integrated circuits, and silicon wafers are examples of such materials. Single crystalline semiconductor or insulating surfaces, such as SiO<sub>2</sub> or Si surfaces, can also be provided with the desired surface roughness, planarity and cleanliness. Keeping the surfaces in high or ultra-high vacuum simplifies obtaining surfaces sufficiently free of contamination and atomic reconstruction to achieve the strong bonding according to the invention. Other semiconductor or insulator materials such as InP, GaAs, SiC, sapphire, etc., may also be used. Also, since PECVD SiO<sub>2</sub> may be deposited on many types of materials at low temperatures, many different combinations of materials may be bonded according to the invention at room temperature. Other materials may also be deposited as long as appropriate processes and chemical reactions are available for the VSE, surface activation, and termination.

For example, the method may also be used with silicon nitride as the bonding material. Silicon nitride may be bonded to silicon nitride, or to silicon dioxide and silicon. Silicon oxide may also be bonded to silicon. Other types of dielectric materials may be bonded together including aluminum nitride and diamond-like carbon.

The method may be applied to planar wafers having no devices or circuits and one wafer with devices and circuits. The planar wafer may be coated with a bonding layer, such as PECVD oxide or amorphous silicon, and then processed as described above to bond the two wafers. The planar wafer may not need to be coated with a bonding layer if it has sufficient smoothness and planarity and the proper bonding material.

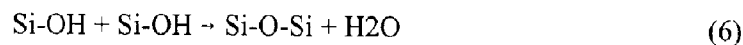
As can be appreciated, the bonding process may be repeated with any number of wafers, materials or functional elements. For example, two device or IC wafers may be joined, followed by removing one of the exposed substrates to transfer a layer or more of

devices, or just the active regions of an IC.

The bonding according to the invention may be applied to joining different types of materials. For example, a silicon wafer can be bonded to another silicon wafer, or bond to an oxidized silicon wafer. The bare silicon wafer and the oxide covered wafer are immersed in HF, NH<sub>4</sub>F and/or NH<sub>4</sub>OH and bonded after drying. The time for the immersion should be less than about twenty minutes for the silicon wafer covered with the thin oxide since the NH<sub>4</sub>OH solution etches silicon oxide. Since HF and NH<sub>4</sub>F etches oxides strongly, very diluted solutions, preferably in 0.01-0.2% range should be used for dipping of the silicon wafers.

After drying the silicon wafer and the oxide-covered wafer are bonded in ambient at room temperature. Reactions (2), (3), (4) and/or (5) take place at the bonding interface between the two wafers. The plasma-treated wafers may also be immersed in deionized water instead of the NH<sub>4</sub>OH solution.

The silicon bonding may be conducted with a bare silicon wafer, i.e. having a native oxide or a silicon wafer having an oxide layer formed on its surface as described above. During the oxygen plasma treatment, the native oxide which if formed on the bare silicon wafer is sputter etched, and the oxide layer formed on the silicon surface is etched. The final surface is an activated (native or formed) oxide. When rinsed in deionized water, the activated oxide surface is mainly terminated with Si-OH groups. Since oxide growth in oxygen plasma has been found to have less water than in normal native oxide layers, the water from the original bonding bridge and generated by the following polymerization reaction (6) can be absorbed into the plasma oxide readily.



FIGS. 5A-5E illustrate bonding two silicon wafers. Wafers 50 and 52 have respective surfaces 51 and 53 with native oxides (not shown) subjected to a VSE process. Surface 53 is in FIG. 5C is shown terminated with a desired species 54. The two wafers are brought together and bonds 55 begin to form (FIG. 5D). The bonding propagates and bonding by-products, in this case H<sub>2</sub> gas, are removed. The by-products being removed are shown as arrows 56 in FIG. 5E.

In addition to removal of the water from the bonding interface by dissolving into the plasma activated oxide of the oxidized silicon wafer, the water can also diffuse through the

thin oxide layer on the bare silicon wafer to react with silicon. As the silicon surface underneath the oxide has a damaged or defective zone, extending for a few monolayers, the water molecules that diffuse through the oxide layer and reach the damaged or defective zone can be converted to hydrogen at room temperature and be removed readily:



The reverse reaction of (6) is thus avoided and the room temperature bonding energy increases enormously due to the formation of covalent Si-O-Si bonds.

If a relatively thick (~5 nm) oxide layer is formed, it will take a long period of time for the water molecules to diffuse through this thick layer. On the other hand, if after the plasma treatment a thin oxide layer is left or a too narrow defective zone is formed, water that can reach the silicon surface may not react sufficiently with the silicon and convert to hydrogen. In both cases the bonding energy enhancement will be limited. The preferred oxygen plasma treatment thus leaves a minimum plasma oxide thickness (e.g., about 0.1-1.0 nm) and a reasonably thick defective zone (e.g., about 0.1-0.3 nm) on the silicon surface.

In a second embodiment, the VSE process uses wet chemicals. For example, an InP wafer having a deposited silicon oxide layer, as in the first embodiment, and a device layer are bonded to a AlN substrate having a deposited oxide layer. After smoothing and planarizing the InP wafer bonding surface and the AlN wafer bonding surface, both wafers are cleaned in an standard RCA cleaning solution. The wafers are very slightly etched using a dilute HF aqueous solution with an HF concentration preferably in the range of 0.01 to 0.2%. About a few tenths of a nm is removed and the surface smoothness is not degraded as determined by AFM (atomic force microscope) measurements. Without deionized water rinse, the wafers are spin dried and bonded in ambient air at room temperature. The resulting bonding energy has been measured to reach ~700 mJ/m<sup>2</sup> after storage in air. After annealing this bonded pair at 75°C the bonding energy of 1500 mJ/m<sup>2</sup> was obtained. The bonding energy has been measured to reach silicon bulk fracture energy (about 2500 mJ/m<sup>2</sup>) after annealing at 100°C. If the wafers are rinsed with deionized water after the HF dip, the bonding energy at 100°C is reduced to 200 mJ/m<sup>2</sup>, that is about one tenth of that obtained without the rinse. This illustrates the preference of F to OH as a terminating species.

In a third embodiment the VSE process consists of 0.1% HF etching followed by 5 min dip in 0.02% HN<sub>4</sub>F solution of thermally oxidized silicon wafers at room temperature

after a standard cleaning process. Without rinsing in deionized water, the wafers are bonded after spin drying at room temperature. The bonding energy of the bonded pairs reaches  $\sim 1700 \text{ mJ/m}^2$  after  $100^\circ\text{C}$  annealing. If the wafers are rinsed in de-ionized water after the HF etching before bonding, the bonding energy of bonded pairs is only  $400 \text{ mJ/m}^2$ , again illustrating the preference of F to OH as a terminating species.

Dilute  $\text{NH}_4\text{F}$  is used in the VSE process to etch silicon oxide covered wafers in a fourth embodiment. The concentration of the  $\text{NH}_4\text{F}$  should be below 0.02% to obtain the desired bonding. The bonding energy of  $\sim 600 \text{ mJ/m}^2$  can be achieved at room temperature after storage.

A fifth embodiment of the invention is used to bond Si surfaces having a native oxide of about 1 nm in thickness. In the fifth embodiment, after cleaning the Si surface by a standard RCA1 cleaning process, a VSE process using 5 min etching in 70%  $\text{HNO}_3$  + diluted HF (preferably 0.01 to 0.02%) is performed. Wafers are pulled out of the solution vertically with a basically hydrophobic surface. Without rinsing in water, the wafers were bonded at room temperature in air. In this process covalent bonding occurs at room temperature with measured bonding energies typically about  $600 \text{ mJ/m}^2$ . This bonding energy is significantly increased to  $1300 \text{ mJ/m}^2$  after annealing at  $75^\circ\text{C}$  and reaches the fracture energy of bulk silicon (about  $2500 \text{ mJ/m}^2$ ) at a temperature of  $100^\circ\text{C}$ .

Instead of 70%  $\text{HNO}_3$ , diluted  $\text{HNO}_3$  with water can be used in the solution to achieve similar results. According to AMF measurements and high resolution transmission electron microscopy measurement results, the silicon is etched in the dilute  $\text{HNO}_3$  VSE process at a rate of 0.1-0.15 nm/min and a new thick oxide 2.5-3.5 nm in thickness is formed.

As further embodiments, the VSE process may consist of a dry etch that has chemical and/or physical components. For a bare Si surface, chemical etching may result from  $\text{SF}_4/\text{H}_2$  gas mixture while physical etching may result from Ar etch. For a silicon oxide surface, chemical etching may use  $\text{CF}_4$  while physical etching may use oxygen or argon gas. It is also possible to use a thermally stable polymer material for the bonding materials and bond two polymer surfaces together. Examples are polyimides or spin-on materials.

The mechanisms governing the increased bond energy at low or room temperature are similar. A very slight etching (VSE) of the bonding wafers by plasma to clean and activate the surfaces, and improve removal of by-products of interface polymerization to prevent the

undesirable reverse reaction and rinse in appropriate solution to terminate the surface with desired species to facilitate room temperature covalent bonding. The oxide covered wafer bonding case is similar except that a different surface termination is preferred. In bare silicon wafer bonding, the highly reactive surface layers of oxide and silicon to allow water adsorption and conversion to hydrogen should be formed. The highly reactive layers can be a plasma thin oxide layer and a damaged silicon surface layer. The oxide on the silicon wafer will also have some damage. Not only O<sub>2</sub> plasma but also plasma of other gases (such as Ar, CF<sub>4</sub>) are adequate. Because during and after VSE the silicon surface is readily to react with moisture to form an oxide layer, and the underlying damaged silicon layer is created by VSE. Since the VSE and by-products removal methods are rather general in nature, this approach can be implemented by many means and apply to many materials.

#### EXAMPLE 1

In a first example, three inch <100>, 1-10 ohm-cm, boron doped silicon wafers were used. PECVD oxide was deposited on some of the silicon wafers. For comparison, thermal oxidized silicon wafers were also studied. The PECVD oxide thickness was 0.5  $\mu\text{m}$  and 0.3  $\mu\text{m}$  on the front side and the back side of the wafers, respectively. Oxide is deposited on both sides of the wafer to minimize wafer bow during polishing and improve planarization. A soft polish was performed to remove about 30 nm of the oxide and to smooth the front oxide surface originally having a root mean square of the micro-roughness (RMS) of  $\sim 0.56$  nm to a final  $\sim 0.18$  nm. A modified RCA1 solution was used to clean the wafer surfaces followed by spin-drying.

Two wafers were loaded into the plasma system, both wafers are placed on the RF electrode and treated in plasma in RIE mode. For comparison, some wafers were treated in plasma mode in which the wafers were put on the grounded electrode. An oxygen plasma was used with a nominal flow rate of 16 scc/m. The RF power was 20-400 W (typically 80 W) at 13.56 MHz and the vacuum level was 100 mTorr. The oxide covered wafers were treated in plasma for times between 15 seconds to 5 minutes. The plasma treated silicon wafers were then dipped in an appropriate solution or rinse with de-ionized water followed by spin-drying and room temperature bonding in air. Some of the plasma treated wafers were also directly bonded in air without rinse or dipping.



The bonding energy was measured by inserting a wedge into the interface to measure the crack length according to the equation:

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4 (E_1 t_{w1}^3 + E_2 t_{w2}^3)}$$

$E$  and  $t_w$  are the Young's modulus and thickness for wafers one and two and  $t_b$  is the thickness of a wedge inserted between the two wafers that results in a wafer separation of length  $L$  from the edge of the wafers.

The room temperature bonding energy as a function of storage time of bonded plasma treated oxide covered silicon wafers is shown in FIG. 6A. This figure shows measured room temperature bonding energy versus storage time for 4 different cases as shown. The results can be summarized as follows: (1) for dipped and bonded RIE plasma treated oxide wafers, the room temperature bonding energy increases with storage time and reaches a stable value after ~20 h in air or at low vacuum; (2) RIE mode results in higher bonding energies than plasma mode; (3) too short a plasma exposure time or too low a plasma power provides a small or negligible increase in bond energy; (4)  $\text{NH}_4\text{OH}$  dip after plasma treatment shows a much higher increase in bonding energy than water rinse; (5) direct bonding in air after plasma treatment without dipping or rinse shows an almost constant bonding energy with time. The bonding energy of the directly bonded wafer pairs immediately after room temperature bonding is slightly higher than the de-ionized water rinsed or  $\text{NH}_4\text{OH}$  dipped wafer pairs.

FIG. 6B shows room temperature bonding of Si and AlN wafers with PECVD oxide deposited layers. After about 100 h of storage time a bonding energy of over 2000 mJ/m<sup>2</sup> were observed.

Comparing different bonding materials, the bonding energy as a function of storage time of  $\text{O}_2$  plasma treated thermally oxidized silicon wafer pairs is similar to wafers with PECVD oxide, although the values of the room temperature bonding energy are somewhat lower.

After ~24 h storage in air at room temperature, the bonding energy as high as ~1000 mJ/m<sup>2</sup> was reached in the RIE mode plasma treated and  $\text{NH}_4\text{OH}$  dipped PECVD oxide

covered wafer pairs. Since the maximum bonding energy of a van der Waals bonded silicon oxide covered wafer pairs is about 200 mJ/m<sup>2</sup>, a large portion of the bonding energy is attributed to the formation of covalent bonds at the bonding interface at room temperature according to the above equation.

### EXAMPLES 2-3

The above process was applied to bond processed InP wafers (600  $\mu\text{m}$  thick) to AlN wafers (380  $\mu\text{m}$  thick), or to bond processed Si (380  $\mu\text{m}$  thick) and InP (600  $\mu\text{m}$  thick) wafers, as second and third examples. The processed InP device wafers are covered with PECVD oxide and planarized and smoothed by chemical-mechanical polishing CMP. A PECVD oxide layer is also deposited on the AlN wafers and is planarized and smoothed to improve the RMS surface roughness. The processed Si and processed InP wafers are deposited with PECVD oxide and planarized and smoothed using CMP. After VSE similar to the example 1 bonding at room temperature, the bonded wafers are left in ambient air at room temperature.

After 24 hours storage at room temperature, bonding energy of 1000 mJ/m<sup>2</sup> and 1100 mJ/m<sup>2</sup> were achieved for the InP/Si and InP/AlN bonded pairs, respectively. For processed Si (380  $\mu\text{m}$  thick) /oxide covered AlN (280  $\mu\text{m}$  thick) wafer pairs, the bonding energy at room temperature as high as 2500 mJ/m<sup>2</sup> has been achieved. These room temperature bonded plasma treated wafer pairs have sufficient bonding strength to sustain subsequent substrate lapping and etching and other typical semiconductor fabrication processes before or after substrate removal.

The InP substrate in the room temperature bonded InP/AlN pairs was lapped with 1900# Al<sub>2</sub>O<sub>3</sub> powder from initial 600  $\mu\text{m}$  thick to ~50  $\mu\text{m}$  thick followed by etching in an HCl/H<sub>3</sub>PO<sub>4</sub> solution to leave about a 2.0  $\mu\text{m}$  thick InP device layer on the AlN or Si wafer. The water and etching solution did not penetrate into the bonding interface.

Surfaces are sputter etched by energetic particles such as radicals, ions, photons and electrons in the plasma or RIE mode. For example, the O<sub>2</sub> plasma under conditions that bring about the desired VSE is sputter-etching about 2 Å /min of PECVD oxide as measured by a reflectance spectrometry. For thermal oxide the sputter etching rate is about 0.5 Å/min. The thickness of oxide before and after plasma treatment was measured by a reflectance

spectrometry and averaged from 98 measured points on each wafer. The etching by  $O_2$  plasma has not only cleaned the surface by oxidation and sputtering but also broken bonds of the oxide on the wafer surfaces.

However, the surface roughness of plasma treated oxide surfaces must not be degraded by the etching process. AFM measurements show that compared with the initial surface roughness, the RMS of the  $O_2$  plasma treated oxide wafers was  $\sim 2 \text{ \AA}$  and did not change noticeably. On the other hand, if the etching is not sufficiently strong, the bonding energy enhancement effect is also small. Keeping other conditions unchanged when the  $O_2$  plasma treatment was performed with plasma mode rather than RIE mode, the etching of oxide surfaces is negligible and the oxide thickness does not change. The final room temperature bonding energy is only  $385 \text{ mJ/m}^2$  compared to  $1000 \text{ mJ/m}^2$  of RIE treated wafers (see FIG. 6A).

Other gas plasma has shown a similar effect.  $CF_4/O_2$  RIE was used to remove  $\sim 4 \text{ nm}$  of PECVD oxide from the wafer surfaces prior to bonding. The bonding energy of room temperature bonded PECVD oxide covered silicon wafers was also enhanced significantly in this manner and exceeds  $1000 \text{ mJ/m}^2$  after sufficient storage time (see also FIG. 6A).

An argon plasma has also been used for the VSE with a nominal flow rate of  $16 \text{ scc/m}$ . The RF power was typically  $60 \text{ W}$  at  $13.56 \text{ MHz}$  and the vacuum level was  $100 \text{ mTorr}$ . The oxide covered silicon wafers were treated in plasma in RIE mode for times between 30 seconds to 2 minutes. The plasma treated silicon wafers were then dipped in an  $NH_4OH$  solution followed by spin-drying and room temperature bonding in air. The bonding energy reached  $\sim 800 \text{ mJ/m}^2$  at room temperature after only 8 h storage in air.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

**Claims:**

1. A bonding method, comprising:  
forming first and second bonding surfaces;  
etching said first and second bonding surfaces; and  
bonding together at room temperature said first and second bonding surfaces after said etching step.
2. A method as recited in claim 1, wherein said etching step comprises:  
etching said first and second bonding surfaces such that respective surface roughnesses of said first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching.
3. A method as recited in claim 2, comprising:  
forming said first and second bonding surfaces to have a surface roughness in a range of 0.1 to 3.0 nm.
4. A method as recited in claim 1, wherein said etching step comprises:  
activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.
5. A method as recited in claim 4, comprising:  
forming bonding groups capable of forming chemical bonds at approximately room temperature.
6. A method as recited in claim 1, comprising:  
forming chemical bonds between said bonding surfaces allowing bonded groups to diffuse or dissociate away from an interface of said first and second bonding surfaces.
7. A method as recited in claim 6, comprising:  
increasing bonding strength between said first and second bonding surfaces by diffusing or dissociating away said bonding groups.
8. A method as recited in claim 1, wherein said etching step comprises:  
forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.
9. A method as recited in claim 8, wherein said etching step comprises:  
forming a few monolayers of one of a desired atom and a desired molecule on said bonding surface.

10. A method as recited in claim 1, comprising:  
after said etching step, immersing said first and second bonding surfaces in a solution to form bonding surfaces terminated with desired species.

11. A method as recited in claim 10, wherein said species comprise at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group.

12. A method as recited in claim 10, wherein said etching step comprises:  
forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.

13. A method as recited in claim 1, wherein said etching comprises:  
exposing said first and second bonding surfaces to a plasma.

14. A method as recited in claim 1, comprising:  
exposing said first and second bonding surfaces to one of an oxygen, argon,  $\text{NH}_3$  and  $\text{CF}_4$  plasma process.

15. A method as recited in claim 14, comprising:  
conducting said plasma process in one of RIE mode, ICP mode, plasma mode and sputtering mode.

16. A method as recited in claim 1, comprising:  
polishing respective first and second bonding surfaces to respective desired surface roughnesses and planarity; and  
etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

17. A method as recited in claim 16, wherein:  
forming at least one of said first and second bonding surfaces comprises depositing a polishable material on a non-planar surface.

18. A method as recited in claim 17, wherein depositing said polishable material comprises depositing one of silicon oxide, silicon nitride or a dielectric polymer.

19. A method as recited in claim 1, wherein said etching step comprises:  
increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature.

20. A method as recited in claim 19, comprising:  
obtaining a bond of at least  $500 \text{ mJ/m}^2$ .

21. A method as recited in claim 19, comprising:  
obtaining a bond of at least 1000 mJ/m<sup>2</sup>.
22. A method as recited in claim 19, comprising:  
obtaining a bond of at least 2000 mJ/m<sup>2</sup>.
23. A method as recited in claim 1, comprising:  
forming a bond of at least 500 mJ/m<sup>2</sup>.
24. A method as recited in claim 1, comprising:  
obtaining a bond of at least 1000 mJ/m<sup>2</sup>.
25. A method as recited in claim 1, comprising:  
obtaining a bond of at least 2000 mJ/m<sup>2</sup>.
26. A method as recited in claim 1, comprising:  
forming chemical bonds between said bonding surfaces.
27. A method as recited in claim 26, comprising:  
forming chemical bonds between said bonding surfaces in one of ambient and vacuum.
28. A method as recited in claim 26, comprising:  
forming chemical bonds between said bonding surfaces in one of low and ultra high and vacuum.
29. A method as recited in claim 1, comprising:  
forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent processing of said bonded bonding surfaces.
30. A method as recited in claim 29, comprising:  
forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent thermal cycling of said bonded bonding surfaces.
31. A method as recited in claim 1, wherein said etching step comprises:  
increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature; and  
propagating said bonding at room temperature.
32. A method as recited in claim 31, comprising:  
propagating chemical bonding at room temperature.
33. A method as recited in claim 1, comprising:

depositing silicon dioxide as first and second bonding materials having said first and second bonding surfaces; and

etching said first and second bonding surfaces using an oxygen plasma.

34. A method as recited in claim 33, comprising:

rinsing said bonding materials in an ammonia-based solution after said etching.

35. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium hydroxide after said etching.

36. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium fluoride after said etching.

37. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces under vacuum; and

bonding said first and second bonding surfaces without breaking said vacuum.

38. A method as recited in claim 1, comprising:

depositing a bonding material on each of first and second surfaces to obtain said first and second bonding surfaces.

39. A method as recited in claim 38, comprising:

depositing one of silicon dioxide and silicon nitride as said bonding material.

40. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of oxygen,  $\text{CF}_4$ , and Ar plasma RIE; and

rinsing said silicon dioxide in an ammonia-based solution after said etching.

41. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a wet etch process.

42. A method as recited in claim 42, comprising:

immersing said first and second bonding surfaces into a solution after said etching.

43. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of diluted HF and diluted  $\text{NH}_4\text{F}$ .

44. A method as recited in claim 43, comprising:

rinsing said silicon dioxide in an ammonia-based solution after said etching.

45. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon; and  
etching said bonding surfaces using a solution of  $\text{HNO}_3$  and diluted HF.

46. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon each having a native oxide layer; and

activating said native oxide layer using said etching step.

47. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces each as silicon having a native oxide layer; and

exposing said first and second bonding surfaces to an oxygen plasma to etch said native oxide layers.

48. A method as recited in claim 47,

creating a defective zone in said silicon during plasma etching.

49. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a plasma RIE process;

forming a region having defects proximate to said bonding surface; and

removing bonding by-products using said region.

50. A method as recited in claim 1, wherein said etching comprises:

activating said first and second bonding surfaces; and

creating a region under said first and second bonding surfaces for removing bonding by-products.

51. A method as recited in claim 1, comprising:

creating a region proximate to said first and second bonding surfaces for at least one of removal and conversion of bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces.

52. A method as recited in claim 1, comprising:

forming said first bonding surface by depositing an oxide layer on a first semiconductor wafer;

forming said second bonding surface by depositing an oxide layer on a second semiconductor wafer; and

bonding said first and second semiconductor wafers.



53. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a first semiconductor wafer, said first wafer comprising a first substrate and a first active region;

forming said second bonding surface as a deposited oxide layer on a second semiconductor wafer, said second wafer comprising a second substrate and a second active region;

bonding said first and second semiconductor wafers; and

removing at least a substantial portion of one of said first and second substrates after said bonding.

54. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a semiconductor wafer, said wafer comprising a substrate and an active region;

forming said second bonding surface as a surrogate substrate;

bonding said wafer and said surrogate substrate; and

removing at least a substantial portion of said first substrate after said bonding.

55. A method as recited in claim 1, wherein said bonding comprises:

maintaining contact between said first and second bonding surfaces for a specified period to produce bonding polymerization and allow removal of by-products.

56. A method as recited in claim 55, comprising:

maintaining said contact between said first and second bonding surfaces for a period less than about 20 hours.

57. A method as recited in claim 1, wherein said bonding comprises:

maintaining said first and second bonding surfaces for a specified period in ambient to remove bonding by-products.

58. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces using a bonding fixture under vacuum;

bonding said first and second bonding surfaces using said fixture to bring together said first and second bonding surfaces while maintaining said vacuum.

59. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices; and

polishing said first oxide layer to form said first bonding surface.

60. A method as recited in claim 59, comprising:  
forming a second oxide layer on a second wafer containing electrical devices; and  
polishing said second oxide layer to form said second bonding surface.
61. A method as recited in claim 60, comprising:  
forming said first oxide layer on said first wafer containing electrical devices of a first technology; and  
forming said second oxide layer on said second wafer containing electrical devices of a second technology different from said first technology.
62. A method as recited in claim 60, comprising:  
interconnecting said first and second devices.
63. A method as recited in claim 60, comprising:  
forming said first bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.
64. A method as recited in claim 60, comprising:  
forming said second bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.
65. A method as recited in claim 1, comprising:  
forming said first bonding surface on a first wafer containing a first integrated circuit.
66. A method as recited in claim 65, comprising:  
forming said second bonding surface on a second wafer containing a second integrated circuit.
67. A method as recited in claim 66, comprising:  
forming said first bonding surface on said first wafer containing said first integrated circuit of a first technology; and  
forming said second bonding surface on said second wafer containing said second integrated circuit of a second technology different from said first technology.
68. A method as recited in claim 66, comprising:  
interconnecting said first and second integrated circuits.
69. A method as recited in claim 1, comprising:  
said first and second bonding surfaces being substantially planar.
70. A method as recited in claim 1, wherein:

forming said first and second bonding surfaces comprises depositing a dielectric material.

71. A method as recited in claim 70, comprising:

polishing said dielectric material to a desired planarity and surface roughness.

72. A method as recited in claim 70, comprising:

depositing said dielectric material on a non-planar surface.

73. A method as recited in claim 72, wherein:

said polishing comprises chemical-mechanical polishing.

74. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces to be non-planar; and

polishing said first and second bonding surfaces to a desired planarity and surface roughness

75. A method as recited in claim 74, wherein:

said polishing comprises chemical-mechanical polishing.

76. A method as recited in claim 1, where said etching comprises:

activating said bonding surfaces; and

terminating said bonding surfaces with a desired species.

77. A method as recited in claim 1, wherein said etching comprises:

a first etching step to activate said bonding surfaces; and

a second etching step to terminate said bonding surfaces with a desired species.

78. A method as recited in claim 1, comprising:

obtaining etched bonding surfaces using said etching step; and

exposing said bonding surfaces to a gaseous chemical environment to terminate said etched bonding surfaces with a desired species.

79. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having a non-planar surface; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

80. A method as recited in claim 79, comprising:

forming said second oxide layer on said second wafer having a non-planar surface.

81. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having an irregular surface topology; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

82. A method as recited in claim 81, comprising:

forming said second oxide layer on said second wafer having an irregular surface topology.

83. A bonding method, comprising:

forming first and second bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm;

removing material from said first and second bonding surfaces while maintaining said surface roughness; and

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m<sup>2</sup>.

84. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m<sup>2</sup>.

85. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m<sup>2</sup>.

86. A method as recited in claim 83, comprising:

activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.

87. A method as recited in claim 83, comprising:

polishing respective first and second bonding surfaces to said surface roughness; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

88. A method as recited in claim 83, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

89. A method as recited in claim 83, comprising:

etching said first and second bonding surfaces using a plasma RIE process;

forming a subsurface layer having defects; and

removing bonding by-products using said subsurface layer.

90. A method as recited in claim 83, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

91. A method as recited in claim 90, comprising:

removing a substantial portion of said one of said first and second wafers.

92. A method as recited in claim 90, comprising:

interconnecting devices in said first and second wafers.

93. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

94. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices and having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

95. A bonding method, comprising:

forming first and second bonding surfaces;

etching said first and second bonding surfaces;

terminating said first and second bonding surfaces with a species allowing formation of chemical bonds at about room temperature; and

bonding said first and second bonding surfaces at about room temperature.

96. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m<sup>2</sup>.

97. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m<sup>2</sup>.

98. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m<sup>2</sup>.

99. A method as recited in claim 95, comprising:

activating said first and second bonding surfaces prior to said bonding step.

100. A method as recited in claim 95, comprising:

polishing said first and second bonding surfaces; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

101. A method as recited in claim 95, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

102. A method as recited in claim 95, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

103. A method as recited in claim 102, wherein one of said first and second wafers comprises a substrate, said method comprising:

removing a substantial portion of said one of said first and second wafers.

104. A method as recited in claim 102, comprising:

interconnecting devices in said first and second wafers.

105. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

106. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices and

having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and

having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

107. A bonded device, comprising:

a first material having a first etched bonding surface; and

a second material having a second etched bonding surface directly bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m<sup>2</sup>.

108. A device as recited in claim 107, comprising:

said first and second bonding surfaces being activated and terminated with a desired bonding species.

109. A device as recited in claim 108, wherein said desired species comprise:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

110. A device as recited in claim 108, wherein said desired species comprise at least one of a silanol group, an NH<sub>2</sub> group, a fluorine group and an HF group.

111. A device as recited in claim 107, comprising:

said first and second bonding surfaces each having a defective region located proximate to said first and second bonding surfaces, respectively.

112. A device as recited in claim 107, wherein:

said first material comprises a surface of a first semiconductor wafer having devices formed therein; and

said second material comprises a surface of a second semiconductor wafer having devices formed therein.

113. A device as recited in claim 112, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

114. A device as recited in claim 112, comprising:  
devices in said first and second wafers being interconnected.

115. A device as recited in claim 112, comprising:  
said first and second wafers being different technologies.

116. A device as recited in claim 107, wherein:  
one of said first and second wafers comprises an integrated circuit.

117. A device as recited in claim 116, comprising:  
devices in said first and second wafers being interconnected.

118. A device as recited in claim 116, comprising:  
said first and second wafers having an irregular surface topology.

119. A device as recited in claim 107, wherein:  
said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

120. A device as recited in claim 119, wherein:  
said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

121. A method as recited in claim 107, wherein:  
said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and  
said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

122. A method as recited in claim 121, comprising:



said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.

123. A bonded device, comprising:

a first material having a first etched and activated bonding surface terminated with a first desired bonding species; and

a second material having a second etched and activated bonding surface terminated with a second desired bonding species bonded to said first bonding surface at room temperature.

124. A device as recited in claim 123, wherein said species comprise at least one of a silanol group, an  $\text{NH}_2$  group, a fluorine group and an HF group.

125. A device as recited in claim 123, comprising:

said first and second bonding surfaces each having a defective region located proximate to said surfaces.

126. A device as recited in claim 123, wherein said desired species comprises:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

127. A device as recited in claim 123, comprising:

said second bonding surface bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m<sup>2</sup>.

128. A device as recited in claim 123, wherein:

said first bonding surface comprises a surface of a first semiconductor wafer having devices formed therein; and

said second bonding surface comprises a surface of a second semiconductor wafer having devices formed therein.

129. A device as recited in claim 128, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

130. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

131. A device as recited in claim 123, comprising:

said first and second wafers being different technologies.

132. A device as recited in claim 123, wherein:

one of said first and second wafers comprises an integrated circuit.

133. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

134. A device as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

135. A device as recited in claim 134, wherein:

said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

136. A method as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and

said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

137. A method as recited in claim 123, wherein:

said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.

138. A method as recited in claim 1, wherein said first and second bonding surfaces are respective surfaces of first and second substrates, the method comprising:

removing a substantial portion of one of said first and second substrates.

139. A method as recited in claim 138, comprising:

annealing said bonded substrates after said removing step.

140. A method as recited in claim 138, wherein said first and second substrates have

first and second electrical devices, the method comprising:

interconnecting said first and second devices after said removing step.

141. A method as recited in claim 91, comprising:

annealing said bonded substrates after said removing step.

142. A method as recited in claim 91, comprising:

interconnecting devices in said first and second semiconductor wafers after said removing step.

143. A method as recited in claim 103, comprising:

annealing said bonded substrates after said removing step.

144. A device as recited in claim 113, wherein:

said device region comprises an annealed device region.

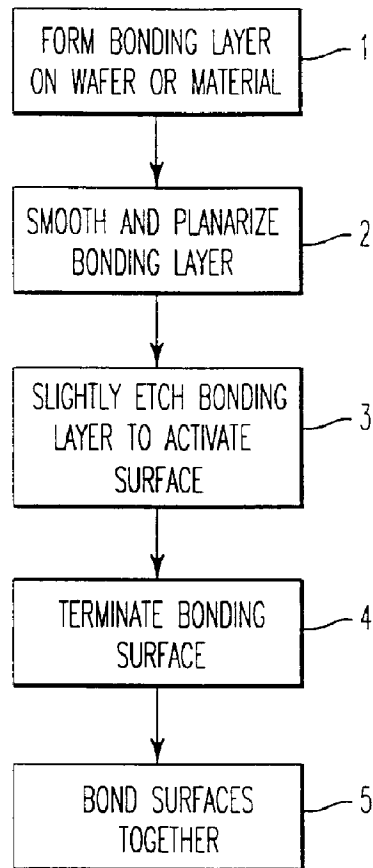
145. A device as recited in claim 129, wherein;

said first and second materials comprise respective first and second substrates; and one of said first and second substrates comprises a substrate region obtained by removing a substantial portion of a substrate of said one of said first and second substrate.

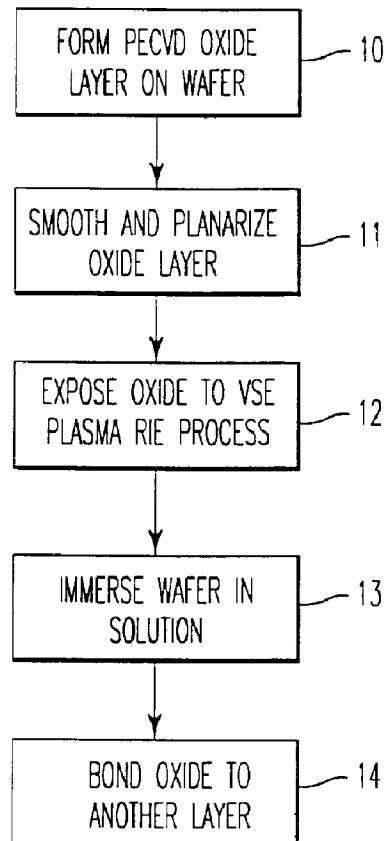
146. A device as recited in claim 145, wherein:

said substrate region comprises an annealed substrate region.

1/9

*FIG. 1*

2/9

*FIG. 2*

3/9

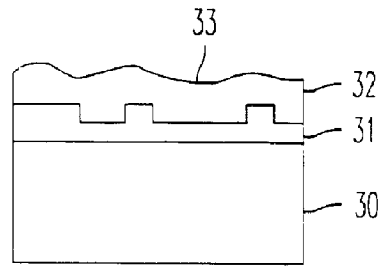


FIG. 3A

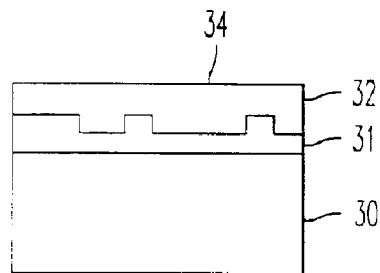


FIG. 3B

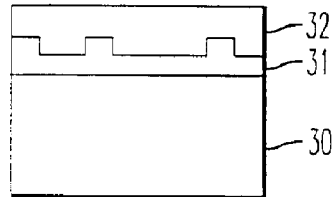
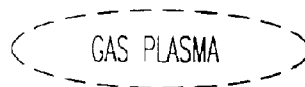


FIG. 3C

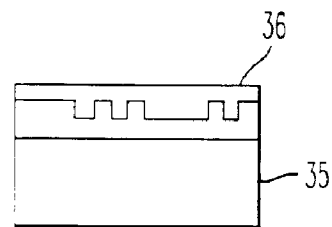


FIG. 3D

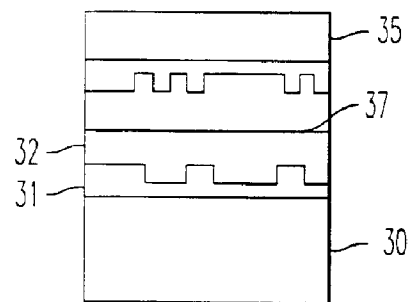
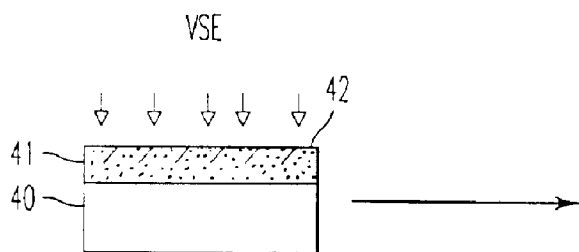
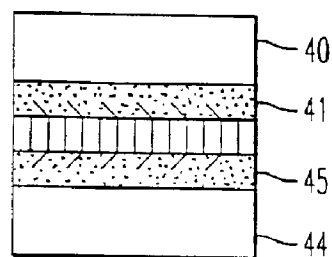
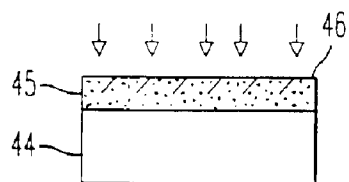
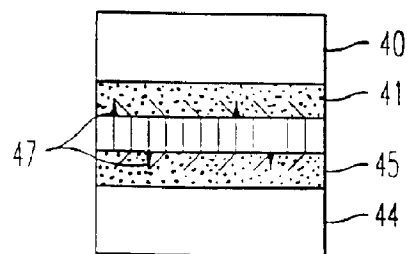
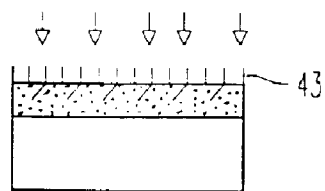


FIG. 3E

SUBSTITUTE SHEET (RULE 26)

*FIG. 4A**FIG. 4D**FIG. 4B**FIG. 4E**FIG. 4C*

VSE

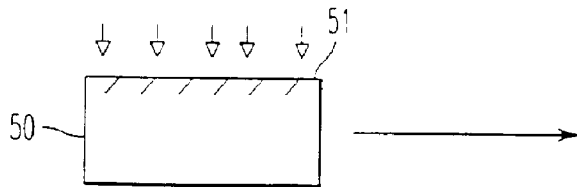


FIG. 5A

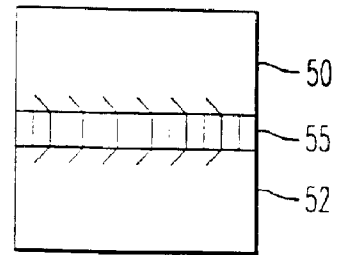


FIG. 5D

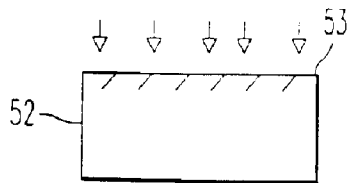


FIG. 5B

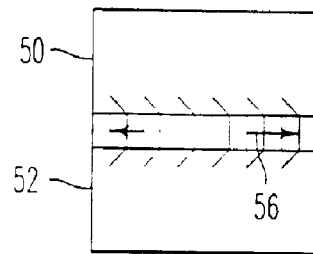


FIG. 5E

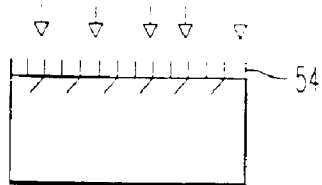
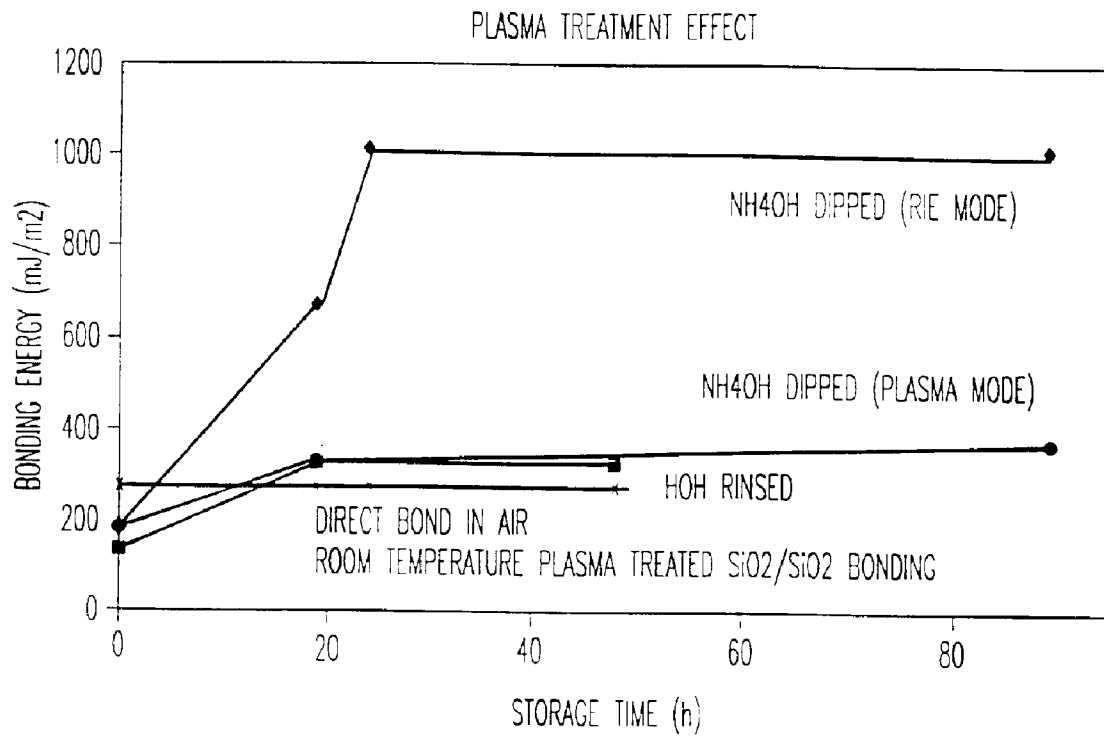
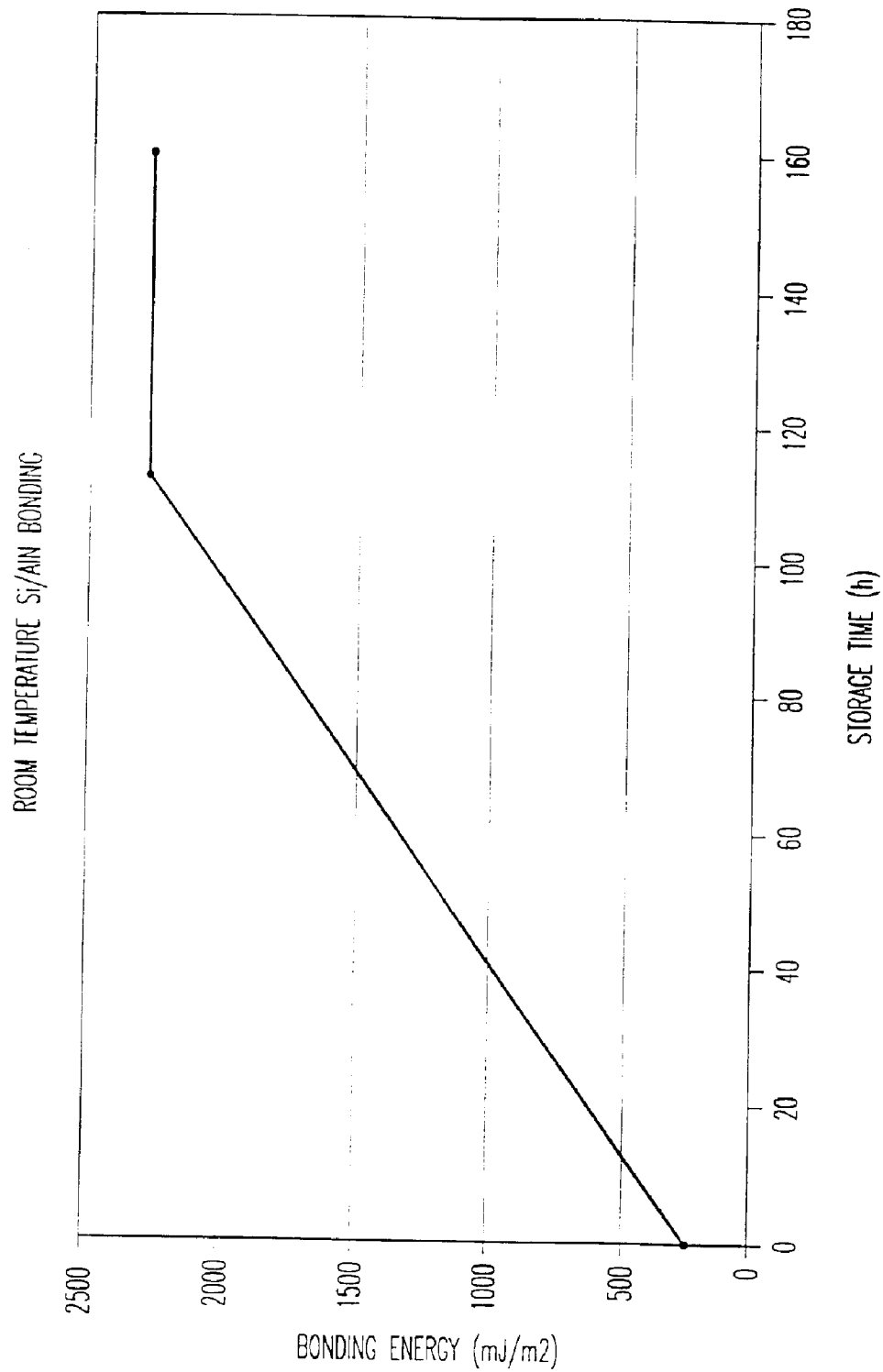


FIG. 5C

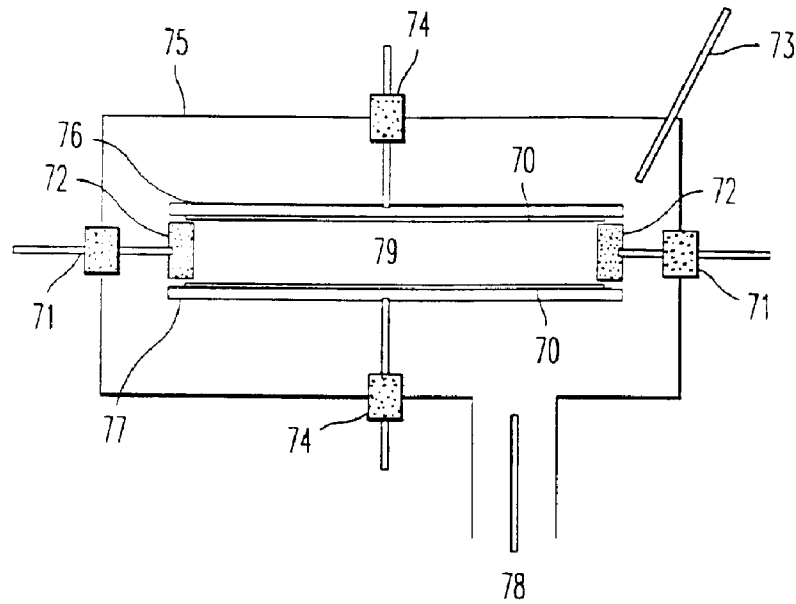


6/9

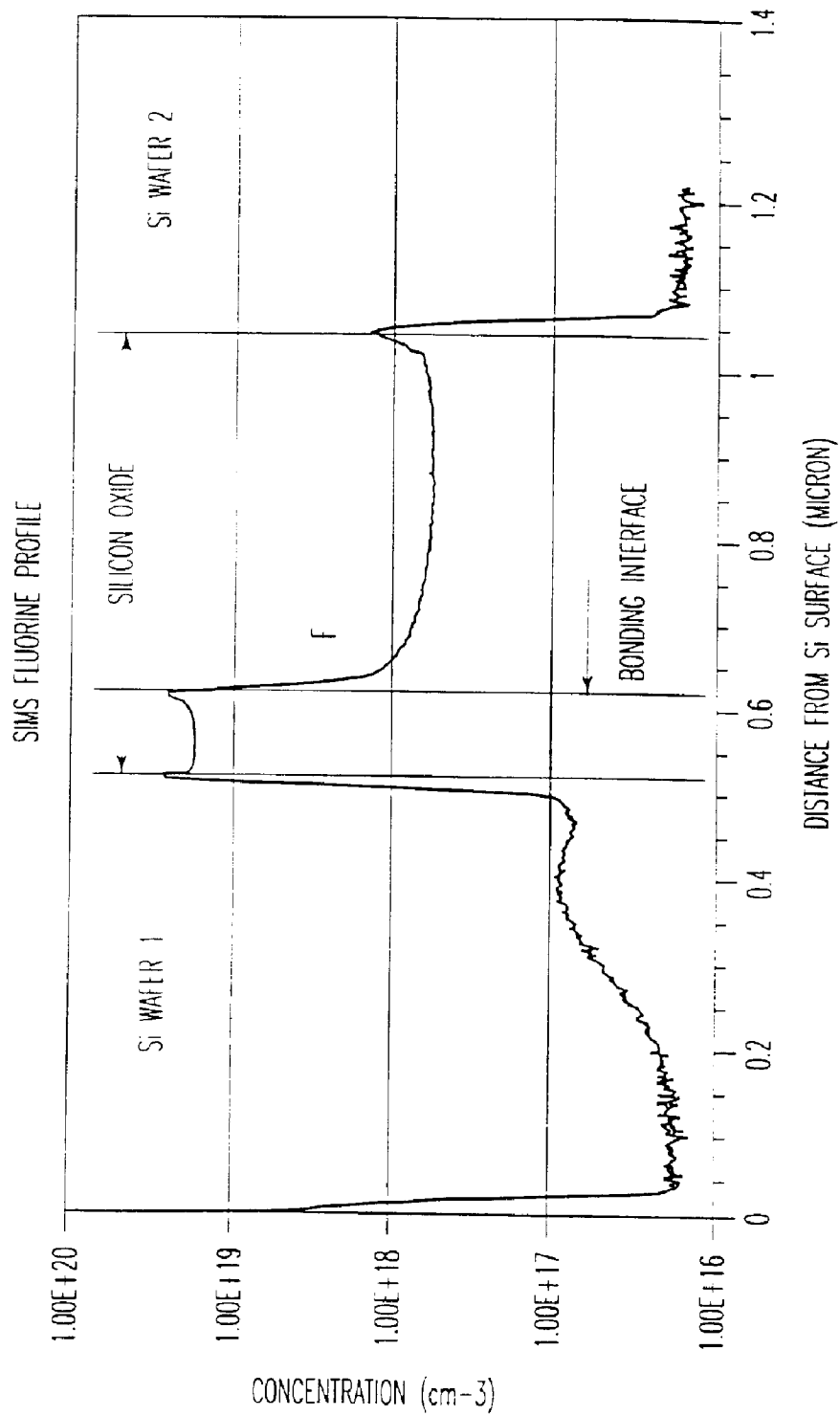
*FIG. 6A*

*FIG. 6B*

SUBSTITUTE SHEET (RULE 26)



*FIG. 7*



**FIG. 8**

(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開平8-195334

(43) 公開日 平成8年(1996)7月30日

(51) Int.Cl. <sup>6</sup>	識別記号	庁内整理番号	F I	技術表示箇所
H 0 1 L	21/02	B		
	21/308	G		
	27/12	B		

審査請求 未請求 請求項の数 8 O L (全 5 頁)

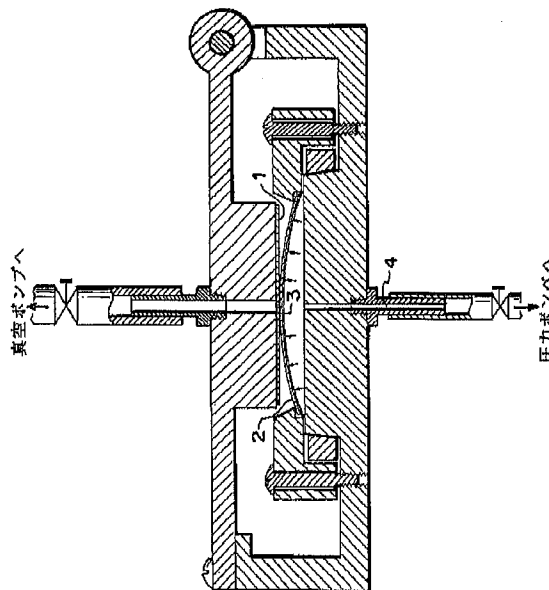
(21) 出願番号	特願平7-40398	(71) 出願人	000001007 キヤノン株式会社 東京都大田区下丸子3丁目30番2号
(22) 出願日	平成7年(1995)2月28日	(72) 発明者	高木 博嗣 東京都大田区下丸子3丁目30番2号 キヤ ノン株式会社内
(31) 優先権主張番号	特願平6-283470	(72) 発明者	赤池 正剛 東京都大田区下丸子3丁目30番2号 キヤ ノン株式会社内
(32) 優先日	平6(1994)11月17日	(72) 発明者	八木 隆行 東京都大田区下丸子3丁目30番2号 キヤ ノン株式会社内
(33) 優先権主張国	日本 (J P)	(74) 代理人	弁理士 山下 穰平

(54) 【発明の名称】 シリコン基板の接合方法

(57) 【要約】

【目的】 シリコン基板どうしの接合工程において、低温処理で強固な接合を可能とすることにより、また、これにより高温に耐える材料以外の材料も利用可能とし、更に膜はがれや、ボイドの発生も防止する。

【構成】 シリコン基板1, 2表面を疎水化処理する工程と、該疎水化処理した前記基板どうしを加圧下で接触させて接合する工程と、その後加熱処理して前記接合を強化する工程と、を有することを特徴とするシリコン基板の接合方法。前記基板どうし1, 2を加圧下で接触させて接合する工程は、前記基板1, 2の中央部から順次接触させることを特徴とする。



## 【特許請求の範囲】

【請求項1】 シリコン基板表面を疎水化処理する工程と、該疎水化処理した前記基板どうしを加圧下で接触させて接合する工程と、その後加熱処理して前記接合を強化する工程と、を有することを特徴とするシリコン基板の接合方法。

【請求項2】 前記疎水化処理は、フッ酸により前記基板表面の自然酸化膜を除去することを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項3】 前記疎水化処理は、バッファーフッ酸を用いることを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項4】 前記疎水化処理は、高真空中で基板表面に加速した不活性イオンを照射し、清浄なシリコン表面を形成した後、水素ガスを導入して基板表面を水素原子で終端することを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項5】 前記基板どうしを加圧下で接触させて接合する工程は、前記基板の中央部から順次接触させることを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項6】 前記加熱処理は250℃～700℃で行なうことを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項7】 前記加熱処理は、前記シリコン基板の中央より温度上昇させることを特徴とする請求項1に記載のシリコン基板の接合方法。

【請求項8】 前記加熱処理は、前記シリコン基板の端部より温度上昇させることを特徴とする請求項1に記載のシリコン基板の接合方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は、半導体基板の製造方法に関し、特にシリコン基板どうしの接合方法に関する。

## 【0002】

【従来の方法】シリコン基板どうしの接合は、SOI (Silicon on Insulator) 基板の作製に不可欠な技術である。従来、シリコン基板同士の接合は、特開昭39-17869号公報あるいは特開昭62-27040号公報に見られるように、基板を接触後、酸化雰囲気中で加熱する、あるいは親水化処理した基板を接触後加熱する方法が用いられており、基板は酸化層を介して接合されている。

## 【0003】

【発明が解決しようとする課題】しかしながら、これまでの方法では、強固な接合を得るためには、接触後1000℃前後に加熱する必要がある。従って、接合前に基板上に素子が形成されているような場合、このような高温に耐えるためには使用する材料が極めて制限されるとい問題がある。

【0004】さらに、積層された構造においては各層材料の熱膨張差により膜剥がれが発生するという問題もある。従来の方法はまた、基板表面の水酸基の脱水分解により発生したガスがボイドとして残りやすく、これが接合強度を低下させるという問題もあった。

【0005】(発明の目的) 本発明の目的は、シリコン基板の接合工程において、低温処理で強固な接合を可能とすることにあり、また、これにより高温に耐える材料以外の材料も利用可能とし、更に膜はがれや、ボイドの発生も防止することにある。

## 【0006】

【課題を解決するための手段】本発明のシリコン基板の接合方法は、前記課題を解決するための手段としてシリコン基板表面の疎水化処理工程、加圧しながらの基板どうしの接触工程、加熱処理工程の3つの工程を有することを特徴とする。

【0007】まず、シリコン表面の疎水化は、代表的にはフッ酸による表面の自然酸化膜を除去することでおこなわれる。フッ酸処理によりシリコン表面の大部分が水素原子で終端される。使用されるフッ酸の濃度は10重量%以下であり、1～5%のフッ酸処理が疎水化処理に適している。PHを3～6に調整したバッファーフッ酸を使用してもよい。またフッ酸処理前に基板表面に付着している有機物等の不純物を除去する処理をしてもよい。この場合、基板表面に凹凸を形成するような処理は避けなければならない。疎水化処理方法としては上記フッ酸処理の他、高真空中で基板表面に加速した不活性イオンを照射し、清浄なシリコン表面を形成した後、水素ガスを真空槽に導入し、基板表面を水素原子で終端する方法がある。

【0008】次に、疎水化処理された2枚の基板は圧力を加えながら接触させられる。図1は本発明で基板の接合に使用した装置の概略図である。この装置は第1の基板1を平坦に保持し、流体導入口4から加圧された流体(液体、気体のどちらでもよい)を導入し、この流体圧を第2の基板2の裏面に印加しながら2枚の基板を近接させるものである。図1の装置では流体圧は薄いメンブレン3に加えられ、このメンブレンが球面状にたわむため、それに接する第2基板2も球面状にたわむ。第2基板2がたわむことにより2枚の基板はそれぞれの中央部から接触していく。この接触方法では、接触過程で雰囲気ガスが周辺部に追い出されるため、大気中においても基板間にガスが残留することがない。もちろん2枚の基板を真空中で接触させてもよい。流体圧は3kg/cm<sup>2</sup>以上あれば十分効果がある。

【0009】次に、接触した2枚のシリコン基板の接合を強固にするために加熱する。本発明では加熱温度が250℃以上あれば実用上十分な接合強度が得られるが、300℃～700℃、さらに好ましくは500～700℃であれば従来方法に匹敵する強固な接合が達成され

る。ヒータ加熱、ランプ加熱等の加熱手段により接合基板を昇温する。また、加熱中の雰囲気は接合には制限がなく大気中、不活性ガス中、真空中いずれでもよい。

【0010】加熱する効果は以下のように推測される。加熱によりシリコン基板表面に吸着している水素原子が脱離することにより、基板最表面にあるシリコン原子同士が直接結合するか、あるいは水素原子と大気中の酸素原子が置き変わり、酸素原子を介してシリコン原子が結合することによって2枚のシリコン基板の接合がおこなわれる。

【0011】加熱中における接合強度の増加過程において、基板周辺部より強い結合がすすんだ場合において、基板の中央部にしばしば空洞（ボイド）が発生することがある。一旦強固に接合した部分はひずみを緩和することができず、未接合部にひずみが集中した結果ボイドとして残るものと考えられる。こうしたボイドは基板温度の不均一性により強固に接合した部分がランダムに作られたときにも発生する。

【0012】したがって、ボイドを発生させずにシリコン基板を接合させるためには一点より接合をすることが有効である。その方法として、図3に示すように接触が完了したシリコン基板5を石英やセラミクス等熱伝導率が比較的小さい2枚の板6および6'で挟み、これらの板の背後の基板中央を加熱することが有効である。こうした手段により2枚のシリコン基板は中央より徐々に加熱され、強固な接合部が中央より周辺に広がりボイドの発生が抑えられる。

【0013】他の方法として図4に示すように、接触させたシリコン基板8を搬送ローラ10によって細長い加熱手段9、9'の短辺方向に搬送させ、基板の端より徐々に強固な接合部を形成する方法がある。遮蔽板12および冷却ローラ11は未接合部への熱伝導を低下させることにより温度上昇部を制御する働きをする。図3、図4いずれの方法においても加熱手段を上下2組設置することにより、2枚の基板の温度差をできるだけ小さくしている。また、図4に示した方法においては基板を搬送するかわりに加熱手段を基板の端より移動させても同様の効果が期待できる。

【0014】

【作用】本発明によれば、あらかじめ基板表面を疎水化処理しておくため、低温度でも強固な接合が可能となる。

【0015】また、前記疎水化処理は、フッ酸、パーフルオロ酸により行なうことにより、疎水化処理を効果的に行なうことができる。

【0016】また、前記疎水化処理は、高真空中で基板表面に加速した不活性イオンを照射し、清浄なシリコン表面を形成した後、水素ガスを導入して基板表面を水素原子で終端することにより、基板表面の疎水化を完全にすることができる。

【0017】また、前記基板どうしを加圧下で接触させて接合する工程は、前記基板の中央部から順次接触させることにより、接合界面に基体等を含むことがなくなり、ボイドの発生を防止できる。

【0018】また、前記加熱処理は250℃～700℃で行なうことにより、十分な接合強度を得ることができる。

【0019】

【実施例】

【実施例1】2枚の(100)シリコン基板を2%フッ酸で表面疎水化処理し、ただちに図1の接触装置により5気圧のガス圧を印加しつつ、大気中で2枚のシリコン基板を接触させた。

【0020】つぎに大気中で2時間加熱して接合した。加熱温度（熱処理温度）は、図2に示した各温度とした。

【0021】こうして作製した接合試料の曲げ強度を測定した。図2は曲げ強度より算出した破壊時の界面せん断応力を図示したものである。同様の方法で測定したシリコン基板の破壊強度は55 kg/cm<sup>2</sup>であり、250℃で加熱すれば十分強固に接合されていることがわかった。

【0022】【実施例2】(100)シリコン基板を200℃で10分間紫外線処理し、基板表面の有機不純物を除去した後、フッ化アンモニウムでPH4に調整したバッファーフッ酸で疎水化処理した。

【0023】その後実施例1と同様に2枚の基板を接触させた後、加熱処理を行った。

【0024】実施例1と同様にして強度を測定したところ、同等の強度で接合することが確かめられた。

【0025】【比較例】(100)シリコン基板を親水化処理し、実施例1と同様に接触、加熱処理をした試料の接合強度を測定したところ、図2に示したように、600℃以上では強固に接合したが、低温では十分な強度が得られなかった。また、400℃以下の場合、ダイシングソー切断時において接合面で剥離した。

【0026】【実施例3】2枚の(100)シリコン基板を85℃の硫酸および過酸化水素混合水溶液中に5分浸漬した後、10分間純水により洗浄した。ひきつづき、2%フッ酸水溶液で20秒間疎水化処理を行い、2分間純水洗浄した。以上の前処理を施した2枚のシリコン基板を図1に示した接触装置により5気圧を印加しつつ接触させた。次に図3に概略を示すように、接触した2枚のシリコン基板5を2枚のアルミナセラミクス板6、6'に挟み、このアルミナセラミクス板の中央部を加熱温度が500℃となるようにヒータ7、7'により加熱した。

【0027】以上のように接合した2枚のシリコン基板に赤外線を照射し、透過光を赤外線カメラにより観察したところ、ボイドの発生は見られなかった。また、破壊

5

時のせん断応力は  $85 \text{ kg/cm}^2$  であり十分な強度をもつことが確認された。

【0028】【実施例4】2枚の(100)シリコン基板を酸素雰囲気中で  $200^\circ\text{C}$  に加熱しながら、紫外線を20分間照射したのち、2%フッ酸水溶液で20秒間疎水化処理を行い、2分間純水洗浄した。以上の疎水化処理を施した2枚のシリコン基板を図1に示した接触装置により5気圧を印加しつつ接触させた。次に図4に概略を示す試料搬送装置を有する加熱装置により接触したシリコン基板8を加熱した。図4において、10は搬送ローラ、11は水冷されたローラであり、12は熱遮蔽板である。シリコン基板8は矢印方向に移動する過程で熱遮蔽板12の中央部に設置されたヒータ9、9'により加熱される。シリコン基板のヒータ直下部分は温度上昇するが、そこからはなれた部分は水冷ローラにより熱が遮断され低温に保たれるため、強固な接合は起こらない。本実施例においてはヒータ直下でのシリコン基板温度が  $550^\circ\text{C}$  となるようにヒータ電力を調整した。

【0029】以上のように接合したシリコン基板を実施例3と同様に赤外線カメラで観察したがボイドの発生は見られなかった。また、破壊時のせん断応力は  $91 \text{ kg/cm}^2$  であった。

【0030】

【発明の効果】以上説明したように、本発明の接合方法は、従来に比べ低温でシリコン基板の強固な接合を可能\*

6

＊にする効果が得られる。また、本発明の方法によれば、低温で接合可能であるため、素子形成後のシリコン基板どうしも接合することができ、マイクロマシン等の立体構造体の形成に有効な手段を提供することができる。

【0031】また、積層構造の熱膨張差による膜はがれや、ボイドの発生等も、少なくすることができるため、品質や、信頼性も向上できる。

【図面の簡単な説明】

【図1】本発明で基板の接触に使用した装置の概略図

【図2】曲げ強度より算出した実施例と比較例の破壊時の界面せん断応力の図

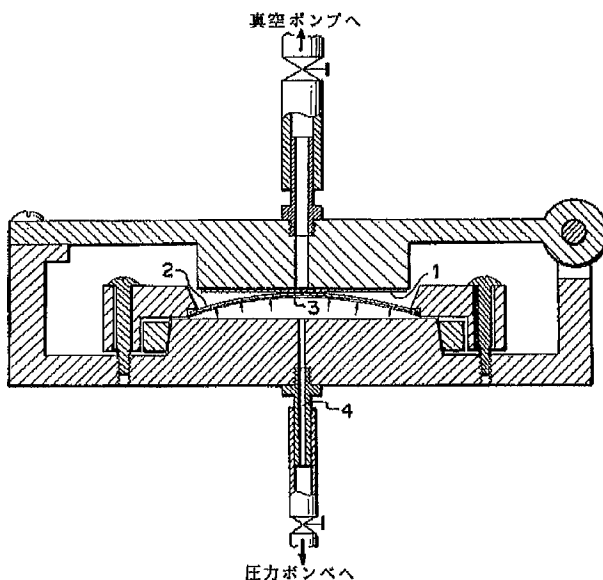
【図3】実施例3で用いた加熱方法の概略図

【図4】実施例4で用いた加熱装置の概略図

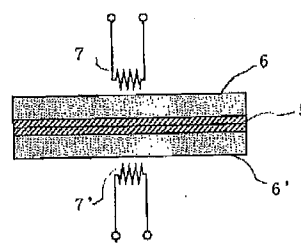
【符号の説明】

- 1 第1の基板
- 2 第2の基板
- 3 メンブレン
- 4 流体導入口
- 5、8 接触させたシリコン基板
- 6、6' セラミクス板
- 7、7'、9、9' 加熱手段
- 10 搬送ローラ
- 11 水冷ローラ
- 12 熱遮蔽板

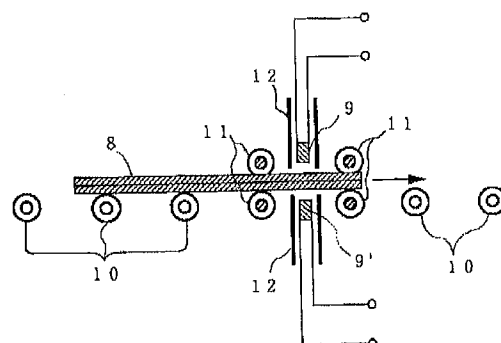
【図1】



【図3】

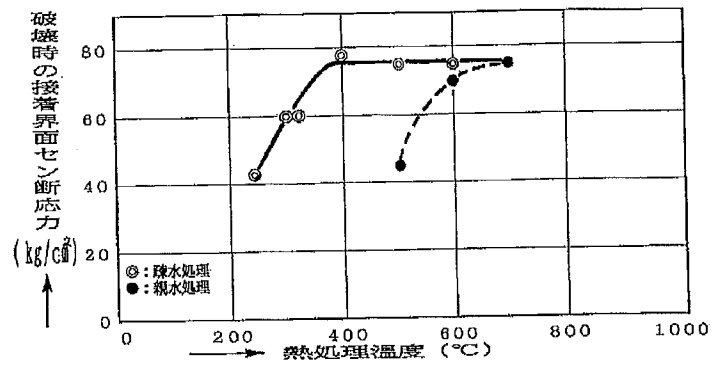


【図4】





【図2】



(11)Publication number 08-195334  
(43)Date of publication of application 30.07.1996  
(51)Int.Cl. H01L 21/02  
H01L 21/308  
H01L 27/12

(21)Application number 07-040398  
(22)Date of filing 28.02.1995  
(71)Applicant CANON INC  
(72)Inventor TAKAGI HIROTSUGU  
AKAIKE MASATAKE  
YAGI TAKAYUKI

---

(30)Priority

Priority number :06283470 Priority date :17.11.1994 Priority country :JP

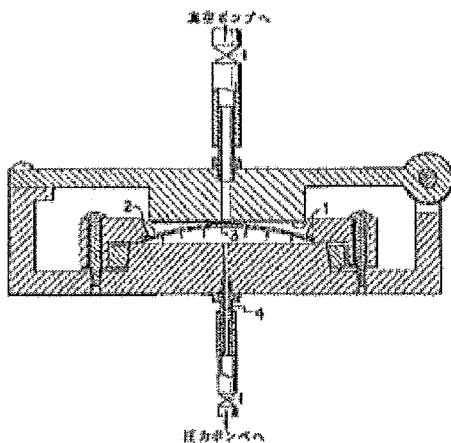
---

(54)METHOD FOR BONDING SILICON SUBSTRATE

(57)Abstract

PURPOSE: To firmly bond silicon substrates at low temperature, to utilize materials which cannot stand high temperature and to prevent films from separating and voids from being produced.

CONSTITUTION: The method comprises the steps of hydrophobing the surfaces of silicon substrates 1 and 2, contacting both hydrophobed silicon substrates, press-bonding them, and heating them to strengthen the bond. And the press-bonding step, the substrates 1 and 2 are brought into contact from the central portions of the substrates 1 and 2 to the peripheries.



## CLAIMS

[Claim(s)]

[Claim 1]A joining method of a silicon substrate characterized by comprising the following.

A process of carrying out hydrophobing processing of the silicon substrate surface.

A process which the aforementioned substrates which carried out hydrophobing processing are contacted under application of pressure, and is joined, and its process of carrying out afterbaking processing and strengthening the aforementioned junction.

[Claim 2]A joining method of the silicon substrate according to claim 1, wherein the aforementioned hydrophobing processing removes a natural oxide film of the aforementioned substrate surface by fluoric acid.

[Claim 3]A joining method of the silicon substrate according to claim 1, wherein the aforementioned hydrophobing processing uses buffer fluoric acid.

[Claim 4]A joining method of the silicon substrate according to claim 1 after irradiating inactive ions accelerated to a substrate surface in a high vacuum and forming a pure silicon surface, wherein the aforementioned hydrophobing processing introduces hydrogen gas and carries out the termination of the substrate surface with a hydrogen atom.

[Claim 5]A joining method of the silicon substrate according to claim 1 contacting sequentially a process which the aforementioned substrates are contacted under application of pressure, and is joined from a central part of the aforementioned substrate.

[Claim 6]A joining method of the silicon substrate according to claim 1 performing the aforementioned heat-treatment at 250 degrees C - 700 degrees C.

[Claim 7]A joining method of the silicon substrate according to claim 1 carrying out temperature rise of the aforementioned heat-treatment from a center of the aforementioned silicon substrate.

[Claim 8]A joining method of the silicon substrate according to claim 1 carrying out temperature rise of the aforementioned heat-treatment from an end of the aforementioned silicon substrate.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]The present invention relates to the manufacturing method of a semiconductor substrate, and relates especially to the joining method of silicon substrates.

[0002]

[The conventional method] Junction of silicon substrates is technology indispensable to production of a SOI (Silicon on Insulator) substrate. A method of carrying out contact afterbaking of the substrate which heated or carried out hydrophilization treatment of the substrate in an oxidizing atmosphere after contacting is used so that junction of silicon substrates may be conventionally looked at by JP,S39-17869,A or JP,S62-27040,A.

A substrate is joined via an oxidizing zone.

[0003]

[Problem to be solved by the invention]However, in an old method, in order to acquire firm junction, it is necessary to heat at around 1000 degrees C after contact. Therefore, when the element is formed on the substrate before junction, in order to bear such an elevated temperature, there is a problem that the material to be used is restricted extremely.

[0004]There is also a problem that film peeling occurs according to the thermal expansion difference of class material in the laminated structure. The gas emitted by drying disassembly of the hydroxyl group of a substrate surface remained easily as a void again, and the conventional method also had the problem of this making bonding strength be deteriorated.

[0005](The object of invention) There is the object of this invention in supposing that materials other than the material which is in enabling firm junction by low temperature treatment, and bears an elevated temperature by this are also available, and also preventing film peeling and generating of a void in the joining process of a silicon substrate.

[0006]

[Means for solving problem]The joining method of the silicon substrate of the present invention is characterized by hydrophobing down stream processing of a silicon substrate surface, and having three processes of the contact process of substrates while pressurizing, and a heat-treatment process as above-mentioned The means for solving a technical problem.

[0007]First, hydrophobing of a silicon surface is typically performed by removing the natural oxide film of the surface by fluoric acid. The termination of most silicon surfaces is carried out by fluoric acid processing with a hydrogen atom. The concentration of the fluoric acid used is 10 % by weight or less, and 1 to 5% of fluoric acid processing is suitable for hydrophobing processing. The buffer fluoric acid which adjusted PH to 3-6 may be used. Processing which removes impurities, such as an organic matter which has adhered to the substrate surface before fluoric acid processing, may be carried out. In this case, processing which forms unevenness in a substrate surface must be avoided. After irradiating the inactive ions accelerated to the substrate surface in the high vacuum besides the above-mentioned fluoric acid processing as a hydrophobing processing method and forming a pure silicon surface, hydrogen gas is introduced into a vacuum chamber and there is the method of carrying out the termination of the substrate surface with a hydrogen atom.

[0008]Next, the substrate of two sheets by which hydrophobing processing was carried out is contacted while applying a pressure. Fig.1 is a schematic view of the equipment used for contact of a substrate by the present invention. This equipment holds the first substrate 1 evenly, introduces the fluid (either a liquid or a gas is OK) pressurized from the fluid introducing port 4, and it makes the substrate of two sheets approach, applying this hydrostatic pressure to the back surface of the second substrate 2. Since hydrostatic pressure is applied to the thin membrane 3 and this membrane is bent by the equipment of Fig.1 in sphere form, the 2nd substrate 2 that touches it is also bent by it in sphere form. When the 2nd substrate 2 bends, the substrate of two sheets contacts from each central part. Since a controlled atmosphere is driven out by the periphery in a contact process in this contact method, into the atmosphere, gas does not have a residual thing [ carrying out ] between substrates. Of course, the substrate of two sheets may be contacted in a vacuum. If, as for hydrostatic pressure, there is more than 3 kg/cm<sup>2</sup>, it is effective enough.

[0009]Next, it heats in order to strengthen junction of the silicon substrate of two sheets which contacted. In the present invention, if the heating temperature is 250 degrees C or more, practically sufficient bonding strength will be obtained, but 300 degrees C - 700 degrees C, if it is 500-700 degrees C still more preferably, the firm junction which is equal to the conventional method will be attained. The temperature rise of the joined substrate is carried out by heating means, such as heater heating and lamp heating. Restriction may not be in junction and any may be sufficient as the atmosphere under heating among the atmosphere, inactive gas, and a vacuum.

[0010]The effect to heat is guessed as follows. When the hydrogen atom which is sticking to a silicon substrate surface by heating disconnects itself, The silicon atoms in the substrate outermost surface couple directly, or a hydrogen atom and the oxygen atom in the atmosphere place and change, and when a silicon atom joins together via an oxygen atom, junction of the silicon substrate of two sheets is performed.

[0011]In the increasing process of the bonding strength under heating, when a strong combination progresses from a substrate periphery, a hole (void) may often occur in the central part of the substrate. It is thought that the portion once joined firmly remains as a void as a result of being unable to ease a strain but a strain concentrating on an unsealed part. Such a void occurs, also when the portion firmly joined by the heterogeneity of substrate temperature is made at random.

[0012]Therefore, in order to join a silicon substrate, without generating a void, joining from one point is effective. It is effective to pinch the silicon substrate 5 which contact completed as the method, by the board 6 and 6' which are two sheets whose thermal conductivity, such as quartz and ceramics, is comparatively small, as shown in Fig.3, and to heat the center of a substrate of these boards in back. The silicon substrate of two sheets is gradually heated from a center by such a means, a firm junction spreads on a periphery from a center, and generating of a void is suppressed.

[0013]As shown in Fig.4 as other methods, the short side direction of the long and slender heating means 9 and 9' is made to convey the contacted silicon substrate 8 with the conveying roller 10, and there is the method of forming a firm junction gradually from the end of a substrate. The shield 12 and the cooling roller 11 serve to control a temperature rise part by making heat conduction to an unsealed part be deteriorated. The temperature gradient of the substrate of two sheets is made as small as possible by 2 sets of upper and lower sides installing a heating means also in which method of Fig.3 and Fig.4. The same effect is expectable even if it moves a heating means from the end of a

substrate instead of conveying a substrate in the method shown in Fig.4.

[0014]

[Function]According to the present invention, in order to carry out hydrophobing processing of the substrate surface beforehand, firm joining becomes possible also for low temperature.

[0015]Hydrophobing processing can be effectively performed by performing the aforementioned hydrophobing processing by fluoric acid and buffer fluoric acid.

[0016]After the aforementioned hydrophobing processing irradiates the inactive ions accelerated to the substrate surface in the high vacuum and forms a pure silicon surface, it can carry out hydrophobing of a substrate surface completely by introducing hydrogen gas and carrying out the termination of the substrate surface with a hydrogen atom.

[0017]By making it contact sequentially from the central part of the aforementioned substrate, it is lost that a base substance etc. are included of the process which the aforementioned substrates are contacted under application of pressure, and is joined in a bonding interface, and it can prevent generating of a void.

[0018]Sufficient bonding strength can be obtained by performing the aforementioned heat-treatment at 250 degrees C - 700 degrees C.

[0019]

[Working example]

[Working example 1] The silicon substrate of two sheets was contacted in the atmosphere, carrying out surface hydrophobing processing of (100) the silicon substrate of two sheets by fluoric acid 2%, and applying 5-atmosphere gas pressure with the contactor of Fig.1 immediately.

[0020]Next, in the atmosphere, it heated for 2 hours and joined. Heating temperature (heat treatment temperature) was made into each temperature shown in Fig.2.

[0021]In this way, the flexural strength of the produced junction sample was measured. Fig.2 illustrates the interface shearing stress at the time of the destruction computed from flexural strength. The disruptive strength of the silicon substrate measured in the similar way was 55 kg/cm<sup>2</sup>, and when heating at 250 degrees C, it turned out that it is joined sufficiently firmly.

[0022][Working example 2] (100) After carrying out ultraviolet treatment of the silicon substrate for 10 minutes at 200 degrees C and removing the organic impurities of a substrate surface, hydrophobing processing was carried out by the buffer fluoric acid adjusted to PH4 with ammonium fluoride.

[0023]Heat-treatment was performed after contacting the substrate of two sheets like the working example 1 after that.

[0024]When strength was measured like the working example 1, joining by equivalent strength was confirmed.

[0025][Comparative example] (100) Hydrophilization treatment of the silicon substrate was carried out, when the bonding strength of the sample which carried out contact and heat-treatment like the working example 1 was measured, as shown in Fig.2, above 600 degrees C, it joined firmly, but strength sufficient at low temperature was not obtained. In the case of 400 degrees C or less, it exfoliated in the plane of composition at the time of dicing saw cutting.

[0026][Working example 3] After (100) the silicon substrate of two sheets was immersed for 5 minutes into sulfuric acid and a hydrogen peroxide mixed aqueous solution of 85 degrees C, pure

water washed for 10 minutes. It pulled and continued, and performed and carried out pure water washing of the hydrophobing processing for 2 minutes for 20 seconds in the 2% fluoric acid aqueous solution. It was made to contact, applying 5 atmospheres with the contactor which showed the silicon substrate of two sheets which pretreated more than to Fig.1. Next, as an outline was shown in Fig.3, the two alumina ceramic boards 6 and 6' pinched the silicon substrate 5 of two sheets which contacted, and the central part of this alumina ceramic board was heated by the heater 7 and 7' so that heating temperature might be 500 degrees C.

[0027]Generating of the void was not seen, when infrared rays were irradiated to the silicon substrate of two sheets joined as mentioned above and the transmitted light was observed with the infrared camera. The shearing stress at the time of destruction is 85 kg/cm<sup>2</sup>, and having sufficient strength was checked.

[0028][Working example 4] After irradiating ultraviolet rays for 20 minutes, heating (100) the silicon substrate of two sheets at 200 degrees C in oxygen environment, pure water washing of the hydrophobing processing was performed and carried out for 2 minutes for 20 seconds in the 2% fluoric acid aqueous solution. It was made to contact, applying 5 atmospheres with the contactor which showed the silicon substrate of two sheets which performed the above hydrophobing processing to Fig.1. Next, the silicon substrate 8 which contacted with the heating apparatus which has a sample conveying machine which shows an outline to Fig.4 was heated. In Fig.4, 10 is a roller for conveyance, and the roller with which 11 was water-cooled, and 12 is a heat shielding plate. The silicon substrate 8 is heated by the heater 9 installed in the central part of the thermal shield version 12 in the process in which it moves to an arrow direction, and 9'. Although temperature rise of the part for the heater direct lower part of a silicon substrate is carried out, since heat is intercepted with a water-cooled roller and the portion which got used from there is maintained at low temperature, firm junction does not take place. Heater power was adjusted so that the silicon substrate temperature directly under a heater might be 550 degrees C in this example.

[0029]Generating of the void was not seen although the silicon substrate joined as mentioned above was observed with the infrared camera like the working example 3. The shearing stress at the time of destruction was 91 kg/cm<sup>2</sup>.

[0030]

[Effect of the Invention]As described above, the effect that the joining method of the present invention enables firm junction of a silicon substrate at low temperature compared with the former is acquired. According to the method of the present invention, since it is joinable at low temperature, the silicon substrates after element formation can be joined and a means effective in formation of spacial configuration objects, such as a micromachine, can be provided.

[0031]Since film peeling by the thermal expansion difference of a laminated structure, generating of a void, etc. can be lessened, quality and reliability can also improve.

(11)Publication number 08-195334  
(43)Date of publication of application 30.07.1996  
(51)Int.Cl. H01L 21/02  
H01L 21/308  
H01L 27/12

(21)Application number 07-040398  
(22)Date of filing 28.02.1995  
(71)Applicant CANON INC  
(72)Inventor TAKAGI HIROTSUGU  
AKAIKE MASATAKE  
YAGI TAKAYUKI

---

**(30)Priority**

Priority number : 06283470 Priority date : 17.11.1994 Priority country : JP

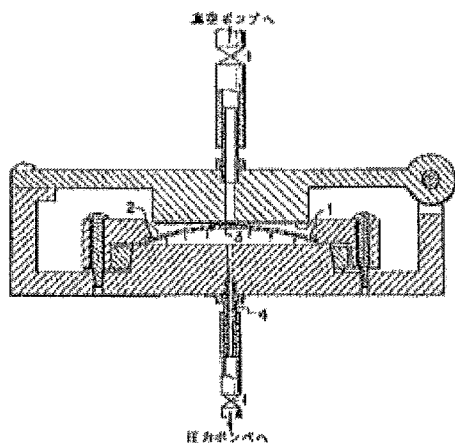
---

**(54)METHOD FOR BONDING SILICON SUBSTRATE**

**(57)Abstract**

PURPOSE: To firmly bond silicon substrates at low temperature, to utilize materials which cannot stand high temperature and to prevent films from separating and voids from being produced.

CONSTITUTION: The method comprises the steps of hydrophobing the surfaces of silicon substrates 1 and 2, contacting both hydrophobed silicon substrates, press-bonding them, and heating them to strengthen the bond. And the press-bonding step, the substrates 1 and 2 are brought into contact from the central portions of the substrates 1 and 2 to the peripheries.





## CLAIMS

[Claim(s)]

[Claim 1]A joining method of a silicon substrate characterized by comprising the following.

A process of carrying out hydrophobing processing of the silicon substrate surface.

A process which the aforementioned substrates which carried out hydrophobing processing are contacted under application of pressure, and is joined, and its process of carrying out afterbaking processing and strengthening the aforementioned junction.

[Claim 2]A joining method of the silicon substrate according to claim 1, wherein the aforementioned hydrophobing processing removes a natural oxide film of the aforementioned substrate surface by fluoric acid.

[Claim 3]A joining method of the silicon substrate according to claim 1, wherein the aforementioned hydrophobing processing uses buffer fluoric acid.

[Claim 4]A joining method of the silicon substrate according to claim 1 after irradiating inactive ions accelerated to a substrate surface in a high vacuum and forming a pure silicon surface, wherein the aforementioned hydrophobing processing introduces hydrogen gas and carries out the termination of the substrate surface with a hydrogen atom.

[Claim 5]A joining method of the silicon substrate according to claim 1 contacting sequentially a process which the aforementioned substrates are contacted under application of pressure, and is joined from a central part of the aforementioned substrate.

[Claim 6]A joining method of the silicon substrate according to claim 1 performing the aforementioned heat-treatment at 250 degrees C - 700 degrees C.

[Claim 7]A joining method of the silicon substrate according to claim 1 carrying out temperature rise of the aforementioned heat-treatment from a center of the aforementioned silicon substrate.

[Claim 8]A joining method of the silicon substrate according to claim 1 carrying out temperature rise of the aforementioned heat-treatment from an end of the aforementioned silicon substrate.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]The present invention relates to the manufacturing method of a semiconductor substrate, and relates especially to the joining method of silicon substrates.

[0002]

[The conventional method] Junction of silicon substrates is technology indispensable to production of a SOI (Silicon on Insulator) substrate. A method of carrying out contact afterbaking of the substrate which heated or carried out hydrophilization treatment of the substrate in an oxidizing atmosphere after contacting is used so that junction of silicon substrates may be conventionally looked at by JP,S39-17869,A or JP,S62-27040,A.

A substrate is joined via an oxidizing zone.

[0003]

[Problem to be solved by the invention]However, in an old method, in order to acquire firm junction, it is necessary to heat at around 1000 degrees C after contact. Therefore, when the element is formed on the substrate before junction, in order to bear such an elevated temperature, there is a problem that the material to be used is restricted extremely.

[0004]There is also a problem that film peeling occurs according to the thermal expansion difference of class material in the laminated structure. The gas emitted by drying disassembly of the hydroxyl group of a substrate surface remained easily as a void again, and the conventional method also had the problem of this making bonding strength be deteriorated.

[0005](The object of invention) There is the object of this invention in supposing that materials other than the material which is in enabling firm junction by low temperature treatment, and bears an elevated temperature by this are also available, and also preventing film peeling and generating of a void in the joining process of a silicon substrate.

[0006]

[Means for solving problem]The joining method of the silicon substrate of the present invention is characterized by hydrophobing down stream processing of a silicon substrate surface, and having three processes of the contact process of substrates while pressurizing, and a heat-treatment process as above-mentioned The means for solving a technical problem.

[0007]First, hydrophobing of a silicon surface is typically performed by removing the natural oxide film of the surface by fluoric acid. The termination of most silicon surfaces is carried out by fluoric acid processing with a hydrogen atom. The concentration of the fluoric acid used is 10 % by weight or less, and 1 to 5% of fluoric acid processing is suitable for hydrophobing processing. The buffer fluoric acid which adjusted PH to 3-6 may be used. Processing which removes impurities, such as an organic matter which has adhered to the substrate surface before fluoric acid processing, may be carried out. In this case, processing which forms unevenness in a substrate surface must be avoided. After irradiating the inactive ions accelerated to the substrate surface in the high vacuum besides the above-mentioned fluoric acid processing as a hydrophobing processing method and forming a pure silicon surface, hydrogen gas is introduced into a vacuum chamber and there is the method of carrying out the termination of the substrate surface with a hydrogen atom.

[0008]Next, the substrate of two sheets by which hydrophobing processing was carried out is contacted while applying a pressure. Fig.1 is a schematic view of the equipment used for contact of a substrate by the present invention. This equipment holds the first substrate 1 evenly, introduces the fluid (either a liquid or a gas is OK) pressurized from the fluid introducing port 4, and it makes the substrate of two sheets approach, applying this hydrostatic pressure to the back surface of the second substrate 2. Since hydrostatic pressure is applied to the thin membrane 3 and this membrane is bent by the equipment of Fig.1 in sphere form, the 2nd substrate 2 that touches it is also bent by it in sphere form. When the 2nd substrate 2 bends, the substrate of two sheets contacts from each central part. Since a controlled atmosphere is driven out by the periphery in a contact process in this contact method, into the atmosphere, gas does not have a residual thing [ carrying out ] between substrates. Of course, the substrate of two sheets may be contacted in a vacuum. If, as for hydrostatic pressure, there is more than 3 kg/cm<sup>2</sup>, it is effective enough.

[0009]Next, it heats in order to strengthen junction of the silicon substrate of two sheets which contacted. In the present invention, if the heating temperature is 250 degrees C or more, practically sufficient bonding strength will be obtained, but 300 degrees C - 700 degrees C, if it is 500-700 degrees C still more preferably, the firm junction which is equal to the conventional method will be attained. The temperature rise of the joined substrate is carried out by heating means, such as heater heating and lamp heating. Restriction may not be in junction and any may be sufficient as the atmosphere under heating among the atmosphere, inactive gas, and a vacuum.

[0010]The effect to heat is guessed as follows. When the hydrogen atom which is sticking to a silicon substrate surface by heating disconnects itself, The silicon atoms in the substrate outermost surface couple directly, or a hydrogen atom and the oxygen atom in the atmosphere place and change, and when a silicon atom joins together via an oxygen atom, junction of the silicon substrate of two sheets is performed.

[0011]In the increasing process of the bonding strength under heating, when a strong combination progresses from a substrate periphery, a hole (void) may often occur in the central part of the substrate. It is thought that the portion once joined firmly remains as a void as a result of being unable to ease a strain but a strain concentrating on an unsealed part. Such a void occurs, also when the portion firmly joined by the heterogeneity of substrate temperature is made at random.

[0012]Therefore, in order to join a silicon substrate, without generating a void, joining from one point is effective. It is effective to pinch the silicon substrate 5 which contact completed as the method, by the board 6 and 6' which are two sheets whose thermal conductivity, such as quartz and ceramics, is comparatively small, as shown in Fig.3, and to heat the center of a substrate of these boards in back. The silicon substrate of two sheets is gradually heated from a center by such a means, a firm junction spreads on a periphery from a center, and generating of a void is suppressed.

[0013]As shown in Fig.4 as other methods, the short side direction of the long and slender heating means 9 and 9' is made to convey the contacted silicon substrate 8 with the conveying roller 10, and there is the method of forming a firm junction gradually from the end of a substrate. The shield 12 and the cooling roller 11 serve to control a temperature rise part by making heat conduction to an unsealed part be deteriorated. The temperature gradient of the substrate of two sheets is made as small as possible by 2 sets of upper and lower sides installing a heating means also in which method of Fig.3 and Fig.4. The same effect is expectable even if it moves a heating means from the end of a

substrate instead of conveying a substrate in the method shown in Fig.4.

[0014]

[Function]According to the present invention, in order to carry out hydrophobing processing of the substrate surface beforehand, firm joining becomes possible also for low temperature.

[0015]Hydrophobing processing can be effectively performed by performing the aforementioned hydrophobing processing by fluoric acid and buffer fluoric acid.

[0016]After the aforementioned hydrophobing processing irradiates the inactive ions accelerated to the substrate surface in the high vacuum and forms a pure silicon surface, it can carry out hydrophobing of a substrate surface completely by introducing hydrogen gas and carrying out the termination of the substrate surface with a hydrogen atom.

[0017]By making it contact sequentially from the central part of the aforementioned substrate, it is lost that a base substance etc. are included of the process which the aforementioned substrates are contacted under application of pressure, and is joined in a bonding interface, and it can prevent generating of a void.

[0018]Sufficient bonding strength can be obtained by performing the aforementioned heat-treatment at 250 degrees C - 700 degrees C.

[0019]

[Working example]

[Working example 1] The silicon substrate of two sheets was contacted in the atmosphere, carrying out surface hydrophobing processing of (100) the silicon substrate of two sheets by fluoric acid 2%, and applying 5-atmosphere gas pressure with the contactor of Fig.1 immediately.

[0020]Next, in the atmosphere, it heated for 2 hours and joined. Heating temperature (heat treatment temperature) was made into each temperature shown in Fig.2.

[0021]In this way, the flexural strength of the produced junction sample was measured. Fig.2 illustrates the interface shearing stress at the time of the destruction computed from flexural strength. The disruptive strength of the silicon substrate measured in the similar way was 55 kg/cm<sup>2</sup>, and when heating at 250 degrees C, it turned out that it is joined sufficiently firmly.

[0022][Working example 2] (100) After carrying out ultraviolet treatment of the silicon substrate for 10 minutes at 200 degrees C and removing the organic impurities of a substrate surface, hydrophobing processing was carried out by the buffer fluoric acid adjusted to PH4 with ammonium fluoride.

[0023]Heat-treatment was performed after contacting the substrate of two sheets like the working example 1 after that.

[0024]When strength was measured like the working example 1, joining by equivalent strength was confirmed.

[0025][Comparative example] (100) Hydrophilization treatment of the silicon substrate was carried out, when the bonding strength of the sample which carried out contact and heat-treatment like the working example 1 was measured, as shown in Fig.2, above 600 degrees C, it joined firmly, but strength sufficient at low temperature was not obtained. In the case of 400 degrees C or less, it exfoliated in the plane of composition at the time of dicing saw cutting.

[0026][Working example 3] After (100) the silicon substrate of two sheets was immersed for 5 minutes into sulfuric acid and a hydrogen peroxide mixed aqueous solution of 85 degrees C, pure

water washed for 10 minutes. It pulled and continued, and performed and carried out pure water washing of the hydrophobing processing for 2 minutes for 20 seconds in the 2% fluoric acid aqueous solution. It was made to contact, applying 5 atmospheres with the contactor which showed the silicon substrate of two sheets which pretreated more than to Fig.1. Next, as an outline was shown in Fig.3, the two alumina ceramic boards 6 and 6' pinched the silicon substrate 5 of two sheets which contacted, and the central part of this alumina ceramic board was heated by the heater 7 and 7' so that heating temperature might be 500 degrees C.

[0027]Generating of the void was not seen, when infrared rays were irradiated to the silicon substrate of two sheets joined as mentioned above and the transmitted light was observed with the infrared camera. The shearing stress at the time of destruction is 85 kg/cm<sup>2</sup>, and having sufficient strength was checked.

[0028][Working example 4] After irradiating ultraviolet rays for 20 minutes, heating (100) the silicon substrate of two sheets at 200 degrees C in oxygen environment, pure water washing of the hydrophobing processing was performed and carried out for 2 minutes for 20 seconds in the 2% fluoric acid aqueous solution. It was made to contact, applying 5 atmospheres with the contactor which showed the silicon substrate of two sheets which performed the above hydrophobing processing to Fig.1. Next, the silicon substrate 8 which contacted with the heating apparatus which has a sample conveying machine which shows an outline to Fig.4 was heated. In Fig.4, 10 is a roller for conveyance, and the roller with which 11 was water-cooled, and 12 is a heat shielding plate. The silicon substrate 8 is heated by the heater 9 installed in the central part of the thermal shield version 12 in the process in which it moves to an arrow direction, and 9'. Although temperature rise of the part for the heater direct lower part of a silicon substrate is carried out, since heat is intercepted with a water-cooled roller and the portion which got used from there is maintained at low temperature, firm junction does not take place. Heater power was adjusted so that the silicon substrate temperature directly under a heater might be 550 degrees C in this example.

[0029]Generating of the void was not seen although the silicon substrate joined as mentioned above was observed with the infrared camera like the working example 3. The shearing stress at the time of destruction was 91 kg/cm<sup>2</sup>.

[0030]

[Effect of the Invention]As described above, the effect that the joining method of the present invention enables firm junction of a silicon substrate at low temperature compared with the former is acquired. According to the method of the present invention, since it is joinable at low temperature, the silicon substrates after element formation can be joined and a means effective in formation of spacial configuration objects, such as a micromachine, can be provided.

[0031]Since film peeling by the thermal expansion difference of a laminated structure, generating of a void, etc. can be lessened, quality and reliability can also improve.

# 公告本

389965

申請日期	87.12.31
案 號	87121975
類 別	H01L 21/324

A4  
C4

389965

(以上各欄由本局填註)

發 明 專 利 說 明 書		
一、發明 名稱	中 文	以三氟化氮退火處理製程改善開極氧化層可靠度之方法
	英 文	
二、發明人 創作	姓 名	(1)趙 天 生 (2)雷 添 福 (3)張 子 云 (4)周 宗 賢 (5)陳 希 寬
	國 籍	(1)、(2)、(3)、(4) 中華民國 (5) 美 國
	住、居所	(1)新竹市國後街七二巷五號四樓 (2)新竹市建中一路三七號七樓之一 (3)新竹縣新埔鎮新埔里中正路三五九巷六號 (4)新竹縣竹北市泰和里泰和路二一號 (5)美國賓夕凡尼亞州錫安斯維市耶克爾斯·米爾路六九八一號
三、申請人	姓 名 (名稱)	三福化工股份有限公司
	國 籍	中華民國
	住、居所 (事務所)	台北市中山北路二段廿一號五樓
	代 表 人 姓 名	張 純 明

經濟部中央標準局員工消費合作社印製

本紙張尺度適用中國國家標準 (CNS) A4規格 (210×297公釐)

(由本局填寫)

承辦人代碼：
大 類：
I P C 分類：

A6  
B6

本案已向：

國(地區) 申請專利 申請日期： 案號： ☐有 ☐無主張優先權  
本案無向國外申請專利

有關微生物已寄存於：

，寄存日期：

，寄存號碼：

(請先閱讀背面之注意事項再填寫本頁各欄)

裝

訂

線

經濟部中央標準局員工消費合作社印製

本紙張尺度適用中國國家標準 (CNS) A4規格 (210×297公釐)

## 五、發明說明 ( 1 )

### [ 發明之範圍 ]

本發明係關於一種改善閘極氧化層可靠度的方法，特別是利用三氟化氮 ( $\text{NF}_3$ ) 對閘極退火處理的製程，以降低閘極漏電流的方法。

### [ 發明之背景 ]

隨著半導體元件的縮小 (scale down)，閘極氧化層 (gate oxide) 的可靠度也變得更為重要，如何獲得高可靠度的閘極氧化層就變成當今最重要的問題。閘極 (gate) 漏電流 (leakage current) 是一個判斷閘極氧化層優劣的主要因素，尤其是在 FN 穿透 (F-N tunneling) 前低電場下的漏電流。因此，如何得到一個低漏電流的閘極氧化層便成為當今主要的問題。

目前有幾項技術可增進閘極氧化層的品質，例如，在形成氧化層的同時通入少量的氟 (F)，使其與氧氣同時在矽晶圓上反應；又如，使用氮離子佈植 (ion implantation) 在多晶矽閘極 (poly-Si-gate)，對於閘極氧化層的品質也有所改善。

而就另一方面來說，在深次微米的製程中，如何減低閘極的電阻也是一個重要的關鍵。傳統的鈦矽化物 (Ti-silicide) 雖可以有效的降低閘極電阻，但其在閘極線寬變窄後，其電阻值也會隨之而變大。鈷矽化物 (Co-silicide) 是一個取代的方法，因為鈷矽化物的電阻值不會因線寬的變窄而變大；但鈷矽化物又存在著另一個問題，其漏電流太大。

(請先閱讀背面之注意事項再填寫本頁)

訂



## 五、發明說明(2)

### [發明之目的與概述]

本發明之目的在於，提供一種改善閘極氧化層可靠度的方法，特別是利用三氟化氮( $\text{NF}_3$ )對閘極氧化層做退火處理的製程，其可顯著改善閘極氧化層的漏電流及崩潰電場。

本發明之另一目的在於，提供一種改善閘極氧化層可靠度的方法，特別是利用三氟化氮( $\text{NF}_3$ )對閘極氧化層做退火處理的製程，其可有效減少因形成閘極銻矽化物而來的漏電流。

本發明之以三氟化氮退火處理製程改善閘極氧化層可靠度之方法，係一項結合氮、氟優點的技術來改善閘極氧化層的可靠度，其係以三氟化氮( $\text{NF}_3$ )對多晶矽(poly-Si)閘極作退火(annealing)處理，使氟化矽( $\text{Si-F}$ )與氮化矽( $\text{Si-N}$ )的鍵結在二氧化矽與矽晶圓的界面( $\text{SiO}_2/\text{Si interface}$ )中產生，此種較強的鍵結會取代較弱的鍵結，例如氫化矽( $\text{Si-H}$ )與氫氧化矽( $\text{Si-OH}$ )，而使得氧化層的可靠度增強。

### [附圖之簡要說明]

圖1係為本發明製程之一實施例之試片製作流程圖。

圖2係為不同退火時間的鋁電極試片之崩潰電場分佈圖。

圖3係為不同退火時間的鋁電極試片之漏電流分佈圖。

圖4係為以三氟化氮退火處理試片之二次離子分佈圖。

圖5係為本發明製程之另一實施例之試片製作流程圖。

圖6係為不同退火時間的銻矽化物電極試片之崩潰電場分佈圖。

(請先閱讀背面之注意事項再填寫本頁)

訂

### 五、發明說明(3)

圖7係為不同退火時間的銦矽化物電極試片之漏電流分佈圖。

#### [發明之詳細說明]

以下參照附圖說明本發明之實施例。

如圖1所示本發明製程之一實施例之試片製作流程圖，在P型(100)矽晶圓上製作一金氧半電容(MOS capacitor)，其步驟為：首先，以傳統爐管在晶圓上形成一層5000埃的阻隔氧化層(field oxide)，並蝕刻出一主動區(active region)。其次，在用氮氣稀釋的氧氣下( $N_2:O_2=10:1$ )，形成一約33埃厚的超薄氧化層(ultra-thin oxide)(該超薄氧化層的厚度並不限定於33埃，其範圍可為15至70埃)，並用低壓化學氣相沉積法(LPCVD)堆疊一層3000埃的多晶矽(poly-Si)。然後，在攝氏620度低壓的環境下，用三氟化氮( $NF_3$ )對多晶矽做不同時間(5至20分鐘)的退火處理。最後，以鋁做成閘極電極。

在上述以三氟化氮對多晶矽做退火處理的過程中，會有氟化矽(Si-F)與氮化矽(Si-N)的鍵結在二氧化矽與矽晶圓的界面( $SiO_2/Si$  interface)中產生，此種較強的鍵結會取代較弱的鍵結，例如氫化矽(Si-H)與氫氧化矽(Si-OH)，而使得氧化層的可靠度增強。如圖4所示，經由對三氟化氮退火處理的試片做二次離子分析(SIMS)，可確知在二氧化矽與矽晶圓的界面有氟與氮的鍵結形成。

圖2及圖3分別為不同退火時間之鋁電極試片的崩潰電場(breakdown field)及漏電流(leakage current)之統計分

(請先閱讀背面之注意事項再填寫本頁)

訂

## 五、發明說明(4)

佈圖，其中使用三氟化氮做退火處理的試片其崩潰電場皆比對照組試片高，且其漏電流亦皆比對照組試片低。

如圖5所示本發明製程之另一實施例之試片製作流程圖，其中，除了最後步驟係以鈷化矽做成閘極電極外，其餘步驟皆與前一實施例相同。圖6及圖7分別為不同退火時間之鈷化矽電極試片的崩潰電場及漏電流之統計分佈圖，其中使用三氟化氮做退火處理的試片其崩潰電場皆比對照組試片高，且其漏電流亦皆比對照組試片低。又，在此實施例中，以三氟化氮對鈷化矽電極試片做退火處理的時間之最佳化條件係為10分鐘。

綜上所述，以三氟化氮對多晶矽做退火處理，確可顯著改善氧化層的崩潰電場及漏電流，增進氧化層的可靠度。

本發明雖已參照附圖及實施例詳細說明，然其並不圖限於上述二實施例。任何依本發明之精神及申請專利範圍所做的變化及修改，仍應屬於本發明之範圍。

(請先閱讀背面之注意事項再填寫本頁)

訂

四、中文發明摘要(發明之名稱： 以三氟化氮退火處理製程改善閘極)  
氧化層可靠度之方法

本發明之以三氟化氮退火處理製程改善閘極氧化層可靠度之方法，係一項結合氮、氟優點的技術來改善閘極氧化層的可靠度，其係以三氟化氮( $\text{NF}_3$ )對多晶矽(poly-Si)閘極作退火(annealing)處理，使氟化矽( $\text{Si-F}$ )與氮化矽( $\text{Si-N}$ )的鍵結在二氧化矽與矽晶圓的界面( $\text{SiO}_2/\text{Si interface}$ )中產生，此種較強的鍵結會取代較弱的鍵結，例如氫化矽( $\text{Si-H}$ )與氫氧化矽( $\text{Si-OH}$ )，而使得氧化層的可靠度增強。

英文發明摘要(發明之名稱： )

(請先閱讀背面之注意事項再填寫本頁各欄)

裝

訂

線

## 六、申請專利範圍

1. 一種以三氟化氮退火處理製程改善閘極氧化層可靠度之方法，其具有下列主要步驟：

在晶圓上形成一阻隔氧化層 (field oxide)，並蝕刻一主動區 (active region)；

形成一超薄氧化層 (ultra-thin oxide)，並堆疊一層多晶矽 (poly-Si)；

以三氟化氮 ( $\text{NF}_3$ ) 對多晶矽作退火處理；及

形成閘極電極。

2. 如申請專利範圍第1項之方法，其中該超薄氧化層之厚度係為15至70埃。

3. 如申請專利範圍第1項之方法，其中該多晶矽係以低壓化學氣相沉積 (LPCVD) 堆疊。

4. 如申請專利範圍第1項之方法，其中該退火處理係於攝氏620度低壓的環境下進行。

5. 如申請專利範圍第1項之方法，其中該退火處理之時間係為5至20分鐘。

6. 如申請專利範圍第1項之方法，其中該閘極電極係為鋁電極。

7. 如申請專利範圍第1項之方法，其中該閘極電極係為鈷矽化物電極。

8. 如申請專利範圍第7項之方法，其中該退火處理之時間係以10分鐘為最佳。

(請先閱讀背面之注意事項再填寫本頁)

訂

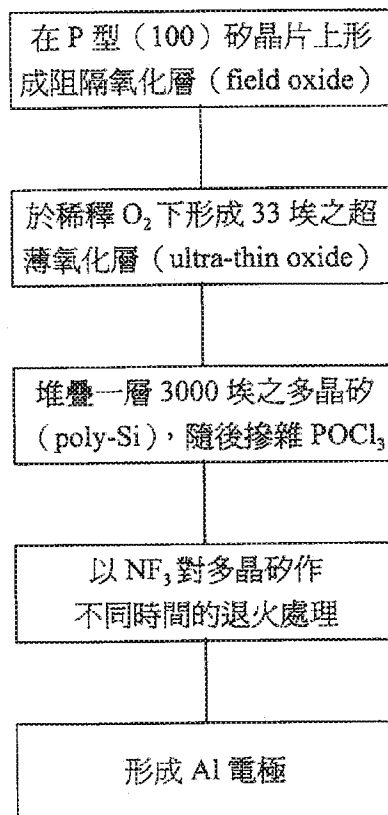


圖 1

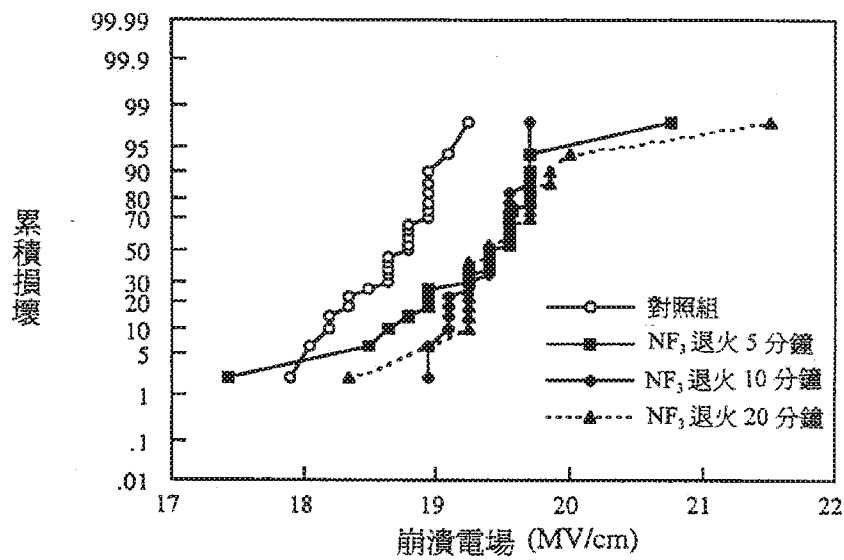


圖 2

389965

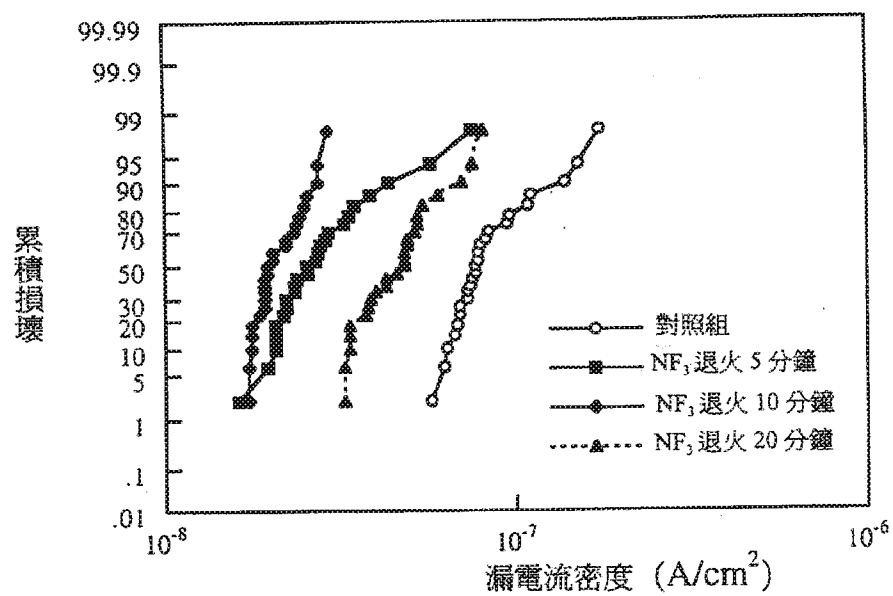


圖 3



389965

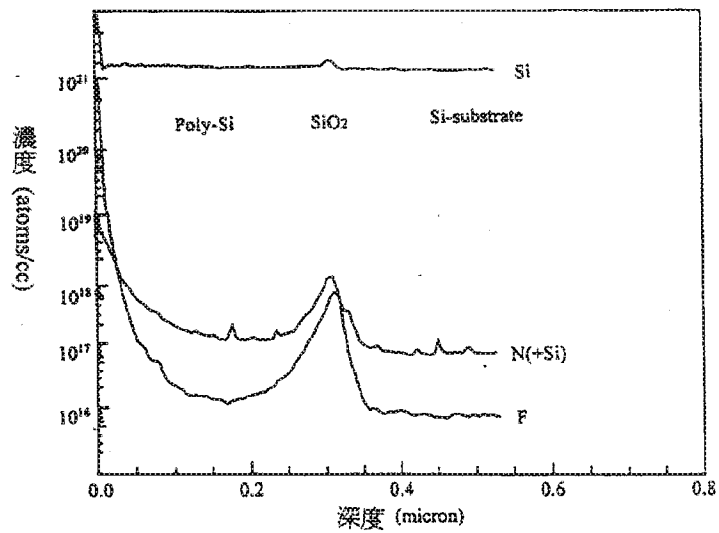


圖 4

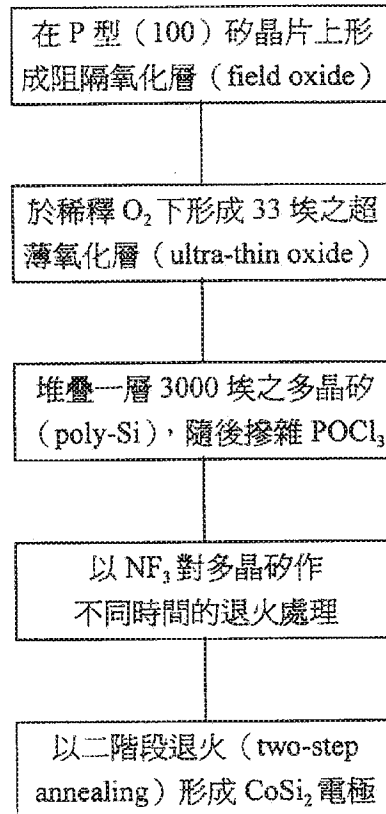


圖 5

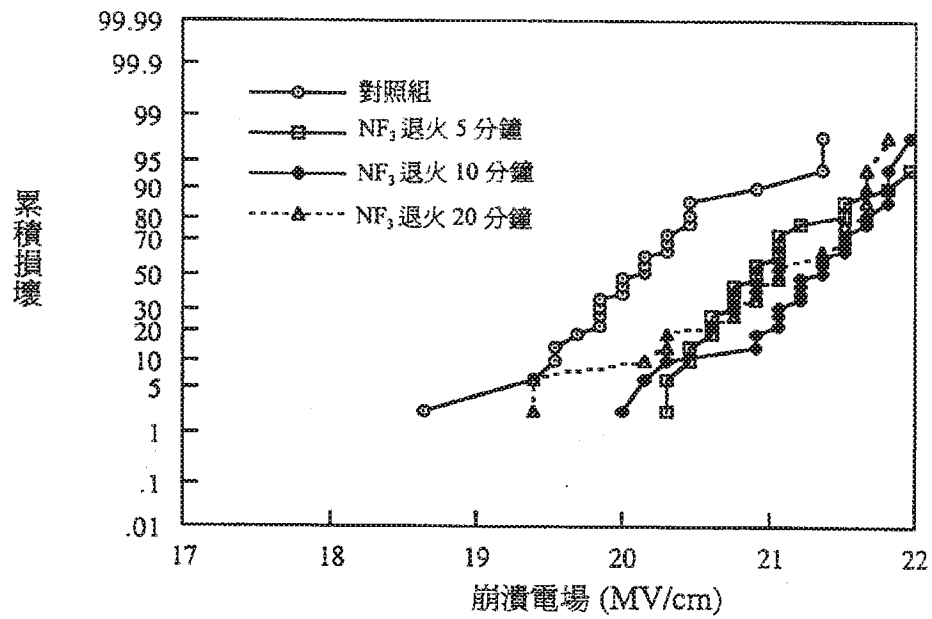


圖 6

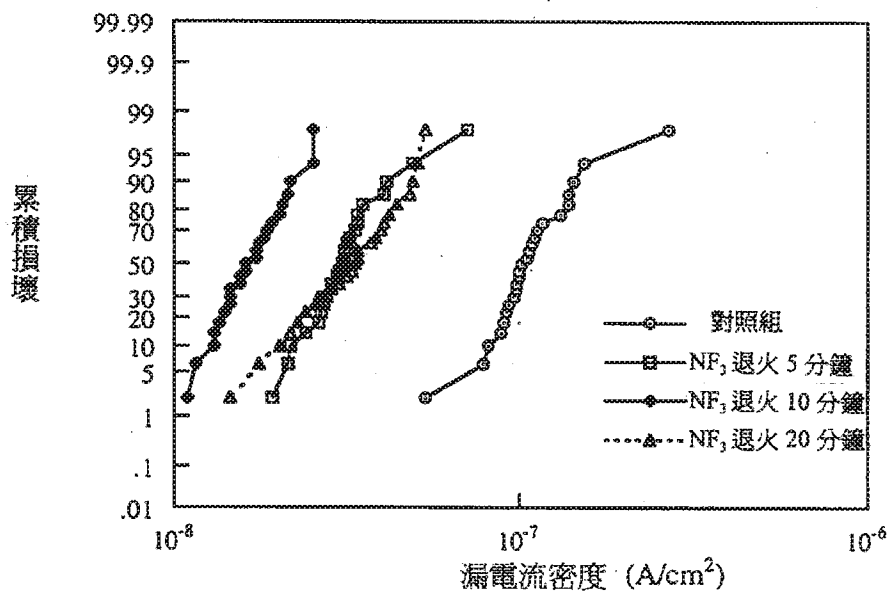


圖 7

1 TW389965B 2000-05-11 Method for improving reliability of a gate oxide layer by NF3 annealing (en)

2 (Electronic English Translation)

3 **English Abstract:**

4  
5  
6 This invention provides a method for improving reliability of a gate oxide layer by NF3 annealing, which  
7 combines the advantages of nitrogen and fluorine to enhance the reliability of the gate oxide layer. A  
8 polysilicon gate is annealed by using NF3 to produce Si-F and Si-N bonding at the Si/SiO2 interface. Such  
9 stronger bonding replaces the weaker bonding such as Si-H and Si-OH to enhance the reliability of the  
10 oxide layer.

11  
12 **English Description:**

13  
14  
15 **Technical Field**

16  
17 This invention is about a kind of improved gate method for reliable degree of the oxide layer, in  
18 particular through the use of nitrogen trifluoride (NF 3) the manufacturing process of treatment of the  
19 gate annealing, in order to reduce the gate leakage current method.

20  
21 **Background Art**

22  
23 Reduced along with the semiconductor element (scale down), the reliability of the gate oxide layer (gate  
24 oxide) has also become more important, how to obtain high-reliability of the gate oxide layer to become  
25 the most important issue. Gate (gate) leakage current (leakage current) is a judging gate oxide layer of  
26 the main factors, especially in the low electric field before penetrating FN (F-N tunneling) drain current.  
27 Therefore, how to get a low leakage current of the gate oxide layer will become a major problem today.

28  
29 There are currently several technology can improve the quality of the gate oxide layer, for example, at  
30 the same time forming the oxide layer of the inject a small amount of fluorine (F), the oxygen reaction  
31 on a silicon wafer at the same time; and if, the polycrystalline (ion implantation) using nitrogen ion  
32 implanter is [...] (poly-Si-gate), the quality of the gate oxide layer has also improved.

33  
34 On the other hand, in the deep sub-micron in the process of, how to reduce gate resistance is also an  
35 important key. Although traditional [...] compound (Ti-silicide) gate resistance can be reduced  
36 effectively, but the narrowing of the line width of the gate, its resistance will be thereupon and becomes  
37 larger. (Co-silicide) cobalt silicon compound is a substituted method, because the resistance of the  
38 cobalt silicon compound will not become great due to the narrowing of the line width; but the cobalt  
39 silicon compound also exists another problem works, its leakage current is too large.

40  
41 Summary of the Invention

42  
43 The purpose of this invention is to, provide a degree of improved gate method of the oxide layer, in  
44 particular through the use of nitrogen trifluoride (NF<sub>3</sub>) gate oxidation layer as the process of annealing,  
45 which can remarkably improve the leakage current of the gate oxide layer and collapse the electric field.

46  
47 Another purpose of this invention is to, provide a degree of improved gate method of the oxide layer, in  
48 particular through the use of nitrogen trifluoride (NF<sub>3</sub>) gate oxidation layer as the process of annealing,  
49 the formed can be effectively reduced to cobalt silicon compound gate leakage current.

50  
51 In the invention nitrogen trifluoride gate oxide layer to improve the process for preparing of annealing  
52 treatment method for reliability, is a combined nitrogen, fluoro the advantages of the technology to  
53 improve the reliability of the gate oxide layer, the nitrogen trifluoride (NF<sub>3</sub>) of the polycrystalline silicon  
54 (poly-Si) gate as the annealing treatment (annealing), the silicon nitride silicon fluoride with (Si-F) (Si-N)  
55 the bonding of the silicon wafer, the silicon dioxide interface (SiO<sub>2</sub>/Si interface) generated in, such  
56 strong the key ties the meeting substituted weaker bonding, for example with silicon hydroxide (Si-H)  
57 (Si-OH) [...], enhanced reliability of the oxide layer.

58  
59 Description of Drawings

60  
61 Figure 1 is the embodiment of the process of this invention one of the manufacturing flow chart of the  
62 test piece.

63  
64 Figure 2 is a different annealing time collapse of the aluminum electrode of the electric field distribution  
65 map of the test piece.

66  
67 Figure 3 is a different annealing time aluminum electrode of the leakage current distribution map of the  
68 test piece.

69  
70 Figure 4 is to nitrogen trifluoride annealing treatment test piece secondary ion distribution map of.

71  
72 Figure 5 is the manufacturing process for this invention another embodiment of the manufacturing flow  
73 chart of the test piece.

74  
75 Figure 6 is a different annealing time of the test piece of the electrode of the cobalt silicon compound  
76 collapse of the distribution of the electric field.

77  
78 Fig. 7 is a different annealing time of the cobalt silicon compound electrode leakage current distribution  
79 map of the test piece.

80  
81 (Detailed description of invention)

82  
83 By the following with reference to the embodiment of the present invention.

84  
85 As shown in Figure 1 one of the invention the embodiment of the test process of the manufacturing flow  
86 chart, in the P-type (100) silicon wafer (MOS capacitor) making a MOS capacitor, its steps are: first, to  
87 traditional furnace tube is formed on the wafer a layer of 5000 angstroms (field oxide) of the barrier  
88 oxide layer, and etching the active region (active region). Secondly, in a nitrogen-diluted oxygen (N<sub>2</sub>: O  
89 2 = 10:1), forming a approximately 33 angstroms thick ultra-thin oxide layer (ultra-thin oxide) (the ultra-  
90 thin the thickness of the oxide layer does not defines in 33 heydon, its range can be is 15 to 70  
91 angstroms), and using low pressure chemical vapor deposition (LPCVD) stacking a layer of 3000  
92 angstroms of polycrystal silicon (poly-Si). Furthermore, at 620 degrees under low-pressure environment,  
93 nitrogen trifluoride for (NF<sub>3</sub>) of the polycrystalline silicon to do different time (5 to 20 minutes) the  
94 annealing treatment. Finally, the gate electrode is made of aluminum.

95  
96 In the above-mentioned by using nitrogen trifluoride of the polycrystalline silicon as in the process of  
97 annealing, with a silicon nitride silicon fluoride (Si-N) (Si-F) the bonding of the silicon wafer, the silicon  
98 dioxide interface (SiO<sub>2</sub>/Si interface) generated in, such strong the key ties the meeting substituted  
99 weaker bonding, for example with silicon hydroxide (Si-H) (Si-OH) [...], enhanced reliability of the oxide  
100 layer. As shown in Figure 4 is shown, through the nitrogen trifluoride annealing treatment of the test  
101 piece to the secondary ion analysis (SIMS), can be sure in the silicon dioxide with the interface of the  
102 silicon wafer with the nitrogen to form a bonded fluorine.

103  
104 Figure 2 and Figure 3 are respectively for different annealing time of the collapse of the aluminum test  
105 piece of the electrode and the drain current (leakage current) electric field (breakdown field) the  
106 statistical profile, wherein to use nitrogen trifluoride its collapse test piece annealing treatment of the  
107 electric field than the control test piece are high, and the leakage current test than the control group are  
108 also low.

109  
110 As shown in Figure 5 the invention the embodiment of the process for preparing the test piece  
111 preparation flowdiagram, wherein the final steps in addition to the gate electrode silicon cobalt is made,  
112 the remaining steps are the same as the previous embodiment. Figure 6 and Figure 7 are respectively for  
113 different annealing time of the collapse of the cobalt [...] the test piece of the electrode of the electric  
114 field and leakage current statistical profile, wherein to use nitrogen trifluoride its collapse test piece  
115 annealing treatment of the electric field than the control test piece are high, and the leakage current  
116 test than the control group are also low. Also, in this embodiment, the nitrogen trifluoride cobalt in  
117 silicon the test piece of the electrode to the time of annealing to the optimization conditions for 10  
118 minutes.

119  
120 To sum up, by using nitrogen trifluoride of the polycrystalline silicon as annealing processing, the oxide  
121 layer can remarkably improve the collapse of the electric field and leakage current, to enhance the  
122 reliability of the oxide layer.

The invention, although reference has been made to the attached drawing and detailed description of the embodiment, however, it does not the park is restricted in the above-mentioned second embodiment. Any in accordance with this invention the spirit and the scope of the Patent application the change and modification, should still belongs to the scope of this invention.

**ENGLISH CLAIMS:**

A nitrogen trifluoride gate oxide layer to improve the process for preparing of annealing treatment method for reliability, it has the following main steps: on the wafer (field oxide) forming a barrier oxide layer, and etching a active region (active region) ; (ultra-thin oxide) to form a ultra-thin oxide layer, and stacking a layer of polycrystal silicon (poly-Si); to nitrogen trifluoride (NF 3) of the polycrystalline silicon for annealing process; and forming the gate electrode.

Method according to Claim 1, wherein the ultra-thin oxide layer of a thickness of 15 to 70 angstroms.

Method according to Claim 1, wherein the polycrystalline silicon is stacked low-pressure chemical vapor deposition (LPCVD).

Method according to Claim 1, wherein on the annealing treatment at 620 degrees the low-pressure environment.

Method according to Claim 1, wherein the annealing treatment time is 5 to 20 minutes.

Method according to Claim 1, wherein the gate electrode is an aluminum electrode.

Method according to Claim 1, wherein the gate electrode is a cobalt silicon compound electrode.

Method according to Claim 7, wherein the annealing treatment uses the time of 10 minutes is the best.



## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24585269
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	11-JAN-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	16:05:39
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-01-11_IDS_TSSRA-012C1.pdf	166178 32cfa4a9d5744dedb5e4fb402e69026db85c443	yes	7

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	7	
Warnings:					
Information:					
2	Foreign Reference	CA2399282A1.pdf	1664146	no	49
			e4c658ae4d30f1fea01f42b1a792e75723197f8f		
Warnings:					
Information:					
3	Foreign Reference	JP-H08-195334.pdf	1116815	no	17
			36e2a73435cbc50d34c3c90e32e22b19f71d121d		
Warnings:					
Information:					
4	Foreign Reference	TW389965.pdf	5816655	no	19
			204efd8dfe4aa7ab27c6dc6374540f8ebf7f546d		
Warnings:					
Information:					
5	Non Patent Literature	Abe-et-al_Bonded-SOI-wafers-with-various-substrates.pdf	4188360	no	12
			69d140b4109fe3bfa173f66c64588eed2c19ccd		
Warnings:					
Information:					
6	Non Patent Literature	Amirfeiz_Formation-of-silicon-structures-by-plasma-activated.pdf	598721	no	6
			7b96a21348284f855ef98c05a1b8bbe561e37222		
Warnings:					
Information:					
7	Non Patent Literature	Arnold_Silicon-on-insulator-devices-for-high.pdf	4423025	no	16
			4c29ff05c475cac45edb8e977faa9859ca5b0d57		
Warnings:					
Information:					
8	Non Patent Literature	Beitman-et-al_Bonded-SOI-in-a-bipolar-IC.pdf	3285426	no	9
			4df2e5b32c7c99dbcfcd5d91aa7e9092d46004f97		
Warnings:					
Information:					

9	Non Patent Literature	Booth-et-al_Full-three-dimensional-microcircuit-integration.pdf	3751127	no	11
			a4cbc8d744c22b7e66acf75e18b411dfd4dff3430		
Warnings:					
Information:					
10	Non Patent Literature	Brugger-et-al_High-precision-aligned.pdf	3642926	no	11
			253fcf802972454d3b6b24e0503bcbbfcd0aa913		
Warnings:					
Information:					
11	Non Patent Literature	Cha-et-al_Design-considerations-for-wafer-bonding.pdf	3693535	no	11
			f17685092a149b0bb1261c73ad82a5906258dfdd		
Warnings:					
Information:					
12	Non Patent Literature	Christel-et-al_Silicon-fusion-bonding_An-important-tool.pdf	4251022	no	14
			e0b89ddb9520ebd03fbcadd8a69f9915a76e9417		
Warnings:					
Information:					
13	Non Patent Literature	Ciarlo_High-and-low-temperature-bonding.pdf	4777968	no	15
			63f6374663c0438fe780ae557aef11d41ff25146		
Warnings:					
Information:					
14	Non Patent Literature	Desmond-et-al_The-effects-of-process-induced-defects.pdf	4326281	no	11
			dbdff02790c102a6081fc64fac719abcccc00968c		
Warnings:					
Information:					
15	Non Patent Literature	Eda-et-al_Quartz-crystal-on-silicon-technique.pdf	3526622	no	10
			56c8ef797bc70cbf10614892b8d953c0ccdb6d33		
Warnings:					
Information:					
16	Non Patent Literature	Esashi_Complex-micromechanical-structures-by-low-temperature.pdf	4337850	no	16
			71987f9e512a22e8848d6595c0bdfb9da07d2f13		
Warnings:					
Information:					
17	Non Patent Literature	Farrens-et-al_Analysis-of-bond-characteristics-in-Si-direct-bonded-materials.pdf	4473292	no	16
			f5b830bc93b16d218f1e9bfb53d2055d34eec328		
Warnings:					

18	Non Patent Literature	Farrens-et-al_Chemical-free-room-temperature-wafer-to-wafer.pdf	1095722	no	7
			71b48bf9a69d98279739aa198830d4d83c7cdcca		
Warnings:					
Information:					
19	Non Patent Literature	Farrens-et-al_Chemical-free-wafer-bonding.pdf	1955768	no	6
			9cc749227a83d7c94d335e8cdf8b6b64e7921907		
Warnings:					
Information:					
20	Non Patent Literature	Feijoo-et-al_BE-SOI-with-etch-stop-layers.pdf	3926965	no	14
			0b2ba7e0d461d571e4411281ec2fc2dde737f324		
Warnings:					
Information:					
21	Non Patent Literature	Feindt-et-al_A-complementary-bipolar-process.pdf	3159629	no	9
			1fddf510d88e41e68012c4dc411fd66848b6e2ce		
Warnings:					
Information:					
22	Non Patent Literature	FirstOfficeAction_JP2012-107053_7pages.pdf	726480	no	7
			0af8df79f228a9498c74a9fb8ce278c6b3c42eb9		
Warnings:					
Information:					
23	Non Patent Literature	Folta-et-al_Low-temperature-wafer-bonding-of-surfaces.pdf	3332513	no	8
			42ec4aa7f6677ac006f4464446e98ee415a0538		
Warnings:					
Information:					
24	Non Patent Literature	Gan_Surface-activation-enhanced-low-temperature.pdf	6532007	no	192
			a8d934bf29219e361923569ef3bab1e488b1d453		
Warnings:					
Information:					
25	Non Patent Literature	Garofalini_Atomic-structure-and-dynamic-behavior.pdf	4534609	no	15
			404433524def75a08fa0082d2577a0f4db562723		
Warnings:					
Information:					
26	Non Patent Literature	Gassel-et-al_SIMOS-and-wafer-bonding-Combination.pdf	3460418	no	11
			02cc5282e9d2aecf4f870096a7ee6137bef9531d		
Warnings:					

27	Non Patent Literature	Gosele-et-al_Semiconductor-Wafer-Bonding_A-flexible-approach-to-materials.pdf	2086483	no	10
			2cf1b8fffa66b813baf4afad78f6291385a218b8		
Warnings:					
Information:					
28	Non Patent Literature	Gosele-et-al_Silicon-layer-transfer-by-wafer-bonding.pdf	4704876	no	16
			f05a967d546f68b815dab335501543d6b8d135e9		
Warnings:					
Information:					
29	Non Patent Literature	Harendt-et-al_Bonded-wafer-SOI-smart-power-circuits.pdf	4511974	no	16
			e2b050dcc7d8837f6a33379dcaabb5772b175d0d		
Warnings:					
Information:					
30	Non Patent Literature	Horning-et-al_Wafer-to-wafer-bond-characterization.pdf	3722229	no	9
			004d23ac2baf620bdb0c6f2ca1affff7f3399af		
Warnings:					
Information:					
31	Non Patent Literature	Hughes_Silicon-silicon-direct-wafer-bonding.pdf	4758914	no	16
			57e70ab8cac521e070cea31b4622e36d0248453c		
Warnings:					
Information:					
32	Non Patent Literature	Iyer-et-al_Ultra-thin-silicon-on-insulator.pdf	4558780	no	15
			207dc9a114b1a0644a45e5fed91b36e01c0e53fe		
Warnings:					
Information:					
33	Non Patent Literature	Jiao-et-al_Silicon-direct-bonding-at-low-temperature.pdf	2530932	no	4
			0926ef42b110be9ab6761119ee8382f65e90d4fe		
Warnings:					
Information:					
34	Non Patent Literature	Kawai-et-al_Structure-of-the-interface-bonded.pdf	3418370	no	10
			292eae8d5e6041118c31ed60a75ac74ba1aae66		
Warnings:					
Information:					
35	Non Patent Literature	Ling-et-al_Influence-of-bonding-temperature.pdf	3918466	no	11
			c338d324a1401f36b5d15c79b9bec3c4489678ea0		
Warnings:					
Information:					

page 169 of 331

SAMSUNG EXHIBIT 100

36	Non Patent Literature	Ljungberg-et-al_Buried-silicide-layers-in-silicon.pdf	3352587	no	9
			f18bc19827d393ac41cc076ec4d7ec9de28a ca5b		
Warnings:					
Information:					
37	Non Patent Literature	Ljungberg-et-al_Spontaneity-of-hydrophobic-Si-Si-bonding.pdf	3664928	no	11
			fda6707fe234872c97037af095feb3ebe9c2 197e		
Warnings:					
Information:					
38	Non Patent Literature	Macary-et-al_Influence-of-the-wafer-cleaning.pdf	2280162	no	11
			e37a8681b90ae441cf6513e2f8ed920c38ea 6942		
Warnings:					
Information:					
39	Non Patent Literature	McLachlan-et-al_A-bonded-wafer-bipolar-process-in-manufacturing.pdf	4176833	no	13
			9ba4bd8ecb795c92a896251482ea57dc642 da4c7		
Warnings:					
Information:					
40	Non Patent Literature	Mitani-et-al_Investigation-of-the-N-type-inversion-layer.pdf	3774811	no	11
			b643dc928947dd294a318b3cc312e739342 ad2c7		
Warnings:					
Information:					
41	Non Patent Literature	Mumola-et-al_Plasma-thinned-silicon-on-insulator.pdf	4569996	no	14
			00dd4056f47c535d897010426294655db6b 98b61		
Warnings:					
Information:					
42	Non Patent Literature	Nakanishi-et-al_Studies-on-SiO2-SiO2-bonding-with-hydrofluoric-acid-room-temperature.pdf	1425609	no	8
			506aa41c2758e47a765be193226408487ee f8b35		
Warnings:					
Information:					
43	Non Patent Literature	Nishizawa-et-al_An-advanced-dielectric-isolation-structure-for-SOI-CMOS.pdf	3720712	no	14
			8e2f8086ab743ef826a7414865d9835fe0cf 9f71		
Warnings:					
Information:					
44	Non Patent Literature	Reiche-et-al_Characterization-of-interfaces-of-directly.pdf	7960353	no	6
			3cbb2707b2d2210481586210bb2b9fd167 8f7d2e		
Warnings:					
Information:					

page 170 of 331

SAMSUNG EXHIBIT 100

45	Non Patent Literature	Reiche-et-al_The-effect-of-a-plasma-pretreatment.pdf	4357119	no	8
			56fe448fea21ba733351a191133b624217d10497		
Warnings:					
Information:					
46	Non Patent Literature	Robb-et-al_High-temperature-lateral-dopant-diffusion-in-WSi2.pdf	3444799	no	11
			a1c406a6216a0dbcb6456e028975698371a18aac		
Warnings:					
Information:					
47	Non Patent Literature	Roberds-et-al_Low-temperature-in-situ-plasma-activated.pdf	3260176	no	9
			c98dc35bdc909b0aaec3593c677af86e89efea1db		
Warnings:					
Information:					
48	Non Patent Literature	Roberds-et-al_Low-temperature-silicon-direct-bonding.pdf	1001193	no	9
			30e7b4656ad963a7e88a77764531cc579f4ff8cc1		
Warnings:					
Information:					
49	Non Patent Literature	Rouse-et-al_Application-of-150-mm-bonded-wafer-technology.pdf	3963050	no	11
			69e5ae2f9d3c7f91a075c996552cfc38be18d15		
Warnings:					
Information:					
50	Non Patent Literature	Saitoh-et-al_Characterization-of-directly-bonded-silicon-on-insulator.pdf	3352219	no	10
			3366edd8777aae8a08726c218173b4a2ec6f4a5e		
Warnings:					
Information:					
51	Non Patent Literature	Sakakibara-et-al_A-wafer-bonded-SOI-bipolar-transistor.pdf	3226317	no	10
			6ea83585af9b78b1d4318a76d50270c59fe33f04		
Warnings:					
Information:					
Total Files Size (in bytes):			178505948		

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**



**INFORMATION DISCLOSURE STATEMENT**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Unknown
Art Unit	:	2895
Conf. No.	:	1033

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**References and Listing**

Pursuant to 37 CFR 1.56, an Information Disclosure Statement listing references is provided herewith. Copies of any listed foreign and non-patent literature references are being submitted.

**No Disclaimers**

To the extent that anything in the Information Disclosure Statement or the listed references could be construed as a disclaimer of any subject matter supported by the present application, Applicant hereby rescinds and retracts such disclaimer.

**Timing of Disclosure**

This Information Disclosure Statement is being filed within three months of the filing date, and no fee is believed to be required.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

**Application No.:** 14/957,501  
**Filing Date:** December 2, 2015

Respectfully submitted,  
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: January 11, 2016

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22415314  
011116

---

Please Direct All Correspondence to Customer Number 135,980

---

**EFS WEB CONTINUING IDS COVER LETTER**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Unknown
Art Unit	:	2895
Conf No.	:	1033

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Submitted herewith are references numbered 55 to 66 listed on the PTO/SB/08 or equivalent filed under EFS ID 24585269.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: January 11, 2016

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22434451  
011116

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24587990
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	11-JAN-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	16:13:27
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-01-11_Cont-IDS_TSSRA-012C1.pdf	63258 e3b6bdcfc307127364d6db6d0d9827acd749918d	no	1

### Warnings:

Information:

2	Non Patent Literature	Shajii-et-al_A-backside-contact-technology.pdf	3174356	no	9
			e7f8a80c212fa64f145706eb78f271d70d4e db4e		
Warnings:					
Information:					
3	Non Patent Literature	Soderbarg-et-al_Formation-of-heat-sinks-using-bonding.pdf	3875985	no	11
			2418631b35929b9758a3484e238860eb40 095e13		
Warnings:					
Information:					
4	Non Patent Literature	Sooriakumar-et-al_Thermal-mismatch-strain-in-anodically.pdf	2682215	no	6
			9a20ba63dae23fb380179556aa83f55da7cf e23c		
Warnings:					
Information:					
5	Non Patent Literature	Stanley_Revenue-sensitivity-to-yield-and-starting-wafer-cost.pdf	3071971	no	8
			43d5c91ebdd1cf259fb04e693c549613674f da4b		
Warnings:					
Information:					
6	Non Patent Literature	Suga_Room-temperature-bonding-on-metals-and-ceramics.pdf	3804575	no	11
			918a799d6e7c6863be5f71c569863b36e6f7 076f		
Warnings:					
Information:					
7	Non Patent Literature	Tong-et-al_A-smarter-cut-approach-to-low-temperature-silicon-layer-transfer.pdf	452914	no	3
			f691591fd75f1fb956eb7166741a97490c4e 1709		
Warnings:					
Information:					
8	Non Patent Literature	Tong-et-al_Hydrophobic-silicon-wafer-bonding.pdf	759418	no	4
			0e93eb65b1aa2bf50364b7e165e5ac48e2a c1f08		
Warnings:					
Information:					
9	Non Patent Literature	Tong-et-al_Low-temperature-InP-layer-transfer.pdf	536373	no	2
			6b75ea98f310793bfb7798c248f4b7a58ac0 4a1c		
Warnings:					
Information:					
10	Non Patent Literature	Tong-et-al_Low-temperature-wafer-direct-bonding.pdf	4290041	no	12
			38949929f18c6264234a007640e56efc3094 d193		
Warnings:					

11	Non Patent Literature	Tong-et-al_Wafer-bonding-and-layer-splitting.pdf	950230 c1cc801e40d43b3fac829d37686ffc4676b0e053	no	17
Warnings:					
Information:					
12	Non Patent Literature	Weldon-et-al_Physics-and-chemistry-of-silicon-wafer-bonding.pdf	748476 0c02a3e27f61b0091e2e3e5f8dcb6da88eb107df	no	13
Warnings:					
Information:					
13	Non Patent Literature	Yallup_Analog-CMOS-circuits-on-thick-films.pdf	4201931 290b9043e310805baf3f24e373f2e2cb06fd3804	no	13
Warnings:					
Information:					
Total Files Size (in bytes):			28611743		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1	1033
135980	7590	02/03/2016	EXAMINER	
Knobbe, Martens, Olson & Bear, LLP 2040 main Street Fourteenth Floor Irvine, CA 92614			GARCIA, JOANNIE A	
			ART UNIT	PAPER NUMBER
			2895	
			NOTIFICATION DATE	DELIVERY MODE
			02/03/2016	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jayna.cartee@knobbe.com  
efiling@knobbe.com

<b>Office Action Summary</b>	<b>Application No.</b> 14/957,501	<b>Applicant(s)</b> TONG ET AL.	
	<b>Examiner</b> JOANNIE A. GARCIA	<b>Art Unit</b> 2895	<b>AIA (First Inventor to File) Status</b> No

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on December 2, 2015, and January 11, 2016.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims\***

- 5) ☒ Claim(s) 2-34 is/are pending in the application.  
5a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 6) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 7) ☒ Claim(s) 2-34 is/are rejected.
- 8) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 9) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

\* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).

**Application Papers**

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on December 2, 2015 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

- a) ☐ All    b) ☐ Some\*\*    c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 3) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)<br>Paper No(s)/Mail Date <u>January 11, 2016</u> . | 4) <input type="checkbox"/> Other: ____.  |



The present application is being examined under the pre-AIA first to invent provisions.

### **DETAILED ACTION**

This action is responsive to: the Application filed December 2, 2015, and the Information Disclosure Statement (IDS) Document, Form PTO-1449, filed January 11, 2016.

Claims 2-34 are pending. Claims 1, 22, 32, and 33, are independent.

### **Information Disclosure Statement**

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Document filed January 11, 2016.

This Information Disclosure Statement (IDS) Document has been considered, and a signed and dated copy is included herein.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper time wise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct

from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 1 and 6**, of U.S. Patent Application 2015/0303263. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent Application 2015/0303263. In this regard, the limitations of instant application claim 22 appear to be anticipated or obvious over '263 claims 1 and 6.

For example, instant application claim 22 recites, "...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...", which includes the similarly recited limitations in '263 claims 1 and 6, *namely*, "...a processed semiconductor device wafer comprising a first surface and a planarized insulating material having a first bonding surface wherein said planarized insulating material is opposite said first surface; a first material having a second surface and a second bonding surface opposite said second surface, wherein no devices are disposed in said first material; wherein said first bonding surface is an etched surface terminated with a species; and wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...", and "...and wherein said species comprises nitrogen...".

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 30**, of U.S. Patent Application 2015/0303263. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent Application

Art Unit: 2895

2015/0303263. In this regard, the limitations of instant application claims 22 and 27 appear to be anticipated or obvious over '263 claim 30.

For example, instant application claim 22 recites, "...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...", and "...wherein said planarized insulating material comprises silicon oxide...", which includes the similarly recited limitations in '263 claim 30, *namely*, "...a processed semiconductor device wafer comprising a first surface having a thickness, a planarized insulating material of deposited silicon oxide having a first bonding surface, wherein said planarized insulating material is opposite said first surface, and a device layer between said first surface and said planarized insulating material; a first material comprising silicon having a second surface and a second bonding surface opposite said second surface, wherein no devices are disposed in said first material; wherein said first bonding surface is an etched surface terminated with nitrogen; wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...".

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 31 and 36**, of U.S. Patent

Application 2015/0303263. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent Application 2015/0303263. In this regard, the limitations of instant application claim 22 appear to be anticipated or obvious over '263 claims 31 and 36.

For example, instant application claim 22 recites, "...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...", which includes the similarly recited limitations in '263 claims 31 and 36, *namely*, "...a first silicon material comprising a first surface and a planarized insulating material having a first bonding surface wherein said planarized insulating material is opposite said first surface; a second material having a second surface and a second bonding surface opposite said second surface, wherein no devices are disposed in said second material; wherein said first bonding surface is an etched surface terminated with a species; and wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive..." and "...wherein said species comprises nitrogen...".

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 60**, of U.S. Patent Application 2015/0303263. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent Application 2015/0303263. In this regard, the limitations of instant application claims 22 and 27 appear to be anticipated or obvious over '263 claim 60.

For example, instant application claim 22 recites, "...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...", and "...wherein said planarized insulating material comprises silicon oxide...", which includes the similarly recited limitations in '263 claim 60, *namely*, "...a planarized insulating material of deposited silicon oxide having a first bonding surface, wherein said planarized insulating material is opposite said first surface, and a device layer between said first surface and said planarized insulating material; a second material comprising silicon having a second surface and a second bonding surface opposite said second surface, wherein no devices are disposed in said second material; wherein said first bonding surface is an etched surface terminated with nitrogen; wherein said first and second bonding

surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...".

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 77 and 82**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claim 22 appear to be anticipated or obvious over '505 claims 77 and 82.

For example, instant application claim 22 recites, "...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...", which includes the similarly recited limitations in '505 claims 77 and 82, *namely*, "...a processed semiconductor device wafer comprising a first surface and a planarized insulating material having a first bonding surface wherein said planarized insulating material is opposite said first surface; a first material having a second surface and a second bonding surface opposite said second surface; wherein said first bonding surface is an etched surface terminated with a species; and wherein said first and second bonding surfaces are in direct contact

with each other and bonded together with a chemical bond without any adhesive...”,  
and “...wherein said species comprises nitrogen...”.

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 115**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claims 22 and 27, appear to be anticipated or obvious over '505 claim 115.

For example, instant application claim 22 recites, “...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...”, and “...wherein said planarized insulating material comprises silicon oxide...”, which includes the similarly recited limitations in '505 claim 115, *namely*, “...a processed semiconductor device wafer comprising a first surface having a thickness, a planarized insulating material of deposited silicon oxide having a first bonding surface, wherein said planarized insulating material is opposite said first surface, and a device layer between said first surface and said planarized insulating material; a first material comprising silicon having a second



surface and a second bonding surface opposite said second surface; wherein said first bonding surface is an etched surface terminated with nitrogen; and wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...”.

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 192 and 197**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claim 22 appear to be anticipated or obvious over '505 claims 192 and 197.

For example, instant application claim 22 recites, “...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...”, which includes the similarly recited limitations in '505 claims 192 and 197, *namely*, "...a first silicon material comprising a first surface and a planarized insulating material having a first bonding surface wherein said planarized insulating material is opposite said first surface; a second material having a second surface and a second bonding surface opposite said

second surface; wherein said first bonding surface is an etched surface terminated with a species; and wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...”, and “...wherein said species comprises nitrogen...”.

**Claims 22-31** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 230**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claims 22 and 27, appear to be anticipated or obvious over ’505 claim 230.

For example, instant application claim 22 recites, “...a first semiconductor material comprising a planarized insulating material having a first bonding surface; and a second material having a second bonding surface, wherein the first bonding surface is an etched surface terminated with a nitrogen- containing species, and wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive...”, and “...wherein said planarized insulating material comprises silicon oxide...”, which includes the similarly recited limitations in ’505 claim 230, *namely*, “...a first silicon material comprising a first surface having a thickness, a planarized insulating material of deposited silicon oxide having a first bonding surface, wherein said planarized insulating material is opposite

said first surface, and a device layer between said first surface and said planarized insulating material; a second material comprising silicon having a second surface and a second bonding surface opposite said second surface; wherein said first bonding surface is an etched surface terminated with nitrogen; wherein said first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any adhesive...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 1 and 9**, of U.S. Patent 9,082,627. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 9,082,627. In this regard, the limitations of instant application claim 2 appear to be anticipated or obvious over '627 claims 1 and 9.

For example, instant application claim 1 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material in a reaction space; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material outside the reaction space; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '627

Art Unit: 2895

claims 1 and 9, *namely*, "...forming a planarized insulating material on a processed semiconductor wafer; exposing said planarized insulating material to a plasma RIE process in a plasma chamber; terminating said planarized insulating material with a species; bringing into direct contact said terminated and planarized insulating material and a first material outside of said plasma chamber; and forming a chemical bond between said terminated and planarized insulating material and said first material...", and "...exposing said insulating material to a plasma RIE process in said plasma chamber using nitrogen gas...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 1 and 9**, of U.S. Patent 9,082,627. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 9,082,627. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over '627 claims 1 and 9.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material; and forming a chemical bond between the

Art Unit: 2895

terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '627 claims 1 and 9, *namely*, "...forming a planarized insulating material on a processed semiconductor wafer; exposing said planarized insulating material to a plasma RIE process in a plasma chamber; terminating said planarized insulating material with a species; bringing into direct contact said terminated and planarized insulating material and a first material outside of said plasma chamber; and forming a chemical bond between said terminated and planarized insulating material and said first material...", and "...exposing said insulating material to a plasma RIE process in said plasma chamber using nitrogen gas...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 1**, of U.S. Patent 9,082,627. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 9,082,627. In this regard, the limitations of instant application claim 33 appear to be anticipated or obvious over '627 claim 1.

For example, instant application claim 33 recites, "...forming a planarized insulating material on a processed semiconductor wafer; exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas; terminating the planarized insulating material with a species; bringing into direct contact the terminated and planarized insulating material and a first material outside of

Art Unit: 2895

said plasma chamber; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '627 claim 1, *namely*, "...forming a planarized insulating material on a processed semiconductor wafer; exposing said planarized insulating material to a plasma RIE process in a plasma chamber; terminating said planarized insulating material with a species; bringing into direct contact said terminated and planarized insulating material and a first material outside of said plasma chamber; and forming a chemical bond between said terminated and planarized insulating material and said first material...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 1, 2, and 11**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 9,082,627. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over '627 claims 1, 2, and 11.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated

and planarized insulating material; and forming a chemical bond between the terminated and planarized insulating material and the first material...”, which includes the similarly recited limitations in ‘627 claims 1 and 9, *namely*, "...forming a planarized insulating material on a processed semiconductor wafer; exposing said planarized insulating material to a plasma RIE process; terminating said planarized insulating material with a species; after said exposing and terminating steps, bringing into direct contact said terminated planarized insulating material and a first material; and forming a chemical bond between said terminated planarized insulating material and said first material...”, "...wherein said chemical bond is formed without any adhesive...", and "...wherein said plasma RIE process comprises a nitrogen gas...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 39, 40, and 48**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over ‘505 claims 39, 40, and 48.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing

Art Unit: 2895

solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '505 claims 39, 40, and 48, *namely*, "...forming a planarized insulating material on a processed semiconductor wafer; exposing said planarized insulating material to a plasma RIE process; terminating said planarized insulating material with a first species; terminating a first material with a second species; bringing into direct contact said terminated planarized insulating material with said terminated first material; and forming a chemical bond between said terminated planarized insulating material and said terminated first material...", "...wherein said chemical bond is formed without any adhesive...", and "...wherein said plasma RIE process contains a nitrogen gas...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 116, 117, and 126**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over '505 claims 116, 117, and 126.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material;



terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '505 claims 116, 117, and 126, *namely*, "...forming a planarized insulating material on a first silicon material; exposing said planarized insulating material to a plasma RIE process; terminating said planarized insulating material with a species; after exposing and terminating steps, bringing into direct contact said terminated planarized insulating material and a second material; and forming a chemical bond between said terminated planarized insulating material and said second material...", "...wherein said chemical bond is formed without any adhesive...", and "...wherein said plasma RIE process contains a nitrogen gas..."

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 154, 155, and 163**, of U.S. Patent 8,153,505. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent 8,153,505. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over '505 claims 154, 155, and 163.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '505 claims 154, 155, and 163, *namely*, "...forming a planarized insulating material on a first silicon material; exposing said planarized insulating material to a plasma RIE process; terminating said planarized insulating material with a first species; terminating a second material with a second species; bringing into direct contact said terminated planarized insulating material with said terminated second material; and forming a chemical bond between said terminated planarized insulating material and said terminated second material...", "...wherein said chemical bond is formed without any adhesive...", and "...wherein said plasma RIE process contains a nitrogen gas...".

**Claims 2-21, and 32-34**, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claims 105, 106, and 107**, of U.S. Patent 6,902,987. Although the conflicting claims are not identical, it is not patentably distinct from each other because the claims of the current application, U.S. Patent Application 14/957,501, are broader than the claims of the U.S. Patent

6,902,987. In this regard, the limitations of instant application claim 32 appear to be anticipated or obvious over '987 claims 105, 106, and 107.

For example, instant application claim 32 recites, "...forming a planarized insulating material on a semiconductor wafer; etching the planarized insulating material; terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching; bringing a first material into direct contact with the terminated and planarized insulating material; and forming a chemical bond between the terminated and planarized insulating material and the first material...", which includes the similarly recited limitations in '5987 claims 105, 106, and 107, *namely*, "...depositing first and second bonding layers on respective first and second workpieces; planarizing said first and second bonding layers; etching said first and second bonding layers after planarizing to activate respective first and second surfaces of said first and second bonding layers; terminating said first and second surfaces with a terminating chemical species after etching; bringing into direct contact said first and second surfaces after said etching step; and forming a chemical bond between said first and second workpieces at room temperature...", "...depositing each of said first and second bonding layers comprises depositing a silicon oxide layer; planarizing comprises polishing said first and second bonding layers; etching comprises exposing said first and second bonding layers to a plasma; and terminating comprises immersing said first and second bonding surfaces in an ammonia-based solution...", and "...wherein said first and second workpieces each comprise a semiconductor wafer..."

### ***Conclusion***

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joannie García, whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad K. Islam, can be reached on (571) 270-5878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/JOANNIE A GARCIA/  
Examiner, Art Unit 2895  
/KYOUNG LEE/  
Primary Examiner, Art Unit 2895

<b>Notice of References Cited</b>	Application/Control No. 14/957,501	Applicant(s)/Patent Under Reexamination TONG ET AL.	
	Examiner JOANNIE A. GARCIA	Art Unit 2895	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2002/0055208 A1	05-2002	Ohtani, Hisashi	H01L21/2022	438/151
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 1 OF 5	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	4,700,466	10-20-1987	Nakagawa et al.	
	2	4,983,251	01-08-1991	Haisma et al.	
	3	5,427,638	06-27-1995	Goetz et al.	
	4	5,451,547	09-19-1995	Himi et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	5	CA 2 399 282 A1	08-23-2001	Ziptronix, Inc.		
	6	JP H08-195334	07-30-1996	Canon Inc.		T
	7	TW 389965B	05-11-2000	San Fu Chemical Co. Ltd.		T

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	8	ABE et al., "Bonded SOI wafers with various substrates for IC fabrication," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 32-42.	
	9	AMIRFEIZ et al., "Formation of silicon structures by plasma-activated wafer bonding," Journal of The Electrochemical Society, 2000, Vol. 147, No. 7, pp. 2693-2698.	
	10	ARNOLD, Emil, "Silicon-on-insulator devices for high voltage and power IC applications," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 161-175.	
	11	BEITMAN et al., "Bonded SOI in a bipolar IC without trench isolation," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 144-151.	
	12	BOOTH et al., "Full three dimensional microcircuit integration techniques using wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 293-302.	
	13	BRUGGER et al., "High-precision aligned silicon wafer bonding for a micromachined AFM sensor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 363-372.	

Examiner Signature /Joannie Garcia/	Date Considered 01/25/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 2 OF 5	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	14	CHA et al., "Design considerations for wafer bonding of dissimilar materials," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 257-266.	
	15	CHRISTEL et al., "Silicon fusion bonding: An important tool for the design of micromechanical silicon devices," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 327-339.	
	16	CIARLO, D., "High - and low - temperature bonding techniques for microstructures," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 313-326.	
	17	DESMOND et al., "The effects of process-induced defects on the chemical selectivity of highly-doped boron etchstops," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 423-432.	
	18	EDA et al., "Quartz crystal on silicon technique using direct bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 373-381.	
	19	ESASHI, "Complex micromechanical structures by low temperature bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 348-362.	
	20	FARRENS et al., "Analysis of bond characteristics in Si direct-bonded materials," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 81-95.	
	21	FARRENS et al., "Chemical free room temperature wafer to wafer direct bonding," J. Electrochem. Soc., The Electrochemical Society, Inc., November 1995, Vol. 142, No. 11. pp. 3949-3955.	
	22	FARRENS et al., "Chemical free wafer bonding of silicon to glass and sapphire," Electrochemical Society Proceedings Volume 95-7, 1995, pp. 72-77.	
	23	FEIJÓO et al, "BE-SOI with etch stop layers grown by RTCVD," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 267-279.	
	24	FEINDT et al., "A complementary bipolar process on bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 189-196.	
	25	First Office Action (English translation) mailed October 6, 2015, issued in Japanese Patent Application No. 2012-107053, 7 pages.	
	26	FOLTA et al., "Low-temperature wafer bonding of surfaces using a reactive sputtered oxide," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 107-113.	
	27	GAN, Qing, "Surface activation enhanced low temperature silicon wafer bonding," Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, Department of Mechanical Engineering and Materials Science, Duke University, August 4, 2000, 192 pages.	

Examiner Signature /Joannie Garcia/	Date Considered 01/25/2016
-------------------------------------	----------------------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 3 OF 5	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	28	GAROFALINI, Stephen H., "Atomistic structure and dynamic behavior of silica surfaces," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 57-70.	
	29	GASSEL et al., "SIMOX and wafer bonding: Combination of competitors complements one another," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 433-442.	
	30	GÖSELE et al., "SEMICONDUCTOR WAFER BONDING: A flexible approach to materials combinations in microelectronics; micromechanics and optoelectronics," IEEE, 1997, pp. 23-32.	
	31	GÖSELE et al., "Silicon layer transfer by wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 395-409.	
	32	HARENDT et al., "Bonded-wafer SOI smart power circuits in automotive applications," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 129-143.	
	33	HORNING et al., "Wafer-to-wafer bond characterization by defect decoration etching," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 199-206.	
	34	HUGHES, Donald L., "Silicon-silicon direct wafer bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 17-31.	
	35	IYER et al., "Ultra thin silicon-on insulator using epitaxial etch stops," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 3-16.	
	36	JIAO et al., "Silicon direct bonding at low temperature near the boiling point of water," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 280-282.	
	37	KAWAI et al., "Structure of the interface of a bonded wafer," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 216-224.	
	38	LING et al., "Influence of bonding temperature on the electrical properties of Si/SiO <sub>2</sub> interfaces in bonded silicon-on-insulator-wafers" Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 453-462.	
	39	LJUNGBERG et al., "Buried silicide layers in silicon using wafer bonding with cobalt as interfacial layer," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 249-256.	
	40	LJUNGBERG et al., "Spontaneity of hydrophobic Si-Si bonding and properties of the bonded interfaces," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 473-482.	

Examiner Signature	/Joannie Garcia/	Date Considered	01/25/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 4 OF 5	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	41	MACARY et al, "Influence of the wafer cleaning on the electrical properties of Si-Si bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 463-472.	
	42	MCLACHLAN et al., "A bonded wafer bipolar process in manufacturing," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 43-54.	
	43	MITANI et al, "Investigation of the N-type inversion layer induced at the bottom of P-type active silicon layers in bonded SOI wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 443-452.	
	44	MUMOLA et al., "Plasma-thinned silicon-on-insulator bonded wafers," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 410-422.	
	45	NAKANISHI et al., "Studies on SiO <sub>2</sub> -SiO <sub>2</sub> bonding with hydrofluoric acid --- room temperature and low stress bonding technique for MEMS ---" 1998 IEEE, pp. 609-614.	
	46	NISHIZAWA et al., "An advanced dielectric isolation structure for SOI-CMOS/BiCMOS VLSIs," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 176-188.	
	47	REICHE et al., "Characterization of interfaces of directly bonded silicon wafers: A comparative study of secondary ion mass spectroscopy multiple internal reflection spectroscopy, and transmission electron microscopy," Jpn. J. Appl. Phys., Vol. 35 (1996), pp. 2102-2107, Part 1, No. 4A, April 1996.	
	48	REICHE et al., "The effect of a plasma pretreatment on the Si/Si bonding behaviour," Electrochemical Society Proceedings, 1998, Vol. 97-36, pp. 437-444.	
	49	ROBB et al., "High temperature lateral dopant diffusion in WSi <sub>2</sub> , TiSi <sub>2</sub> and TiN films," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society, Proceedings Vol. 93-29 (1993), pp. 230-239.	
	50	ROBERDS et al., "Low temperature, in situ, plasma activated wafer bonding," Electrochemical Society Proceedings, 1997, Vol. 97-36, pp. 598-606.	
	51	ROBERDS et al., "Low temperature silicon direct bonding," Department of Mechanical, Aeronautical, and Materials Engineering, University of California, Davis, 1997, pp. 240-248.	
	52	ROUSE et al, "Application of 150 mm bonded wafer technology to a power asic process," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 283-292.	
	53	SAITOH et al., "Characterization of directly bonded silicon-on-insulator structures using spectroscopic ellipsometry," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 207-215.	
	54	SAKAKIBARA et al., "A wafer bonded - SOI bipolar transistor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 152-160.	

Examiner Signature /Joannie Garcia/	Date Considered 01/25/2016
-------------------------------------	----------------------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 5 OF 5	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	55	SHAJII et al., "A backside contact technology for a wafer-bonded liquid shear-stress sensor," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 340-347.	
	56	SÖDERBÄRG et al., "Formation of heat sinks using bonding and etch back technique in combination with diamond deposition," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 382-391.	
	57	SOORIAKUMAR et al., "Thermal mismatch strain in anodically bonded silicon and glass," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 225-229.	
	58	STANLEY, Timothy, "Revenue sensitivity to yield and starting wafer cost in SOI SRAM production," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 303-309.	
	59	SUGA, T., "Room-temperature bonding on metals and ceramics," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 71-80.	
	60	TONG et al., "A "smarter-cut" approach to low temperature silicon layer transfer," Appl. Phys. Lett. January 5, 1998, Vol. 72, No. 1, pp. 49-51.	
	61	TONG et al., "Hydrophobic silicon wafer bonding," Appl. Phys. Lett., January 31, 1994, Vol. 64, No. 5, pp. 625-627.	
	62	TONG et al., "Low temperature InP layer transfer," Electronics Letters, February 18, 1999, Vol. 35, No. 4, pp. 341-342.	
	63	TONG et al., "Low temperature wafer direct bonding," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 96-106.	
	64	TONG et al., "Wafer bonding and layer splitting for microsystems**," Advanced Materials, 1999, Vol. 11, No. 17, pp. 1409-1425.	
	65	WELDON et al., "Physics and chemistry of silicon wafer bonding investigated by infrared absorption spectroscopy," Journal of Vacuum Science & Technology B, July/August 1996, Vol. 14, No. 4, pp. 3095-3106.	
	66	YALLUP, Kevin, "Analog CMOS circuits on thick film SOI," Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society Proceedings, Vol. 93-29 (1993), pp. 117-128.	

22415270  
010716

Examiner Signature	/Joannie Garcia/	Date Considered	01/25/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	472066	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
L2	58187	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
L3	865929	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
L4	140	L1 with L2 with L3	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
L5	22	L4 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
L6	19956	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:45
L7	5551	((438/405) or (438/455) or (438/459) or (438/974) or (148/DIG12)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:51
L8	24326	6 or 7	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:51
L9	1406	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room-temperature" or "room T" or "room-T")	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:52
L10	28	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 18:53
L11	4	((4700466) or (4983251) or	US-	OR	OFF	2016/01/25

		("5427638") or ("5451547")).PN.	PGPUB; USPAT; USOCR			18:58
L12	1	("20150303263").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 19:30
L13	86	"planarized insulating material"	US- PGPUB; USPAT; USOCR	OR	ON	2016/01/25 19:30
L14	1	L12 and L13	US- PGPUB; USPAT; USOCR	OR	ON	2016/01/25 19:30
S1	1	("20140203407").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:41
S2	1	("8153505").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:42
S3	1349	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room- temperature" or "room T" or "room-T")	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:47
S4	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room- temperature" or "room T" or "room-T") with ("chemical bond" or "chemical- bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:50
S5	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room- temperature" or "room T" or "room-T") same ("chemical bond" or "chemical- bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:50
S6	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room- temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:51
S7	0	((bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room- T") and ("chemical bond" or "chemical- bond"))).clm.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:51
S8	436228	(bond\$.clm.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:53
S9	53191	(anneal\$.clm.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:53
S10	802974	(heat or heats or heated or heating).clm.	US-	OR	OFF	2014/10/17

			PGPUB; USPAT; USOCR			09:54
S11	134	S8 with S9 with S10	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:54
S12	19293	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:07
S13	6	S11 and S12	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:09
S14	18	S11 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US- PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:50
S15	1386	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room-temperature" or "room T" or "room-T")	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S16	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") with ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S17	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") same ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S18	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S19	0	((bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))).clm.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S20	457036	(bond\$).clm.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S21	56069	(anneal\$).clm.	US- PGPUB; USPAT;	OR	OFF	2015/07/22 15:54

			USOCR			
S22	839493	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S23	138	S20 with S21 with S22	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S24	19807	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S25	6	S23 and S24	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S26	20	S23 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S27	465993	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S28	57339	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S29	855382	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S30	139	S27 with S28 with S29	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S31	21	S30 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S32	1	("20150303263").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:41
S33	1	("5451547").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:41
S34	1286659	adhesive	US-	OR	ON	2015/11/10

			PGPUB; USPAT; USOCR			16:41
S35	0	S33 and S34	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:41
S36	2043	terminated with species	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:45
S37	1	S32 and S36	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:45
S38	909961	etch\$	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:48
S39	1	S33 and S38	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:49
S40	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room- temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:58
S41	28	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room- temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:58
S42	0	S33 and S41	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:58
S43	48227	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching)	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:58
S44	0	S33 and S43	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S45	2042101	bond or bonds or bonded or bonding	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S46	1	S33 and S45	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S47	567781	CMP or polish\$ or planarize or planarizes or planarized or planarizing or planarization	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:04
S48	1	S33 and S47	US- PGPUB;	OR	ON	2015/11/10 17:04

			USPAT; USOCR			
S49	3009473	plasma or gas	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:09
S50	1	S33 and S49	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:09
S51	1	S39 and S46 and S48 and S50	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:10
S52	913511	etch\$ or VSE	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:49
S53	1	S33 and S52	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:49
S54	790750	specie	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:53
S55	0	S33 and S54	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:54
S56	1	("5451547").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/11/14 10:09
S57	1	("20150303263").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/11/14 10:38
S58	85	"planarized insulating material"	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/14 10:43
S59	1	S57 and S58	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/14 10:43

1/ 25/ 2016 7:31:19 PM  
C:\ Users\ jgarcia1\ Documents\ EAST\ Workspaces\ 14957501.wsp






## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

## BIB DATA SHEET

CONFIRMATION NO. 1033

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/957,501	12/02/2015	257	2895	TSSRA.012C1
<b>RULE</b>				
<b>APPLICANTS</b> ZIPTRONIX, INC., Morrisville, NC;				
<b>INVENTORS</b> Qin-Yi Tong, Durham, NC; Gaius Gillman Fountain JR., Youngsville, NC; Paul M. Enquist, Cary, NC;				
<b>** CONTINUING DATA *****</b> This application is a CON of 14/754,111 06/29/2015 which is a DIV of 14/197,070 03/04/2014 PAT 9082627 which is a DIV of 13/341,273 12/30/2011 ABN which is a CON of 12/954,740 11/26/2010 PAT 8153505 which is a CON of 12/720,368 03/09/2010 PAT 7871898 which is a CON of 11/980,664 10/31/2007 PAT 7807549 which is a CON of 10/913,441 08/09/2004 PAT 7387944 which is a CON of 09/505,283 02/16/2000 PAT 6902987				
<b>** FOREIGN APPLICATIONS *****</b>				
<b>** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **</b> 12/11/2015				
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/JOANNIE A GARCIA/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance JAG Initials	<b>STATE OR COUNTRY</b> NC	<b>SHEETS DRAWINGS</b> 9	<b>TOTAL CLAIMS</b> 33
<b>INDEPENDENT CLAIMS</b> 4				
<b>ADDRESS</b> Knobbe, Martens, Olson & Bear, LLP 2040 main Street Fourteenth Floor Irvine, CA 92614 UNITED STATES				
<b>TITLE</b> METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE				
<b>FILING FEE RECEIVED</b> 3200	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit	

<b>Search Notes</b>  	<b>Application/Control No.</b>  14957501	<b>Applicant(s)/Patent Under Reexamination</b>  TONG ET AL.
	<b>Examiner</b>  JOANNIE A GARCIA	<b>Art Unit</b>  2895

CPC- SEARCHED		
Symbol	Date	Examiner
H01L: 21/02032,21/185,21/187,21/2007,21/2022,21/26506,21/30,21/302,21/306,21/3065,21/3226,21/324,21/38,21/46,21/461,21/67092,21/76251,21/76254	01/25/2016	JAG

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	405,455,459,974,FOR103,FOR127,FOR388,FOR395	01/25/2016	JAG
257	459,676,684,701,702,E21.088,E21.122,E21.215,E21.218,E21.219,E21.224,E21.243,E21.245,E21.249,E21.33,E23.02,E23.04	01/25/2016	JAG
148	DIG12	01/25/2016	JAG

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	01/25/2016	JAG

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

--	--

<b>Doc Code: DIST.E.FILE</b> <b>Document Description: Electronic Terminal Disclaimer - Filed</b>		PTO/SB/25 PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce	
Electronic Petition Request	<b>TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION AND TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT</b>		
Application Number	14957501		
Filing Date	02-Dec-2015		
First Named Inventor	Qin-Yi Tong		
Attorney Docket Number	TSSRA.012C1		
Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
<input checked="" type="checkbox"/> Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action  <input checked="" type="checkbox"/> This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.			
Owner		Percent Interest	
ZIPTRONIX, INC.		100 %	
The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)			
14754111    filed on    06/29/2015  as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.  In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.			
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)			

8153505

9082627

6902987

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicants claims the following fee status:

☐ Small Entity

☐ Micro Entity

☒ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 68287

☐ A sole inventor

☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

☐ A joint inventor; all of whom are signing this request

Signature

/Paul Stellman/

Name	Paul Stellman
------	---------------

\*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).  
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	14957501			
<b>Filing Date:</b>	02-Dec-2015			
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE			
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong			
<b>Filer:</b>	Paul Steven Stellman/Anthony Bonilla			
<b>Attorney Docket Number:</b>	TSSRA.012C1			
Filed as Large Entity				
<b>Filing Fees for Utility under 35 USC 111(a)</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
Statutory or Terminal Disclaimer	1814	1	160	160
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>160</b>

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 14957501

Filing Date: 02-Dec-2015

Applicant/Patent under Reexamination: Tong et al.

Electronic Terminal Disclaimer filed on February 8, 2016

☒ APPROVED

**This patent is subject to a terminal disclaimer**

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office



## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24854569
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Anthony Bonilla
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	08-FEB-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	18:23:16
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	5749
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

<b>File Listing:</b>					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	37207	no	3
			ab936ebc4ecd29254e40fcd88d5aa6c0a243df43		
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (SB06)	fee-info.pdf	30677	no	2
			346f24103b946738312373fd73cf1a1ade06f6d5		
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			67884		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Joannie A. Garcia
Art Unit	:	2895
Conf. No.	:	1033

**RESPONSE TO NON-FINAL OFFICE ACTION****Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated February 3, 2016, Applicant submits the following remarks.

**A Listing of Claims** begins on page 2 of this paper.

**Remarks/Arguments** begin on page 6 of this paper.

**LISTING OF THE CLAIMS**

1. (Canceled)
2. (Previously Presented) A bonding method, comprising:  
forming a planarized insulating material on a semiconductor wafer;  
etching the planarized insulating material in a reaction space;  
terminating the planarized insulating material with a nitrogen-containing species  
by at least one of:  
a nitrogen-containing plasma during the etching, and  
a nitrogen-containing solution after the etching;  
bringing a first material into direct contact with the terminated and planarized  
insulating material outside the reaction space; and  
forming a chemical bond between the terminated and planarized insulating  
material and the first material.
3. (Previously Presented) The method of Claim 2, wherein the etching the  
planarized insulating material is conducted in a vacuum chamber, the reaction space comprising  
the vacuum chamber.
4. (Previously Presented) The method of Claim 2, wherein the etching the  
planarized insulating material is conducted in a plasma chamber, the reaction space comprising  
the plasma chamber.
5. (Previously Presented) The method of Claim 2, wherein the etching and the  
terminating comprise exposing the planarized insulating material to the plasma etching process  
in a plasma chamber, the reaction space comprising the plasma chamber.
6. (Previously Presented) The method of Claim 5, wherein the exposing the  
planarized insulating material to the plasma etching process comprises exposing the planarized  
insulating material to a reactive ion etching process.
7. (Previously Presented) The method of Claim 5, wherein the exposing the  
planarized insulating material to the plasma etching process in the plasma chamber comprises  
using nitrogen gas.
8. (Previously Presented) The method of Claim 2, wherein the terminating  
comprises exposing the planarized insulating material to a nitrogen-containing solution after the  
etching.

9. (Previously Presented) The method of Claim 8, wherein the nitrogen-containing solution comprises an ammonia-based solution.

10. (Previously Presented) The method of Claim 2, wherein the first material comprises a second planarized insulating material on a second semiconductor wafer.

11. (Previously Presented) The method of Claim 10, wherein the first material comprises silicon oxide.

12. (Previously Presented) The method of Claim 2, wherein the bringing into direct contact comprises bringing into direct contact the terminated planarized insulating material and a silicon material having a native oxide, the first material comprising the silicon material.

13. (Previously Presented) The method of Claim 2, further comprising, after the terminating, rinsing the insulating material.

14. (Previously Presented) The method of Claim 13, wherein the rinsing comprises immersing the insulating material in deionized water.

15. (Previously Presented) The method of Claim 2, wherein the bringing into direct contact is performed at room temperature.

16. (Previously Presented) The method of Claim 2, wherein the bringing into direct contact is conducted in air.

17. (Previously Presented) The method of Claim 2, wherein the forming the planarized insulating material comprises forming silicon oxide on the semiconductor wafer.

18. (Previously Presented) The method of Claim 2, further comprising forming a bond between the planarized insulating material and the first material with a strength of at least  $500 \text{ mJ/m}^2$  without annealing at more than about  $200^\circ \text{C}$ .

19. (Previously Presented) The method of Claim 2, further comprising forming a bond between the planarized insulating material and the first material with a strength of at least  $2000 \text{ mJ/m}^2$  without annealing at more than about  $200^\circ \text{C}$ .

20. (Previously Presented) The method of Claim 2, further comprising annealing the planarized insulating material and the first material at a temperature of no more than about  $200^\circ \text{C}$  after the bringing into direct contact.

21. (Previously Presented) The method of Claim 2, wherein the planarized insulating material has a surface roughness between about 0.5 and 1.5 nm after the etching and before the bringing into direct contact.

22. (Previously Presented) A bonded structure comprising:  
a first semiconductor material comprising a planarized insulating material having a first bonding surface; and  
a second material having a second bonding surface,  
wherein the first bonding surface is an etched surface terminated with a nitrogen-containing species, and  
wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive.
23. (Previously Presented) The structure of Claim 22, further comprising at least one integrated circuit in the first semiconductor material.
24. (Previously Presented) The structure of Claim 22, wherein the second material comprises silicon.
25. (Previously Presented) The structure of Claim 22, wherein the chemical bond has a strength of at least  $500 \text{ mJ/m}^2$ .
26. (Previously Presented) The structure of Claim 22, wherein the chemical bond has a strength of at least  $2000 \text{ mJ/m}^2$ .
27. (Previously Presented) The structure of Claim 22, wherein the planarized insulating material comprises silicon oxide.
28. (Previously Presented) The structure of Claim 22, wherein the second bonding surface comprises an etched surface.
29. (Previously Presented) The structure of Claim 28, wherein the etched surface of the second bonding surface is terminated with a nitrogen-containing species.
30. (Previously Presented) The structure of Claim 22, wherein the first bonding surface is terminated with a nitrogen-containing species by at least one of a nitrogen-containing plasma during etching and a nitrogen-containing solution after etching.
31. (Previously Presented) The structure of Claim 22, wherein the chemical bond is a covalent bond.
32. (Previously Presented) A bonding method, comprising:  
forming a planarized insulating material on a semiconductor wafer;  
etching the planarized insulating material;

terminating the planarized insulating material with a nitrogen-containing species by at least one of:

a nitrogen-containing plasma during the etching, and  
a nitrogen-containing solution after the etching;

bringing a first material into direct contact with the terminated and planarized insulating material; and

forming a chemical bond between the terminated and planarized insulating material and the first material.

33. (Previously Presented) A bonding method, comprising:

forming a planarized insulating material on a processed semiconductor wafer;

exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas;

terminating the planarized insulating material with a species;

bringing into direct contact the terminated and planarized insulating material and a first material outside of said plasma chamber; and

forming a chemical bond between the terminated and planarized insulating material and the first material.

34. (Previously Presented) The bonding method of Claim 33, wherein the species comprises nitrogen.

### **REMARKS**

By way of summary, Claims 2-34 were pending as of the outstanding Office Action. Claims 2-34 stand rejected. No claims are amended herein. Applicant respectfully requests reconsideration in view of the remarks set forth herein.

Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1 and 6 of U.S. Patent Publication No. US 2015/0303263, which corresponds to U.S. Patent Application No. 14/754,111 (hereinafter “the ‘111 Application”). Claims 22-31 also stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 30 of the ‘111 Application. Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 31 and 36 of the ‘111 Application. Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 60 of the ‘111 Application.

Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 77 and 82 of U.S. Patent No. 8,153,505 (hereinafter “the ‘505 Patent”). Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 115 of the ‘505 Patent. Claims 22-31 also stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 192 and 197 of the ‘505 Patent. Claims 22-31 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claim 230 of the ‘505 Patent.

Claims 2-21 and 32-34 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1 and 9 of U.S. Patent No. 9,082,627 (hereinafter “the ‘627 Patent”). Claims 2-21 and 32-34 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1, 2, and 11 of the ‘627 Patent. Note that there appears to be an erroneous reference to the ‘505 patent in this rejection.

Claims 2-21 and 32-34 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 39, 40, and 48 of the ‘505 Patent. Claims 2-21 and 32-34 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 116, 117, and 126 of the ‘505 Patent. Claims 2-21 and 32-34



stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 154, 155, and 163 of the ‘505 Patent.

Claims 2-21 and 32-34 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 105, 106, and 107 of U.S. Patent 6,902,987 (hereinafter “the ‘987 Patent”).

Without acquiescing to the merits of the double patenting rejections, Applicant files herewith by electronic submission a Terminal Disclaimer for each of the ‘111 Application, the ‘505 Patent, the ‘627 Patent, and the ‘987 Patent, which disclaims, except as provided in the Terminal Disclaimer, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of each of the aforementioned patents and patent application.

Furthermore, as M.P.E.P. § 804.02(II) instructs, “[t]he filing of a terminal disclaimer to obviate a rejection based on nonstatutory double patenting is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. v. Union Sanitary District*, 946 F.2d 870, 20 USPQ2d 1392 (Fed. Cir. 1991). In *Quad Environmental Technologies*, The court indicated that the ‘filing of a terminal disclaimer simply serves the statutory function of removing the rejection of double patenting, and raises neither a presumption nor estoppel on the merits of the rejection.’”

Accordingly, Applicant respectfully submits that the outstanding double patenting rejections are moot and that the Application is in condition for allowance.

#### **No Disclaimers or Disavowals**

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not

**Application No.:** 14/957,501  
**Filing Date:** December 2, 2015

reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

**Co-Pending Applications of Assignee**

Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

<b>Docket No.</b>	<b>Serial No.</b>	<b>Title</b>	<b>Filed</b>
TSSRA.012D2	14/754,111	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE	June 29, 2015
TSSRA.015C3	14/746,425	THREE DIMENSIONAL DEVICE INTEGRATION METHOD AND INTEGRATED DEVICE	June 22, 2015
TSSRA.016C4	14/474,501	METHOD OF ROOM TEMPERATURE COVALENT BONDING	September 2, 2014

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: February 8, 2016

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22646757  
020816

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24856867
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Anthony Bonilla
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	08-FEB-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	18:19:22
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-02-08_Response_TSSRA-012C1.pdf	135954 3ecfd3a7a3cec193b4632c19aa7adf6fb7a3973e	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	8
Warnings:			
Information:			
Total Files Size (in bytes):		135954	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 1 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	3,423,823	01-28-1969	Ansley	
	2	3,488,834	01-13-1970	Baird	
	3	3,508,980	04-28-1970	Jackson, Jr. et al.	
	4	3,534,467	10-20-1970	Sachs et al.	
	5	3,579,391	05-18-1971	Buie	
	6	3,587,166	06-28-1971	Alexander et al.	
	7	3,602,981	09-07-1971	Kool	
	8	3,607,466	09-21-1971	Miyazaki	
	9	3,640,807	02-08-1972	Van Dijk	
	10	3,647,581	03-07-1972	Mash	
	11	3,888,708	06-10-1975	Wise et al.	
	12	4,416,054	11-22-1983	Thomas et al.	
	13	4,612,083	09-16-1986	Yasumoto et al.	
	14	4,617,160	10-14-1986	Belanger et al.	
	15	4,649,630	03-13-1987	Boland et al.	
	16	4,700,466	10-20-1987	Nakagawa et al.	
	17	4,754,544	07-05-1988	Hanak	
	18	4,829,018	05-09-1989	Wahlstrom	
	19	4,935,386	06-19-1990	Nakagawa	
	20	4,939,101	07-03-1990	Black et al.	
	21	4,962,879	10-16-1990	Gösele et al.	
	22	4,963,505	10-16-1990	Fujii et al.	
	23	4,970,175	11-13-1990	Haisma et al.	
	24	4,978,421	12-18-1990	Bassous et al.	
	25	4,983,251	01-08-1991	Haisma et al.	
	26	4,992,149	02-12-1991	Nguyen	
	27	5,007,071	04-09-1991	Nakano	
	28	5,013,471	05-07-1991	Ogawa	
	29	5,024,723	06-18-1991	Gösele et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 2 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	30	5,034,343	07-23-1991	Rouse et al.	
	31	5,070,026	12-03-1991	Greenwald et al.	
	32	5,071,792	12-10-1991	Van Vonno et al.	
	33	5,081,061	01-14-1992	Rouse et al.	
	34	5,087,585	02-11-1992	Hayashi	
	35	5,089,431	02-18-1992	Slatter et al.	
	36	5,121,706	06-16-1992	Nichols et al.	
	37	5,162,251	11-10-1992	Poole et al.	
	38	5,183,783	02-02-1993	Ohta et al.	
	39	5,196,375	03-23-1993	Hoshi	
	40	5,207,864	05-04-1993	Bhat et al.	
	41	5,234,860	08-10-1993	Gluck	
	42	5,236,118	08-17-1993	Bower et al.	
	43	5,238,875	08-24-1993	Ogino	
	44	5,266,511	11-30-1993	Takao	
	45	5,266,824	11-30-1993	Abe	
	46	5,270,259	12-14-1993	Ito et al.	
	47	5,270,261	12-14-1993	Bertin et al.	
	48	5,272,104	12-21-1993	Schrantz et al.	
	49	5,284,707	02-08-1994	Ogawa et al.	
	50	5,321,301	06-14-1994	Sato et al.	
	51	5,324,566	06-28-1994	Ogawa et al.	
	52	5,324,687	06-28-1994	Wojnarowski	
	53	5,354,695	10-11-1994	Leedy	
	54	5,362,659	11-08-1994	Cartagena	
	55	5,376,579	12-27-1994	Annamalai	
	56	5,380,681	01-10-1995	Hsu	
	57	5,383,993	01-24-1995	Katada et al.	
	58	5,407,856	04-18-1995	Quenzer et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 3 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	5,413,955	05-09-1995	Lee et al.	
	60	5,420,449	05-30-1995	Oji	
	61	5,421,953	06-06-1995	Nagakubo et al.	
	62	5,422,302	06-06-1995	Yonehara	
	63	5,427,638	06-27-1995	Goetz et al.	
	64	5,432,729	07-11-1995	Carson et al.	
	65	5,437,894	08-01-1995	Ogawa et al.	
	66	5,441,591	08-15-1995	Imthum et al.	
	67	5,441,911	08-15-1995	Malhi	
	68	5,459,104	10-17-1995	Sakai	
	69	5,460,659	10-24-1995	Krut	
	70	5,485,540	01-16-1996	Eda	
	71	5,489,554	02-06-1996	Gates	
	72	5,497,033	03-05-1996	Fillion et al.	
	73	5,503,704	04-02-1996	Bower et al.	
	74	5,514,235	05-07-1996	Mitani et al.	
	75	5,516,727	05-14-1996	Broom	
	76	5,517,754	05-21-1996	Bellstein, Jr., et. al.	
	77	5,523,602	06-04-1996	Horiuchi	
	78	5,534,465	07-09-1996	Frye et al.	
	79	5,543,648	08-06-1996	Miyawaki	
	80	5,546,494	08-13-1996	Eda	
	81	5,547,896	08-20-1996	Linn et al.	
	82	5,548,178	08-20-1996	Eda et al.	
	83	5,561,303	10-01-1996	Schrantz et al.	
	84	5,563,084	10-08-1996	Ramm et al.	
	85	5,567,657	10-22-1996	Wonjnarowski et al.	
	86	5,569,620	10-29-1996	Linn et al.	
	87	5,580,407	12-03-1996	Haisma et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 4 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	88	5,591,678	01-07-1997	Bendik et al.	
	89	5,627,106	05-06-1997	Hsu	
	90	5,647,932	07-15-1997	Taguchi et al.	
	91	5,650,353	07-22-1997	Yoshizawa et al.	
	92	5,652,436	07-29-1997	Stoner et al.	
	93	5,653,019	08-05-1997	Bernhardt et al.	
	94	5,659,192	08-19-1997	Sarma et al.	
	95	5,661,316	08-26-1997	Kish, Jr., et al.	
	96	5,661,901	09-02-1997	King	
	97	5,666,706	09-16-1997	Tomita et al.	
	98	5,668,057	09-16-1997	Eda et al.	
	99	5,672,240	09-30-1997	Stoner et al.	
	100	5,673,478	10-07-1997	Beene et al.	
	101	5,698,471	12-16-1997	Namba et al.	
	102	5,741,733	04-21-1998	Bertagnolli et al.	
	103	5,747,857	05-05-1998	Eda et al.	
	104	5,753,529	05-19-1998	Chang et al.	
	105	5,755,914	05-26-1998	Yonehara	
	106	5,759,753	06-02-1998	Namba et al.	
	107	5,760,478	06-02-1998	Bazso et al.	
	108	5,763,318	06-09-1998	Bertin et al.	
	109	5,766,984	06-16-1998	Ramm et al.	
	110	5,771,555	06-30-1998	Eda et al.	
	111	5,783,477	07-21-1998	Kish, Jr. et al.	
	112	5,785,874	07-28-1998	Eda et al.	
	113	5,793,115	08-11-1998	Zavracky et al.	
	114	5,804,086	09-08-1998	Bruel	
	115	5,807,783	09-15-1998	Gaul et al.	
	116	5,821,665	10-13-1998	Onishi et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 5 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	117	5,841,197	11-24-1998	Adamic, Jr.	
	118	5,849,627	12-15-1998	Linn et al.	
	119	5,851,894	12-22-1998	Ramm	
	120	5,858,876	01-12-1999	Chew	
	121	5,866,942	02-02-1999	Suzuki et al.	
	122	5,869,354	02-09-1999	Leedy et al.	
	123	5,872,025	02-16-1999	Cronin et al.	
	124	5,876,497	03-02-1999	Atoji	
	125	5,877,034	03-02-1999	Ramm et al.	
	126	5,877,070	03-02-1999	Gösele et al.	
	127	5,877,516	03-02-1999	Mermagen et al.	
	128	5,880,010	03-09-1999	Davidson	
	129	5,889,302	03-30-1999	Liu	
	130	5,902,118	05-11-1999	Hubner	
	131	5,903,018	05-11-1999	Shimawaki	
	132	5,904,860	05-18-1999	Nagakubo et al.	
	133	5,910,669	06-08-1999	Namba et al.	
	134	5,915,167	06-22-1999	Leedy	
	135	5,915,193	06-22-1999	Tong et al.	
	136	5,920,142	07-06-1999	Onishi et al.	
	137	5,936,280	08-10-1999	Liu	
	138	5,966,622	10-12-1999	Levine et al.	
	139	5,980,770	11-09-1999	Ramachandran et al.	
	140	5,982,010	11-09-1999	Namba et al.	
	141	5,990,472	11-23-1999	Rinne	
	142	5,990,562	11-23-1999	Vallett	
	143	5,991,989	11-30-1999	Onishi et al.	
	144	6,004,865	12-21-1999	Horiuchi	
	145	6,004,866	12-21-1999	Nakano et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 6 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	146	6,018,211	01-25-2000	Kanaboshi et al.	
	147	6,048,752	04-11-2000	Lindemann	
	148	6,054,371	09-29-1998	Tsuchiaki et al.	
	149	6,071,761	06-06-2000	Jacobs	
	150	6,087,719	04-23-1998	Tsunashima	
	151	6,087,760	07-11-2000	Yamaguchi et al.	
	152	6,103,009	08-15-2000	Atoji	
	153	6,120,917	09-19-2000	Eda	
	154	6,133,640	10-17-2000	Leedy	
	155	6,136,691	05-26-1998	Chen	
	156	6,143,628	11-07-2000	Sato et al.	
	157	6,146,992	11-14-2000	Lauterbach et al.	
	158	6,153,445	11-28-2000	Yamazaki et al.	
	159	6,153,495	11-28-2000	Kub et al.	
	160	6,154,940	12-05-2000	Onishi et al.	
	161	6,156,624	12-05-2000	Yamagata et al.	
	162	6,165,817	12-26-2000	Akram et al.	
	163	6,180,496	01-30-2001	Farrens et al.	
	164	6,190,778	02-20-2001	Batz-Sohn et al.	
	165	6,194,323	02-27-2001	Downey et al.	
	166	6,197,663	03-06-2001	Chandross et al.	
	167	6,198,159	03-06-2001	Hosoma et al.	
	168	6,236,141	05-22-2001	Sato et al.	
	169	6,242,324	06-05-2001	Kub	
	170	6,246,068	06-12-2001	Sato et al.	
	171	6,255,731	07-03-2001	Ohmi et al.	
	172	6,255,899	07-03-2001	Bertin et al.	
	173	6,270,202	08-07-2001	Namba et al.	
	174	6,274,892	08-14-2001	Kub et al.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 7 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	175	6,284,085	09-04-2001	Gwo	
	176	6,313,012	11-06-2001	Horiuchi	
	177	6,316,332	11-13-2001	Lo et al.	
	178	6,323,108	11-27-2001	Kub et al.	
	179	6,328,796	12-11-2001	Kub	
	180	6,328,841	09-24-1997	Klumpp et al.	
	181	6,448,174	09-10-2002	Ramm	
	182	6,500,694	12-31-2002	Enquist	
	183	6,562,647	05-13-2003	Zandman et al.	
	184	6,563,224	05-13-2003	Leedy	
	185	6,613,678	05-17-1999	Sakaguchi et al.	
	186	6,627,531	09-30-2003	Enquist	
	187	7,553,744	06-30-2009	Tong	
	188	2002/0094661	07-18-2002	Enquist et al.	
	189	2002/0164839	11-07-2002	Enquist	
	190	2002/0173120	11-21-2002	Enquist	
	191	2003/0057423	03-27-2003	Shimoda	
	192	2003/0119279	06-26-2003	Enquist	
	193	2003/0211705	11-13-2003	Tong et al.	
	194	2004/0152282	08-05-2004	Tong et al.	
	195	2006/0292744	12-28-2006	Enquist et al.	
	196	2009/0263953	10-22-2009	Qin-Yi Tong	
	197	8,153,505	04-10-2012	Tong et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	198	EP 0905767 A1	03-31-1999	SHINETSU HANDOTAI KK		
	199	EP 0933810 A1	08-04-1999	CANON KK		

Examiner Signature	Date Considered
--------------------	-----------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 8 OF 22	Attorney Docket No.	TSSRA.012C1

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	200	EP 0209173 A	01-21-1987	PHILIPS NV		
	201	EP 1130647 A2	09-05-2001	HALKIAS GEORGE		
	202	JP S54-116888 A	09-11-1979	HITACHI LTD		
	203	JP S54-155770 A	12-08-1979	NIPPON ELECTRIC CO		
	204	JP S60-167439 A	08-30-1985	NIPPON ELECTRIC CO		
	205	JP S62-031138 A	02-10-1987	NEC CORP		
	206	JP S63-237408 A	10-03-1988	SUMITOMO METAL MINING CO		
	207	JP S63-246841 A	10-13-1988	TOSHIBA CORP		
	208	JP H01-259546 A	10-17-1989	FUJITSU LTD		
	209	JP H02-177435 A	07-10-1990	SONY CORP		
	210	JP H03-070155 A	03-26-1991	OKI ELECTRIC IND CO LTD		
	211	JP H03-101128 A	04-25-1991	CASIO COMPUTER CO LTD		
	212	JP H06-302486	10-28-1994	NIPPONDENSO CO LTD		
	213	JP H08-213548	08-20-1996	FRAUNHOFER GES FORSCHUNG		
	214	JP H10-092702 A	04-10-1998	AGENCY OF IND SCIENCE & TECHNOL		
	215	JP H10-223495	08-21-1998	NIPPON TELEGRAPH & TELEPHONE		
	216	JP H11-335631	12-07-1999	DEGUSSA		
	217	JP 2006-517344 A	07-20-2006	ZIPTRONIX INC		
	218	JP 2008-535230 A	08-28-2008	SOITEC SILICON ON INSULATOR		
	219	KR 1999-0083518	04-27-1999	DEGUSSA		
	220	WO 96/13060 A	05-02-1996	DAIMLER-BENZ AKTIENGESELLSCHAFT		

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 9 OF 22	Attorney Docket No.	TSSRA.012C1

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	221	WO 98/13860	04-02-1998	FRAUNHOFER-GESELLSCHAFT ZUR FÖRDERUNG DER ANGEWANDTEN FORSCHUNG E.V.		
	222	WO 98/45130 A	10-15-1998	LEEDY, Glenn J.		
	223	WO 99/46809	09-16-1999	HARRIS CORPORATION		
	224	WO 01/026137 A	04-12-2001	ZIPTRONIX, INC.		
	225	WO 01/061743 A	08-23-2001	ZIPTRONIX, INC.		
	226	WO 04/071700 A2	08-26-2004	ZIPTRONIX, INC.		
	227	WO 06/111533 A1	10-26-2006	S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	228	"Deliberate Design for Assuring Adequate Thermal Oxide Sidewall at the Corners of Trenches", IBM Technical Disclosure Bulletin, Jul. 1991, pp. 261-262.	
	229	"Metal Oxide Circuits on Silicon Membranes", IBM Technical Disclosure Bulletin, Oct. 1979, p. 2079.	
	230	"Smart Cut: A Promising New SOI Material Technology", M. Bruel et al.; Proceedings 1995 IEEE Int'l SOI Conference, Oct. 1995, pp. 178-179.	
	231	"Wafer Bonding With Stress-Free Trench Isolation", IBM Technical Disclosure Bulletin, Jul. 1991, pp. 304-305.	
	232	"Fabrication on Planar Arrays of Semiconductor Chips Separated by Insulating Barriers," IBM Technical Disclosure Bulletin, Apr. 1965, p. 1103.	
	233	A. Berthold, et al., Sensors and Actuators, vol. A68, pp. 410-413, "Wafer-to-Wafer Fusion Bonding of Oxidized Silicon to Silicon at Low Temperatures", 1998.	
	234	A. Kazor, et al., Appl. Phys. Lett., vol. 65, No. 12, pp. 1572-1574, "Fluorine Enhanced Oxidation of Silicon at Low Temperatures", Sep. 19, 1994.	
	235	A. Plössl, et al., Materials Science & Engineering, vol. R 25, Nos. 1-2, pp. 1-88, "Wafer Direct Bonding: Tailoring Adhesion Between Brittle Materials", Mar. 10, 1999.	
	236	A. von Keudell, et al., Appl. Phys. Lett., vol. 71, No. 26, pp. 3832-3834, "Evidence for Atomic H Insertion Into Strained Si-Si Bonds in the Amorphous Hydrogenated Silicon Subsurface From in Situ Infrared Spectroscopy", Dec. 29, 1997.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 10 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	237	A.H. Mahan, et al., Physical Review B., vol. 40, No. 17, pp. 12024-12027, "Characterization of Microvoids in device-quality Hydrogenated Amorphous Silicon by Small-Angle X-Ray Scattering and Infrared Measurements", Dec. 15, 1989.	
	238	Alex Q. Huang, IEEE Transactions on Electron Devices, vol. 43, No. 6, pp. 1029-1032, "Analysis of the Inductive Turn-Off of Double Gate MOS Controlled Thyristors", Jun. 1996.	
	239	Amirfeiz et al., "Formation of Silicon Structures by Plasma Activated Wafer Bonding", Proceedings of the 5.sup.th Semiconductor Wafer Bonding Symposium, Oct. 1999, 11 pages.	
	240	Andreas Plössl et al., "The Interface of Silicon Sampled Joined at Room Temperature by Wafer Direct Bonding in Ultrahigh Vacuum", Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology, vol. 2, pp. 1361-1372, 1998.	
	241	Andreas Schumacher et al., The Bonding Energies of Oxidized Silicon Wafers for Micromechanical Applications at Moderate Temperatures, 97-36 Electrochemical Society Proceedings 155 (1998).	
	242	Auberton-Herve, et al., Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology, Silicon Materials Science and Technology, vol. 2, Electrochemical Society Proceedings, vol. 98-1, pp. 1341-1360, "Silicon on Insulator Wafers Using the Smart Cut.RTM. Technology", 1998.	
	243	B. Agarwal, et al., IEEE Electron Device Letters, vol. 18, No. 5, pp. 228-231, "A 227-GHz fmax Transferred-Substrate Heterojunction Bipolar Transistor", May 1997.	
	244	B. Anthony et al., "In situ Cleaning of Silicon Substrate Surfaces by Remote Plasma-Excited Hydrogen" J. Vac. Sci. Technol. B7, 621-626 (Jul./Aug. 1989), American Vacuum Society 1989.	
	245	B. Aspar et al., "Smart-Cut Process Using Metallic Bonding Application to Transfer of Si, GaAs, InP thin films", Electronics Letters, Jun. 10, 1999, vol. 35, No. 12 pp. 1024-1025.	
	246	B. Aspar, et al., Microelectronic Engineering, vol. 36, pp. 233-240, "Basic Mechanisms Involved in the Smart-Cut.RTM. Process", 1997.	
	247	B.E. Roberds, et al., Electrochemical Society Proceedings, vol. 97-36, pp. 592-597, "Wafer Bonding of GaAs, InP, and Si Annealed Without Hydrogen for Advanced Device Technologies," 1997.	
	248	B.E. Roberds, et al., Electrochemical Society Proceedings, vol. 97-36, pp. 598-606, "Low Temperature, in Situ, Plasma Activated Wafer Bonding," 1997.	
	249	B.M. Arora, et al., J. Vac. Sci. Technol. vol. B5, No. 4, pp. 876-882, "Reactive Ion-Etching-Induced Damage in Silicon Using SF6 Gas Mixtures", Jul./Aug. 1987.	
	250	Barry E. Burke, et al., Soft-X-Ray CCD Imagers for AXAF, IEEE Transactions on Electron Devices, vol. 44, No. 10, Oct. 1997, pp. 1633-1642.	
	251	Baumgart et al., "Evaluation of Wafer Bonding and Etch Back for Soi Technology" Philips J. Res., vol. 49, No. 1/2 (1995) 91-124.	
	252	Bernard S. Meyerson, et al., Appl. Phys. Lett., vol. 57, No. 10, pp. 1034-1036, "Bistable Conditions for Low-Temperature Silicon Epitaxy", Sep. 3, 1990.	
	253	Biermann et al., "Direct Bonding: From an Optical Technology to a Broad Research Topic" Special Issue on Direct Bonding, Philips J. Res., vol. 49, p. 1-10, 1995.	
	254	Bollmann et al., Three Dimensional Metallization for Vertically Integrated Circuits, 1997 Materials for Advanced Metallization MAM '97 Abstracts Booklet 94.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 11 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	255	Burhan Bayraktaroglu, et al., IEEE Electron Device Letters, vol. 14, No. 10, pp. 493-495, "Very High-Power-Density CW Operation of GaAs/AlGaAs Microwave Heterojunction Bipolar Transistors", Oct. 1993.	
	256	C. B. Eom et al., Fabrication of Double Sided YBa2Cu3O7 Thin Films on 2 Inch Diameter LaAlO3 Wafers by Direct Wafer Bonding, 7 IEEE Transactions on Applied Superconductivity 1244 (1997).	
	257	C. den Besten, et al., IEEE Micro Electro Mechanical Systems, pp. 104-109, "Polymer Bonding of Micro-Machined Silicon Structures", Feb. 4-7, 1992.	
	258	C. Gui et al., "Present and Future Role of Chemical Mechanical Polishing in Wafer Bonding", Journal of the Electrochemical Society, vol. 145, No. 6, pp. 2198-2204, Jun. 1998.	
	259	C. Harendt et al., "Vertical Polysilicon Interconnects by Aligned Wafer Bonding," 97-36 Electrochemical Society Proceedings 501 (1998).	
	260	Ciarlo, Dino R., Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 93-29, pp. 313-326, "High- and Low-Temperature Bonding Techniques for Microstructures", May 1993.	
	261	Cynthia A. Desmond et al., Low-Temperature Atmospheric Silicon-Silicon Wafer Bonding for Power Electronic Applications, 97-36 Electrochemical Society Proceedings 459 (1998).	
	262	D. Graf, et al., J. Vac. Sci. Technol., A7(3), pp. 808-813, "Reaction of Water with Hydrofluoric Acid Treated Silicon (111) and (100) Surfaces", May/Jun. 1989.	
	263	D.E. Booth et al., Backside Imaging CCD Using Bonded and Etched Back Silicon on Epoxy, 97-36 Electrochemical Society Proceedings 584 (1998).	
	264	Darrell Hill, et al., IEEE Microwave and Guided Wave Letters, vol. 5, No. 11, pp. 373-375, "Novel HBT with Reduced Thermal Impedance", Nov. 1995.	
	265	David W. Oberlin, A New Air-Isolation Process for Monolithic Integrated Circuits, 17 IEEE Transactions on Electron Devices 485 (1970).	
	266	Diego Feijoó et al., Silicon Wafer Bonding Studied by Infrared Absorption Spectroscopy, 65 Applied Physics Letters 2548, 2548 (1994).	
	267	Donato Pasquariello, et al., Journal of the Electrochemical Society, vol. 147, No. 6, pp. 2343-2346, "Mesa-Spacers: Enabling Nondestructive Measurement of Surface Energy in Room Temperature Wafer Bonding", 2000.	
	268	Donato Pasquariello, et al., Journal of the Electrochemical Society, vol. 147, No. 7, pp. 2699-2703, "Oxidation and Induced Damage in Oxygen Plasma in Situ Wafer Bonding", 2000.	
	269	E. Bertagnolli, et al., Interchip Via Technology Three-Dimensional Metallization for Vertically Integrated Circuits, Electrochemical Society Proceedings, vol. 97-36, pp. 509-520 (2000).	
	270	E. Jalaguier et al., "Transfer of 3 in GaAs Film on Silicon Substrate by Proton Implantation Process", Electronic Letters, Feb. 19, 1998, vol. 34, No. 4 pp. 408-409.	
	271	E. Jalaguier et al., Transfer of Thin InP Films onto Silicon Substrate by Proton Implantation Process, 11th Int. Conf. on Indium Phosphide and Related Materials, May 16-20, IEEE 1999, pp. 26-27.	
	272	Egloff et al., "Evaluation of Strain Sources in Bond and Etchback Silicon-on-Insulator" Philips J. Res. 49 (1995) pp. 125-138.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 12 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	273	Eliezer M. Rabinovich, et al., J. Am. Ceram. Soc., vol. 72, No. 7, pp. 1229-1232, "Retention of Fluorine in Silica Gels and Glass", 1989.	
	274	EP 01 92 0489; European Search Report; Jun. 6, 2003, 4 pages.	
	275	F.J. Kub et al., "Single-Crystal Ferroelectric Microwave Capacitor Fabricated by Separation by Hydrogen Implantation", Electronics Letters, Mar. 18, 1999, vol. 35, No. 6, pp. 477-478.	
	276	F.J. Kub, et al., The 1999 Joint International Meeting, vol. 99-2, Abstract No. 1031, 1 page, "A Double-Side IGBT by Low Temperature Wafer Bonding," Oct. 17-22, 1999.	
	277	Farrens et al., "Chemical Free Room Temperature Wafer to Wafer Direct Bonding", J. Electrochem. Soc., vol. 142, No. 11, Nov. 1995, pp. 3949-3955.	
	278	Farzad Pourahmadi, et al., IEEE Solid-State Sensor and Actuator Workshop: Technical Digest, pp. 144-147, "Variable-Flow Micro-Valve Structure Fabricated with Silicon Fusion Bonding", Jun. 4-7, 1990.	
	279	Fritz J. Kub et al., Electrical Characteristics of Low Temperature Direct Silicon-Silicon Bonding for Power Device Applications, 97-36 Electrochemical Society Proceedings 466 (1998).	
	280	Fromm et al., Interaction of Oxygen and Nitrogen With Clean Transition Metal Surfaces, Surface Science 74 (1978) pp. 259-275.	
	281	G. Hess, et al., Appl. Phys. Lett., vol. 71, No. 15, pp. 2184-2186, "Evolution of Subsurface Hydrogen From Boron-Doped Si(100)," Oct. 13, 1997.	
	282	G. Krauter et al., "Low Temperature Silicon Direct Bonding for Application in Micromechanics: Bonding Energies for Different Combinations of Oxides", Sensors and Actuators A 70, 271-275, 1998 Elsevier Science S.A.	
	283	G.A.C.M. Spierings, et al., "Direct Bonding of Organic Polymeric Materials", Philips J. Res. 49 (1995) pp. 139-149.	
	284	G.A.C.M. Spierings, et al., Philips Journal of Research, vol. 49, No. 1/2, pp. 47-63, "Surface-Related Phenomena in the Direct Bonding of Silicon and Fused-Silica Wafer Pairs", 1995.	
	285	G.A.C.M. Spierings, et al., Proceedings of the First International Symposium on Semiconductor Wafer Bonding. Science, Technology, and Applications, Proceedings vol. 92-7, pp. 18-32, "Diversity and Interfacial Phenomena in Direct Bonding", (1992).	
	286	George P. Imthum, et al., J. Appl. Phys., vol. 72, No. 6, pp. 2526-2527, "Bonded Silicon-on-Sapphire Wafers and Devices", Sep. 15, 1992.	
	287	Goetz, "Generalized Reactive Bonding," Proceedings of the 1 <sup>st</sup> Semiconductor Wafer Bonding Symposium, 1991, pp. 65-73.	
	288	Gösele, U., et al., "Semiconductor Wafer Bonding, a Flexible Approach to Materials Combinations in Microelectronics, Micromechanics and Optoelectronics", 1997 IEEE, pp. 23-32.	
	289	Gudrun Kissinger, et al., Sensors and Actuators, vol. A36, pp. 149-156, "Void-Free Silicon-Wafer-Bond Strengthening in the 200-400°C Range", 1993.	
	290	H. J. Quenzer et al., Low Temperature Wafer Bonding for Micromechanical Applications, 1992 Micro Electro Mechanical Systems, 1992, MEMS '92 49, 52.	
	291	H. Takagi, et al., Appl. Phys. Lett., vol. 68, No. 16, pp. 2222-2224, "Surface Activated Bonding of Silicon Wafers at Room Temperature," Apr. 15, 1996.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 13 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	292	H. Takagi, et al., Jpn. J. Appl. Phys. vol. 28, Part 1, No. 3A, pp. 1589-1594, "Transmission Electron Microscope observations of Si/Si Interface Bonded at Room Temperature by Ar Beam Surface Activation", Mar. 1999.	
	293	Haisma et al., "Diversity and Feasibility of Direct Bonding: A Survey of a Dedicated Optical Technology", Applied Optics, 33, pp. 1154-1169 (Mar. 1994).	
	294	Haisma et al., "Non-Silicon Applications of Direct Bonding" Philips J. Res. 49 (1995) pp. 151-163.	
	295	Haisma et al., "Silicon-Wafer Fabrication and (Potential) Applications of Direct-Bonded Silicon", Philips J. Res. 49 (1995) pp. 65-89.	
	296	Haisma et al., "Surface Preparation and Phenomenological Aspects of Direct Bonding", Philips J. Res. 49 (1995) pp. 23-46.	
	297	Henry Nielsen, et al., J. Electrochem. Soc.: Solid-State Science and Technology, vol. 130, No. 3, pp. 708-711, "Some Illumination on the Mechanism of SiO <sub>2</sub> Etching in HF Solutions", Mar. 1983.	
	298	Hideki Takagi et al., "Low-Temperature Direct Bonding of Silicon and Silicon Dioxide by the Surface Activation Method", Sensors and Actuators A, vol. 70, No. 1-2, pp. 164-170, Oct. 1, 1998.	
	299	Hideki Takagi, et al., Appl. Phys. Lett., vol. 74, No. 16, pp. 2387-2389, "Room-Temperature Bonding of Lithium Niobate and Silicon Wafers by Argon-Beam Surface Activation", Apr. 19, 1999.	
	300	Hideki Yokoi et al., Analysis of GaInAsP Surfaces by Contact-Angle Measurement for Wafer Direct Bonding with Garnet Crystals, 38 Japanese J. Applied Physics 4780 (1999).	
	301	Hochbauer, et al., Appl. Phys. Lett., vol. 75, No. 25, pp. 3938-3940, "Hydrogen Blister Depth in Boron and Hydrogen Coimplanted N-Type Silicon", Dec. 20, 1999.	
	302	Hyeokjae Lee, et al., IEDM Technical Digest, vol. 95-683, pp. 28.2.1-28.2.4, "A New Leakage Component Caused by the Interaction of Residual Stress and the Relative Position of Poly-Si Gate at Isolation Edge", Dec. 10-13, 1995.	
	303	International Conference on Compliant & Alternative Substrate Technology, Meeting Program & Abstract Book, Sep. 19-23, 1999 Disney's Boardwalk Inn, Lake Buena Vista, FL total of 6 pages.	
	304	Itoh et al., "Room temperature vacuum sealing surface activated bonding method," June 8-12, 2003, IEEE, pp. 1828-1831.	
	305	J. Bagdahn, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 291-298, "Characterization of Directly Bonded Silicon Wafers by Means of the Double Cantilever Crack Opening Method", (1998).	
	306	J. Haisma et al., "Silicon-on-Insulator Wafer Bonding-Wafer Thinning"; Japanese J. Appl. Phys, vol. 28, No. 8; pp. 1426-1443; 1989.	
	307	J. Haisma, "Direct Bonding in Patent Literature ", Philips Journal of Research, vol. 49, No. 1/2 (1995), pp. 165-170.	
	308	J. Haisma, "Direct Bonding: Retrospect and Outlook", Philips Journal of Research, vol. 49, No. 1/2 (1995), pp. 171-177.	
	309	J. Köhler et al., Weibull Fracture Probability for Silicon Wafer Bond Evaluation, 147 J. Electrochemical Society 4683, 4683, 4685 (2000).	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 14 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	<b>310</b>	J.B. Lasky, Appl. Phys. Lett., vol. 48, No. 1, "Wafer Bonding for Silicon-on-Insulator Technologies", Jan. 6, 1986.	
	<b>311</b>	J.B. Lasky, et al., IEDM Technical Digest, vol. 85, pp. 684-687, "Silicon-on-Insulator (SOI) by Bonding and Etch-Back", Dec. 1-4, 1985.	
	<b>312</b>	J.F. Jensen, et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 10, pp. 1119-1127, "A 3.2-GHz Second-Order Delta-Sigma Modulator Implemented in InP HBT Technology", Oct. 1995.	
	<b>313</b>	J.F. Klem et al., "Characterization of Thin AlGaAs/InGaAs/GaAs Quantum-Well Structure Bonded Directly to SiO <sub>2</sub> /Si and Glass Substrates," J. Appl. Phys., 66(1), Jul. 1989, pp. 459-462.	
	<b>314</b>	Jan Haisma et al., "Frameworks for Direct Bonding", Philips J. Res. 49 (1995) pp. 11-21.	
	<b>315</b>	Japanese Office Action issued May 29, 2012, in Patent Application No. 2001-560438 (with English Translation).	
	<b>316</b>	Jeffrey T. Borenstein, et al., J. Appl. Phys., vol. 73, No. 6, pp. 2751-2754, "Kinetic Model for Hydrogen Reactions in Boron-Doped Silicon", Mar. 15, 1993.	
	<b>317</b>	Jiwei Jiao, et al., Sensors and Actuators, vol. A50, pp. 117-120, "Low-Temperature Silicon Direct Bonding and Interface Behaviours", 1995.	
	<b>318</b>	John S. Judge, J. Electrochem. Soc.: Solid State Science, vol. 118, No. 11, pp. 1772-1775, "A Study of the Dissolution of SiO <sub>2</sub> in Acidic Fluoride Solutions", Nov. 1971.	
	<b>319</b>	K. Bergman, et al., Physical Review B, vol. 37, No. 5, pp. 2770-2773, "Donor-Hydrogen Complexes in Passivated Silicon", Feb. 15, 1988.	
	<b>320</b>	K. Henttinen et al., Mechanically Induced Si Layer Transfer in Hydrogen-Implanted Si Wafers, 76 Applied Physics Letters 2370 (2000).	
	<b>321</b>	K.D. Hobart et al., Fabrication of a Double-Side IGBT by Very Low Temperature Wafer Bonding, 1999 Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs 45, 46 (1999).	
	<b>322</b>	K.D. Hobart, et al., Applied Physics Letters, vol. 72, No. 9, pp. 1095-1097, "Characterization of Si pn Junctions Fabricated by Direct Wafer Bonding in Ultra-High Vacuum," Mar. 2, 1998.	
	<b>323</b>	Karin Ljungberg et al., Improved Direct Bonding of Si and SiO <sub>2</sub> Surfaces by Cleaning in H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :HF, 67 Applied Physics Letters 650 (1995).	
	<b>324</b>	Karin Ljungberg, et al., Appl. Phys. Lett., vol. 62, No. 12, pp. 1362-1364, "Spontaneous Bonding of Hydrophobic Silicon Surfaces", Mar. 22, 1993.	
	<b>325</b>	Karin Ljungberg, et al., Electrochemical Society Proceedings, vol. 95-7, pp. 163-173, "Modification of Silicon Surfaces with H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :HF and HNO <sub>3</sub> :HF for Wafer Bonding Applications", (1996).	
	<b>326</b>	Kim, et al., Appl. Phys. Lett., vol. 69, No. 25, pp. 3869-3871, "Effects of B Doping on Hydrogen Desorption from Si(001) During Gas-Source Molecular-Beam Epitaxy From Si <sub>2</sub> H <sub>6</sub> and B <sub>2</sub> H <sub>6</sub> ," Dec. 16, 1996.	
	<b>327</b>	Kiyoshi Mitani, et al., Jpn. J. Appl. Phys., vol. 30, No. 4, pp. 615-622, "Causes and Prevention of Temperature-Dependent Bubbles in Silicon Wafer Bonding", Apr. 1991.	
	<b>328</b>	Kiyoshi Mitani, et al., Jpn. J. Appl. Phys., vol. 31, Part 1, No. 4, pp. 969-974, "A New Evaluation Method of Silicon Wafer Bonding Interfaces and Bonding Strength by KOH Etching", Apr. 1992.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 15 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	<b>329</b>	Ko, W.H., et al., Micromachining and Micropackaging of Transducers, pp. 41-61, "Bonding Techniques for Microsensors", 1985.	
	<b>330</b>	Korean Office Action issued Dec. 28, 2011, in Patent Application No. 10-2011-7015751 (with English-language translation).	
	<b>331</b>	Korean Office Action Issued Nov. 27, 2012 in Patent Application No. 10-2011-7015751 (with English translation).	
	<b>332</b>	Kouvatsos, et al., Appl. Phys. Lett., vol. 61, No. 7, pp. 780-782, "Silicon-Fluorine Bonding and Fluorine Profiling in SiO <sub>2</sub> Films Grown by NF <sub>3</sub> -Enhanced Oxidation", Aug. 17, 1992.	
	<b>333</b>	Ku et al., "Low Stress Tungsten Absorber for X-Ray Masks", Microelectronic Engineering, vol. 11, No. 1-4, Apr. 1990, pp. 303-308.	
	<b>334</b>	L. Di Cioccio et al., "Silicon Carbide on Insulator Formation Using the Smart Cut Process", Electronics Letters, Jun. 6, 1996, vol. 32, No. 12, pp. 1144-1147.	
	<b>335</b>	L. Rayleigh, Proceedings of the Royal Society of London, Series A-Mathematical and Physical Sciences, vol. 156, pp. 326-349, "A Study of Glass Surfaces in Optical Contact", Sep. 1, 1936.	
	<b>336</b>	Lehmann et al., "Bubble-Free Wafer Bonding of GaAs and InP on Silicon in a Microcleanroom", Jpn. J. Appl. Phys., 28, pp. 2141-2143 (Dec. 1989).	
	<b>337</b>	Leslie A. Field, et al., Sensors and Actuators, vol. A21-A23, pp. 935-938, "Fusing Silicon Wafers with Low Melting Temperature Glass", 1990.	
	<b>338</b>	Li et al., Low temperature direct bonding using pressure and temperature, SPIE, vol. 3184, 124-27 (1997).	
	<b>339</b>	Lusson, et al., J. Appl. Phys., vol. 81, No. 7, pp. 3073-3080, "Hydrogen Configurations and Stability in Amorphous Sputtered Silicon", Apr. 1, 1997.	
	<b>340</b>	M. Bruel, Electronics Letters, vol. 31, No. 14, pp. 1201-1202, "Silicon on Insulator Material Technology", Jul. 6, 1995.	
	<b>341</b>	M. Grundner, et al., Appl. Phys. A, vol. 39, pp. 73-82, "Investigations on Hydrophilic and Hydrophobic Silicon (100) Wafer Surfaces by X-Ray Photoelectron and High-Resolution Electron Energy Loss-Spectroscopy", 1986.	
	<b>342</b>	M. Morita, et al., Appl. Phys. Lett., vol. 45, No. 12, pp. 1312-1314, "Fluorine-Enhanced Thermal Oxidation of Silicon in the Presence of NF <sub>3</sub> ", Dec. 15, 1984.	
	<b>343</b>	M. Petzold, et al., Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications Proceedings vol. 95-7, pp. 380-389, "Interface Strength Characterization of Bonded Wafers" (1995).	
	<b>344</b>	M. S. Ismail et al., One-Step Direct Bonding Process of Low Temperature Si <sub>3</sub> N <sub>4</sub> and TiN Technology, 1993 Proceedings of the 7th International Conference on Solid State Sensors and Actuators, 188 (1993).	
	<b>345</b>	M. Shimbo, et al., J. Appl. Phys., vol. 60, No. 8, pp. 2987-2989, "Silicon-to-Silicon Direct Bonding Method", Oct. 15, 1986.	
	<b>346</b>	M. Yoshimaru, et al., J. Vac. Sci. Technol. A, vol. 15, No. 6, pp. 2915-2922, "Interaction Between Water and Fluorine-Doped Silicon Oxide Films Deposited by Plasma-Enhanced Chemical Vapor Deposition", Nov./Dec. 1997.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 16 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	347	M.E. Grupen-Shemansky et al., "Stress in GaAs Bonded to Si", Proceedings of 1st International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, vol. 92-7, The Electrochemical Society, Pennington, NJ, 1992, pp. 132-145.	
	348	M.K. Weldon, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 229-248, "Mechanistic Studies of Silicon Wafer Bonding and Layer Exfoliation", (1998).	
	349	Martin A. Schmidt, Wafer-To-Wafer Bonding for Microstructure Formation, 86 Proceedings of the IEEE 1575, 1578 (1998).	
	350	Maszara et al., "Role of Surface Morphology in Wafer Bonding", J. Appl. Phys. 69(1) (Jan. 1991) pp. 257-260.	
	351	Michalske et al., "Closure and Repropagation of Healed Cracks in Silicate Glass," Journal of American Ceramic Society, vol. 68 pp. 586-590 (1985).	
	352	Mitani, Kiyoshi, Wafer Bonding: Studies of Interface Bubbles and Electrical Characterization, Department of Electrical Engineering, Duke University, 1991.	
	353	Mohd Salleh Ismail et al., Digital Pressure-Switch Array with Aligned Silicon Fusion Bonding, 1 J. Micromechanics and Microengineering 231 (1991).	
	354	N.Q. Khanh, et al., J. Electrochem. Soc., vol. 142, No. 7, pp. 2425-2429, "Nondestructive Detection of Microvoids at the interface of Direct Bonded Silicon Wafers by Scanning Infrared Microscopy", Jul. 1995.	
	355	Nakamura, et al., IEDM Technical Digest, vol. 95, pp. 889-892, "Giga-Bit DRAM Cells with Low Capacitance and Low Resistance Bit-Lines on Buried MOSFET's and Capacitors by Using Bonded SOI Technology-Reversed-Stacked-Capacitor (RSTC) Cell-", Dec. 10-13, 1995.	
	356	Nakanishi et al., "Studies on SiO <sub>2</sub> -SiO <sub>2</sub> Bonding with Hydrofluoric Acid-Room Temperature and Low Stress Bonding Technique for MEMS-", IEEE 1998, pp. 609-614.	
	357	Niwano, et al., J. Appl. Phys., vol. 71, No. 11, pp. 5646-5649, "Morphology of Hydrofluoric Acid and Ammonium Fluoride-Treated Silicon Surfaces Studied by Surface Infrared Spectroscopy", Jun. 1, 1992.	
	358	No Author, Electronics Letters, vol. 14, No. 18, pp. 593-594, "C.M.O.S. Devices Fabricated on Buried SiO <sub>2</sub> Layers Formed by Oxygen Implantation into Silicon", Aug. 31, 1978.	
	359	Office Action issued August 19, 2014 in Japanese Patent Application No. 2012-107053 (with English language translation)	
	360	Office Action issued Jan. 8, 2013 in Japanese Patent Application No. 2001-560438 (English language translation only).	
	361	Office Action issued May 13, 2014 In Japanese Patent Application No. 2013 -143038 with English language translation	
	362	Office Action issued Oct. 15, 2013 in Japanese patent Application No. 2001-560438 with English language translation.	
	363	Office Action mailed on Dec. 17, 2013, in Japanese Patent Application 2012-107053 (English Translation Only).	
	364	P. Gupta, et al., Physical Review B, vol. 37, No. 14, pp. 8234-8243, "Hydrogen Desorption Kinetics From Monohydride and Dihydride Species on Silicon Surfaces", May 15, 1988.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 17 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	<b>365</b>	P.J.H. Denteneer, et al., Physical Review B, vol. 39, No. 15, pp. 10809-10824, "Microscopic Structure of the Hydrogen-Boron Complex in Crystalline Silicon", May 15, 1989.	
	<b>366</b>	Peter Bjeletich, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 349-357, "Electrical Characterization of Plasma Bonded SOI", (1999).	
	<b>367</b>	Peter J. Wright, et al., IEEE Transactions on Electron Devices, vol. 36, No. 5, pp. 879-889, "The Effect of Fluorine in Silicon Dioxide Gate Dielectrics", May 1989.	
	<b>368</b>	Peter P. Gillis, et al., Journal of Applied Physics, vol. 35, No. 3 (Part I), pp. 647-658, "Double-Cantilever Cleavage Mode of Crack Propagation", Mar. 1964.	
	<b>369</b>	Petersen et al., "Silicon fusion bonding for pressure sensors," in Technol. Dig. IEEE Solid State Sens. & Actuators Workshop, Hilton Head, SC, 1988, pp. 144-147.	
	<b>370</b>	Plossl, et al., Mat. Res. Soc. Symp. Proc., vol. 483, pp. 141-146, "Covalent Silicon Bonding at Room Temperature in Ultrahigh Vacuum," 1998.	
	<b>371</b>	Q. Lee, et al., IEEE Electron Device Letters, vol. 19, No. 3, pp. 77-79, "A > 400 GHz fmax Transferred-Substrate Heterojunction Bipolar Transistor IC Technology", Mar. 1998.	
	<b>372</b>	Q. Lee, et al., IEEE Electron Device Letters, vol. 20, No. 8, pp. 396-398, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors", Aug. 1999.	
	<b>373</b>	Q.-Y. Tong, "Room Temperature Silicon and SiO <sub>2</sub> Covalent Bonding in Ambient," Dec. 10, 1999, 9 pages.	
	<b>374</b>	Q.-Y. Tong et al, "The Role of Surface Chemistry in Bonding of Standard Silicon Wafers," J. Electrochem. Soc., vol. 144, No. 1, pp. 384-389 (Jan. 1997).	
	<b>375</b>	Q.-Y. Tong et al., "Wafer Bonding of Si With Dissimilar Materials," pp. 524-526 (1995).	
	<b>376</b>	Q.-Y. Tong et al., 1999 IEEE International SOI Conference, pp. 104-105, "IOS-A New Type of Materials Combination for System-on-a Chip Preparation," Oct. 1999.	
	<b>377</b>	Q.-Y. Tong et al., Adv. Mater., vol. 11, No. 17, pp. 1409-1425, "Wafer Bonding and Layer Splitting for Microsystems", 1999.	
	<b>378</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 64, No. 5, pp. 625-627, "Hydrophobic Silicon Wafer Bonding," Jan. 31, 1994.	
	<b>379</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 70, No. 11, pp. 1390-1392, "Layer Splitting Process in Hydrogen-Implanted Si, Ge, SiC, and Diamond Substrates", Mar. 17, 1997.	
	<b>380</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 72, No. 1, pp. 49-51, "A "Smarter-Cut" Approach to Low Temperature Silicon Layer Transfer", Jan. 5, 1998.	
	<b>381</b>	Q.-Y. Tong et al., Diffusion and Oxide Viscous Flow Mechanism in SDB Process and Silicon Wafer Rapid Thermal Bonding, 26 Electronic Letters 697 (1990).	
	<b>382</b>	Q.-Y. Tong et al., Electrochemical and Solid-State Letters, vol. 1, No. 1, pp. 52-53, "Low Vacuum Wafer Bonding", 1998.	
	<b>383</b>	Q.-Y. Tong et al., Electronics Letters, vol. 35, No. 4, pp. 341-342, "Low Temperature InP Layer Transfer", Feb. 18, 1999.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 18 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	384	Q.-Y. Tong et al., Feasibility Study of VLSI Device Layer Transfer by CMP PETEOS Direct Bonding, Proceedings 1996 IEEE International SOI Conference, Oct. 1996 pp. 36 and 37.	
	385	Q.-Y. Tong et al., J. Electrochem. Soc., vol. 143, No. 5, pp. 1773-1779, "A Model of Low-Temperature Wafer Bonding and its Applications", May 1996.	
	386	Q.-Y. Tong et al., Low Temperature Si Layer Splitting, 1997 Proceedings 1997 IEEE International SOI Conference 126.	
	387	Q.-Y. Tong et al., Materials Chemistry and Physics, vol. 37, pp. 101-127, "Semiconductor Wafer Bonding: Recent Developments", 1994.	
	388	Q.-Y. Tong et al., MRS Bulletin, pp. 40-44, "Beyond "Smart-Cut.RTM.": Recent Advances in Layer Transfer for Material Integration", Dec. 1998.	
	389	Q.-Y. Tong et al., Semiconductor Wafer Bonding Science and Technology, John Wiley & Sons, Inc., 1999.	
	390	Q.-Y. Tong et al., Silicon Carbide Wafer Bonding, 142 J. Electrochemical Society 232 (1995).	
	391	Q.-Y. Tong et al., Thickness Considerations in Direct Silicon Wafer Bonding, 142 J. Electrochemical Society 3975 (1995).	
	392	Q.-Y. Tong et al., Transfer of Semiconductor and Oxide Films by Wafer Bonding and Layer Cutting, 29 J. Electronic Materials 928 (2000).	
	393	Qing-An Huang et al., Biased-Voltage Controlled Thinning for Bonded Silicon-On-Insulator Wafers, 66 Applied Physics Letters 2990 (1995).	
	394	R. Dekker, et al., IEDM Technical Digest, vol. 97, pp. 921-923, "An Ultra Low-Power RF Bipolar Technology on Glass", Dec. 7-10, 1997.	
	395	R. Kasi, et al., Appl. Phys. Lett., vol. 58, No. 25, pp. 2975-2977, "Chemistry of Fluorine in the Oxidation of Silicon", Jun. 24, 1991.	
	396	R. Stengl, et al., Jpn. J. Appl. Phys., vol. 28, No. 10, pp. 1735-1741, "A Model for the Silicon Wafer Bonding Process", Oct. 1989.	
	397	R. Stengl, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2311-L2314, "Bubble-Free Silicon Wafer Bonding in a NonCleanroom Environment", Dec. 1988.	
	398	R.W. Bower et al., Aligned Wafer Bonding: A Key to Three Dimensional Microstructures, 20 J. Electronic Materials 383, 383 (1991).	
	399	Reiche et al., "The Effect of a Plasma Pretreatment of the Si/Si Bonding Behavior", Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science and Technology and Applications, the Electrochemical Society, Pennington, NJ 1998, pp. 437-444.	
	400	Ritsuo Takizawa, et al., Jpn. J. Appl. Phys., vol. 27, No. 11, pp. L2210-L2212, "Ultraclean Technique for Silicon Wafer Surfaces with HNO3-HF Systems", Nov. 1998.	
	401	Robert W. Bower et al., Design Considerations of a Digital Pressure Sensor Array, 1991 International Conference on SolidState Sensors and Actuators, 1991. Digest of Technical Papers, Transducers, '91 312.	
	402	Robert W. Bower et al., Low Temperature S3N4 Direct Bonding, 62 Applied Physics Letters 3485 (1993).	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 19 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	403	Rochdi Messoussi, et al., Jpn. J. Appl. Phys., vol. 35, Part 1, No. 4A, pp. 1989-1992, "Improvement of Rinsing Efficiency After Sulfuric Acid Hydrogen Peroxide Mixture (H <sub>2</sub> SO <sub>4</sub> /H <sub>2</sub> O <sub>2</sub> ) by HF Addition", 1996.	
	404	Room Temperature Silicon Wafer Direct Bonding in Vacuum by Ar Beam Irradiation by Takagi H., Maeda R., Ando Y., Suga T., Micro Electron Mechanical Systems, 1997. MEMS '97, Proceedings, IEEE., Tenth Annual International Workshop on pp. 191-196, Jan. 23-30, 1997.	
	405	Ross, R.C., et al., Journal of Non-Crystalline Solids, vol. 66, pp. 81-86, "Physical Microstructure in Device-Quality Hydrogenated Amorphous Silicon", 1984.	
	406	S. Bengtsson, et al., International Conference on Compliant & Alternative Substrate Technology, p. 10, "Low Temperature Bonding," Sep. 1999.	
	407	S. Farrens, Electromechanical Society Proceedings, vol. 97-36, pp. 425-436, "Low Temperature Wafer Bonding," 1997.	
	408	S. Fujino, et al., Jpn. J. Appl. Phys., vol. 34, No. 10B, 1 page, "Silicon Wafer Direct Bonding Through the Amorphous Layer," Oct. 15, 1995.	
	409	S. Mack, et al., J. Electrochem. Soc., vol. 144, No. 3, pp. 1106-1111, "Analysis of Bonding-Related Gas Enclosure in Micromachined Cavities Sealed by Silicon Wafer Bonding", Mar. 1997.	
	410	S. N. Farrens et al., A Kinetics Study of the Bond Strength of Direct Bonded Wafers, 141 J. Electrochemical Society 3225 (1994).	
	411	S. Schulze, et al., Proceedings of the Second International Symposium on Microstructures and Microfabricated Systems, Proceedings vol. 95-27, pp. 309-318, "Investigation of Bonded Silicon-Silicon-Interfaces Using Scanning Acoustic Microscopy", (1995).	
	412	S. V. Hattangady et al., "In situ Cleaning of GaAs Surface Using Hydrogen Dissociated With a Remote Noble-Gas Discharge," J. Appl. Phys. 68(3), pp. 1233-1236, (Aug. 1990).	
	413	S.A. McQuaid, et al., J. Appl. Phys., vol. 81, No. 11, pp. 7612-7618, "Passivation, Structural Modification, and Etching of Amorphous Silicon in Hydrogen Plasmas", Jun. 1, 1997.	
	414	S.J. Pearton, et al., Appl. Phys. A, vol. 43, pp. 153-195, "Hydrogen in Crystalline Semiconductors", 1987.	
	415	Sailer et al., Creating 3D Circuits Using Transferred Films, Circuits and Devices, IEEE 1997, Nov. 1997, pp. 27-30.	
	416	Sakaguchi et al., Extremely High Selective Etching of Porous Si for Single Etch-Stop Bond-and-Etch-Back Silicon-on-Insulator, Jpn. J. Appl. Phys., vol. 34 (1995), pp. 842-847.	
	417	Satoshi Matsumoto et al., Thin-Film Quasi-SOI Power MOSFET Fabricated by Reversed Silicon Wafer Direct Bonding, 45 IEEE Transactions on Electron Devices 105 (1998).	
	418	Shi-Ji Lu et al., A New Silicon Micromachining Method Using SOI/SDB Technology, 23 Sensors and Actuators 961 (1990).	
	419	Shoji Yamahata, et al., IEEE Gallium Arsenide Integrated Circuit Symposium, Technical Digest 1995, pp. 163-166, "Over-220-GHz-fT-AND-fmax InP/InGaAs Double-Heterojunction Bipolar Transistors with a New Hexagonal Shaped Emitter", Oct. 29-Nov. 1, 1995.	
	420	Stefan Bengtsson et al., The Influence of Wafer Dimensions on the Contact Wave Velocity in Silicon Wafer Bonding, 69 Applied Physics Letters 3381 (1996).	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 20 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	421	Sun et al., "Cool Plasma Activated Surface in Silicon Wafer Direct Bonding Technology," Journal De Physique, pp. C4-79-C4-82, Sep. 1988.	
	422	Suzuki et al., "SiN Membrane Masks for X-Ray Lithography", Journal of Vacuum Science and Technology, vol. 20, No. 2, Feb. 1982, pp. 191-194.	
	423	T. Akatsu, et al., Journal of Applied Physics, vol. 86, No. 12, pp. 7146-7150, "GaAs Wafer Bonding by Atomic Hydrogen Surface Cleaning", Dec. 15, 1999.	
	424	T.M. Duncan, et al., J. Appl. Phys., vol. 60, No. 1, pp. 130-136, "Study of Fluorine in Silicate Glass With 19 F Nuclear Magnetic Resonance Spectroscopy", Jul. 1, 1986.	
	425	Tadahiro Ohmi, et al., Proceedings Fifth International IEEE VLSI Multilevel Interconnection Conference, pp. 261-267, "VLSI Interconnects for Ultra High Speed Signal Propagation", Jun. 13-14, 1988.	
	426	Takagi et al., "Wafer-scale room-temperature bonding between silicon and ceramic wafers by means of argon-beam surface activation", 2001, IEEE, pp.60-63.	
	427	Takao Abe, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2311-L2314, "Silicon Wafer Bonding Mechanism for Silicon-on-Insulator Structures", Dec. 1990.	
	428	Takashi Kurahashi et al., Sensors Utilizing Si Wafer Direct Bonding at Low Temperature, 1991 Proceedings of the 2nd International Symposium on Micro Machine and Human Science 173, 173.	
	429	Takeshi Sunada, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2408-L2410, "The Role of Fluorine Termination in the Chemical Stability of HF-Treated Si Surfaces", Dec. 1990.	
	430	Tong et al., Fabrication of Ultrathin SOI by SIMOX Wafer Bonding (SWB), Journal of Electronic Materials, vol. 22, No. 7, 1993, 763-768.	
	431	Tong et al., Materials with a Buried C60 Layer Produced by Direct Wafer Bonding, J. Electrochem. Soc., vol. 141, No. 10, Oct. 1994, 137-38.	
	432	Tong et al., Ultrathin single-crystalline silicon on quartz (SOQ) by 150 C wafer bonding, Sensors and Actuators A 48 (1995) 117-123.	
	433	Tong, Qin-Yi, "Low Temperature Wafer Direct Bonding", IEEE 1994, Journal of Microelectromechanical Systems, vol. 3, No. 1, Mar. 1994, pp. 29-35.	
	434	Trimble et al., "Evaluation of Polycrystalline Silicon Membranes on Fused Silica for X-Ray Lithography Masks", Journal of Vacuum Science and Technology B (Microelectronics Processing Phenomena), vol. 7, No. 6, Nov./Dec. 1989, pp. 1675-1679.	
	435	TSMC Answer to Second Amended Complaint, filed Aug. 27, 2012, pp. 1-80.	
	436	U. Bhattacharya, et al., IEEE Electron Device Letters, vol. 16, No. 8, pp. 357-359, "Transferred Substrate Schottky-Collector Heterojunction Bipolar Transistors: First Results and Scaling Laws for High f <sub>max</sub> ", Aug. 1995.	
	437	U. Gösele et al., "Wafer Bonding for Microsystems Technologies", Sensors and Actuators 74 (1999) 161-168, 1999 Elsevier Science S.A.	
	438	U. Gösele et al., "Fundamental Issues in Wafer Bonding", J. Vac. Sci. Technol. A 17(4), Jul./Aug., 1145-1152, (1999), American Vacuum Society.	
	439	U. Gösele et al., "Semiconductor Wafer Bonding", Annu. Rev. Mater. Sci. 1998, 28:215-41.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 21 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	440	U. Gösele et al., History and Future of Semiconductor Wafer Bonding, 47-48 Solid State Phenomena 33 (1996).	
	441	U. Gösele, et al., Appl. Phys. Lett., vol. 67, No. 24, pp. 3614-3616, "Self-Propagating Room-Temperature Silicon Wafer Bonding in Ultrahigh Vacuum," Dec. 11, 1995.	
	442	V.H.C. Watt et al., Low Temperature Direct Bonding on Nonhydrophilic Surfaces, 30 Electronic Letters 693, 694 (1994).	
	443	Vanderwater et al, "High-Brightness AlGaInP Light Emitting Diodes," Proc. IEEE, vol. 85, No. 11, pp. 1752-1764, Nov. 1997.	
	444	W.E. Stanchina, et al., IEEE Gallium Arsenide Integrated Circuit Symposium, Technical Digest 1995, pp. 31-34, "An InP-Based HBT FAB for High-Speed Digital, Analog, Mixed-Signal, and Optoelectronic Ics", Oct. 29-Nov. 1, 1995.	
	445	W.K. Chu, et al., Physical Review B, vol. 16, No. 9, pp. 3851-3859, "Distribution of Irradiation Damage in Silicon Bombarded with Hydrogen", Nov. 1, 1977.	
	446	W.P. Maszara, et al., J. Appl. Phys., vol. 64, No. 10, pp. 4943-4950, "Bonding of Silicon Wafers for Silicon-on-Insulator", Nov. 15, 1988.	
	447	W.P. Maszara, J. Electrochem. Soc., vol. 138, No. 1, pp. 341-347, "Silicon-on-Insulator by Wafer Bonding: a Review", Jan. 1991.	
	448	Wen Hsiung Ko, et al., IEEE Transactions on Electron Devices, vol. ED-26, No. 12, pp. 1896-1905, "Development of a Miniature Pressure Transducer for Biomedical Applications", Dec. 1979.	
	449	William Liu, et al., IEEE Transactions on Electron Devices, vol. 40, No. 11, pp. 1917-1927, "Current Gain Collapse in Microwave Multifinger Heterojunction Bipolar Transistors Operated at Very High Power Densities", Nov. 1993.	
	450	Williams, et al., Journal of Applied Physics, vol. 46, No. 2, pp. 695-698, "Mobile Fluoride Ions in SiO <sub>2</sub> ", Feb. 1975.	
	451	Xu et al., Novel Two-Step SDB Technology for High-Performance Thin-Film SOI/MOSFET Applications, Electronics Letters, 3-16/1989, vol. 25, No. 6 pp. 394-395.	
	452	Xu et al., Silicon on Quartz by Solid-State Diffusion Bonding (SSDB) Technology, Electronics Letters, May 26, 1988, vol. 24, No. 11 pp. 691-692.	
	453	Y. Albert Li, et al., Jpn. J. Appl. Phys., vol. 39, Part 1, No. 1, pp. 275-276, "Surface Roughness of Hydrogen Ion Cut Low Temperature Bonded Thin Film Layers", Jan. 2000.	
	454	Y. Zhou et al., "Electrical Properties of Wafer-Bonded GaAs/Si Heterojunctions", Appl. Phys. Lett., vol. 73, No. 16, 1998 American Institute of Physics, pp. 2337-2339.	
	455	Y.H. Lo et al., "Wafer Bonding Technology and its Optoelectronic Applications," SPIE proc., vol. 3006, pp. 26-35, 1997.	
	456	Yasushiro Nishioka, et al., Appl. Phys. Lett., vol. 54, No. 12, pp. 1127-1129, "Dielectric Characteristics of Fluorinated Ultradry SiO <sub>2</sub> ", Mar. 20, 1999.	
	457	Yozo Kanda, et al., Sensors and Actuators, vol. A21-A23, pp. 939-943, "The Mechanism of Field-Assisted Silicon-Glass Bonding", 1990.	
	458	Zhu et al., "Wafer Bonding Technology and its Applications in Optoelectronic Devices and Materials," IEEE Journal of Selected Topics in Quantum Electronics, vol. 3, No. 3, Jun. 1997 pp. 927-936.	

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 22 OF 22	Attorney Docket No.	TSSRA.012C1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	459	Zucker et al., "Application of Oxygen Plasma Processing to Silicon Direct Bonding", Sensors and Actuators A, 36 (1993), pp. 227-231.	
	460	Stefan Bengtsson et al., Journal of Electronic Materials, vol. 29, No. 7, "Room Temperature Wafer Bonding Of Silicon Oxidized Silicon, and Crystalline Quartz," 2000, pp. 909-915.	
	461	PLOSSL et al., "Wafer direct bonding: Tailoring adhesion between brittle materials," Materials Science & Engineering, March 10, 1999, Vol. R 25, Nos. 1-1, pp. 1-88.	
	462	TAKAGI et al, "Low temperature direct bonding of silicon and silicon dioxide by the surface activation method," Transducers 1997, 1997 Int. Conf. on Solid State Sensors and Actuators, Jun. 16-19, 1997, pp. 657-660.	Abstract
	463	TAKAGI et al., "Wafer-scale room-temperature bonding between silicon and ceramic wafers by means of argon-beam surface activation," 2001, IEEE, p. 60-63.	
	464	Ziptronix, Inc. v. Omnivision Technologies, Complaint for Patent Infringement, Case 4:10-cv-05525-SBA, Document 48, filed May 4, 2011, pp. 1-29.	
	465	Ziptronix, Inc. v. Omnivision Technologies, Defendant TSMC's Answer and Affirmative Defenses to Ziptronix First Amended Complaint, Case No. 4:10-cv-05525-SBA, Document 49, filed May 4, 2011, pp. 1-45.	
	466	Ziptronix, Inc. v. Omnivision Technologies, Complaint for Patent Infringement, Case No. 4:10-cv-05525-SBA Document 1, filed December 16, 2010, pp. 1-17.	

22453282  
021616

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	24920204
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	16-FEB-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	13:28:02
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Plossl-et-al_Wafer-direct-bonding_tailoring-adhesion-between-brittle-materials.pdf	3587507 62f5e1cff280c536f54c5e49fcfcfe46fea871b4	no	88

### Warnings:

Information:

2	Non Patent Literature	Takagi-et-al_Low-temperature-direct-bonding-of-silicon-and-silicon-dioxide.pdf	194919 6336bbe6dcaea9995cdfc58c46bf655585a9dc7b	no	2
Warnings:					
Information:					
3	Non Patent Literature	Takagi-et-al_Wafer-scale-room-temperature-bonding-between-silicon_FullArticle.pdf	493605 0c1da782b5e480ad28be62e3e33082af0d0d4461	no	4
Warnings:					
Information:					
4	Non Patent Literature	Ziptronix-v-Omnivision_Document-1.pdf	21305852 a31b3a3ec03d306053bc43a84dd91dd475a20e63	no	17
Warnings:					
Information:					
5	Non Patent Literature	Ziptronix-v-Omnivision_Document-48.pdf	2210046 79675ffd0aaf278506f4f622e53f0a7a0b385afc	no	29
Warnings:					
Information:					
6	Non Patent Literature	Ziptronix-v-Omnivision_Document-49.pdf	3399874 90cd8676c958b50126aa444f7dc40de1c681034d	no	45
Warnings:					
Information:					
7		2016-02-16_IDS_TSSRA-012C1.pdf	277521 8c1feb81f5ce87ab41a545c650108d54ef7b5bae	yes	24
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	24	
Warnings:					
Information:					
Total Files Size (in bytes):			31469324		

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

**INFORMATION DISCLOSURE STATEMENT**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Joannie A. Garcia
Art Unit	:	2895
Conf. No.	:	1033

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**References and Listing**

Pursuant to 37 CFR 1.56, an Information Disclosure Statement listing references is provided herewith. Listed references are of record in one or more of U.S. patent application No. 14/754,111, filed June 29, 2015, U.S. patent application No. 14/197,070, filed March 4, 2014, U.S. patent application No. 13/341,273, filed December 30, 2011, U.S. patent application No. 12/954,740, filed November 26, 2010, U.S. patent application No. 12/720,368, filed March 9, 2010, U.S. patent application No. 11/980,664, filed October 31, 2007, U.S. patent application No. 10/913,441, filed August 9, 2004, and U.S. patent application No. 09/505,283, filed February 16, 2000, which are parent applications of this continuation application, and are relied upon for an earlier filing date under 35 USC 120. Copies of the references are not submitted pursuant to 37 CFR 1.98(d).

**No Disclaimers**

To the extent that anything in the Information Disclosure Statement or the listed references could be construed as a disclaimer of any subject matter supported by the present application, Applicant hereby rescinds and retracts such disclaimer.

**Application No.:** 14/957,501  
**Filing Date:** December 2, 2015

**Timing of Disclosure**

This Information Disclosure Statement is being filed within three months of the filing date, and no fee is believed to be required.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

Respectfully submitted,  
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: February 16, 2016

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22625377  
021616

Please Direct All Correspondence to Customer Number 135,980

---

**RESPONSE TO INFORMATIONAL NOTICE**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Art Unit	:	2895
Conf No.	:	1033

**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313-1450**

Dear Sir:

The above-captioned application was filed without a Declaration and/or Substitute Statement. Enclosed in compliance with 37 CFR 1.53(f) are the following.

(X) Substitute Statement in Lieu of Declaration document(s) for:  
Qin-Yi Tong

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.

/Paul Stellman/

Paul Stellman

Registration No. 68,287

Attorney of Record

Customer No. 135,980

(415) 954-4114

22790207  
022916



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY  
OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)**

Title of Invention	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
This statement is directed to:			
<input type="checkbox"/> The attached application,			
OR			
<input checked="" type="checkbox"/> United States application or PCT international application number <u>14/957,501</u> filed on <u>December 2, 2015</u>			
LEGAL NAME of inventor to whom this substitute statement applies:			
(E.g., Given Name (first and middle (if any)) and Family Name or Surname)			
Qin-Yi Tong			
Residence (except for a deceased or legally incapacitated inventor):			
City	State	Country	
Mailing Address (except for a deceased or legally incapacitated inventor):			
City	State	Zip	Country
I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.			
The above-identified application was made or authorized to be made by me.			
I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.			
Relationship to the inventor to whom this substitute statement applies:			
<input type="checkbox"/> Legal Representative (for deceased or legally incapacitated inventor only).			
<input checked="" type="checkbox"/> Assignee.			
<input type="checkbox"/> Person to whom the inventor is under an obligation to assign.			
<input type="checkbox"/> Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or			
<input type="checkbox"/> Joint Inventor.			

[Page 1 of 2]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☒ Inventor is deceased,  
☐ Inventor is under legal incapacity,  
☐ Inventor cannot be found or reached after diligent effort, or  
☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).


### WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

### PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: **Paul Davis**

1/6/2016  
Date (Optional)

Signature: 

### APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

**ZIPTRONIX, INC.**

Applicant Name:

Title of Person Executing This Substitute Statement: **Senior Vice President, General Counsel and Secretary**

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

Residence of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

City

State

Country

Mailing Address of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent)

City

State

Zip

Country

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

[Page 2 of 2]

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	25052671
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Kealani Aguon
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	29-FEB-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	17:15:33
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
------------------------	----

### File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-02-29_SubstituteStatement_TSSRA-012C1.pdf	382004 c8bb872f939d2acff9ac9d82921782b8c17e9350	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Applicant Response to Pre-Exam Formalities Notice	1	1
	Oath or Declaration filed	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		382004	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 1 OF 1	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	1	AMIRFEIZ et al., "Formation of silicon structures by plasma activated wafer bonding," Vol. 99-2, Abstract No. 963, 1999 Joint Int'l Meeting of the Electrochem. Soc'y, December 16, 1999.	
	2	AMIRFEIZ et al., "Formation of silicon structures by plasma activated wafer bonding," Electrochemical Society Proceedings: Semiconductor Wafer Bonding: Science, Technology, and Applications V, Volume 99-35, (1999), pp. 29-39.	
	3	Ziptronix, Inc. v. Omnivision Technologies, Inc., Defendants' Third Supplemental Consolidated Invalidity Contentions Under Patent Local Rule 3-3, Case No. 4:10-cv-05525-SBA, dated June 14, 2013, pp. 1-5379, (submitted in multiple parts).	

22889096  
031116

Examiner Signature	Date Considered
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Electronic Patent Application Fee Transmittal				
Application Number:		14957501		
Filing Date:		02-Dec-2015		
Title of Invention:		METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE		
First Named Inventor/Applicant Name:		Qin-Yi Tong		
Filer:		Paul Steven Stellman/Jonathan Pan		
Attorney Docket Number:		TSSRA.012C1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Miscellaneous:</b>				
Submission- Information Disclosure Stmt	1806	1	180	180
<b>Total in USD (\$)</b>				<b>180</b>

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	25178415
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	11-MAR-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	19:02:11
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 180
RAM confirmation Number	5259
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)



<b>File Listing:</b>					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-03-11_IDS_TSSRA-012C1.pdf	144402 9f0024d0219d102a969cf3fd628ac1f7d237c31d	yes	3
	<b>Multipart Description/PDF files in .zip description</b>				
	<b>Document Description</b>		<b>Start</b>	<b>End</b>	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	3	
<b>Warnings:</b>					
<b>Information:</b>					
2	Fee Worksheet (SB06)	fee-info.pdf	30909 ec693c5756dcfa3947854bfee15334358949561d	no	2
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			175311		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

**INFORMATION DISCLOSURE STATEMENT**

First Inventor :	Tong et al.
App. No. :	14/957,501
Filed :	December 2, 2015
For :	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner :	Joannie A. Garcia
Art Unit :	2895
Conf. No. :	1033

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**References and Listing**

Pursuant to 37 CFR 1.56, an Information Disclosure Statement listing references is provided herewith. Listed references are of record in U.S. patent application No. 14/754,111, filed June 29, 2015, which is the parent of this continuation application, and is relied upon for an earlier filing date under 35 USC 120. Copies of the references are not submitted pursuant to 37 CFR 1.98(d).

**No Disclaimers**

To the extent that anything in the Information Disclosure Statement or the listed references could be construed as a disclaimer of any subject matter supported by the present application, Applicant hereby rescinds and retracts such disclaimer.

**Timing of Disclosure**

This Information Disclosure Statement is being filed after receipt of a First Office Action, but before the mailing date of a Final Action and before the mailing date of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 CFR 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

**Application No.:** 14/957,501  
**Filing Date:** December 2, 2015

Respectfully submitted,  
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 11, 2016

By: /Paul Stellman/

Paul Stellman  
Registration No. 68,287  
Attorney of Record  
Customer No. 135,980  
(415) 954-4114

22889121  
031116



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1

**CONFIRMATION NO. 1033**

## PUBLICATION NOTICE



\*OC000000081677620\*

135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

**Title:**METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

**Publication No.**US-2016-0086913-A1

**Publication Date:**03/24/2016

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at [www.uspto.gov](http://www.uspto.gov). The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at [www.uspto.gov](http://www.uspto.gov) using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

## NOTICE OF ALLOWANCE AND FEE(S) DUE

135980 7590 05/24/2016  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

EXAMINER

GARCIA, JOANNIE A

ART UNIT

PAPER NUMBER

2895

DATE MAILED: 05/24/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

14/957,501

12/02/2015

Qin-Yi Tong

TSSRA.012C1

1033

TITLE OF INVENTION: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/24/2016

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

### HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, Virginia 22313-1450**  
**or Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

135980 7590 05/24/2016  
**Knobbe, Martens, Olson**  
**& Bear, LLP**  
**2040 main Street**  
**Fourteenth Floor**  
**Irvine, CA 92614**

## Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1	1033

TITLE OF INVENTION: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/24/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
GARCIA, JOANNIE A	2895	257-684000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature \_\_\_\_\_

Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_

Registration No. \_\_\_\_\_



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1	1033

135980 7590 05/24/2016  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

EXAMINER

GARCIA, JOANNIE A

ART UNIT PAPER NUMBER

2895

DATE MAILED: 05/24/2016

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

### Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



<b>Notice of Allowability</b>	<b>Application No.</b> 14/957,501	<b>Applicant(s)</b> TONG ET AL.	
	<b>Examiner</b> JOANNIE A. GARCIA	<b>Art Unit</b> 2895	<b>AIA (First Inventor to File) Status</b> No

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to claims, remarks, and TD filed 02/08/2016.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_\_.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_\_; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 2-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

- a) ☐ All    b) ☐ Some    \*c) ☐ None of the:
  1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.  
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08),  
 Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit  
 of Biological Material
4. ☐ Interview Summary (PTO-413),  
 Paper No./Mail Date \_\_\_\_\_.
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other \_\_\_\_\_.

/JOHN P DULKA/  
 Primary Examiner, Art Unit 2895

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 02/16/2016, and 03/11/2016.

### **DETAILED ACTION**

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

#### ***Status of Application***

In response to the Office action mailed 02/03/2016 ("02-03-16 OA"), Applicant's reply and Terminal Disclaimer filed on 02/08/2016 ("02-08-16 Reply").

Pending claims 2-34 of which claims 2, 22, 32, and 33, are independent.

#### ***Information Disclosure Statements (IDS)***

The IDS filed 02/16/2016, and 03/11/2016, have been considered, and a signed and dated copy of each, is included herein.

It is noted that the prosecution history for the following related application has been reviewed and considered: 14/754,111, 14/197,070, 14/197,056, 13/341,273, 12/954,740, 12/720,368, 11/980,664, 10/913,441, 11/980,664, 11/980,415, 12/493,957, 10/762,318, 10/460,418, and 09/505,283.

#### ***Response to Arguments***

- Applicant's reply and Terminal Disclaimer have overcome the nonstatutory obviousness-type double patenting rejection(s) as set forth in pages 2-20 of the 02-03-16 OA.
- Applicants' Remarks (pages 6-8) in the 02-08-16 Reply with respect the nonstatutory obviousness-type double patenting rejection(s), have been fully considered and are persuasive.

***Reasons for Allowance***

**Claims 2-34 are allowed.**

The following is an examiner's statement of reasons for allowance:

**Independent claim 2 is allowed**, because the prior art of record, singularly or in combination, does not disclose or suggest, in combination with the other claimed elements in claim 2, *terminating the planarized insulating material with a nitrogen-containing species by at least one of:*

*a nitrogen-containing plasma during the etching, and*

*a nitrogen-containing solution after the etching;*

*bringing a first material into direct contact with the terminated and planarized insulating material outside the reaction space; and*

*forming a chemical bond between the terminated and planarized insulating material and the first material.*

**Claims 3-21 are allowed**, because they depend on allowed claim 2.

**Independent claim 22 is allowed**, because the prior art of record, singularly or in combination, does not disclose or suggest, in combination with the other claimed elements in claim 22, *wherein the first bonding surface is an etched surface terminated with a nitrogen-containing species, and*

*wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive.*

**Claims 23-31 are allowed**, because they depend on allowed claim 22.

**Independent claim 32 is allowed**, because the prior art of record, singularly or in combination, does not disclose or suggest, in combination with the other claimed elements in claim 32, *terminating the planarized insulating material with a nitrogen-containing species by at least one of:*

*a nitrogen-containing plasma during the etching, and*

*a nitrogen-containing solution after the etching;*

*bringing a first material into direct contact with the terminated and planarized insulating material; and*

*forming a chemical bond between the terminated and planarized insulating material and the first material.*

**Independent claim 33 is allowed**, because the prior art of record, singularly or in combination, does not disclose or suggest, in combination with the other claimed elements in claim 33, *terminating the planarized insulating material with a species,*

*bringing into direct contact with the terminated and planarized insulating material and a first material outside of said plasma chamber; and*

*forming a chemical bond between the terminated and planarized insulating material and the first material.*

**Claim 34 is allowed**, because it depends on allowed claim 33.

Therefore, the prior-art of record neither anticipates nor renders obvious the claimed subject matter.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joannie García, whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad K. Islam, can be reached on (571) 270-5878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 14/957,501  
Art Unit: 2895

Page 6

/JOANNIE A GARCIA/  
Examiner, Art Unit 2895

/JOHN P DULKA/  
Primary Examiner, Art Unit 2895



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

## BIB DATA SHEET

CONFIRMATION NO. 1033

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/957,501	12/02/2015	257	2895	TSSRA.012C1
<b>RULE</b>				
<b>APPLICANTS</b> ZIPTRONIX, INC., Morrisville, NC;				
<b>INVENTORS</b> Qin-Yi Tong, Durham, NC; Gaius Gillman Fountain JR., Youngsville, NC; Paul M. Enquist, Cary, NC;				
<b>** CONTINUING DATA *****</b> This application is a CON of 14/754,111 06/29/2015 PAT 9331149 which is a DIV of 14/197,070 03/04/2014 PAT 9082627 which is a DIV of 13/341,273 12/30/2011 ABN which is a CON of 12/954,740 11/26/2010 PAT 8153505 which is a CON of 12/720,368 03/09/2010 PAT 7871898 which is a CON of 11/980,664 10/31/2007 PAT 7807549 which is a CON of 10/913,441 08/09/2004 PAT 7387944 which is a CON of 09/505,283 02/16/2000 PAT 6902987				
<b>** FOREIGN APPLICATIONS *****</b>				
<b>** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **</b> 12/11/2015				
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged <u>/JOANNIE A GARCIA/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	<b>STATE OR COUNTRY</b> NC	<b>SHEETS DRAWINGS</b> 9	<b>TOTAL CLAIMS</b> 33
<b>INDEPENDENT CLAIMS</b> 4				
<b>ADDRESS</b> Knobbe, Martens, Olson & Bear, LLP 2040 main Street Fourteenth Floor Irvine, CA 92614 UNITED STATES				
<b>TITLE</b> METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE				
<b>FILING FEE RECEIVED</b> 3200	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit	



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 1 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	3,423,823	01-28-1969	Ansley	
	2	3,488,834	01-13-1970	Baird	
	3	3,508,980	04-28-1970	Jackson, Jr. et al.	
	4	3,534,467	10-20-1970	Sachs et al.	
	5	3,579,391	05-18-1971	Buie	
	6	3,587,166	06-28-1971	Alexander et al.	
	7	3,602,981	09-07-1971	Kool	
	8	3,607,466	09-21-1971	Miyazaki	
	9	3,640,807	02-08-1972	Van Dijk	
	10	3,647,581	03-07-1972	Mash	
	11	3,888,708	06-10-1975	Wise et al.	
	12	4,416,054	11-22-1983	Thomas et al.	
	13	4,612,083	09-16-1986	Yasumoto et al.	
	14	4,617,160	10-14-1986	Belanger et al.	
	15	4,649,630	03-13-1987	Boland et al.	
	16	4,700,466	10-20-1987	Nakagawa et al.	
	17	4,754,544	07-05-1988	Hanak	
	18	4,829,018	05-09-1989	Wahlstrom	
	19	4,935,386	06-19-1990	Nakagawa	
	20	4,939,101	07-03-1990	Black et al.	
	21	4,962,879	10-16-1990	Gösele et al.	
	22	4,963,505	10-16-1990	Fujii et al.	
	23	4,970,175	11-13-1990	Haisma et al.	
	24	4,978,421	12-18-1990	Bassous et al.	
	25	4,983,251	01-08-1991	Haisma et al.	
	26	4,992,149	02-12-1991	Nguyen	
	27	5,007,071	04-09-1991	Nakano	
	28	5,013,471	05-07-1991	Ogawa	
	29	5,024,723	06-18-1991	Gösele et al.	

Examiner Signature /Joannie Garcia/	Date Considered 05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 2 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	30	5,034,343	07-23-1991	Rouse et al.	
	31	5,070,026	12-03-1991	Greenwald et al.	
	32	5,071,792	12-10-1991	Van Vonno et al.	
	33	5,081,061	01-14-1992	Rouse et al.	
	34	5,087,585	02-11-1992	Hayashi	
	35	5,089,431	02-18-1992	Slatter et al.	
	36	5,121,706	06-16-1992	Nichols et al.	
	37	5,162,251	11-10-1992	Poole et al.	
	38	5,183,783	02-02-1993	Ohta et al.	
	39	5,196,375	03-23-1993	Hoshi	
	40	5,207,864	05-04-1993	Bhat et al.	
	41	5,234,860	08-10-1993	Gluck	
	42	5,236,118	08-17-1993	Bower et al.	
	43	5,238,875	08-24-1993	Ogino	
	44	5,266,511	11-30-1993	Takao	
	45	5,266,824	11-30-1993	Abe	
	46	5,270,259	12-14-1993	Ito et al.	
	47	5,270,261	12-14-1993	Bertin et al.	
	48	5,272,104	12-21-1993	Schranz et al.	
	49	5,284,707	02-08-1994	Ogawa et al.	
	50	5,321,301	06-14-1994	Sato et al.	
	51	5,324,566	06-28-1994	Ogawa et al.	
	52	5,324,687	06-28-1994	Wojnarowski	
	53	5,354,695	10-11-1994	Leedy	
	54	5,362,659	11-08-1994	Cartagena	
	55	5,376,579	12-27-1994	Annamalai	
	56	5,380,681	01-10-1995	Hsu	
	57	5,383,993	01-24-1995	Katada et al.	
	58	5,407,856	04-18-1995	Quenzer et al.	

Examiner Signature /Joannie Garcia/	Date Considered 05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 3 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	5,413,955	05-09-1995	Lee et al.	
	60	5,420,449	05-30-1995	Oji	
	61	5,421,953	06-06-1995	Nagakubo et al.	
	62	5,422,302	06-06-1995	Yonehara	
	63	5,427,638	06-27-1995	Goetz et al.	
	64	5,432,729	07-11-1995	Carson et al.	
	65	5,437,894	08-01-1995	Ogawa et al.	
	66	5,441,591	08-15-1995	Imthum et al.	
	67	5,441,911	08-15-1995	Malhi	
	68	5,459,104	10-17-1995	Sakai	
	69	5,460,659	10-24-1995	Krut	
	70	5,485,540	01-16-1996	Eda	
	71	5,489,554	02-06-1996	Gates	
	72	5,497,033	03-05-1996	Fillion et al.	
	73	5,503,704	04-02-1996	Bower et al.	
	74	5,514,235	05-07-1996	Mitani et al.	
	75	5,516,727	05-14-1996	Broom	
	76	5,517,754	05-21-1996	Bellstein, Jr., et. al.	
	77	5,523,602	06-04-1996	Horiuchi	
	78	5,534,465	07-09-1996	Frye et al.	
	79	5,543,648	08-06-1996	Miyawaki	
	80	5,546,494	08-13-1996	Eda	
	81	5,547,896	08-20-1996	Linn et al.	
	82	5,548,178	08-20-1996	Eda et al.	
	83	5,561,303	10-01-1996	Schranz et al.	
	84	5,563,084	10-08-1996	Ramm et al.	
	85	5,567,657	10-22-1996	Wonjnarowski et al.	
	86	5,569,620	10-29-1996	Linn et al.	
	87	5,580,407	12-03-1996	Haisma et al.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 4 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	88	5,591,678	01-07-1997	Bendik et al.	
	89	5,627,106	05-06-1997	Hsu	
	90	5,647,932	07-15-1997	Taguchi et al.	
	91	5,650,353	07-22-1997	Yoshizawa et al.	
	92	5,652,436	07-29-1997	Stoner et al.	
	93	5,653,019	08-05-1997	Bernhardt et al.	
	94	5,659,192	08-19-1997	Sarma et al.	
	95	5,661,316	08-26-1997	Kish, Jr., et al.	
	96	5,661,901	09-02-1997	King	
	97	5,666,706	09-16-1997	Tomita et al.	
	98	5,668,057	09-16-1997	Eda et al.	
	99	5,672,240	09-30-1997	Stoner et al.	
	100	5,673,478	10-07-1997	Beene et al.	
	101	5,698,471	12-16-1997	Namba et al.	
	102	5,741,733	04-21-1998	Bertagnolli et al.	
	103	5,747,857	05-05-1998	Eda et al.	
	104	5,753,529	05-19-1998	Chang et al.	
	105	5,755,914	05-26-1998	Yonehara	
	106	5,759,753	06-02-1998	Namba et al.	
	107	5,760,478	06-02-1998	Bazso et al.	
	108	5,763,318	06-09-1998	Bertin et al.	
	109	5,766,984	06-16-1998	Ramm et al.	
	110	5,771,555	06-30-1998	Eda et al.	
	111	5,783,477	07-21-1998	Kish, Jr. et al.	
	112	5,785,874	07-28-1998	Eda et al.	
	113	5,793,115	08-11-1998	Zavracky et al.	
	114	5,804,086	09-08-1998	Bruel	
	115	5,807,783	09-15-1998	Gaul et al.	
	116	5,821,665	10-13-1998	Onishi et al.	

Examiner Signature <u>/Joannie Garcia/</u>	Date Considered <u>05/11/2016</u>
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 5 OF 22	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	117	5,841,197	11-24-1998	Adamic, Jr.	
	118	5,849,627	12-15-1998	Linn et al.	
	119	5,851,894	12-22-1998	Ramm	
	120	5,858,876	01-12-1999	Chew	
	121	5,866,942	02-02-1999	Suzuki et al.	
	122	5,869,354	02-09-1999	Leedy et al.	
	123	5,872,025	02-16-1999	Cronin et al.	
	124	5,876,497	03-02-1999	Atoji	
	125	5,877,034	03-02-1999	Ramm et al.	
	126	5,877,070	03-02-1999	Gösele et al.	
	127	5,877,516	03-02-1999	Mermagen et al.	
	128	5,880,010	03-09-1999	Davidson	
	129	5,889,302	03-30-1999	Liu	
	130	5,902,118	05-11-1999	Hubner	
	131	5,903,018	05-11-1999	Shimawaki	
	132	5,904,860	05-18-1999	Nagakubo et al.	
	133	<del>5,910,699</del>	06-08-1999	Namba et al.	
	134	5,915,167	06-22-1999	Leedy	
	135	5,915,193	06-22-1999	Tong et al.	
	136	5,920,142	07-06-1999	Onishi et al.	
	137	5,936,280	08-10-1999	Liu	
	138	5,966,622	10-12-1999	Levine et al.	
	139	5,980,770	11-09-1999	Ramachandran et al.	
	140	5,982,010	11-09-1999	Namba et al.	
	141	5,990,472	11-23-1999	Rinne	
	142	5,990,562	11-23-1999	Vallett	
	143	5,991,989	11-30-1999	Onishi et al.	
	144	6,004,865	12-21-1999	Horiuchi	
	145	6,004,866	12-21-1999	Nakano et al.	

Change  
applied to  
document  
/J.G./  
05/11/2016

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH SAMSUNG EXHIBIT 1002

Samsung v. Invenssas Bonding

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 6 OF 22	Attorney Docket No.	TSSRA.012C1

## U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
Changes applied to document /J.G./ 05/11/2016	146	6,018,211	01-25-2000	Kanaboshi et al.	
	147	6,048,752	04-11-2000	Lindemann	
	148	6,054,371 04/2000	<del>06-25-1999</del>	Tsuchiaki et al.	
	149	6,071,761	06-06-2000	Jacobs	
	150	6,087,719 07/2000	<del>04-23-1998</del>	Tsunashima	
	151	6,087,760	07-11-2000	Yamaguchi et al.	
	152	6,103,009	08-15-2000	Atoji	
	153	6,120,917	09-19-2000	Eda	
	154	6,133,640	10-17-2000	Leedy	
	155	6,136,691 10/2000	<del>05-26-1999</del>	Chen	
	156	6,143,628	11-07-2000	Sato et al.	
	157	6,146,992	11-14-2000	Lauterbach et al.	
	158	6,153,445	11-28-2000	Yamazaki et al.	
	159	6,153,495	11-28-2000	Kub et al.	
	160	6,154,940	12-05-2000	Onishi et al.	
	161	6,156,624	12-05-2000	Yamagata et al.	
	162	6,165,817	12-26-2000	Akram et al.	
	163	6,180,496	01-30-2001	Farrens et al.	
	164	6,190,778	02-20-2001	Batz-Sohn et al.	
	165	6,194,323	02-27-2001	Downey et al.	
	166	6,197,663	03-06-2001	Chandross et al.	
	167	6,198,159	03-06-2001	Hosoma et al.	
	168	6,236,141	05-22-2001	Sato et al.	
	169	6,242,324	06-05-2001	Kub	
	170	6,246,068	06-12-2001	Sato et al.	
	171	6,255,731	07-03-2001	Ohmi et al.	
	172	6,255,899	07-03-2001	Bertin et al.	
	173	6,270,202	08-07-2001	Namba et al.	
	174	6,274,892	08-14-2001	Kub et al.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 7 OF 22	Attorney Docket No.	TSSRA.012C1

Changes  
applied to  
document  
U.G./  
05/11/2016

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	175	6,284,085	09-04-2001	Gwo	
	176	6,313,012	11-06-2001	Horiuchi	
	177	6,316,332	11-13-2001	Lo et al.	
	178	6,323,108	11-27-2001	Kub et al.	
	179	6,328,796	12-11-2001	Kub	
	180	6,328,841 12/2001	<del>09-24-1997</del>	Klumpp et al.	
	181	6,448,174	09-10-2002	Ramm	
	182	6,500,694	12-31-2002	Enquist	
	183	6,562,647	05-13-2003	Zandman et al.	
	184	6,563,224	05-13-2003	Leedy	
	185	6,613,678 9/2003	<del>05-17-1999</del>	Sakaguchi et al.	
	186	6,627,531	09-30-2003	Enquist	
	187	7,553,744	06-30-2009	Tong	
	188	2002/0094661	07-18-2002	Enquist et al.	
	189	2002/0164839	11-07-2002	Enquist	
	190	2002/0173120	11-21-2002	Enquist	
	191	2003/0057423	03-27-2003	Shimoda	
	192	2003/0119279	06-26-2003	Enquist	
	193	2003/0211705	11-13-2003	Tong et al.	
	194	2004/0152282	08-05-2004	Tong et al.	
	195	2006/0292744	12-28-2006	Enquist et al.	
	196	2009/0263953	10-22-2009	Qin-Yi Tong	
	197	8,153,505	04-10-2012	Tong et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	198	EP 0905767 A1	03-31-1999	SHINETSU HANDOTAI KK		
	199	EP 0933810 A1	08-04-1999	CANON KK		

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL FIGURES AND FIGURE CAPTIONS ARE CONSIDERED EXCEPT WHERE INDICATED OTHERWISE THROUGH SAMSUNG EXHIBIT 1002

Samsung v. Invenssas Bonding

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 8 OF 22	Attorney Docket No.	TSSRA.012C1

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	200	EP 0209173 A	01-21-1987	PHILIPS NV		
	201	EP 1130647 A2	09-05-2001	HALKIAS GEORGE		
	202	JP S54-116888 A	09-11-1979	HITACHI LTD		
	203	JP S54-155770 A	12-08-1979	NIPPON ELECTRIC CO		
	204	JP S60-167439 A	08-30-1985	NIPPON ELECTRIC CO		
	205	JP S62-031138 A	02-10-1987	NEC CORP		
	206	JP S63-237408 A	10-03-1988	SUMITOMO METAL MINING CO		
	207	JP S63-246841 A	10-13-1988	TOSHIBA CORP		
	208	JP H01-259546 A	10-17-1989	FUJITSU LTD		
	209	JP H02-177435 A	07-10-1990	SONY CORP		
	210	JP H03-070155 A	03-26-1991	OKI ELECTRIC IND CO LTD		
	211	JP H03-101128 A	04-25-1991	CASIO COMPUTER CO LTD		
	212	JP H06-302486	10-28-1994	NIPPONDENSO CO LTD		
	213	JP H08-213548	08-20-1996	FRAUNHOFER GES FORSCHUNG		
	214	JP H10-092702 A	04-10-1998	AGENCY OF IND SCIENCE & TECHNOL		
	215	JP H10-223495	08-21-1998	NIPPON TELEGRAPH & TELEPHONE		
	216	JP H11-335631	12-07-1999	DEGUSSA		
	217	JP 2006-517344 A	07-20-2006	ZIPTRONIX INC		
	218	JP 2008-535230 A	08-28-2008	SOITEC SILICON ON INSULATOR		
	219	KR 1999-0083518	04-27-1999	DEGUSSA		
	220	WO 96/13060 A	05-02-1996	DAIMLER-BENZ AKTIENGESELLSCHAFT		

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 9 OF 22	Attorney Docket No.	TSSRA.012C1

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>
	221	WO 98/13860	04-02-1998	FRAUNHOFER-GESELLSCHAFT ZUR FÖRDERUNG DER ANGEWANDTEN FORSCHUNG E.V.		
	222	WO 98/45130 A	10-15-1998	LEEDY, Glenn J.		
	223	WO 99/46809	09-16-1999	HARRIS CORPORATION		
	224	WO 01/026137 A	04-12-2001	ZIPTRONIX, INC.		
	225	WO 01/061743 A	08-23-2001	ZIPTRONIX, INC.		
	226	WO 04/071700 A2	08-26-2004	ZIPTRONIX, INC.		
	227	WO 06/111533 A1	10-26-2006	S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	228	"Deliberate Design for Assuring Adequate Thermal Oxide Sidewall at the Corners of Trenches", IBM Technical Disclosure Bulletin, Jul. 1991, pp. 261-262.	
	229	"Metal Oxide Circuits on Silicon Membranes", IBM Technical Disclosure Bulletin, Oct. 1979, p. 2079.	
	230	"Smart Cut: A Promising New SOI Material Technology", M. Bruel et al.; Proceedings 1995 IEEE Int'l SOI Conference, Oct. 1995, pp. 178-179.	
	231	"Wafer Bonding With Stress-Free Trench Isolation", IBM Technical Disclosure Bulletin, Jul. 1991, pp. 304-305.	
	232	"Fabrication on Planar Arrays of Semiconductor Chips Separated by Insulating Barriers," IBM Technical Disclosure Bulletin, Apr. 1965, p. 1103.	
	233	A. Berthold, et al., Sensors and Actuators, vol. A68, pp. 410-413, "Wafer-to-Wafer Fusion Bonding of Oxidized Silicon to Silicon at Low Temperatures", 1998.	
	234	A. Kazor, et al., Appl. Phys. Lett., vol. 65, No. 12, pp. 1572-1574, "Fluorine Enhanced Oxidation of Silicon at Low Temperatures", Sep. 19, 1994.	
	235	A. Plössl, et al., Materials Science & Engineering, vol. R 25, Nos. 1-2, pp. 1-88, "Wafer Direct Bonding: Tailoring Adhesion Between Brittle Materials", Mar. 10, 1999.	
	236	A. von Keudell, et al., Appl. Phys. Lett., vol. 71, No. 26, pp. 3832-3834, "Evidence for Atomic H Insertion Into Strained Si-Si Bonds in the Amorphous Hydrogenated Silicon Subsurface From in Situ Infrared Spectroscopy", Dec. 29, 1997.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 10 OF 22	Attorney Docket No.	TSSRA.012C1

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	237	A.H. Mahan, et al., Physical Review B., vol. 40, No. 17, pp. 12024-12027, "Characterization of Microvoids in device-quality Hydrogenated Amorphous Silicon by Small-Angle X-Ray Scattering and Infrared Measurements", Dec. 15, 1989.	
	238	Alex Q. Huang, IEEE Transactions on Electron Devices, vol. 43, No. 6, pp. 1029-1032, "Analysis of the Inductive Turn-Off of Double Gate MOS Controlled Thyristors", Jun. 1996.	
	239	Amirfeiz et al., "Formation of Silicon Structures by Plasma Activated Wafer Bonding", Proceedings of the 5.sup.th Semiconductor Wafer Bonding Symposium, Oct. 1999, 11 pages.	
	240	Andreas Plössl et al., "The Interface of Silicon Sampled Joined at Room Temperature by Wafer Direct Bonding in Ultrahigh Vacuum", Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology, vol. 2, pp. 1361-1372, 1998.	
	241	Andreas Schumacher et al., The Bonding Energies of Oxidized Silicon Wafers for Micromechanical Applications at Moderate Temperatures, 97-36 Electrochemical Society Proceedings 155 (1998).	
	242	Auberton-Herve, et al., Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology, Silicon Materials Science and Technology, vol. 2, Electrochemical Society Proceedings, vol. 98-1, pp. 1341-1360, "Silicon on Insulator Wafers Using the Smart Cut.RTM. Technology", 1998.	
	243	B. Agarwal, et al., IEEE Electron Device Letters, vol. 18, No. 5, pp. 228-231, "A 227-GHz fmax Transferred-Substrate Heterojunction Bipolar Transistor", May 1997.	
	244	B. Anthony et al., "In situ Cleaning of Silicon Substrate Surfaces by Remote Plasma-Excited Hydrogen" J. Vac. Sci. Technol. B7, 621-626 (Jul./Aug. 1989), American Vacuum Society 1989.	
	245	B. Aspar et al., "Smart-Cut Process Using Metallic Bonding Application to Transfer of Si, GaAs, InP thin films", Electronics Letters, Jun. 10, 1999, vol. 35, No. 12 pp. 1024-1025.	
	246	B. Aspar, et al., Microelectronic Engineering, vol. 36, pp. 233-240, "Basic Mechanisms Involved in the Smart-Cut.RTM. Process", 1997.	
	247	B.E. Roberds, et al., Electrochemical Society Proceedings, vol. 97-36, pp. 592-597, "Wafer Bonding of GaAs, InP, and Si Annealed Without Hydrogen for Advanced Device Technologies," 1997.	
	248	B.E. Roberds, et al., Electrochemical Society Proceedings, vol. 97-36, pp. 598-606, "Low Temperature, in Situ, Plasma Activated Wafer Bonding," 1997.	
	249	B.M. Arora, et al., J. Vac. Sci. Technol. vol. B5, No. 4, pp. 876-882, "Reactive Ion-Etching-Induced Damage in Silicon Using SF6 Gas Mixtures", Jul./Aug. 1987.	
	250	Barry E. Burke, et al., Soft-X-Ray CCD Imagers for AXAF, IEEE Transactions on Electron Devices, vol. 44, No. 10, Oct. 1997, pp. 1633-1642.	
	251	Baumgart et al., "Evaluation of Wafer Bonding and Etch Back for Soi Technology" Philips J. Res., vol. 49, No. 1/2 (1995) 91-124.	
	252	Bernard S. Meyerson, et al., Appl. Phys. Lett., vol. 57, No. 10, pp. 1034-1036, "Bistable Conditions for Low-Temperature Silicon Epitaxy", Sep. 3, 1990.	
	253	Biermann et al., "Direct Bonding: From an Optical Technology to a Broad Research Topic" Special Issue on Direct Bonding, Philips J. Res., vol. 49, p. 1-10, 1995.	
	254	Bollmann et al., Three Dimensional Metallization for Vertically Integrated Circuits, 1997 Materials for Advanced Metallization MAM '97 Abstracts Booklet 94.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 11 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	255	Burhan Bayraktaroglu, et al., IEEE Electron Device Letters, vol. 14, No. 10, pp. 493-495, "Very High-Power-Density CW Operation of GaAs/AlGaAs Microwave Heterojunction Bipolar Transistors", Oct. 1993.	
	256	C. B. Eom et al., Fabrication of Double Sided YBa2Cu3O7 Thin Films on 2 Inch Diameter LaAlO3 Wafers by Direct Wafer Bonding, 7 IEEE Transactions on Applied Superconductivity 1244 (1997).	
	257	C. den Besten, et al., IEEE Micro Electro Mechanical Systems, pp. 104-109, "Polymer Bonding of Micro-Machined Silicon Structures", Feb. 4-7, 1992.	
	258	C. Gui et al., "Present and Future Role of Chemical Mechanical Polishing in Wafer Bonding", Journal of the Electrochemical Society, vol. 145, No. 6, pp. 2198-2204, Jun. 1998.	
	259	C. Harendt et al., "Vertical Polysilicon Interconnects by Aligned Wafer Bonding," 97-36 Electrochemical Society Proceedings 501 (1998).	
	260	Ciarlo, Dino R., Proceedings of the Second International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 93-29, pp. 313-326, "High- and Low-Temperature Bonding Techniques for Microstructures", May 1993.	
	261	Cynthia A. Desmond et al., Low-Temperature Atmospheric Silicon-Silicon Wafer Bonding for Power Electronic Applications, 97-36 Electrochemical Society Proceedings 459 (1998).	
	262	D. Graf, et al., J. Vac. Sci. Technol., A7(3), pp. 808-813, "Reaction of Water with Hydrofluoric Acid Treated Silicon (111) and (100) Surfaces", May/Jun. 1989.	
	263	D.E. Booth et al., Backside Imaging CCD Using Bonded and Etched Back Silicon on Epoxy, 97-36 Electrochemical Society Proceedings 584 (1998).	
	264	Darrell Hill, et al., IEEE Microwave and Guided Wave Letters, vol. 5, No. 11, pp. 373-375, "Novel HBT with Reduced Thermal Impedance", Nov. 1995.	
	265	David W. Oberlin, A New Air-Isolation Process for Monolithic Integrated Circuits, 17 IEEE Transactions on Electron Devices 485 (1970).	
	266	Diego Feijoó et al., Silicon Wafer Bonding Studied by Infrared Absorption Spectroscopy, 65 Applied Physics Letters 2548, 2548 (1994).	
	267	Donato Pasquariello, et al., Journal of the Electrochemical Society, vol. 147, No. 6, pp. 2343-2346, "Mesa-Spacers: Enabling Nondestructive Measurement of Surface Energy in Room Temperature Wafer Bonding", 2000.	
	268	Donato Pasquariello, et al., Journal of the Electrochemical Society, vol. 147, No. 7, pp. 2699-2703, "Oxidation and Induced Damage in Oxygen Plasma in Situ Wafer Bonding", 2000.	
	269	E. Bertagnolli, et al., Interchip Via Technology Three-Dimensional Metallization for Vertically Integrated Circuits, Electrochemical Society Proceedings, vol. 97-36, pp. 509-520 (2000).	
	270	E. Jalaguier et al., "Transfer of 3 in GaAs Film on Silicon Substrate by Proton Implantation Process", Electronic Letters, Feb. 19, 1998, vol. 34, No. 4 pp. 408-409.	
	271	E. Jalaguier et al., Transfer of Thin InP Films onto Silicon Substrate by Proton Implantation Process, 11th Int. Conf. on Indium Phosphide and Related Materials, May 16-20, IEEE 1999, pp. 26-27.	
	272	Egloff et al., "Evaluation of Strain Sources in Bond and Etchback Silicon-on-Insulator" Philips J. Res. 49 (1995) pp. 125-138.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 12 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	273	Eliezer M. Rabinovich, et al., J. Am. Ceram. Soc., vol. 72, No. 7, pp. 1229-1232, "Retention of Fluorine in Silica Gels and Glass", 1989.	
	274	EP 01 92 0489; European Search Report; Jun. 6, 2003, 4 pages.	
	275	F.J. Kub et al., "Single-Crystal Ferroelectric Microwave Capacitor Fabricated by Separation by Hydrogen Implantation", Electronics Letters, Mar. 18, 1999, vol. 35, No. 6, pp. 477-478.	
	276	F.J. Kub, et al., The 1999 Joint International Meeting, vol. 99-2, Abstract No. 1031, 1 page, "A Double-Side IGBT by Low Temperature Wafer Bonding," Oct. 17-22, 1999.	
	277	Farrens et al., "Chemical Free Room Temperature Wafer to Wafer Direct Bonding", J. Electrochem. Soc., vol. 142, No. 11, Nov. 1995, pp. 3949-3955.	
	278	Farzad Pourahmadi, et al., IEEE Solid-State Sensor and Actuator Workshop: Technical Digest, pp. 144-147, "Variable-Flow Micro-Valve Structure Fabricated with Silicon Fusion Bonding", Jun. 4-7, 1990.	
	279	Fritz J. Kub et al., Electrical Characteristics of Low Temperature Direct Silicon-Silicon Bonding for Power Device Applications, 97-36 Electrochemical Society Proceedings 466 (1998).	
	280	Fromm et al., Interaction of Oxygen and Nitrogen With Clean Transition Metal Surfaces, Surface Science 74 (1978) pp. 259-275.	
	281	G. Hess, et al., Appl. Phys. Lett., vol. 71, No. 15, pp. 2184-2186, "Evolution of Subsurface Hydrogen From Boron-Doped Si(100)," Oct. 13, 1997.	
	282	G. Krauter et al., "Low Temperature Silicon Direct Bonding for Application in Micromechanics: Bonding Energies for Different Combinations of Oxides", Sensors and Actuators A 70, 271-275, 1998 Elsevier Science S.A.	
	283	G.A.C.M. Spierings, et al., "Direct Bonding of Organic Polymeric Materials", Philips J. Res. 49 (1995) pp. 139-149.	
	284	G.A.C.M. Spierings, et al., Philips Journal of Research, vol. 49, No. 1/2, pp. 47-63, "Surface-Related Phenomena in the Direct Bonding of Silicon and Fused-Silica Wafer Pairs", 1995.	
	285	G.A.C.M. Spierings, et al., Proceedings of the First International Symposium on Semiconductor Wafer Bonding. Science, Technology, and Applications, Proceedings vol. 92-7, pp. 18-32, "Diversity and Interfacial Phenomena in Direct Bonding", (1992).	
	286	George P. Imthum, et al., J. Appl. Phys., vol. 72, No. 6, pp. 2526-2527, "Bonded Silicon-on-Sapphire Wafers and Devices", Sep. 15, 1992.	
	287	Goetz, "Generalized Reactive Bonding," Proceedings of the 1 <sup>st</sup> Semiconductor Wafer Bonding Symposium, 1991, pp. 65-73.	
	288	Gösele, U., et al., "Semiconductor Wafer Bonding, a Flexible Approach to Materials Combinations in Microelectronics, Micromechanics and Optoelectronics", 1997 IEEE, pp. 23-32.	
	289	Gudrun Kissinger, et al., Sensors and Actuators, vol. A36, pp. 149-156, "Void-Free Silicon-Wafer-Bond Strengthening in the 200-400°C Range", 1993.	
	290	H. J. Quenzer et al., Low Temperature Wafer Bonding for Micromechanical Applications, 1992 Micro Electro Mechanical Systems, 1992, MEMS '92 49, 52.	
	291	H. Takagi, et al., Appl. Phys. Lett., vol. 68, No. 16, pp. 2222-2224, "Surface Activated Bonding of Silicon Wafers at Room Temperature," Apr. 15, 1996.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 13 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	292	H. Takagi, et al., Jpn. J. Appl. Phys. vol. 28, Part 1, No. 3A, pp. 1589-1594, "Transmission Electron Microscope observations of Si/Si Interface Bonded at Room Temperature by Ar Beam Surface Activation", Mar. 1999.	
	293	Haisma et al., "Diversity and Feasibility of Direct Bonding: A Survey of a Dedicated Optical Technology", Applied Optics, 33, pp. 1154-1169 (Mar. 1994).	
	294	Haisma et al., "Non-Silicon Applications of Direct Bonding" Philips J. Res. 49 (1995) pp. 151-163.	
	295	Haisma et al., "Silicon-Wafer Fabrication and (Potential) Applications of Direct-Bonded Silicon", Philips J. Res. 49 (1995) pp. 65-89.	
	296	Haisma et al., "Surface Preparation and Phenomenological Aspects of Direct Bonding", Philips J. Res. 49 (1995) pp. 23-46.	
	297	Henry Nielsen, et al., J. Electrochem. Soc.: Solid-State Science and Technology, vol. 130, No. 3, pp. 708-711, "Some Illumination on the Mechanism of SiO <sub>2</sub> Etching in HF Solutions", Mar. 1983.	
	298	Hideki Takagi et al., "Low-Temperature Direct Bonding of Silicon and Silicon Dioxide by the Surface Activation Method", Sensors and Actuators A, vol. 70, No. 1-2, pp. 164-170, Oct. 1, 1998.	
	299	Hideki Takagi, et al., Appl. Phys. Lett., vol. 74, No. 16, pp. 2387-2389, "Room-Temperature Bonding of Lithium Niobate and Silicon Wafers by Argon-Beam Surface Activation", Apr. 19, 1999.	
	300	Hideki Yokoi et al., Analysis of GaInAsP Surfaces by Contact-Angle Measurement for Wafer Direct Bonding with Garnet Crystals, 38 Japanese J. Applied Physics 4780 (1999).	
	301	Hochbauer, et al., Appl. Phys. Lett., vol. 75, No. 25, pp. 3938-3940, "Hydrogen Blister Depth in Boron and Hydrogen Coimplanted N-Type Silicon", Dec. 20, 1999.	
	302	Hyeokjae Lee, et al., IEDM Technical Digest, vol. 95-683, pp. 28.2.1-28.2.4, "A New Leakage Component Caused by the Interaction of Residual Stress and the Relative Position of Poly-Si Gate at Isolation Edge", Dec. 10-13, 1995.	
	303	International Conference on Compliant & Alternative Substrate Technology, Meeting Program & Abstract Book, Sep. 19-23, 1999 Disney's Boardwalk Inn, Lake Buena Vista, FL total of 6 pages.	
	304	Itoh et al., "Room temperature vacuum sealing surface activated bonding method," June 8-12, 2003, IEEE, pp. 1828-1831.	
	305	J. Bagdahn, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 291-298, "Characterization of Directly Bonded Silicon Wafers by Means of the Double Cantilever Crack Opening Method", (1998).	
	306	J. Haisma et al., "Silicon-on-Insulator Wafer Bonding-Wafer Thinning", Japanese J. Appl. Phys, vol. 28, No. 8; pp. 1426-1443; 1989.	
	307	J. Haisma, "Direct Bonding in Patent Literature ", Philips Journal of Research, vol. 49, No. 1/2 (1995), pp. 165-170.	
	308	J. Haisma, "Direct Bonding: Retrospect and Outlook", Philips Journal of Research, vol. 49, No. 1/2 (1995), pp. 171-177.	
	309	J. Köhler et al., Weibull Fracture Probability for Silicon Wafer Bond Evaluation, 147 J. Electrochemical Society 4683, 4683, 4685 (2000).	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 14 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	310	J.B. Lasky, Appl. Phys. Lett., vol. 48, No. 1, "Wafer Bonding for Silicon-on-Insulator Technologies", Jan. 6, 1986.	
	311	J.B. Lasky, et al., IEDM Technical Digest, vol. 85, pp. 684-687, "Silicon-on-Insulator (SOI) by Bonding and Etch-Back", Dec. 1-4, 1985.	
	312	J.F. Jensen, et al., IEEE Journal of Solid-Stated Circuits, vol. 30, No. 10, pp. 1119-1127, "A 3.2-GHz Second-Order Delta-Sigma Modulator Implemented in InP HBT Technology", Oct. 1995.	
	313	J.F. Klem et al., "Characterization of Thin AlGaAs/InGaAs/GaAs Quantum-Well Structure Bonded Directly to SiO <sub>2</sub> /Si and Glass Substrates," J. Appl. Phys., 66(1), Jul. 1989, pp. 459-462.	
	314	Jan Haisma et al., "Frameworks for Direct Bonding", Philips J. Res. 49 (1995) pp. 11-21.	
	315	Japanese Office Action issued May 29, 2012, in Patent Application No. 2001-560438 (with English Translation).	
	316	Jeffrey T. Borenstein, et al., J. Appl. Phys., vol. 73, No. 6, pp. 2751-2754, "Kinetic Model for Hydrogen Reactions in Boron-Doped Silicon", Mar. 15, 1993.	
	317	Jiwei Jiao, et al., Sensors and Actuators, vol. A50, pp. 117-120, "Low-Temperature Silicon Direct Bonding and Interface Behaviours", 1995.	
	318	John S. Judge, J. Electrochem. Soc.: Solid State Science, vol. 118, No. 11, pp. 1772-1775, "A Study of the Dissolution of SiO <sub>2</sub> in Acidic Fluoride Solutions", Nov. 1971.	
	319	K. Bergman, et al., Physical Review B, vol. 37, No. 5, pp. 2770-2773, "Donor-Hydrogen Complexes in Passivated Silicon", Feb. 15, 1988.	
	320	K. Henttinen et al., Mechanically Induced Si Layer Transfer in Hydrogen-Implanted Si Wafers, 76 Applied Physics Letters 2370 (2000).	
	321	K.D. Hobart et al., Fabrication of a Double-Side IGBT by Very Low Temperature Wafer Bonding, 1999 Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs 45, 46 (1999).	
	322	K.D. Hobart, et al., Applied Physics Letters, vol. 72, No. 9, pp. 1095-1097, "Characterization of Si pn Junctions Fabricated by Direct Wafer Bonding in Ultra-High Vacuum," Mar. 2, 1998.	
	323	Karin Ljungberg et al., Improved Direct Bonding of Si and SiO <sub>2</sub> Surfaces by Cleaning in H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :HF, 67 Applied Physics Letters 650 (1995).	
	324	Karin Ljungberg, et al., Appl. Phys. Lett., vol. 62, No. 12, pp. 1362-1364, "Spontaneous Bonding of Hydrophobic Silicon Surfaces", Mar. 22, 1993.	
	325	Karin Ljungberg, et al., Electrochemical Society Proceedings, vol. 95-7, pp. 163-173, "Modification of Silicon Surfaces with H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :HF and HNO <sub>3</sub> :HF for Wafer Bonding Applications", (1996).	
	326	Kim, et al., Appl. Phys. Lett., vol. 69, No. 25, pp. 3869-3871, "Effects of B Doping on Hydrogen Desorption from Si(001) During Gas-Source Molecular-Beam Epitaxy From Si <sub>2</sub> H <sub>6</sub> and B <sub>2</sub> H <sub>6</sub> ," Dec. 16, 1996.	
	327	Kiyoshi Mitani, et al., Jpn. J. Appl. Phys., vol. 30, No. 4, pp. 615-622, "Causes and Prevention of Temperature-Dependent Bubbles in Silicon Wafer Bonding", Apr. 1991.	
	328	Kiyoshi Mitani, et al., Jpn. J. Appl. Phys., vol. 31, Part 1, No. 4, pp. 969-974, "A New Evaluation Method of Silicon Wafer Bonding Interfaces and Bonding Strength by KOH Etching", Apr. 1992.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 15 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	<b>329</b>	Ko, W.H., et al., Micromachining and Micropackaging of Transducers, pp. 41-61, "Bonding Techniques for Microsensors", 1985.	
	<b>330</b>	Korean Office Action issued Dec. 28, 2011, in Patent Application No. 10-2011-7015751 (with English-language translation).	
	<b>331</b>	Korean Office Action Issued Nov. 27, 2012 in Patent Application No. 10-2011-7015751 (with English translation).	
	<b>332</b>	Kouvatsos, et al., Appl. Phys. Lett., vol. 61, No. 7, pp. 780-782, "Silicon-Fluorine Bonding and Fluorine Profiling in SiO <sub>2</sub> Films Grown by NF <sub>3</sub> -Enhanced Oxidation", Aug. 17, 1992.	
	<b>333</b>	Ku et al., "Low Stress Tungsten Absorber for X-Ray Masks", Microelectronic Engineering, vol. 11, No. 1-4, Apr. 1990, pp. 303-308.	
	<b>334</b>	L. Di Cioccio et al., "Silicon Carbide on Insulator Formation Using the Smart Cut Process", Electronics Letters, Jun. 6, 1996, vol. 32, No. 12, pp. 1144-1147.	
	<b>335</b>	L. Rayleigh, Proceedings of the Royal Society of London, Series A-Mathematical and Physical Sciences, vol. 156, pp. 326-349, "A Study of Glass Surfaces in Optical Contact", Sep. 1, 1936.	
	<b>336</b>	Lehmann et al., "Bubble-Free Wafer Bonding of GaAs and InP on Silicon in a Microcleanroom", Jpn. J. Appl. Phys., 28, pp. 2141-2143 (Dec. 1989).	
	<b>337</b>	Leslie A. Field, et al., Sensors and Actuators, vol. A21-A23, pp. 935-938, "Fusing Silicon Wafers with Low Melting Temperature Glass", 1990.	
	<b>338</b>	Li et al., Low temperature direct bonding using pressure and temperature, SPIE, vol. 3184, 124-27 (1997).	
	<b>339</b>	Lusson, et al., J. Appl. Phys., vol. 81, No. 7, pp. 3073-3080, "Hydrogen Configurations and Stability in Amorphous Sputtered Silicon", Apr. 1, 1997.	
	<b>340</b>	M. Bruel, Electronics Letters, vol. 31, No. 14, pp. 1201-1202, "Silicon on Insulator Material Technology", Jul. 6, 1995.	
	<b>341</b>	M. Grundner, et al., Appl. Phys. A, vol. 39, pp. 73-82, "Investigations on Hydrophilic and Hydrophobic Silicon (100) Wafer Surfaces by X-Ray Photoelectron and High-Resolution Electron Energy Loss-Spectroscopy", 1986.	
	<b>342</b>	M. Morita, et al., Appl. Phys. Lett., vol. 45, No. 12, pp. 1312-1314, "Fluorine-Enhanced Thermal Oxidation of Silicon in the Presence of NF <sub>3</sub> ", Dec. 15, 1984.	
	<b>343</b>	M. Petzold, et al., Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications Proceedings vol. 95-7, pp. 380-389, "Interface Strength Characterization of Bonded Wafers" (1995).	
	<b>344</b>	M. S. Ismail et al., One-Step Direct Bonding Process of Low Temperature Si <sub>3</sub> N <sub>4</sub> and TiN Technology, 1993 Proceedings of the 7th International Conference on Solid State Sensors and Actuators, 188 (1993).	
	<b>345</b>	M. Shimbo, et al., J. Appl. Phys., vol. 60, No. 8, pp. 2987-2989, "Silicon-to-Silicon Direct Bonding Method", Oct. 15, 1986.	
	<b>346</b>	M. Yoshimaru, et al., J. Vac. Sci. Technol. A, vol. 15, No. 6, pp. 2915-2922, "Interaction Between Water and Fluorine-Doped Silicon Oxide Films Deposited by Plasma-Enhanced Chemical Vapor Deposition", Nov./Dec. 1997.	

Examiner Signature /Joannie Garcia/	Date Considered 05/11/2016
-------------------------------------	----------------------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 16 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	347	M.E. Grupen-Shemansky et al., "Stress in GaAs Bonded to Si", Proceedings of 1st International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, vol. 92-7, The Electrochemical Society, Pennington, NJ, 1992, pp. 132-145.	
	348	M.K. Weldon, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 229-248, "Mechanistic Studies of Silicon Wafer Bonding and Layer Exfoliation", (1998).	
	349	Martin A. Schmidt, Wafer-To-Wafer Bonding for Microstructure Formation, 86 Proceedings of the IEEE 1575, 1578 (1998).	
	350	Maszara et al., "Role of Surface Morphology in Wafer Bonding", J. Appl. Phys. 69(1) (Jan. 1991) pp. 257-260.	
	351	Michalske et al., "Closure and Repropagation of Healed Cracks in Silicate Glass," Journal of American Ceramic Society, vol. 68 pp. 586-590 (1985).	
	352	Mitani, Kiyoshi, Wafer Bonding: Studies of Interface Bubbles and Electrical Characterization, Department of Electrical Engineering, Duke University, 1991.	
	353	Mohd Salleh Ismail et al., Digital Pressure-Switch Array with Aligned Silicon Fusion Bonding, 1 J. Micromechanics and Microengineering 231 (1991).	
	354	N.Q. Khanh, et al., J. Electrochem. Soc., vol. 142, No. 7, pp. 2425-2429, "Nondestructive Detection of Microvoids at the interface of Direct Bonded Silicon Wafers by Scanning Infrared Microscopy", Jul. 1995.	
	355	Nakamura, et al., IEDM Technical Digest, vol. 95, pp. 889-892, "Giga-Bit DRAM Cells with Low Capacitance and Low Resistance Bit-Lines on Buried MOSFET's and Capacitors by Using Bonded SOI Technology-Reversed-Stacked-Capacitor (RSTC) Cell-", Dec. 10-13, 1995.	
	356	Nakanishi et al., "Studies on SiO <sub>2</sub> -SiO <sub>2</sub> Bonding with Hydrofluoric Acid-Room Temperature and Low Stress Bonding Technique for MEMS-", IEEE 1998, pp. 609-614.	
	357	Niwano, et al., J. Appl. Phys., vol. 71, No. 11, pp. 5646-5649, "Morphology of Hydrofluoric Acid and Ammonium Fluoride-Treated Silicon Surfaces Studied by Surface Infrared Spectroscopy", Jun. 1, 1992.	
	358	No Author, Electronics Letters, vol. 14, No. 18, pp. 593-594, "C.M.O.S. Devices Fabricated on Buried SiO <sub>2</sub> Layers Formed by Oxygen Implantation into Silicon", Aug. 31, 1978.	
	359	Office Action issued August 19, 2014 in Japanese Patent Application No. 2012-107053 (with English language translation)	
	360	Office Action issued Jan. 8, 2013 in Japanese Patent Application No. 2001-560438 (English language translation only).	
	361	Office Action issued May 13, 2014 In Japanese Patent Application No. 2013 -143038 with English language translation	
	362	Office Action issued Oct. 15, 2013 in Japanese patent Application No. 2001-560438 with English language translation.	
	363	Office Action mailed on Dec. 17, 2013, in Japanese Patent Application 2012-107053 (English Translation Only).	
	364	P. Gupta, et al., Physical Review B, vol. 37, No. 14, pp. 8234-8243, "Hydrogen Desorption Kinetics From Monohydride and Dihydride Species on Silicon Surfaces", May 15, 1988.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 17 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	<b>365</b>	P.J.H. Denteneer, et al., Physical Review B, vol. 39, No. 15, pp. 10809-10824, "Microscopic Structure of the Hydrogen-Boron Complex in Crystalline Silicon", May 15, 1989.	
	<b>366</b>	Peter Bjeletich, et al., Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Proceedings vol. 97-36, pp. 349-357, "Electrical Characterization of Plasma Bonded SOI", (1999).	
	<b>367</b>	Peter J. Wright, et al., IEEE Transactions on Electron Devices, vol. 36, No. 5, pp. 879-889, "The Effect of Fluorine in Silicon Dioxide Gate Dielectrics", May 1989.	
	<b>368</b>	Peter P. Gillis, et al., Journal of Applied Physics, vol. 35, No. 3 (Part I), pp. 647-658, "Double-Cantilever Cleavage Mode of Crack Propagation", Mar. 1964.	
	<b>369</b>	Petersen et al., "Silicon fusion bonding for pressure sensors," in Technol. Dig. IEEE Solid State Sens. & Actuators Workshop, Hilton Head, SC, 1988, pp. 144-147.	
	<b>370</b>	Plossl, et al., Mat. Res. Soc. Symp. Proc., vol. 483, pp. 141-146, "Covalent Silicon Bonding at Room Temperature in Ultrahigh Vacuum," 1998.	
	<b>371</b>	Q. Lee, et al., IEEE Electron Device Letters, vol. 19, No. 3, pp. 77-79, "A > 400 GHz fmax Transferred-Substrate Heterojunction Bipolar Transistor IC Technology", Mar. 1998.	
	<b>372</b>	Q. Lee, et al., IEEE Electron Device Letters, vol. 20, No. 8, pp. 396-398, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors", Aug. 1999.	
	<b>373</b>	Q.-Y. Tong, "Room Temperature Silicon and SiO <sub>2</sub> Covalent Bonding in Ambient," Dec. 10, 1999, 9 pages.	
	<b>374</b>	Q.-Y. Tong et al, "The Role of Surface Chemistry in Bonding of Standard Silicon Wafers," J. Electrochem. Soc., vol. 144, No. 1, pp. 384-389 (Jan. 1997).	
	<b>375</b>	Q.-Y. Tong et al., "Wafer Bonding of Si With Dissimilar Materials," pp. 524-526 (1995).	
	<b>376</b>	Q.-Y. Tong et al., 1999 IEEE International SOI Conference, pp. 104-105, "IOS-A New Type of Materials Combination for System-on-a Chip Preparation," Oct. 1999.	
	<b>377</b>	Q.-Y. Tong et al., Adv. Mater., vol. 11, No. 17, pp. 1409-1425, "Wafer Bonding and Layer Splitting for Microsystems", 1999.	
	<b>378</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 64, No. 5, pp. 625-627, "Hydrophobic Silicon Wafer Bonding," Jan. 31, 1994.	
	<b>379</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 70, No. 11, pp. 1390-1392, "Layer Splitting Process in Hydrogen-Implanted Si, Ge, SiC, and Diamond Substrates", Mar. 17, 1997.	
	<b>380</b>	Q.-Y. Tong et al., Appl. Phys. Lett., vol. 72, No. 1, pp. 49-51, "A "Smarter-Cut" Approach to Low Temperature Silicon Layer Transfer", Jan. 5, 1998.	
	<b>381</b>	Q.-Y. Tong et al., Diffusion and Oxide Viscous Flow Mechanism in SDB Process and Silicon Wafer Rapid Thermal Bonding, 26 Electronic Letters 697 (1990).	
	<b>382</b>	Q.-Y. Tong et al., Electrochemical and Solid-State Letters, vol. 1, No. 1, pp. 52-53, "Low Vacuum Wafer Bonding", 1998.	
	<b>383</b>	Q.-Y. Tong et al., Electronics Letters, vol. 35, No. 4, pp. 341-342, "Low Temperature InP Layer Transfer", Feb. 18, 1999.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 18 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	384	Q.-Y. Tong et al., Feasibility Study of VLSI Device Layer Transfer by CMP PETEOS Direct Bonding, Proceedings 1996 IEEE International SOI Conference, Oct. 1996 pp. 36 and 37.	
	385	Q.-Y. Tong et al., J. Electrochem. Soc., vol. 143, No. 5, pp. 1773-1779, "A Model of Low-Temperature Wafer Bonding and its Applications", May 1996.	
	386	Q.-Y. Tong et al., Low Temperature Si Layer Splitting, 1997 Proceedings 1997 IEEE International SOI Conference 126.	
	387	Q.-Y. Tong et al., Materials Chemistry and Physics, vol. 37, pp. 101-127, "Semiconductor Wafer Bonding: Recent Developments", 1994.	
	388	Q.-Y. Tong et al., MRS Bulletin, pp. 40-44, "Beyond "Smart-Cut.RTM.": Recent Advances in Layer Transfer for Material Integration", Dec. 1998.	
	389	Q.-Y. Tong et al., Semiconductor Wafer Bonding Science and Technology, John Wiley & Sons, Inc., 1999.	
	390	Q.-Y. Tong et al., Silicon Carbide Wafer Bonding, 142 J. Electrochemical Society 232 (1995).	
	391	Q.-Y. Tong et al., Thickness Considerations in Direct Silicon Wafer Bonding, 142 J. Electrochemical Society 3975 (1995).	
	392	Q.-Y. Tong et al., Transfer of Semiconductor and Oxide Films by Wafer Bonding and Layer Cutting, 29 J. Electronic Materials 928 (2000).	
	393	Qing-An Huang et al., Biased-Voltage Controlled Thinning for Bonded Silicon-On-Insulator Wafers, 66 Applied Physics Letters 2990 (1995).	
	394	R. Dekker, et al., IEDM Technical Digest, vol. 97, pp. 921-923, "An Ultra Low-Power RF Bipolar Technology on Glass", Dec. 7-10, 1997.	
	395	R. Kasi, et al., Appl. Phys. Lett., vol. 58, No. 25, pp. 2975-2977, "Chemistry of Fluorine in the Oxidation of Silicon", Jun. 24, 1991.	
	396	R. Stengl, et al., Jpn. J. Appl. Phys., vol. 28, No. 10, pp. 1735-1741, "A Model for the Silicon Wafer Bonding Process", Oct. 1989.	
	397	R. Stengl, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2311-L2314, "Bubble-Free Silicon Wafer Bonding in a NonCleanroom Environment", Dec. 1988.	
	398	R.W. Bower et al., Aligned Wafer Bonding: A Key to Three Dimensional Microstructures, 20 J. Electronic Materials 383, 383 (1991).	
	399	Reiche et al., "The Effect of a Plasma Pretreatment of the Si/Si Bonding Behavior", Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science and Technology and Applications, the Electrochemical Society, Pennington, NJ 1998, pp. 437-444.	
	400	Ritsuo Takizawa, et al., Jpn. J. Appl. Phys., vol. 27, No. 11, pp. L2210-L2212, "Ultraclean Technique for Silicon Wafer Surfaces with HNO3-HF Systems", Nov. 1998.	
	401	Robert W. Bower et al., Design Considerations of a Digital Pressure Sensor Array, 1991 International Conference on SolidState Sensors and Actuators, 1991. Digest of Technical Papers, Transducers, '91 312.	
	402	Robert W. Bower et al., Low Temperature S3N4 Direct Bonding, 62 Applied Physics Letters 3485 (1993).	

Examiner Signature /Joannie Garcia/	Date Considered 05/11/2016
-------------------------------------	----------------------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 19 OF 22	Attorney Docket No.	TSSRA.012C1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	403	Rochdi Messoussi, et al., Jpn. J. Appl. Phys., vol. 35, Part 1, No. 4A, pp. 1989-1992, "Improvement of Rinsing Efficiency After Sulfuric Acid Hydrogen Peroxide Mixture (H <sub>2</sub> SO <sub>4</sub> /H <sub>2</sub> O <sub>2</sub> ) by HF Addition", 1996.	
	404	Room Temperature Silicon Wafer Direct Bonding in Vacuum by Ar Beam Irradiation by Takagi H., Maeda R., Ando Y., Suga T., Micro Electron Mechanical Systems, 1997. MEMS '97, Proceedings, IEEE., Tenth Annual International Workshop on pp. 191-196, Jan. 23-30, 1997.	
	405	Ross, R.C., et al., Journal of Non-Crystalline Solids, vol. 66, pp. 81-86, "Physical Microstructure in Device-Quality Hydrogenated Amorphous Silicon", 1984.	
	406	S. Bengtsson, et al., International Conference on Compliant & Alternative Substrate Technology, p. 10, "Low Temperature Bonding," Sep. 1999.	
	407	S. Farrens, Electromechanical Society Proceedings, vol. 97-36, pp. 425-436, "Low Temperature Wafer Bonding," 1997.	
	408	S. Fujino, et al., Jpn. J. Appl. Phys., vol. 34, No. 10B, 1 page, "Silicon Wafer Direct Bonding Through the Amorphous Layer," Oct. 15, 1995.	
	409	S. Mack, et al., J. Electrochem. Soc., vol. 144, No. 3, pp. 1106-1111, "Analysis of Bonding-Related Gas Enclosure in Micromachined Cavities Sealed by Silicon Wafer Bonding", Mar. 1997.	
	410	S. N. Farrens et al., A Kinetics Study of the Bond Strength of Direct Bonded Wafers, 141 J. Electrochemical Society 3225 (1994).	
	411	S. Schulze, et al., Proceedings of the Second International Symposium on Microstructures and Microfabricated Systems, Proceedings vol. 95-27, pp. 309-318, "Investigation of Bonded Silicon-Silicon-Interfaces Using Scanning Acoustic Microscopy", (1995).	
	412	S. V. Hattangady et al., "In situ Cleaning of GaAs Surface Using Hydrogen Dissociated With a Remote Noble-Gas Discharge," J. Appl. Phys. 68(3), pp. 1233-1236, (Aug. 1990).	
	413	S.A. McQuaid, et al., J. Appl. Phys., vol. 81, No. 11, pp. 7612-7618, "Passivation, Structural Modification, and Etching of Amorphous Silicon in Hydrogen Plasmas", Jun. 1, 1997.	
	414	S.J. Pearton, et al., Appl. Phys. A, vol. 43, pp. 153-195, "Hydrogen in Crystalline Semiconductors", 1987.	
	415	Sailer et al., Creating 3D Circuits Using Transferred Films, Circuits and Devices, IEEE 1997, Nov. 1997, pp. 27-30.	
	416	Sakaguchi et al., Extremely High Selective Etching of Porous Si for Single Etch-Stop Bond-and-Etch-Back Silicon-on-Insulator, Jpn. J. Appl. Phys., vol. 34 (1995), pp. 842-847.	
	417	Satoshi Matsumoto et al., Thin-Film Quasi-SOI Power MOSFET Fabricated by Reversed Silicon Wafer Direct Bonding, 45 IEEE Transactions on Electron Devices 105 (1998).	
	418	Shi-Ji Lu et al., A New Silicon Micromachining Method Using SOI/SDB Technology, 23 Sensors and Actuators 961 (1990).	
	419	Shoji Yamahata, et al., IEEE Gallium Arsenide Integrated Circuit Symposium, Technical Digest 1995, pp. 163-166, "Over-220-GHz-fT-AND-fmax InP/InGaAs Double-Heterojunction Bipolar Transistors with a New Hexagonal Shaped Emitter", Oct. 29-Nov. 1, 1995.	
	420	Stefan Bengtsson et al., The Influence of Wafer Dimensions on the Contact Wave Velocity in Silicon Wafer Bonding, 69 Applied Physics Letters 3381 (1996).	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 20 OF 22	Attorney Docket No.	TSSRA.012C1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	421	Sun et al., "Cool Plasma Activated Surface in Silicon Wafer Direct Bonding Technology," Journal De Physique, pp. C4-79-C4-82, Sep. 1988.	
	422	Suzuki et al., "SiN Membrane Masks for X-Ray Lithography", Journal of Vacuum Science and Technology, vol. 20, No. 2, Feb. 1982, pp. 191-194.	
	423	T. Akatsu, et al., Journal of Applied Physics, vol. 86, No. 12, pp. 7146-7150, "GaAs Wafer Bonding by Atomic Hydrogen Surface Cleaning", Dec. 15, 1999.	
	424	T.M. Duncan, et al., J. Appl. Phys., vol. 60, No. 1, pp. 130-136, "Study of Fluorine in Silicate Glass With 19 F Nuclear Magnetic Resonance Spectroscopy", Jul. 1, 1986.	
	425	Tadahiro Ohmi, et al., Proceedings Fifth International IEEE VLSI Multilevel Interconnection Conference, pp. 261-267, "VLSI Interconnects for Ultra High Speed Signal Propagation", Jun. 13-14, 1988.	
	426	Takagi et al., "Wafer-scale room-temperature bonding between silicon and ceramic wafers by means of argon-beam surface activation", 2001, IEEE, pp.60-63.	
	427	Takao Abe, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2311-L2314, "Silicon Wafer Bonding Mechanism for Silicon-on-Insulator Structures", Dec. 1990.	
	428	Takashi Kurahashi et al., Sensors Utilizing Si Wafer Direct Bonding at Low Temperature, 1991 Proceedings of the 2nd International Symposium on Micro Machine and Human Science 173, 173.	
	429	Takeshi Sunada, et al., Jpn. J. Appl. Phys., vol. 29, No. 12, pp. L2408-L2410, "The Role of Fluorine Termination in the Chemical Stability of HF-Treated Si Surfaces", Dec. 1990.	
	430	Tong et al., Fabrication of Ultrathin SOI by SIMOX Wafer Bonding (SWB), Journal of Electronic Materials, vol. 22, No. 7, 1993, 763-768.	
	431	Tong et al., Materials with a Buried C60 Layer Produced by Direct Wafer Bonding, J. Electrochem. Soc., vol. 141, No. 10, Oct. 1994, 137-38.	
	432	Tong et al., Ultrathin single-crystalline silicon on quartz (SOQ) by 150 C wafer bonding, Sensors and Actuators A 48 (1995) 117-123.	
	433	Tong, Qin-Yi, "Low Temperature Wafer Direct Bonding", IEEE 1994, Journal of Microelectromechanical Systems, vol. 3, No. 1, Mar. 1994, pp. 29-35.	
	434	Trimble et al., "Evaluation of Polycrystalline Silicon Membranes on Fused Silica for X-Ray Lithography Masks", Journal of Vacuum Science and Technology B (Microelectronics Processing Phenomena), vol. 7, No. 6, Nov./Dec. 1989, pp. 1675-1679.	
	435	TSMC Answer to Second Amended Complaint, filed Aug. 27, 2012, pp. 1-80.	
	436	U. Bhattacharya, et al., IEEE Electron Device Letters, vol. 16, No. 8, pp. 357-359, "Transferred Substrate Schottky-Collector Heterojunction Bipolar Transistors: First Results and Scaling Laws for High fmax", Aug. 1995.	
	437	U. Gösele et al., "Wafer Bonding for Microsystems Technologies", Sensors and Actuators 74 (1999) 161-168, 1999 Elsevier Science S.A.	
	438	U. Gösele et al., "Fundamental Issues in Wafer Bonding", J. Vac. Sci. Technol. A 17(4), Jul./Aug., 1145-1152, (1999), American Vacuum Society.	
	439	U. Gösele et al., "Semiconductor Wafer Bonding", Annu. Rev. Mater. Sci. 1998, 28:215-41.	

Examiner Signature /Joannie Garcia/	Date Considered 05/11/2016
-------------------------------------	----------------------------

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 21 OF 22	Attorney Docket No.	TSSRA.012C1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	440	U. Gösele et al., History and Future of Semiconductor Wafer Bonding, 47-48 Solid State Phenomena 33 (1996).	
	441	U. Gösele, et al., Appl. Phys. Lett., vol. 67, No. 24, pp. 3614-3616, "Self-Propagating Room-Temperature Silicon Wafer Bonding in Ultrahigh Vacuum," Dec. 11, 1995.	
	442	V.H.C. Watt et al., Low Temperature Direct Bonding on Nonhydrophilic Surfaces, 30 Electronic Letters 693, 694 (1994).	
	443	Vanderwater et al., "High-Brightness AlGaInP Light Emitting Diodes," Proc. IEEE, vol. 85, No. 11, pp. 1752-1764, Nov. 1997.	
	444	W.E. Stanchina, et al., IEEE Gallium Arsenide Integrated Circuit Symposium, Technical Digest 1995, pp. 31-34, "An InP-Based HBT FAB for High-Speed Digital, Analog, Mixed-Signal, and Optoelectronic Ics", Oct. 29-Nov. 1, 1995.	
	445	W.K. Chu, et al., Physical Review B, vol. 16, No. 9, pp. 3851-3859, "Distribution of Irradiation Damage in Silicon Bombarded with Hydrogen", Nov. 1, 1977.	
	446	W.P. Maszara, et al., J. Appl. Phys., vol. 64, No. 10, pp. 4943-4950, "Bonding of Silicon Wafers for Silicon-on-Insulator", Nov. 15, 1988.	
	447	W.P. Maszara, J. Electrochem. Soc., vol. 138, No. 1, pp. 341-347, "Silicon-on-Insulator by Wafer Bonding: a Review", Jan. 1991.	
	448	Wen Hsiung Ko, et al., IEEE Transactions on Electron Devices, vol. ED-26, No. 12, pp. 1896-1905, "Development of a Miniature Pressure Transducer for Biomedical Applications", Dec. 1979.	
	449	William Liu, et al., IEEE Transactions on Electron Devices, vol. 40, No. 11, pp. 1917-1927, "Current Gain Collapse in Microwave Multifinger Heterojunction Bipolar Transistors Operated at Very High Power Densities", Nov. 1993.	
	450	Williams, et al., Journal of Applied Physics, vol. 46, No. 2, pp. 695-698, "Mobile Fluoride Ions in SiO <sub>2</sub> ", Feb. 1975.	
	451	Xu et al., Novel Two-Step SDB Technology for High-Performance Thin-Film SOI/MOSFET Applications, Electronics Letters, 3-16/1989, vol. 25, No. 6 pp. 394-395.	
	452	Xu et al., Silicon on Quartz by Solid-State Diffusion Bonding (SSDB) Technology, Electronics Letters, May 26, 1988, vol. 24, No. 11 pp. 691-692.	
	453	Y. Albert Li, et al., Jpn. J. Appl. Phys., vol. 39, Part 1, No. 1, pp. 275-276, "Surface Roughness of Hydrogen Ion Cut Low Temperature Bonded Thin Film Layers", Jan. 2000.	
	454	Y. Zhou et al., "Electrical Properties of Wafer-Bonded GaAs/Si Heterojunctions", Appl. Phys. Lett., vol. 73, No. 16, 1998 American Institute of Physics, pp. 2337-2339.	
	455	Y.H. Lo et al., "Wafer Bonding Technology and its Optoelectronic Applications," SPIE proc., vol. 3006, pp. 26-35, 1997.	
	456	Yasushiro Nishioka, et al., Appl. Phys. Lett., vol. 54, No. 12, pp. 1127-1129, "Dielectric Characteristics of Fluorinated Ultradry SiO <sub>2</sub> ", Mar. 20, 1999.	
	457	Yozo Kanda, et al., Sensors and Actuators, vol. A21-A23, pp. 939-943, "The Mechanism of Field-Assisted Silicon-Glass Bonding", 1990.	
	458	Zhu et al., "Wafer Bonding Technology and its Applications in Optoelectronic Devices and Materials," IEEE Journal of Selected Topics in Quantum Electronics, vol. 3, No. 3, Jun. 1997 pp. 927-936.	

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
--------------------	------------------	-----------------	------------

\***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 22 OF 22	Attorney Docket No.	TSSRA.012C1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	459	Zucker et al., "Application of Oxygen Plasma Processing to Silicon Direct Bonding", Sensors and Actuators A, 36 (1993), pp. 227-231.	
	460	Stefan Bengtsson et al., Journal of Electronic Materials, vol. 29, No. 7, "Room Temperature Wafer Bonding Of Silicon Oxidized Silicon, and Crystalline Quartz," 2000, pp. 909-915.	
	461	PLOSSL et al., "Wafer direct bonding: Tailoring adhesion between brittle materials," Materials Science & Engineering, March 10, 1999, Vol. R 25, Nos. 1-1, pp. 1-88.	
	462	TAKAGI et al, "Low temperature direct bonding of silicon and silicon dioxide by the surface activation method," Transducers 1997, 1997 Int. Conf. on Solid State Sensors and Actuators, Jun. 16-19, 1997, pp. 657-660.	Abstract
	463	TAKAGI et al., "Wafer-scale room-temperature bonding between silicon and ceramic wafers by means of argon-beam surface activation," 2001, IEEE, p. 60-63.	
	464	Ziptronix, Inc. v. Omnivision Technologies, Complaint for Patent Infringement, Case 4:10-cv-05525-SBA, Document 48, filed May 4, 2011, pp. 1-29.	
	465	Ziptronix, Inc. v. Omnivision Technologies, Defendant TSMC's Answer and Affirmative Defenses to Ziptronix First Amended Complaint, Case No. 4:10-cv-05525-SBA, Document 49, filed May 4, 2011, pp. 1-45.	
	466	Ziptronix, Inc. v. Omnivision Technologies, Complaint for Patent Infringement, Case No. 4:10-cv-05525-SBA Document 1, filed December 16, 2010, pp. 1-17.	

22453282  
021616

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	Application No.	14/957,501
	Filing Date	December 2, 2015
	First Named Inventor	Tong et al.
	Art Unit	2895
(Multiple sheets used when necessary)	Examiner	Joannie A. Garcia
SHEET 1 OF 1	Attorney Docket No.	TSSRA.012C1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>


NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
	1	AMIRFEIZ et al., "Formation of silicon structures by plasma activated wafer bonding," Vol. 99-2, Abstract No. 963, 1999 Joint Int'l Meeting of the Electrochem. Soc'y, December 16, 1999.	
	2	AMIRFEIZ et al., "Formation of silicon structures by plasma activated wafer bonding," Electrochemical Society Proceedings: Semiconductor Wafer Bonding: Science, Technology, and Applications V, Volume 99-35, (1999), pp. 29-39.	
	3	Ziptronix, Inc. v. Omnivision Technologies, Inc., Defendants' Third Supplemental Consolidated Invalidity Contentions Under Patent Local Rule 3-3, Case No. 4:10-cv-05525-SBA, dated June 14, 2013, pp. 1-5379, (submitted in multiple parts).	

22889096  
031116

Examiner Signature	/Joannie Garcia/	Date Considered	05/11/2016
<b>*Examiner:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE BY SAMSUNG EXHIBIT 1002


Samsung v. Invenssas Bonding

<b>Issue Classification</b> 	<b>Application/Control No.</b> 14957501	<b>Applicant(s)/Patent Under Reexamination</b> TONG ET AL.	
	<b>Examiner</b> JOANNIE A GARCIA	<b>Art Unit</b> 2895	

CPC					
Symbol				Type	Version
H01L	29	/	16	F	2013-01-01
Y10T	156	/	1043	A	2015-01-15
Y10T	156	/	10	A	2015-01-15
H01L	21	/	0206	I	2013-01-01
H01L	21	/	2007	I	2013-01-01
H01L	21	/	31105	I	2013-01-01
H01L	21	/	31116	I	2013-01-01
H01L	21	/	76251	I	2013-01-01
H01L	24	/	26	I	2013-01-01
H01L	24	/	83	I	2013-01-01
H01L	2224	/	8319	A	2013-01-01
H01L	2224	/	8385	A	2013-01-01
H01L	2224	/	83894	A	2013-01-01
H01L	2924	/	01005	A	2013-01-01
H01L	2924	/	01013	A	2013-01-01
H01L	2924	/	01018	A	2013-01-01
H01L	2924	/	01033	A	2013-01-01
H01L	2924	/	01039	A	2013-01-01
H01L	2924	/	0106	A	2013-01-01
H01L	2924	/	01061	A	2013-01-01
H01L	2924	/	01074	A	2013-01-01
H01L	2924	/	01075	A	2013-01-01
H01L	2924	/	01093	A	2013-01-01
H01L	2924	/	07802	A	2013-01-01
H01L	2924	/	10329	A	2013-01-01
H01L	2924	/	14	A	2013-01-01
H01L	24	/	75	I	2013-01-01
H01L	2924	/	01006	A	2013-01-01
H01L	2924	/	0102	A	2013-01-01
H01L	2924	/	01023	A	2013-01-01
H01L	2924	/	01072	A	2013-01-01

/JOANNIE A GARCIA/ Examiner.Art Unit 2895  (Assistant Examiner)	05/11/2016  (Date)	<b>Total Claims Allowed:</b>  33	
/JOHN P DULKA/ Primary Examiner.Art Unit 2895  (Primary Examiner)	05/13/2016  (Date)	O.G. Print Claim(s)  1	O.G. Print Figure  4A-4E




<b>Issue Classification</b> 	<b>Application/Control No.</b> 14957501	<b>Applicant(s)/Patent Under Reexamination</b> TONG ET AL.	
	<b>Examiner</b> JOANNIE A GARCIA	<b>Art Unit</b> 2895	

H01L	2924	/	01084	A	2013-01-01
H01L	2924	/	0132	A	2013-01-01
Y10S	148	/	012	A	2013-01-01
Y10S	438	/	974	A	2013-01-01
H01L	29	/	06	I	2013-01-01
H01L	21	/	322	I	2013-01-01
H01L	27	/	085	I	2013-01-01
H01L	2224	/	8301	A	2013-01-01
H01L	2224	/	8303	A	2013-01-01
H01L	2224	/	8309	A	2013-01-01
H01L	2224	/	83099	A	2013-01-01
H01L	2224	/	83896	A	2013-01-01
H01L	2224	/	83948	A	2013-01-01
H01L	2924	/	01007	A	2013-01-01
H01L	2924	/	10253	A	2013-01-01

CPC Combination Sets							
Symbol				Type	Set	Ranking	Version
H01L	2924	/	0132	A	1	1	2013-01-01
H01L	2924	/	01006	A	1	2	2013-01-01
H01L	2924	/	01014	A	1	3	2013-01-01
H01L	2924	/	0132	A	2	1	2013-01-01
H01L	2924	/	01015	A	2	2	2013-01-01
H01L	2924	/	01049	A	2	3	2013-01-01
H01L	2924	/	0132	A	3	1	2013-01-01
H01L	2924	/	01031	A	3	2	2013-01-01
H01L	2924	/	01033	A	3	3	2013-01-01
H01L	2924	/	3512	A	4	1	2013-01-01
H01L	2924	/	00	A	4	2	2013-01-01

/JOANNIE A GARCIA/ Examiner.Art Unit 2895  (Assistant Examiner)	05/11/2016  (Date)	<b>Total Claims Allowed:</b>  33	
/JOHN P DULKA/ Primary Examiner.Art Unit 2895  (Primary Examiner)	05/13/2016  (Date)	O.G. Print Claim(s)  1	O.G. Print Figure  4A-4E



<b>Issue Classification</b> 	<b>Application/Control No.</b> 14957501	<b>Applicant(s)/Patent Under Reexamination</b> TONG ET AL.
	<b>Examiner</b> JOANNIE A GARCIA	<b>Art Unit</b> 2895

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant															
<input type="checkbox"/> CPA <input checked="" type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	16	17	32	33										
1	2	17	18	33	34										
2	3	18	19												
3	4	19	20												
4	5	20	21												
5	6	21	22												
6	7	22	23												
7	8	23	24												
8	9	24	25												
9	10	25	26												
10	11	26	27												
11	12	27	28												
12	13	28	29												
13	14	29	30												
14	15	30	31												
15	16	31	32												

/JOANNIE A GARCIA/ Examiner.Art Unit 2895  (Assistant Examiner)	05/11/2016  (Date)	<b>Total Claims Allowed:</b>  33	
/JOHN P DULKA/ Primary Examiner.Art Unit 2895  (Primary Examiner)	05/13/2016  (Date)	O.G. Print Claim(s)  1	O.G. Print Figure  4A-4E

## EAST Search History

## EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	480415	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:05
L2	59338	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:05
L3	880726	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:05
L4	143	L1 with L2 with L3	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:05
L5	25	L4 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:05
L8	5	((("4700466") or ("4983251") or ("5427638") or ("5451547") or ("4992149")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/05/11 20:09
S1	1	("20140203407").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:41
S2	1	("8153505").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:42
S3	1349	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room-temperature" or "room T" or "room-T")	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:47
S4	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") with ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:50
S5	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") same ("chemical bond" or "chemical-	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:50

		bond"))				
S6	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:51
S7	0	((bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:51
S8	436228	(bond\$.clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:53
S9	53191	(anneal\$.clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:53
S10	802974	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:54
S11	134	S8 with S9 with S10	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 09:54
S12	19293	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:07
S13	6	S11 and S12	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:09
S14	18	S11 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2014/10/17 10:50
S15	1386	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room-temperature" or "room T" or "room-T")	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S16	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") with ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S17	0	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-	US-PGPUB; USPAT;	OR	OFF	2015/07/22 15:54

		temperature" or "room T" or "room-T") same ("chemical bond" or "chemical-bond"))	USOCR			
S18	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S19	0	((bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S20	457036	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S21	56069	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S22	839493	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:54
S23	138	S20 with S21 with S22	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S24	19807	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S25	6	S23 and S24	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S26	20	S23 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2015/07/22 15:55
S27	465993	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S28	57339	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S29	855382	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT;	OR	OFF	2015/11/10 16:40

			USOCR			
S30	139	S27 with S28 with S29	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S31	21	S30 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:40
S32	1	("20150303263").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:41
S33	1	("5451547").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:41
S34	1286659	adhesive	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:41
S35	0	S33 and S34	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:41
S36	2043	terminated with species	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:45
S37	1	S32 and S36	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:45
S38	909961	etch\$	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:48
S39	1	S33 and S38	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:49
S40	5	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	OFF	2015/11/10 16:58
S41	28	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:58
S42	0	S33 and S41	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:58
S43	48227	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching)	US-PGPUB;	OR	ON	2015/11/10 16:58

			USPAT; USOCR			
S44	0	S33 and S43	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S45	2042101	bond or bonds or bonded or bonding	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S46	1	S33 and S45	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 16:59
S47	567781	CMP or polish\$ or planarize or planarizes or planarized or planarizing or planarization	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:04
S48	1	S33 and S47	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:04
S49	3009473	plasma or gas	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:09
S50	1	S33 and S49	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:09
S51	1	S39 and S46 and S48 and S50	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:10
S52	913511	etch\$ or VSE	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:49
S53	1	S33 and S52	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:49
S54	790750	specie	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:53
S55	0	S33 and S54	US- PGPUB; USPAT; USOCR	OR	ON	2015/11/10 17:54
S56	1	("5451547").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/11/14 10:09
S57	1	("20150303263").PN.	US- PGPUB; USPAT; USOCR	OR	OFF	2015/11/14 10:38




S58	85	"planarized insulating material"	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/14 10:43
S59	1	S57 and S58	US-PGPUB; USPAT; USOCR	OR	ON	2015/11/14 10:43
S60	472066	(bond\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
S61	58187	(anneal\$).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
S62	865929	(heat or heats or heated or heating).clm.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
S63	140	S60 with S61 with S62	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
S64	22	S63 AND ( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:29
S65	19956	((257/459) or (257/676) or (257/684) or (257/701) or (257/702) or (257/e21.088) or (257/e21.122) or (257/e21.215) or (257/e21.218) or (257/e21.219) or (257/e21.224) or (257/e21.24) or (257/e21.243) or (257/e21.245) or (257/e21.246) or (257/e21.249) or (257/e21.33) or (257/e21.567) or (257/e23.02) or (257/e23.04)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:45
S66	5551	((438/405) or (438/455) or (438/459) or (438/974) or (148/DIG12)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:51
S67	24326	S65 or S66	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:51
S68	1406	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with ("25" or "room temperature" or "room-temperature" or "room T" or "room-T")	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:52
S69	28	(bond or bonds or bonded or bonding) with (etch or etches or etched or etching) with (("25" or "room temperature" or "room-temperature" or "room T" or "room-T") and ("chemical bond" or "chemical-bond"))	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 18:53
S70	4	((("4700466") or ("4983251") or ("5427638") or ("5451547"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 18:58

S71	1	("20150303263").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 19:30
S72	86	"planarized insulating material"	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 19:30
S73	1	S71 and S72	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 19:30
S74	1352309	nitrogen	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 20:26
S75	0	S70 and S74	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 20:26
S76	1304100	adhesive	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 20:27
S77	1	S70 and S76	US-PGPUB; USPAT; USOCR	OR	ON	2016/01/25 20:27
S78	1	("8153505").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/01/25 21:14

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	8028	( (H01L21/324 OR H01L21/2022 OR H01L21/26506 OR H01L21/187 OR H01L21/2007 OR H01L21/76251 OR H01L23/38 OR H01L21/02032 OR H01L21/3065 OR H01L21/3226 OR H01L21/67092).CPC. )	USPAT	OR	OFF	2016/05/11 20:05
L7	12	L6 AND (bond\$ with anneal\$ with (heat or heats or heated or heating)).CLM.	USPAT	OR	OFF	2016/05/11 20:09
L9	5	((("4700466") or ("4983251") or ("5427638") or ("5451547") or ("4992149")).PN.	US-PGPUB; USPAT	OR	OFF	2016/05/11 20:09

5/ 11/ 2016 8:10:29 PM  
C:\ Users\ jgarcia1\ Documents\ EAST\ Workspaces\ 14957501.wsp

<b>Search Notes</b>  	<b>Application/Control No.</b>  14957501	<b>Applicant(s)/Patent Under Reexamination</b>  TONG ET AL.
	<b>Examiner</b>  JOANNIE A GARCIA	<b>Art Unit</b>  2895

CPC- SEARCHED		
Symbol	Date	Examiner
H01L: 21/02032,21/185,21/187,21/2007,21/2022,21/26506,21/30,21/302,21/306,21/3065,21/3226,21/324,21/38,21/46,21/461,21/67092,21/76251,21/76254	05/11/2016	JAG

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
438	405,455,459,974,FOR103,FOR127,FOR388,FOR395	05/11/2016	JAG
257	459,676,684,701,702,E21.088,E21.122,E21.215,E21.218,E21.219,E21.224,E21.243,E21.245,E21.249,E21.33,E23.02,E23.04	05/11/2016	JAG
148	DIG12	05/11/2016	JAG

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	05/11/2016	JAG
Consulted Primary Examiner John P. Dulka	05/11/2016	JAG

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L	21/02032,21/185,21/187,21/2007,21/2022,21/26506,21/30,21/302,21/306,21/3065,21/3226,21/324,21/38,21/46,21/461,21/67092,21/76251,21/76254	05/11/2016	JAG

/JOANNIE A GARCIA/  
Examiner, Art Unit 2895

## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, Virginia 22313-1450**  
**or Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

135980 7590 05/24/2016  
**Knobbe, Martens, Olson**  
**& Bear, LLP**  
**2040 main Street**  
**Fourteenth Floor**  
**Irvine, CA 92614**

## Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/957,501	12/02/2015	Qin-Yi Tong	TSSRA.012C1	1033

TITLE OF INVENTION: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/24/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
GARCIA, JOANNIE A	2895	257-684000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Knobbe, Martens,  
 2 Olson & Bear LLP  
 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

**ZIPTRONIX, INC.**

**Morrisville, NC**

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 11-1410 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Paul Stellman/

Date May 25, 2016

Typed or printed name Paul Stellman

Registration No. 68,287

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor	:	Tong et al.
App. No.	:	14/957,501
Filed	:	December 2, 2015
For	:	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
Examiner	:	Joannie A. Garcia
Art Unit	:	2895
Conf. No.	:	1033

**COMMENTS ON REASONS FOR ALLOWANCE****Mail Stop AF**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Applicants note that the Reasons for Allowance stated in the Notice of Allowance mailed May 24, 2016, pursuant to MPEP 1302.14, are not intended to necessarily state all the reasons for allowance or all the details why the claims are allowed, and therefore does not specifically or impliedly state that all the reasons for allowance are set forth. Furthermore, the fact that Applicants have not specifically commented on the Examiner's characterizations of the reasons for allowance in the Statement of Reasons for Allowance shall not be taken as an acknowledgement of the accuracy of such characterizations. Accordingly, Applicants submit that the allowed claims may be allowable for reasons other than those stated in the Statement for Reasons for Allowance and that Applicants are not bound by the reasons for allowance provided therein.

**Application No.:** 14/957,501  
**Filing Date:** December 2, 2015

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: May 25, 2016

By: /Paul Stellman/

Paul Stellman

Registration No. 68,287

Attorney of Record

Customer No. 20,995

(415) 954-4114

23409915  
052516

## Electronic Patent Application Fee Transmittal

<b>Application Number:</b>	14957501			
<b>Filing Date:</b>	02-Dec-2015			
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE			
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong			
<b>Filer:</b>	Paul Steven Stellman/Jonathan Pan			
<b>Attorney Docket Number:</b>	TSSRA.012C1			
Filed as Large Entity				
<b>Filing Fees for    Utility under 35 USC 111(a)</b>				
<b>Description</b>	<b>Fee Code</b>	<b>Quantity</b>	<b>Amount</b>	<b>Sub-Total in USD(\$)</b>
<b>Basic Filing:</b>				
<b>Pages:</b>				
<b>Claims:</b>				
<b>Miscellaneous-Filing:</b>				
<b>Petition:</b>				
<b>Patent-Appeals-and-Interference:</b>				
<b>Post-Allowance-and-Post-Issuance:</b>				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
<b>Extension-of-Time:</b>				
<b>Miscellaneous:</b>				
<b>Total in USD (\$)</b>				<b>960</b>



## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	25885232
<b>Application Number:</b>	14957501
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1033
<b>Title of Invention:</b>	METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE
<b>First Named Inventor/Applicant Name:</b>	Qin-Yi Tong
<b>Customer Number:</b>	135980
<b>Filer:</b>	Paul Steven Stellman/Chelsea Burdeno
<b>Filer Authorized By:</b>	Paul Steven Stellman
<b>Attorney Docket Number:</b>	TSSRA.012C1
<b>Receipt Date:</b>	25-MAY-2016
<b>Filing Date:</b>	02-DEC-2015
<b>Time Stamp:</b>	17:33:10
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	4321
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

<b>File Listing:</b>					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2016-05-25_IssueFeeTransmittal_TSSRA-012C1.pdf	84957	no	1
			743507b930368d6840e71e29659b6380fe8a23a8		
<b>Warnings:</b>					
<b>Information:</b>					
2	Miscellaneous Incoming Letter	2016-05-25_Comments_TSSRA-012C1.pdf	71533	no	2
			477fc556dfce772e5603a393e2bfc687e8966ad6		
<b>Warnings:</b>					
<b>Information:</b>					
3	Fee Worksheet (SB06)	fee-info.pdf	30804	no	2
			2914d1c6c0d97c24513dc52d998a980af6ac8e16		
<b>Warnings:</b>					
<b>Information:</b>					
<b>Total Files Size (in bytes):</b>			187294		
<p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b>  If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b>  If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b>  If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/957,501	12/02/2015	2895	3200	TSSRA.012C1	33	4

CONFIRMATION NO. 1033  
CORRECTED FILING RECEIPT



135980  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

Date Mailed: 06/09/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Qin-Yi Tong, Durham, NC, Deceased;  
Gaius Gillman Fountain JR., Youngsville, NC;  
Paul M. Enquist, Cary, NC;

**Applicant(s)**

ZIPTRONIX, INC., Morrisville, NC;

**Power of Attorney:** The patent practitioners associated with Customer Number 135980

**Domestic Priority data as claimed by applicant**

This application is a CON of 14/754,111 06/29/2015 PAT 9331149  
which is a DIV of 14/197,070 03/04/2014 PAT 9082627  
which is a DIV of 13/341,273 12/30/2011 ABN  
which is a CON of 12/954,740 11/26/2010 PAT 8153505  
which is a CON of 12/720,368 03/09/2010 PAT 7871898  
which is a CON of 11/980,664 10/31/2007 PAT 7807549  
which is a CON of 10/913,441 08/09/2004 PAT 7387944  
which is a CON of 09/505,283 02/16/2000 PAT 6902987

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

**Permission to Access Application via Priority Document Exchange:** Yes

**Permission to Access Search Results: Yes**

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted: 12/11/2015**

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/957,501**

**Projected Publication Date:** Not Applicable

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE

**Preliminary Class**

257

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No**

**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

**LICENSE FOR FOREIGN FILING UNDER**  
**Title 35, United States Code, Section 184**  
**Title 37, Code of Federal Regulations, 5.11 & 5.15**

**GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

---

***SelectUSA***

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/957,501	07/12/2016	9391143	TSSRA.012C1	1033

135980 7590 06/22/2016  
Knobbe, Martens, Olson  
& Bear, LLP  
2040 main Street  
Fourteenth Floor  
Irvine, CA 92614

## ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

### **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)** (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

ZIPTRONIX, INC., Morrisville, NC;  
Qin-Yi Tong, Durham, NC, Deceased;  
Gaius Gillman Fountain JR., Youngsville, NC;  
Paul M. Enquist, Cary, NC;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit [SelectUSA.gov](http://SelectUSA.gov).