

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.; AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner

v.

INVENSAS BONDING TECHNOLOGIES, INC.,
Patent Owner

Patent No. 9,391,143

**DECLARATION OF DR. CHARLES HUNT IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,391,143**

SAMSUNG EXHIBIT 1003

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1. I, Dr. Charles Hunt, declare as follows:

I. INTRODUCTION

2. I have been retained by Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”).

3. I have been asked to consider whether certain references teach or suggest the features recited in Claims 1, 3-4, 6, 14-15, 20-22, 24, and 29-33 of U.S. Patent No. 9,391,143 (“the ’143 Patent”) (Ex-1001).¹ My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my ordinary and customary consulting rate of \$400 per hour for my work. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

¹ Where appropriate, I refer to exhibits that I understand are attached to the petition for *Inter Partes* Review of the ’143 Patent.

II. BACKGROUND AND QUALIFICATIONS

5. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching the technology referenced in this declaration.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted as Ex-1004. The following provides a brief overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I am a Full, Tenured Professor in the Department of Electrical and Computer Engineering at the University of California - Davis, where I have been on the faculty since 1986. I teach a wide variety of classes at the undergraduate and graduate level covering electrical and computer engineering theory and practice, including electronic materials, analog and digital microelectronics, semiconductor device physics, photovoltaics and solar cells, and engineering ethics and professional practice. Many of these classes incorporate both lecture and laboratory experiences in conceptual and detailed design, implementation, and measurement.

8. Courses I have taught include topics such as materials science relevant to use in the micro and nano-electronics, as well as MEMS and photonic devices. Notably, this includes the theory and practice of semiconductor wafer bonding. I also teach about energy-efficient light sources, as well as sustainable energy production techniques, notably using solar energy. Bi-annually, I teach the Department's graduate class examining advanced semiconductor device research as reported in the latest literature. As a service to non-majors, I teach a laboratory-based class in analog and digital microelectronics, as well as the College's basic course in fundamentals of electric circuits (a class required of almost all engineering undergraduate students). I developed and have taught the Department's courses in integrated-circuit fabrication technology for many years. I developed and have taught the Department's bi-annual graduate course in nanofabrication theory and practice. I have organized and hosted the Department's annual graduate seminars, and have developed and taught the undergraduate required course in engineering professionalism and ethics of practice.

9. The structures and methods claimed in the '143 Patent generally relate to semiconductor wafer bonding technology.

10. With respect to semiconductor wafer bonding, I first became engaged in research using techniques relevant to this field in 1990, when I was searching for improved methods for fabrication of Silicon On Insulator (SOI). My dissertation

research was in new synthesis methods for SOI, and in 1990 there was a general need for substantial improvements in the SOI wafer material in order for commercial realization to proceed. For the ensuing decade, my research focus was on theoretical and experimental research associated with “Bond and Etch-back Silicon on Insulator (BESOI).” My Team at UC Davis became pioneers in this technique, resulting in publications and patents relevant to BESOI materials synthesis. This has become one of the techniques that is commercially employed in SOI, which is a standard commodity now in the high-speed, high-performance digital nanoelectronics industry. From 1991 until the 2005, I was Chair, or Co-Chair of the Electrochemical Society’s bi-annual Symposium on Semiconductor Wafer Bonding, which has continuously been the principal forum for research in this field.

11. Beyond research in wafer bonding, I have also served as a consultant to several companies and to Lawrence Livermore National Laboratory, specific to problem-solving engineering solutions using wafer bonding of multiple materials types, but predominantly using silicon and silicon-oxide bonding interfaces.

12. I have taught courses at the undergraduate and graduate level in electronic materials and solid-state fabrication technologies, incorporating wafer bonding, including the ancillary technique used in wafer bonding, as a core component within the curriculum.

13. As part of my faculty role at the University of California - Davis, I participate in the supervision of doctoral and masters-level research performed by graduate students as part of obtaining their degrees. Several of my advisees who have received their degrees, both M.S. and Ph.D., had as the central theme of their thesis one or more fabrication methods which were investigated for the improvement of wafer-bonding technology. These graduate students were either in the Electrical Engineering or the Engineering Materials Science at UC Davis, as well as one Ph.D. student in Applied Physics at the University of Barcelona.

14. Applications using the wafer-bonding techniques that were developed in the research within my Group at UC Davis have included Semiconductor on Insulator (SOI), microchannel coolers for heat dissipation from laser-diode arrays, Micro-Electro-Mechanical Systems (MEMS) for various uses, Atomic-Force Microscopy (AFM) cantilevers, backside imagers for ultraviolet radiation spectroscopy in large-scale astronomical telescopes, submicron membranes for use as debris shields and optical components in xray and near-xray lasers and aligners, and deep-well high-voltage or high-power discrete electronic devices.

15. Since obtaining my Ph.D. in 1986, I have actively consulted in industry and national laboratories in multiple areas of technology development, analysis, and assessment, directed to both product development, problem solving and analysis of intellectual property portfolios, patent infringement, and validity.

The fields of technology in which I have consulted and/or served as a technical expert, beyond wafer bonding, include non-electronic semiconductor microsystems, integrated-circuit fabrication technology in multiple aspects, electronic materials growth and etching, and column-IV semiconductor epitaxy. Companies and laboratories which I have worked for in these fields of expertise include Analog Devices, Applied Materials, Lawrence Semiconductor Research Laboratory, IBM, Lawrence Livermore National Laboratory, Lam Research, Motorola, Sandia National Laboratory, Hewlett Packard, Brucker XRAY, LightLab AB (Sweden), Argonne National Laboratory, IREC (Spain), Jins Optronics (Japan), Keck Observatories, and others.

16. I received a B.S. and M.S. in Electrical Engineering from the University of Utah in 1980 and 1983, respectively. I further received a Ph.D. in Electrical Engineering and Electronic Materials Science from Cornell University in 1986.

III. INFORMATION CONSIDERED

17. In preparation for this declaration, I have considered the materials discussed in this declaration, including, for example, the '143 Patent, the references cited by the '143 Patent, the prosecution history of the '143 Patent, various background articles and books referenced in this declaration, and the prior art references identified in this declaration. In addition, my opinions are further

based on my education, training, research, experience, and knowledge in the relevant field.

IV. RELEVANT LEGAL STANDARDS

18. I am not an attorney and offer no legal opinions. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis, as summarized below.

A. Claim Interpretation

19. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board.

20. To resolve the grounds addressed below, I do not believe any term requires construction, and the terms should be interpreted according to their ordinary and customary meaning.

B. Perspective of One of Ordinary Skill in the Art

21. I have been informed and understand that a patent is to be understood from the perspective of a hypothetical “person of ordinary skill in the art” (“POSITA”). Such an individual is considered to possess normal skills and knowledge in a particular technical field (as opposed to being a genius). I understand that in considering what the claims of a patent require, what was known prior to that patent, what a prior art reference discloses, and whether an invention

is obvious or not, one must use the perspective of such a person of ordinary skill in the art.

C. Obviousness

22. I have been informed and understand that a patent claim is obvious under 35 U.S.C. § 103, and therefore invalid, if the claimed subject matter, as a whole, would have been obvious to a person of ordinary skill in the art as of the priority date of the patent based on one or more prior art references and/or the knowledge of one of ordinary skill in the art.

23. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

24. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a person of ordinary skill in the art, and that this knowledge may be used to combine multiple references. I further understand that a person of ordinary skill in the art is presumed to know the relevant prior art. I understand that the obviousness analysis

may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

25. In determining whether a prior art reference would have been combined with other prior art or other information known to a person of ordinary skill in the art, I understand that the following principles may be considered:

- a. whether the references to be combined involve non-analogous art;
- b. whether the references to be combined are in different fields of endeavor than the alleged invention in the Patent;
- c. whether the references to be combined are reasonably pertinent to the problems to which the inventions of the Patent are directed;
- d. whether the combination is of familiar elements according to known methods that yields predictable results;
- e. whether a combination involves the substitution of one known element for another that yields predictable results;
- f. whether the combination involves the use of a known technique to improve similar items or methods in the same way that yields predictable results;
- g. whether the combination involves the application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

- h. whether the combination is “obvious to try”;
- i. whether the combination involves the known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces, where the variations are predictable to a person of ordinary skill in the art;
- j. whether there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention;
- k. whether the combination requires modifications that render the prior art unsatisfactory for its intended use;
- l. whether the combination requires modifications that change the principle of operation of the reference;
- m. whether the combination is reasonably expected to be a success; and
- n. whether the combination possesses the requisite degree of predictability at the time the invention was made.

26. I understand that in determining whether a combination of prior art references renders a claim obvious, it is helpful to consider whether there is some teaching, suggestion, or motivation to combine the references and a reasonable

expectation of success in doing so. I understand, however, that a teaching, suggestion, or motivation to combine is not required.

V. LEVEL OF ORDINARY SKILL IN THE ART

27. I am familiar with the level of ordinary skill in the art with respect to the '143 Patent around its filing date. Based on my experience working, teaching, and conducting research in the relevant field, and based on my review of the '143 Patent specification, claims, file history, and prior art, I believe one of ordinary skill in the art around the time of the alleged invention of the '143 Patent would have had a master's degree in electrical engineering, materials science, chemistry, or physics, focusing on semiconductor processes as applied to bonding structures; a bachelor's degree in electrical engineering, materials science, chemistry, or physics and 3-5 years of experience in semiconductor bonding technology; or equivalent degree and an equivalent amount of relevant work or research experience. Additional education could substitute for work experience and vice versa.

28. In determining the level of ordinary skill in the art, I considered, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

29. My opinions concerning the '143 Patent claims and the prior art are from the perspective of a person of ordinary skill in the art ("POSITA"), as set forth above.

VI. SUMMARY OF MY OPINIONS

30. I have been asked to consider whether Claims 1, 3-4, 6, 14-15, 20-22, 24, and 29-33 of the '143 Patent are obvious over certain prior art references. As explained below in detail in this declaration, it is my opinion that:

(1) Claims 1, 3-4, 6, 14-15, 21-22, 24, and 29-33 of the '143 Patent are obvious over Y. Li et al., *Systematic Low Temperature Silicon Bonding Using Pressure and Temperature*, 1998 Jpn. J. Appl. Phys. 37 (1998) ("Li") and M. Reiche et al., *The Effect of a Plasma Pretreatment on the Si/Si Bonding Behaviour*, 97-36 Electrochemical Society Proceedings 437 (1997) ("Reiche"); and

(2) Claims 1, 3-4, 6, 14-15, 20-22, 24, and 29-33 of the '143 Patent are obvious over Li, Reiche, and U.S. Patent No. 5,503,704 ("Bower").

VII. OVERVIEW OF TECHNOLOGY AS OF FILING DATE

31. The '143 Patent is directed to well-known semiconductor wafer bonding technology, particularly "activating" and "terminating" a bonding surface.

32. To provide background for the element-by-element analysis of the claims to follow, below I will present an overview of the state of the art existing as

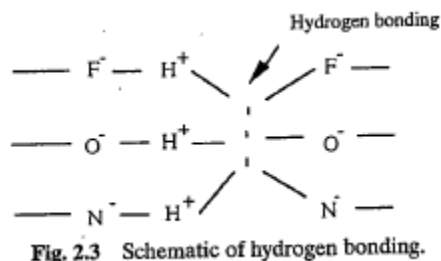
of the time of the alleged invention relating to semiconductor wafer bonding technology. As I will describe below, all of these technologies and techniques were well known to those of ordinary skill in the art at the time of the alleged invention claimed in the '143 Patent, and a person of ordinary skill in the art would have readily understood the combination of elements of the claims to have been obvious.

33. “Wafer bonding” or “direct bonding” generally refers to the process in which two mirror-polished, flat, and clean wafers of almost any material are brought into direct contact, and adhere or “bond” to each other. *See, e.g.,* Q. Tong et al., *Semiconductor Wafer Bonding: Science and Technology*, John Wiley & Sons, Inc. (1999) (Ex-1008), 1, 17-31, 49-101, 103-35. Based on difficulties encountered in the late-1980s, “wafer bonding was characterized as ‘black magic’ and as a technology that is not easily manufacturable.” *Id.*, 6. However, over the decade leading up to the filing of the '143 Patent, “the science behind wafer bonding has been investigated thoroughly and most of the difficulties associated with silicon wafer bonding have been ironed out, so that little if any black magic remains.” *Id.*

34. Wafer bonding is commonly applied to semiconductor wafers used in microelectronics, such as silicon. *Id.*, 1. These applications generally require post-bonding processing, such as thinning, etching, and/or polishing. *Id.*, 1-15, 137-73,

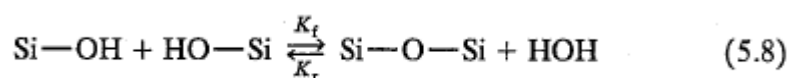
203-21, 223-88. If bonds of adequate strengths are not obtained, then the bonded wafers will not be able to withstand such processing. *Id.* Thus, obtaining strong bonds is a requisite goal of wafer bonding. *Id.*, *passim*. The initial adhesion between the two surfaces, however, is generally a result of van der Waals forces and hydrogen bonding, and is relatively weak compared to solids bonded by chemical (*e.g.*, covalent) bonds. *Id.*, 1, 17-31, 49-101, 103-35. Thus, bonded wafers generally have to undergo a heat treatment to strengthen the bonds across the interface—that is to convert the van der Waals forces and hydrogen bonds to covalent bonds. *Id.*, 1, 103-35.

35. Van der Waals forces and hydrogen bonds depend on an extremely short-range attraction between surfaces and thus strongly decrease as the distance between two molecules increases. *Id.*, 17-20. Hydrogen bonding occurs when the hydrogen atom in a polar molecule interacts with an electronegative atom of either an adjacent molecule or the same molecule. *Id.*, 20, 57-59. A hydrogen atom can participate in a hydrogen bond if it is bonded to oxygen, nitrogen, or fluorine because H-F, H-O, and H-N bonds are strongly polarized, leaving the hydrogen atom with a partial positive charge. *Id.* As shown in Figure 2.3 below, this electrophilic hydrogen has a strong affinity for nonbonding electrons so that it can form intermolecular attachments with an electronegative atom such as oxygen, nitrogen, or fluorine. *Id.*, 20, 57-59, Fig. 2.3.



Water is a polarized molecule consisting of hydrogen as well as oxygen, which allows hydrogen bonding to form between water molecules themselves. *Id.*, 20, 57-59. Therefore, if water is present, the linkage of water molecules may bridge two interacting atoms or molecules. *Id.*

36. Covalent bonds, on the other hand, are chemical bonds that involve the sharing of electrons between atoms, which results in a stable balance of attractive and repulsive forces between the atoms. *Id.*, 1-15, 57-67, 80-87, 103-35, 215-21. Hydrogen bonds can convert to covalent bonds if the elements or molecules they are associated with are in close enough proximity. *Id.* Heat treatments (“anneals” or “annealing”) may also be used to convert hydrogen-bonded interfaces to covalent-bonded interfaces. *Id.* For example, as shown below in Reaction (5.8), hydrogen bonding between silanol bonds on opposite surfaces are transformed into covalent siloxane bonds provided that the interface molecular water can be removed:



Id., 1-15, 57-67, 80-87, 103-135, 215-221, Reaction (5.8). Molecular water can desorb or diffuse from wafer surfaces at above 110°C. *Id.* These conversions are illustrated in Figures 5.8 and 5.9, shown below. *Id.*, Figs. 5.8, 5.9.

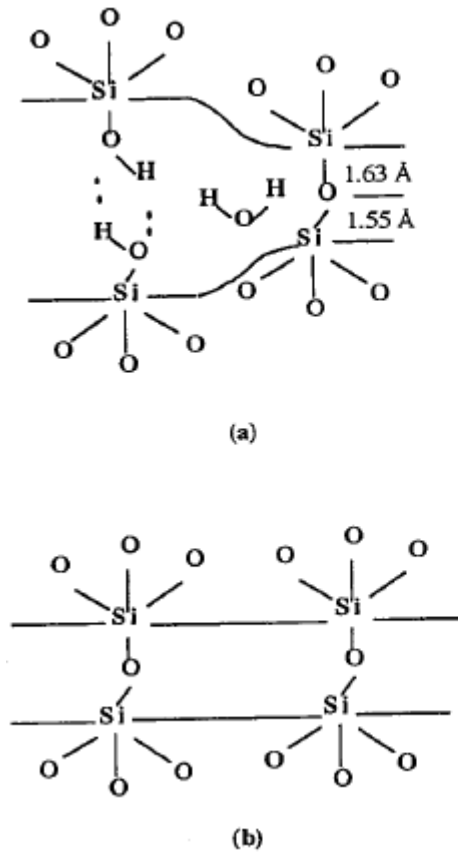


Fig. 5.8 Proposed chemical structure of hydrophilic Si/Si, Si/SiO₂, and SiO₂/SiO₂ pairs during and after annealing at 150–800°C for a sufficiently long time. Only isolated silanol groups are shown: (a) during annealing; (b) after long annealing.

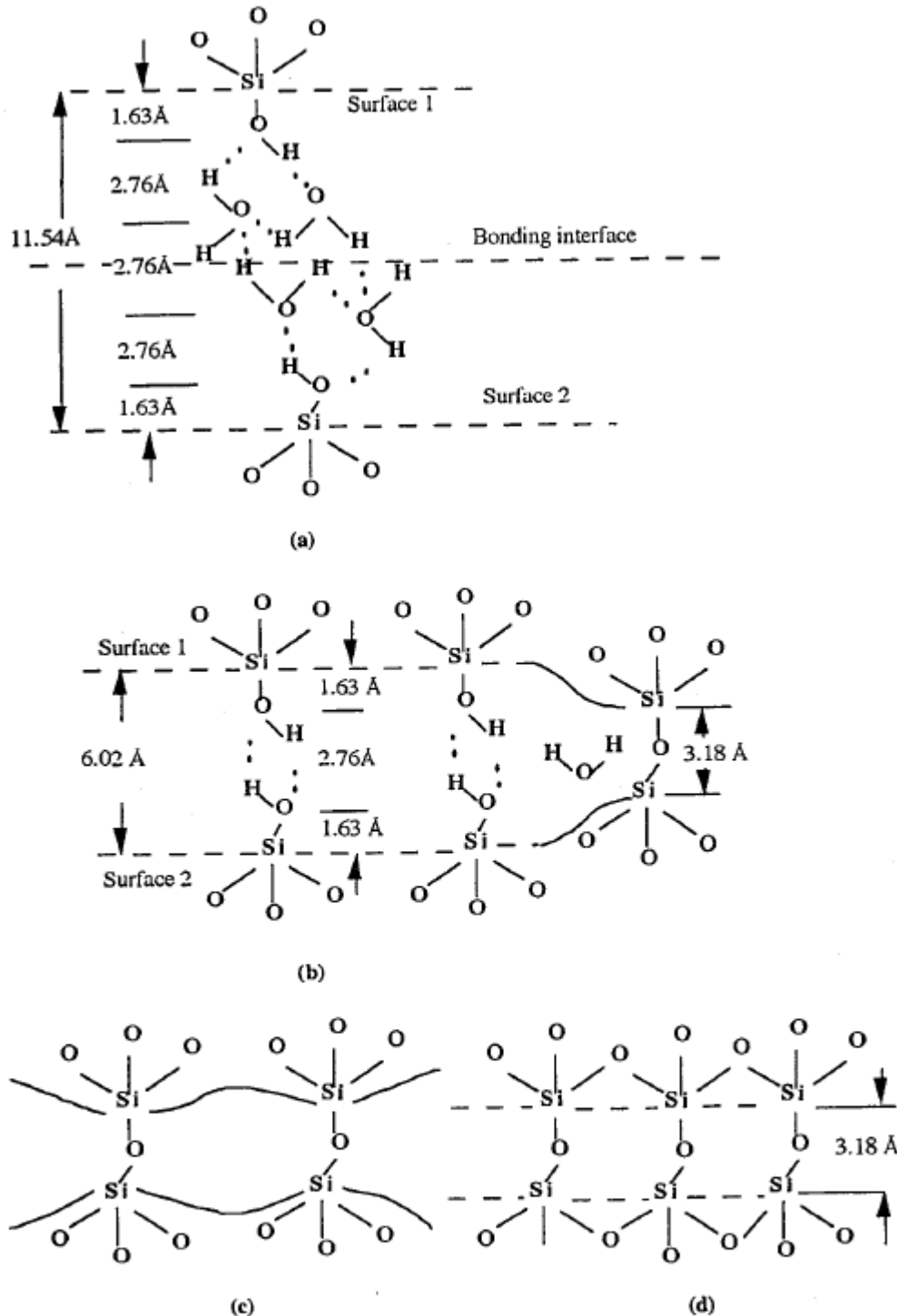


Fig. 5.9 Proposed bonding model for hydrophilic Si wafer bonding at different temperatures. (a) Room temperature-110°C: formation of stable hydrogen bonding between molecular water across the bonding interface. (b) 110-150°C: removal of interface molecular water and formation of siloxane bonds. (c) 150-800°C: stable siloxane bonds. (d) > 800°C: viscous flow of interface oxide (> 800°C for Si/Si, > 1000°C for Si/SiO₂ and SiO₂/SiO₂ pairs).

37. Based on this understanding of wafer bonding mechanics, it was well-understood that adequate surface smoothness, cleanliness, and reactivity are essential for successful wafer bonding. *Id.*, 49. A smooth bonding surface is critical because direct wafer bonding depends on an extremely short-range attraction between surfaces. *Id.*, 1-15, 17-31, 33-67, 80-87. If the wafer surfaces are not smooth—that is, if they have microscopic peaks and valleys—the surfaces will only bond where they are close together (*i.e.*, peak-to-peak), and they will not bond where they are far apart (*i.e.*, valley-to-valley). *Id.* Thus, the surface smoothness of bonding surfaces enables the attraction and bonding forces necessary for wafer bonding. *Id.* Since only molecules that are in sufficient proximity can form bonds between each other, surface roughness will limit the number of bonds and thus the strength of the bond between the two surfaces. *Id.* Similarly, wafer bonding requires clean surfaces, free of particles and contaminations, as these materials prevent bonding and lead to unbonded areas. *Id.*, 1-15, 17-31, 33-56. However, some cleaning techniques were known to roughen the bonding surfaces, thus it was understood that appropriate techniques must be able to remove all contamination from the surface while maintaining an adequate surface smoothness. *Id.*

38. Surface “activation” makes a surface more “reactive” for bonding purposes by increasing the number of bonding sites between the surfaces and/or

increasing the surface molecules' tendency to form bonds. *Id.*, 1-15, 49-67, 80-87, 103-23, 203-21. Increasing the surface reactivity thus increases the strength of the bond between the two surfaces. *Id.*

39. A silicon atom forms a crystal lattice by bonding with each of its four nearest-neighbor silicon atoms. *Id.* At the surface of a silicon layer, it is not possible for silicon atoms to form a complete crystal lattice and satisfy all four of its bonds because atoms on the surface do not have enough silicon neighbors to satisfy all of their normal bonds. *Id.* Therefore, the silicon surface is left with unsatisfied or "dangling" bonds, which may be satisfied when an atom or molecule attaches to the bonds. *Id.* Surface activation involves increasing the number of these dangling bonds. *Id.* Etching and some plasma processes may be used to activate a surface since these processes attack bonds in the surface material and/or dislodge surface atoms, thus increasing the number of dangling bonds. *Id.*

40. After a surface has been activated, the resulting dangling bonds may be "terminated" with a desired atom or molecule, which forms a temporary bond until the surface is brought together with another surface for permanent bonding. *Id.* Surface termination can be achieved by subjecting the wafer to various surface treatments. *Id.* For example, wafers may be immersed in a solution or exposed to a plasma from which certain atoms or molecules will attach to the dangling bonds. *Id.* However, similar to cleaning techniques, such activation techniques were

known to sometimes roughen the bonding surfaces, thus it was understood that appropriate techniques must be able to activate the surface while maintaining an adequate surface smoothness. *Id.*, 53-55, 62-65, 66-67; *see also id.*, 1-15, 49-67, 80-87, 103-23, 203-21.

41. Different atoms or molecules used to terminate a surface result in different chemical reactions, different reaction by-products, and different types of wafer bonds. *Id.* For example, Reaction 5.8, discussed above and illustrated in Figures 5.8 and 5.9 above, describes OH-terminated silicon wafers forming Si-O-Si covalent bonds with water as a by-product. *Id.* Examples of different solutions to which wafers may be exposed to terminate the surface before bonding, and the resulting bonding reactions, are outlined below in Table 4.6. *Id.*, Table 4.6.

TABLE 4.6 Some Chemicals for SiO₂ Surface Hydrophilization and the Products of the Reactions

	Chemicals	Reaction Products
Si—O—Si +	H ₂ O	Si—OH + HO—Si
	NH ₄ OH	Si—NH ₂ + HO—Si
	HNO ₃	Si—NO ₃ + H—Si + HO—Si
	H ₂ SO ₄	Si—SO ₄ + H—Si + HO—Si
	CH ₃ OH	Si—OCH ₃ + HO—Si
	(CH ₃) ₂ NH	Si—N(CH ₃) ₂ + HO—Si
	CH ₃ NH ₂	Si—NHCH ₃ + HO—Si

It was well-understood prior to the claimed invention that hydrogen bonds form most easily with F, O, and N, and, as a result, dangling bonds terminated with molecules comprising these atoms yield reactive surfaces. *Id.*, 1-15, 49-67, 80-87, 103-23, 203-21, Table 4.6. Thus, as illustrated in Table 4.6, it was well-known

that terminating solutions should comprise H in combination with F, O, and/or N.

Id.

42. It was also understood that exposure to certain chemical solutions would result in dangling bonds on the same surface terminated by different atoms or molecules. *Id.* For example, wafers immersed in dilute aqueous HF “are mainly terminated by H, but a significant amount” of Si-F bonds are also found. *Id.*, 63; *see also id.*, 1-15, 49-67, 80-87, 103-23, 203-21. Thus, the “bondability of HF-dipped Si wafers is most likely correlated to the presence of Si-F bonds.” *Id.* Similarly, in addition to terminating with H and/or OH, NH₃ chemical solutions can form Si-NH₂ and/or Si-NH groups for hydrogen bonding. *Id.*, 62, 66, 122-23, 217-19; *see also id.*, 1-15, 49-67, 80-87, 103-23, 203-21.

43. As discussed above, it was well-understood that by-products of these bonding reactions desorb from wafer surfaces at certain temperatures. *Id.*, 1-15, 49-67, 80-101, 103-135, 203-221. For example, molecular water can desorb from wafer surfaces at above 110°C, and at 150-800°C, silanol groups convert to siloxane bonds. *Id.* Thus, after bonding, wafers generally undergo an “annealing” heat treatment to strengthen the bonds across the interface. *Id.*

44. These understandings led to the basic wafer bonding method, where surfaces are prepared to be sufficiently smooth, clean, reactive, and terminated, room-temperature bonded, annealed, and then post-bond processed (*e.g.*, thinned,

etched, or polished). *Id.*, 1-15, 49-67, 80-87, 103-23, 203-21. Figure 1.2 below illustrates this “generic process flow.” *Id.*, 1, Fig. 1.2. However, “[m]odifications of this process flow are quite common for specific applications, (for example, no heating ... step may be involved).” *Id.*, 1.

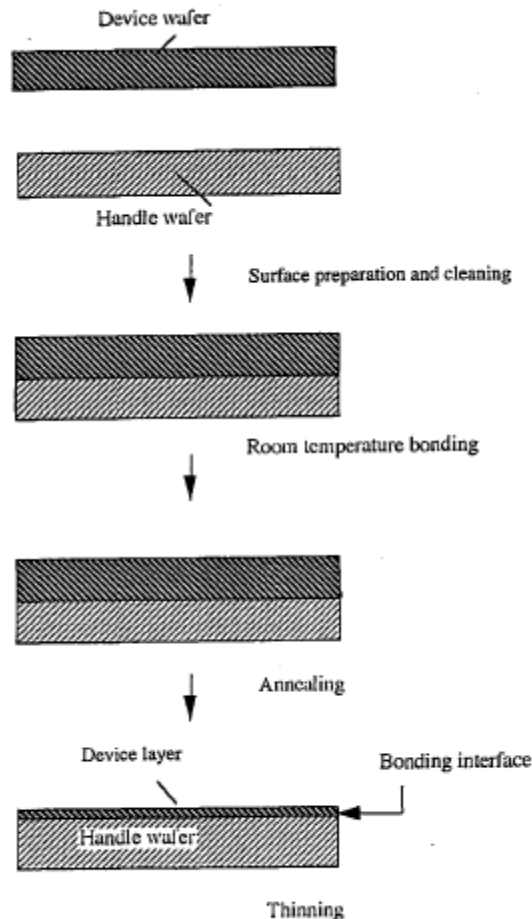


Fig. 1.2 Schematic of wafer-bonding process flow.

45. Because to-be-bonded wafers often comprise temperature-sensitive structures, it was a known goal of wafer bonding to achieve adequate bond strengths employing low-temperature bonding techniques. *Id.*, 1-15, 49-87, 103-23, 203-88. Thus, prior to the claimed invention, techniques were developed to

increase bond strengths without high-temperature anneals via maximizing a surface's reactivity while maintaining adequate smoothness. *Id.*, 1-15, 49-67, 80-87, 103-23, 203-21.

VIII. THE '143 PATENT

46. The '143 Patent discloses a “method for bonding at low or room temperature,” “based on etching and chemical bonding,” that can be used to “achieve high bonding strength adequate for subsequent fabrication and/or a desired application.” Ex-1001, Abstract, 1:26-31, 2:30-31. Figure 1 below “is a flow chart of the method according to the invention.” *Id.*, 4:50-51, Fig. 1. The method comprises five steps: (1) forming a bonding layer on a wafer or material; (2) smoothing and planarizing the bonding layer; (3) slightly etching the bonding layer to activate the surface; (4) terminating the bonding surface with a desired chemical species; and (5) bonding the surface to another. *Id.*

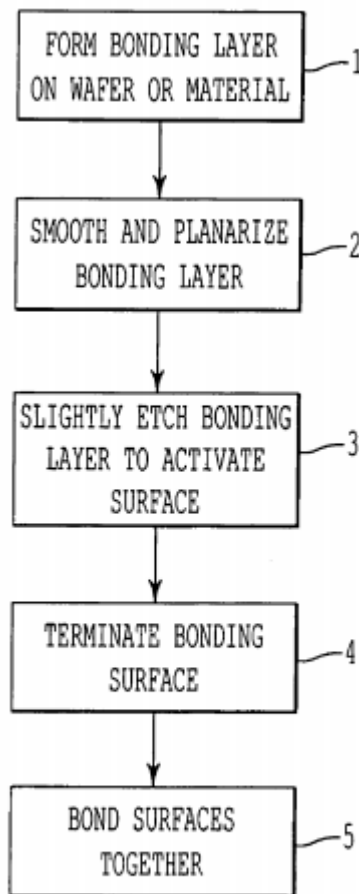


FIG. 1

47. In step 1, the '143 Patent discloses forming “bonding layer 32,” which “may be an insulator, such as SiO₂, silicon nitride, [or] silicon,” or “[o]ther materials such as ... semiconductors ... may also be used.” *Id.*, 5:23-27. However, a “planar wafer may not need to be coated with a bonding layer if it has sufficient smoothness and planarity and the proper bonding material.” *Id.*, 10:11-14.

48. In step 2, the “surface 33 of layer 32 is planarized and smoothed” “to a high degree of smoothness and planarity.” *Id.*, Abstract, 5:30-31. The ’143 Patent discloses that “surface 33” “is preferably polished to a roughness of about no more than about 3 nm and preferably no more than about 0.1 nm” and that this “step may be accomplished using chemical-mechanical polishing.” *Id.*, 5:33-40.

49. In step 3, “[s]urface 34 ... undergoes an activation process”— “[t]his activation process is an etching process and preferably a very slight etch (VSE) process.” *Id.*, 5:54-57. In the preferred VSE process, “the root-mean-square micro-roughness (RMS) [surface roughness] of the very slightly etched surface remains at approximately the unetched value, typically <0.5 nm and preferably in the range of 0.1 nm to 3 nm.” *Id.*, 5:57-61. Thus, the “VSE process etches the surface very slightly ... and preferably is controlled to not degrade the surface roughness of the bonding surfaces.” *Id.*, 6:15-18. In addition to removing material, the etching process “also includes the breaking of bonds on the treated surfaces.” *Id.*, 5:61-66, 6:24-26. The etching process “can thus enhance the surface activation significantly.” *Id.*, 6:24-26.

50. In step 4, a post-etching treatment that terminates the surface with a desired bonding species may be used. *Id.*, 6:25-31. Alternatively, the termination step may occur during the etching process. *Id.* In the termination step, a “desired species ... preferably forms a temporary bond to the surface 34 atomic layer,

effectively terminating the atomic layer, until a subsequent time that this surface can be brought together with a surface terminated by the same or another bonding species.” *Id.*, 6:32-36. “Desired species on the surfaces will ... preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between [the] surfaces ... at low or room temperature.” *Id.*, 6:37-43. Then, after termination, the “wafers are optionally rinsed then dried.” *Id.*, 7:4.

51. The '143 Patent's post-etching termination process “preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species.” *Id.*, 6:44-54. The termination step “may include rinsing ... in an ammonia-based solution,” such as “ammonium hydroxide.” *Id.*, 3:34-37. The termination process may also consist of a plasma or a second etching process “whereby appropriate ... chemistries are introduced to result in termination ... with the desired species.” *Id.*, 6:55-64.

52. The '143 Patent provides examples explaining its terminating and bonding process:

- After a plasma treatment (such as oxygen), an SiO₂ surface is mainly terminated by Si-OH groups due to moisture in the plasma system and in air. *Id.*, 8:52-55. When the wafers are then immersed in an ammonium hydroxide (NH₄OH) solution, many Si-OH groups are

replaced by Si-NH₂ groups. *Id.*, 8:55-65. The hydrogen bonded Si-NH₂:Si-OH groups or Si—NH₂:Si—NH₂ groups across the bonding interface can then form Si-O-Si or Si-N-N-Si (or Si-N-Si) covalent bonds. *Id.*, 8:66-9:6.

- After an oxygen plasma treatment, an oxide surface rinsed in deionized water is mainly terminated with Si-OH groups. *Id.*, 10:39-45. Si-O-Si covalent bonds can then be formed as water is desorbed. *Id.*, 10:45-51.

53. In step 5, “[t]wo wafers are bonded by ... bringing them together to form a bonding interface.” *Id.*, 7:4-6. According to the ’143 Patent, its invention allows for wafers to be bonded together via chemical bonds that are formed at low or room temperature. *Id.*, 2:24-31. The strength of the bond between the two wafers is characterized by a “bonding energy,” which is defined as the specific surface energy of one of the separated surfaces at the bonding interface that is partially de-bonded by inserting a wedge. *Id.*, 7:17-20. The ’143 Patent teaches that, after bringing the wafers together, “annealing the bonded wafers ... may increase the bonding strength” by increasing the chemical bonding between the wafers, but the “annealing temperature should be below 200°C and may be typically in the range of 75-100°C.” *Id.*, 8:27-29. The ’143 Patent discloses that, because of its method, “wafers are bonded with sufficient strength to allow

subsequent processing operations” and that “[b]onding energies of ... 500-2000 mJ/m² or more can be achieved.” *Id.*, 8:33-37, Fig. 6A. “Since the maximum bonding energy of a van der Waals bonded silicon oxide covered wafer is about 200 mJ/m², a large portion of the bonding energy is attributed to the formation of covalent bonds at the bonding interface” using the disclosed method. *Id.*, 13:44-48.

IX. LI AND REICHE

A. Overview of Li (Ex-1005)

54. Li is a printed publication that was made publicly available in 1998, and is thus prior art under Pre-AIA 35 U.S.C. §102(a) and (b). *See* Ex-1005.

55. Li discloses a “systematic ... process to low temperature direct bond silicon and/or SiO₂ surfaces.” Ex-1005, 737. “The process begins with a cleaning process and is followed by a surface activation.” *Id.* Li discloses that its “activation processes allow a very strong low temperature bond to be created.” *Id.* Li’s “process activates the surface with ammonia [or] oxygen plasma” using a “reactive ion etcher (RIE).” *Id.*, 737-38. The wafers are then placed in direct contact, and the two are bonded at room temperature. *Id.* The bonded pair is then annealed at 200°C, resulting in a bond strength of more than 1000 erg/cm². *Id.*, 737-40.

B. Overview of Reiche (Ex-1006)

56. Reiche is a printed publication that was made publicly available in 1997, and is thus prior art under Pre-AIA 35 U.S.C. §102(a) and (b). *See* Ex-1006.

57. In Reiche, the “effect of plasma treatments (reactive ion etching in oxygen[-] containing plasmas) on Si/Si wafer bonding was investigated,” including the reactive ion etching plasma treatment’s effect on surface roughness. Ex-1006, 437-38, Table 1. Reiche reports that “adding O₂ to the feed gas caused the Si(100) surfaces to become hydrophilic and spontaneous bonding was achieved.” *Id.*, 437. As a result, “[v]ery strong bonds ... are ... obtained by lower temperature annealing (T≤400°C) after plasma treatments in O₂.” *Id.*

C. Reasons to Combine

58. A POSITA would have found it obvious to combine Li and Reiche. Both references disclose improvements to the wafer bonding process and methods to increase the bond strength between bonded wafers. Ex-1005, 737-40; Ex-1006, 437. Given that they are in a common field of endeavor and disclose similar goals, a POSITA would have found it obvious to combine their teachings.

59. Li discloses “activat[ing] the surface with ... ammonia [or] oxygen plasma” using a “reactive ion etcher (RIE),” which “allow[s] a very strong low temperature bond to be created.” Ex-1005, 737-38. Reiche details the effects of such plasma treatments on wafer bonding as it investigates the “effect of plasma

treatments (reactive ion etching in oxygen[-]containing plasmas) on ... wafer bonding” and reports that these treatments “cause[] the Si(100) surfaces to become hydrophilic,” “spontaneous bonding [to be] achieved,” and “[v]ery strong bonds [to be] obtained by low[] temperature annealing.” Ex-1006, 437-38. As a result, a POSITA would have been motivated to combine Li and Reiche as Reiche provides further information regarding an issue specifically identified by Li.

60. Li further discloses low temperature direct bonding’s requirement of “smooth, flat samples.” Ex-1005, 737. Thus, a POSITA would have understood Li to teach the importance of surface roughness in wafer bonding. Reiche discloses the effect of various treatments, including plasma activation treatments, on surface roughness, and discloses that a relatively small change in surface roughness and “[v]ery strong bonds” are achieved by reducing the concentration of gases such as CHF₃ or SF₆, which are reactive etchants, in the plasma chamber. Ex-1006, 437-38, Table 1. As a result, a POSITA would have been further motivated to combine Li and Reiche as Reiche provides even further information regarding another issue specifically identified by Li.

61. A POSITA would have found it obvious to apply Reiche’s teachings to Li’s “plasma activation process” as both disclose “activat[ing] the surface with ... plasma” using a “reactive ion etcher (RIE)” and both disclose using oxygen as the reagent gas. Moreover, as Reiche discloses that “the wafers were plasma

treated” “[a]fter cleaning in standard RCA[] solutions” (Ex-1006, 438), a POSITA would have understood that Reiche’s “silicon wafers” (*id.*) were covered in a native oxide layer, similar to Li’s disclosed SiO₂ oxide bonding layer (Ex-1005, 737-39). Ex-1008, 53-54 (“A ... native oxide ... will grow on the Si surface during the RCA cleaning process.”). Thus, Li and Reiche further both teach the same bonding surfaces. Thus, a POSITA would have found it obvious to similarly control the plasma process of Li as taught by Reiche such that the concentration of gases such as CHF₃ or SF₆ in the plasma chamber was reduced, or replace the Li process with the Reiche process, to achieve the same surface roughness results taught by Reiche.

D. Claim 1

1. Preamble ([1pre]): “A bonding method, comprising:”

62. Li describes a “developed ... systematic ... process to low temperature direct bond silicon and/or SiO₂ surfaces.” Ex-1005, 737. “The process begins with a cleaning process and is followed by a surface activation.” *Id.* “The process activates the surface with ammonia [or] oxygen plasma,” which “allow[s] a very strong low temperature bond to be created.” *Id.* The wafers are then annealed to 200°C, leading to bond strengths greater than 1000 mJ/m². *Id.* Thus, Li discloses bonding methods.

63. Accordingly, to the extent limiting, Li discloses the preamble
(Element [1pre]).

2. [1a]: “forming a planarized insulating material on a semiconductor wafer;”

64. Li discloses forming an insulating material on a semiconductor wafer. It discloses that its “process works for both bare silicon and SiO₂ surfaces.” Ex-1005, 737-39. Silicon oxides, including SiO₂, were well-known insulating materials and, therefore, a POSITA would have understood that Li’s SiO₂ bonding surfaces comprise an insulating material. Indeed, the ’143 Patent discloses the claimed “insulating material” as comprising silicon oxide and silicon dioxide. Ex-1001, 2:66-3:4, 5:19-29, Claims 16, 26. Li further explains that “semiconductor surfaces” comprising “100-mm commercial Czochralski (CZ) <100> silicon wafers [were] used in this work.” Ex-1005, 737. Thus, a POSITA would have understood that Li’s SiO₂ bonding surfaces were formed on semiconductor wafers. Thus, Li discloses forming an insulating material on a semiconductor wafer.

65. Li also renders obvious forming a planarized insulating material on a semiconductor wafer. It teaches that “direct bonding requires ... flat samples.” Ex-1005, 737. Thus, a POSITA would have understood that Li’s disclosed SiO₂ bonding surfaces were planarized. To the extent planarized bonding surfaces are not expressly disclosed in Li, a POSITA would have found it obvious to planarize Li’s disclosed SiO₂ bonding surfaces as Li teaches that “direct bonding requires

smooth, flat samples” (Ex-1005, 737), a POSITA would have understood that planarization produces smooth, flat samples, and planarization techniques to produce smooth, flat samples were well-known in the art. Thus, Li renders obvious forming a planarized insulating material on a semiconductor wafer.

66. Accordingly, Li renders obvious Element [1a].

3. [1b]: “etching the planarized insulating material in a reaction space;”

67. Li renders obvious etching the bonding surfaces. Li’s disclosed “process activates the surface with ammonia [or] oxygen plasma.” Ex-1005, 737. “A ... reactive ion *etcher (RIE)* is used for the surface plasma activation process.” *Id.*, 738.^{2,3} This is consistent with the ’143 Patent’s disclosure that its etching activation process comprises “RIE mode plasma treat[ing] ... wafers,” “O₂ plasma treat[ing] [in] RIE mode,” and “etching by O₂ plasma.” Ex-1001, 13:41-48, 14:14-37.

68. To the extent the term “etching” is interpreted to require enhancing activation, Li still renders obvious this element. Li’s disclosed “process *activates the surface* with ammonia [or] oxygen plasma,” which “allow a very strong low

² All emphases are added unless otherwise specified.

³ Although Li discloses that its “surface plasma activation process” was performed using a “reactive ion etcher,” it does not explicitly state that a plasma etching process was performed.

temperature bond to be created.” Ex-1005, 737. A POSITA would have understood that Li’s plasma process “activates the surface” and “allow[s] a very strong low temperature bond to be created” (*id.*, 737) by breaking existing bonds at the bonding surface to allow their subsequent termination with a desired atom or molecule. This is consistent with the ’143 Patent’s disclosure that its etching activation process “serves to ... break bonds ... on the wafer surface” and “can thus enhance the surface activation significantly.” Ex-1001, 6:24-26.

69. To the extent Li does not render obvious this element, it would have been obvious in view of Reiche. A POSITA would have been motivated to combine Li and Reiche for the reasons discussed above. Section IX.C. In particular, a POSITA would have been motivated to modify Li’s disclosed “surface plasma activation process” to include Reiche’s “reactive ion etching ... plasma[.]” “activation process.” Thus, the combined teachings of Li and Reiche disclose a “***reactive ion etching*** ... plasma[.]” treatment to activate the bonding surface. Ex-1005, 738 (“[a] ***reactive ion etcher (RIE)*** is used for the ***surface plasma activation process***”); Ex-1006, 437-38 (disclosing a “***reactive ion etching*** ... ***plasma[.]***” “***activation process***”). This is consistent with the ’143 Patent’s disclosure that its etching activation process comprises “RIE mode plasma treat[ing] ... wafers” and “O₂ plasma treat[ing] [in] RIE mode.” Ex-1001, 13:41-48, 14:14-37. Reiche discloses that “[v]ery strong bonds ... are ... obtained by lower temperature

annealing ($T \leq 400^\circ\text{C}$) after plasma treatments in O_2 .” Ex-1006, 437. A POSITA also would have understood that Reiche’s “reactive ion etching ... plasma[]” “activation process” activates the surface and leads to “[v]ery strong bonds” (*id.*) by breaking existing bonds at the bonding surface to allow their subsequent termination with a desired atom or molecule. This is consistent with the ’143 Patent’s disclosure that its etching activation process “serves to ... break bonds ... on the wafer surface” and “can thus enhance the surface activation significantly.” Ex-1001, 6:24-26.

70. Li further renders obvious etching the bonding surfaces in a reaction space. It discloses that “[a] Technics 800 series micro reactive ion etcher (RIE)” “*chamber*” “is used for the surface plasma activation process.” Ex-1005, 738. This is consistent with the ’143 Patent’s disclosure of the claimed “reaction space” comprising a “plasma chamber.” Ex-1001, Claims 3, 4. Thus, Li renders obvious etching the bonding surfaces in a reaction space as claimed by the ’143 Patent.

71. Accordingly, Li and Reiche render obvious Element [1b].

4. **[1c]: “terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching;”**

72. Li and Reiche render obvious terminating the bonding surfaces of the planarized insulating material with a nitrogen-containing species by a nitrogen-containing plasma during the etching. As discussed above, Li and Reiche render

obvious an “**ammonia** [$(\underline{N}H_3)$]” “**reactive ion etching** ... plasma[]” activation treatment using a “reactive ion etcher (RIE)” (Ex-1005, 737-38; Ex-1006, 437-38). *See supra*, Element [1b]; Section IX.D.3. A POSITA would have understood Li’s disclosed **ammonia** ($\underline{N}H_3$) plasma treatment to contain nitrogen. *See* Ex-1001, 3:34-37 (disclosing that the termination step may comprise the use of “an **ammonia**-based solution”).

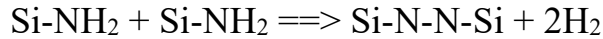
73. An ammonia plasma treatment step, such as the one disclosed in Li, terminates a bonding surface, and the mechanisms of this termination were well-understood. First, the ammonia plasma treatment forms silicon nitride on a silicon surface. Ex-1009, 14 (disclosing that an ammonia plasma etching treatment “chemically react[s] with Si to form a thin layer of Si_xN_y ” (*e.g.*, Si_3N_4)). Then, the **ammonia** plasma treatment creates free radicals of ***Si-(N_xH_y) groups*** and/or breaks bonds at the surface to ***form Si-(N_xH_y) groups*** at the dangling bonds, thereby ***terminating*** the surface. Ex-1010, 1411 (disclosing that an ammonia plasma etching treatment “attack[s] the Si-N-Si bond[s] to form ... ***Si-NH groups for hydrogen bonding***”), 1415 (“***Si-(N_xH_y) groups*** can be formed on Si_3N_4 surfaces by an ... NH_3 plasma treatment.”); Ex-1011, 3485-87 (disclosing that “ NH_3 plasma activation” on “ Si_3N_4 ” surfaces creates “free radicals of ***Si-N-H***”); Ex-1007. Next, the ***Si-(N_xH_y) groups*** at the bonding interface react to form ***Si-N-Si*** covalent bonds with H_2 as a by-product. Ex-1010, 1415 (“Si-NH groups ... can ... react to form

strong covalent bonds at temperatures as low as 90°C: $\text{Si}-(\text{N}_x\text{H}_y) + (\text{H}_y\text{N}_x)-\text{Si} \Rightarrow \text{Si}-(2\text{N}_x)-\text{Si} + y\text{H}_2$ "); Ex-1011, 3487 ("free radicals of Si-N-H [result in a] cohesive direct bond of the Si-(N)-Si-type [and] a chemical reaction as follows: $\text{Si}-(\text{N}_x\text{H}_y) + (\text{N}_x\text{H}_y)-\text{Si} \Rightarrow \text{Si}-(2\text{N}_x)-\text{Si} + y\text{H}_2$ "). Thus, a POSITA would have understood that the terminating process occurs during the etching process in Li's plasma treatment step. A POSITA also would have understood that Li's ammonia plasma treatment would terminate the bonding surfaces with Si-(N_xH_y) groups.

74. Li's disclosed "reactive ion etcher (RIE)" "ammonia ... plasma" treatment step is consistent with the '143 Patent's disclosure that its surface activation and termination processes can occur in a single step, where the "VSE served to ... break bonds ... on the wafer surface" and "[a] desired bonding species can [then] be used to terminate [the] surface 34 during the VSE by proper design of the VSE." Ex-1001, 6:24-31; *see also id.*, 6:44-54 ("The [termination] process preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species.").

75. Moreover, Li's disclosed "reactive ion etcher (RIE)" "ammonia ... plasma" treatment step is also consistent with the '143 Patent's disclosure that its termination step "may include [exposure to] an ammonia-based solution." *Id.*,

3:34-37.⁴ The '143 Patent acknowledges that when wafers are immersed in such a solution, the surface is terminated by Si-NH₂ groups, and the following bonding reaction then takes place:



Id., 8:51-9:5.

76. Li therefore discloses an identical nitrogen-based surface terminating solution, identical nitrogen-based surface terminating species, and identical nitrogen-based bonding reactions as those disclosed by the '143 Patent. Ex-1005, 737-38; Ex-1009, 14; Ex-1010, 1411, 1415; Ex-1011, 3485-87; Ex-1007; Ex-1001, 3:34-37, 8:51-9:5. Thus, Li and Reiche render obvious terminating the bonding surfaces of the planarized insulating material with a nitrogen-containing species by a nitrogen-containing plasma during the etching.

77. Accordingly, Li render and Reiche render obvious Element [1c].

5. [1d]: “bringing a first material into direct contact with the terminated and planarized insulating material outside the reaction space; and”

78. Li discloses a first material. It discloses that its “process works for both bare silicon and SiO₂ surfaces.” Ex-1005, 737-39. This is consistent with the '143 Patent's disclosure of the claimed “first material” comprising a “[l]ayer [of]

⁴ While the '143 Patent refers to a liquid-based surface treatment, a POSITA would have understood that liquid- and plasma-based treatments accomplish the same results.

SiO₂” (Ex-1001, 5:23-27), a “silicon wafer” (*id.*, 10:11-14, 10:22-24), or a “silicon wafer ... having a native oxide [or] an oxide layer formed on its surface” (*id.*, 10:37-39). *See id.*, Claims 9-11, 23. Thus, Li discloses a first material.

79. Li also discloses bringing the bonding surfaces into direct contact after terminating. It discloses that “[a]fter the plasma surfaces treatment,” the surfaces are “placed face-to-face” without “temperature [being] applied.” Ex-1005, 737-40. Thus, Li discloses bringing the bonding surfaces into direct contact after terminating. Indeed, Li discloses its surfaces were bonded without vacuum conditions, adhesive, or applied electric field. Ex-1005, 737-38; *see also* Ex-1001, 1:56-63, 7:44-58.

80. Li further discloses bringing the bonding surfaces into direct contact outside the reaction space. As discussed above, Li renders obvious etching the bonding surfaces in a reaction space as it discloses that its “plasma surfaces treatment” occurs in a “reactive ion etcher (RIE)” “chamber” (Ex-1005, 738). *See supra*, Element [1b]; Section IX.D.3. Li further discloses that “[a]fter the plasma surfaces treatment, a pair of samples is placed face-to-face into a pressure fixture” for bonding. Ex-1005, 738. Thus, a POSITA would have understood that Li’s bonding surfaces were brought into direct contact outside of its “reactive ion etcher (RIE)” “chamber” as a POSITA would have understood Li’s “pressure fixture” to be a separate apparatus than its “reactive ion etcher (RIE)” “chamber.” Thus, Li

discloses bringing the bonding surfaces into direct contact outside the reaction space as claimed by the '143 Patent.

81. Accordingly, Li discloses Element [1d].

6. [1e]: “forming a chemical bond between the terminated and planarized insulating material and the first material.”

82. Li renders obvious forming a chemical bond between the bonding surfaces of the terminated and planarized insulating material and the first material. Surfaces terminated by Si-(N_xH_y) groups, such as those exposed to Li's ammonia plasma treatment, result in the formation of *covalent bonds*, and the mechanisms of this process were well-understood. Ex-1010, 1415 (“Si-NH groups ... can ... react to form *strong covalent bonds* at temperatures as low as 90°C: Si-(N_xH_y) + (H_yN_x)-Si ==> Si-(2N_x)-Si + yH₂”); Ex-1011, 3487 (“free radicals of Si-N-H [result in a] cohesive direct bond of the Si-(N)-Si-type [and] a chemical reaction as follows: Si-(N_xH_y) + (N_xH_y)-Si ==> Si-(2N_x)-Si + yH₂”).

83. The '143 Patent acknowledges that surfaces terminated by Si-(N_xH_y) groups, such as those exposed to Li's ammonia plasma treatment, react with one another to form *covalent bonds*. Ex-1001, 8:51-9:5 (explaining that when surfaces are “terminated by ... Si-NH₂ groups,” “the following ... reaction” takes place: “Si-NH₂ + Si-NH₂ ==> Si-N-N-Si + 2H₂,” “*forming ... Si-N-N-Si (or Si-N-Si) covalent bonds*”).

84. It was well-understood that covalent bonds are chemical bonds and that covalent bonds between the surfaces indicate that the surfaces are bonded by a chemical bond. Ex-1008, *passim*.; Sections VII and VIII. Thus, a POSITA would have understood that Li's surfaces were bonded by a chemical bond.

85. Moreover, Li discloses that the bonded pair is "anneal[ed] [at] 200°C for [approximately] 24 h[, resulting in a] bond strength greater than ... 1,000 erg/cm²." Ex-1005, 737-40. A POSITA would have understood an "erg/cm²" to be a unit equivalent to a "mJ/m²," and thus would have understood Li's surfaces to have a bond strength of more than 1000 mJ/m². A POSITA also would have understood that Li's surfaces were bonded by a chemical bond as bond strengths in excess of 1000 mJ/m², as disclosed by Li, are not possible without a chemical bond, that is, having only van der Waals or hydrogen bonds. Ex-1001, 13:44-48 ("Since the maximum bonding energy of a van der Waals bonded silicon oxide covered wafer is about 200 mJ/m², a large portion of the bonding energy is attributed to the formation of covalent bonds at the bonding interface..."). Thus, Li renders obvious forming a chemical bond between the bonding surfaces of the terminated and planarized insulating material and the first material.

86. Accordingly, Li renders obvious Element [1e].

87. Thus, Li and Reiche render obvious Claim 1.

E. Claim 3: “wherein the etching the planarized insulating material is conducted in a plasma chamber, the reaction space comprising the plasma chamber”

88. *See supra*, Element [1b]. Section IX.D.3.

89. As explained above, Li and Reiche render obvious performing an “ammonia” “*reactive ion etching ... plasma[]*” activation treatment in a “*reactive ion etcher (RIE)*” “*chamber*” (Ex-1005, 737-38; Ex-1006, 437-38). *See supra*, Element [1b]; Section IX.D.3. Thus, the etching comprises exposing the bonding surfaces to a plasma etching process in a reaction space comprising a plasma chamber, *i.e.*, “[a] Technics 800 series micro reactive ion etcher (RIE)” “*chamber.*” Ex-1005, 738.

90. For these reasons, and for those stated above for Claim 1, Li and Reiche render obvious Claim 3. *See supra*, Claim 1.

F. Claim 4: “wherein the etching and the terminating comprise exposing the planarized insulating material to the plasma etching process in a plasma chamber, the reaction space comprising the plasma chamber”

91. *See supra*, Elements [1b], [1c]. Sections IX.D.3 and D.4.

92. Specifically, Li and Reiche render obvious performing an “ammonia” “*reactive ion etching ... plasma[]*” treatment step in a “*reactive ion etcher (RIE)*” “*chamber*” to both etch and terminate the bonding surfaces (Ex-1005, 737-38; Ex-1006, 437-38). *See supra*, Elements [1b], [1c]; Sections IX.D.3 and D.4. For example, as explained above, an ammonia plasma treatment step, such as the one

disclosed in Li, performs the etching and the terminating in the same step. *See supra*, Element [1c]; Section IX.D.4. Thus, the etching and terminating comprise exposing the bonding surfaces to a plasma etching process in a reaction space comprising a plasma chamber, *i.e.*, “[a] Technics 800 series micro reactive ion etcher (RIE)” “**chamber.**” Ex-1005, 738.

93. For these reasons, and for those stated above for Claim 1, Li and Reiche render obvious Claim 4. *See supra*, Claim 1.

G. Claim 6: “wherein the exposing the planarized insulating material to the plasma etching process in the plasma chamber comprises using nitrogen gas”

94. *See supra*, Element [1b]. Section IX.D.3.

95. As explained above, Li and Reiche render obvious performing an “**ammonia** [(NH₃)]” “**reactive ion etching ... plasma**” treatment step in a “**reactive ion etcher (RIE)**” “**chamber**” to both etch and terminate the bonding surfaces (Ex-1005, 737-38; Ex-1006, 437-38). *See supra*, Elements [1b], [1c]; Sections IX.D.3 and D.4. A POSITA would have understood the ammonia plasma treatment to comprise using nitrogen gas.

96. For these reasons, and for those stated above for Claims 1 and 4, Li and Reiche render obvious Claim 6. *See supra*, Claims 1, 4.

H. Claim 14: “wherein the bringing into direct contact is performed at room temperature”

97. *See supra*, Element [1d]. Section IX.D.5.

98. As explained above, Li discloses that the bonding surfaces are “placed face-to-face” without “temperature [being] applied” (Ex-1005, 737-40). *See supra*, Element [1d]; Section IX.D.5. Thus, a POSITA would have understood Li’s bonding process to comprise bringing the bonding surfaces into direct contact at room temperature.

99. For these reasons, and for those stated above for Claim 1, Li and Reiche render obvious Claim 14. *See supra*, Claim 1.

I. Claim 15: “wherein the bringing into direct contact is conducted in air”

100. *See supra*, Element [1d]. Section IX.D.5.

101. As explained above, Li discloses that the bonding surfaces are “placed face-to-face” without “temperature [being] applied” and without vacuum conditions, adhesive, or applied electric field (Ex-1005, 737-38; *see also* Ex-1001, 1:56-63, 7:44-58). *See supra*, Element [1d]; Section IX.D.5. Thus, a POSITA would have understood Li’s bonding process to comprise bringing the bonding surfaces into direct contact in air.

102. For these reasons, and for those stated above for Claim 1, Li and Reiche render obvious Claim 15. *See supra*, Claim 1.

J. Claim 21

1. Preamble ([21pre]): “A bonded structure comprising:”

103. *See supra*, Elements [1pre], [1d], [1e]. Sections IX.D.1, D.5, and D.6.

2. [21a]: “a first semiconductor material comprising a planarized insulating material having a first bonding surface; and”

104. *See supra*, Element [1a]. Section IX.D.2.

105. As explained above, Li discloses that its “process works for” “smooth, flat samples” of “both bare silicon and SiO₂ surfaces” (Ex-1005, 737-39) and thus renders obvious forming a planarized insulating material on a semiconductor wafer. *See supra*, Element [1a]; Section IX.D.2. For these reasons, and for those stated above for Element [1a], Li renders obvious a first semiconductor material comprising a planarized insulating material having a first bonding surface. *See supra*, Element [1a].

3. [21b]: “a second material having a second bonding surface,”

106. *See supra*, Element [1d]. Section IX.D.5.

107. As explained above, Li discloses that its “process works for both bare silicon and SiO₂ surfaces” (Ex-1005, 737-39). *See supra*, Element [1d]; Section IX.D.5. This is consistent with the ’143 Patent’s disclosure of the claimed “second material” comprising a “[l]ayer [of] SiO₂” (Ex-1001, 5:23-27), a “silicon wafer” (*id.*, 10:11-14, 10:22-24), or a “silicon wafer ... having a native oxide [or] an oxide layer formed on its surface” (*id.*, 10:37-39). *See id.*, Claims 9-11, 23. Thus, Li discloses a second material having a second bonding surface.

4. [21c]: “wherein the first bonding surface is an etched surface terminated with a nitrogen-containing species, and”

108. *See supra*, Elements [1b], [1c]. Sections IX.D.3 and D.4.

5. [21d]: “wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive.”

109. *See supra*, Elements [1d], [1e]. Sections IX.D.5 and D.6.

110. As explained above, Li discloses that the bonding surfaces are “placed face-to-face” without “temperature [being] applied” and without vacuum conditions, adhesive, or applied electric field (Ex-1005, 737-38; *see also* Ex-1001, 1:56-63, 7:44-58). *See supra*, Element [1d]; Section IX.D.5. The bonded pair is then “anneal[ed] [at] 200°C” “for [approximately] 24 h,” resulting in a chemical bond with a “bond strength greater than” 1,000 mJ/m² (Ex-1005, 737-40). *See supra*, Element [1e]; Section IX.D.6.

111. Accordingly, Li and Reiche render obvious Claim 21.

K. Claim 22: “further comprising at least one integrated circuit in the first semiconductor material”

112. *See supra*, Element [21a]. Section IX.J.2.

113. As explained above, Li discloses that its “process works for” “smooth, flat samples” of “both bare silicon and SiO₂ surfaces” (Ex-1005, 737-39) and thus renders obvious a first semiconductor material comprising a planarized insulating material having a first bonding surface. *See supra*, Element [21a]; Section IX.J.2.

To the extent at least one integrated circuit in the first semiconductor material is not expressly disclosed in Li, a POSITA would have found it obvious as Li teaches the applicability of its disclosed process to “[d]irect bonding of silicon and other materials commonly used in semiconductor structures” (Ex-1005, 737), a POSITA would have understood semiconductor materials comprising at least one integrated circuit in the semiconductor material were “materials commonly used in semiconductor structures,” and semiconductor materials comprising at least one integrated circuit in the semiconductor material were well-known in the art. Thus, Li renders obvious a first semiconductor material comprising at least one integrated circuit in the first semiconductor material.

114. For these reasons, and for those stated above for Claim 21, Li and Reiche render obvious Claim 22. *See supra*, Claim 21.

L. Claim 24: “wherein the chemical bond has a strength of at least 500 mJ/m²”

115. *See supra*, Element [1e]. Section IX.D.6.

116. As explained above, in Li, after bringing the bonding surfaces into direct contact at room temperature, the bonds were annealed at 200°C for approximately 24 hours, resulting in chemical bonds with a bond strength of *more than 1000 mJ/m²* (Ex-1005, 737-40). *See supra*, Element [1e]; Section IX.D.6.

117. For these reasons, and for those stated above for Claim 21, Li and Reiche render obvious Claim 24. *See supra*, Claim 21.

M. Claim 29: “wherein the first bonding surface is terminated with a nitrogen-containing species by at least one of a nitrogen-containing plasma during etching and a nitrogen-containing solution after etching”

118. *See supra*, Element [1c]. Section IX.D.4.

119. For these reasons, and for those stated above for Claim 21, Li and Reiche render obvious Claim 29. *See supra*, Claim 21.

N. Claim 30: “wherein the chemical bond is a covalent bond”

120. *See supra*, Element [1e]. Section IX.D.6.

121. For these reasons, and for those stated above for Claim 21, Li and Reiche render obvious Claim 30. *See supra*, Claim 21.

O. Claim 31

1. Preamble ([31pre]): “A bonding method, comprising:”

122. *See supra*, Element [1pre]. Section IX.D.1.

2. [31a]: “forming a planarized insulating material on a semiconductor wafer;”

123. *See supra*, Element [1a]. Section IX.D.2.

3. [31b]: “etching the planarized insulating material;”

124. *See supra*, Element [1b]. Section IX.D.3.

4. [31c]: “terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching;”

125. *See supra*, Element [1c]. Section IX.D.4.

5. **[31d]: “bringing a first material into direct contact with the terminated and planarized insulating material; and”**

126. *See supra*, Element [1d]. Section IX.D.5.

6. **[31e]: “forming a chemical bond between the terminated and planarized insulating material and the first material.”**

127. *See supra*, Element [1e]. Section IX.D.6.

128. Accordingly, Li and Reiche render obvious Claim 31.

P. Claim 32

1. **Preamble ([32pre]): “A bonding method, comprising:”**

129. *See supra*, Element [1pre]. Section IX.D.1.

2. **[32a]: “forming a planarized insulating material on a processed semiconductor wafer;”**

130. *See supra*, Element [1a]. Section IX.D.2.

131. As explained above, Li discloses that its “process works for” “smooth, flat samples” of “both bare silicon and SiO₂ surfaces” (Ex-1005, 737-39) and thus renders obvious a planarized insulating material on a semiconductor wafer. *See supra*, Element [1a]; Section IX.D.2. Moreover, as Li discloses that its “attempted bonding samples” were “commercial ... silicon wafers” that were “cut” and “RCA clean[ed]” (Ex-1005, 737), a POSITA would have understood that Li’s disclosed SiO₂ bonding surfaces were formed on a processed semiconductor wafer. To the extent forming an SiO₂ bonding surface on a processed semiconductor wafer is not expressly disclosed in Li, a POSITA would have found it obvious as Li teaches the

applicability of its disclosed process to “[d]irect bonding of silicon and other materials commonly used in semiconductor structures” (Ex-1005, 737), a POSITA would have understood processed semiconductor wafers were “materials commonly used in semiconductor structures,” and forming SiO₂ bonding layers on processed semiconductor wafers was well-known in the art. Thus, Li renders obvious forming a planarized insulating material on a processed semiconductor wafer.

3. [32b]: “exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas;”

132. *See supra*, Elements [1b], [1c]. Sections IX.D.3 and D.4.

133. As explained above, Li’s disclosed “process activates the surface with *ammonia* [(NH₃)] *plasma*,” and a “reactive ion *etcher (RIE)*” “*chamber*” “is used for the surface *plasma activation* process” (Ex-1005, 737-38). *See supra*, Elements [1b], [1c]; Sections IX.D.3 and D.4. Moreover, the combined teachings of Li and Reiche disclose an “*ammonia* [(NH₃)]” “*reactive ion etching ... plasma*” treatment to activate the bonding surface. Ex-1005, 738 (“[a] *reactive ion etcher (RIE)* is used for the surface *plasma* activation process”); Ex-1006, 437-38 (disclosing a “*reactive ion etching ... plasma*” “activation process”). Thus, Li’s disclosed *ammonia* (NH₃) plasma treatment comprises exposing the bonding surfaces of the planarized insulating material to a plasma process in a

reaction space comprising a plasma chamber, *i.e.*, “[a] Technics 800 series micro reactive ion etcher (RIE)” “**chamber.**” Ex-1005, 738. A POSITA would have understood Li’s disclosed **ammonia** (NH₃) plasma treatment to comprise using a nitrogen-containing gas. Thus, Li and Reiche render obvious exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas. *See* Ex-1001, 6:24-26, 13:41-48, 14:14-37.

4. [32c]: “**terminating the planarized insulating material with a species;**”

134. *See supra*, Element [1c]. Section IX.D.4.

5. [32d]: “**bringing into direct contact the terminated and planarized insulating material and a first material outside of said plasma chamber; and**”

135. *See supra*, Element [1d]. Section IX.D.5.

6. [32e]: “**forming a chemical bond between the terminated and planarized insulating material and the first material.**”

136. *See supra*, Element [1e]. Section IX.D.6.

137. Accordingly, Li and Reiche render obvious Claim 32.

Q. Claim 33: “wherein the species comprises nitrogen”

138. *See supra*, Element [1c]. Section IX.D.4.

139. For these reasons, and for those stated above for Claim 32, Li and Reiche render obvious Claim 33. *See supra*, Claim 32.

X. LI, REICHE, AND BOWER

A. Overview of Bower (Ex-1007)

140. Bower is a United States Patent that issued on April 2, 1996, and is thus prior art under Pre-AIA 35 U.S.C. §102(a), (b), and (e). *See* Ex-1007.

141. Bower discloses a “process” for “direct bonding” “at low temperatures” “in which a ... surface is rendered ... reactive” “through ammonia plasma activation” (*i.e.*, “a plasma of NH₃”) “by creating nitrogen based radicals on the surface.” *Id.*, Abstract, 2:12-25. “[T]he surface is [then] direct bonded to a second surface, and the bonded surfaces are annealed at” a “low temperature” “typically in the range of ... 90°C to ... 300°C.” *Id.*, Abstract, 4:32-44. Bower discloses that its process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like.” *Id.*, 3:10-20, 4:45-5:65, 6:64-7:6. Bower further discloses that, for “successful[] bonding,” the “[m]aterial preparation” for its “low temperature nitrogen bonding” process “require[s]” both “[s]urface flatness” and a “surface microroughness [of] less than 10 Å.” *Id.*, 6:64-7:6.

B. Reasons to Combine

142. A POSITA would have found it obvious to combine Li, Reiche, and Bower. All three references disclose improvements to the wafer bonding process

and methods to increase the bond strength between bonded wafers. Ex-1005, 737-40; Ex-1006, 437; Ex-1007, Abstract. Given that they are in a common field of endeavor and disclose similar goals, a POSITA would have found it obvious to combine their teachings.

143. Further, a POSITA would have found it obvious to combine Li and Bower's teachings based on the similarities of their disclosures. Li discloses "activat[ing] the surface with ... ammonia [or] oxygen plasma," which "allow[s] a very strong low temperature bond to be created." Ex-1005, 737-38. Similarly, Bower discloses a "process" for "direct bonding" "at low temperatures" "in which a ... surface is rendered ... reactive" "through ammonia plasma activation" (*i.e.*, "a plasma of NH₃"). Ex-1007, Abstract, 2:12-25. Li further discloses that its "process works for both bare silicon and SiO₂ surfaces." Ex-1005, 737-39. Similarly, Bower describes applying its disclosed activating and bonding process to "silicon wafer[s]," "silicon," "silicon dioxide, and the like." Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6.

144. Li discloses low temperature direct wafer bonding's requirement of "smooth, flat samples." Ex-1005, 737. Bower reiterates this point, explaining that, for "successful[] bonding," the "[m]aterial preparation" for its "low temperature nitrogen bonding" process "require[s]" both "[s]urface flatness" and a "surface microroughness [of] less than 10 Å." Ex-1007, 6:64-7:6. Bower further discloses

applying its disclosed activating and bonding process to “planarized surfaces.” *Id.*, 3:10-20. As a result, a POSITA would have been motivated to combine Li and Bower as Bower provides further information regarding an issue specifically identified by Li.

145. Li further discloses the applicability of its process to the “[d]irect bonding of silicon and other materials commonly used in semiconductor structures.” Ex-1005, 737-39. Bower describes examples of its process being used for the “[d]irect bonding” of “silicon and other materials commonly used in semiconductor structures,” such as “planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like.” Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6. As a result, a POSITA would have been further motivated to combine Li and Bower as Bower provides even further information regarding another issue specifically identified by Li.

C. Claim 1

1. Preamble ([1pre]): “A bonding method, comprising:”

146. *See supra*, Ground 1, Element [1pre]. Section IX.D.1.

2. [1a]: “forming a planarized insulating material on a semiconductor wafer;”

147. *See supra*, Ground 1, Element [1a]. Section IX.D.2.

148. To the extent Li does not disclose or render obvious this element, it would have been obvious in view of Bower. A POSITA would have been motivated to combine Li, Reiche, and Bower for the reasons discussed above. Section X.B. In particular, a POSITA would have been motivated to apply Bower's teachings of applying its disclosed activating and bonding process to "planarized surfaces of 'completed' integrated circuit chips and wafers," "silicon integrated circuits," "silicon wafer[s]," "silicon," "silicon dioxide, and the like" to Li's bonding process.

149. Bower discloses forming an insulating material on a semiconductor wafer. It discloses applying its disclosed activating and bonding process to "silicon wafer[s]," "silicon," "silicon dioxide, and the like." Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6. Silicon oxides, including silicon dioxide, were well-known insulating materials and, therefore, a POSITA would have understood that Bower's silicon dioxide bonding surfaces comprise an insulating material. Indeed, the '143 Patent discloses the claimed "insulating material" as comprising silicon oxide and silicon dioxide. Ex-1001, 2:66-3:4, 5:19-29, Claims 16, 26. Bower further discloses applying its process to "silicon wafer[s]," and explains that its "invention pertains generally to semiconductor direct bonding techniques" and "provide[s] for direct bonding of semiconductor chips." Ex-1007, 1:14-17, 3:10-20, 3:54-55, 4:45-5:65, 6:64-7:6. Thus, a POSITA would have understood that Bower's silicon

dioxide bonding surfaces were formed on semiconductor wafers. Thus, Bower discloses forming an insulating material on a semiconductor wafer.

150. Bower also renders obvious forming a planarized insulating material on a semiconductor wafer. It teaches that its process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers.” Ex-1007, 3:10-20. Thus, a POSITA would have understood that Bower’s disclosed silicon dioxide bonding surfaces were planarized. To the extent planarized silicon dioxide bonding surfaces are not expressly disclosed in Bower, a POSITA would have found it obvious to planarize Bower’s disclosed silicon dioxide bonding surfaces based on its teaching of being “applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers” (Ex-1007, 3:10-20), a POSITA would have understood that silicon dioxide bonding surfaces were common on “‘completed’ integrated circuit chips and wafers,” and the planarization of silicon dioxide on “‘completed’ integrated circuit chips and wafers” was well-known in the art. Thus, Bower renders obvious forming a planarized insulating material on a semiconductor wafer.

151. Accordingly, Li and Bower render obvious Element [1a].

3. [1b]: “etching the planarized insulating material in a reaction space;”

152. *See supra*, Ground 1, Element [1b]. Section IX.D.3.

4. **[1c]: “terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching;”**

153. *See supra*, Ground 1, Element [1c]. Section IX.D.4.

5. **[1d]: “bringing a first material into direct contact with the terminated and planarized insulating material outside the reaction space; and”**

154. *See supra*, Ground 1, Element [1d]. Section IX.D.5.

6. **[1e]: “forming a chemical bond between the terminated and planarized insulating material and the first material.”**

155. *See supra*, Ground 1, Element [1e]. Section IX.D.6.

156. Accordingly, Li, Reiche, and Bower render obvious Claim 1.

- D. Claim 3: “wherein the etching the planarized insulating material is conducted in a plasma chamber, the reaction space comprising the plasma chamber”**

157. *See supra*, Ground 1, Claim 3. Section IX.E.

- E. Claim 4: “wherein the etching and the terminating comprise exposing the planarized insulating material to the plasma etching process in a plasma chamber, the reaction space comprising the plasma chamber”**

158. *See supra*, Ground 1, Claim 4. Section IX.F.

- F. Claim 6: “wherein the exposing the planarized insulating material to the plasma etching process in the plasma chamber comprises using nitrogen gas”**

159. *See supra*, Ground 1, Claim 6. Section IX.G.

G. Claim 14: “wherein the bringing into direct contact is performed at room temperature”

160. *See supra*, Ground 1, Claim 14. Section IX.H.

H. Claim 15: “wherein the bringing into direct contact is conducted in air”

161. *See supra*, Ground 1, Claim 15. Section IX.I.

I. Claim 20: “wherein the planarized insulating material has a surface roughness between about 0.5 and 1.5 nm after the etching and before the bringing into direct contact”

162. This element would have been obvious over Li and Reiche in view of Bower. A POSITA would have been motivated to combine Li, Reiche, and Bower for the reasons discussed above. Section X.B. In particular, a POSITA would have been motivated to apply Bower’s teaching that, for “successful[] bonding,” the “[m]aterial preparation” for its “low temperature nitrogen bonding” process “require[s]” both “[s]urface flatness” and a “surface microroughness [of] less than 10 Å” to Li’s bonding process.

163. As explained above, Li and Reiche render obvious preparing an oxide surface for bonding through an “ammonia” “reactive ion etching ... plasma[]” “activation process” (Ex-1005, 737-39; Ex-1006, 437-38). *See supra*, Ground 1, Element [1b]; Section IX.D.3. Bower also discloses preparing an oxide surface for bonding “through [an] ammonia plasma activation” treatment. Ex-1007, Abstract, 2:12-25, 3:10-20, 4:45-5:65, 6:64-7:6. Although Bower does not disclose that its

“ammonia” “plasma activation treatment” etches the bonding surface, Bower and Li disclose identical bonding surfaces and an identical nitrogen-based bonding process. Bower further explains that, for “successful[] bonding,” the surface “preparation” for its “low temperature nitrogen bonding” process “require[s]” a “surface microroughness [of] less than 10 Å.” Ex-1007, 6:64-7:6. A POSITA would have understood that Bower’s surface “preparation” “require[ment]” of a “surface microroughness [of] less than 10 Å” was applicable to all surface preparation treatments for “low temperature nitrogen bonding,” including an “ammonia” “reactive ion etching ... plasma[]” “activation process.” Thus, to the extent the effect of ammonia plasma etching on surface roughness is not expressly disclosed in Li and Reiche, a POSITA would have found it obvious to configure the ammonia plasma treatment so that it etched the bonding surface to a “surface microroughness [of] less than 10 Å [1.0 nm].”

164. Notably, the ’143 Patent does not identify any critical value for surface roughness within the range of 0.5 to 1.5 nm, and states that “surface roughness may be in a range of 0.1 to 3.0 nm.” Ex-1001, 2:50-59. Thus, the disclosure of Bower is consistent with the disclosure of the ’143 Patent.

165. Thus, Li, Reiche, and Bower render obvious the bonding surface having a surface roughness between about 0.5 and 1.5 nm after the etching and before the bringing into direct contact.

166. For these reasons, and for those stated above for Claim 1, Li, Reiche, and Bower render obvious Claim 20. *See supra*, Claim 1.

J. Claim 21

1. Preamble ([21pre]): “A bonded structure comprising:”

167. *See supra*, Ground 1, Element [21pre]. Section IX.J.1.

2. [21a]: “a first semiconductor material comprising a planarized insulating material having a first bonding surface; and”

168. *See supra*, Ground 2, Element [1a]. Section X.C.2.

169. To the extent Li does not disclose or render obvious this element, it would have been obvious in view of Bower. As explained above, Bower discloses that its process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like” (Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6) and thus renders obvious forming a planarized insulating material on a semiconductor wafer. *See supra*, Ground 2, Element [1a]; Section X.C.2. For these reasons, and for those stated above for Element [1a], Li and Bower render obvious a first semiconductor material comprising a planarized insulating material having a first bonding surface. *See supra*, Ground 2, Element [1a].

3. [21b]: “a second material having a second bonding surface,”

170. *See supra*, Ground 1, Element [21b]. Section IX.J.3.

4. **[21c]: “wherein the first bonding surface is an etched surface terminated with a nitrogen-containing species, and”**

171. *See supra*, Ground 1, Element [21c]. Section IX.J.4.

5. **[21d]: “wherein the first and second bonding surfaces are in direct contact with each other and bonded together with a chemical bond without any intervening adhesive.”**

172. Accordingly, Li, Reiche, and Bower render obvious Claim 21.

- K. **Claim 22: “further comprising at least one integrated circuit in the first semiconductor material”**

173. *See supra*, Ground 2, Element [21a]. Section X.J.2.

174. To the extent Li does not disclose or render obvious this element, it would have been obvious in view of Bower. A POSITA would have been motivated to combine Li, Reiche, and Bower for the reasons discussed above. Section X.B. In particular, a POSITA would have been motivated to apply Bower’s teachings of applying its disclosed activating and bonding process to “planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like” to Li’s bonding process.

175. Bower discloses forming an insulating material on a semiconductor material. It discloses applying its disclosed activating and bonding process to “silicon wafer[s],” “silicon,” “silicon dioxide, and the like.” Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6. Silicon oxides, including silicon dioxide, were well-known

insulating materials and, therefore, a POSITA would have understood that Bower's silicon dioxide bonding surfaces comprise an insulating material. Indeed, the '143 Patent discloses the claimed "insulating material" as comprising silicon oxide and silicon dioxide. Ex-1001, 2:66-3:4, 5:19-29, Claims 16, 26. Bower further discloses applying its process to "silicon wafer[s]," and explains that its "invention pertains generally to semiconductor direct bonding techniques" and "provide[s] for direct bonding of semiconductor chips." Ex-1007, 1:14-17, 3:10-20, 3:54-55, 4:45-5:65, 6:64-7:6. Thus, a POSITA would have understood that Bower's silicon dioxide bonding surfaces were formed on a semiconductor material. Thus, Bower discloses forming an insulating material on a semiconductor material.

176. Bower also discloses a semiconductor material comprising at least one integrated circuit in the semiconductor material. It teaches that its process "can be applied to planarized surfaces of 'completed' integrated circuit chips and wafers." Ex-1007, 3:10-20. A POSITA would have understood "'completed' integrated circuit chips and wafers" to comprise a semiconductor material comprising at least one integrated circuit in the semiconductor material. Thus, Bower discloses a semiconductor material comprising at least one integrated circuit in the semiconductor material.

177. Bower renders obvious forming a planarized insulating material on a semiconductor material comprising at least one integrated circuit. It teaches that

its process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers.” Ex-1007, 3:10-20. Thus, a POSITA would have understood that the silicon dioxide bonding surfaces of the “‘completed’ integrated circuit chips and wafers” were planarized. To the extent planarized silicon dioxide bonding surfaces of “integrated circuit chips and wafers” are not expressly disclosed in Bower, a POSITA would have found it obvious to planarize Bower’s disclosed silicon dioxide bonding surfaces of “integrated circuit chips and wafers” as silicon dioxide bonding surfaces were common on “integrated circuit chips and wafers,” Bower teaches its process being “applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers” (Ex-1007, 3:10-20), and the planarization of silicon dioxide bonding surfaces on “‘completed’ integrated circuit chips and wafers” was well-known in the art. Thus, Bower renders obvious forming a planarized insulating material on a semiconductor wafer. Accordingly, Bower renders obvious a first semiconductor material comprising a planarized insulating material having a first bonding surface and comprising at least one integrated circuit in the semiconductor material.

178. For these reasons, and for those stated above for Claim 21, Li, Reiche, and Bower render obvious Claim 22. *See supra*, Claim 21.

L. Claim 24: “wherein the chemical bond has a strength of at least 500 mJ/m²”

179. *See supra*, Ground 1, Claim 24. Section IX.L.

M. Claim 29: “wherein the first bonding surface is terminated with a nitrogen-containing species by at least one of a nitrogen-containing plasma during etching and a nitrogen-containing solution after etching”

180. *See supra*, Ground 1, Claim 29. Section IX.M.

N. Claim 30: “wherein the chemical bond is a covalent bond”

181. *See supra*, Ground 1, Claim 30. Section IX.N.

O. Claim 31

1. Preamble ([31pre]): “A bonding method, comprising:”

182. *See supra*, Ground 1, Element [31pre]. Section IX.O.1.

2. [31a]: “forming a planarized insulating material on a semiconductor wafer;”

183. *See supra*, Ground 1, Element [31a]. Section IX.O.2.

184. To the extent Li does not disclose or render obvious this element, it would have been obvious in view of Bower. A POSITA would have been motivated to combine Li, Reiche, and Bower for the reasons discussed above. Section X.B. In particular, a POSITA would have been motivated to apply Bower’s teachings of applying its disclosed activating and bonding process to “planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like” to Li’s bonding process.

185. Bower discloses forming an insulating material on a semiconductor wafer. It discloses applying its disclosed activating and bonding process to

“silicon wafer[s],” “silicon,” “silicon dioxide, and the like.” Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6. Silicon oxides, including silicon dioxide, were well-known insulating materials and, therefore, a POSITA would have understood that Bower’s silicon dioxide bonding surfaces comprise an insulating material. Indeed, the ’143 Patent discloses the claimed “insulating material” as comprising silicon oxide and silicon dioxide. Ex-1001, 2:66-3:4, 5:19-29, Claims 16, 26. Bower further discloses applying its process to “silicon wafer[s],” and explains that its “invention pertains generally to semiconductor direct bonding techniques” and “provide[s] for direct bonding of semiconductor chips.” Ex-1007, 1:14-17, 3:10-20, 3:54-55, 4:45-5:65, 6:64-7:6. Thus, a POSITA would have understood that Bower’s silicon dioxide bonding surfaces were formed on semiconductor wafers. Thus, Bower discloses forming an insulating material on a semiconductor wafer.

186. Bower also renders obvious forming a planarized insulating material on a semiconductor wafer. It teaches that its process “can be applied to planarized surfaces of ‘completed’ integrated circuit chips and wafers.” Ex-1007, 3:10-20. Thus, a POSITA would have understood that Bower’s disclosed silicon dioxide bonding surfaces were planarized. To the extent planarized silicon dioxide bonding surfaces are not expressly disclosed in Bower, a POSITA would have found it obvious to planarize Bower’s disclosed silicon dioxide bonding surfaces based on its teaching of being “applied to planarized surfaces of ‘completed’

integrated circuit chips and wafers” (Ex-1007, 3:10-20), a POSITA would have understood that silicon dioxide bonding surfaces were common on “‘completed’ integrated circuit chips and wafers,” and the planarization of silicon dioxide on “‘completed’ integrated circuit chips and wafers” was well-known in the art. Thus, Bower renders obvious forming a planarized insulating material on a semiconductor wafer.

187. Accordingly, Li and Bower render obvious Element [31a].

3. [31b]: “etching the planarized insulating material;”

188. *See supra*, Ground 1, Element [31b]. Section IX.O.3.

4. [31c]: “terminating the planarized insulating material with a nitrogen-containing species by at least one of: a nitrogen-containing plasma during the etching, and a nitrogen-containing solution after the etching;”

189. *See supra*, Ground 1, Element [31c]. Section IX.O.4.

5. [31d]: “bringing a first material into direct contact with the terminated and planarized insulating material; and”

190. *See supra*, Ground 1, Element [31d]. Section IX.O.5.

6. [31e]: “forming a chemical bond between the terminated and planarized insulating material and the first material.”

191. *See supra*, Ground 1, Element [31e]. Section IX.O.6.

192. Accordingly, Li, Reiche, and Bower render obvious Claim 31.

P. Claim 32

1. Preamble ([32pre]): “A bonding method, comprising:”

193. *See supra*, Ground 1, Element [32pre]. Section IX.P.1.

2. [32a]: “forming a planarized insulating material on a processed semiconductor wafer;”

194. *See supra*, Ground 2, Element [1a]. Section X.C.2.

195. To the extent Li does not disclose or render obvious this element, it would have been obvious in view of Bower. As explained above, Bower discloses applying its disclosed activating and bonding process to “planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” “wafers which include conventional Al metalization,” “silicon wafer[s],” “silicon,” “silicon dioxide, and the like” (Ex-1007, 3:10-20, 4:45-5:65, 6:64-7:6) and thus renders obvious a planarized insulating material on a semiconductor wafer. *See supra*, Ground 2, Element [1a]; Section X.C.2. A POSITA would have understood “planarized surfaces of ‘completed’ integrated circuit chips and wafers,” “silicon integrated circuits,” and “wafers which include conventional Al metalization” to comprise a processed semiconductor wafer. Thus, Bower renders obvious forming a planarized insulating material on a processed semiconductor wafer.

196. Accordingly, Li and Bower render obvious Element [32a].

3. **[32b]: “exposing the planarized insulating material to a plasma process in a plasma chamber using a nitrogen-containing gas;”**

197. *See supra*, Ground 1, Element [32b]. Section IX.P.3.

4. **[32c]: “terminating the planarized insulating material with a species;”**

198. *See supra*, Ground 1, Element [32c]. Section IX.P.4.

5. **[32d]: “bringing into direct contact the terminated and planarized insulating material and a first material outside of said plasma chamber; and”**

199. *See supra*, Ground 1, Element [32d]. Section IX.P.5.

6. **[32e]: “forming a chemical bond between the terminated and planarized insulating material and the first material.”**

200. *See supra*, Ground 1, Element [32e]. Section IX.P.6.

201. Accordingly, Li, Reiche, and Bower render obvious Claim 32.

Q. Claim 33: “wherein the species comprises nitrogen”

202. *See supra*, Ground 1, Claim 33. Section IX.Q.

Declaration of Dr. Charles Hunt
U.S. Patent No. 9,391,143

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 30, 2018



Dr. Charles Hunt