SEMICONDUCTOR WAFER BONDING: SCIENCE AND TECHNOLOGY

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Samsung v. Invensas Bonding

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SERIES PREFACE

The Solid-State Monograph Series of the Electrochemical Society (ECS) is aimed at providing detailed and focused expositions by recognized experts on current topics of interest in solid-state science and technology. ECS is an international, nonprofit, educational society serving over 7000 members engaged in solid-state and electrochemical science and technology (on the Web at http://www.electrochem.org). These topics are of broad interest to the various solid-state divisions of ECS, including the Electronics, the Dielectric Science and Technology, the High Temperature Materials, and the Luminescence and Display Materials divisions. The Energy Technology and the Sensor divisions also have extensive interests in solid-state topics. Each monograph is expected to include a historical discussion of the subject, an exposition of its current status, and a projection of future trends, along with appropriate scientific and technical content and literature references.

It is a pleasure to introduce the first volume in this Monograph Series, *Semiconductor Wafer Bonding: Science and Technology*, written by Q.-Y. Tong and U. Gösele of Duke University, North Carolina, USA and the Max-Planck-Institute for Microstructure Physics, Halle, Germany, respectively. Wafer bonding is the process that results in the joining of semiconductor wafers without the addition of an adhesive agent. It is a technique that has received extensive attention for its application in microelectronics, power electronics, microelectromechanical systems technology, and optoelectronics.

Wafer bonding has established itself as a commercial means for the production of silicon-on-insulator (SOI) wafers. Tong and Gösele are leading researchers in the field of wafer bonding, credited with inventing the Micro-CleanRoom setup for bonding, modeling the processes of hydrophobic and hydrophilic bonding, inventing the low-temperature bonding of dissimilar materials (such as Si/quartz, Si/glass, Si/SiC, Si/sapphire, Si/GaAs, and Si/InP), studying device-layer transfer of bonded and etched-back materials and circuits, inventing the Smarter-Cut process with the co-implantation of boron and hydrogen, introducing the bonding of ultrathick layers, and investigating the applications of low-vacuum bonding.

This monograph describes the role of fundamental physical and chemical mechanisms in the bonding process. It covers the practical aspects of the influence of particles, surface steps, and cavities, surface preparation techniques, the effects of thermal treatments, the electrical properties of bonded

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interfaces, stresses in bonded wafers, and the bonding of dissimilar materials and structured wafers. This monograph then details the mainstream applications of bonding in VLSI, high-voltage and high-power devices, and micromechanics. It concludes with an assessment of emerging and future applications in optoelectronics, electroacoustics, electromagnetooptics, new materials combinations, and gettering applications.

Authors interested in contributing to this series are encouraged to contact the Chair of the Solid-State Monograph Committee or the ECS Publications Manager.

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PREFACE

Wafer bonding allows one to join mirror-polished semiconductor or other wafers without the addition of any glue. Wafer bonding has been applied in microelectronics, power electronics, micromechanics, and optoelectronics to name just a few areas. Bonded silicon-on-insulators (SOI) wafers are commercially available from a number of companies. Materials that have been used for wafer bonding include not only silicon, but also III-V compounds, fused and crystalline quartz, glass, silicon carbide, sapphire, ferroelectrics and many other materials. Wafer bonding is deceivingly simple and allows one to produce a variety of materials combinations not available otherwise. Nevertheless, it appears that most researchers and engineers, when considering the use of wafer bonding technology, are initially confronted with a number of down-to earth questions and problems. The answers to these questions on wafer bonding are mostly available somewhere, but unfortunately are distributed over close to one thousand publications in a variety of journals, proceedings and book chapters. The present book tries to give in one volume the science governing wafer bonding and associated thinning processes as well as information on technology and applications of wafer bonding. The book is intended for materials scientists and electrical engineers charged or interested in taking advantage of the potential wafer bonding technology offers as well as for graduate students who would like to get familiar with this interdisciplinary field involving surface chemistry, solid state physics, materials science, and electrical engineering.

Over the past decade, we have done extensive research and consulting in the area of wafer bonding at Duke University, Durham, North Carolina, USA, at MPI of Microstructure Physics, Halle, Germany and at Southeast University in Nanjing, China. We would like to express our thanks to the many graduate students, post-docs, visiting scientists, and colleagues who made this research endeavor successful, challenging, and enjoyable. U. Gösele would like to express thanks specifically to two of the post-docs involved in the early wafer bonding research at Duke University, Reinhard Stengl and Volker Lehmann, both now at Siemens Research Laboratories, Munich, Germany. Their unconventional approaches inspired him to remain in this research area and uncover the science involved so that wafer bonding could be moved from the early stages with a touch of "black magic" to the attractive and flexible technology of today. Q.-Y. Tong is grateful for the

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constant support from the Microelectronics Center, Southeast University, China, where he has been enjoying a stimulating collaboration with the wafer bonding research group. He is indebted to his wife, Shi-Hui Kan and their children, Hui and Ling; without their support, understanding, and encouragement the book writing would have not been possible.

Our research over the years was supported by many companies such as Shin-Etsu-Handotai, AT & T, IBM, Texas Instruments, Siemens, Bosch, Ford, Intel, General Motors, Hughes Optical Systems, SOITEC and others, as well as by foundations and research organizations such as NREL, Argonne National Laboratory, Lord Foundation, Mobil Foundation, the German Ministry of Science and Technology, and the German Science Foundation. This support is highly appreciated. Finally, it is our pleasure to appreciate the input of Hisham Massoud from Duke University, who suggested to us to write this book many years ago and exerted gentle pressure to keep our interest in this book project alive.

Because of continuous advances in wafer bonding, the present book is far from being able to cover all aspects and developments in this area. We, nevertheless, hope that it proves to be helpful in advancing the field and that input from the readers will find its way into an extended edition in the near future.

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SELECTED LIST OF SYMBOLS

Symbol	Definition
A	Area, Hamaker constant
a	Lattice constant, radius of a hole
C	Concentration
D	Diffusivity
d	Distance between two wafers
d_{OHi}	Surface density of isolated silanol groups
d_{OHH}	Surface density of associated silanol groups
$d_{\mathrm{Si-F}}$	Surface density of Si—F bonds
$d_{\mathrm{Si-Si}}$	Surface density of Si—Si bonds
E_{total}	Total energy
E_{elas}	Elastic energy
E_{g}	Energy band gap
E_{hi}	Hydrogen bond energy of isolated silanol groups
E_{hH}	Hydrogen bond energy of associated silanol groups
E_{hHF}	Hydrogen bond energy of HF cluster
$E_{\mathrm{Si-O}}$	Silanol bond energy
$E_{\mathrm{Si-Si}}$	Si—Si bond energy
$E_{\mathrm{Si-F}}$	Si—F bond energy
E	Young's modulus, potential energy
E'	Biaxial modulus
e	Electron charge
F	Force
f	Misfit
G	Free energy
σ	Stress, charge density
α	Thermal expansion coefficient, surface tension of a liquid
λ	Wavelength
γ	Specific surface energy

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γ_{eff}^{m}	Effective specific energy in a medium
$\gamma_{s,s}$	Specific energy of bonded state
$\gamma_{m,s}$	Specific energy of debonded state in a medium
θ	Angle
θ_{ws}	Contact angle
ν	Poisson ratio, frequency
μ	Mobility
τ	Shearing stress
H	Height of a gap
h	Height of a dip, Planck constant
I	Moment of inertial
k	Reaction constant
k, k_B	Boltsman constant
l	Distance from a center
L	Crack length
ε	Electric constant
N	Number of fringers
P	Pressure, power, peeling stress
ΔP	Pressure difference
P_w^{eff}	Effective water vapor pressure
P_w^{sat}	Saturated water vapor pressure
ρ	Radius of curvature
R	Gap extension, radius
RT	Room temperature
S	Etching selectivity
TTV	Total thickness variation
t, t_w	Wafer thickness
t_f	Film thickness
t_b	Razor blade thickness
t_s	Critical thickness of separator
u	Small displacement
V	Molar volume
W	Work
W_c	Interaction energy
x	Distance from center

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1

Introduction

1.1 WHAT IS "WAFER BONDING"?

"Wafer bonding" generally refers to a process by which two mirror-polished wafers adhere to each other at room temperature without the application of any macroscopic gluing layer or outside force. Wafer bonding is alternatively known as "direct bonding" and "fusion bonding" or more colloquially as "gluing without glue." Although by no means required, in most cases the wafers involved in actual applications are typical semiconductor wafers consisting of single-crystalline material used in micro- or optoelectronics such as silicon or gallium arsenide. After starting the bonding process by locally applying a slight pressure to adjacent wafers, the bonded area spreads laterally over the whole wafer area, typically in a few seconds, as shown in Fig. 1.1. The bonding achieved at room temperature is usually relatively weak compared to the bonding within metallically, covalently, or ionically bonded solids. Therefore, for many applications, the room temperature bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface. Frequently, one of the two wafers is then thinned to a thickness that depends on the specific application and may be in the range of many microns down to a couple of nanometers. This generic process flow is schematically shown in Fig. 1.2. Modifications of this process flow are quite common for specific applications, (for example, no heating or thinning step may be involved, or the heating and bonding steps may be combined).

This book deals with the underlying science of wafer bonding in many of its variants as well as technological and application questions. In this chapter, a short historical background and an explanation of the growing interest in wafer bonding during the past decade are given. Typical problems and solutions involved in wafer bonding are also mentioned in a general way. Detailed discussions of various topics are contained in the chapters that follow.

1.2 HISTORICAL BACKGROUND

The adhesion of solids to each other has been observed for centuries. In 1792 Desagulier showed that two spheres of lead, when pressed together, strongly

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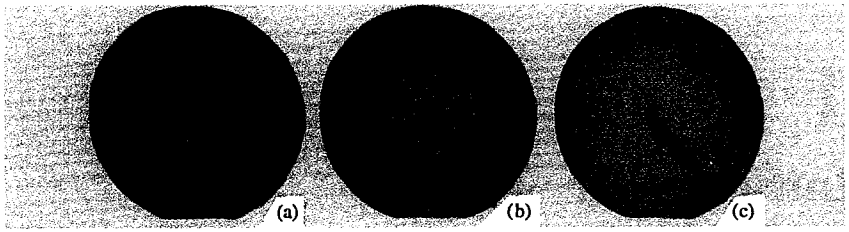

Fig. 1.1 Infrared picture of initiation and propagation of a bonding wave in wafer bonding of 4-in. silicon wafers. (*a*) Local starting of the contact wave, (*b*) extension after about 2 sec, and (*c*) complete bonding after about 5 sec. The radial dark line comes from the tong used to initiate the bonding.

adhere to each other (1). In this case strong plastic deformation is involved, which is not a desirable option for typical, highly brittle semiconductor wafers. The phenomenon that optically polished bulk pieces of metals, used for precision length measurements, stick to each other was observed about a century ago by German craftsmen and termed "Ansprengen" or "jumping into contact." The analogous phenomenon was found also for optically polished glasses such as precision prisms. This effect was and still is used to precisely position optical elements with respect to each other without leaving an optically undesirable space between the elements. The first systematic investigation of room temperature adhesion between two optically polished glass plates was performed in 1936 by Lord Rayleigh (2) who was the first to determine that the interaction energy per area was on the order of 100 mJ/m^2. For a long time, this adhesion phenomena did not have any noticeable technological impact except in the well-known traditional area of optics, and now and then for some isolated specific applications.

The bonding of silicon wafers to sodium-containing glass wafers at elevated temperatures (around 500°C) under the influence of an applied electric field was pioneered by Wallis and Pommerantz in 1969 (3). Ever since it has been used in the area of encapsulation of sensors. This type of bonding, termed "anodic bonding," is restricted to electrically conducting glasses with a thermal expansion coefficient close to that of the semiconductor wafer to be bonded and the presence of mobile ions, such as sodium, which is not desirable for most advanced microelectronic devices. We will, therefore, hardly touch on the subject of anodic bonding, although there are a number of similarities to the direct bonding described in this book. For an overview of anodic bonding, the reader is referred to a review by Obermeier (4). The transfer of a thin gallium arsenide layer to a glass substrate was first performed by "wafer fusion" at elevated temperatures by Antypas and Edgecumbe in 1975. They used an epitaxial, aluminum-rich AlGaAs etch-stop layer to etch off the GaAs substrate but leave a thin GaAs layer to be transferred. This etch-stop concept became essential for many wafer bonding applications (5)

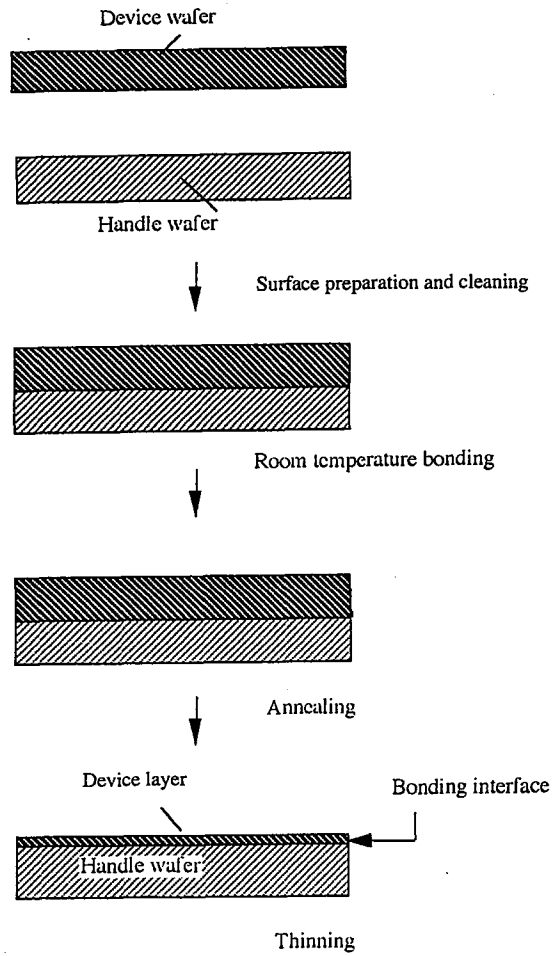

Fig. 1.2 Schematic of wafer-bonding process flow.

Widespread interest in modern wafer bonding techniques was generated by reports on silicon–silicon wafer bonding by two groups (6–8) in 1985–1986 in which the initial bonding of the two wafers at room temperature was followed by a high-temperature bond-strengthening heat treatment. Shimbo and co-workers from Toshiba (6) investigated the bonding of silicon wafers without any thermal oxide between the wafers. Wafer bonding served as a substitute process for the growth of thick epitaxial layers of single-crystalline silicon on silicon for potential applications in power devices (Fig.1.3*a*). In contrast, Lasky from IBM (7, 8) bonded two silicon wafers, with one or both of the wafers being covered by a thermally grown, electrically insulating, silicon dioxide layer (Fig.1.3*b*). One of the silicon wafers was thinned to

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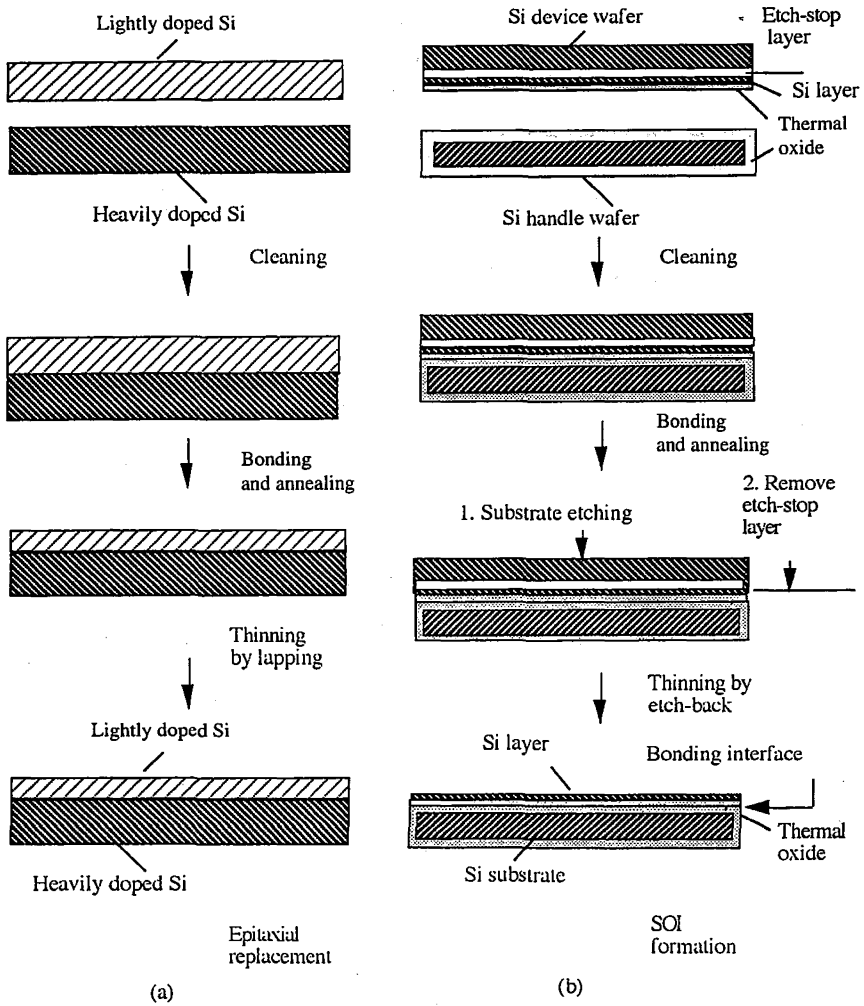

Fig. 1.3 Schematic of bonded and thinned silicon wafers (*a*) for replacement of an epitaxial layer and (*b*) for silicon-on-insulator (SOI) structure.

a few microns, leaving a thin single-crystalline silicon layer on top of an insulator layer (the thermally grown oxide layer), which is on top of a silicon handle wafer. The silicon handle wafer acts mainly as a mechanical support for the thin-layer structure. This silicon-on-insulator (SOI) structure is desirable because of its high resistance against the undesirable side effects of radiation-induced electron-hole pair generation encountered in outer-space experiments or for military purposes. This "radiation hardness," which had originally driven the development of SOI materials including silicon-on-

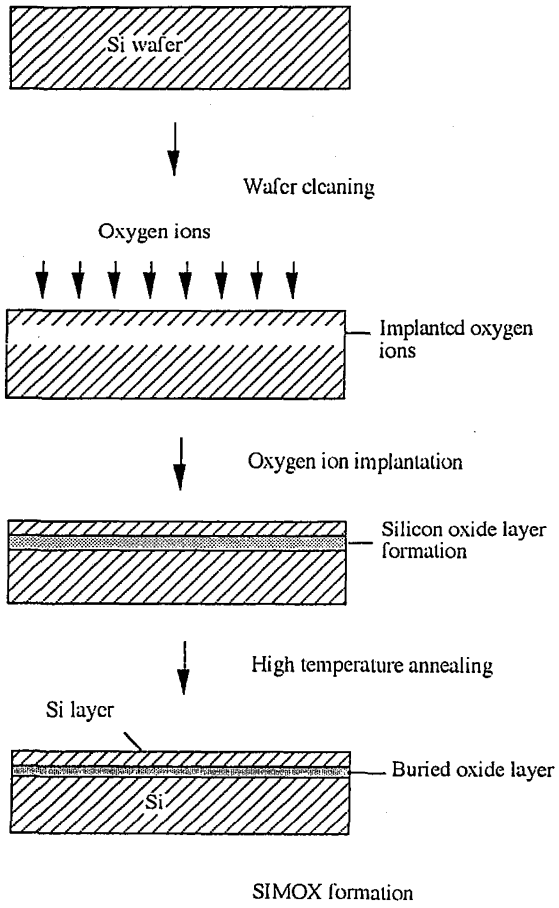

Fig. 1.4 Schematic of SIMOX approach.

sapphire (SOS) and others, is however of minor importance compared to commercial applications based on the ability of SOI materials to allow operation at lower voltages (e.g., for hand-held devices) and a higher packing density of devices as well as the simultaneous use of low- and high-voltage devices on one chip (9). At the time of Lasky's fabrication of SOI material by silicon wafer bonding and thinning, the main approach to generate equivalent silicon structures was based on high-energy, high-dose implantation of oxygen ions into silicon. At temperatures close to the melting point of silicon, the implanted oxygen agglomerates in the form of a continuous buried layer of silicon dioxide. This so-called Separation by IMplanted OXygen (SIMOX) (10, 11) approach (Fig. 1.4) left a high density of implantation-induced dislocations in the silicon layer and, in addition, was very expensive. At the

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time it was hoped that silicon wafer bonding and thinning would constitute a less expensive and technologically much simpler approach to fabricate SOI layers with the added advantage that the silicon layer would be as good as the bulk silicon material since no implantation damage was involved.

Parallel to the electronics-related work on silicon wafer bonding at Toshiba and IBM, in 1988 Petersen and Barth (12) pioneered the use of silicon wafer bonding for pressure sensors, in which at least one of the silicon wafers was structured containing holes or cavities (Fig. 1.5). The process was termed "fusion bonding" and actually went into production.

Although the work of Shimbo et al. (6) and Lasky (7, 8) generated a lot of interest and follow-up research, it did not immediately lead to viable products in the area of microelectronics, because the difficulties associated with wafer bonding were also noticed quickly. The success of bonding depends critically on surface properties, chemical cleaning and conditioning of the surfaces, and to a certain extent on the atmosphere (air, humidity, vacuum) in which the initial bonding is performed. Particles that remain attached to the surfaces to be bonded locally prevent bonding and lead to unbonded areas (termed "interface bubbles" or "voids") with lateral extensions of many millimeters for particles in the micron range. Frequently, interface bubbles are even generated during the heat-treatment step and are not related to particles. Uniform thinning of one of the wafers was a major obstacle. Based on these difficulties, wafer bonding was characterized as "black magic" and as a technology that is not easily manufacturable. Fortunately, during the last decade, the science behind wafer bonding has been investigated thoroughly and most of the difficulties associated with silicon wafer bonding have been ironed out, so that little if any black magic remains, as documented in many review articles (13–22), the proceedings of various wafer bonding conferences (23–26), and a special journal issue on wafer bonding (27). The recent announcement (August 1988) by IBM of a new microchip breakthrough using the SOI technology to boost the performance of computers and communication systems by 35% clearly demonstrates that SOI is becoming the mainstream technology for the next generation of VLSI industry. Not only are bonded SOI wafers now commercially available from a variety of vendors, but a range of other possible applications has opened up, for example, in micromechanics (14, 16, 21) and in optoelectronics (28–30) involving the bonding of III-V compound wafers at elevated temperatures in hydrogen. This book presents not only the science behind wafer bonding technology, but also information on the more mundane aspects of wafer bonding such as cleaning, etching, and thinning procedures. The book touches upon some mainstream applications as well as some approaches that are presently in the research stage or are rather esoteric in nature. In the following section, a short overview of why wafer bonding is such an interesting approach for materials combinations in general and what basic opportunities wafer bonding offers is given.

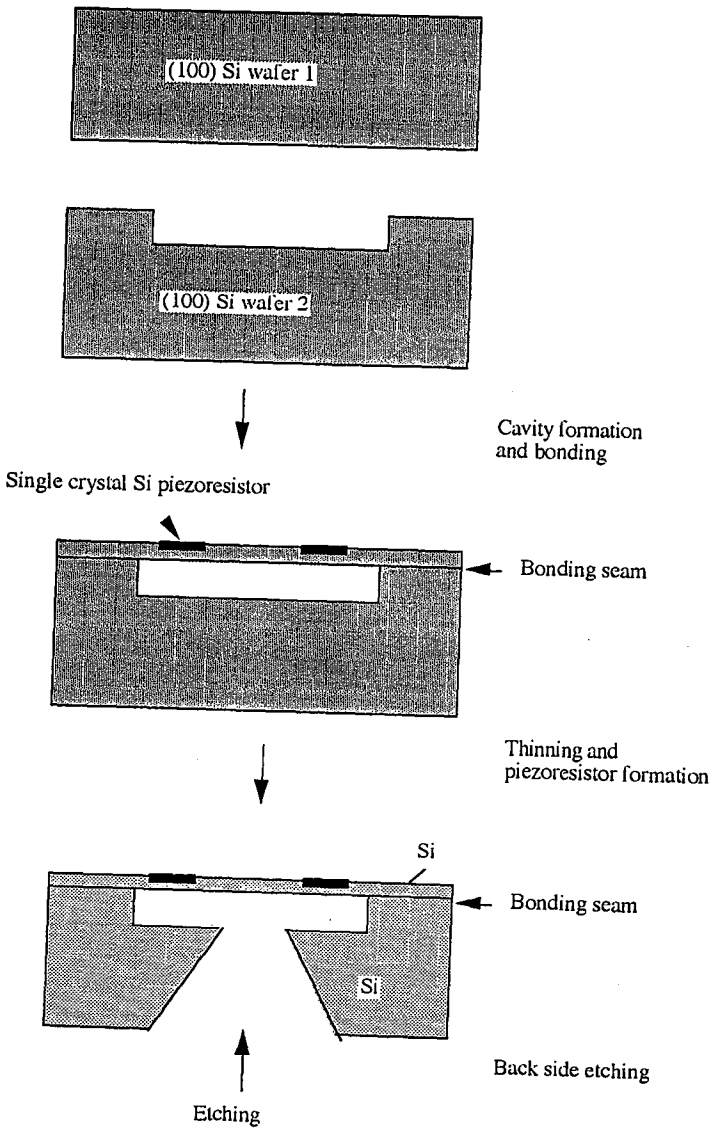

Fig. 1.5 Schematic of pressure sensor fabricated by wafer bonding.

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1.3 WAFER BONDING: ADVANTAGES AND OPPORTUNITIES

After the discussion of the early difficulties associated with wafer bonding in the previous section, a question arises as to the benefits of applying wafer bonding as compared to other methods of joining solids or depositing or growing thin layers on appropriate substrates. Obviously, wafer bonding requires mirror-polished surfaces, whereas most other methods of joining bulk materials, such as gluing, soldering, or welding, can tolerate fairly rough surfaces. For most of the technical applications of wafer bonding, the requirement of mirror-polished surfaces is not a major obstacle, basically for three reasons:

1. As long as comparatively thin wafers are used (in the range below about a millimeter in thickness), the wafers can relatively easily conform to each other and adapt a possible small bow by elastic deformation during bonding. Therefore, in contrast to the expensive "optical polishing" necessary for bonding of bulk pieces (which requires a flatness over the entire surface within a quarter of an optical wavelength, which would limit surface variations to about 100 nm over the whole surface), only "mirror polishing" with much less stringent requirements is required (as described in detail in Chapter 3).
2. Most of the wafers used, such as silicon or gallium arsenide wafers, come in mirror-polished form for reasons not associated with bonding, so that frequently no additional polishing step is required for the wafer-bonding process.
3. Even if the wafer surfaces contain an unfavorable surface topography from previous processing steps, so that polishing is required, this is not a major obstacle because of the wide availability of chemomechanical-polishing (CMP) equipment in any modern microelectronics facility (owing to the steadily increasing need of planarization processes in device fabrication).

Obviously, wafer bonding, if performed properly, is a convenient joining technology which involves no macroscopical gluing or soldering layer and, consequently, no harmful contamination. It allows the joined wafers (if not prohibited by large differences in thermal expansion coefficients of the bonded wafers) to be heated to temperatures well above the thermal stability of conventional organic glues. It works not only for silicon but for many different materials provided they can be polished properly, as demonstrated for room-temperature bonding by Haisma et al. (20) and shown in Table 1.1. Typical wafer-bonding procedures are also fully compatible with microelectronics processing technologies and can thus easily be integrated using equipment already available for microelectronic or micromechanic device manufacturing.

Joining of whole blank or structured wafers is just one of the more mundane applications. The more exciting possibility, which wafer bonding

TABLE 1.1 Experimental Results of Bondability of Various Material Combinations (Bonding Material A to Material B)[a]

Material A	Material B		
	Quartz Glass	Hydrophilic Si	Material B = Material A
Metal			
Ta (poly* layer on Si)	++	++	++
Ti (poly* layer on Si)	ok	ok	–
W (poly* layer on Si)	Local weak bond under pressure	Local weak bond under pressure	–
Cu poly	+	+	N/A
Semimetal	+	+	N/A
Bi poly			
Semiconductor	++	++	++
Si			
Ge	++	++	++
B (poly* layer on Si)	+	+	+
GaAs	++	++	++
InP	++	++	++
Superconductor	+	+	–
$YBa_2Cu_3O_{7-8}$ (polycrystalline)			
Oxide			
$SrTiO_3$	++	++	+
$ZrO_2Y_2O_3$	++	++	+
Ferroelectric			
$BaTiO_3$ (poly*)	+	+	+
$LiNbO_3$	+	+	+
Fluoride			
BaF_2	++	+	+
CeF_3 (on glass)	+	+	+
Nitride			
Si_3N_4 (poly* layer on Si)	+	+	–
AlN (polycrystalline)	+	+	–
Carbide			
B_4C (polycrystalline)	+	+	N/A
Diamond	+	+	Very weak
Insulator			
ZnSe (polycrystalline)	++	++	++

[a]*: Polycrystalline; ++: very good; +: good; –: no bond; N/A: not investigated.

offers, is the fabrication of single crystalline layers of material A on almost any kind of appropriately polished substrate B, even if the substrate is amorphous, polycrystalline, or single crystalline but of a very different lattice constant or crystallographic orientation. Usually, a single crystalline layer can be grown only on top of a single crystalline substrate of the same material (i.e., homoepitaxial growth, silicon on silicon) or a different material which

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has a lattice constant closely matching that of the desired layer to be grown (i.e., heteroepitaxial growth, AlAs on GaAs). If the lattice constants of layer and substrate material differ by a percent or more, the layer will first grow elastically strained, and then, after exceeding a critical thickness, will introduce so-called misfit dislocations at the interface. Because these dislocations generally nucleate at the surface and glide to the interface, these films will contain a high density of dislocations threading through the grown film, thus rendering the film unsuitable for many electronic or optoelectronic applications.

Based on this knowledge of epitaxial growth of single crystalline layers, materials scientists, solid state physicists, and electrical engineers developing solid-state devices have been trained to accept that single crystalline layers generally cannot be fabricated on amorphous, polycrystalline, or single crystalline material that is grossly lattice-mismatched or on the same crystalline material but with an unrelated lattice orientation. Wafer bonding, as described in this book, in many cases allows one to overcome these restrictions, but not in the form of layer growth but rather by transferring a thin single crystalline layer from a first substrate to a second substrate (amorphous, polycrystalline, or nonfitting crystalline). Thus, wafer bonding opens up the possibility of preparing combinations involving single crystalline materials excluded previously because of the lack of a proper crystallographic relationship. Such possible applications are astonishingly diverse and apparently limited more by our lack of imagination than by technological constraints. Two recent developments involving wafer bonding demonstrate this versatility.

The first development concerns the thinning technology utilized after wafer bonding occurs. It had been commonly assumed that thinning of one of the wafers would be associated with the loss of most of this wafer by grinding, lapping, polishing, or etching away everything except the layer to be transferred. The "smart-cut" process recently developed by Bruel (31, 32) has demonstrated that this assumption is not necessarily true. The process flow is schematically shown in Fig. 1.6. In this process, hydrogen ions are implanted before bonding into one of the wafers from which a thin layer should be transferred. Then the wafers are bonded and heated (in the case of silicon to about 500°C), which leads to the development and growth of hydrogen-induced microcracks parallel to the bonding interface. Finally, by growth of the microcracks, the splitting of a thin layer away from the implanted substrate occurs. The transferred layer shows an excellent thickness uniformity. Only slight touch polishing is required to achieve a surface equivalent to typical silicon surfaces. The split-off wafer has typically lost only a layer on the order of 1 μm from a thickness of 500–1000 μm and can thus be used further after repolishing. Repeated application of this process might well lead to major advances in the fabrication of three-dimensionally stacked electronic devices. Presently the process only works for silicon, germanium, diamond, gallium arsenide (33), and silicon carbide (34, 35); it is quite

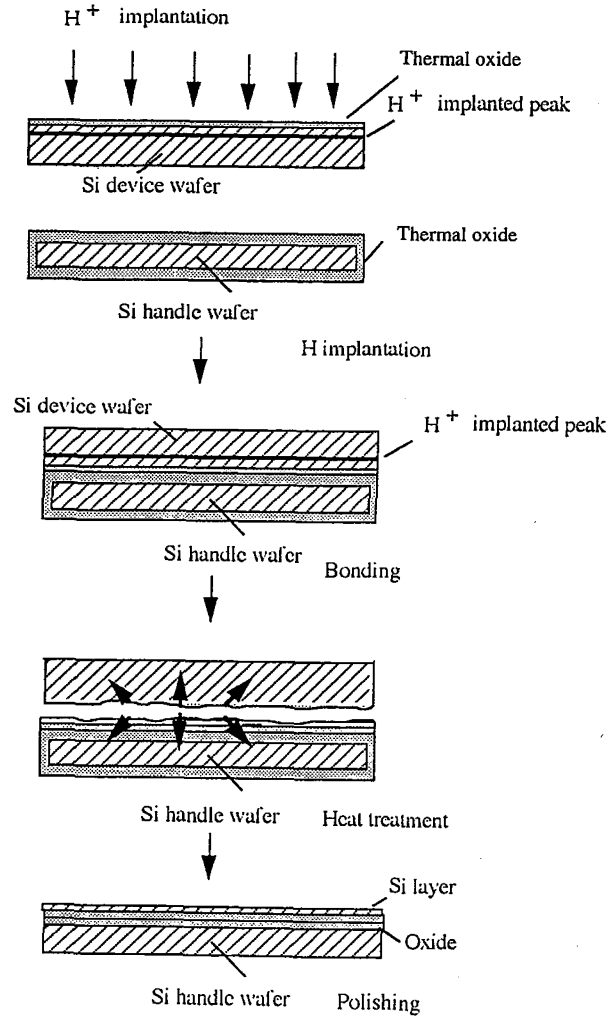

Fig. 1.6 Schematic of different steps in the "smart-cut" process.

possible that further research might enable the splitting of other materials such as ferroelectrics and oxides.

The second astounding development concerns the application of twist wafer bonding to generate a so-called "compliant" substrate. A compliant substrate allows the heteroepitaxial growth of materials with a large misfit in their lattice constants with a drastically reduced density of threading dislocations, even if the heteroepitaxial layer exceeds many times the critical

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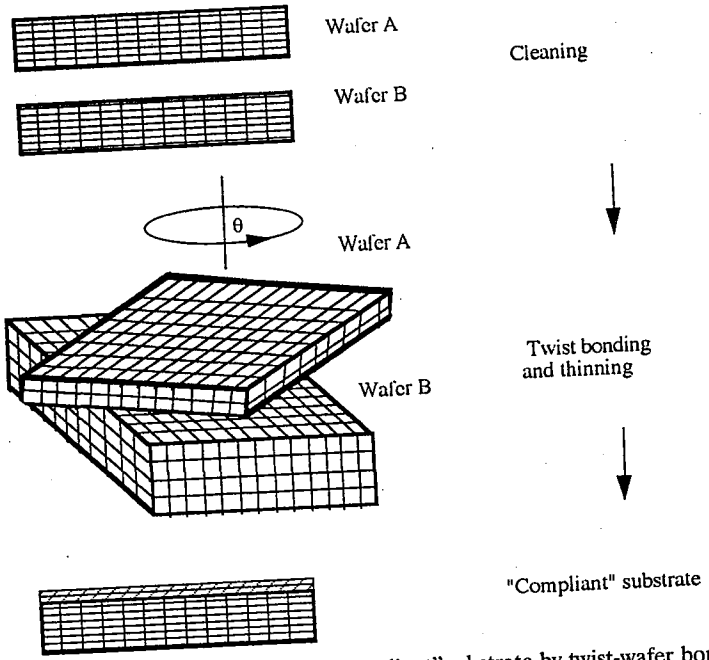

Fig. 1.7 Schematic of fabrication of "compliant" substrate by twist-wafer bonding.

thickness (36) for the generation of misfit dislocations. The basic idea is that misfit dislocation formation could be prevented if the heteroepitaxial growth occurred on a basically free-standing thin film which is below its critical thickness (37, 38). Although the validity of this concept has been shown experimentally (39), it is not practical to work with free-standing films of a thickness on the order of a few nanometers. Rather, it would be desirable to connect this film to a substrate in such a way that it can easily shift laterally with respect to the substrate. One approach to fabricate such a "compliant" substrate involves wafer bonding. The idea here is to generate a weakly bonded zone by the interface between two wafers bonded under a large twist angle such as 10–30° (40, 41). The resulting structure is schematically shown in Fig. 1.7. The system investigated first was that of a (100) GaAs layer twist bonded on a (100) GaAs substrate. The etch-stop method used was that suggested by Antypas and Edgecumbe in 1975 (5) involving a thin etch-stop layer of GaAlAs with a sufficiently high Al concentration grown epitaxially on a GaAs substrate, followed by a second 3- to 10-nm thick epitaxial layer of GaAs to be transferred. The bonding was performed under high mechanical compression and hydrogen flow at temperatures over 500°C. Heteroepitaxial growth of different materials ranging from $In_{0.35}Ga_{0.65}P$ (40) to InSb (41) (with misfits ranging from about 1 to 15%, respectively) well above their

respective critical thickness did not show any threading dislocations in cross-sectional electron micrographs. It is not yet understood how "compliant" substrates really work (42). Nevertheless, if actually reproducible, this approach of twist wafer bonding could be extended to Si/Si bonding or any combination of appropriate materials and allow heteroepitaxial growth of misfitting material without the usual drawback of threading dislocations which are detrimental in many electronic or optoelectronic applications.

In the rest of the book, various aspects of wafer bonding are considered in some detail. Chapter 2 gives a fairly general discussion of interactions between surfaces; Chapter 3 addresses the influence of particles and surface steps; and Chapters 4 and 5 thoroughly discuss surface preparation, room-temperature bonding procedures, and thermal treatments. Chapter 6 is devoted to presently available thinning procedures and Chapter 7 to the electrical properties of bonding interfaces. Chapter 8 deals with stresses in bonded wafers in general and Chapter 9 with bonding of dissimilar materials for which the occurrence of mechanical stresses due to different thermal expansion coefficients is of major concern. Chapter 10 concentrates on the bonding of structured wafers as important mostly for micromechanical applications. Chapters 11 and 12 deal with mainstream and emerging applications, respectively.

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2

Basics of Interactions Between Flat Surfaces

2.1 INTERACTION FORCES BETWEEN SURFACES

The first step in the wafer direct bonding process is bonding (contacting) at room temperature. Since there is no adhesive or external electrical field involved in the wafer bonding process, surface forces between the wafers determine the adhesion. Therefore, a knowledge of surface forces and the resulting interaction between mating wafers is necessary to understand the direct bonding process.

A number of interactions occur between two surfaces. Depending on the environmental conditions (e.g., vacuum, vapors, liquids), different forces may be dominating. Let us consider the interfaces of identical or dissimilar extended solids which are close together in vacuum, in the presence of water vapor, or in water. There are mainly three types of surface forces acting between two solids in sufficient proximity: (1) van der Waals attraction forces, (2) electrostatic Coulombic forces, and (3) capillary forces. Figure 2.1 shows schematically these three types of interactions.

2.1.1 Van der Waals Interactions

It is well known that electrically polarized or at least polarizable (identical or different) atoms or molecules are attracted to each other by so-called van der Waals interactions. Van der Waals forces originate from atomic and molecular electric dipoles whose orientations are correlated in such a way that they attract each other. Usually one distinguishes between the following three types of van der Waals forces: (1) the dipole–dipole force between two polar molecules, (2) the dipole-induced force between a polar and a nonpolar molecule, and (3) the dispersion force between two nonpolar molecules resulting from the nonzero average value of the square of the temporary dipole moment due to charge distribution fluctuations (1, 2). It should be noted that in some disciplines the term "van der Waals force" refers only to the dispersion force. The three van der Waals forces are all considered to be long ranged on an atomic scale, but short ranged on a macroscopic scale. The

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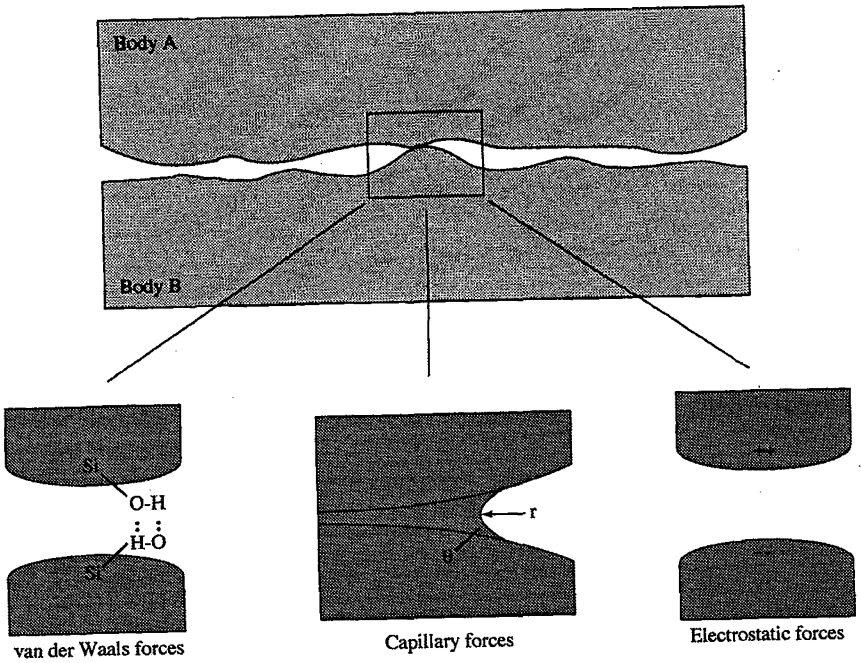

Fig. 2.1 Schematic of three types of interactions between two solids.

three van der Waals forces, F_v, diminish rapidly as the distance d between two molecules increases (1):

$$F_v \propto d^{-7} \tag{2.1}$$

The force acting between two macroscopic bodies is a result of many-body effects. In general, the force between any two atoms is influenced by other nearby atoms. Therefore, the force between two surfaces cannot be calculated accurately by a simple pair-wise addition of the forces between every pair of atoms. However, the pair-wise summation of all of the interatomic forces acting between all of the atoms of the two bodies plus any additional medium can be considered as a first approximation of the force acting between the two bodies. The surface force F_v between two bodies has much longer range and decreases with the inverse third or second power of the surface separation d depending on the geometry of the bodies (2). The dispersion van der Waals force (per unit area) between two flat plates is of the form

$$F_v = \frac{A}{6\pi d^3} \tag{2.2}$$

where A is the Hamaker constant and d is the separation of their surfaces (3). The dispersion van der Waals force between two spheres of equal radius R is given by

$$F_v = \frac{AR}{6d^2} \tag{2.3}$$

For bodies 1 and 2 separated by a medium 3, if the three materials have the same ultraviolet relaxation frequency ω_0, the Hamaker constant is approximately given by (2)

$$A_{132} = \frac{3kT}{2} \sum_{m=0}^{\infty}{}' \frac{\left(n_1^2 - n_3^2\right)\left(n_2^2 - n_3^2\right)}{\left(n_1^2 + n_3^2 + 2b^2m^2\right)\left(n_2^2 + n_3^2 + 2b^2m^2\right)} \tag{2.4}$$

where

$$b = \frac{2\pi kT}{(h/2\pi)\,\omega_0} \tag{2.5}$$

and k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, n_i is the refractive index of material i, and the prime on the summation indicates that half weight is given to the $m = 0$ term. For a thorough treatment of the calculation of Hamaker constants and a computation of values for different materials contribution we refer to the book by Israelachvili (4).

The Hamaker constant is 6.5×10^{-20} J for silica–air–silica, 8.3×10^{-21} J for silica–water–silica (5), and 6.5×10^{-20} J for sapphire–water–sapphire (6).

Figure 2.2 shows a schematic diagram of an equilibrium crack interface where d_0 is the surface separation at contact (in a crystal it represents the lattice spacing). Ignoring the curvature of the surfaces, we use Eq. (2.2) to

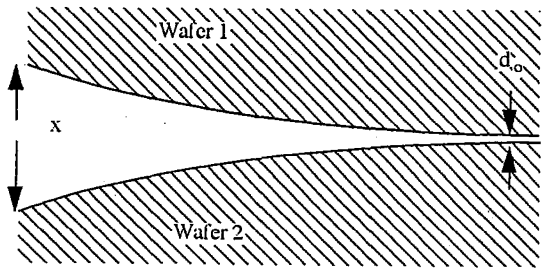

Fig. 2.2 Schematic of a crack interface of two surfaces in close proximity.

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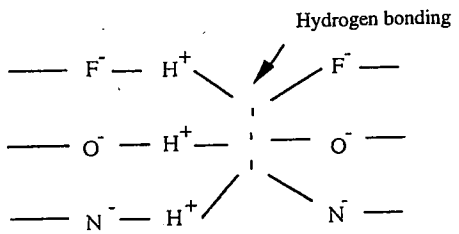

Fig. 2.3 Schematic of hydrogen bonding.

calculate the van der Waals specific interaction energy W_v per unit area:

$$W_v = \int_{d_0}^{\infty} \frac{A}{6\pi x^3} dx = \frac{A}{12\pi d_0^2} \tag{2.6}$$

The corresponding Hamaker constant A should be used depending on the medium, if any, in which contact occurs.

An especially strong form of dipole–dipole attraction is hydrogen bonding in which the hydrogen atom in a polar molecule interacts with an electronegative atom of either an adjacent molecule or the same molecule. A hydrogen atom can participate in a hydrogen bond if it is bonded to oxygen, nitrogen, or fluorine because H—F, H—O, and H—N bonds are strongly polarized, leaving the hydrogen atom with a partial positive charge. As shown in Fig. 2.3, this electrophilic hydrogen has a strong affinity for nonbonding electrons so that it can form intermolecular attachments with an electronegative atom such as oxygen, nitrogen, or fluorine. Water is a polarized molecule consisting of hydrogen as well as oxygen, which allows hydrogen bonding to form between water molecules themselves. Therefore, if water is present, the linkage of water molecules may bridge two interacting atoms or molecules (7). In this way, a "long-range" intermolecular force can be realized.

2.1.2 Electrostatic (Coulombic) Forces

When two uncharged surfaces come close to each other in vacuum, van der Waals forces between the two solid bodies themselves are the only forces which determine their adhesion. If the two surfaces are in contact with vapors, either chemical or physical adsorption, or both, can take place. The interaction is then mainly determined by van der Waals forces between the adsorbed layers. On the other hand, direct Coulombic forces (electrostatic forces) may also be involved if the surfaces become macroscopically charged by either adsorbing or desorbing electrons or ions. The direct Coulombic forces are generally strong and are usually the dominating interface forces whenever charging occurs. However, the Coulombic forces usually become

unimportant when water or water vapor are present in the environment, which partly compensates the charges on the surfaces.

For ionic materials, the chemical bonds themselves involve oppositely charged ions. When an ionic material is cleaved, ions with opposite charges may attach to one or the other surface. The two surfaces may still have no macroscopic charge since the ions with either charge are distributed randomly with an equal charge density σ. But microscopically there is an electrostatic attraction between the opposing surfaces with charge domains of linear dimension l. The force per unit area between the two surfaces F_i can be written as (3)

$$F_i = \frac{32\sigma^2}{\pi^2 \varepsilon \varepsilon_0} \exp\left(-\frac{\sqrt{2}\,\pi d}{l}\right) \tag{2.7}$$

where ε is the dielectric constant of the intervening medium and ε_0 is the permittivity of free space. It should be noted that in vapors the surfaces are usually terminated by adsorbates which determine the interactions between the two surfaces. A vapor may also condense in a narrow gap of the two surfaces that can effectively screen the electrostatic interaction.

When two dissimilar surfaces are in good microscopic contact, a transfer of charge from one surface to another usually occurs because of Fermi level effects (chemical equilibrium). Transferred charge densities in the range of 5 to 10 mC/cm^2 have been reported between silica and mica surfaces with the silica being negatively charged relative to the mica. The charge transfer results in a strong electrostatic attraction between the surfaces on the order of 10 MPa with a range of several micrometers (3) and is the dominant mechanism for adhesion at relative humidity less than 5%.

When two bodies are in a polar liquid such as water or aqueous electrolyte solution, the surfaces generally acquire a charge due to chemical equilibrium (Fermi level effects) with the contacting solution. Ions of opposite charge in the solution are attracted to the surfaces. The surface charge together with the layer of opposite charge form an "electrical double layer" (8). The thickness of the double layer depends on the ion concentrations in solution. Similar or identical bodies have the same charge, leading to a repulsive force between them when their double layers are interacting. The magnitude of the forces is significantly lower than that of direct Coulombic forces owing to a screening effect of the counter-ions. Therefore, the two forces acting between two surfaces in a polar liquid are the attractive van der Waals force and the repulsive electrostatic double-layer force.

Figure 2.4 shows schematically a typical potential energy E as a function of the surface separation between two flat surfaces in a high-concentration polar liquid (8). The double-layer potential is repulsive and positive, and decreases roughly exponentially as the surface separation d increases. The van der Waals potential energy E_v is negative and, according to Eq. (2.6), is

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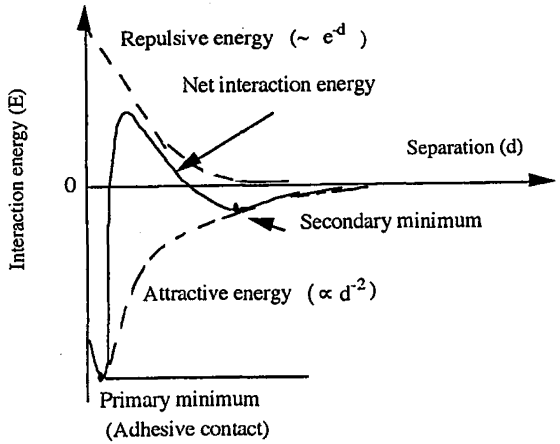

Fig. 2.4 (*a*) Interaction potential energy as a function of surface separation distance between two flat surfaces in an aqueous electrolyte solution and (*b*) the derivative of potential energy, that is, the corresponding interaction forces.

related to the surface separation d by

$$E_v \propto A/d^2 \tag{2.8}$$

for flat plates per unit area. For the interaction energy between two spheres,

$$E_v \propto A/t \tag{2.9}$$

is valid. The net potential energy of the system is the sum of the two and has a primary minimum where the two surfaces are at contact and adhere strongly. If the ion concentration of the solution is high, the double-layer potential may decay so rapidly that the van der Waals attraction is still significant at a separation outside the range of (double-layer) repulsion. In this case, a secondary energy minimum appears where the adhesion is much weaker and reversible.

2.1.3 Capillary Forces

When two surfaces are in a vapor which can condense on the surfaces and whose liquid has a contact angle with the surfaces of less than 90°, if the narrow gap between the two surfaces is smaller than a critical distance, it can be filled by a capillary-condensed liquid, resulting in an additional capillary attractive force. The critical distance depends on the radius of curvature of the condensed liquid, as discussed below. Figure 2.5 is a schematic showing capillary condensation of liquid around asperity contacts. The curvature $1/r$ of the cylindrical meniscus of the liquid introduces a Laplace pressure p_{Lap} on the liquid

$$p_{Lap} = \frac{\alpha}{r} \tag{2.10}$$

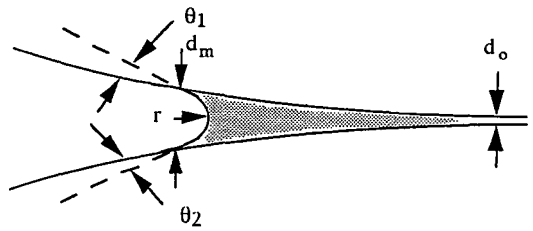

Fig. 2.5 Schematic of capillary condensation around an asperity contact.

where α is the surface tension of the liquid (72 mJ/m^2 for water). The radius of curvature r is given by the Kelvin equation

$$r = \frac{\alpha V}{kT \ln (p_s/p)} \tag{2.11}$$

where V is the molar volume of the liquid (V = Avogadro's constant $N_A \times$ molecular volume, $6.022 \times 10^{23} \times 0.030$ nm^3 for water), k is the Boltzmann constant, T is the absolute temperature, and p/p_s is the relative vapor pressure of the liquid species. If the liquid is water, the radius of curvature r can be written as

$$r = \frac{\alpha V}{kT \ln (1/\mathrm{RH})} \tag{2.12}$$

where RH is the relative humidity (between 0 and 1). In completely dry air, $r = 0$ and in saturated water vapor, $r = \infty$. In air with RH of 10 or 50%, $r = 5$ or 16 Å, respectively.

In order to give a force pulling the two surfaces together, the Laplace pressure must be negative, meaning that the surface of the meniscus should be concave (contact angles θ_1 and θ_2 are less than 90°). If we ignore the curvature of the two surfaces, the separation of the two surfaces is given by

$$d_m = r(\cos\theta_1 + \cos\theta_2) + d_0 \tag{2.13}$$

d_0 is the surface separation at contact. This is the critical distance between the two surfaces below which a liquid bridge will form between the two surfaces.

For two flat surfaces in contact over an area A, the capillary force is $A\alpha/r$. The interaction energy, W_c, originating from the capillary force for an equilibrium crack shown in Fig. 2.5 can be obtained as the work to separate the two surfaces against the Laplace pressure (3):

$$W_c = \int_{d_o}^{d_m} p_{Lap}\, dx \tag{2.14}$$

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Using Eqs. (2.10) and (2.13) we get

$$W_c = \alpha(\cos\theta_1 + \cos\theta_2) \tag{2.15}$$

A typical value for two flat and hydrophilic silica surfaces interacting via a water layer is at most 144 mJ/m^2 under the assumption of $\theta_1 = \theta_2 = 5°$.

The capillary force between two contacting spheres of radius R with a small condensed meniscus is approximately expressed as (9)

$$F_c = 2\pi R\alpha(\cos\theta_1 + \cos\theta_2) \tag{2.16}$$

Since most surfaces are not perfectly flat and smooth, under dry conditions only a few isolated asperities are in true contact between two surfaces. The condensed liquid increases the contact area remarkably, resulting in a significant increase in adhesion. We mention specifically that the interaction energy between adsorbed water layers on two opposite surfaces is of the same order (100 mJ/m^2) as the adhesion energy due to capillary forces resulting from a liquid water layer because physically it is based on the same type of molecular interactions. The major difference is associated with the fact that the adsorbed water molecules are attached to the surfaces and can withstand considerable shear forces without the two surfaces sliding against each other, whereas for thin water layer sliding will occur.

2.1.4 Very Short-Ranged Forces

When atoms from opposing surfaces get very close to each other (< 1–2 Å), additional strong short-ranged forces become effective as a result of the overlap of electron clouds. This can result in covalent and metallic chemical bonds. In these cases, the electrons function as a "glue" (10). Bonding under ultrahigh vacuum conditions is based on these interactions. At even smaller separations, the electrostatic repulsion between the nuclei (Born repulsion) sets in and the balance between these repulsive and the attractive forces determines the equilibrium distance.

2.2 SURFACE ENERGIES, BOND STRENGTHS, AND THEIR MEASUREMENT

2.2.1 Interaction Energy and Surface Energy

The interaction energy of a bonded pair per unit area can be defined as the work W associated with the mechanical separation of a bonded pair of surface 1 and surface 2 from their original distance at contact d_0 to infinity in

adiabatic conditions:

$$W = \gamma_1 + \gamma_2 = \int_{d_0}^{\infty} F(d)\,dx \tag{2.17}$$

where γ_1 and γ_2 are surface energies of surface 1 and surface 2 at the moment of their separation, and $F(d)$ is the attraction force per unit area as a function of separation. The interaction energy of a bonded pair is sometimes termed "bonding energy" and is used to represent the strength of the bond. It can be considered as equivalent to the fracture energy of monolithic materials. In this book, the energy associated with the formation of a unit area of the surface has been termed surface energy, which is employed to characterize the energy of the bond of a pair. If the two bonding wafers are made of the same materials, we have $\gamma_1 = \gamma_2 = \gamma$. The definition in Eq. (2.17) implies that the process is reversible. However, in a certain medium, the fresh separated surface may adsorb species from the ambient to lower its energy. Moreover, reconstruction may also take place on the separated surfaces. The surface energy will then decrease and gradually reach a stable value $\gamma_{m,s}$. Obviously, the final surface energy cannot represent the original interaction energy and the process becomes irreversible. Changing the surface energy of newly created surfaces by debonding in a certain medium is discussed in more detail in Chapter 4.

2.2.2 Surface Energy Measurement: Crack-Opening and Related Methods

The most convenient method of measuring the surface energy of bonded pairs is the crack-opening method (11, 12) schematically shown in Fig. 2.6. This technique is based on the equilibrium of elastic forces of the bent separated part of a pair and bonding forces at the crack tip (13).

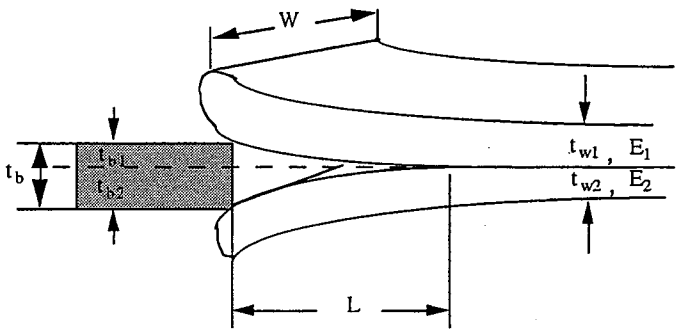

Fig. 2.6 Schematic diagram of the crack-opening method.

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Let us consider a bonded pair consisting of two beams of dissimilar materials with the same width w. When inserting a separating material such as a razor blade with a thickness of t_b, the two bent parts of the pair generate two different elastic energies, $E_{elas\,1}$ and $E_{elas\,2}$, which are functions of the respective Young's modulus, E, and thickness, t_w. The inserted blade also creates two new surfaces of area Lw where L is the equilibrium crack length. The total energy is given by

$$E_{total} = E_{elas\,1} + E_{elas\,2} + (\gamma_1 + \gamma_2)Lw \tag{2.18}$$

where γ_1 and γ_2 are the respective specific surface energies of the two newly generated surfaces. Equation (2.18) is based on the assumption that no plastic deformation is involved in the crack-opening process. To obtain the equilibrium between the elastic forces and the bonding force of the pair, the first derivative of E_{total} with respect to the crack length L must be zero:

$$\frac{\partial E_{total}}{\partial L} = 0 \tag{2.19}$$

The elastic energies $E_{elas,\,i}$, (where i = 1,2) can be expressed as (14)

$$E_{elas,\,i} = \frac{F_i^2 L^3}{6E_i I_i} \tag{2.20}$$

where the bending force F_i is given by

$$F_i = \frac{E_i w t_{wi}^3 t_{bi}}{4L^3} \tag{2.21}$$

and the moment of inertia, I, of the beam is given by

$$I_i = \frac{t_{wi}^3 w}{12} \tag{2.22}$$

Substituting Eqs. (2.20)–(2.22) into Eq. (2.18), the total energy can be obtained as

$$E_{total} = \frac{wE_1 t_{w1}^3 t_{b1}^2 + wE_2 t_{w2}^3 t_{b2}^2}{8L^3} + (\gamma_1 + \gamma_2)Lw \tag{2.23}$$

Using Eq. (2.19), the summation of the surface energies of the two surfaces is given by

$$(\gamma_1 + \gamma_1) = \frac{3\left(E_1 t_{w1}^3 t_{b1}^2 + E_2 t_{w2}^3 t_{b2}^2\right)}{8L^4} \tag{2.24}$$

Since the thickness of the razor blade is $t_b = t_{b1} + t_{b2}$; t_{b1} can be replaced by $(t_b - t_{b2})$ in Eqs. (2.23) and (2.24), and then Eq. (2.24) is substituted back into Eq. (2.23) to express the total energy in terms of t_{b2} only:

$$E_{total} = \frac{wE_1 t_{w1}^3 (t_b - t_{b2})^2 + wE_2 t_{w2}^3 t_{b2}^2}{2L^3} \tag{2.25}$$

To obtain the values t_{b1} and t_{b2}, the first derivative of the total energy with respect to t_{b2} is set to zero. From this procedure, one gets

$$t_{b1} = \frac{t_b E_2 t_{w2}^3}{E_1 t_{w1}^3 + E_2 t_{w2}^3} \tag{2.26}$$

$$t_{b2} = \frac{t_b E_1 t_{w1}^3}{E_1 t_{w1}^3 + E_2 t_{w2}^3} \tag{2.27}$$

and finally, after substituting Eqs. (2.26) and (2.27) into Eq. (2.24),

$$(\gamma_1 + \gamma_2) = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{8L^4\left(E_1 t_{w1}^3 + E_2 t_{w2}^3\right)} \tag{2.28}$$

The average surface energy γ in the case of asymmetrical bending due to dissimilar materials and different thicknesses involved in a bonded pair can be expressed as

$$\gamma = \frac{1}{2}(\gamma_1 + \gamma_2) = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{16L^4\left(E_1 t_{w1}^3 + E_2 t_{w2}^3\right)} \tag{2.29}$$

In the case of bonded pairs with identical wafers (i.e., $t_{b1} = t_{b2}$ and $E_1 = E_2 = E$), Eq. (2.29) becomes

$$\gamma = \frac{3Et_w^3 t_b^2}{32L^4} \tag{2.30}$$

When $t_{w2} \gg t_{w1}$ and $E_1 = E_2 = E$, which corresponds to the case that only one wafer of the pair is actually bent, the surface energy is expressed as

$$\gamma = \frac{3Et_{w1}^3 t_b^2}{16L^4} \tag{2.31}$$

It is worth mentioning that for the bonding of structured wafers in which only area A_b of the total surface area A_0 is available for bonding, γ of the actually bonded surface area is related to the crack length L by multiplying

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TABLE 2.1 Formulas for Surface Energy in Various Configurations

Configuration	Formula of Surface Energy
Pairs of identical wafers	$\gamma = \dfrac{3Et_w^3t_b^2}{32L^4}$
Pairs of dissimilar wafers	$(\gamma_1 + \gamma_2) = \dfrac{3t_b^2E_1t_{w1}^3E_2t_{w2}^3}{8L^4(E_1t_{w1}^3 + E_2t_{w2}^3)}$
Pairs with one wafer very thick ($t_{w2} \gg t_{w1}$)	$\gamma = \dfrac{3Et_{w1}^3t_b^2}{16L^4}$

the right-hand side of the approximate formula by the factor A_0/A_b; for example, Eq. (2.30) would become

$$\gamma = \frac{3Et_w^3t_b^2}{32L^4}\frac{A_0}{A_b} \tag{2.32}$$

This relation, which only holds if the pattern dimensions are sufficiently small compared to L, may also be used to estimate L for bonded patterned or structured plain wafers provided γ is known from experiments on unstructured plain wafers (15). Table 2.1 lists the formulas of surface energy in various configurations.

2.2.3 Bond Strength Measurement: Fracture Strength Method

Besides the crack-opening method, the surface energy may also be measured by the so-called "blister test" (16) schematically shown in Fig. 2.7. The test samples consist of two bonded wafers with one wafer containing a hole. Hydrostatic oil pressure is applied through the hole of the bottom wafer, which is kept fixed, and the critical pressure p_f for debonding is measured. Although the critical pressure measured would usually be associated with

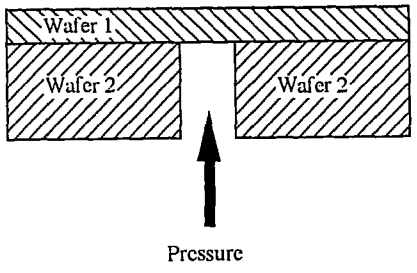

Fig. 2.7 Schematic diagram of the blister test method.

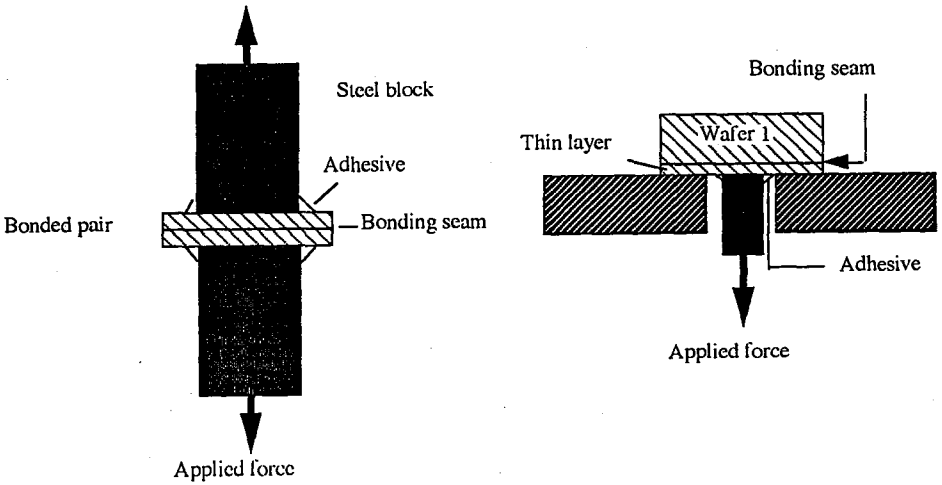

Fig. 2.8 Two tensile strength measurement configurations: (*a*) a tensile tester is used to pull the bonded pieces apart and (*b*) a tensile tester is employed to pull a thin film apart from a bonded pair.

a critical stress, in this specific measurement configuration, the physical quantity controlling the debonding is again the surface energy related to p_f via (17)

$$\gamma = \frac{0.088p_f^2a^4}{Et_w^3} \tag{2.33}$$

where we have assumed that the wafer with the hole is mechanically kept in a position so that its thickness and elastic properties do not enter Eq. (2.33). In Eq. (2.33), a is the radius of the hole, E is Young's modulus of the top wafer, and t_w is its thickness.

Besides the crack-opening and blister-test method, which both measure the surface energy of the bonded wafers, there are other methods to characterize the mechanical properties of the interface of bonded wafers.

Figure 2.8 shows two tensile strength measurement configurations (18, 19): (*a*) a tensile tester is used to pull from two opposite directions perpendicularly to the bonded surfaces to separate the bonded pieces, and (*b*) a tensile tester is employed to pull apart a thin film from a bonded thick substrate.

A tensile strain test machine can be used to measure the tensile strength of bonded pairs. Test samples are cut from bonded pairs into certain size chips (e.g., 2.5 cm^2) which are then glued using a high-strength epoxy resin to the sample fixture which consists of two steel blocks of a cross section smaller than the samples (e.g., 2 cm^2), see Fig. 2.8*a*. The larger size of the chips than

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the test block can prevent the glue from spreading to the side faces of the bonded chip. The test fixture then pulls the bonded pieces apart. The bond strength is given by the force at separation divided by the area of the sample. The method is very sensitive to residual damage originating from sample cutting. The configuration shown in Fig. 2.8*b* can alleviate these problems in the case of thin films and the bond strength of the final thin film structure is measured. These techniques can still be used for strongly bonded pairs which do not allow characterization by the crack-opening method because a razor blade cannot be inserted without breaking the bonded wafers. However, the maximum bond strength which can be measured is limited by the tensile strength of the epoxy adhesive.

From Eq. (2.17) it appears that if we knew the net interactive force, $F(t)$, versus separation between two bonding wafers, we could relate the interaction or surface energy of the bonded pair to the tensile strength or fracture strength. This is generally not possible. Not only do we not known the details of $F(d)$, but more important, in reality, the tensile strength is normally not determined by the maximum of $F(d)$ but rather by various imperfections at the interface.

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3

Influence of Particles, Surface Steps, and Cavities

3.1 INVESTIGATION METHODS FOR UNBONDED AREAS

One of the most common problems associated with wafer bonding is the occurrence of unbonded interface areas which are frequently termed "interface bubbles" or "voids." Interface bubbles either form immediately during the room temperature bonding process, during storage, or during a heat treatment or thinning of one of the bonded wafers. The causes of the bubbles formed during room temperature bonding include: (1) particles on the bonding surfaces, (2) localized surface protrusions, (3) localized absence of sufficient density of bonding species, and (4) trapped air pockets. Interface bubbles developed during storage or annealing usually originate from: (1) reaction of the interface bonding species with the bonding materials (e.g., water molecules react with silicon to generate hydrogen in bonded hydrophilic Si/Si pairs), (2) dissociation of bonding groups on the bonding surfaces (e.g., hydrogen is released from Si—H groups on bonding surfaces in bonded hydrophobic Si/Si pairs), or (3) desorption or outgassing from contaminants on or inside the bonding materials.

Many different techniques may be used to image interface bubbles. The choice of method depends on bubble size, efficiency, cost, materials, and crystallinity. This chapter describes the most common methods for viewing interface bubbles. Formulas for determining bubble sizes and heights are given and the influence of surface flatness, steps, and cavities on bonding behavior is discussed.

3.1.1 Optical Transmission

The most commonly used method to detect interface bubbles in a bonded pair is based on optical transmission. If the energy of the incident radiant photons, $h\nu$ (h: Planck constant = 6.62617×10^{-34} J-s; ν: frequency of the light) is equal to or greater than the band gap energy, E_g, of the material under the irradiation, the photons can break the covalent bonds in the lattice to generate electrons and holes and thus be absorbed almost entirely. The

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material therefore strongly adsorbs light unless the frequency, ν, or wavelength, λ, is in the range

$$\nu < E_g/h \tag{3.1}$$

or

$$\lambda > hc/E_g \tag{3.2}$$

based on $c = \lambda\nu$ where c is the speed of light (2.998×10^{10} cm/s in vacuum).

The absorption behavior is generally described in the form of a decrease of light intensity given by

$$I(z) = I_0 \exp(-\alpha z) \tag{3.3}$$

where I_0 is the incident light intensity, z is the distance traveled in the material perpendicular to the surface, and α is the absorption coefficient. The behavior of the adsorption coefficient of Si, Ge, and GaAs as a function of λ or ν can be found in the literature (e.g., reference 1).

If one of the bonding wafers is transparent to normal visible light, such as glass, quartz, ZnS, $LaAlO_3$, or GaN, the interface bubbles can easily be viewed by the naked eye. When both bonding materials are not transparent to normal visible light, the transmitting light with an appropriate wavelength based on Eq. (3.2) must be employed, where E_g is the smaller band gap among the two bonding materials if different materials are used.

To view the image with the light of wavelength λ, a detector that is able to sense the wavelength must also be employed. Figure 3.1 shows a typical

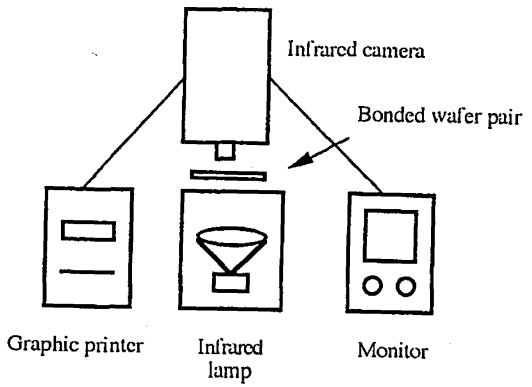

Fig. 3.1 Typical configuration of an imaging system for detecting interface bubbles in bonded Si/Si pairs.

TABLE 3.1 Minimum Wavelengths of Incident Light for Which the Materials are Transparent

Material	E_g(eV)	λ(μm)
Si	1.12	1.10
GaAs	1.43	0.86
InP	1.35	0.91
Ge	0.67	1.84
α-SiC (3C—SiC)	2.2	0.56
β-SiC (6H—SiC)	2.93	0.42
GaN	3.4	0.36
AlN	6.2	0.20
SiO_2 (Quartz)	8	0.15
ZnS	3.6	0.34
C (Diamond)	5.48	0.22

configuration of an imaging system for detecting interface bubbles in bonded Si/Si pairs. Since silicon has a band gap energy of 1.12 eV at room temperature, according to Eq. (3.2), light with wavelengths longer than 1.10 μm [in the infrared (IR) region of the electromagnetic spectrum] can pass through silicon. An IR lamp and an IR viewing camera are thus employed in the imaging system for bonded Si/Si pairs shown in Fig. 3.1. For a number of materials commonly used for wafer bonding, Table 3.1 lists the minimum wavelengths λ_{min} of incident light to which the materials are transparent.

If one of the silicon wafers in a bonded pair is heavily doped, strong free-carrier absorption occurs even for $\lambda > \lambda_{min}$. The absorption coefficient, α, owing to free carrier adsorption increases with the concentration of the free carrier, n, as well as the square of the wavelength of the incident light, λ^2, according to (2):

$$\alpha \propto n\lambda^2 \tag{3.4}$$

Therefore, the transmission method does not work for metals because of their high electron concentration (except for extremely thin films, which are not relevant in this context).

Figure 3.2 shows an IR image of a bonded Si/Si pair. The interference fringes in the bubbles can clearly be seen. Assuming the content in the bubbles is air with refractive index of 1.0, the height H of the bubbles can be estimated by the number of the fringes N:

$$H = N\frac{\lambda}{2} \tag{3.5}$$

Since bubbles down to half of a fringe can be detected by this method, the minimum detectable bubble height is $\lambda/4$, corresponding to 0.275 μm if a wavelength $\lambda = 1.10$ μm is used. The minimum lateral size that can be observed by this method depends on the resolution of the detector in the

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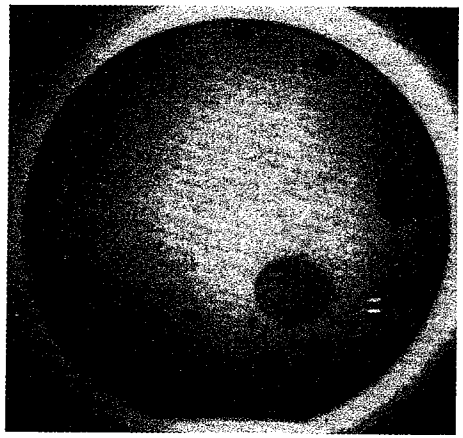

Fig. 3.2 Infrared image of a bonded Si/Si pair.

image camera. Usually, bubbles with a diameter greater than 1 mm can be observed (3), unless IR microscopes are used.

The described optical transmission method for detecting interface bubbles is relatively inexpensive, convenient to use, as well as real-time and nondestructive. However, the limited lateral resolution for detecting interface bubbles is a major drawback for some investigations.

3.1.2 X-ray Topography

X-ray topography (XRT) is a method to obtain an image of deviations from ideal, undistorted lattice planes (4). Therefore, it can only be applied to single-crystalline materials. The bonded pair of single crystal wafers is scanned by a collimated and monochromatic X-ray beam and is aligned on a specific Bragg angle, θ, so that only those X-rays diffracted from the measuring lattice planes will form a transmission image on the camera:

$$n\lambda = 2d \sin \theta \tag{3.6}$$

where λ is the X-ray wavelength, d is the interplanar spacing, θ is the Bragg diffraction angle, and n is the integer giving the order of the diffraction.

Figure 3.3 is a schematic diagram of the X-ray transmission topography method. The primary X-ray beam is transmitted through the bonded wafer pair and stopped in a lead screen. The diffracted beam strikes a photographic film through a slit of the screen. Any strain centers or defects in the entire volume of the wafer pair such as interface bubbles, dislocations, or lattice distortion due to elastic or plastic deformation will cause intensity changes of the diffracted beam owing to local variation in the Bragg condition. By scanning the bonded wafer pair and the photographic film synchronously, a topographic image of the whole wafer area is obtained.

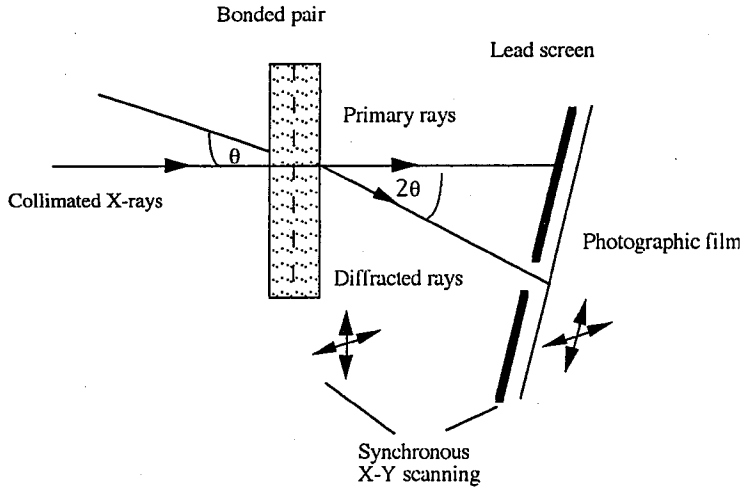

Fig. 3.3 Schematic diagram of X-ray transmission topography method.

X-ray topography has a typical spatial resolution of 2–20 μm, which is much better than that of the conventional IR transmission technique without an IR microscope and is especially suitable to detect very small interface bubbles. However, XRT is expensive and time consuming. For example, it can take several hours to get an image of a 4-in. bonded pair. Figure 3.4 is the X-ray topography image of the same bonded 4-in. Si/Si pair used in Fig. 3.2. None of the small bubbles shown can be seen in Fig. 3.2 using the IR

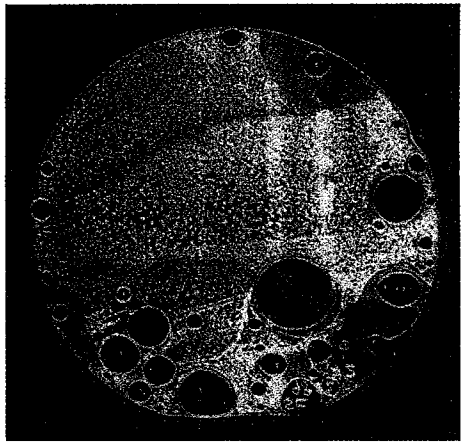

Fig. 3.4 X-ray topography image of the same bonded 4-in. Si/Si pair used in Fig. 3.2.

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system. Normally the two single crystal wafers are not perfectly aligned with respect to their lattice orientations; therefore, each wafer can separately be used for XRT topography. In this way, for example, the wafer of a bonded wafer pair in which plastic deformation has occurred can be distinguished.

3.1.3 Acoustic Microscopy

Scanning acoustic microscopy has become a powerful, nondestructive test technique in material investigations (5, 6). The schematic configuration of a scanning acoustic microscope as used in the reflection mode is shown in Fig. 3.5.

A coupling liquid (usually water) which is in contact with both the lens and the sample must be used to convey the acoustic beam. A piezoelectric transducer is employed to convert the electrical signal to an acoustic plane wave. Usually, the transducer is a sputtered ZnO film sandwiched between two gold films. When the electrical pulse signal is applied to the transducer, an acoustic plane wave is generated which is typically in the 50- to 800-MHz range, but a frequency as high as 3 GHz can be reached. The plane wave travels through the sapphire crystal to the surface spherical lens. Since there is a large velocity change between the acoustic wave that travels in the sapphire (11.1 km/s) and the wave that propagates in the water (1.55 km/s), a large angle of refraction at the lens–liquid interface takes place. Because of this effect, the acoustic wave leaves the lens close to the normal and converges to a focal point (7). The probe or the sample is mechanically

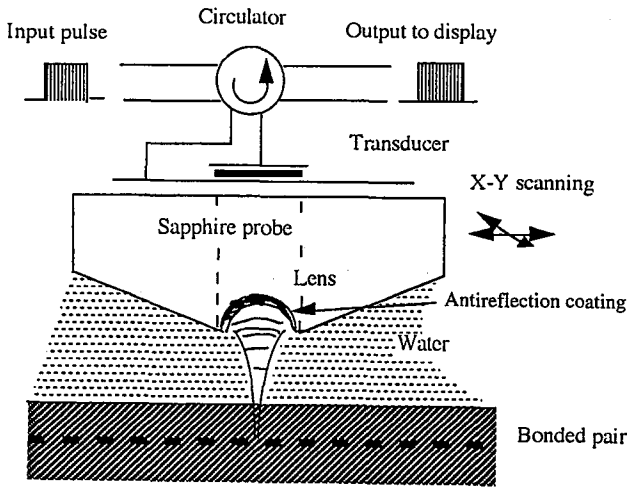

Fig. 3.5 Schematic configuration of a scanning acoustic microscope as used in the reflection mode.

scanned in a raster pattern. The returning reflected signal from the sample under study is monitored by the same transducer, separated from the input pulse, and used to generate an acoustic image. Because the scattering of acoustic waves is dependent on the change in elastic properties, when the acoustic beam is focused to the bubbles at the bonding interface of a bonded pair, the reflected signal is enhanced. The interface bubbles are thus detected.

The spatial resolution is diffraction limited and therefore depends on the wavelength/frequency of the acoustic beam. Since acoustic absorption in solid-state materials is usually low, the maximum frequency is essentially determined by the acoustic absorption in the liquid. In water it is known that the acoustic attenuation increases as the square of the frequency (5). At 160 MHz, a resolution of about 10 μm was reported, which is much better than for a conventional infrared system. Figure 3.6 is an acoustic image of the same bonded Si/Si pair shown in Figs. 3.4 and 3.2. It is clear that more details of the interface structure are shown in Fig. 3.6, using the acoustic microscope, compared to Fig. 3.2, using the infrared system.

The acoustic microscope technique for detecting inhomogeneities at the bonding interface is nondestructive, easy to operate, relatively quick and inexpensive, and applicable to basically all materials, including amorphous materials, as long as they do not contain large inhomogeneities in the bubble. However, the cost of the acoustic imaging system is relatively high (although much cheaper than XRT) and the measurement has to be performed in liquid, usually in water. This last point is a particular disadvantage only for weakly bonded wafers because the water may penetrate into the bonding interface during the acoustic measurement.

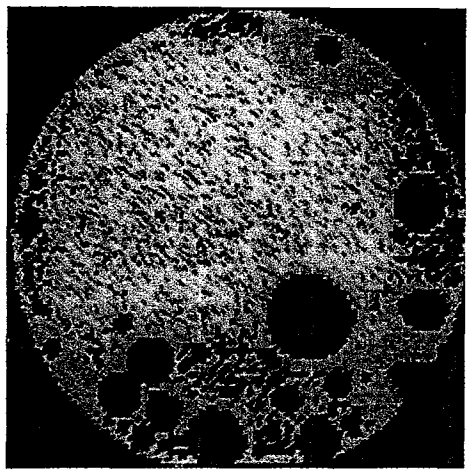

Fig. 3.6 Acoustic image of the same bonded Si/Si pair shown in Figs. 3.2 and 3.4.

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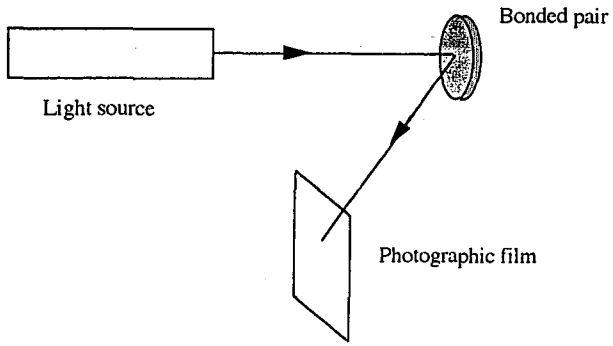

Fig. 3.7 Schematic of the magic mirror method.

3.1.4 Magic Mirror Method

The magic mirror method is a simple, fast, nondestructive yet sensitive technique to detect surface irregularities of polished wafers. Figure 3.7 is a schematic of the magic mirror method (8).

In this method, a wafer-size collimated beam of white light from a lamp is used to illuminate the mirror-polished surface of a bonded pair that is oriented off by a small angle from the normal. The topographic image of the whole wafer surface is formed by the reflected rays projected onto a screen or a photographic film.

Owing to divergence effects induced by deviations of the surface from an ideal flat plane, a convex surface will form a dark contrast in the topographic

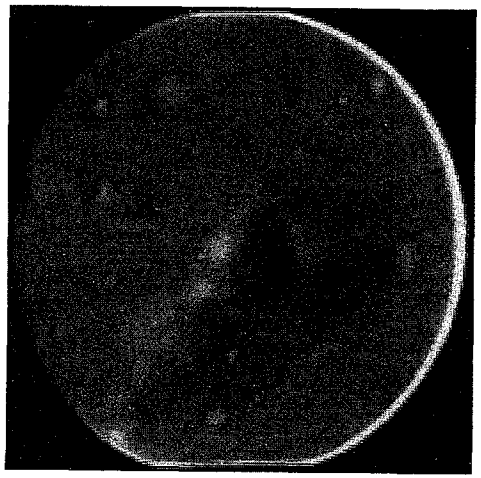

Fig. 3.8 Topographic image obtained by the magic mirror method.

image while the concave surface generates a bright contrast. The topographic image obtained by the magic mirror method clearly shows many dark areas (see Fig. 3.8). These dark areas correspond to the interface bubbles which generate local convex areas on the surface of the bonded pair by bending the wafers locally away from the interface. This interpretation has been confirmed by acoustic microscopy and X-ray topography images (8).

Since the basic condition used to generate the magic mirror image is the formation of sufficient irregularities on a mirror-polished surface, the magic mirror method to detect interface bubbles is especially useful for bonded pairs in which at least one of the wafers is relatively thin and double-side polished. Spatial resolution of the method depends on the thickness of the wafers and very small bubbles may not be detectable. Large interface bubbles with diameters on the order of the wafer thickness may also be detected in as-bonded wafers (double-side polished) without any thinning.

3.1.5 Interface Etching

Interface bubbles can be observed visually by thinning one of the wafers in the bonded pair to a sufficiently small thickness to allow bulging up of the bubbles (3).

Another approach to detect small interface bubbles in bonded silicon wafers is to cut the bonded pair and etch the cross section of the bonded Si/Si pair by KOH aqueous solution (9). The bonded pair must have sufficiently high bonding strength to withstand the dicing and etching procedures. After etching in 44% KOH at 85°C for 15–30 min, a clear straight etching groove can be seen at the bonding interface where no bubbles exist. At unbonded areas, KOH etches preferentially, resulting in etched holes deeper than the groove at the interface where no bubble was located. This method can only decorate the interface bubbles at the cut cross section and is used to investigate the presence of very small bubbles when X-ray topography is not conveniently available. Both etching approaches are destructive and time consuming.

3.1.6 Transmission Electron Microscopy

When the bonded pair is cut and thinned to the thickness range of 1000–3000 Å, transmission electron microscopy (TEM) can be employed to inspect the sample containing the bonding interface of the bonded pair in either cross-sectional or plan view. The primary advantage of the TEM method is its high resolution, approaching 1.8–2 Å, because the short wavelength of the electron beam at high voltage (e.g., at 100 kV, $\lambda \approx 0.04$ Å) results in a Bragg diffraction process occurring at a distance on the order of the interplanar spacings (10, 11). Therefore, TEM is the best method for investigating details of the interface structure of bonded wafers (12, 13).

The main disadvantages of the TEM method for detecting interface bubbles are the limited viewing area (typically much less than 1×1 mm^2 for

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plan view), and that it is destructive and time consuming for sample preparation and viewing.

3.2 BUBBLE DIAMETER AS A FUNCTION OF PARTICLE SIZE

During wafer bonding at room temperature, wafers are deformed around particles on bonding surfaces, leaving circularly unbonded interface areas or bubbles. In the situation schematically shown in Fig 3.9*a*, the particle size (radius h or height $H = 2h$) is much smaller than the wafer thickness t_w (i.e., $h \ll t_w$) and the radius R of the resulting unbonded circular area is much larger than t_w (i.e., $2t_w < R$). Assuming, in addition, that the particle is incompressible, we may use the simple theory of small elastic deflections of a thin plate to arrive at the approximate expression (14, 15):

$$R = \left[\frac{2}{3}E'\frac{t_w^3}{\gamma}\right]^{1/4} h^{1/2} \tag{3.7}$$

where γ is the surface energy of each wafer in the pair when partially debonded, $E' = E/(1 - \nu^2)$, and E and ν are the Young's modulus and the Poisson ratio of the wafers used, respectively.

For (100) Si, $\nu = 0.29$, Eq. (3.7) can be rewritten as

$$R = \left[0.73Et_w^3/\gamma\right]^{1/4} h^{1/2} \tag{3.8}$$

The unbonded areas resulting from even small particles are fairly large,for example, a particle of about 1 μm diameter leads to an unbonded area with a diameter of about 0.5 cm for typical 4-in. diameter silicon wafers with a thickness of 525 μm. A reduction of the wafer thickness leads to a strong reduction in unbonded area.

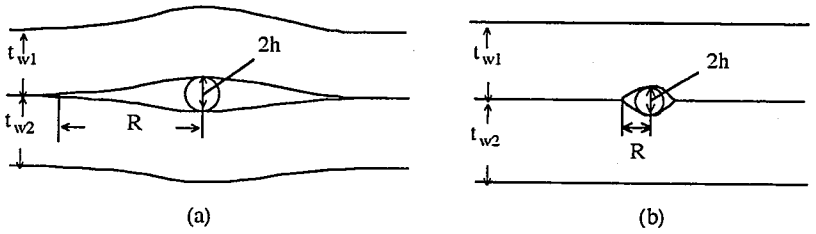

Fig. 3.9 (*a*) Schematic of particle leading to an unbonded area with radius R larger than wafer thickness t_w; (*b*) the same for sufficiently small particles leading to $R \ll t_w$.

For wafers of different thicknesses, t_{w1} and t_{w2}, and possibly different Young's moduli, E_1 and E_2, Eq. (3.7) may approximately be modified as

$$R = \left[\frac{1.3E_1't_{w1}^3E_2't_{w2}^3}{\gamma\left(E_1't_{w1}^3 + E_2't_{w2}^3\right)}\right]^{1/4} h^{1/2} \tag{3.9}$$

where $E_1' = E_1/(1 - \nu_1^2)$ and $E_2' = E_2/(1 - \nu_2^2)$.

It has been suggested that with decreasing particle size, the situation changes drastically. If R calculated by Eq. (3.7) leads to values below $R_{crit} = 2t_w$ (i. e., $R < 2t_w$) corresponding to a particle size $h < h_{crit}$ (16)

$$h_{crit} = 5(t_w\gamma/E')^{1/2} \tag{3.10}$$

then an elastomechanical instability is supposed to occur, leading to an unbonded area with a much smaller radius (Fig. 3.9*b*):

$$R \approx kh \tag{3.11}$$

where the dimensionless constant k is on the order of 1. For typical 4-in. silicon wafers, after room temperature bonding, h_{crit} is on the order of 1000 Å (0.1 μm). At this particle size, the radius of the unbonded area would change from about $2t_w$ (1000 μm) to about h_{crit} ($\approx$ 0.1 μm), corresponding to a decrease by a factor of 10,000 in R and to a decrease by a factor of 10^8 in unbonded area (see Fig. 3.10).

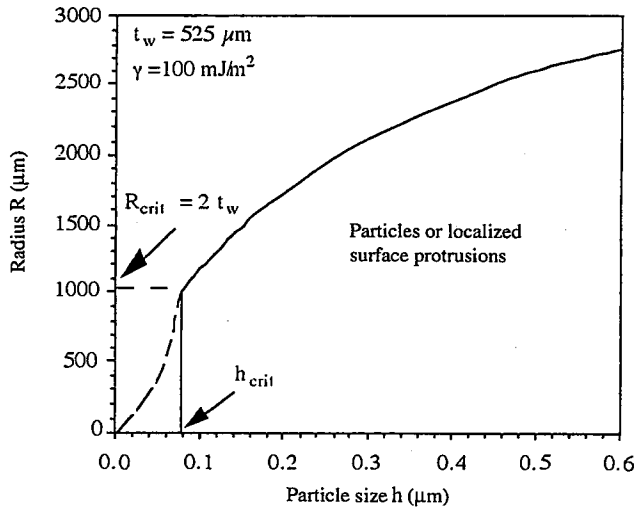

Fig. 3.10 Radius R of unbonded area around a particle as a function of particle height h for Si wafer thickness of 525 μm and $\gamma = 100$ mJ/m^2. Note the elastomechanical instability at h_{crit} predicted by Eq. (3.9).

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A similar treatment should also hold for localized surface protrusions and surface steps. The described instability may be used to explain why pressing wafers together using an outside force [e.g., during anodic bonding (17)] sometimes allows bonding to occur for wafers which would not otherwise bond. This "elastomechanical instability effect" has not been demonstrated experimentally and is presently under investigation. Numerical calculations (18) indicate that instead of the "elastomechanical instability" predicted by Eq. (3.11), a smooth transition will occur. For small particles, the corresponding expression is then given by

$$R = \frac{h^2 E'}{12\gamma} \tag{3.12}$$

3.3 INFLUENCE OF SURFACE FLATNESS, STEPS, AND CAVITIES

Surface flatness is a global, macroscopic measure of the deviation of the front surface of a wafer from a specified reference plane when the back surface of the wafer is ideally flat, as when the wafer is pulled down by vacuum onto an ideally clean, flat chuck (19). The total thickness variation (TTV) is commonly used to specify the surface flatness. Figure 3.11 is a schematic definition of TTV, which is the difference between the highest and the lowest elevation of the top surface of the wafer. During silicon wafer bonding at room temperature, each wafer of the pair is elastically deformed to achieve conformity of the two surfaces (20). The flatness nonuniformity of starting wafers can result in periodic strain patterns (contrast fluctuations) corresponding to typical spatial frequencies of a bonded pair which can be detected by X-ray topography. However, if the flatness nonuniformity is sufficiently large, unbonded areas may result.

Let us assume gaps between wafers caused by a flatness nonuniformity with a lateral extension, R, (or spatial period $2R$) much larger than their depth (or gap height), h, as schematically shown in Fig. 3.12 in the symmetrical case. The condition for gap closing depends on the ratio of R to the wafer thickness t_w.

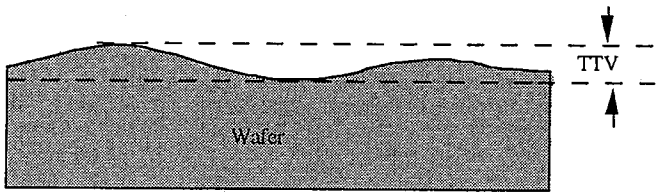

Fig. 3.11 Schematic of definition of total thickness variation (TTV).

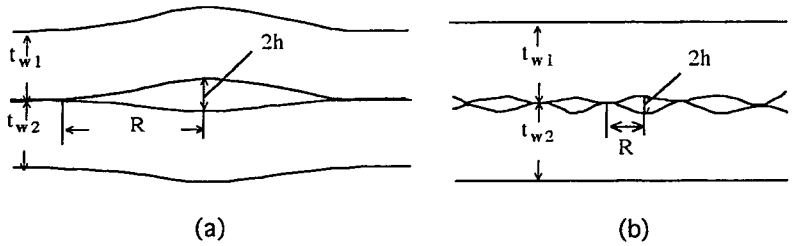

Fig. 3.12 (a) Schematic of gaps between wafers for the case of $R > 2t_w$ and (b) for the case of $R < 2t_w$.

For $R > 2t_w$ (Fig. 3.12a), the condition for gap closing depends on wafer thickness t_w and is given by

$$h < \frac{R^2}{\sqrt{\frac{2}{3}\frac{E' t_w^3}{\gamma}}} \tag{3.13}$$

For $R < 2t_w$ (Fig. 3.12b), the condition for gap closing is independent of wafer thickness t_w and is given by

$$h < 3.5(R\gamma/E')^{1/2} \tag{3.14}$$

For wafers of different thicknesses, t_{w1} and t_{w2}, and possibly different Young's moduli, E_1 and E_2, the Eqs. (3.13) and (3.14) may be changed into the approximate expressions

$$h < \frac{R^2}{\sqrt{\frac{4}{3}\frac{E_1' t_{w1}^3 E_2' t_{w2}^3}{\gamma(E_1' t_{w1}^3 + E_2' t_{w2}^3)}}} \tag{3.15}$$

for sufficiently large R values and

$$h < 3.5(R\gamma/2)^{1/2}\left(\frac{1}{E_1'} + \frac{1}{E_2'}\right)^{1/2} \tag{3.16}$$

for sufficiently small R values.

The changeover from Eq. (3.15) to Eq. (3.16) occurs approximately at

$$R \cong 2\left(\frac{E_1' + E_2'}{E_1' t_{w1}^3 + E_2' t_{w2}^3}\right)^{1/3} t_{w1} t_{w2} \tag{3.17}$$

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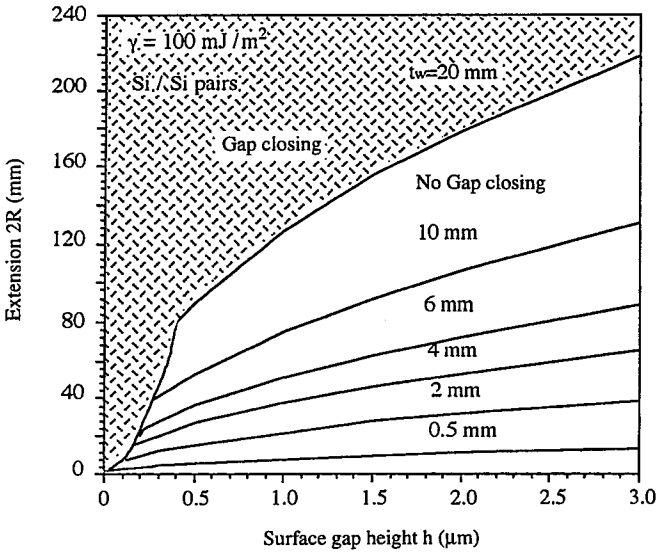

Fig. 3.13 Parameter combinations of gap height h and lateral extensions R of gaps which can be closed for a Si wafer thickness of 525 μm and $\gamma = 100$ mJ/m^2. The area in which closing of the gap can occur is shaded.

Basically, the thinner wafer (for equal E) determines the bonding behavior. In Fig. 3.13, the regions of gap closing or not closing are shown for two silicon wafers of equal thickness t_w based on $\gamma = 100$ mJ/m^2 and for various different values of t_w.

In practice, the flatness variation of 1–3 μm over commercial 4-in. silicon wafers poses no obstacle for wafer bonding at room temperature because the deformation of the two wafers can easily accommodate this scale of surface waviness. Bow and warpage of wafers up to about 25 μm are also tolerable. The expressions above may be used to predict whether wafer bonding is possible, provided γ and the waviness of the surface are known. In reality, the waviness is represented in a whole Fourier spectrum of amplitudes for certain wavelengths. If more than one single spatial frequency (like the macroscopic bow) dominates, an integral formulation has to be used.

For bonding a standard silicon wafer to a silicon wafer with cavities, the equations above can be used to predict whether the parts of the unstructured wafer covering the cavities will bond to the bottom of the cavity. We discuss this issue in Chapter 10 in more detail. In most cases, it appears that there is no problem with bonding to the bottom of cavities. For example, cavities on one of the bonding wafers can be used to absorb gases generated from the bonding interface during heat treatment of the bonded pair to avoid bubble generation (21).

Microroughness is a local, microscopic parameter of wafer surface quality that is crucial in wafer bonding. Microroughness is usually characterized by a value such as RMS (root mean square), abbreviated as R_q, that is measured by scanning tunneling microscopy (STM) or atomic force microscopy (AFM). It has been demonstrated experimentally that R_q less than 5 Å is adequate for silicon wafer bonding at room temperature via hydrogen bonds (22). This average roughness value is typical for commercially available prime grade bulk silicon wafers and silicon wafers with surface average roughness of less than 1 Å are also achievable. For such small steps or peaks, no available mathematical treatment is available to predict bondability. Nevertheless, in principle, the equations above may still be applicable to the case of surface roughness, provided the proper wavelength of lateral variations is known, for example, from measurements made using AFM.

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4

Surface Preparation and Room-Temperature Wafer Bonding

In Chapters 2 and 3, we have seen that the forces involved in wafer bonding are mainly short-range intermolecular forces. Therefore, adequate surface smoothness and flatness, surface cleanliness, and surface reactivity of the mating wafers are essential for successful bonding at room temperature. An appropriate smoothness of Si surfaces can be achieved by chemical–mechanical (chemomechanical) polishing techniques commonly used in the semiconductor industry. In this chapter, we focus on practical surface preparation approaches which can meet the requirements of surface cleanliness and reactivity of polished Si wafers. The design principle of the microclean room setup is described, which does not demand a conventional cleanroom environment to achieve particle-free bonding surfaces. For room-temperature bonding of Si pieces thicker than industrial standard Si wafers, special attention is necessary to realize the desired surface flatness, which may not be achievable through common semiconductor polishing technology. We find that commercially available optical polishing techniques may be used to this end.

The physical process involved in room temperature bonding and the estimation of the bonding strength are given, expressed by the specific surface energy of one of the bonding wafers when they are separated. Propagation of the bonding front during the initial stage of room-temperature bonding is also discussed. We show that the bonding velocity is mainly determined by the squeezing out of trapped gas between the two mating wafers.

Finally, approaches to debonding room-temperature bonded Si/Si, Si/SiO_2, SiO_2/SiO_2, and Si/sapphire pairs are discussed and a simple analytical model is introduced.

4.1 POLISHING OF WAFER SURFACES

As in very large scale integration (VLSI) device fabrication, a silicon surface with a high degree of smoothness and flatness is also a key concern for

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spontaneous wafer bonding at room temperature. This VLSI compatibility allows adoption of the fully developed VLSI polishing technology for Si wafer bonding.

Although a high degree of flatness ($\sim 0.05\ \mu m$), parallelism ($< 0.2\ \mu m$), and smoothness (mean microroughness < 1 Å) of Si and silica glass pieces up to 200 mm in diameter can be achieved by pure mechanical polishing (1), it does introduce a significant subsurface damage layer of $\sim 20\ \mu m$ in depth. To overcome this problem, a chemomechanical polishing technology has been developed for Si wafers which produces a surface smoothness similar to that of pure mechanical polishing but without subsurface damage.

After grinding or lapping, wafers are mounted on a flat plate by vacuum or wax and an external pressure is applied to press the wafers against the polishing pad, which is driven across the wafer surface. A polishing slurry of a colloidal dispersion of silica (SiO_2) in an aqueous solution of potassium hydroxide is dropped onto the pad to perform the polishing. The polishing pad materials are usually poromeric artificial fabrics such as polyester felt or polyurethane. The diameter of silica particles is in the range of 40 to 1000 Å, typically 100 Å (2). The pH value of the slurry is around 10–11 and the concentration of silica is typically 3–4% (3). Some properties of a typical chemomechanical polishing slurry are listed in Table 4.1.

The polishing first removes the native oxide layer on the Si wafers and then chemomechanically etches the Si itself. The OH^- groups in the polishing slurry are provided at high density by the surfaces of the silica particles and are transferred through the boundary layer to the Si surface by the mechanical action of the polishing process. The heat generated by friction between the sliding wafers and the pad leads to an oxidation reaction of Si by KOH with the OH^- radicals (4, 5):

$$\begin{aligned} Si + 4OH^- &\longrightarrow Si(OH)_4 + 4e^- \\ 4HOH + 4e^- &\longrightarrow 4OH^- + 2H_2 \end{aligned} \qquad (4.1)$$

This is the main chemical reaction involved in the polishing process. To control the polishing rate and to avoid the formation of surface haze, the temperature of the polishing pad must be controlled. A typical temperature of the pad is about 40°C during operation.

The silicic acid $Si(OH)_4$ monolayers are then frictionally removed away by the silica particles in the slurry, which have a hardness slightly higher than

TABLE 4.1 Some Properties of Chemomechanical Polishing Slurry

Composition	Typical Size of Silica Particles	pH Value	Concentration
$SiO_2 + KOH + H_2O$	100 Å	10–11	3–4%

TABLE 4.2 Representative Si Polishing Technology

Solution	Pad Material and Temperature	Si Removed	Microroughness	Flatness
3–4% 100 Å silica in aqueous KOH, pH = 10–11	Polyurethane and ~ 40°C	$\sim 25\ \mu m$	~ 1 Å	$1–2\ \mu m$

silicon. Silica is not likely to leave foreign impurities on the Si surface that are insoluble in solutions which are not reactive to silicon. The new surface formed by this polishing mechanism subsequently reacts again with OH^- radicals. The thickness of the Si layer which has to be removed strongly depends on prepolishing lapping method. Typically, an Si layer of $\sim 25\ \mu m$ has to be removed by the polishing process to reach a damage-free smooth surface.

To prevent the formation of surface haze and stains, the residual slurry must be removed from the polished wafers by rinsing the wafers in deionized (DI) water immediately after polishing. Finally, a chemical cleaning process is usually performed to thoroughly clean the polished Si wafers. The mean microroughness of the resultant Si surface is typically in the range of 1 to 2 Å. The representative Si polishing technology is summarized in Table 4.2.

Although the chemomechanical polishing produces Si surfaces with sufficient smoothness that are free from haze and damage, the resilient polishing pad and batch wafer polishing method make it difficult to maintain the polishing conditions exactly uniform across each wafer as well as between wafers; therefore, the polishing process is likely to more or less degrade the surface flatness achieved by the prepolishing lapping operation. The present trend toward single-wafer polishing may improve the surface flatness. The resultant surface flatness of $1–2\ \mu m$ over up to 8-in. wafers can satisfy the requirements of room-temperature bonding of Si wafers with standard thickness and optical projection lithography of current VLSI applications. However, it may not be adequate for thick Si piece bonding in which a better surface flatness is required. In this case, optical polishing technology may be adopted to achieve a better surface flatness because subsurface damage is not as critical in thick Si piece bonding for micromechanical applications. We discuss this aspect in some detail in Section 4.7.

4.2 WAFER SURFACE CLEANING

4.2.1 Cleaning Principle of Hydrogen-Peroxide-Based RCA Solutions

Wafer bonding requires wafers with clean surfaces which are free of particulate, organic, and metallic contaminations. This is important because the surface cleanliness has a direct effect on both the structural and electrical

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properties of the bonding interface as well as on the resulting electrical properties of the bonded materials.

The cleaning techniques employed prior to room-temperature wafer bonding must be able to remove all contamination on the surfaces without degrading surface smoothness. These requirements are again fully compatible with VLSI technology. Therefore, the wet-chemistry wafer cleaning commonly used in the semiconductor industry is fully applicable to wafer bonding. However, since the quality of the bonding interface is extremely sensitive to particulate and organic contamination, additional cleaning techniques may be needed.

Hydrogen-peroxide-based "RCA" wet cleans are most commonly used in the semiconductor industry and also in wafer bonding. The basic cleaning steps involve two solutions: RCA1 (or SC-1, refers to Standard Clean-1) and RCA2 (SC-2), which are used sequentially (6). The typical compositions of the RCA solutions and operating conditions are listed in Table 4.3.

Water-insoluble organic compounds can make Si surfaces hydrophobic, preventing the effective removal of metal contaminants. Therefore, stripping the organic contaminants from Si wafer surfaces should be performed first in the cleaning process. Solution RCA1 is designed to remove organic contaminants by both the solvating action of the NH_4OH and the oxidizing action of the H_2O_2 at high pH. The compound NH_4OH is also a strong complexing agent for some metals of group I and II such as Cu, Ag, Ni, Co, and Cd (6).

For a bubble-free interface of bonded wafer pairs, the removal of insoluble particulate contamination is vital. The RCA1 solution can remove particulate contaminants efficiently. The main adhesion forces of particles on the wafer surface are electrostatic forces introduced by static charges on the particle and surface, van der Waals forces, capillary forces, and possible chemical bonds between the particle and the surface. It is speculated that, as a liquid, the RCA1 solution can reduce the strength of the capillary forces and surface charges and may also modify the surface of the particles and the wafer so that the particle is separated from the surface. The removal of

TABLE 4.3 Compositions of Standard and Modified RCA1 and RCA2 Cleaning and Operating Conditions in Si Wafer Cleaning

	Compositions by Volume[a]	Operating Temperature (°C)	Operating Time (min)	Designed to Remove
RCA1	$NH_4OH:H_2O_2:H_2O$ = 1:1:5 to 1:2:7	75 to 85	10–20	Particles, organics, some metals
Modified RCA1	$NH_4OH:H_2O_2:H_2O$ = 0.01–0.25:1:5	70–75	5–10	Particles, organics, some metals
RCA2	$HCl:H_2O_2:H_2O$ = 1:1:6 to 1:2:8	75–85	10–20	Alkali and heavy metals

[a]Note: CMOS grade, 30% unstabilized H_2O_2, 29% NH_4OH, 37% HCl, and DI water are used.

particles from the Si surface can be enhanced by the use of megasonic (700–900 kHz) acoustic cleaning in an RCA1 solution (7). With an input power density of 5–10 W/cm^2, the sonic pressure waves impact the Si surface and efficiently remove particles ranging in size from several micrometers down to ~ 0.3 μm from the Si surface (8).

After cleaning in RCA1, the wafers are rinsed thoroughly in DI water with a resistivity of 18 M Ωcm. The RCA2 solution is then employed to remove metal and alkali contaminants such as Al, Fe, Mg, Au, Cu, Cr, Ni, Mn, W, Pb, Nb, Co, and Na. The HCl in H_2O_2 forms soluble alkali and metal salts by dissolving and/or complexing, and prevents redeposition by forming soluble complexes with the resulting ions.

Because both NH_4OH, HCl, and H_2O_2 can generate gases at room temperature, the two solutions are preferably prepared immediately before use. Wafer cleaning is performed at 75 to 85°C for 10–20 min, followed by a DI water rinse.

4.2.2 Microroughening and Modified RCA1 Solution

It is known that a native oxide of a few Å is grown at room temperature on silicon surfaces exposed to air or in water when oxygen and moisture coexist (9). Chemomechanical polished Si wafers usually have an initial native oxide layer with a thickness of 2–10 Å. Since the native oxide may trap trace impurities, it is usually removed by a dip in a 1% HF water solution for 15 sec. However, high-quality and particle-free HF must be used under controlled conditions, otherwise the highly reactive bare Si surface will attract particles, metals, and organic contaminants from the HF solution, DI water, and the air (6). Since RCA1 can remove most of the possible contaminants, especially particles caused by the HF dip, a common processing operation is to preclean the polished wafers by a $H_2SO_4:H_2O_2$ mixture (2:1 or 4:1 in volume) followed by the 1% HF dip and then RCA1 and RCA2 cleaning.

If the native oxide is removed by the HF dip, the NH_4OH in RCA1 solution will attack the bare Si surface. Although when H_2O_2 is present, the Si surface quickly forms a native oxide of ~ 4 Å (6, 9) which can protect the Si surface from NH_4OH attack, the RCA1 cleaning at 80°C can still cause microroughening of the Si surface. The mean microroughness may increase from ~ 1 Å up to ~ 5 Å (10).

It has been found that for a modified RCA1 cleaning in which the NH_4OH mixing ratio is reduced to 0.05, the Si surface is free of microroughening (10). The disadvantage of this procedure is the reduction of particle removal efficiency. The compromise is to use a modified RCA1 with its NH_4OH mixing ratio reduced to ~ 0.25. It has also been found that RCA2 cleaning does not introduce microroughening of the surface.

A hydrous thin oxide (frequently also called "native oxide") will grow on the Si surface during the RCA cleaning process. The hydrous oxide is a strained oxide (11) and is highly reactive. It reacts readily with water to form

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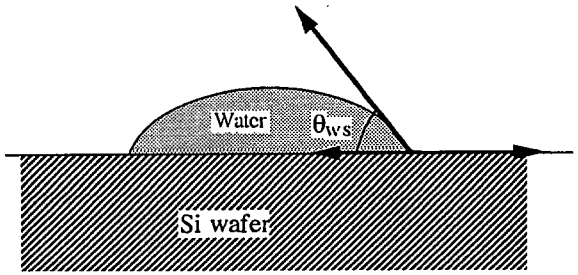

Fig. 4.1 Schematic of the equilibrium contact angle between water droplet and Si surface.

Si—OH (silanol) groups on its surface. Because OH groups are strongly polarized, they can form hydrogen bridge bonds with water, which causes the Si surface to become hydrophilic after RCA cleaning. If the Si surface is covered by thermal oxide during RCA cleaning, water and OH ions can also break the Si—O—Si (siloxane) bonds of the oxide and form Si—OH groups (12). The Si wafers with a hydrophilic surface can bond spontaneously at room temperature. For certain applications of wafer bonding such as SOI preparation, the native oxide presents no obstacle for the resultant structures.

The hydrophilicity of a Si surface can be measured by the contact angle between water and the Si surface. Figure 4.1 is a schematic of the concept of a contact angle θ. It has been found that after boiling in RCA1, the contact angle θ of the Si surface is about 5°, while a surface which has undergone full RCA1 and RCA2 cleaning shows a contact angle that depends on the RCA2 temperature, and is $\sim$ 25° if the RCA2 solution is kept at 95°C or lower and $\sim$ 9° if the solution is kept at 100°C (13).

4.2.3 Alternative Cleaning Technologies

4.2.3.1 Sulfuric- and HF-Based Solutions Another cleaning solution commonly used for Si wafers is sulfuric based. The conventional composition is H_2SO_4 (98%):H_2O_2 (30%) = 4:1 or 2:1. The cleaning action of the concentrated H_2SO_4:H_2O_2 solution is similar to that of RCA1. Compared with the reagents used in the RCA solution, which are completely volatile, the sulfuric-based solution requires acid reprocessing technology and is more hazardous. However, the problems with surface roughening are eliminated (10) and metallic contamination is also reduced. The contact angle of the Si surface cleaned by the sulfuric-based solution is about 8°.

For some applications of wafer bonding, such as replacement of epitaxial growth, removal of the surface native oxide is essential. Moreover, as the native oxide often acts as a contaminant trap, the stripping of the native

oxide can remove any metals that are still present on the Si surface. Removal of the oxide is usually achieved by a dip in dilute high-purity HF, typically 1% HF for 15 sec. or 0.6% HF for 1 min, followed by a DI water rinse. It is performed at room temperature without appreciable surface recontamination and roughening. The Si surface after the HF-only process is terminated mostly by hydrogen (Si—H) and also by a small amount of fluorine (Si—F). Because the Si—H bond is weakly polarized, having dynamic effective charge of only 0.1e, where e is the charge of an electron (14), the Si surface is highly hydrophobic with a contact angle of $\sim$ 70°.

Hydrophobic Si wafers prepared by RCA cleaning followed by a HF dip without a subsequent DI water rinse have shown a spontaneous room-temperature bonding similar to hydrophilic wafer bonding. If DI water rinse is performed after the HF dip, the Si—F groups will be replaced quickly by Si—OH groups. There is also a slow replacement of Si—H by Si—OH. The room-temperature bonding is also spontaneous and is attributed to Si—OH···(HOH)···HO—Si, similar to hydrophilic wafer bonding. We discuss this effect in Section 4.3.2.2.

4.2.3.2 Hydrogen Plasma Cleaning and Thermal Treatment in UHV As described in previous sections, a thin hydrous oxide (or native oxide), hydroxyl (OH) groups and water molecules are present on the hydrophilic Si surface after cleaning in RCA or sulfuric-based solutions. If they are removed by an HF dip without DI water rinse, hydrogen and some fluorine will exist on the hydrophobic Si surface (15). The native oxide or the fluorine will remain at the bonded interface even after 1100°C annealing and can introduce defects and electron traps at the bonding interface. Although these species are the sources of the interwafer attraction forces for room-temperature wafer bonding and can be tolerated in most wafer-bonding applications, they may not be desirable for some device applications in which the bonded interface is involved in active device areas requiring long carrier lifetime. To produce a defect-free bonded interface, it is necessary to remove all the foreign species from the mating Si surfaces prior to bonding.

It has been demonstrated that excited or ionized hydrogen is able to remove native oxide as well as hydrocarbons from a hydrophilic Si surface resulting in a pure hydrogen terminated surface (16–17). A representative hydrogen plasma cleaning setup is shown schematically in Figure 4.2. Argon and hydrogen are fed into the cleaning chamber where a potential between the filament and ground (chamber wall) is applied and a dc discharge current is generated. The wafer is pushed into the plasma cleaning chamber and immersed in the Ar: H_2 = 1:1 plasma for $\sim$ 10 min. The wafer temperature is about 200°C during cleaning. The native oxide and hydrocarbons on the Si surface are removed and the Si wafer surface is fully hydrogen terminated after H-plasma cleaning (18). The H-treated Si wafers are strongly hydrophobic and do not bond to each other even if a small external pressure is applied.

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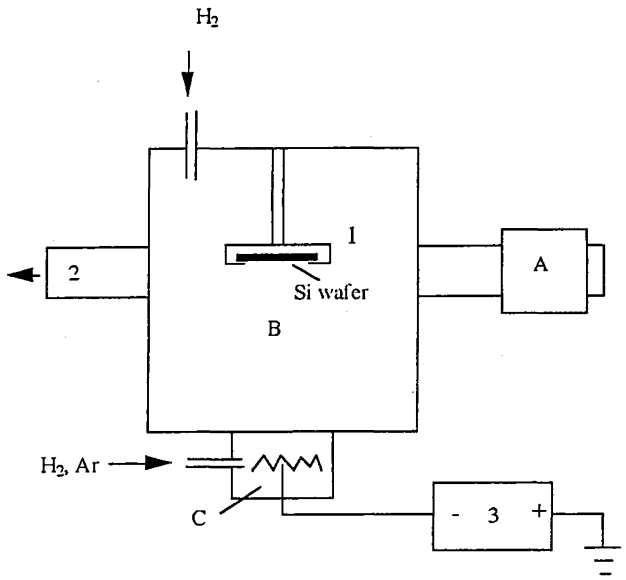

Fig. 4.2 Schematic of configuration of hydrogen plasma cleaning setup: (*A*) load-lock; (*B*) plasma cleaning chamber; (*C*) plasma source. (1) grounded substrate holder; (2) transport channel to MBE growth chamber for thermal desorption treatment; (3) power supply.

To remove the surface hydrogen, the wafer is directly transferred into an Si MBE growth chamber in ultrahigh vacuum (UHV) of around 1×10^{-9} Torr in situ via a transport channel and is treated at 600°C for 4 min after H-cleaning. The integrated hydrogen content on the wafer surface is reduced drastically after the 600°C thermal desorption treatment and the surface becomes hydrophilic and bondable. If the Si wafers would then bond together in UHV in situ, the resulting interface would be much closer to perfect in terms of avoiding surface contamination.

Alternatively, the native oxide on the RCA cleaned Si surface may also be removed by heating to 850°C for 30 min in UHV at a pressure of less than 2×10^{-8} Torr (19–21). The mechanism for the SiO_2 decomposition can be expressed by the reaction

$$Si + SiO_2 \longrightarrow 2SiO \uparrow \tag{4.2}$$

The UHV is essential for preventing reoxidation of the gaseous SiO and for avoiding the direct etching of the Si surface by reaction of Si and O_2.

4.3 ACTIVATION OF WAFER SURFACE

From the discussion in Section 3.1, it is obvious that the van der Waals dispersion force is ubiquitous and is applicable to almost all substances which are in intimate contact (so-called optical contact). Therefore, in principle, two solid-state plates of almost any material can bond to each other at room temperature provided that their surfaces are sufficiently flat and clean to allow the surface molecules of two plates to get close enough (sometimes only after some local elastic or plastic deformation of the solid) and van der Waals forces between atoms on the touching surfaces to be sufficiently strong. In practice, it is very costly to produce an optically smooth and flat surface, and hardly possible at all for some materials. Therefore, it would be highly desirable to create a reactive bonding surface to alleviate the surface smoothness requirement.

4.3.1 Hydrogen Bonding

The hydrogen bond is a bond by hydrogen between two atoms and has the form of

$$X—H + Y \longrightarrow X—H \cdots Y \tag{4.3}$$

where H is a hydrogen atom, — and ··· represent a covalent and a hydrogen bond, respectively. Usually, X and Y are atoms with high electronegativity values (i.e., the most electronegative atoms, F, O, and N should form hydrogen bonds easily). Table 4.4 gives the electronegativity values of some elements. However, there are some exceptions. For example, chlorine has the same electronegativity value as nitrogen, but it does not possess the ability to form hydrogen bonds in most cases, probably owing to its large size. On the

TABLE 4.4 Electronegativity Values for Some Elements[a]

Element	Electronegativity
F	4.0
O	3.5
N	3.0
Cl	3.0
Br	2.8
C	2.5
H	2.1
Si	1.8

[a] From reference 22.

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TABLE 4.5 Electronegativity Difference and Amount of Partial Ionic Character

Hydrogen bond	Difference in Electronegativity	Ionic Character
H—F	1.9	45%
H—O	1.4	39%
H—N	0.9	18%

other hand, in some molecules, for example, C—H in N≡C—H and Si—H in $=SI\begin{matrix}F\\H\end{matrix}$, the formation of hydrogen bonds was observed. In both cases, from the electronegativity scales the C—H and Si—H bond would show a small amount of ionic character insufficient to attract another electronegative atom to form a hydrogen bond. However, the neighboring N or F atom can increase the electronegativity of the carbon or silicon atom sufficiently to permit the formation of hydrogen bonds such as C—H···N or Si—H···F (22, 23).

The hydrogen atom, having only one stable 1s orbital, can form only one pure covalent bond; therefore, the attraction forces between hydrogen and another atom in a hydrogen bond is largely ionic (i.e., electrostatic) in nature (22). The amount of partial ionic character of some hydrogen bonds due to their electronegativity difference is listed in Table 4.5. For example, in the O—H bond, 61% of the 1s orbital of the hydrogen atom is used in covalent bond formation with the oxygen atom and the remaining 39% is available for formation of another largely ionic bond (a fractional covalent bond) with the more distant oxygen atom of the hydrogen bonded group O—H···O. Therefore, in almost all hydrogen bonds, the hydrogen atom is closer to one of the two adjacent electronegative atoms than to the other.

The energy of the hydrogen bond (which essentially determines the bond strength) increases with increasing electronegativity of the two bonded atoms and is in the range 0.1–0.4 eV. The hydrogen bond is not a strong bond compared to covalent bonds (e.g., the bond energies of 1.9 and 4.5 eV for a Si—Si bond and a Si—O bond, respectively). However, the hydrogen bond can play a key role in reactions occurring at normal temperatures, such as that in room-temperature wafer bonding, owing to its relatively weak bond and the small activation energy involved in its formation and rupture.

If hydrogen bonding can be realized across two mating surfaces, it will result in strong dipole–dipole van der Waals attraction forces between these surfaces. Moreover, when the mating surfaces are hydrophilic and water molecules are present, the linkages of two or three water molecules may bridge the gaps between the two mating surfaces. Since the size of an OH group is 1.01 Å (24) and the distance between two hydrogen-bonded oxygen atoms in ice is 2.76 Å (25), hydrophilic Si surfaces separated up to 10 Å can be bridged to adhere through clusters of three hydrogen bonded water

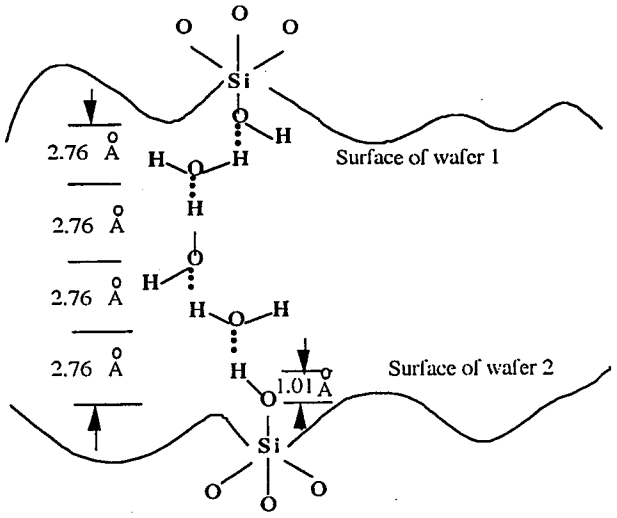

Fig. 4.3 Schematic of a linkage of three water molecules between two hydrophilic mating surfaces to bridge the wafers at RT.

molecules at room temperature (26) (see Fig. 4.3). This long-range hydrogen bonding will ease the smoothness requirements of the mating surfaces for successful room-temperature bonding.

The purpose of surface activation is thus to realize a reactive surface with practically available smoothness and flatness for room-temperature bonding. Since hydrogen bonding is an especially strong form of dipole–dipole attraction, a surface suitable for hydrogen bonding is highly desirable. It appears that any material that can form H—F, H—O, or H—N bonds, or attach electrophilic hydrogen on its surface, can bond via hydrogen bonding at room temperature to the same or a different material with a surface containing a sufficient density of nonbonding electrons on oxygen, nitrogen, or fluorine provided that the surfaces are sufficiently smooth, flat, and clean.

Another possible type of reactive surface is the superclean surface in UHV. Since the pure Si surfaces are not terminated by foreign atoms, the two mating surfaces would be highly reactive to form covalent bonds between Si atoms during room temperature bonding. Room-temperature, large-area, self-propagating UHV bonding of silicon wafers has recently been realized, as discussed in Section 12.7.1.

4.3.2 Wet Chemical Activation of Si or SiO_2 Surface

4.3.2.1 Wet Chemical Hydrophilization of SiO_2 Surface Native oxide-covered Si or thermally oxidized Si surfaces can be activated by wet chemical

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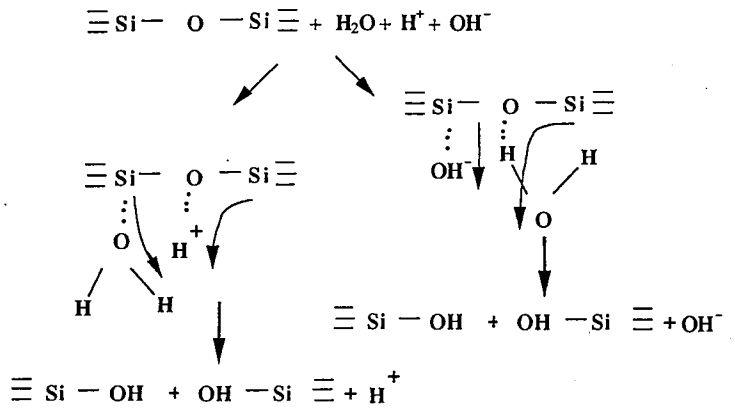

Fig. 4.4 Schematic of the effect of H^+ and OH^- during hydrophilization process of Si surface covered with native oxide or thermal oxide.

treatments based on the reactions between the silica network and H^+ or OH^- groups (27, 28):

$$\begin{aligned} Si{-}O{-}Si + OH^- &\longrightarrow Si{-}OH + Si{-}O^- \\ Si{-}O^- + HOH &\longrightarrow Si{-}OH + OH^- \end{aligned} \qquad (4.4)$$

and

$$Si{-}O{-}Si + H^+ + HOH \longrightarrow 2Si{-}OH + H^+ \qquad (4.5)$$

The reactions above are schematically represented in Fig. 4.4. It can be seen that the H^+ or OH^- ions determine the surface hydrophilization rate.

The equations above may be simplified as

$$Si{-}O{-}Si + HOH \longrightarrow Si{-}OH + HO{-}Si \qquad (4.6)$$

However, Eq. (4.6) is valid only when the surface siloxane bonds (Si—O—Si) are strained (12).

The native oxide formed by wet chemical cleaning has been found to be a strained oxide with a mean Si—O—Si bond angle of ~ 130°, deviating from its equilibrium value of 144° in bulk vitreous silica (11). The bond angle deformation significantly increases the chemical reactivity of the Si—O—Si bond. Therefore, the reaction of Eq. (4.6) occurs readily on the surface native oxide of Si wafers.

It has been determined that the fully hydroxylated silica surface contains about 4.6 OH groups per nm^2, that is, 4.6 OH groups/100 $Å^2$ (29). There are two main types of silanol (Si—OH) groups on the surface: (1) isolated groups and (2) hydrogen-bonded (associated) groups (see Fig. 4.5). The latter

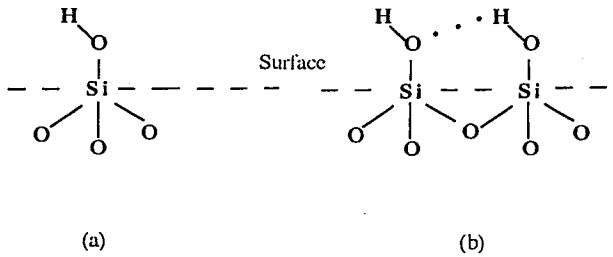

Fig. 4.5 Two types of silanol groups on Si surface covered with native oxide or thermal oxide. (a) Isolated group and (b) hydrogen-bonded groups.

occur because adjacent silanol groups are close enough and are suitably orientated toward one another that they form hydrogen bonds. The surface density of the isolated silanol groups is ~ 1.4 groups/100 $Å^2$ and that of hydrogen-bonded groups is ~ 3.2 groups/100 $Å^2$ (29).

The surface hydroxyl groups are polarized and are therefore reactive. They are the most important sites for the surface adsorption of silica via hydrogen bonding. It has been found that water molecules appear to prefer to be adsorbed on the hydrogen-bonded silanol groups while ammonia, nitrogen, and diethylamine strongly prefer the isolated silanol groups (30).

Equation (4.6) is reversible up to ~ 425°C. It implies that surfaces dehydrated (polymerization of silanols) up to 425°C are readily rehydrated when water is available. However, above this temperature rehydration becomes increasingly difficult. The cause of the irreversibility is still not known, but probably involves the restructuring of the surface, resulting in relaxing of the strain of the Si—O—Si bond.

Compared to the native oxide, the Si—O—Si bond of thermal oxide is less strained. Although the surface of thermal oxide still has a few isolated OH groups (e.g., 0.06 OH/100 $Å^2$ after 1100°C annealing) (31), it is essentially hydrophobic (see Fig. 4.6). The water may be adsorbed on these remaining silanol sites and then react with the strained neighboring siloxane bond, resulting in a very slow fracture process. The surface can be fully hydrated only after being boiled in water for long periods, such as 60 h (31).

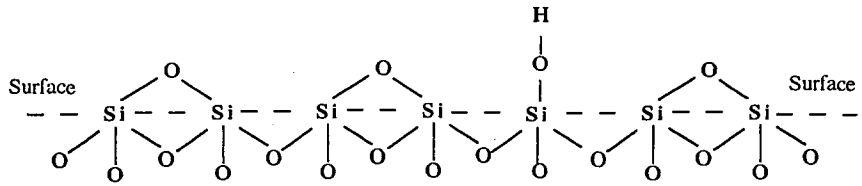

Fig. 4.6 Surface of thermal oxide on Si wafer prior to surface activation treatments.

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TABLE 4.6 Some Chemicals for SiO_2 Surface Hydrophilization and the Products of the Reactions

	Chemicals	Reaction Products
	H_2O	Si—OH + HO—Si
	NH_4OH	Si—NH_2 + HO—Si
	HNO_3	Si—NO_3 + H—Si + HO—Si
Si—O—Si +	H_2SO_4	Si—SO_4 + H—Si + HO—Si
	CH_3OH	Si—OCH_3 + HO—Si
	$(CH_3)_2NH$	Si—$N(CH_3)_2$ + HO—Si
	CH_3NH_2	Si—$NHCH_3$ + HO—Si

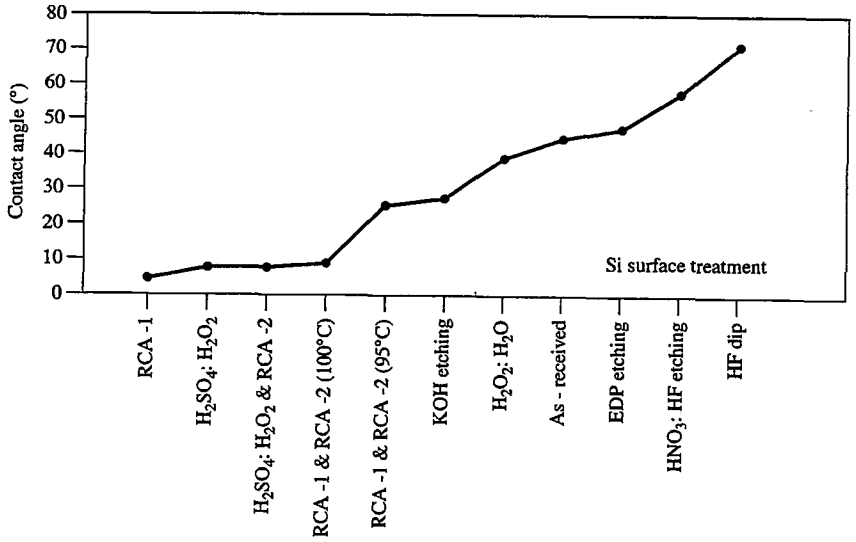

Fig. 4.7 Measured contact angle of water with Si surface prepared by various surface treatment methods.

It is therefore necessary to use a solution containing H^+ or OH^- ions to hydrate the surface of thermally oxidized Si wafers, as suggested by Eqs. (4.4 and (4.5). It should be noted that for high pH values (> 12) SiO_2 will be etched remarkably (4).

Organic chemicals can also react with strained siloxane bonds. In Table 4.6 some chemicals, including organic chemicals which can render the SiO_2 surface hydrophilic, are listed. As mentioned previously, the surface hydrophilicity is usually evaluated by the contact angle between a water droplet on the wafer and the wafer surface. Figure 4.7 shows typical measured contact angles of wafer surfaces covered with native oxide prepared by various surface treatment methods.

4.3.2.2 Wet Chemical Electrophilization of Si Surface As discussed above, silicon wafers with hydrophilic surfaces can bond to each other at room temperature. This has been attributed to the presence of OH groups on the mating surfaces that form hydrogen bonds between the two wafers. It has been found that hydrophobic Si wafers prepared by a dip in diluted HF without subsequent water rinse show a similar room temperature-bonding performance (32).

When the DI water rinse is not performed after a dilute HF dip, the Si surfaces are mainly terminated by H, but a significant amount of F, about 0.12 of a monolayer (23) or $\leq 1 \times 10^{14}$ atoms/cm^2 (33), has also been found on the silicon surface. The bondability of the HF-dipped Si wafers is most likely correlated to the presence of Si—F bonds.

The Si surface is etched off by HF in the form of SiF_4 at the beginning of the HF dip and is subsequently terminated by H, which is essentially stable considering the slow etch rate of low pH HF solutions. However, Si—F bonds appear to remain at reactive sites, such as atomic steps and surface defects, as evidenced by the fact that the F coverage is almost independent of the HF concentration from 0.3 to ~ 20% (23). Moreover, no Si—F bonds are found on Si (111) surfaces prepared by dipping in buffered HF solution ($HF:NH_4F=1:4$) with pH = 5.3, such that the surfaces become ideally smooth owing to the preferential etching of the surface steps and defects by the solution (34). It has also been found that these surfaces do not bond well (32).

Although there is a lack of direct experimental evidence for the presence of Si atoms bonded to both H and F, some partially fluorinated surface bonds $=Si\begin{matrix}F\\H\end{matrix}$, are likely produced (23, 35, 36), probably at chemically reactive sites such as atomic steps or surface defects (23). Since F has the highest electronegativity, charge transfer of valence electron clouds among the neighboring H, Si, and F in the surface $=Si\begin{matrix}F\\H\end{matrix}$ bonds appears possible and the Si—Si bonds as well as the Si—H bonds are stabilized against further attack of HF to form SiF_4 (23). Moreover, since Si—F bonds are located at chemically reactive sites such as atomic steps, valence electron transfer may also take place between Si—F bonds and neighboring Si—H bonds due to their proximity (34). Therefore, the Si—F bonds could behave like $=Si\begin{matrix}F\\H\end{matrix}$ bonds.

The Si—H bond is weakly polarized, having a dynamic effective charge of only 0.1e where e is the charge of an electron. The Si—F bond is strongly polarized and has an ionic nature. The presence of the neighboring Si—F would increase the electronegativity of the Si atom in $=Si\begin{matrix}F\\H\end{matrix}$ significantly and the formation of hydrogen bonding between two hydrophobic Si surfaces

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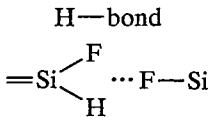
terminated by both hydrogen and fluorine is feasible:



It is also speculated that if an Si-F bond is in sufficient proximity to a H-Si bond and is oriented such that the F can bond with the H of the Si-H bond, the following reaction may be possible (37):

$$Si—F\cdots H—Si$$

Various polymers $(HF)_n$ consisting of hydrogen-bonded HF molecules with n equal to 3 or more are present in gaseous HF and the $(HF)_2$ dimer seems to be less stable than the higher polymers (38). Recently, thermal-desorption spectroscopy results (34, 39) show some physisorbed HF residual molecules on the Si surface after HF dip without a DI water rinse. The distance between two fluorine atoms of $F—H\cdots F$ in a hydrogen-bonded polymer $H—F\cdots H—F\cdots H—F\cdots$ is 2.55 Å (38). The bond angle in the gas polymers is reported to be ~ 140° (38). Crystal chemistry has shown that F ions and OH ions are similar. Not only are they of approximately the same size, but they are also isoelectric (40). It is therefore conceivable that, similar

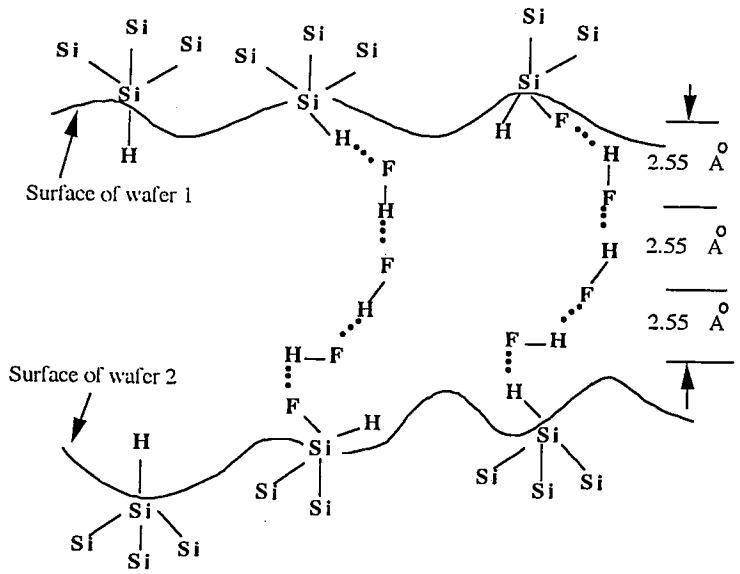


Fig. 4.8 Schematic of HF bridging across the hydrophobic bonding surfaces at room temperature.

to the hydrophilic wafer bonding via hydrogen-bonded water linkages, a cluster of three or more hydrogen-bonded HF molecules may bridge the two mating surfaces so that two surfaces which are separated up to 8 Å can still be bonded by hydrogen bonding (see Fig. 4.8). It is consistent with the fact that although the surface density of Si—F bonds is much smaller ($\lesssim 1 \times 10^{14}/cm^2$) compared to OH groups on hydrophilic Si surfaces ($\sim 4.6 \times 10^{14}/cm^2$) resulting in much smaller bonding energy (10–20 mJ/cm^2 vs. ~ 100 mJ/cm^2), spontaneous room-temperature bonding of the hydrophobic Si wafers with standard surface smoothness is nevertheless achievable (32, 37).

It should be noted that in order to avoid the roughening of the Si surface during an HF dip, very diluted HF aqueous solutions such as 0.6–1% HF have to be used for a short time ranging from 15 sec to 5 min at room temperature.

4.3.3 Surface Activation by Plasma Treatment

4.3.3.1 Plasma Activation via Formation of Surface Bond Defects It has been reported that plasma treatments can activate the Si surface (41). A schematic of a typical plasma activation process is shown in Fig. 4.9. The Si wafers covered with native or thermal oxide are placed in a plasma produced by

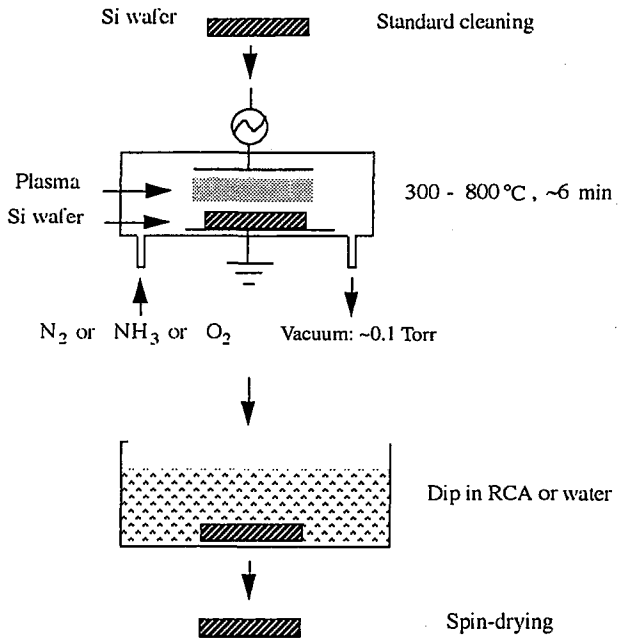


Fig. 4.9 Schematic of plasma-activation process flow.

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low-pressure (~ 0.1 Torr) gas electric discharges at ~ 300°C for 6 min. The plasma-treated surface shows a significantly enhanced chemical reactivity with water and other chemicals to form silanol bonds.

Since the plasma of various gases, including O_2, N_2, and NH_3, results in a similar performance, it is believed that in addition to cleaning the surface, the plasma-induced bond defects on the surface are most likely responsible for the increased chemical reactivity. Compared with room-temperature bonded Si/Si pairs which were treated in standard RCA prior to bonding, a much higher bonding strength (surface energy) has been reported for room-temperature bonded Si/Si pairs whose surfaces were plasma activated (42). A NH_3 plasma treatment has also been applied to activate Si_3N_4 layers on various substrates for low-temperature (90–300°C) bonding (43).

Alternatively, surface activation by oxygen ion bombardment (44) and by depositing a RF magnetron-reactive sputtered SiO_x ($x < 2$) (45) have also been reported.

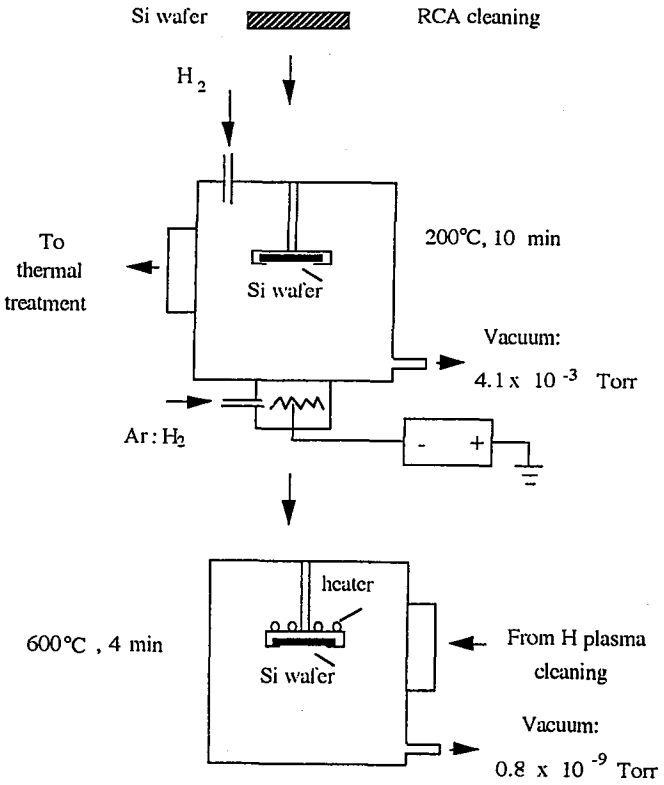

Fig. 4.10 Schematic of hydrogen plasma-cleaning process flow.

4.3.3.2 Plasma Activation via Removal of Surface Layers As described in Section 4.2.3.2, Ar: H = 1:1 hydrogen plasma is able to remove native oxide as well as hydrocarbons from the native oxide-covered Si surface at 200°C for 10 min. The treatment produces a pure hydrogen-terminated Si surface. More than 50% of the terminating hydrogen can be removed by subsequent annealing in UHV at 600°C for 4 min, resulting in a clean and reactive hydrophilic Si surface (46). The process flow of the plasma activation is illustrated in Fig. 4.10.

4.3.4 Surface Activation by UHV Annealing

As discussed in Section 4.2.3.2, the native oxide on the RCA cleaned Si surface can be removed by heating at 850°C for 30 min in UHV at a pressure of less than 2×10^{-8} Torr. The superclean Si surface should be reactive, as evidenced by the fact that it is hydrophilic. By bonding the UHV annealed Si wafers in situ, a near-perfect bonding interface should result since almost no foreign atoms would be present on the mating Si surfaces.

On the other hand, if a selected gas is subsequently fed into the chamber, the Si surface is terminated by the specific molecules. It is one of the potential advantages of the vacuum-based dry-activation processes that a freedom of selection of a desired surface termination prior to bonding is gained for specific applications.

4.4 ROOM-TEMPERATURE BONDING IN A CONVENTIONAL CLEANROOM

After cleaning and activation treatments, two mating Si wafers are brought together face to face in air at room temperature either manually or mechanically. The top wafer is floating on the other owing to the presence of a thin cushion of air between the two wafers. When an external pressure is applied onto a small part of the pair (e.g., by tweezers) to push out the intermediate air, a bond is allowed to be formed by surface attraction forces between the wafers at that location. The bonding area spreads laterally over the entire surface of the wafers within a few seconds. This lateral spreading has sometimes been called a "contacting wave" (47) or a "bonding wave." Infrared photos showing the bonding wave are already given in Fig. 1.1.

If more than one location on the mating pair is initiated to bond simultaneously, corresponding bonding waves can be generated which merge, resulting in trapped air bubbles at the bonding interface. Figure 4.11 shows an example of a large trapped air bubble. To avoid trapped air bubbles, it is important that the bonding wave starts from only one location.

As described in Chapter 3, the interface of the room-temperature bonded pair is extremely sensitive to particulates on the mating surfaces. A particle with diameter of 1 μm can generate an interface bubble with a diameter

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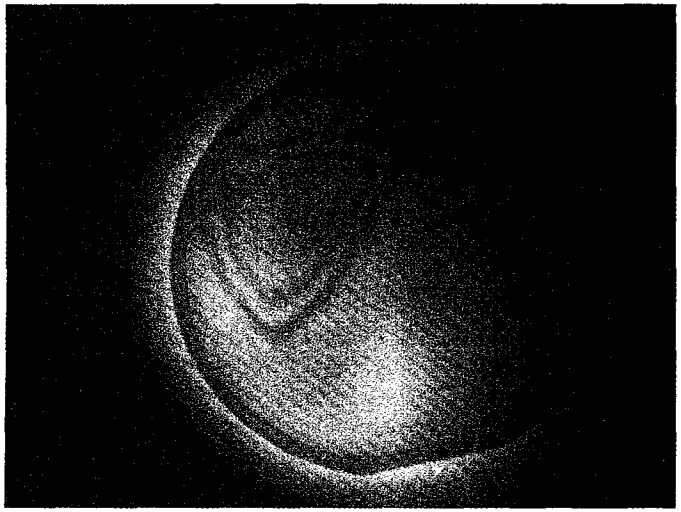

Fig. 4.11 Infrared photos showing spreading of the formation of trapped air bubbles during room-temperature bonding of a hydrophilic Si/Si pair.

which is 5,000 times larger than the particle, that is, 0.5 mm diameter at the bonding interface of a 4-in. standard Si wafer pair. Therefore, it is necessary that room temperature bonding be performed in a clean environment so that particulate recontamination of the cleaned mating surfaces during the bonding process is avoided.

It is natural to adopt the bonding operation to the standard cleanrooms widely used in the semiconductor industry. However, it was found that even in an advanced "Class 1" cleanroom, some of the room temperature bonded wafer pairs contained particulate bubbles (48). This is possible because a "Class 1" environment still has a maximum of 35 particles per cubic foot of air (1240 particles/m^3) with particle size larger than 0.1 μm and a maximum of 1 particle per cubic foot of air ($\sim$ 35 particles/m^3) with particle size larger than 0.5 μm (49). Therefore, an ever cleaner environment and a careful operation are required to enhance the bonding yield.

4.4.1 Manual Bonding

Typically, after cleaning and surface activation, the wafers are spun dry with nitrogen. To avoid surface scratches, vacuum tweezers or tweezers with a specially designed pickup head (e.g., see Fig. 4.12) are preferable.

The two mating wafers are manually placed face to face on a Teflon jig with an inner diameter the same as that of the corresponding Si wafers. The bonding process is monitored by an infrared image-transmission system.

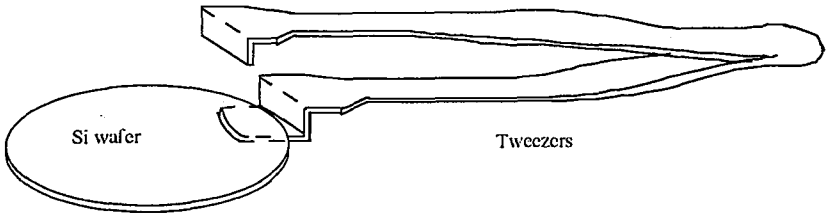

Fig. 4.12 Schematic of a pair of wafer tweezers.

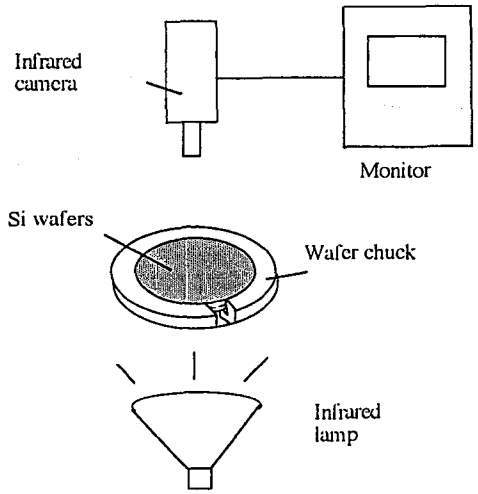

Fig. 4.13 Schematic of a typical manual bonding tool.

Since the top wafer is floating above the other wafer, the rough alignment can be done by rotating the top wafer against the other with reference to either the flat or the patterns of the bonding wafers. The bonding is initiated by pressing one location of the pair to allow the bonding wave to spread over the whole surface. Figure 4.13 is a schematic of a typical manual bonding tool.

4.4.2 Bonding Fixtures and Machines

Several designs of bonding machines have been reported and some examples are described briefly as follows. Figure 4.14 is a schematic of a vacuum-bonding machine developed at Philips Research Laboratories (1). It was originally employed for in situ bonding of two substrates with some pressure applied after coating a metal layer by evaporation in vacuum. The substrates used

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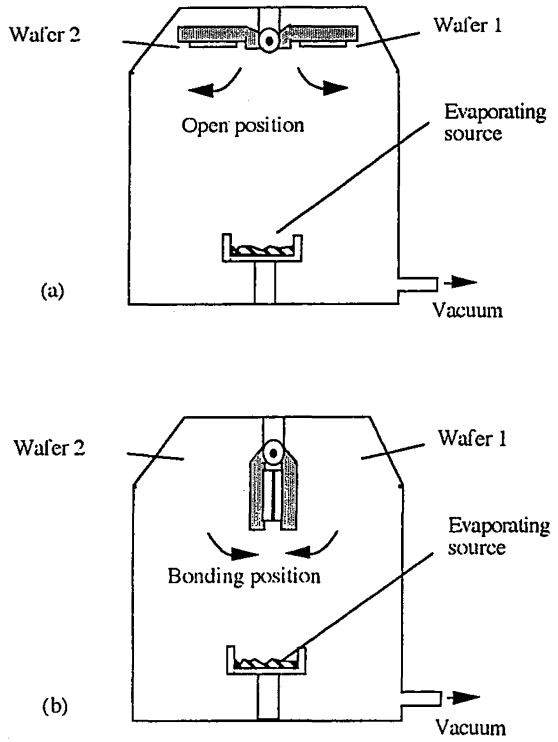

Fig. 4.14 Schematic of metal-bonding setup developed at Philips Laboratory.

included silicon, silica, and ferrites. The metals used were Ti, Cr, Au, Al, Ag, and Ni. The setup is thought to be also suitable for Si wafer bonding in vacuum.

Toshiba developed a bonding machine that holds each wafer on a convex jig surface by vacuum and the vacuum is released upon contacting. The two wafers are contacted starting from one location to finally cover the whole surface with the assistance of the elastically released forces of the wafers.

Researchers at Queen's University of Belfast have used a bonding apparatus shown in Fig. 4.15 (50). The wafers are placed in the PTFE (polytetrafluoroethylene) jig where their flats are aligned to reference flats on the plates and held there by vacuum. Wet chemical cleaning and DI water rinse are performed in situ. The wafers are brought into contact while under 18 MΩ/cm DI water to reduce the chance of recontamination during the bonding operation. The vacuum is removed from one side of the wafer pair and the wafer pair is released from the jig and blown dry in nitrogen. The wafer pair is left in a furnace at 50°C for up to 12 h to allow excess water to escape from the bonding interface.

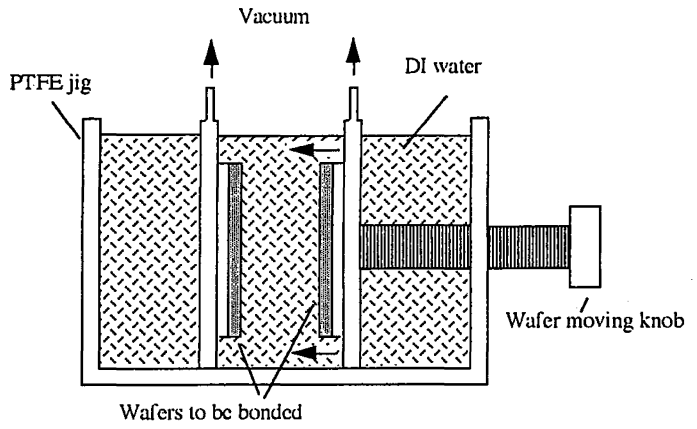

Fig. 4.15 The bonding apparatus developed at Queen's University of Belfast.

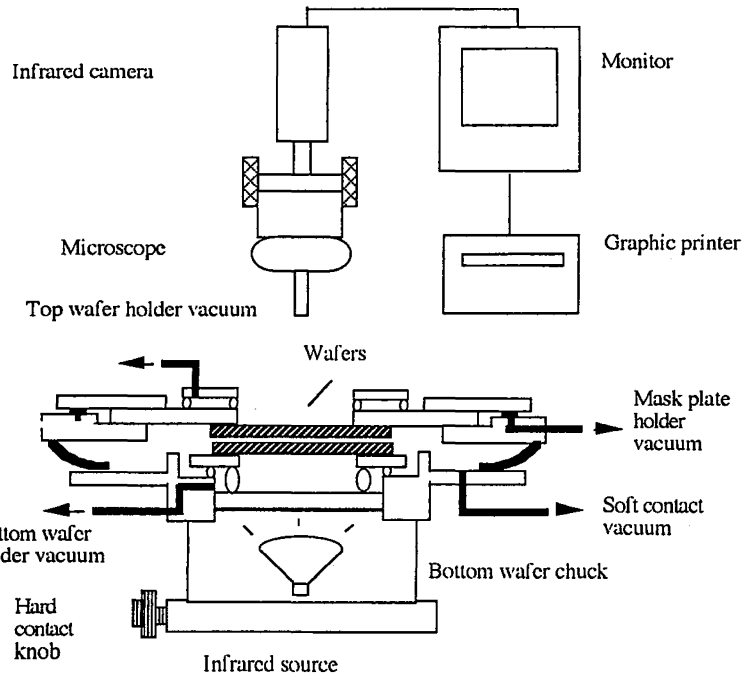

Fig. 4.16 Schematic of the infrared system for aligned wafer bonding developed at the University of California, Davis.

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For wafer bonding requiring precise alignment, the bonding machine is somehow more complicated. A design of such a bonding machine (51), which is capable of aligning wafers with an accuracy of 5 μm, has been reported. A schematic illustration of the machine is shown in Fig. 4.16. The bonding system was a modified Optical Associates Hyperline 400 Infrared Aligner. A fixture was retrofitted to the original mask plate holder and the edges of the top wafer were held by partial vacuum to the upper portion of the alignment column. The bottom chuck plate of the original substrate holder was replaced by an annular metal disk for holding the lower wafer. The design of both upper and lower holders was such that the infrared radiation from a bottom light source is allowed to pass through the two wafers to the imaging camera. The vertical translational control of both the camera and the bottom chuck can bring the focal planes of the two wafers into proximity so that a reasonable focused image of the two wafer surfaces may be viewed simultaneously for alignment operation prior to contacting. Presently, commercial equipment from various vendors is available for aligned wafer bonding.

4.5 ROOM-TEMPERATURE BONDING WITH MICRO-CLEANROOM SETUP

Researchers at Duke University have developed a wafer-bonding machine called the micro-cleanroom setup which allows bubble-free room-temperature bonding outside a cleanroom (48, 52). A schematic of the micro-cleanroom setup is shown in Fig. 4.17. Figure 4.18 is a schematic illustration of the room-temperature hydrophilic wafer-bonding process using the micro-cleanroom setup. The machine is basically a modified spin dryer and is based on the concept that the cleanliness between two mating surfaces is most crucial.

After cleaning and surface-activation treatment, two wafers with hydrophilic surfaces are placed face to face with a gap of approximately 1.5 mm introduced by three polymeric spacers in the setup. Thoroughly filtered 18 MΩ/cm DI water with a pressure of about 20 psi is then flushed through the gap to remove particles from the two mirror-polished wafer surfaces. When the flushing water is stopped, the gap between the wafers remains filled with water owing to the capillary action of the hydrophilic wafer surfaces. After putting a transparent plastic lid over the wafers, the wafers are spin-dryed at 3000 RPM for about 5 min under infrared light from a 250-W infrared lamp. The centrifugal drag forces acting on the particles from the streaming water may detach the loosely adhering particles from the surfaces and water can escape through slits at the edge of the rack.

When water in the gap between the wafers is spun away, the air inside the chamber becomes basically calm during rotating because of the presence

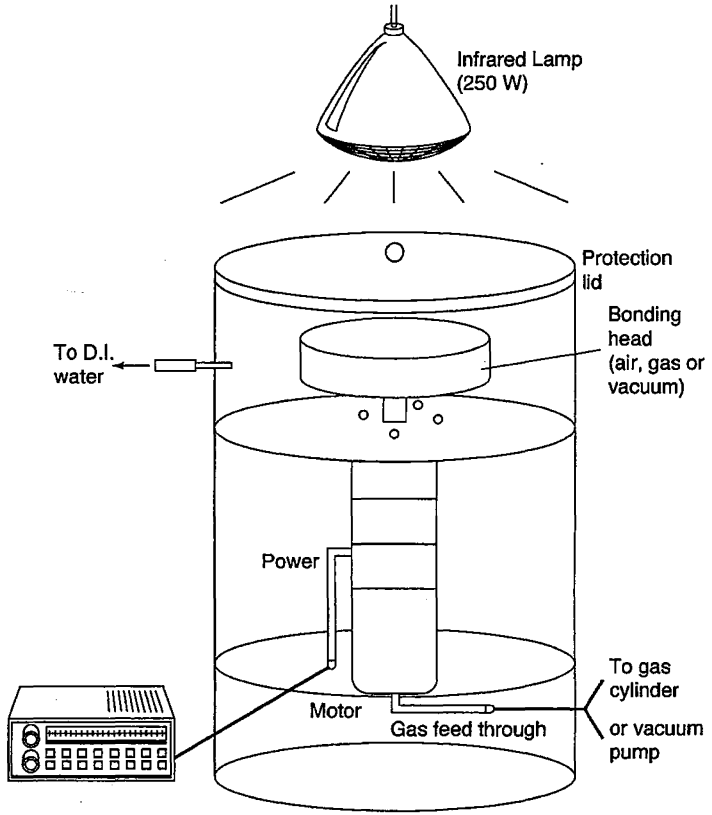

Fig. 4.17 Schematic of the micro-cleanroom setup.

of the lid. Thus, the chance of particulate redeposition is significantly reduced. The temperature of the wafers is about 80–90°C at the end of the spin-drying process.

After removing the three spacers simultaneously by turning the lid against the table without opening it, the top wafer is dropped onto the bottom one and the two wafers are brought into contact. To avoid trapped air pockets, after opening the lid, a tong with Teflon tips is used to press the center of the wafer pair to allow the bonding to begin in the center and then spread radially over the entire wafer. In this way, bubble-free room-temperature bonded wafers can be realized outside of a typical cleanroom.

The micro-cleanroom setup can still be employed for hydrophobic wafer bonding. However, the water flushing and spin-drying steps should be avoided or performed for a short time so that the hydrophilization of the surfaces caused by rapid reaction of Si—F with H_2O to form Si—OH by water or moisture in air (33) can be prevented.

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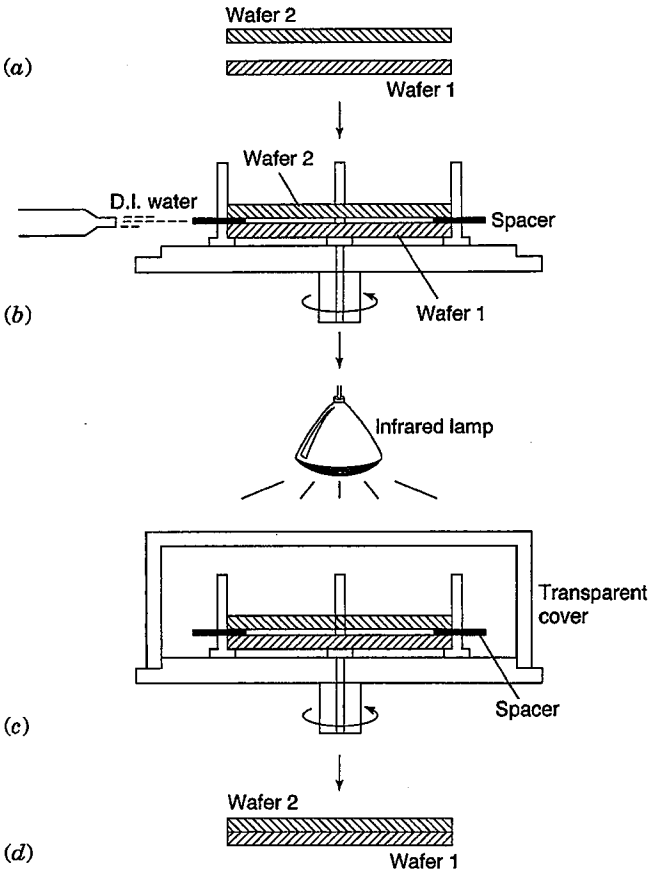

Fig. 4.18 Schematic of wafer-bonding process using a micro-cleanroom setup.

Although the intermediate air at the interface of the bonding pair is mostly squeezed out by the room-temperature bonding process, there are still trapped air pockets in the microgaps at the interface owing to surface microroughness. These microgaps can be eliminated by high-temperature annealing via dissociation of the trapped gas and subsequent diffusion and possible mass migration or viscous flow processes among the interface atoms. However, for bonding of dissimilar materials in which the annealing temperature to strengthen the bond has to be sufficiently low to avoid excess thermal stress, it is desirable to minimize the microtrapped air. To this end a modified micro-cleanroom setup for bonding under low vacuum (~ 1 to 10

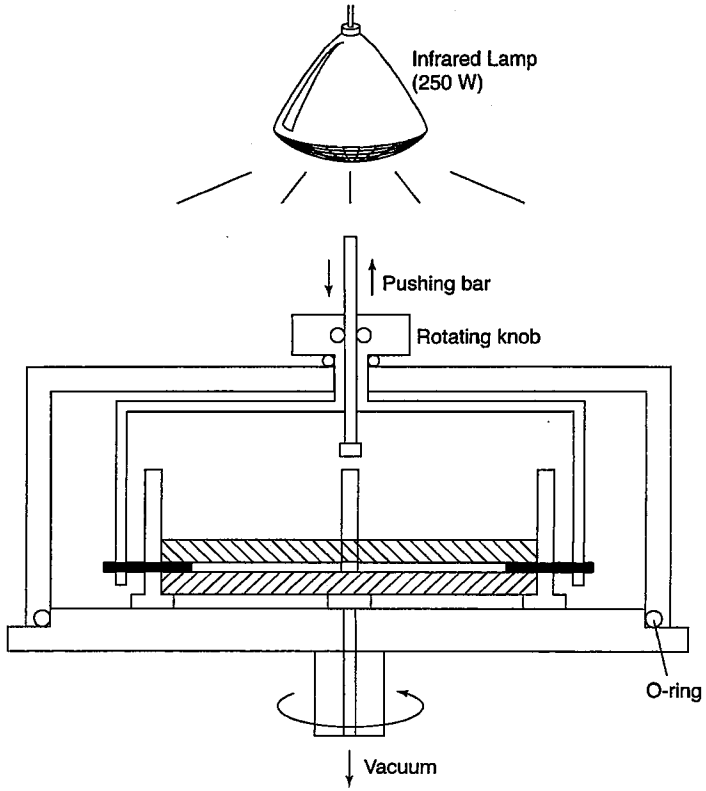

Fig. 4.19 Schematic of the modified micro-cleanroom setup for low-vacuum wafer bonding.

Torr) was developed (53). The schematic of the low-vacuum bonding setup is shown in Fig. 4.19.

Figure 4.20 illustrates the process flow of low-vacuum wafer bonding. During the low-vacuum wafer bonding process, the oil backstream from the pump can contaminate the wafer surfaces and therefore must be avoided. The oil backstream can be eliminated either by using an oil-free pump or by employing a cold trap between the pump and the bonding chamber. The low-vacuum bonding procedures are similar to that of atmospheric bonding except that the vacuum is applied after the wafers are spun dry. The wafers are brought into contact under vacuum and a pin is used to press the center of the pair to initiate the room-temperature bonding.

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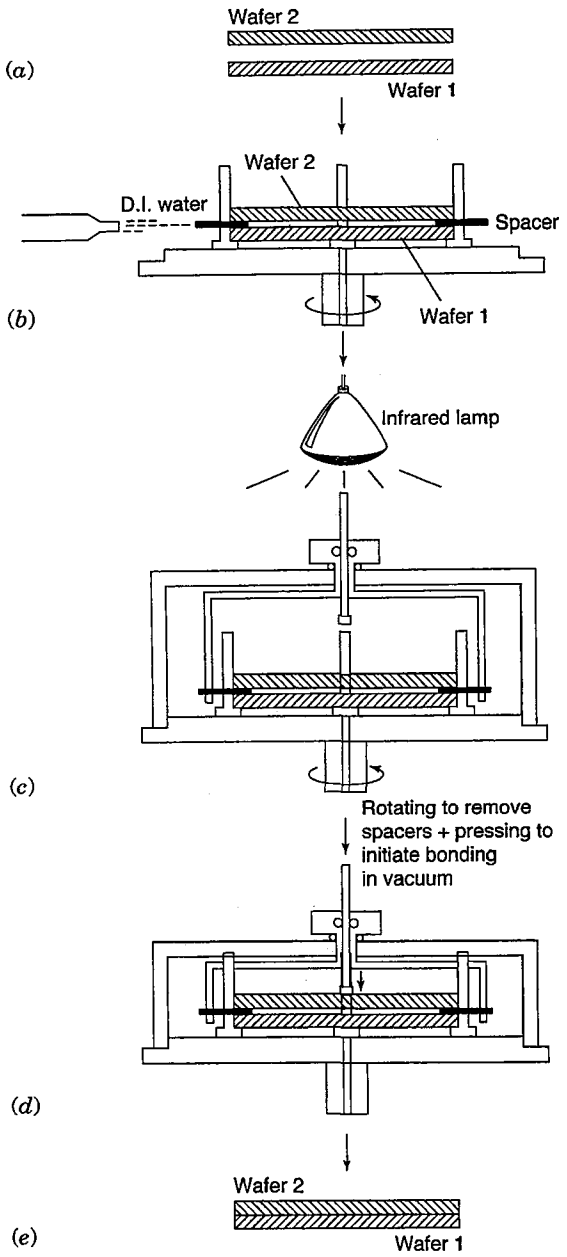

Fig. 4.20 Process flow of wafer bonding in low vacuum.

4.6 INITIATION AND PROPAGATION OF BONDING FRONT

It has been found that during room-temperature wafer bonding, the speed of the bonding wave is mainly determined by the rate of squeezing out the trapped air between the two bonding wafers. Since the hydrophilic or hydrophobic bonding can be considered as nearly reversible within a relatively short time after room-temperature bonding, the behavior of the bonding process may be represented reasonably well by the rebonding process.

Experiments were conducted in which a razor blade was inserted into the bonding seam at the edge of a room-temperature bonded, hydrophilic Si/Si pair under normal air pressure and under reduced air pressure (37, 54). Figure 4.21 shows schematically the top view of the basic equipment used for the experiments. The crack that had been generated by inserting a razor blade was rebonded (closed) again upon withdrawal of the blade. The speed of the rebonding wave increased drastically from 1.9 cm/s when the operation was performed in air at a pressure of 1 atm, to 50 cm/s when rebonding occurred in a chamber of reduced pressure of $\sim 3 \times 10^{-1}$ Torr.

Figure 4.22 shows the measured bonding speed of both hydrophilic and hydrophobic Si pairs as a function of the pressure in the bonding chamber. It is clear that the bonding speed increases as the pressure in the chamber decreases. By filling the chamber with gases of varying viscosities (argon, air, helium, and neon), Fig. 4.23 demonstrates that the measured rebonding speed of hydrophilic Si wafers is higher when rebonding is performed in the ambient gases with lower viscosities.

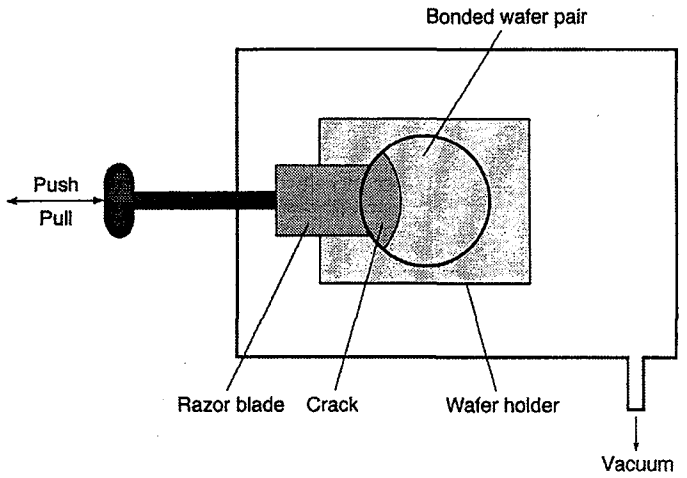

Fig. 4.21 Schematic top view of equipment used for rebonding the crack generated by inserting a razor blade in vacuum.

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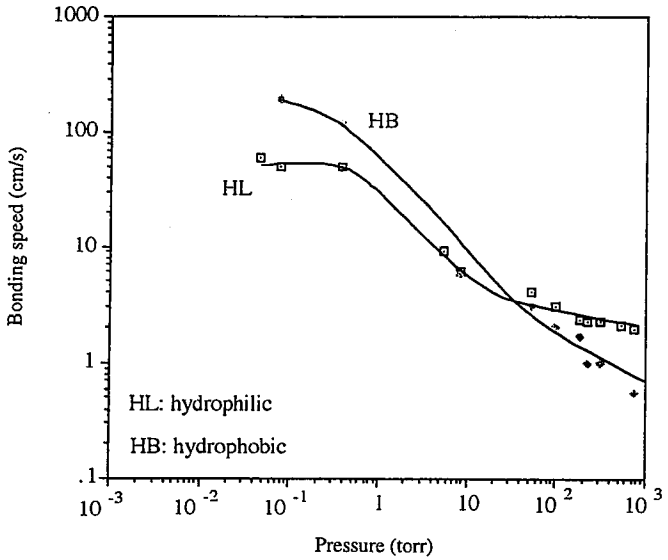

Fig. 4.22 Rebonding speed versus pressure of room-temperature bonded hydrophilic and hydrophobic Si/Si pairs.

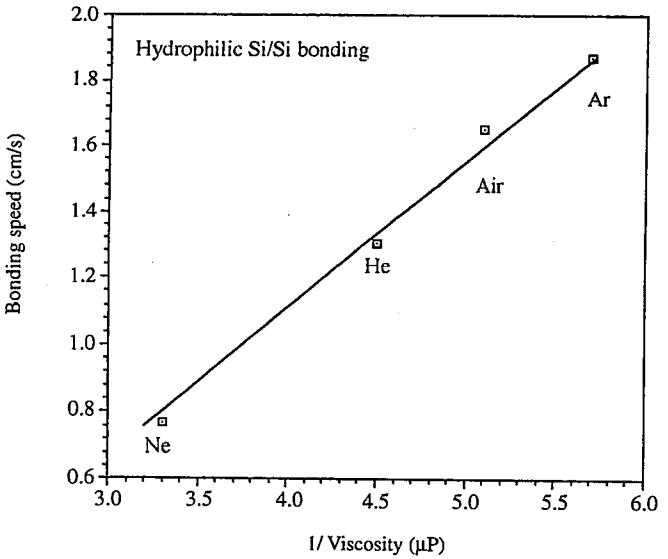

Fig. 4.23 Rebonding velocity of hydrophilic Si/Si pair versus ambient gas viscosity.

Upon removal of the razor blade the attraction forces at the edge of the bonded area are exerted on the gas in the crack. The attraction forces can be transferred to a force in the direction of pushing the gas out of the crack. The unit-area frictional force F acting on the gas along the two wafer surfaces is proportional to the viscosity η of the gas and the velocity gradient $\partial v/\partial y$ vertical to the surfaces:

$$F = \eta \frac{\partial v}{\partial y} \tag{4.7}$$

Since the velocity of the gas next to the wafers is zero (55), it is clear that the gas is squeezed out of the crack with higher velocity when the gas viscosity is lower. The bonding speed is independent of the distance of the bonding front to the rim and also independent of the thickness of the wafers. [In contrast, the bonding speed was found to decrease with the thickness of the bonding wafers by Bengtsson et al. (56), who showed that in the case of bonding wafers with exactly the same material and thickness t, the bonding speed decreases with $t^{3/2}$.]

Upon completion of room-temperature bonding, the two surfaces conform to each other macroscopically by elastic deformation. The contacted area at the bonding interface can be considered as the area between the two wafers in which van der Waals attraction forces, including hydrogen bonding, are effective. This requires a mean microroughness of the bonding surfaces of less than 5 and 4 Å for hydrophilic and hydrophobic Si wafer bonding, respectively, as discussed above. Owing to the presence of the surface microroughness, only a fraction of the surface is actually contacted, which results in many microgaps at the room temperature bonded interface. The

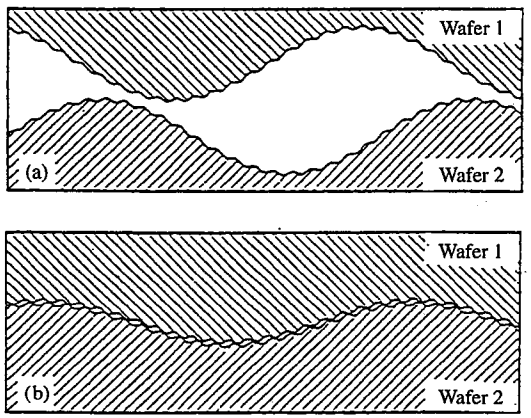

Fig. 4.24 Schematic of bonding interface of low-temperature annealed pairs: (a) Before bonding and (b) after annealing

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resultant interface of the room temperature bonded pair is illustrated schematically in Fig. 4.24. The close of the microgaps is usually achieved by strengthening the bond and by mass migration and/or viscous flow of the surface atoms during high-temperature annealing. However, for hydrophilic Si wafer pairs bonded at room temperature under low vacuum, after annealing at temperatures as low as 150°C for ~ 100 h, a strong bond close to that of thermal oxide was formed at the bonding interface. This phenomenon suggests that most of the interface microgaps were filled during the long annealing at ~ 150°C, possibly because of enhanced oxidation under a high water vapor pressure in the gap (53).

4.7 INTERFACE OF ROOM-TEMPERATURE BONDED SI PAIRS

4.7.1 Interface of Room-Temperature Bonded Hydrophilic Si Pairs

The chemical species at the interface of room-temperature bonded Si/Si pairs can be measured through the multiple internal transmission IR adsorption spectroscopy method (57). The principle of the method is illustrated in Fig. 4.25. The bonded samples with a total thickness of 1 mm are cut to a 3.8 × 1.5 cm rectangular shape and the short ends of the samples are beveled at 45°. The IR radiation is internally reflected at the outer surfaces and exits the sample after passing 38 times through the bonding interface, resulting in an enhancement for adsorption perpendicular to the interface. Compared to the interface adsorption, the outer surfaces' contributions may be negligible. The measured IR adsorption spectra of room temperature bonded hydrophilic Si/Si pairs confirm the presence of OH groups and indicate 2–3 monolayers of water at the interface (57).

There are various possible arrangements for the silanol groups to adsorb water molecules. Figure 4.26 illustrates some of the postulated arrangements (58–61). When the two hydrophilic Si surfaces with adsorbed water are brought into intimate contact, hydrogen bonds develop between the adsorbed

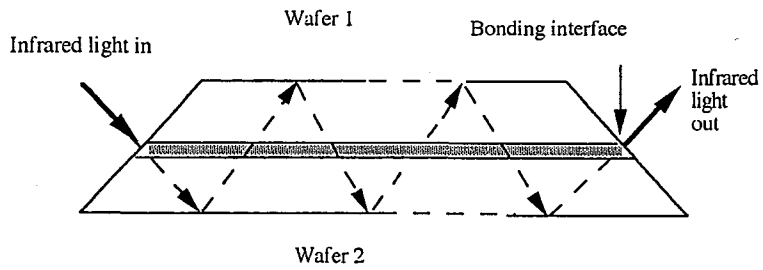

Fig. 4.25 Schematic diagram of the principle of the multiple internal transmission infrared adsorption spectroscopy method.

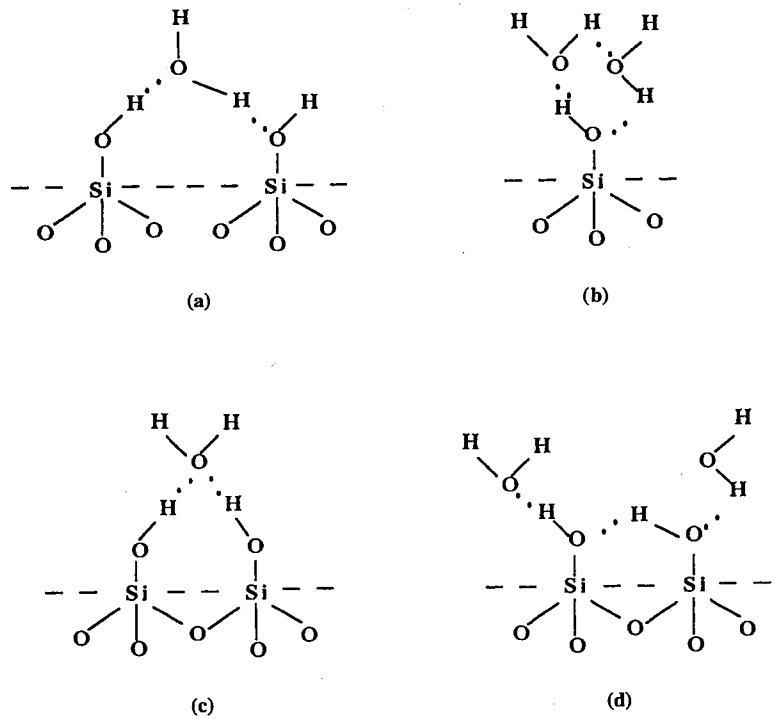

Fig. 4.26 Possible arrangements of absorbed molecular water on isolated—*a* (55), *b* (54), and *c* (57)—and associated—*d* (56)—silanol groups.

water molecules across the two surfaces. The resultant interface structures are likely to be complicated and surface condition dependent. However, for a rough quantitative estimate of the bonding strength, we can assume that there is one adsorbed monolayer of water on each surface and that not only associated but also isolated silanol groups can adsorb water molecules. One of the possible interface structures of room-temperature bonded hydrophilic Si/Si pairs is shown in Fig. 4.27*a* for the associated silanol groups and in Fig. 4.27*b* for the isolated silanol groups (58). It is clear from Fig. 4.27 that for each bonding surface there are two hydrogen bonds formed at the bonding interface by **one pair** of associated silanol groups while one isolated silanol group can form **two** interface hydrogen bonds.

The energies of OH ··· O hydrogen bonds are generally from 2 to 10 kcal/mol (62). The energy of the OH ··· O hydrogen bond between a silanol group and adsorbed water may also be different from that between water molecules. Moreover, because of the complications of the possible pairwise nonadditivity of the energy of a cluster of hydrogen bonds between water

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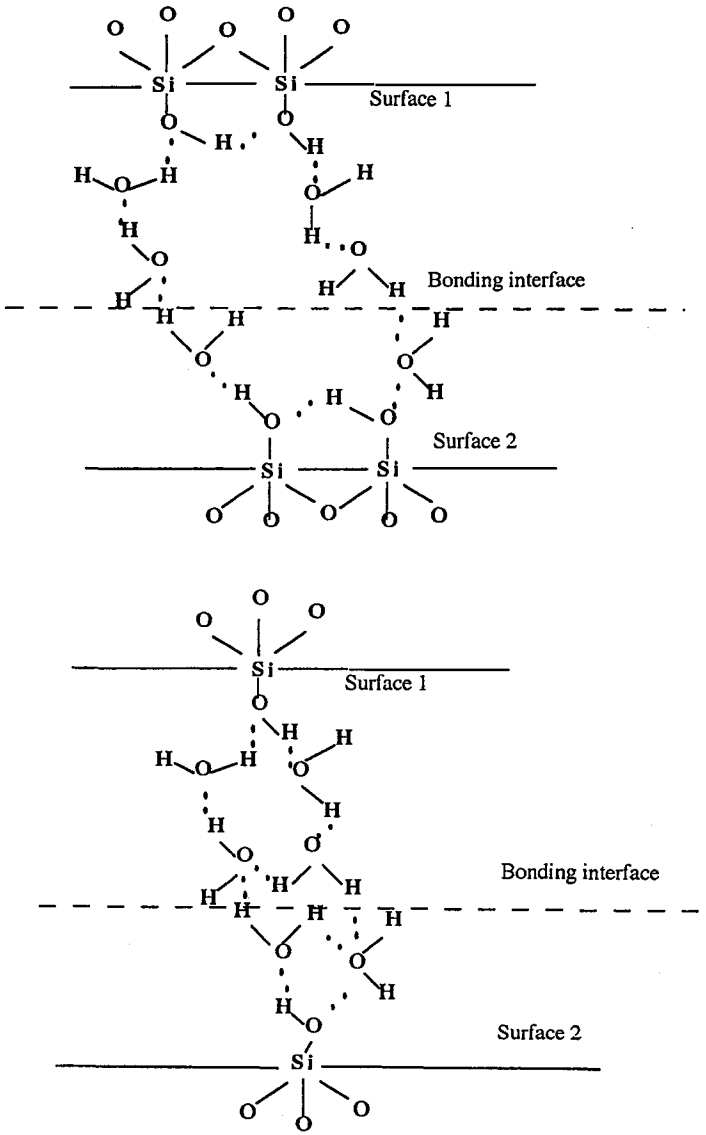

Fig. 4.27 Postulated interface chemical structures of hydrophilic Si/Si pairs immediately after RT contacting: (*a*) at an associated silanol site and (*b*) at an isolated silanol site.

TABLE 4.7 Representative Measured and Calculated Values of Energies E_h of OH ··· O Hydrogen Bonds

Calculated E_h in H_2O Dimer (63)	4.72 kcal/mol	E_h of H_2O adsorbed on associated SiOH (65)	6.6–8.2 kcal/mol
E_h in Ice (50)	5.0 kcal/mol	E_h of H_2O adsorbed on isolated SiOH (65)	10 kcal/mol
Calculated Lowest E_h in H_2O Dimer (64)	6.09 kcal/mol	E_h of SiOH:OH_2 (66)	6.0 kcal/mol
Calculated E_h in H_2O Trimer in Chain (64)	7.09 kcal/mol	E_h of (SiOH:OH_2):OH_2 (66)	10.5 kcal/mol

molecules and its dependence on distance and orientations, the actual value of the energy of the OH ··· O hydrogen bond at the bonding interface is not clear. Table 4.7 lists some representative measured and calculated values of the energies E_h of OH ··· O hydrogen bonds.

According to Table 4.7, it may be reasonable to adopt 6.0 kcal/mol as the energy of the OH ··· O hydrogen bond between water and the associated silanol groups. The energy of the hydrogen bond between water molecules, or that between water and the isolated silanol groups, can be approximated as 10 kcal/mol (67).

To separate a bonded pair, we need to break the bond by applying an interface energy. It will generate two surfaces. The surface energy of each separated surface is half of the value of the bond energy of the pair, that is, the interface fracture energy. Assuming all surface silanol groups adsorb water molecules and all interface water molecules are connected by hydrogen bonds across two surfaces, the specific surface energy γ of the room-temperature bonded hydrophilic Si/Si pair may be estimated as follows:

$$\gamma = \frac{1}{2}(2d_{OHi}E_{hi} + d_{OHH}E_{hH}) \tag{4.8}$$

where d_{OHi}, d_{OHH} and E_{hi}, E_{hH} are the surface density of silanol groups and the hydrogen bond energy of the isolated and the associated silanol groups, respectively.

The following values may be adopted for Eq. (4.8):

$$d_{OHi} = 1.4 \times 10^{14}\ \text{cm}^{-2}$$

$$d_{OHH} = 3.2 \times 10^{14}\ \text{cm}^{-2}$$

$$E_{hi} = 10\ \text{kcal/mol} = 7 \times 10^{-17}\ \text{mJ/bond}$$

$$E_{hH} = 6\ \text{kcal/mol} = 4.2 \times 10^{-17}\ \text{mJ/bond}$$

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The surface energy of room-temperature bonded hydrophilic Si/Si pairs can then be calculated:

$$\gamma = \frac{1}{2}(2d_{OHi}E_{hi} + d_{OHH}E_{hH})$$

$$= 1/2(2 \times 1.4 \times 10^{14}/\text{cm}^2 \times 7 \times 10^{-17}\text{mJ}$$

$$+3.2 \times 10^{14}/\text{cm}^2 \times 4.2 \times 10^{-17}\ \text{mJ})$$

$$= 165\ \text{mJ/m}^2$$

The average measured value of the surface energy of the room-temperature bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pair immediately after bonding is 80, 60, and 50 mJ/m^2, respectively. This would suggest that about 50, 40, and 30% of the surface area in the Si/Si, Si/SiO_2, and SiO_2/SiO_2 pair, respectively, would be in contact via hydrogen bonding at the bonding interface. However, if the diversity of surface energies resulted only from the surface microroughness, it would not cause a large range of contact area percentage between Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs, which have almost identical surface microroughness (~ 1 Å). It is therefore possible that the surface silanol densities are different between these pairs.

The native oxide is strained and hydrophilic. The surface of thermal oxide is less strained than that of native oxide, as evidenced by the fact that for a silica surface annealed to high temperature (> 900°C) the rehydration in water is extremely slow at a time scale of many years (31). Although a surface activation treatment can significantly increase the silanol density on the thermal oxide surface, there will be more silanol groups generated after an identical surface activation treatment on an Si surface covered by native oxide than that on a thermal oxide surface.

There are three main processes taking place during room-temperature storage after room-temperature bonding: (1) the interface molecular water is continuously reacting with the bonding surfaces to generate more silanol groups (slow fracture effect); (2) the interface water molecules can rearrange themselves to reach an energetically more favorable state; and (3) some of the interface water molecules may migrate out of the bonding interface and/or can diffuse into the surrounding oxide. The first reaction results in an increase of surface silanol density with time, finally reaching the saturated value of 4.6 OH/nm^2. The second process leads to a water rearrangement at the interface which is energetically more favorable. The last effect would allow silanol–silanol interaction, that is, direct hydrogen bonding and polymerization of the silanol groups, to occur across the two bonding surfaces if the local separation can be about 4 Å via an elastic deformation (26).

Experimental data have shown that after room-temperature storage for a long period of time (e.g., ~ 100 days), the bonded hydrophilic Si/Si, Si/SiO_2,

TABLE 4.8 Typical Surface Energy (mJ/cm^2) of Bonded Hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 Pairs

	Si/Si	Si/SiO_2	SiO_2/SiO_2
RT bonded	83	59	52
~ 100-day storage	241	250	233

and SiO_2/SiO_2 pairs reached a similar surface energy in the range of 230 to 250 mJ/m^2 even though their original surface energies immediately after room-temperature (RT) bonding are quite different (see Table 4.8). Since the surface mean microroughness of Si and SiO_2 is almost identical, it is likely that upon completion of the slow fracture effect, there are almost identical surface densities of silanol groups on the Si and the SiO_2 surfaces.

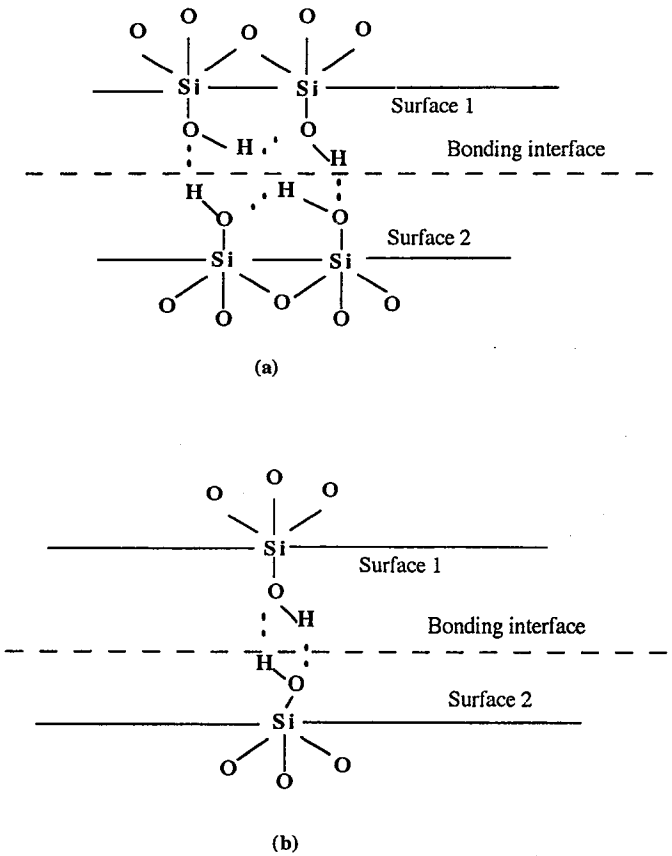

Fig. 4.28 Hydrogen bonds at interface of hydrophilic Si bonding pairs after removal of molecular water: (*a*) at an associated silanol site and (*b*) at an isolated silanol site.

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To roughly estimate the surface energy of a hydrogen-bonded pair after RT storage, we assume an extreme case in which the interface molecular water is completely removed and both isolated and associated silanol groups interact directly across the bonding surfaces. On each surface of the bonding pair one isolated silanol group can form two hydrogen bonds while one pair of associated silanol groups is needed to form two hydrogen bonds; a possible arrangement of the interface bonds is schematically presented in Fig. 4.28.

As seen in Fig. 4.28, both associated and isolated silanol groups at the bonding interface form a cyclic structure, similar to that in water polymers. The energy of the hydrogen bond in a cyclic polymer of water is higher than that in a chain (64). There are four hydrogen bonds in the cyclic structure of the associated silanol groups (see Fig. 4.28*a*); therefore, we may use the energy of the hydrogen bond in a cyclic tetramer E_{h4} of 9.8 kcal/mol (64) as the bond energy of this structure. Similarly, the bond energy E_{h2} of the cyclic isolated silanol groups (see Fig. 4.28*b*) may be approximated as that of an open-chain water trimer (6.09 + 1 kcal/mol) which has a similar structure with two hydrogen bonds (64). Using these values, the surface energy of the bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs can be calculated by

$$\gamma = \frac{1}{2}(2d_{OHi}E_{h2} + d_{OHH}E_{h4})$$

$$= 1/2(2 \times 1.4 \times 10^{14}/\text{cm}^2 \times 7.09 \text{ kcal/mol} + 3.2 \times 10^{14}/\text{cm}^2 \times 9.8 \text{ kcal/mol}) \times 7 \times 10^{-18} \text{ mJ/kcal/mol}$$

$$= 179 \text{ mJ/m}^2 \qquad (4.9)$$

The calculated value of 179 mJ/m^2 is less than the measured maximum value ($\sim$ 240 mJ/m^2) of the surface energy of the bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs. It is suggestive of some other mechanisms involved in the storage process.

It is known that the polymerization of silanol groups can occur even at room temperature if the silanol groups are close enough and are hydrogen bonded (26):

$$\text{Si—OH} + \text{HO—Si} \longrightarrow \text{Si—O—Si} + \text{H}_2 \qquad (4.10)$$

The reaction is reversible at temperatures less than $\sim$ 425°C. As molecular water is migrating or diffusing away from the bonding interface during RT storage, the polymerization of the hydrogen-bonded silanol groups across the wafers to form some siloxane bonds at the interface appears to be feasible. Therefore, it can be understood why after a long storage at RT, the surface energy of the bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs is greater than that calculated from pure hydrogen bonding.

However, most molecular water adsorbed by silanol groups can only be removed from silica upon heating above about 120°C (12, 65). The molecular water that is still present at the bonding interface may rehydrate the mating surfaces and results in formation of limited equilibrium siloxane bonds:

$$\text{Si—OH} + \text{OH—Si} \underset{\text{slow fracture}}{\overset{\text{polymerization}}{\rightleftharpoons}} \text{Si—O—Si} + \text{H}_2\text{O} \qquad (4.11)$$

We discuss the thermal treatment of the bonded wafer pairs in Chapter 5.

4.7.2 Interface of Room-Temperature Bonded Hydrophobic Si Pairs

As discussed in Section 4.3.2.2, Si wafers dipped in HF without DI water rinse can bond to each other readily. It has been speculated that hydrogen bonding between the two hydrophobic surfaces is formed through a linkage of three or more HF molecules, as shown in Fig. 4.8.

For a simple estimate, we assume that each Si—F bond on each of the mating surfaces contributes to form one hydrogen bond across the wafers and other weaker hydrogen bonds, if present, are omitted. The surface energy γ of the RT bonded hydrophobic Si/Si pairs can be estimated by the following equation:

$$\gamma = \frac{1}{2}(2d_{Si-F}E_{hHF}) \qquad (4.12)$$

where d_{Si-F} is the surface density of Si—F bonds and E_{hHF} is the lowest bond energy of the hydrogen-bonded HF cluster across the two mating surfaces.

It has been reported that there is an 0.12 monolayer (23) or $\leq 1 \times 10^{14}/\text{cm}^2$ (33) of Si—F bonds present on the (100) Si surface which is almost constant for Si wafers dipped in HF of concentration in the range of 0.3 to 20% without subsequent DI water rinse (23).

If we use the smaller number of Si—F bonds ($\leq 1 \times 10^{14}/\text{cm}^2$) and the average energy, E_{hHF}, per F—H···F hydrogen bond of 6.02 kcal/mol (69) as the weakest bond energy in the bonding bridge (i.e., assuming the bond energy of Si—H···F—H is also E_{hHF}), we obtain the surface energy γ of the RT bonded hydrophobic Si/Si pair according to Eq. (4.12):

$$\gamma \leq 1/2(2 \times 1 \times 10^{14}/\text{cm}^2 \times 6.02 \text{ kcal/mol} \times 7 \times 10^{-18} \text{ mJ/kcal/mol})$$

$$\leq 42 \text{ mJ/m}^2$$

Experimentally, the surface energy γ of the RT bonded hydrophobic Si/Si pairs of 10–20 mJ/m^2 has been observed, indicating that, owing to surface microroughness, only a fraction of the surface is actually in contact.

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4.8 THICK-WAFER BONDING

There is a growing interest in bonding of wafers with thickness different from standard Si wafers, as is often required by micromechanical applications such as heat sinks or sensors. For thick-wafer bonding, besides an adequate surface smoothness and reactivity, a sufficient surface flatness of the mating wafers becomes also crucial. Since the mating surfaces are never perfectly flat, a sufficient elastic deformation of each wafer has to be introduced by the bonding process to close up the macroscopic gaps at the bonding interface (56). The elastic deformation becomes increasingly difficult as the thickness of bonding wafers increases.

As discussed in Section 3.2 for bonding Si wafers with standard thickness, for thick-wafer bonding, in most cases it is still reasonable to assume that the interface gaps have a lateral extension R which is much larger than the gap height $2h$ and wafer thickness t, see Fig. 4.29. We may use the simple theory of small elastic deflections to estimate the surface gap height h of each wafer with which the gaps can still be closed during the bonding process, as described in Chapter 3, Section 3.3.

Assuming that the two bonding wafers have the same thickness, for Si/Si wafer bonding at room temperature, Fig. 3.13 illustrates the design curves of Eqs. (3.13) and (3.14) for bonding of Si pieces with various thicknesses. The parameter space of gap parameters for which the gaps can be closed is located above the corresponding curve with a given wafer thickness. The surface energy of the RT bonded Si/Si pairs is assumed to be 100 mJ/m^2. Similar design curves for other material combinations such as Si/quartz and Si/ZnS pairs may also be obtained.

These results suggest that, for a successful RT bonding, there appears to be no upper limit to the thickness of the bonding pieces if the mating surfaces are sufficiently flat. The thicker the thinner piece of the bonding pair becomes, the less flatness error of the surfaces can be tolerated.

According to Eqs. (3.13) and (3.14), for successful RT bonding of two 20-mm thick Si pieces, surface gaps with h less than 0.6 μm and $2R$ equal to 100 mm are required. It has been found that after standard Si wafer polishing, the two Si pieces could not bond to each other at RT because they did not meet the flatness requirement. However, when a commercially available optical polishing technology was used to achieve a surface flatness

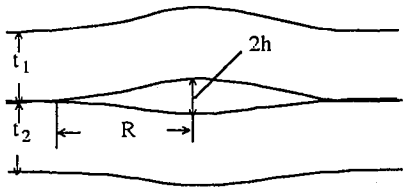

Fig. 4.29 Schematic of gaps between wafers for the case of $R > 2t$.

variation of 630 Å over 100 mm, RT bonding of the two 20-mm thick Si wafers was successful and spontaneous after standard surface cleaning and activation treatments (70). A pair of 19-mm thick, 100-mm diameter quartz wafers which were optically polished to a flatness variation of 639 Å over 100 mm also spontaneously bonded at room temperature (70).

The Si pieces prepared by optical polishing may suffer from subsurface damage, but that may not be of major concern for applications such as those in micromechanics. As downscaling of the device advances, the VLSI industry is also pursuing polishing technologies that can better control the surface smoothness and flatness without subsurface damage. This effort will obviously benefit the development of thick-wafer bonding.

4.9 DEBONDING (71)

Sometimes RT bonded wafer pairs need to be separated (i.e., debonded). For example, debonded wafers can be recleaned before rebonding to gain a higher yield of wafer-bonding process. As VLSI complexity advances, the storage of wafers in plastic boxes appears to be no longer adequate owing to possible organic contamination of wafer surfaces from the plastic containers (72). Reversible RT bonding of bare hydrophilic (73) or hydrophobic (37) Si wafers has been suggested as one promising remedy for the contamination problem associated with transport and storage in plastic containers. RT bonding of bare Si wafers effectively protects the bonded surfaces from organic contamination and from particles (73, 74).

There is a basic assumption that RT bonding is a reversible process, which means that there would be no damage or contamination introduced by the debonding process. As discussed in Chapter 5, the dominating reaction at the interface of the bonded hydrophilic Si/Si pairs in the range from room temperature to 110°C is the rearrangement of molecular water at the interface; therefore, it can still be considered as basically reversible over this temperature range.

The bonded wafers have to be separated again immediately before use in device processing. However, as wafer sizes get larger, the separation (debonding) of RT bonded wafers becomes increasingly difficult because thicker wedges and/or deeper inserting distance into the bonding interface are required to separate the bonded wafers, which may lead to scratching of the wafer surfaces or even to breaking of the wafers. Moreover, as described above, the surface energy of RT bonded hydrophilic wafers can be notably increased even at RT after long storage. A fairly high temperature (around 100°C) and long storage period could involuntarily occur during the transport of reversibly bonded wafers from wafer manufacturers to wafer users. The increased bonding energy is obviously undesirable for the debonding process. Therefore, an effective method to easily separate RT bonded wafers up to 8 in. in diameter is highly desirable.

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4.9.1 Physics Background and Modeling

As discussed in Section 2.2, a crack-opening method was used to characterize the surface energy of bonded pairs. In this method, a blade with thickness t_b is inserted between two wafers of a bonded pair, the two wafers are bent around the inserted region, and a crack is generated. The equilibrium crack length L is given by

$$L = \sqrt[4]{\frac{3Et_w^3t_b^2}{32\gamma}} \tag{4.15}$$

where γ is the interface energy, t_w is the thickness of each of the wafers, and E is Young's modulus. It should be noted that two surfaces, each with specific surface energy γ, are generated as the wafers are separated. Equation (4.15) is derived for the symmetrical case, that is, two identical wafers are bonded and the two wafers are symmetrically bent in the separation region. Hereafter, we will term this the "two-wafer bent" case.

For bonding of wafers with dissimilar materials identified by subscripts 1 and 2, the equation above can be rewritten as

$$L = \sqrt[4]{\frac{3t_b^2E_1t_{w1}^3E_2t_{w2}^3}{16\gamma(E_1t_{w1}^3 + E_2t_{w2}^3)}} \tag{4.16}$$

where the average surface energy γ of the bonded pair can be expressed approximately as

$$\gamma = (\gamma_1 + \gamma_2)/2 \tag{4.17}$$

where γ_1 and γ_2 are the surface energies of material 1 and 2, respectively.

For easy separation, a crack length as long as possible is desirable. According to Eq. (4.15), for a given γ, an increase of the thickness of the wafers or of the blade, or an increase of the value of Young's modulus, leads to an increased crack length. However, the thickness of silicon wafers t_w is fixed by industrial standards and the blade thickness must have a reasonable value to avoid the introduction of any damage to the silicon wafer surfaces during the separation procedure. Young's modulus increases with decreasing temperature. The relative temperature coefficient $(dE/E)(1/dT)$ of silicon's Young's modulus is about -8.5×10^{-6} ($°C^{-1}$) which is not significant (75).

On the other hand, lowering the surface energy γ will enhance the crack length. One way to reduce is to lower the separation temperature, but experimental results have shown that only about a 12% reduction of γ can be accomplished by lowering the temperature from 23 to $-90°C$. A more effective method to increase the crack length is based on combining a "one-wafer bent" concept and a water-enhanced increase of the equilibrium crack length (71).

4.9.2 One-Wafer Bent Concept

In the case that a bonded wafer is sucked down onto a solid chuck by a vacuum pump, only the upper wafer of the bonded pair can be bent around the blade-inserted region. Hereafter, we term this the "one-wafer bent" case. The equilibrium crack length L can be determined similarly to the two-wafer bent case:

$$L = \sqrt[4]{\frac{3Et_w^3t_b^2}{16\gamma}} \tag{4.18}$$

In Eq. (4.18), t_w refers to the thickness of the bent wafer. The thickness of the unbent wafer does not enter Eq. (4.18). Comparing Eq. (4.15) to Eq. (4.18), we see that if other parameters are identical in the one- and the two-wafer bent cases, the crack length L_1 in the one-wafer bent case will be longer than the crack length L_2 in the two-wafer bent case. Quantitatively, it turns out that $L_1 = 1.19\ L_2$. This implies a 19% increase in the equilibrium crack length in the one-wafer bent case compared with the two-wafer bent case, as shown schematically in Fig. 4.30. This increased crack length

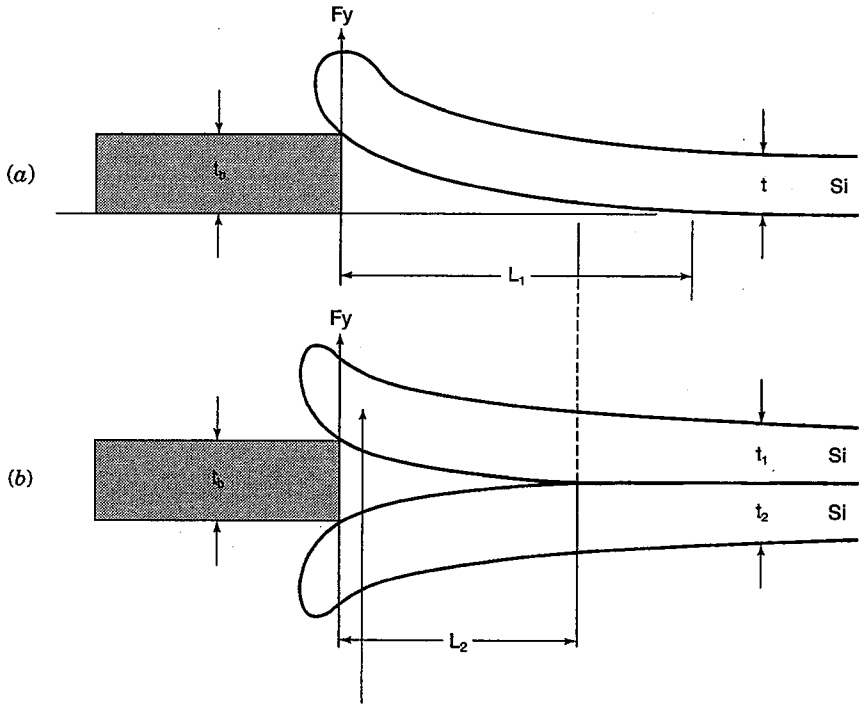

Fig. 4.30 Schematic diagram showing the difference between (*a*) one-wafer bent and (*b*) two-wafer bent case.

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is equivalent to a 50% decrease of the surface energy in the two-wafer bent case.

This analysis is also applicable to asymmetrical or dissimilar material bonding, for example, a silicon wafer covered with a native oxide bonded to a thermally oxidized silicon wafer, or Si bonded to ZnS. The crack length can be expressed as

$$L = \sqrt[4]{\frac{3t_b^2 E_i t_{wi}^3}{16\gamma}} = \sqrt[4]{\frac{3t_b^2 E_i t_{wi}^3}{8(\gamma_1 + \gamma_2)}} \tag{4.19}$$

where i refers to the wafer which is bent and γ_1 and γ_2 are the surface energies of mating material 1 and 2, respectively.

4.9.3 Water-Enhanced Crack Opening

Close inspection of the assumption under which Eq. (4.15) has been derived shows that the specific surface energy γ is actually the effective specific energy γ_{eff}^{m} required to get the interface from the bonded state with specific energy $\gamma_{s,s}$ to the debonded state in a certain medium with specific surface energy $\gamma_{m,s}$:

$$\gamma_{eff}^{m} = \gamma_{m,s} - \gamma_{s,s} \tag{4.20}$$

The medium usually chosen is air with an unspecified amount of humidity. Since $\gamma_{m,s}$ and therefore γ_{eff}^{m} varies with the debonding medium, the equilibrium crack length L can be strongly influenced by the choice of the debonding medium. Increase of L requires a medium with a $\gamma_{m,s}$ lower than that of air. For hydrophilic silicon wafers, such a lower $\gamma_{m,s}$ can be realized in water. For the specific cases of debonding in air or water we obtain the relationships

$$\gamma_{eff}^{air} = \gamma_{air,s} - \gamma_{s,s} \tag{4.21}$$

$$\gamma_{eff}^{w} = \gamma_{w,s} - \gamma_{s,s} \tag{4.22}$$

To estimate the critical equilibrium crack length in water, we make use of the measurable contact angle θ_{ws} between water and silicon which relates $\gamma_{air,s}$ and $\gamma_{m,s}$ to the known surface energy γ_w of water via the well-known Young equation (76) (see Fig. 4.31):

$$\gamma_{air,s}(p_w^{sat}) - \gamma_{w,s} = \gamma_w \cos\theta_{ws} \tag{4.23}$$

In Eq. (4.23) $\gamma_{air,s}(p_w^{sat})$ refers to $\gamma_{air,s}$ in the presence of saturated water vapor pressure. Since hydrophilic silicon wafers are covered with molecular water layers, we assume that we can approximately equate $\gamma_{air,s}$ in Eq. (4.21)

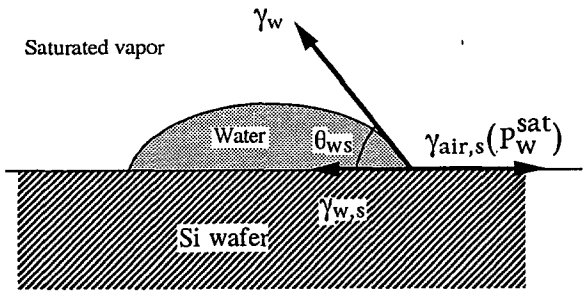

Fig. 4.31 Energy equilibrium at Si–water–air interface.

which corresponds to some unknown effective water vapor pressure, p_w^{eff}, and $\gamma_{air,s}(p_w^{sat})$ in Eq. (4.23); using Eq. (4.22) for γ_{ws} we arrive at

$$\gamma_{eff}^{air} - \gamma_{eff}^{w} = \gamma_w \cos\theta_{ws} \tag{4.24}$$

Since the specific surface energy of water at 20°C is given by about 73 mJ/m^2 (77), and θ_{ws} for hydrophilic silicon wafers ranges from about 5° to 45° (13), we can expect a decrease of γ_{eff} of about 50–70 mJ/m^2 compared to debonding in air and a corresponding increase in the equilibrium crack length L related to

$$\gamma_{eff}^{w} = \gamma_{eff}^{air} - \gamma_w \cos\theta_{ws} = \frac{3Et_w^3 t_b^2}{32L^4} \tag{4.25}$$

in the two-wafer bent case. In the one-wafer bent case the factor of 32 in Eq. (4.25) has to be replaced by a factor of 16.

Equation (4.25) clearly shows that reduction of γ_{eff} by debonding in water should lead to an increase in the equilibrium crack length which is desirable for debonding. Water appears to be the most suitable liquid for this purpose since it has the largest surface energy among commonly used liquids (77). Moreover, high-purity deionized water is extensively used in the semiconductor industry. Therefore, a water-enhanced debonding technique is fully compatible with mainstream VLSI technology.

Typical results for the effective surface energy of a RT bonded wafer as a function of time in water are shown in Fig. 4.32. It is clear that the effective surface energy is drastically reduced within 1 min in water to reach about 90% of the final reduction, which is reached after about 5–10 min in water.

In the case of annealing of the bonded wafers, the molecular water layers on the surface of hydrophilic wafers will react and stronger bonds may be formed. This not only means that $\gamma_{s,s}$ decreases, but also that the debonding surface is no longer fully covered with water molecules. During the opening process, $\gamma_{air,s}$ in Eq. (4.21) now corresponds to a lower effective water vapor

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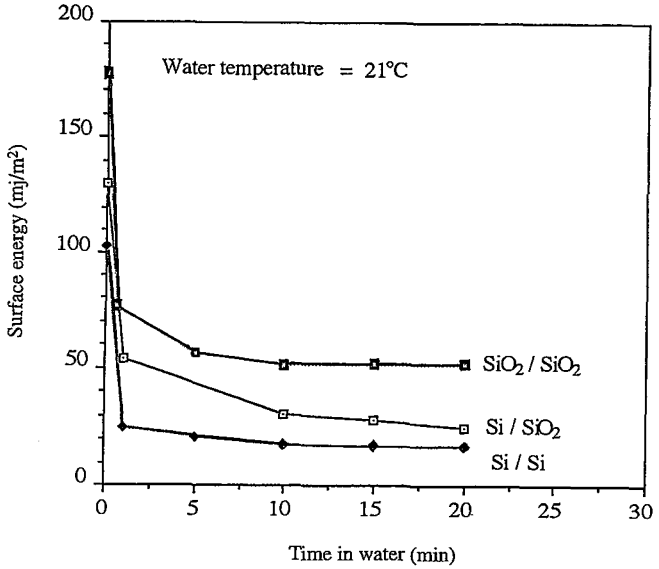

Fig. 4.32 Surface energy of room-temperature bonded Si/Si, Si/SiO_2, and SiO_2/SiO_2 wafers versus time in water.

pressure p_w^{eff} and therefore a higher-energy surface state which can be reduced by a larger amount in contact with H_2O. Instead of Eq. (4.24), we get

$$\gamma_{eff}^{air} - \gamma_{eff}^{w} = \gamma_{air,s}(p_w^{eff}) - \gamma_{air,s}(p_w^{sat}) + \gamma_w \cos\theta_{ws} \qquad (4.26)$$

In Eq. (4.26) we may express the first terms on the right side as

$$\gamma_{air,s}(p_w^{eff}) - \gamma_{air,s}(p_w^{sat}) = RT\int_{p_w^{eff}}^{p_w^{sat}} \Gamma(p)\, d(\ln p) \qquad (4.27)$$

where R is the gas constant, $\Gamma(p)$ is the number of adsorbed H_2O molecules per unit area. In the limiting case of a high-temperature treatment (e.g., at 900°C), there are no longer any H_2O molecules at the bonding interface after annealing. In this case, Eq. (4.27) for $p_w^{eff} = 0$ corresponds to the "spreading pressure," which is known to be around 244 mJ/m^2 for fused quartz (corresponding to thermally grown SiO_2) at 25°C (76). We therefore expect, for bonded and annealed wafers, a large decrease in γ_{eff} when debonding in water compared to debonding in air. As can be seen in Fig. 4.33, by performing the debonding of bonded wafers in water, the effective surface energies of Si/Si bonded wafers which were stored for 110 h in air at 40, 80, and 110°C, respectively, can be reduced drastically.

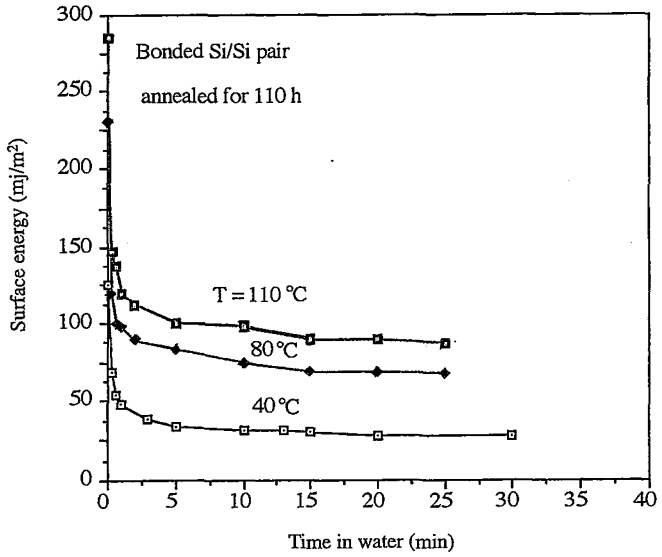

Fig. 4.33 Surface energy versus time in water of bonded Si/Si pairs after 110 h annealing at 40, 80, and 110°C.

It should be noted that annealing of bonded wafers is also associated with a strong decrease of $\gamma_{s,s}$, that is, it leads to a much higher $(\gamma_{eff}^{air})_{anneal}$; therefore $(\gamma_{eff}^{w})_{anneal} > (\gamma_{eff}^{air})_{25°C}$ is possible, resulting in an overall decrease of the equilibrium crack length L with increasing annealing temperature even though the debonding is performed in water.

An increase of the water temperature during the debonding process should lead to lower γ_{eff}^{w} owing to the increased surface energy γ_w of water (78). Figure 4.34 shows that an increase in the water temperature from 23 to 50°C results not only in a lower measured effective surface energy but also in a slightly faster propagation rate of the crack length, as predicted by the model.

The observed reduction of γ_{eff} in water as compared to debonding in air is about 70–90 mJ/m^2 for Si/Si and about 120 mJ/m^2 for SiO_2/SiO_2 interfaces after RT bonding without any additional annealing. These results indicate that the case of Si/Si is close to the expected ideal case of the approximate Eq. (4.23), which neglects the spreading pressure contributions and predicts values of 50–70 mJ/m^2. For the SiO_2/SiO_2 debonding case, a sizable contribution of the spreading pressure is noticeable, as expressed in Eq. (4.26). As expected from the decreasing H_2O coverage of the debonded surface with increasing annealing temperature, the contribution of the spreading pressure becomes increasingly important, for example, after a

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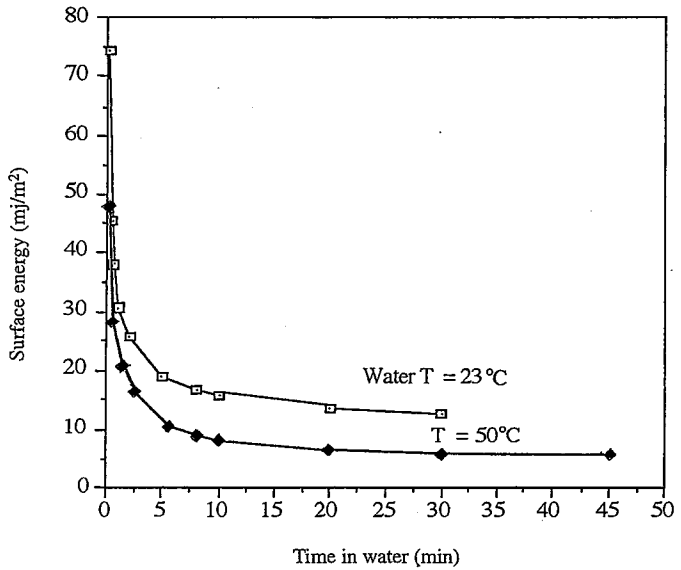

Fig. 4.34 Water temperature effect on surface energy versus time in water.

110-h annealing at 110°C, the water-related decrease of γ_{eff} is about 175 mJ/m^2. In the case of a higher-temperature annealing, the decrease of γ_{eff} in water is increasing and approaching a limit. For example, after 240-h annealing at 150°C, the decrease of γ_{eff} in water is about 300 mJ/m^2 and 370 mJ/m^2 for Si/Si and SiO_2/SiO_2, respectively. These reduction values are in the range of expected values based on Eqs. (4.26) and (4.27) and the spreading pressure of quartz.

Instead of a razor blade, three-point separators at an angle of 120° from each other can be used for actual separation. To separate a bonded wafer pair completely, the critical equilibrium crack length L should be equal to or larger than the radius r of the wafer. In this case, the three cracks created by the three separators will meet and the entire wafers will be debonded. Based on Eq. (4.25), modified for the one-wafer bent arrangement, the critical thickness of the separator t_s required for complete debonding can be calculated as a function of wafer radius r, wafer thickness t_w, and the effective surface energy γ_{eff}.

$$t_s = \sqrt{\frac{16\gamma_{eff} r^4}{3Et_w^3}} \tag{4.28}$$

TABLE 4.9 Calculated Values of the Critical Thickness of a Separator Required for Debonding

Wafer Diameter (mm) $2r$	Wafer Thickness(μm) t_w	Critical Thickness t_s (mm)	
		γ_{eff} = 100 mJ/m^2	γ_{eff} = 20 mJ/m^2
(4 in.) 100 ± 0.5	525 ± 15	0.37	0.17
(5 in.) 125 ± 1.0	625 ± 25	0.46	0.21
(6 in.) 150 ± 0.5	675 ± 15	0.58	0.26
(8 in.) 200 ± 0.2	725 ± 15	0.92	0.41

Table 4.9 provides calculated values of the critical separator thickness t_s for debonding for standard 4- to 8-in. diameter Si/Si bonded wafers using the worst case effective surface energy (100 mJ/m^2) and a typical effective surface energy (20 mJ/m^2) when the crack is in contact with water. The data listed in Table 4.9 suggest that up to 8-in. diameter Si/Si bonded wafers can be separated by three separators with a thickness of the separator which is not expected to introduce any damage to the separated wafers.

If the bonding wafers are dissimilar materials 1 and 2, Eq. (4.28) can be modified as

$$t_s = \sqrt{\frac{8\gamma_{eff} r^4 \left(E_1 t_{w1}^3 + E_2 t_{w2}^3\right)}{3E_1 t_{w1}^3 E_2 t_{w2}^3}} \tag{4.29}$$

where γ_{eff} is the measured surface energy of the bonding pair in water.

After RCA cleaning of Si wafers and RCA1 treatment of sapphire wafers, Si wafers can bond with sapphire wafers spontaneously at RT. The Young's modulus of $(1\bar{1}02)$ crystal sapphire is 5.3×10^{12} dyn/cm^2 which is more than 3 times that of Si (100). Experimentally, it has been found that the bonding strength of RT bonded Si/sapphire pairs was so strong that it was difficult to separate the pair without breaking the Si wafer (79). The typical surface energy of RT bonded Si/sapphire pairs is about 500 mJ/m^2. However, when debonding is performed in water, the Si/sapphire pair can be separated spontaneously within a few minutes.

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5

Thermal Treatment of Bonded Wafer Pairs

To enhance the bonding or surface energy, following room-temperature bonding, wafer pairs are usually thermally treated. However, interface gas bubbles are frequently generated during annealing. This chapter discusses physical and chemical processes occurring during annealing at the bonding interface. Knowledge of the increase in bonding energy as a function of temperature and time allowed the development of a low-temperature bonding technology which is essential for bonding of wafers that contain temperature-sensitive structures or of wafers of dissimilar materials. An understanding of the origin of temperature-dependent gas bubbles at the bonding interface allowed the development of procedures to prevent their formation. Finally, structural changes of thin interface oxide layers in bonded hydrophilic Si/Si pairs during high-temperature annealing as a function of wafer misorientation, oxygen content, and annealing temperature and time are described.

5.1 BONDING ENERGY AS A FUNCTION OF TIME

A measure of the bonding energy of a bonded pair is the specific surface energy when the bonded wafers are partially separated, for example, by inserting a razor blade into the bonding interface. It has been found that the surface energy of bonded Si wafer pairs increases with time at a given temperature and gradually approaches a stable (saturated) value (1–3): for bonded hydrophilic Si wafers, such an increase has been observed already at room-temperature (1) and for bonded hydrophobic Si wafers a noticeable increase starts at above ~150°C (1). Fig. 5.1 shows representative experimental results on the surface energy of hydrophilic and hydrophobic Si/Si pairs as a function of storage time at room-temperature. The saturated surface energy can be 2–4 times of the surface energy measured immediately after room-temperature mating.

At higher temperatures, the surface energies of hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs also increase with time, but approach saturated values

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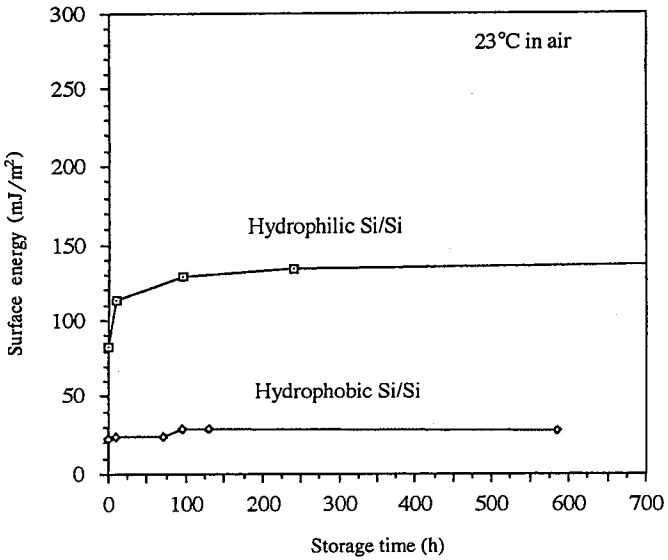

Fig. 5.1 Representative experimental results of surface energy of hydrophilic and hydrophobic Si/Si pairs as a function of storage time at room-temperature.

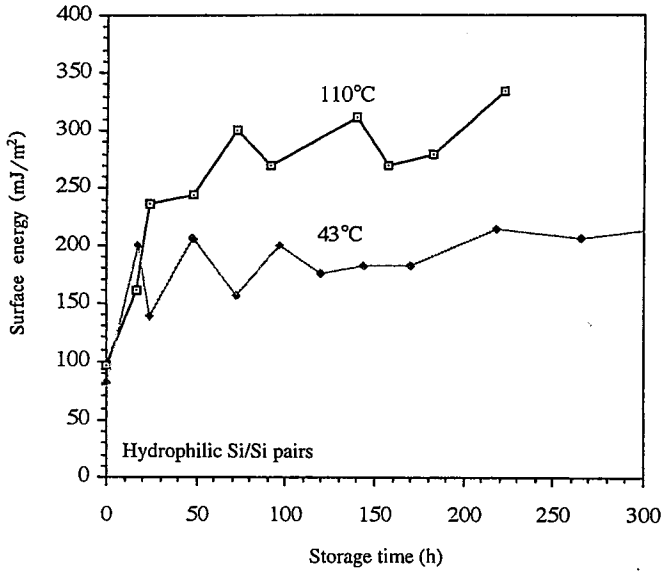

Fig. 5.2 Representative experimental results of surface energy of hydrophilic Si/Si pairs as a function of annealing time at 43 and 110°C.

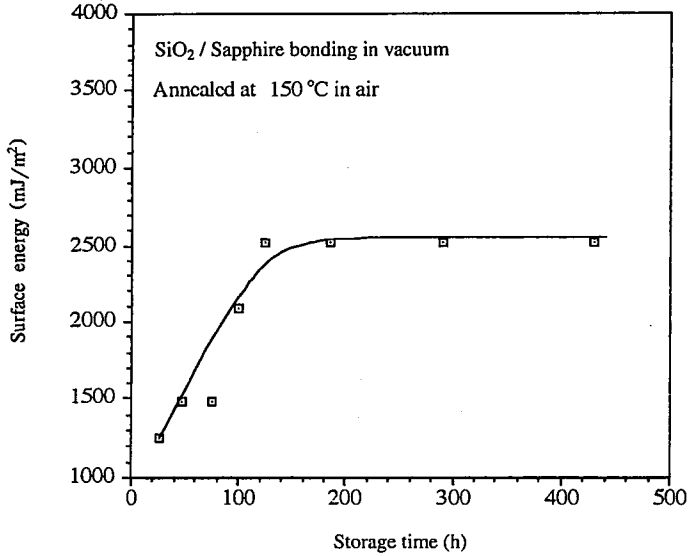

Fig. 5.3 Representative experimental results of surface energy of hydrophilic SiO_2/sapphire pairs as a function of annealing time at 150°C.

more quickly. Fig. 5.2 shows typical experimental observations of the increase of surface energy of hydrophilic Si/Si pairs as a function of storage time at 43 and 110°C. Depending on starting surface conditions, the absolute values may differ for wafers from different vendors. Similar behaviors of bonded hydrophilic Si/quartz, Si/glass, quartz/quartz, or Si/sapphire pairs were also observed. Fig. 5.3 shows the surface energy as a function of time at 150°C for an oxidized Si/sapphire pair.

In contrast, for hydrophobic Si/Si pairs, no significant change of surface energy with time is observed during storage from room-temperature to 150°C, as can be seen from Fig. 5.1 for the room-temperature case. At temperatures higher than 150°C, the increase of surface energy of bonded hydrophobic Si/Si pairs with time becomes noticeable. Fig. 5.4 shows typical experimental results of the changes of surface energy of hydrophobic Si/Si pairs with time at 180 and 300°C.

As described in Chapter 4 and discussed later in this chapter, the physical and chemical reactions occurring at the bonding interface are responsible for changes in the surface energy and some other interface properties with time and with temperature.

For hydrophilic Si/Si pairs, the main reactions include: (1) the slow fracture effect of Si—O—Si bonds via attack by interface water on each surface of the mating wafers, (2) the rearrangement of the interface molecular water to form more stable hydrogen-bonded structures, (3) removal of the

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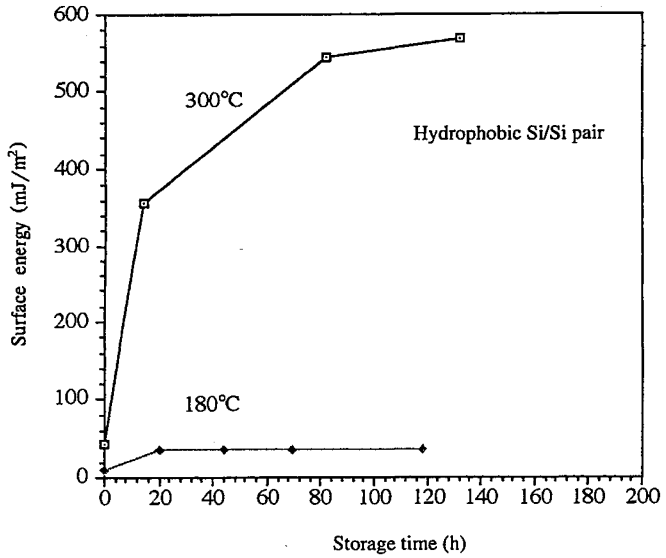

Fig. 5.4 Representative experimental results of surface energy of hydrophobic Si/Si pairs as a function of annealing time at 180 and 300°C.

excess interface molecular water by migration or diffusion, and (4) polymerization of the hydrogen-bonded silanol groups between two wafers. These reactions are expected to be both time and temperature dependent.

For hydrophobic Si/Si pairs, the reactions may be associated with (1) formation of additional hydrogen bonds by reaction of the interface molecular HF with the bonding surfaces, (2) HF and hydrogen release and subsequent covalent Si—Si bond formation across the wafers. Similarly, the reactions are functions of time and temperature, as discussed in more detail below.

Based on the results above, one should be aware that at a given temperature a stable state of the bonding interface is not achieved after a short time annealing, either for hydrophilic or hydrophobic Si/Si pairs. The *stable* (or *saturated*) *values* of the interface properties of bonded wafer pairs, such as surface energy, should be used in any quantitative comparisons. We use the saturated values of surface energy in the following discussion unless specifically indicated otherwise.

5.2 BONDING ENERGY AS A FUNCTION OF TEMPERATURE

5.2.1 Bonding Energy of Hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 Pairs

The experimental observation of surface energy of hydrophilic Si/Si pairs as a function of temperature is shown in Fig. 5.5. Similar results are obtained

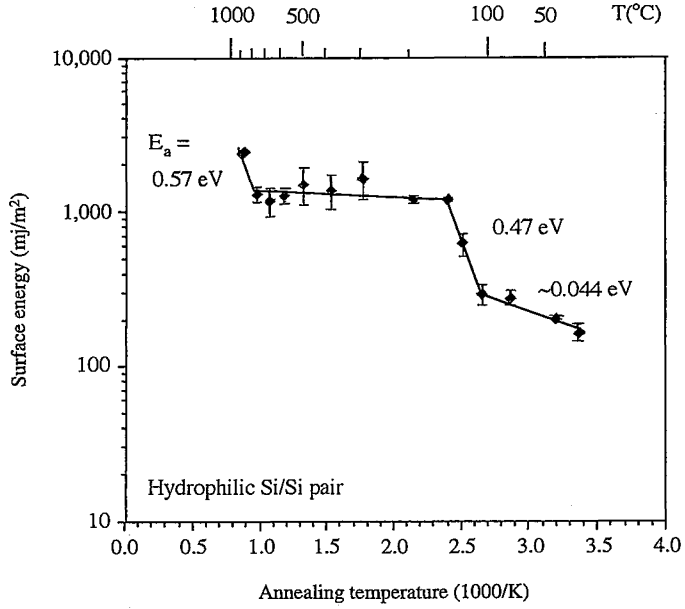

Fig. 5.5 Representative experimental results of (saturated) surface energy of hydrophilic Si/Si pairs as a function of annealing temperature.

for hydrophilic Si/SiO_2 and SiO_2/SiO_2 pairs (see Fig. 5.6 and Fig. 5.7). Figures 5.5–5.7 indicate that the bonding process may consist of four stages (4):

1. From room temperature to 110°C: Slow fracture effect and interface water rearrangement. As described in Chapter 4, during room-temperature bonding, the two wafers bond to each other via hydrogen bonding between adsorbed water molecules on the two surfaces. The linkage of two or three water molecules can form a bridge across the two bonding surfaces. The surface coverage of molecular water on the silica surface depends on relative humidity (rh) but even at 1.2% rh there is still 0.24 monolayer coverage (5). The bonding energy of room-temperature bonded vitreous silica surfaces was found to decrease when bonding was performed at rh < 15% owing to a reduction in water coverage (6). Even at 110°C, water remains on the surface after thermal treatment in air if the air is humid (7). All or most of the molecular water can only be removed from silica surfaces upon heating above 120°C in air (7, 8). If the relative humidity in the environment is 15% or greater, the molecular water at the interface of hydrophilic Si/Si pairs does not change significantly during annealing in the temperature range from room temperature to 110°C.

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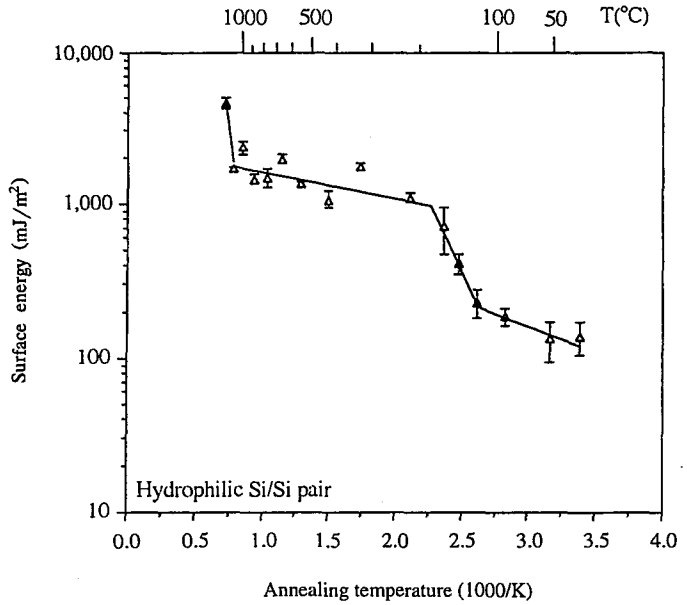

Fig. 5.6 Representative experimental results of (saturated) surface energy of hydrophilic Si/SiO_2 pairs as a function of annealing temperature.

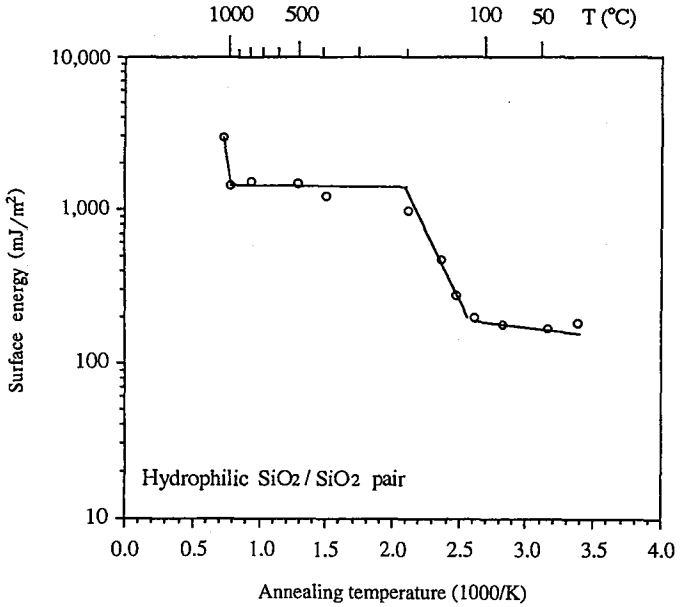

Fig. 5.7 Representative experimental results of (saturated) surface energy of hydrophilic SiO_2/SiO_2 pairs as a function of annealing temperature.

Since a mobile water film structure exists at this stage (5), the main interface reactions in this temperature range should be:

a. The slow fracture effect of Si—O—Si bonds on both bonding surfaces via attack by the interface water (8), that is,

$$\text{Si—O—Si} + \text{HOH} \longrightarrow \text{Si—OH} + \text{HO—Si} \qquad (5.1)$$

which leads to an increased number of OH groups extending from the surfaces into the interface region.

b. Rearrangement of the interface molecular water to form more stable hydrogen-bonded structures. The reactions are both time and temperature dependent. An increased silanol density at the bonding interface results in an enhanced bonding energy. Because the chemical reactivity of the strained native oxide on Si is higher than that of the less-strained thermal oxide, the surface energy immediately after bonding is higher for hydrophilic Si/Si pairs than hydrophilic Si/SiO_2 and SiO_2/SiO_2 pairs. However, since the saturated silanol density for silica is $4.6/nm^2$ (i.e., $4.6 \times 10^{14}/cm^2$) (9), all three bonding structures should show almost identical saturated surface energy if their surface smoothness, and therefore the area which is in real contact, at their interfaces is similar.

The saturated surface energy, γ, of a room-temperature bonded hydrophilic Si/Si pair is estimated in Section 4.7.1 as $\gamma = 179$ mJ/m^2. The calculated value of 179 mJ/m^2 is somewhat less than the measured saturated value ($\sim$ 240 mJ/m^2) of the surface energy of the bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs. It has been suggested that some water molecules may have diffused away from the interface into the surrounding atmosphere or into the SiO_2 network and some strong Si—O—Si bonds may be formed, especially at the wafer edges.

As temperature increases, the water molecules gain increased surface mobility and form energetically more favorable structures. Such a rearrangement may result in an increase in the energy of each hydrogen bond by a few kilocalories per mole, for example, 1 kcal/mol ($\sim$ 0.043 eV) for a water trimer with a chain structure compared to that in a dimer (10). The observed activation energy ($\sim$ 0.044 eV) of the surface energy in this temperature range, as shown in Fig. 5.5, is within this range.

We can model the reactions during the bonding process by equations similar to that used in reference 11. The dominant cause of the increase of surface energy with temperature from room-temperature to around 110°C is the rearrangement of the interface molecular water to form more stable hydrogen bonding structures:

$$[\text{Less stable H-bond}] \xrightarrow{K_1} [\text{More stable H-bond}] \qquad (5.2)$$

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We can write the change in concentration of both H-bonds as

$$\frac{d[\text{More stable H-bond}]}{dt} = K_1(n_{oi}\text{-}[\text{More stable H-bond}]) \quad (5.3)$$

where t denotes time, n_{oi} is the total number of silanol groups, and

$$K_1 = \frac{1}{\tau}\exp(-E_a/kT) \quad (5.4)$$

where k is the Boltzmann constant, T is the absolute temperature, τ is a phenomenological parameter, and E_a is an activation energy which can be determined by experiment. Equation (5.3) has the simple solution

$$[\text{More stable H-bond}] = n_{oi}[1 - \exp(K_1 t)] \quad (5.5)$$

Employing the experimental data, we obtain the saturated surface energy of hydrophilic Si/Si pairs in this temperature range:

$$\gamma = 1010\exp(-0.044/kT)\ \text{mJ/m}^2 \quad (5.6)$$

Assuming that the gain in surface energy with time at each temperature is proportional to the number of more stable hydrogen bonds, we obtain an expression for the surface energy of Si/Si pairs from room-temperature to 110°C:

$$\gamma = [1010\exp(-0.044/kT) - \gamma_0][(1 - \exp(-K_1 t)) + \gamma_0]\ \text{mJ/m}^2 \quad (5.7)$$

where γ_0 is the original surface energy at the beginning of annealing at each temperature.

2. From 110 to 150°C: Polymerization of silanol groups across the interface. It is known that polymerization of silanol groups can take place at temperatures as low as room temperature provided that these groups are in close proximity and are hydrogen-bonded (7):

$$\text{Si—OH} + \text{HO—Si} \underset{K_r}{\overset{K_f}{\rightleftharpoons}} \text{Si—O—Si} + \text{HOH} \quad (5.8)$$

Reaction (5.8) implies that the hydrogen bonding between silanol bonds on opposite surfaces should be transformed into strong siloxane bonds, provided that the interface molecular water can be removed. The reaction is reversible at $T < 425$°C if water is present. For the siloxane bridges to form across the bonding surfaces, excess water has to be removed. Since the molecular water can desorb from the wafer surfaces at above 110°C, independent of air humidity, the interface is drying gradually during annealing at

> 110°C. Presumably, some of the molecular water diffuses along the bonding interface to the outside, but some water molecules will also diffuse through the surrounding native oxide and react with Si to form SiO_2 and hydrogen. The oxide thus formed contributes to close the interface microgaps.

Reaction (5.8) may be described by a temperature-dependent equilibrium constant $K_2(T)$ given by

$$K_2(T) = \frac{K_f}{K_r} = \frac{[\text{Si—O—Si}][H_2O]_s}{[\text{Si—OH}]^2} \quad (5.9)$$

where $[H_2O]_s$ and [Si—OH] are concentrations of molecular water and silanol bonds on bonding surfaces and [Si—O—Si] is the concentration of siloxane bonds across the two wafers. Since most physisorbed water has been removed, the molecular water at the interface is generated by the polymerization reaction at $T > 110$°C.

The concentration of molecular water adsorbed on a surface, $[H_2O]_s$, is a function of concentration of molecular water in the gas phase, $[H_2O]_g$, in contact with the surface. Under conditions of thermal equilibrium, the concentrations of molecular water on a surface and in the surrounding area can be described by a Boltzmann distribution:

$$\frac{[H_2O]_s}{[H_2O]_g} = A\exp(E_a/kT) \quad (5.10)$$

where A is a constant, E_a is an activation energy, and k is the Boltzmann constant.

After a sufficiently long annealing at a given temperature, an equilibrium of $[H_2O]_g$ between the interface of a bonded pair and the outside atmosphere can be established. Since $[H_2O]_g$ outside the bonded pairs can be considered to be almost constant, $[H_2O]_s$ decreases exponentially with temperature. It is known (12) that the equilibrium constant for the reaction between silicate glass and water is constant up to 300°C and increases at temperatures higher than 400°C. We may anticipate that the same is true for reaction (5.8). Therefore, according to Eq. (5.9), the concentration of the interface siloxane bonds [Si—O—Si] should increase exponentially with temperature over the temperature range from 110 to 150°C as long as the Si—OH density has not yet changed considerably.

Figure 5.5 shows that there is a turning point around 110°C beyond which the surface energy increases with temperature much more rapidly than at lower temperatures and the activation energy over the temperature range from 110 to 150°C is ~ 0.47 eV. The activation energy of polymerization of silanol groups was 9–24 kcal/mol (i.e., 0.4–1.04 eV), based on the pH values of the surrounding solution (13). The experimental data on the activation

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energy of 0.47 eV is consistent with that on the polymerization of silanol groups. It implies that once the molecular water is removed from the bonding interface, polymerization of the hydrogen-bonded silanol groups to form strong siloxane bonds occurs. The integrated IR absorbance of HOH and —OH stretching modes obtained from IR spectra of the bonding interface of hydrophilic Si/Si pairs as a function of annealing temperature has indicated that 80% of the molecular water and up to 50% of the interfacial —OH groups have been removed after 70 hours of annealing at 150°C (7). The formation of strong siloxane bonds at the interface results in a rapid increase in surface energy of the bonded pair:

$$\gamma \propto [\text{Si—O—Si}] = \frac{K_2(T)\,[\text{Si—OH}]^2}{[\text{H}_2\text{O}]_s} \tag{5.11}$$

where γ is known from experimental results to be

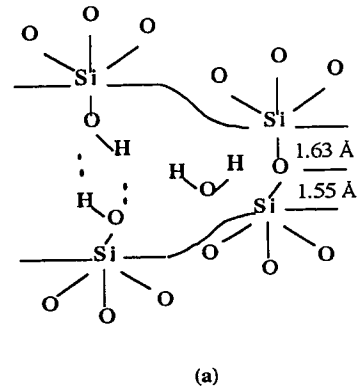
$$\gamma = 4.71 \times 10^8 \exp(-0.47/kT)\ \text{mJ/m}^2 \tag{5.12}$$

In analogy to reaction (5.8), the surface energy as a function of annealing time and temperature can be expressed as

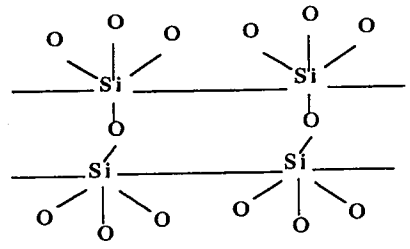
$$\gamma = [4.71 \times 10^8 \exp(-0.47/kT) - \gamma_0][(1 - \exp(-K_2 t)) + \gamma_0]\ \text{mJ/m}^2 \tag{5.13}$$

where γ_0 is the original surface energy at the beginning of annealing at each temperature.

3. From 150 to 800°C: Bonding energy limited by contacted area. For bonded standard Si/Si pairs the saturated surface energy reaches ~1200 mJ/m^2 at 150°C, and an almost constant surface energy is observed from 150 to 800°C (see Fig. 5.5). It was reported (6) that water adsorption on a quartz surface outgassed at temperatures in excess of 150°C is irreversible and the rehydration of the quartz surface is not complete from the vapor phase at low relative vapor pressure. We believe that almost all silanol groups in the real contacted areas have converted to siloxane bonds at ~150°C. Since the bonding surfaces are never perfectly smooth, the area over which bonding really occurs (termed contacted area) is limited. In addition, inert gases such as nitrogen trapped in nanocavities formed by the microroughness of the two bonded surfaces may locally prevent the formation of siloxane bonds. Bonding in low vacuum increases the effective contacted area and will thus allow higher values of the surface energy to be reached at 150°C (14). Figure 5.5 indicates that, from 150 to 800°C, the surface energy of the pairs has reached the value determined by the contacted area at the interface over which all silanol groups at the interface have converted to siloxane bonds. We mention specifically that even though the absolute values of the surface energy in the



(a)



(b)

Fig. 5.8 Proposed chemical structure of hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs during and after annealing at 150–800°C for a sufficiently long time. Only isolated silanol groups are shown: (*a*) during annealing; (*b*) after long annealing.

plateau of Fig. 5.5 may vary depending on both the area in real contact at the bonding interface and the density of the bonding species on the contacted surfaces, it is a rather general behavior of bonded hydrophilic silicon pairs. Figure 5.8 is a proposed chemical structure of hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs during and after annealing at 150–800°C for a sufficiently long time. Only isolated silanol groups are shown during annealing (Fig. 5.8*a*) and after long annealing (Fig. 5.8*b*).

A calculation similar to that in Chapter 4 can be carried out to roughly estimate the surface energy of bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs annealed at 150–800°C for a sufficiently long time. If all the bonding sites on the surfaces are in contact, the surface energy in this temperature range can be estimated by

$$\gamma = \frac{1}{2}(d_{\text{OH}} E_{\text{Si—O}}) \tag{5.14}$$

where d_{OH} is the surface density of silanol groups (4.6×10^{14}/cm^2) and $E_{\text{Si—O}}$ is the energy of a siloxane bond (4.5 eV or 7.2×10^{-16} mJ) (15).

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From Eq. (5.14) we obtain $\gamma = 1658$ mJ/m^2, which is consistent with experimental observation.

4. From 800°C and above: Complete bonding via oxide flow. Compared with Fig. 5.5 for hydrophilic Si/Si pairs, Figs. 5.6 and 5.7 show that higher temperatures (> 1000°C vs. > 800°C) are required for starting an even more rapid increase of the surface energy of hydrophilic Si/SiO_2 and SiO_2/SiO_2 pairs.

It is known that native oxides grown during wet chemical cleaning are a strained hydrous oxide with internal OH groups near the surface (16). It was also reported that the SiO_2 viscosity is greatly reduced when the SiO_2 contains H_2O (17). For hydrophilic Si/Si pairs, the 800°C annealing may be sufficient to increase the contact area at the interface by means of viscous flow of the native oxide to fill up the interface microgaps and to form siloxane bonds. For Si/SiO_2 and SiO_2/SiO_2 pairs consisting of thermal oxide which is less strained and has lower water concentration, annealing at above 1000°C appears to be necessary to introduce SiO_2 mass transport and viscous flow at the bonding interface (18). This explains the ~200°C higher annealing temperature required for Si/SiO_2 and SiO_2/SiO_2 pairs than for Si/Si pairs to complete the bond between two wafers.

The surface energy of completely bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs can be estimated by substituting the bond density d_{Si} of 1.355×10^{15}cm^{-2} on an Si(100) surface for d_{OH} in Eq. (5.14) (19) and $\gamma = 4932$ mJ/m^2 is obtained. However, during the surface energy measurement of completely bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs by inserting a razor blade, fracture is likely to occur at the weakest point of the system, that is, in the bulk Si:

$$\gamma = \frac{1}{2}(d_{Si} E_{Si-Si}) \tag{5.15}$$

where the energy of the Si–Si bond, E_{Si-Si}, is 1.9 eV (14).

We obtain $\gamma = 2082$ mJ/m^2 for the completely bonded hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs, which is consistent with the measured values of γ around 2000 mJ/m^2 for all three bonding structures after high-temperature annealing. It should be noted that during surface energy measurement, when the blade is inserted, the first crack may form in the middle of the bonded oxide layer. Owing to the concentration of stress at the crack tip and the attack of water vapor from air at the tip, the fracture can take place inside the oxide layer, involving much smaller energy than the oxide fracture energy.

According to the measured values of the surface energy and the activation energy (0.57 eV, see Fig. 5.5), expressions similar to Eqs. (5.6) or (5.12) can be formulated for the saturated surface energy (in mJ/m^2) in this temperature range:

$$\gamma = 7.02 \times 10^5 \exp(-0.57/kT) \text{ mJ/m}^2 \tag{5.16}$$

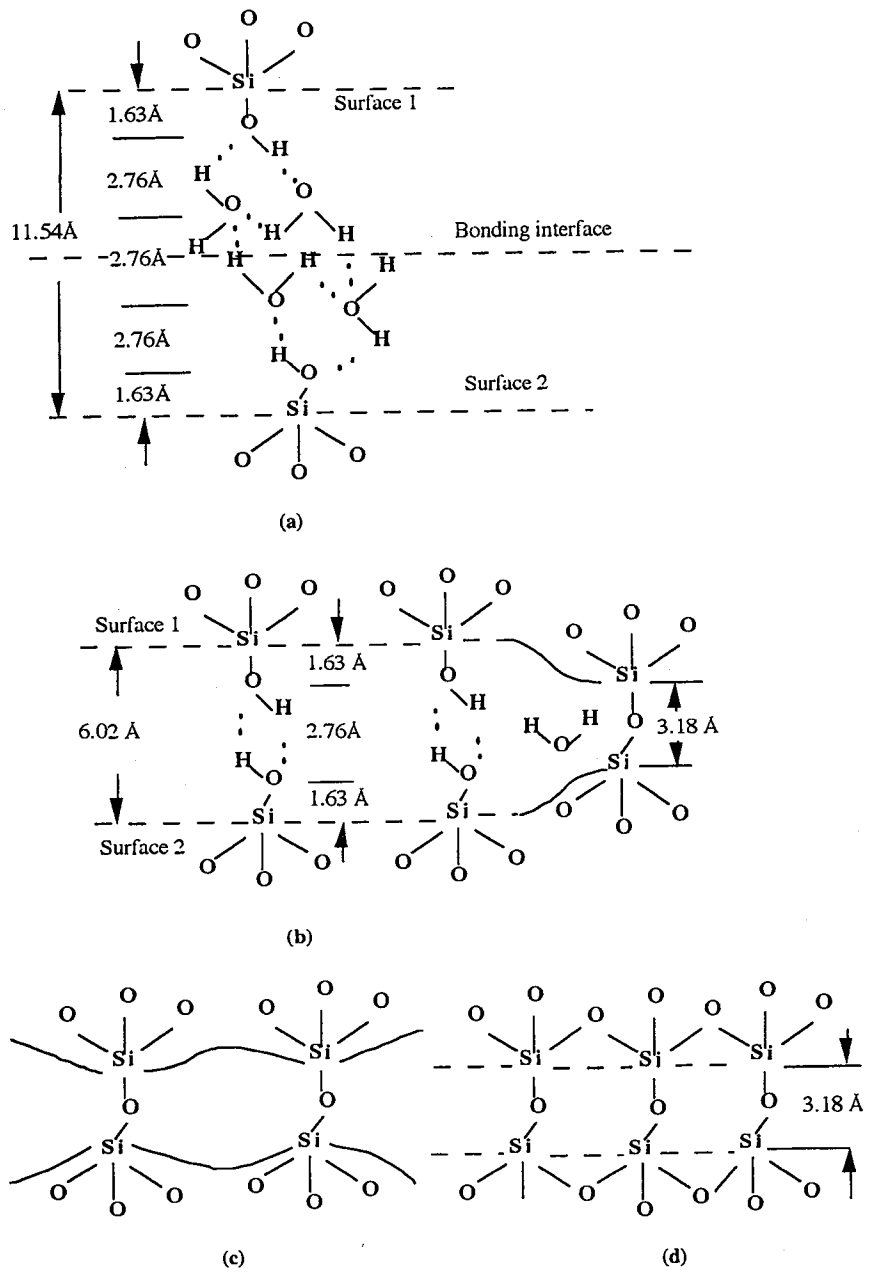

Fig. 5.9 Proposed bonding model for hydrophilic Si wafer bonding at different temperatures. (*a*) Room temperature–110°C: formation of stable hydrogen bonding between molecular water across the bonding interface. (*b*) 110–150°C: removal of interface molecular water and formation of siloxane bonds. (*c*) 150–800°C: stable siloxane bonds. (*d*) > 800°C: viscous flow of interface oxide (> 800°C for Si/Si, > 1000°C for Si/SiO_2 and SiO_2/SiO_2 pairs).

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The time and temperature dependence of the surface energy is then given as

$$\gamma = [7.02 \times 10^5 \exp(-0.57/kT) - \gamma_0][(1 - \exp(-K_3 t)) + \gamma_0] \text{ mJ/m}^2 \quad (5.17)$$

where γ_0 is the original surface energy at the beginning of annealing at each temperature. Equations (5.7), (5.13), and (5.17) can also be applied to hydrophilic Si/SiO_2 and SiO_2/SiO_2 pairs.

Based on this model of bonding, it is clear that a strong bond of hydrophilic Si/Si, Si/SiO_2, and SiO_2/SiO_2 pairs can be realized at temperatures as low as 150°C (SiO_2/SiO_2 pairs may need somewhat higher temperatures) after a sufficiently long annealing time. The four phases of the hydrophilic Si wafer bonding process at different temperatures are schematically illustrated in Fig. 5.9. A comparison of calculated and experimental data of saturated surface energies of hydrophilic Si/Si pairs as a function of temperature from room-temperature to 900°C is given in Fig. 5.10. Figure 5.11 illustrates the calculated and the experimental surface energies of hydrophilic Si/Si pairs versus annealing time at 110°C where $\tau = 2.5$ h and E = 0.044 eV are used.

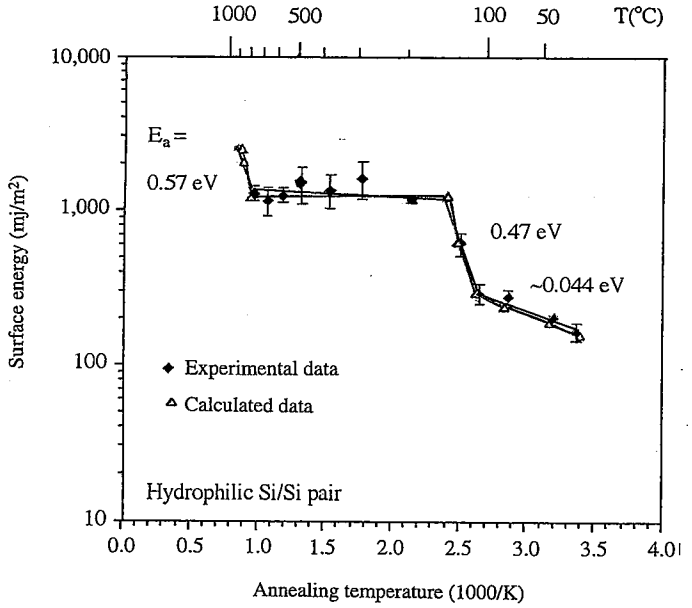

Fig. 5.10 Comparison of calculated and experimental results of surface energies of bonded hydrophilic Si/Si pairs as a function of temperature for 100 h annealing from room-temperature to 900°C.

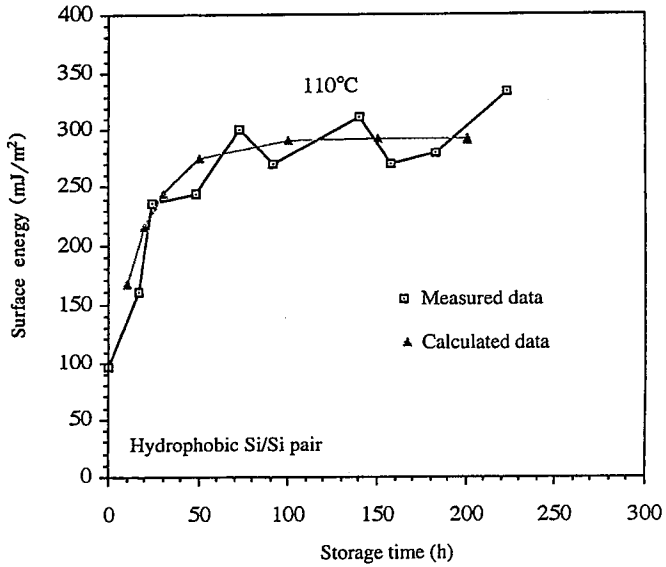

Fig. 5.11 Comparison of calculated and experimental results of surface energies of bonded hydrophilic Si/Si pairs versus annealing time at 110°C.

5.2.2 Bonding Energy of Hydrophobic Si/Si Pairs

The bonding mechanism of hydrophobic Si/Si pairs is not as well understood as that of hydrophilic ones and further detailed investigations are required (4, 20–24). From the discussions in Chapter 4 it is known that hydrophobic Si wafers prepared by a dip in diluted HF with or without subsequent DI water rinse can bond to each other spontaneously (24). Since bonding of DI water rinsed wafers is realized the substituting Si—OH bonds for Si—F bonds during water rinse, the bonding mechanism is expected to be similar to that of hydrophilic bonding. Therefore, the discussion in this section is only related to the case of Si—F bonds.

It is proposed that the linkages of three or more hydrogen-bonded HF molecules may bridge the gap between the two wafers, and wafers which are separated by up to 8 Å may be bonded via hydrogen bonding. It has been found that the surface energy (bonding strength) of bonded hydrophobic Si/Si pairs as a function of annealing temperature is very different from that of hydrophilic Si/Si pairs. Figure 5.12*a* shows a comparison of the surface energies of bonded hydrophilic and hydrophobic Si/Si pairs as a function of air annealing temperature (25). Figure 5.12*b* uses the exponential scale for the surface energy of hydrophobic Si/Si pairs and indicates that the bonding

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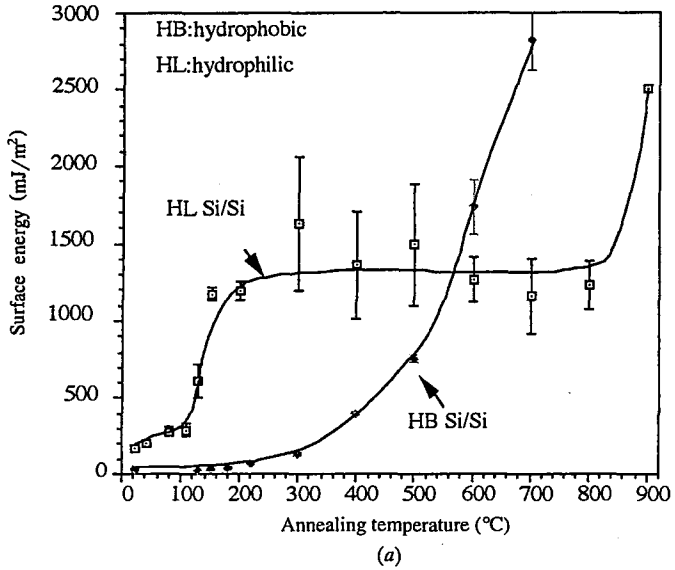
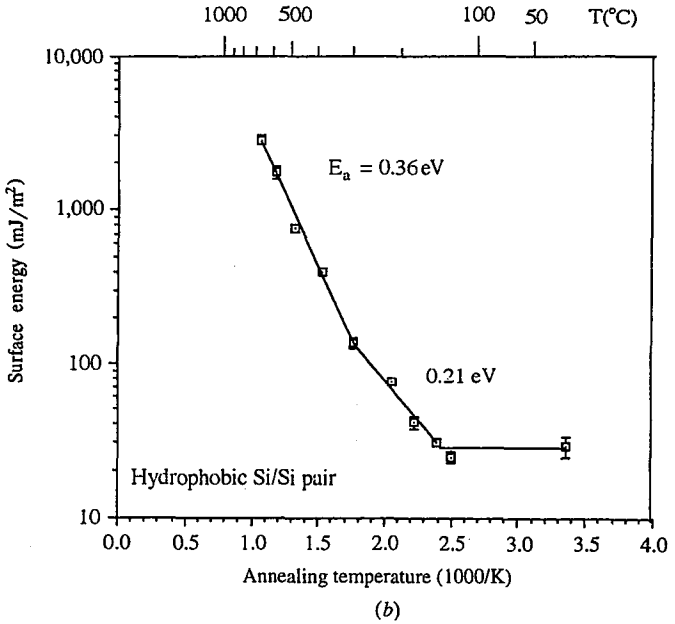


(*a*)



(*b*)

Fig. 5.12 (*a*) Comparison of surface energies of bonded hydrophilic Si/Si pairs and hydrophobic Si/Si pairs as a function of annealing temperature and (*b*) surface energy of hydrophobic Si/Si pairs as a function of annealing temperature.

process can be considered to consist of four stages:

1. From room temperature to 150°C: Stable state. The surface energy appears to be stable during annealing in the range from room-temperature to 150°C, indicating the absence of any relevant interface reactions.

2. From 150 to 300°C: Additional bond formation and HF rearrangement. From 150 to 300°C the surface energy increases with temperature with an activation energy of about 0.21 eV, as shown in Fig. 5.12, while no interface gas bubbles are observed (few bubbles are formed if annealing is done under low vacuum). Since the average energy of each hydrogen bond between HF molecules is 5.02 kcal/mol (26), that is, 0.26 eV, the close match of the two energies suggests that the formation process of additional bonds, or rearrangement of the more stable interface HF structure, may be involved during annealing in this temperature range.

Since some residual HF molecules which are physisorbed on the hydrophobic Si surfaces may be thermally desorbed and become vaporized HF at elevated temperatures, the F coverage could reach 25% of a monolayer on each of the mating surfaces at the bonding interface, as was reported for Si(100) surfaces after exposure to diluted vapor HF (27). Additional bonds could then be formed between the wafers via hydrogen bonding because more Si—F bonds are available.

Similar to the hydrophilic bonding case, rearrangement of molecular HF at the bonding interface to form more energetically favorable structures could also increase the bond energy of each hydrogen bond in the system. An equation identical to Eq. (5.11) can be used to estimate the surface energy of the hydrophobic Si/Si pair if F coverage reaches 25%:

$$\gamma = \frac{1}{2}(2d_{\mathrm{Si-F}}E_{\mathrm{hHF}}) \tag{5.18}$$

where $d_{\mathrm{Si-F}} = 0.25 \times 1.355 \times 10^{15}/\mathrm{cm}^2$.

The calculated value of about 140 $\mathrm{mJ/m^2}$ of the surface energy is consistent with the measured surface energy of 137 $\mathrm{mJ/m^2}$ after the 300°C annealing shown in Fig. 5.12.

3. From 300 to 700°C: Hydrogen desorption and Si–Si covalent bond formation. Fig. 5.12 indicates that, starting from ~300°C, the surface energy of hydrophobic Si/Si pairs increases more rapidly with an activation energy of ~0.36 eV and, at the same time, some interface gas bubbles are generated. Both monohydride (Si—H) and dihydride ($\mathrm{Si—H_2}$) are simultaneously present on the HF-dipped Si(100) surface (28). Hydrogen is less stable in a dihydride structure than in a monohydride structure. Although the desorption of H from the HF-treated Si surface was demonstrated to start at about 367°C from dihydride and 447°C from monohydride in ultrahigh vacuum (29), the occurrence of bubble formation at the interface during

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annealing of bonded hydrophobic Si/Si pairs suggests that H desorption may already start at ~300°C after a sufficiently long time.

Bubbles can be generated at the interface of bonded hydrophobic Si/Si pairs during a 300°C, ~14 h or a 400°C, 0.5 h anneal (25). Most bubbles generated during the 300–400°C anneal disappear after 3–19 days of storage at room-temperature in air. The higher the annealing temperature, the longer is the room-temperature storage period required for bubbles to disappear. Among the possible gases which can be expected in the bubbles, molecular hydrogen is most likely to diffuse along the bonding interface with diffusivity on the order of 10^{-5}–10^{-7} cm^2/s (30). Bubbles that do not disappear during room-temperature storage may contain desorbed HF or hydrocarbons. It is known that the melting point of HF is ~ −80°C and that of methane is −183°C. Experiments have shown that after 8 days of storage at room temperature, the shrunk interface bubbles which were generated by 400°C, 3 h annealing disappeared when the pair was immersed in liquid nitrogen (−196°C).

The Si—F bonds are believed to be stable up to 2000°C (31). It is speculated that some Si—Si bonds can be formed at the bonding interface during annealing at ≥ 300°C when HF and H are released from the two mating surfaces:

$$\text{Si—H} + \text{H—Si} \xrightarrow{K_H} \text{Si—Si} + \text{H}_2 \uparrow \tag{5.19}$$

The released hydrogen molecules may diffuse into the surrounding bulk Si at high temperatures (> 500°C), but mostly will migrate out along the interface. The experimentally determined activation energy E_a of 0.36 eV shown in Fig. 5.12*b* probably represents that of reaction (5.19).

Similar to Eqs. (5.3) and (5.4), the time dependence of reaction (5.19) may be expressed by the change in concentration of Si—Si bonds [Si—Si]:

$$\frac{d[\text{Si—Si}]}{dt} = K_H(n_0 - [\text{Si—Si}]) \tag{5.20}$$

with the reaction constant

$$K_H = \frac{1}{\tau}\exp(-E_a/kT) \tag{5.21}$$

where n_0 is the total number of Si–H bonding sites on each mating surface.

Using the experimental data (γ = 137 mJ/m^2 at 300°C and 2082 mJ/m^2 at 700°C), the saturated surface energy in the range 300–700°C (in mJ/m^2) can roughly be estimated as

$$\gamma = 9.0 \times 10^4 \exp(-0.32/kT)\ mJ/m^2 \tag{5.22}$$

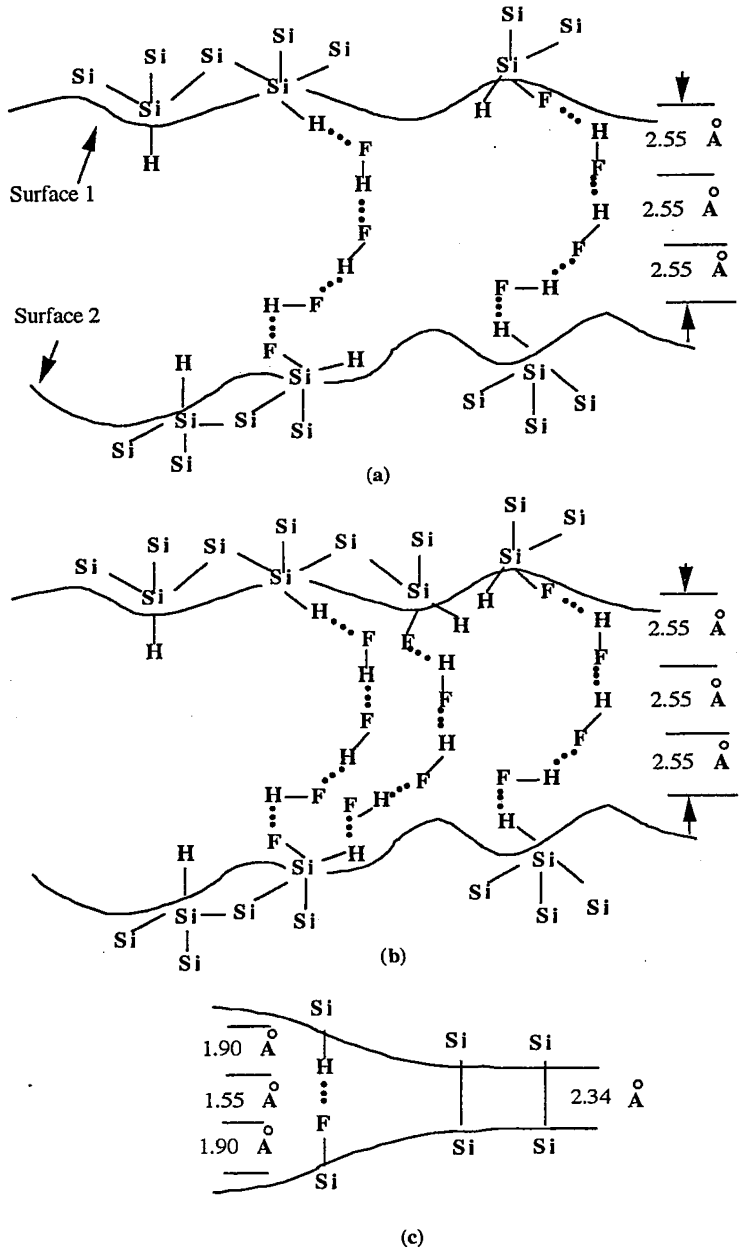

Fig. 5.13 Proposed bonding model for hydrophobic Si wafer bonding at different temperatures. (*a*) Room temperature–150°C: stable hydrogen bonding between molecular HF across the bonding interface. (*b*) 150–300°C: formation of more Si—F bonds on each surface resulting in additional hydrogen bonds between HF molecules across wafers. (*c*) >300°C: removal of HF and H resulting in formation of Si—Si covalent bonds.

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The time dependence of the surface energy is then given by

$$\gamma = [9.0 \times 10^4 \exp(-0.32/kT) - \gamma_0][1 - \exp(-K_H t) + \gamma_0] \text{ mJ/m}^2 \quad (5.23)$$

where γ_0 is the original surface energy at the beginning of annealing at each temperature.

4. From 700°C and above: Complete bonding via surface diffusion of Si atoms on bonding interface. As shown in Fig. 5.12, at around 700°C, the surface energy of hydrophobic Si/Si pairs reaches that of bulk Si. It appears likely that at temperatures as low as 700°C, surface diffusion of Si atoms on the bonding surfaces can occur, which leads to the closing of microgaps at the bonding interface probably catalyzed by hydrogen. Figure 5.13 schematically shows the proposed model of the hydrophobic Si wafer-bonding process.

5.3 LOW-TEMPERATURE WAFER BONDING

Wafer bonding provides a high degree of flexibility in material integration. Although the differences in bonding materials in terms of composition, crystal structure, crystal orientation, wafer thickness, doping type, and profile do not present obstacles for wafer bonding, the thermal mismatch imposes a severe restriction on annealing temperature. Therefore, it is crucial to achieve a strong bond through low-temperature annealing. Low-temperature bonding is also essential for bonding of processed wafers or compound materials, to prevent undesirable changes or decomposition even if the bonding wafers are thermally matched.

For bonding to occur at low temperature, the two mating surfaces must be in sufficient proximity to allow the intermolecular forces to be effective. A significant increase of the bonding area may be achieved by elastic or plastic deformation of the original surface asperities when an external pressure is applied either through electrostatic forces (e.g., in field-assisted metal/glass anodic bonding) (32) or via mechanical forces (e.g., in pressure-assisted metal/metal or metal/ceramic bonding) (33). However, the former depends on the migration of mobile ions (e.g., Na^+) from the glass driven by electrostatic and thermal forces. The latter cannot form a good bond unless high-temperature diffusion occurs. A layer with a low melting or softening temperature, such as a glass, polymer, or metal layer, the eutectic temperature of which with the bonding substrate is low, may be used as an intermediate layer at the bonding interface. However, the reliability, stability, and thermal stress problems associated with the intermediate bonding layer prevent this approach from gaining wide acceptance.

As mentioned in Section 5.2.1, surface energies approaching those obtained after 1100°C annealing may be obtained for hydrophilic Si/Si pairs bonded under low vacuum conditions (~5 Torr) and annealed for long periods (> 60 h) at about 150°C (14). The behavior appears to be associated

with larger contacted area for siloxane bond formation resulting from the lack of trapped nitrogen.

Based on the discussion in Section 5.1, it appears that a strong bond can be formed at low temperatures in the wafer pairs of some materials which are bonded via hydrogen bonding between OH groups owing to the polymerization effect:

$$\text{M—OH} + \text{HO—R} \longrightarrow \text{M—O—R} + \text{HOH} \quad (5.24)$$

where M and R represent the surface atoms of the two bonding materials, respectively. The excess water can be removed by either migrating along the bonding interface or diffusing into the surrounding bonding materials during a long annealing at a low temperature, for example, 150°C for 100 h in the case of hydrophilic Si/Si pairs and hydrophilic Si/Al_2O_3 (sapphire) pairs.

It appears that a strong bond can also be realized at low temperatures for wafer pairs bonded via hydrogen bonding between HN groups, such as the bonding of Si wafers covered with a Si_3N_4 or TiN layer (34):

$$\text{Si—HN} + \text{HN—Si} \longrightarrow \text{Si—(2N)—Si} + \text{H}_2 \quad (5.25)$$

For some metals R with relatively high electronegativity, such as those in group III or higher, and some transitional metals, their oxides show a less ionic character and their hydroxides may also be able to polymerize at low temperatures to form a stronger bond:

$$\text{R—OH} + \text{HO—Si} \longrightarrow \text{R—O—Si} + \text{HOH} \quad (5.26)$$

or

$$\text{R—OH} + \text{HO—R} \longrightarrow \text{R—O—R} + \text{HOH} \quad (5.27)$$

For instance, Fig. 5.3 shows the surface energy of an oxidized Si/sapphire (Al_2O_3) bonded pair as a function of annealing time at 150°C. It is believed that the polymerization effect is responsible for the increase of the bonding strength:

$$\text{Al—OH} + \text{HO—Si} \longrightarrow \text{Al—O—Si} + \text{HOH} \quad (5.28)$$

A similar reaction may also be involved in Si/ZnS bonding:

$$\text{Zn—OH} + \text{HO—Si} \longrightarrow \text{Zn—O—Si} + \text{HOH} \quad (5.29)$$

5.4 TEMPERATURE-DEPENDENT INTERFACE BUBBLES

5.4.1 Causes of Temperature-Dependent Interface Bubbles

In addition to the interface bubbles in room-temperature bonded pairs that are usually caused by particles and surface irregularities, bubbles may appear during annealing at elevated temperatures (35, 36). An example is shown in Fig. 5.14(*a*) and (*b*). The interface bubbles in bonded silicon pairs usually

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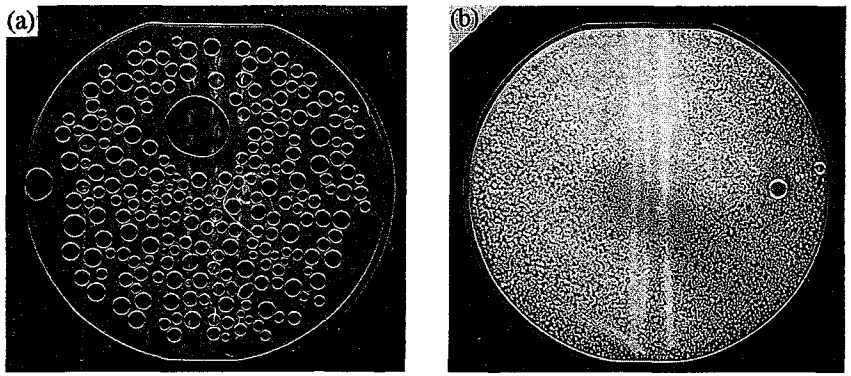

Fig. 5.14 (*a*) X-ray topographic image of large bubbles and (*b*) of tiny bubbles at the interface of bonded hydrophilic Si/Si pairs after annealing at 800°C for 30 min.

disappear after annealing at temperatures over 1000°C. For room-temperature bonded hydrophilic silicon pairs, interface bubbles have been observed even during room-temperature storage for an extended period of time (1). The higher the storage temperature, the shorter is the time required for bubble formation. Figure 5.15 shows the typical storage time required at temperatures from room temperature to 150°C for bubbles to appear at the

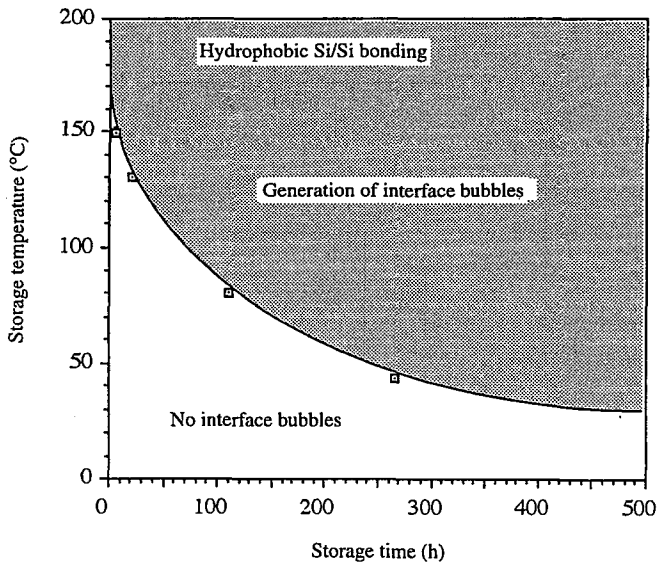

Fig. 5.15 Typical storage time required for bubble generation at the interface of bonded hydrophilic Si/Si wafers as a function of temperature between 40 and 150°C.

hydrophilic Si/Si bonding interface (1). In contrast, no interface bubbles were observed in bonded hydrophobic Si/Si pairs during storage at temperatures up to 220°C for 113 h in air. Bubble generation was demonstrated to start at the interface of bonded hydrophobic Si/Si wafers during a 300°C annealing.

To determine the main content in the bubbles formed after room-temperature bonding, arrays of cavities of the same size but with different areal densities were fabricated on a silicon wafer (30). The cavities were processed in such a way that the bottom of each became a thin membrane. The silicon wafers with cavities were bonded to bare silicon wafers, either hydrophilic or hydrophobic, under high vacuum. The behavior of cavities during annealing can be reasonably considered to simulate that of the temperature-dependent interface bubbles. The test structure and the layout of the cavities on a silicon wafer are shown in Fig. 5.16. The deflection of membranes of the cavities was used to measure sensitively the pressure changes in the cavities. The pressure in the cavities was found to increase after thermal treatments. The pressure increase was measured at room temperature as a function of heating temperature, time, and cavity density. Figure 5.17 shows the results for bonded hydrophobic silicon pairs. The results clearly indicate that the lower-density cavities show a higher increase in pressure corresponding to

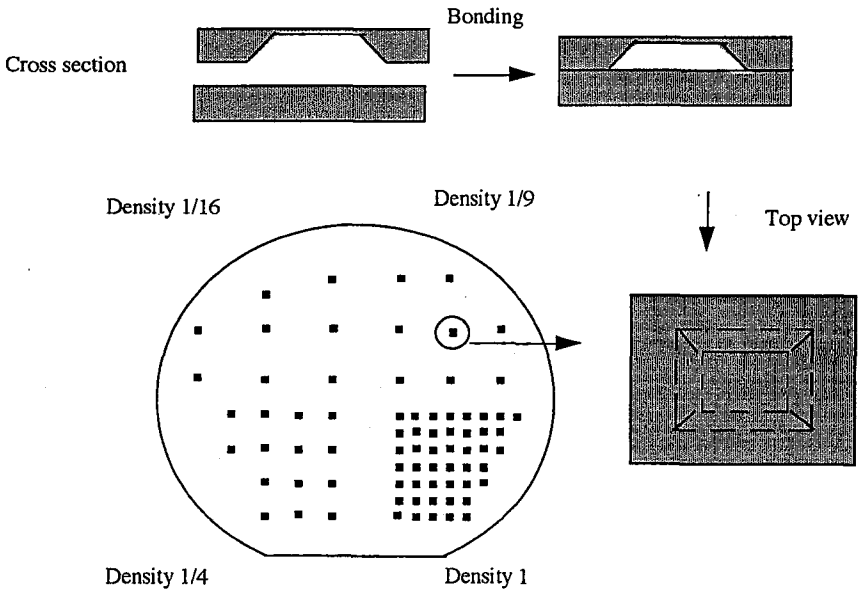

Fig. 5.16 Silicon cavities used for measuring pressure changes due to interface reactions in a bonded pair. Top: Schematic of test structure. Bottom: Cavity arrangement on a silicon wafer.

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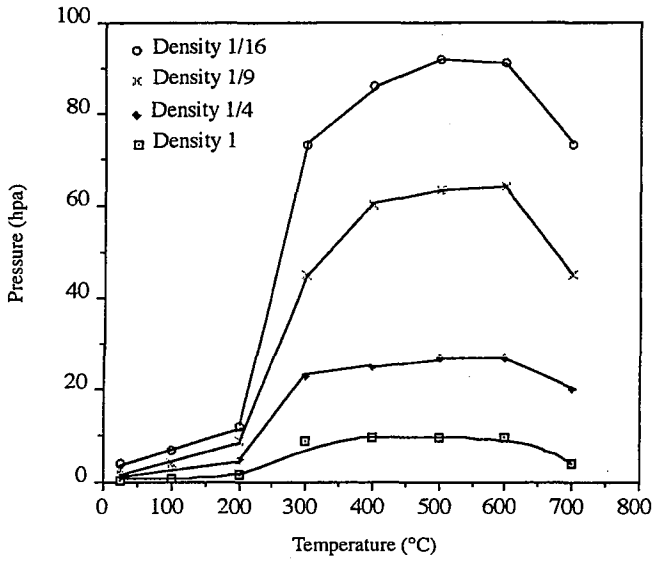

Fig. 5.17 Pressure increase in cavities for bonded hydrophilic silicon wafers as a function of annealing temperature and cavity density. The same annealing time of 70 h is used at all temperatures.

the larger available bonding area around a cavity. A mass spectroscopic analysis showed (37) that in addition to a low percentage of water, hydrocarbons, and nitrogen, the main constituent of the gas in the cavities is hydrogen, in both bonded hydrophilic and hydrophobic silicon pairs, after annealing at temperatures ranging from room temperature to 700°C. The results shown in Fig. 5.17 demonstrate that hydrogen molecules diffuse along the bonding interface until they find a cavity or form an interface bubble around a suitable nucleus, rather then diffusing into the silicon, as long as the temperature is below about 500°C. The hydrogen diffusion along the interface occurs even at room-temperature with a diffusivity on the order of 10^{-5}–10^{-7} cm^2/s (30).

In the case of bonded hydrophilic silicon pairs, the hydrogen mainly originates from the interface molecular water. As discussed previously in this chapter, there are 2–3 monolayers of water molecules at the bonding interface of hydrophilic silicon wafers after room-temperature contacting. Molecular water will also come partly from the polymerization reaction

$$\equiv Si{-}OH + HO{-}Si\equiv \longrightarrow \equiv Si{-}O{-}Si\equiv + H_2O \qquad (5.30)$$

Molecular water at the bonding interface or in the native oxide will diffuse toward and react with the surrounding silicon and form hydrogen:

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2 \qquad (5.31)$$

For hydrophobically bonded wafers, hydrogen is desorbed from the surface hydrides during annealing:

$$\equiv Si{-}H + H{-}S \longrightarrow Si{-}Si\equiv + H_2 \qquad (5.32)$$

5.4.2 Prevention of Temperature-Dependent Interface Bubbles

The cavity experiments just described show that the main constituent of the gas in the cavities and, by extension, in interface bubbles is hydrogen. In contrast, experiments on the nucleation of interface bubbles clearly show that the presence of hydrogen alone is generally not sufficient to nucleate interface bubbles, but that thermally desorbed hydrocarbon molecules appear to play a major role (35).

In addition, the reaction between molecular water and silicon at the bonding interface is the main source of hydrogen in hydrophilicly bonded wafers. Methods to prevent bubble formation at the interface of hydrophilicly bonded silicon wafers can therefore be based on: (a) removal of interface hydrocarbons, (b) removal of interface molecular water, and (c) removal of either desorbed hydrocarbon or hydrogen molecules by adsorbing them in a proper material, such as a silicon oxide layer, which reduces their effective volume concentration and the associated gas pressure.

Two techniques have been reported which allow removal of thermally unstable hydrocarbons from the bonding surfaces. The first involves a prebonding annealing of hydrophilic silicon wafers in oxygen at 600°C for 30 min or in argon at 800°C for 30 min (35). Thermally unstable hydrocarbons on the wafer surfaces may be vaporized and/or oxidized during the annealing. After a subsequent flushing with DI water followed by spin drying, the preannealed wafers were bonded at room temperature. No bubbles were observed after annealing at any temperatures even though interface water was still present. The second method (38) employes a very strong oxidizer, periodic acid ($HIO_4 \cdot 2H_2O$), to remove thermally unstable hydrocarbons on the wafer surfaces by an oxidation reaction. In this case, RCA1-cleaned silicon wafers were dipped in boiling ~1% periodic acid for 15 min.

In thermal oxides (fused silica), only 43% of the lattice space is occupied. Because of the open structure of thermal oxide, hydrogen, gaseous hydrocarbons, and other impurities can easily enter this oxide network, resulting in a significant reduction of the gas pressure at the bonding interface. Therefore, a bonding pair consisting of at least one oxidized silicon wafer is much less prone to the generation of temperature-dependent bubbles.

5.4.3 A Simple Model of Bubble Formation

Temperature-dependent bubbles at the bonding interface are nucleated by desorption of adsorbed hydrocarbons and increased in size by hydrogen when the inner pressure of the gas at the interface becomes sufficiently high to

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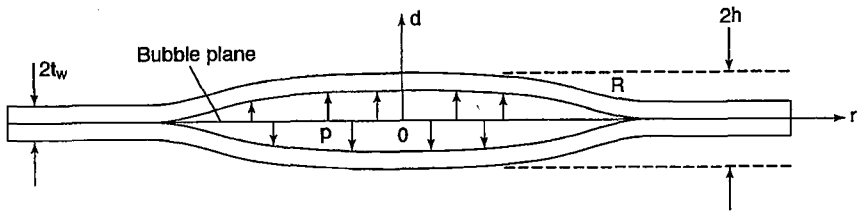

Fig. 5.18 Schematic of a bonded pair with a bubble at the bonding interface (not to scale).

debond the bonding interface. A semiquantitative description of a thermodynamic model of bubble formation has been proposed (39). A simplified model is presented here.

Figure 5.18 is a schematic of a bonded pair with a bubble at the bonding interface. The following assumptions are used in the analysis: (1) the wafers can be treated as elastic thin plates; (2) the bubble radius is large compared to the wafer thickness; (3) the two bonding wafers are of identical thickness and are of the same material; and (4) the height of the bubble is much smaller than the wafer thickness. The thin-plate small elastic deflection theory is therefore valid. The bubble is supported by a uniform excess internal pressure p,

$$p = p_i - p_e \tag{5.33}$$

where p_i and p_e are the internal and external pressures. According to thin-plate elastic theory (40), the local displacement d of each wafer as a function of radial distance r is given by

$$d(r) = h\left[1 - (r/R)^2\right]^2 \qquad 0 \le r \le R \tag{5.34}$$

The central displacement, h, is given by

$$h = \frac{3pR^4(1 - \nu^2)}{16Et_w^3} \tag{5.35}$$

where E is Young's modulus and ν Poisson's ratio.

The bubble volume, V_b, may be calculated by integrating $d(r)$ over the bubble plane (41):

$$V_b = \frac{\pi pR^6(1 - \nu^2)}{8Et_w^3} \tag{5.36}$$

The elastic energy, E_{elas}, of the system is obtained by integrating the uniform internal stresses through the local displacements over the bubble surfaces (41):

$$E_{elas} = \frac{3p^2R^4(1 - \nu^2)}{16Et_w^3} \tag{5.37}$$

Since the elastic energy of the system increases with the bubble extension, R, the bubble will be unstable if the internal excess pressure remains constant. This is the situation in hydrogen-filled bubbles when a hydrogen-implanted silicon wafer is bonded to another silicon wafer and subsequently annealed. Since there is supersaturation of hydrogen in the silicon implanted area, the hydrogen pressure in the hydrogen-filled bubbles does not drop as they grow, resulting in a complete layer splitting. We discuss this process in Chapter 6. Usually, the internal pressure reduces with increasing bubble extension, in this case the bubble becomes stable. At equilibrium, the elastic energy, E_{elas}, equals the bonding energy, 2γ, and the stabilized extension of the bubble is given by

$$R = 1.8\left[\gamma E' t_w^3/p^2\right]^{1/4} \tag{5.38}$$

where $E' = E/(1 - \nu^2)$. If the bubble radius, R, is smaller than the wafer thickness, which is certainly true during the nucleation stage, different expressions must be used. At their nucleation, interface bubbles may contain pressures on the order of 100 MPa. Presently, one can explain a large percentage of experimental results on interface bubbles in bonded silicon wafers by using the assumption that the high pressure associated with bubble nucleation is supplied by desorbed hydrocarbons. As soon as the pressure drops sufficiently during further growth of the bubbles that it becomes smaller than the nucleation pressure of hydrogen at the interface, further growth of the bubbles will occur by incorporation of hydrogen.

5.5 STRUCTURAL DEVELOPMENT OF THIN INTERFACIAL OXIDE LAYERS

It is generally agreed that in bonded Si/Si pairs prepared from hydrophilic surfaces of either Czochralski (CZ) grown or Float Zone (FZ) grown silicon wafers, there is a thin amorphous layer of interfacial oxide present at the bonding interface (Fig. 5.19), whereas the bonding interface of hydrophobic silicon wafers does not show presence of any oxide layer (Fig. 5.20). It has been found that the thickness of the oxide layer in the case of hydrophilic surfaces is ~40–50 Å after room temperature bonding and ~20–25 Å after annealing at >1000°C (42, 43). It is believed to result mostly from the native

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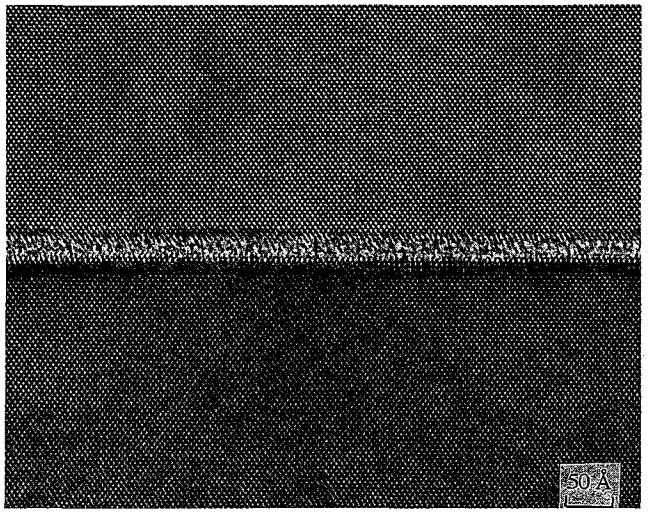

Fig. 5.19 Cross-sectional high-resolution transmission electron micrograph of the bonding interface of hydrophilic bonded (100) silicon wafers after 3 h annealing at 1100°C. The amorphous thin native oxide layer can easily be seen.

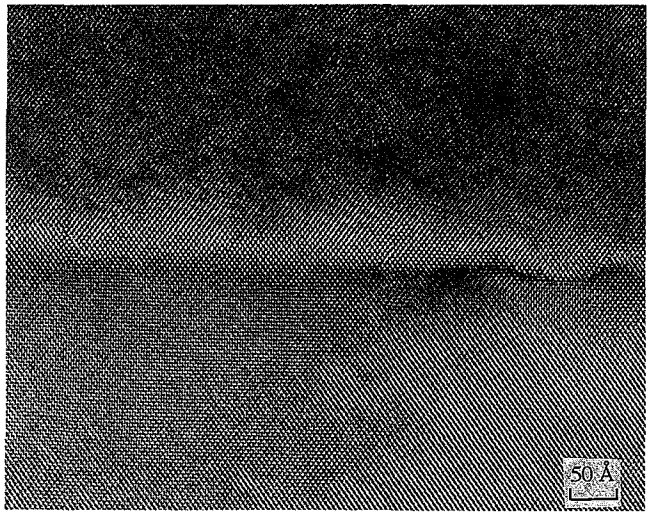

Fig. 5.20 Cross-sectional high-resolution transmission electron micrograph of the bonding interface of hydrophobic bonded (100) silicon wafers after 3 h annealing at 1100°C.

Fig. 5.21 High-resolution transmission electron micrograph of disintegrated interface native oxide layer for slightly misoriented (rotational angle < 1°) float-zone bonded silicon wafer pair after annealing at 1100°C for 2 h in nitrogen.

oxide layers on the surfaces of the hydrophilic wafers prior to mating and partly from the reaction of interfacial water with silicon.

The interfacial oxide layer of well-aligned bonded wafers of the same orientation is found to disintegrate into oxide islands after a few hours at an annealing temperature of around 1100°C. An example is shown in Fig. 5.21. The oxide islands are typically 500–1000 Å in diameter. The oxygen diffusivity is not high enough to allow oxide layer dissolution by diffusion of interfacial oxygen from the oxide layer into the bulk of the silicon wafers. The driving force for the disintegration is the minimization of the total energy associated with the bonding interface and the Si/SiO_2 interfaces.

5.5.1 Influence of Rotational Wafer Misorientation

The disintegration of the oxide layer starts by the formation of holes in the oxide layer. The nucleation energy E_n for the hole formation is proportional to the square of the oxide thickness t_{ox} (44):

$$E_n = \sigma \frac{\pi t_{ox}^2}{2} \tag{5.39}$$

where σ is the energy of the oxide/Si interface per unit area. The hole formation in the oxide layer will become increasingly more difficult and the oxide layer more stable with increasing thickness of the oxide layer. For instance, the nucleation energy of 20 Å-thick oxide is around 3.5 eV. For a 30 Å-thick oxide it will be about 8 eV, making disintegration a very unlikely process.

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After sufficient holes have been formed in the oxide layer, the remaining oxide layer will finally spheroidize to further decrease the interface energy. Since a small rotational misorientation results in the generation of a network of screw dislocations at the interface between two bonded wafers, a positive energy term must be taken into account in addition to a negative energy term, owing to the decrease in oxide/Si interface area. At a certain critical angle, the energy decrease due to disintegration and the energy increase due to dislocation formation will balance each other. If the misorientation angle is larger than the critical angle, the disintegration is energetically unfavorable. The critical angle θ is given by the approximate relation

$$\theta = \frac{4\pi\sigma}{\mu b \ln(1/4\theta)} \tag{5.40}$$

where μ is the shear modulus [0.7×10^{11} N/m^2 for (100) silicon], b is the Burgers vector [3.84 Å for (100) silicon], and σ is the Si/SiO_2 interface energy. Critical angles ranging from 1° to 5° are obtained for silicon wafers from Eq. (5.40) and also experimentally (44).

5.5.2 Influence of Oxygen Content of Si Bonding Wafers

A thickening of the interfacial oxide layer of CZ wafer pairs after further annealing was observed and attributed to the diffusion of supersaturated oxygen from the bulk of the CZ silicon wafers to the interfacial oxide layer (44, 45). For instance, a bonded CZ silicon wafer pair with 1° off-rotational misorientation showed an increase in oxide thickness from 20 to 130 Å after 5 days at 1150°C. The interstitial oxygen concentration in typical CZ silicon is around 7×10^{17} cm^{-3} while the oxygen solubility in silicon at 1150°C is 3.46×10^{17} cm^{-3}. The oxide thickness increase can be estimated by (45)

$$\Delta t_{ox} = \frac{2\left[C_{i1} + C_{i2} - 2C_{ieq}(T)\right]}{n_{ox}} \sqrt{\frac{D_i(T)t}{\pi}} \tag{5.41}$$

where C_{i1} and C_{i2} are concentrations of oxygen interstitials in each bonding wafer, C_{ieq} and D_i are the solid solubility and the diffusivity of oxygen interstitials, and n_{ox} is the concentration of oxygen in the grown oxide layer.

The same equation can be employed to predict the dissolution of interfacial oxide layers in FZ pairs. The interstitial oxygen concentration in typical FZ silicon is around 5.5×10^{14} cm^{-3}, well below the oxygen solubility in silicon at 1150°C (3.46×10^{17} cm^{-3}). Therefore, the oxygen diffuses from the oxide layer into the bulk, resulting in shrinkage and final disappearance of the oxide layer.

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6

Thinning Procedures

6.1 MECHANICAL THINNING

After room-temperature bonding and subsequent annealing, the device wafer of the bonded pair usually needs to be thinned over the entire wafer. Device layer thickness and its uniformity requirements vary with applications. Table 6.1 lists typical specifications of the device layers for sensor, bipolar power device, high-speed bipolar and BiCMOS, and CMOS VLSI applications. There are two approaches to uniform thinning of the device wafer of a bonded pair: (1) mechanical thinning with possibly subsequent refinement by local plasma etching or polishing and (2) layer transfer associated with etch-stop or layer-splitting methods. The applications of these thinning methods are indicated in Table 6.1; we discuss the technologies in the following sections.

Currently, mechanical thinning technology can routinely produce thick device layers (>1 μm) with a thickness variation of ± 0.5 μm (1, 2). If followed by a local polishing or plasma etching, a device layer with a thickness down to less than 0.1 μm with a thickness variation of less than 10% for mainstream VLSI CMOS can be realized (3). There are two main layer-transfer technologies: (1) selective chemical etching and (2) splitting of an H-implanted layer from the device wafer (4). Both technologies have demonstrated the ability to meet VLSI CMOS requirements.

6.1.1 Chemical–Mechanical Polishing (CMP)

The state of the art mechanical thinning approach consists of a grinding technology and a chemical–mechanical polishing (CMP) technology. Lapping is now being replaced by grinding which allows tighter control of the thickness and lower subsurface damage. During the grinding operation, the device wafer is thinned using the back of the handle wafer as a reference. Therefore, the handle wafers should be as flat as possible. Using a grind wheel with diamond or silica particles, the silicon is removed from the device wafer to a total thickness which is the sum of the device layer thickness and the handle wafer thickness. The subsurface damage depth is on the order of a few microns down to the submicron range, depending on the grinder

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TABLE 6.1 Typical Requirements of Silicon Device Layers for Various Applications and the Corresponding Thinning Technologies

	Sensors	Bipolar and Power Device	High Speed Bipolar, BiCMOS	CMOS VLSI
Silicon layer thickness	1–10 μm	4–100 μm	1–2 μm	0.1–0.05 μm
Silicon layer thickness uniformity	± 1 μm	± 0.5 μm	± 0.1 μm	$\pm 5\%$
Thinning technology	Mechanical thinning		Local polishing or etching, or layer transfer	

configuration used. After grinding and the removal of subsurface damage by chemical etching, CMP is used to achieve a smooth surface and the desired thickness. The CMP principle and the resulting surface quality are described in Chapter 4. As noted, multiple wafer polishers are not suitable for thinning the bonded wafers owing to poor thickness control within a batch. Instead, single-wafer polishers have to be used. At present, mechanical thinning can offer device layers thicker than 1 μm with a thickness variation of ± 0.5 μm.

6.1.2 Refinement by Local Thinning

After mechanical thinning the device layer can be further thinned to meet VLSI CMOS requirements by local polishing or plasma etching. A high-density film thickness map with sufficient spatial resolution is first produced and then a localized polish pad or plasma is moved across the surface of the wafer while varying dwell time inversely to the local thickness of the device layer to mechanically or chemically thin the device layer and make its thickness more uniform (3, 5). Because the effective removal rates are low, the local polishing technique has not been widely adapted. However, the local plasma etching method has found its way into production (5).

Fig. 6.1 is a schematic illustration of the thinning process (5). For thin SOI fabrication, a thickness map of the initial SOI layer with a 64×64 point array is obtained by using a visible reflectance technique with a thickness resolution of better than 10 Å. Conventional instruments use a visible to near-IR broadband light source and a microscope objective to illuminate a small sample area on the wafer. Employing a grating to disperse the reflected light onto a one-dimensional detector array, the detector output is serially processed by a computer to determine film thickness by pattern match to stored spectral signatures corresponding to known film thicknesses. This method requires 100 min to measure a 20×20 point array. A new advanced technique has been developed to speed up the measurements. The broadband light source is sequentially filtered and fully illuminates the wafer. The reflected light is imaged onto a two-dimensional CCD array whose output is

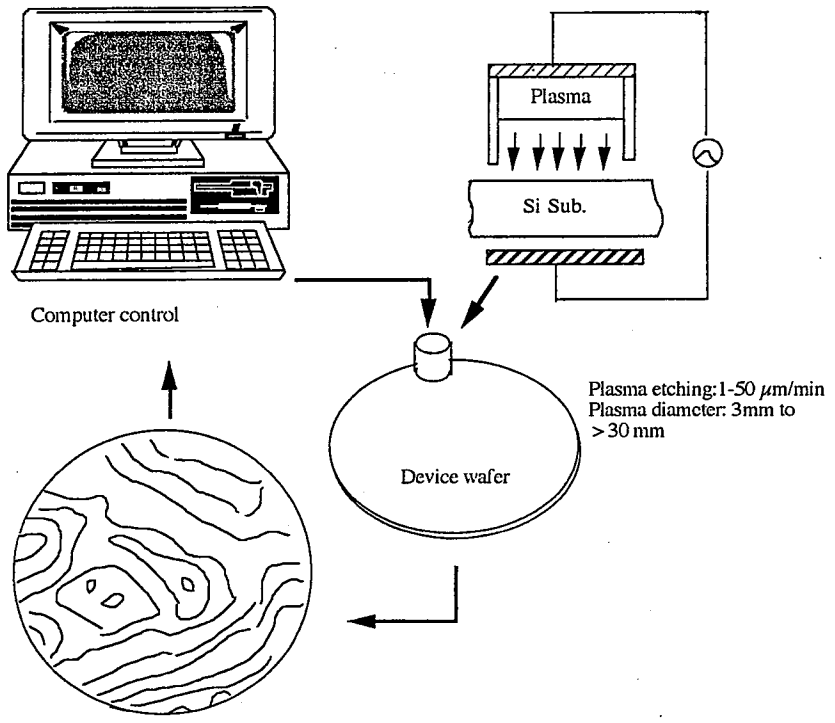

Fig. 6.1 Schematic of refinement process of a mechanically thinned SOI wafer by local plasma-assisted chemical etch.

parallel processed to yield a 64×64 array of measurements in less than 1 min. The buried oxide thickness is also measured.

Having a map of film thickness and the stationary plasma etch profile, the etching time for each position on the wafer can be obtained to achieve a desirable uniform thickness. The dwell times are converted into scanning stage commands. The wafer is scanned under the plasma such that the etch area is local at a time and material removal is controlled by the computer scan commands. Measuring and etching can be iterated for more stringent tolerances. With this process, and using appropriately polished initial SOI wafers, SOI layer thicknesses less than 1000 Å with a uniformity better than 10% have been obtained. The physical properties of resultant SOI layers, such as crystal defects, surface impurities, and surface microroughness, have been evaluated. It appears that the plasma process does not noticeably degrade the intrinsic quality of the original bonded silicon layers.

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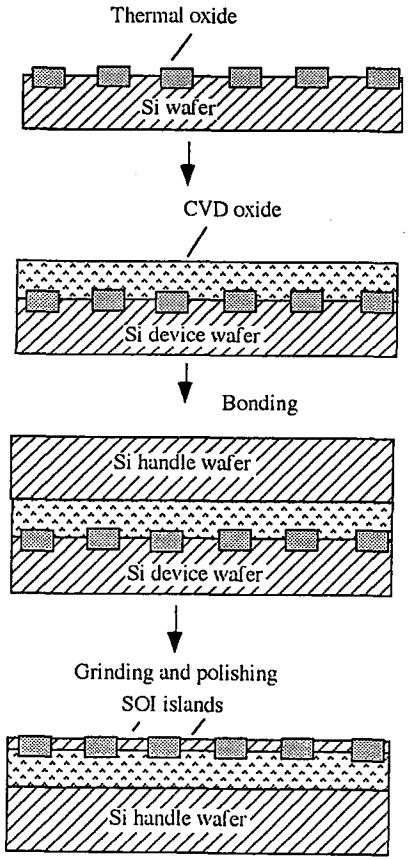

Fig. 6.2 Polish-stop method for small ultrathin SOI islands.

6.1.3 Polish-Stop Technology

To achieve device layers by a mechanical thinning approach with thickness specifications required by VLSI CMOS, a polish-stop technology has also been developed (6) as schematically shown in Fig. 6.2. The polish-stop method employs a selective polishing effect for a material having a polishing rate much lower than silicon present in a predefined pattern on the device wafer. During the thinning process the polishing almost stops when the polish stop is reached. This approach leads to application-specific wafers rather than wafers for general applications. In this process, the thermal oxide is selectively grown on the device wafer by a standard LOCOS (LOCal Oxidation of Silicon) process using nitride as a mask during the oxidation. PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide is then deposited on the device wafer, densified, and smoothened. A handle wafer is subsequently bonded to this CVD oxide. The device wafer is ground to a thickness of a few microns. Final polishing stops when the oxide polish-stop is reached, resulting in device islands with a thickness equal to the thickness of the oxide. In practice, the thickness variation of the device islands depends on the size of the silicon islands. As the silicon island size gets larger, the thickness variation increases. For silicon islands with an area of 20×20 μm, device layers with a thickness of (600 ± 80) Å were demonstrated (6). Polishing selectivity is a function of many polishing parameters such as pressure, pH value, silica concentration, viscosity and flow rate of the slurry, and temperature. Therefore, the polishing process should be optimized to stop on the specific material which is designed for the polish stop. Table 6.2 gives typical CMP polishing selectivities of silicon to thermal oxide (SiO_2), PECVD oxide (TEOS), silicon nitride (Si_3N_4), and BN.

TABLE 6.2 Typical Polishing Selectivities of Silicon to Other Materials

Material	SiO_2	TEOS	Si_3N_4	BN
Selectivity (Si/material)	~ 5–10	~ 2–3	~ 10–100	~ 50–100

6.2 SILICON CHEMICAL ETCHING

The layer transfer process achieved by a chemical etching approach is schematically shown in Fig. 6.3. The process is commonly termed BESOI (Bonding and Etch-back Silicon-On-Insulator). To transfer a single-crystalline silicon layer that is on the top of an etch-stop layer in a device wafer onto a handle wafer, the two wafers are first bonded to each other, followed by an annealing step to strengthen the bond (see Fig. 6.3*a*). Then the entire device wafer in a bonded pair is thinned by grinding and polishing to leave silicon of a few tens of microns, followed by chemical etching until the etching is stopped by the etch-stop layer (Fig. 6.3*b*). During the etching process the handle wafer is protected by a coated mask layer. The etch-stop layer is then removed selectively. The thin and uniform device layer has thus been transferred onto the desired handle wafer (Fig. 6.3*c*).

The etch-stop performance can be described by the etch selectivity (etch-rate ratio) S of silicon to the etch-stop layer:

$$S = R_{si}/R_{e\text{-}s} \tag{6.1}$$

where R_{si} is the etch rate of silicon and $R_{e\text{-}s}$ is the etch rate of the etch-stop. $S = 1$ corresponds to the case of no etch selectivity.

One method to evaluate the etch-stop efficiency is to measure the maximum "etch step" across the etch-stop and nonetch-stop boundary, such as in

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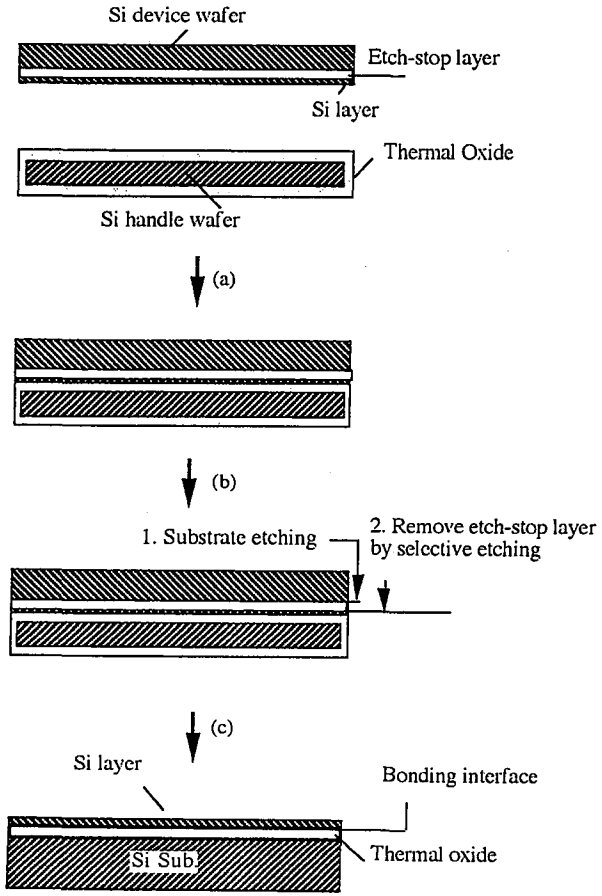

Fig. 6.3 Typical process flow of BESOI approach. (*a*) Bonding and annealing; (*b*) etch-back; (*c*) layer transferred.

the case of an etch-stop formed by ion implantation (7) (see Fig. 6.4). This approach appears to be more meaningful because the etch rate is likely to vary with the implant profile. The maximum etch step is observed when the etch-stop layer has been totally etched off. From a practical point of view, the maximum etch step is a critical quantity because it determines the acceptable thickness variation of the device wafer after grinding and polishing prior to the etch back. For example, if the maximum etch step is 3 μm, the allowable thickness nonuniformity of the device wafer after the usual mechanical thinning procedure should be less than ± 1.5 μm. Obviously, the average etch selectivity S can be derived from the effective etch-stop layer thickness,

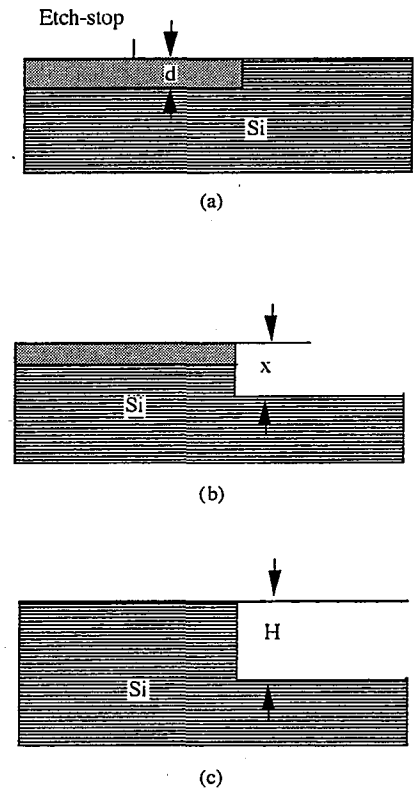

Fig. 6.4 Schematic of maximum etch step measurement. (*a*) Etching time = 0; (*b*) etching time = t_1; (*c*) etching time = t.

d, and the maximum etch step, H, as

$$S = \frac{d + H/t}{d/t} = 1 + \frac{H}{d} \tag{6.2}$$

where t is the etch time for reaching the maximum etch step.

6.2.1 Aqueous Alkaline Etchants

Aqueous alkaline solutions are commonly used anisotropic silicon etchants. There are two types of etching solutions: (1) pure inorganic aqueous alkaline solutions such as KOH, NaOH, CsOH, and NH_4OH and (2) organic alkaline aqueous solutions such as EDP (ethylenediamine–pyrocatechol–water), TMAH (tetramethyl ammonium hydroxide), or hyrazine. An electrochemical model for the reaction mechanisms has been suggested and is believed to be useful for all types of alkaline solutions (8):

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The reaction is a redox (reduction and oxidation) process and the key reacting species is the HOH/OH^- redox couple in the etching solution. In the oxidation reaction, a silicon atom is removed from the surface by reaction with four OH^- ions:

$$Si + 4OH^- \longrightarrow Si(OH)_4 + 4e^- \quad (6.3)$$

The neutral $Si(OH)_4$ can readily diffuse away from the silicon surface into the solution. The four free electrons generated from the reaction above are located in the silicon very close to the surface.

In the reduction reaction, these electrons leave the silicon surface and react with HOH molecules close to the silicon surface:

$$4HOH + 4e^- \longrightarrow 4OH^- + H_2 \quad (6.4)$$

Only these OH^- ions, which are generated at the silicon surface, are considered to be the main reacting species. The OH^- ions from the bulk of the etching solution experience a repulsive force from the negatively charged silicon surface and therefore do not play a major role in the reaction. The negative charges on the silicon surface originate from the higher Fermi level of the HOH/OH^- couple than that of the silicon in the etching solution.

For aqueous KOH solutions with a concentration between 10 and 60%, the etch rate of normally doped silicon can be calculated by

$$R_{si} = k_0[HOH]^4[KOH]^{1/4} e^{-E_a/kT} \quad (6.5)$$

where $E_a = 0.595$ eV and $k_0 = 2480$ μm/h(mol/L)$^{-4.25}$ [for the silicon (100) surface] and $E_a = 0.60$ eV and $k_0 = 4500$ μm/h(mol/L)$^{-4.25}$ [for the silicon (110) surface]. The etch rate of (100) silicon as a function of KOH concentration at a temperature of 72°C is shown in Fig. 6.5. It can be seen that at high KOH concentrations the silicon etch rate becomes limited by the water concentration. Fig. 6.6 is an experimental diagram of the etch rate as a function of temperature for (100) silicon wafers in various KOH solutions.

This reaction model indicates that a change in OH^- concentration in the bulk of the etching solutions causes only little change in the etch rates and that the cations in different etching solutions, K^+, Na^+, Cs^+, and $(NH)_4^+$, make almost no difference in the etching behavior. The selection of the etching solutions is mainly determined by the concerns of etch selectivity, IC process compatibility, handling, anisotropy, and cost for a specific application.

6.2.2 Etch Selectivity of Aqueous Alkaline Solutions

6.2.2.1 Silicon Oxide The etching reaction of silicon oxide can be described as (8)

$$SiO_2 + 2OH^- \longrightarrow SiO_2(OH)_2^{--} \quad (6.6)$$

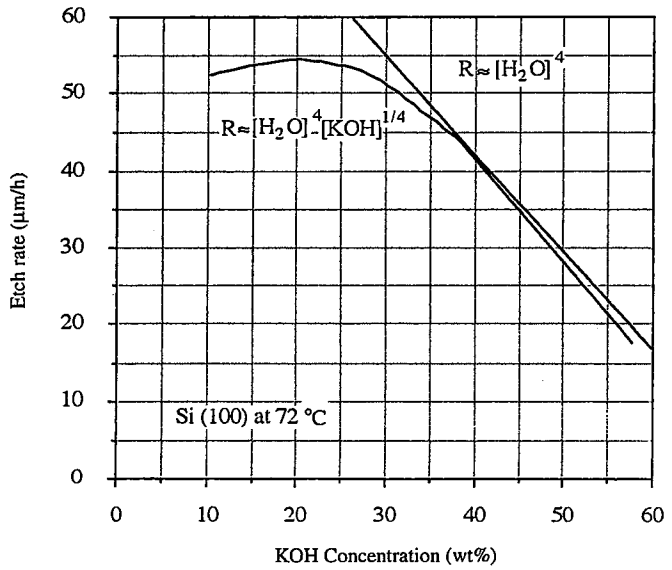

Fig. 6.5 Etch rate of (100) silicon as a function of KOH concentration at 72°C.

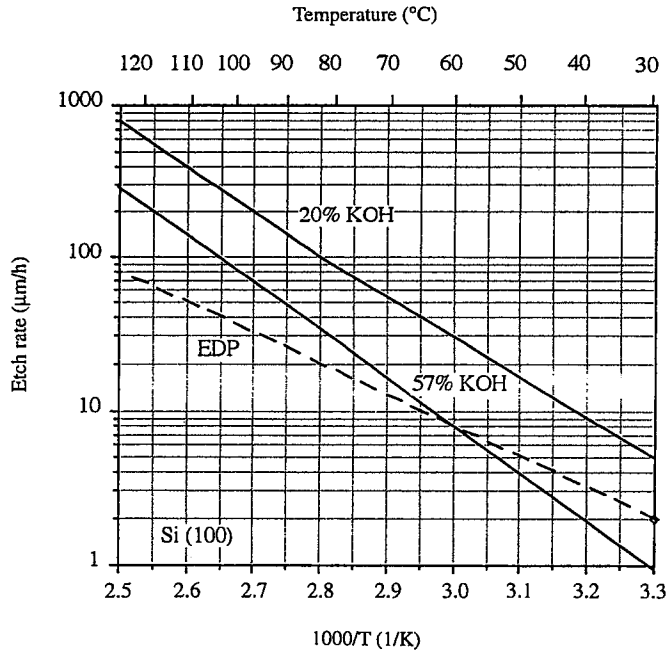

Fig. 6.6 Etch rate of (100) silicon in KOH and EDP as a function of temperature.

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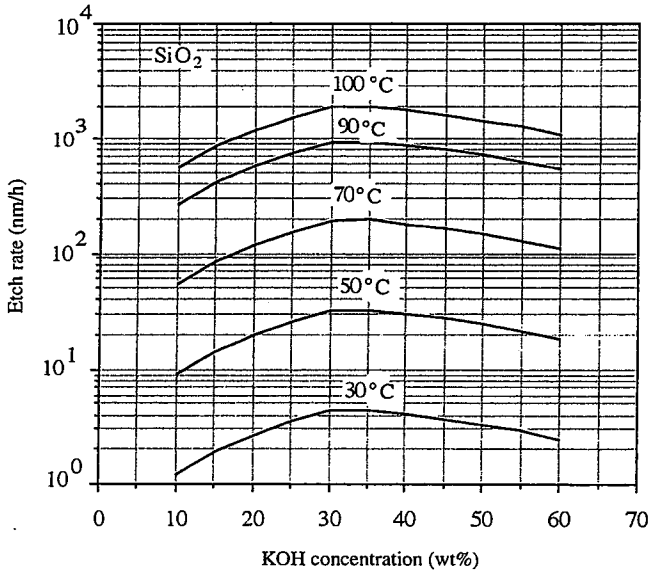

Fig. 6.7 Etch rate of silicon oxide as a function of KOH concentration and temperature.

According to Eq. (6.6), the silicon oxide etch rate depends on the concentration of OH ions in the bulk of the etching solution. The SiO_2 etch rate as a function of KOH concentration and temperature is plotted in Fig. 6.7. A linear dependence on the molar KOH concentration is shown and the maximum etch rate occurs at ~35% KOH. At higher concentrations, the etch rate decreases with the square of the water molar concentration, indicating that water plays a role in the reaction. The reason is as follows: at pH values larger than 2.8, a negative charge builds up on the oxide surface in the KOH solution, hindering the diffusion of OH^- ions, but not the neutral water molecules, to reach the oxide surface.

Fig. 6.8 shows the etch selectivity of (100) silicon to silicon oxide as a function of temperature in KOH and EDP solutions. The etch selectivity in EDP is about two orders of magnitude larger than that in KOH solutions. The compound EDP is a popular aqueous organic alkaline solution for silicon anisotropic etching. The composition of the most commonly used EDP solution is

$$\text{Ethylenediamine } (NH_2(CH_2)_2NH_2):\text{pyrocatechol } (C_6H_4(OH)_2):$$
$$\text{water } (H_2O):\text{pyrazine } (C_4H_4N_2) = 1.0\text{ L}:160\text{ g}:133\text{ mL}:6\text{ g}$$

The etch rate of (100) silicon in the EDP solution is shown in Fig. 6.6. The etch rate of SiO_2 as a function of temperature in EDP and KOH solutions is

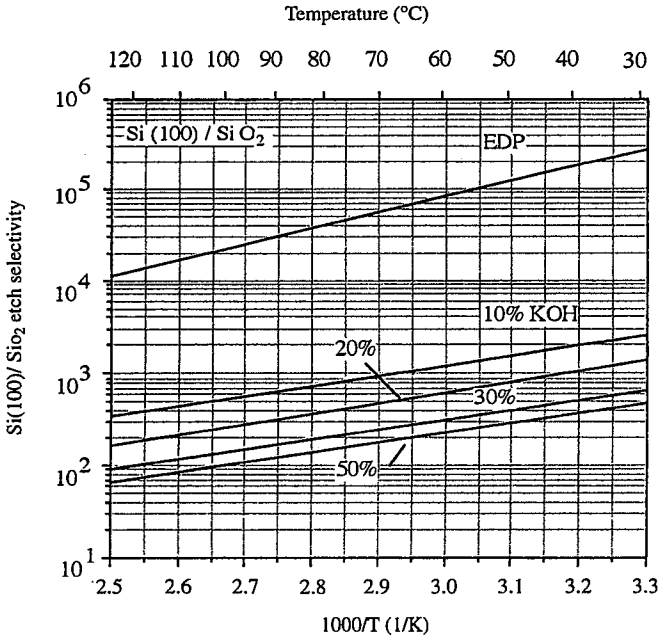

Fig. 6.8 Etch selectivity of (100) silicon to silicon oxide in KOH and EDP.

shown in Fig. 6.9. The three orders of magnitude slower etch rate in EDP than that in KOH is attributed to the three orders of magnitude smaller OH^- ion concentration (0.0034 mol/L) in EDP than in KOH solution (5–10 mol/L).

For process compatibility with mainstream IC fabrication and for nontoxicity, an etch solution based on ammonium hydroxide–water and quaternary ammonium hydroxide–water solutions has been introduced recently for silicon etching. The most commonly used etch solution of this kind is TMAH [tetramethyl ammoniumhydroxide, $(CH_3)_4NOH$]. The dependences of (100) silicon and silicon oxide etch rates in TMAH on concentration and temperature are shown in Figs. 6.10 and 6.11, respectively (9). The etch selectivity of (100) silicon to silicon oxide is slightly smaller than that in EDP.

6.2.2.2 P^{++} Silicon (10, 11) It has been found that the silicon etch rates of all aqueous alkaline etchants are reduced significantly if silicon is doped with boron at concentrations exceeding 2×10^{19} cm^{-3} (see Fig. 6.12) for (100) silicon. This etch-stop effect can be explained according to the etching mechanisms discussed above. At boron concentrations greater than 2.2×10^{19} cm^{-3}, silicon becomes degenerate. The four electrons generated by the oxidation reaction Eq. (6.5) have a high probability of recombination with

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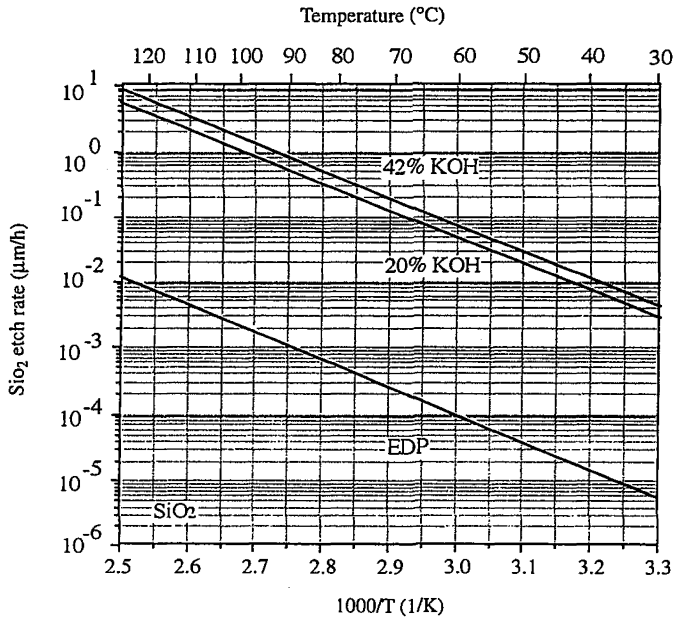

Fig. 6.9 Etch rate of silicon oxide in KOH and EDP as a function of temperature.

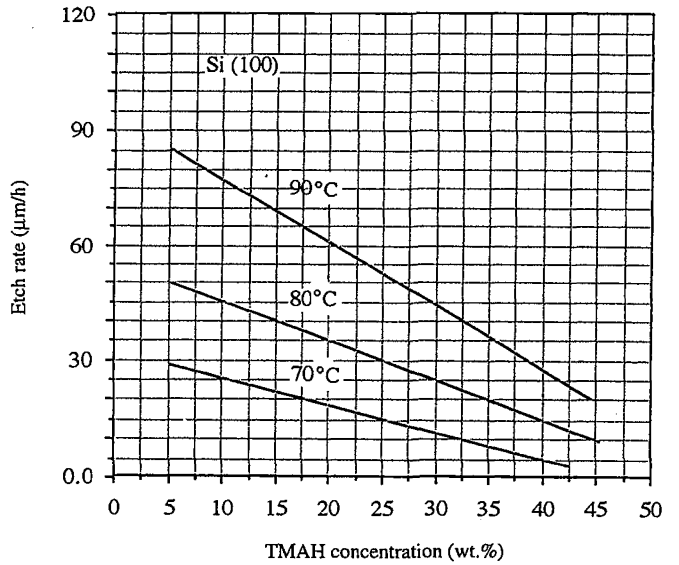

Fig. 6.10 Etch rate of (100) silicon as a function of TMAH concentration and temperature.

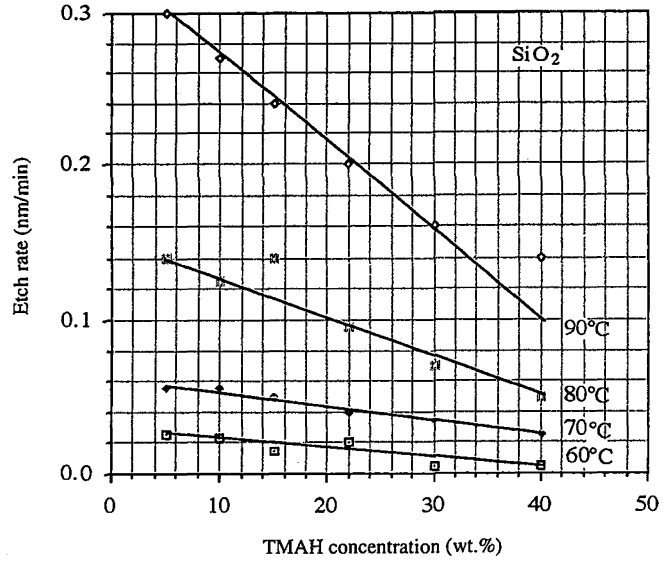

Fig. 6.11 Etch rate of silicon oxide as a function of TMAH concentration and temperature.

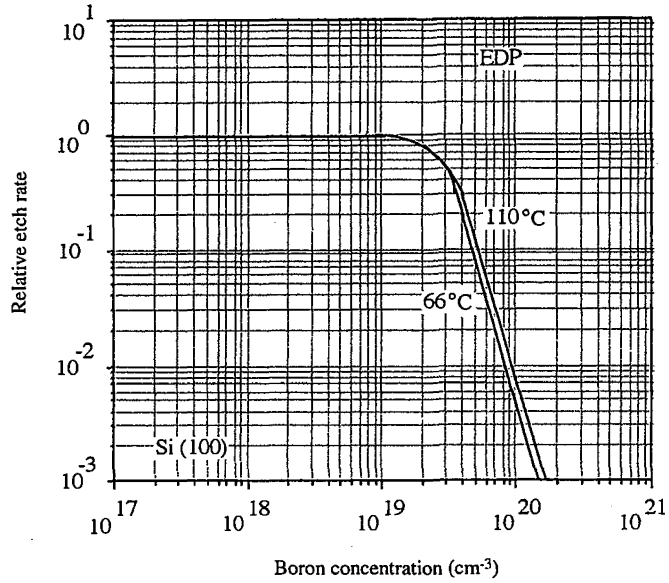

Fig. 6.12 Relative etch rate of (100) silicon as a function of boron concentration in EDP.

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holes which are available in very large quantity in the silicon. As a result, the four electrons are no longer available for the subsequent reduction reaction Eq. (6.6) which is required to continue the etching process. Only the available thermal equilibrium electron concentration $n = n_i/p_2$ determines the remaining silicon etch rate. Since the hole concentration, p, originating from the heavily doped boron or any other III group impurities is so high, the remaining number of the electrons is small. Clearly, the hole concentration in silicon, rather than the boron or any other elements of III group concentration, determines the etch rate. Experimental results show that $\sim 8 \times 10^{19}$ cm^{-3} and 1×10^{20} cm^{-3} of boron doping are required to have an etch selectivity of 100 for lightly doped (100) silicon relative to the heavily boron-doped silicon in EDP and 10% KOH, respectively. At higher KOH concentrations, the etch selectivity is lowered, mainly because of the slower etch rate of lightly doped silicon in the KOH solutions. Addition of isopropyl alcohol (IPA) into KOH solution can increase the etch selectivity owing to its ability to adjust the relative water concentration in the etchant without significantly affecting the pH value.

*6.2.2.3 **Carbon-Doped Silicon*** It has been found that carbon-doped silicon exhibits a significantly reduced etch rate in EDP. Fig. 6.13 shows the experimental etch selectivity of carbon-implanted (100) silicon in EDP and

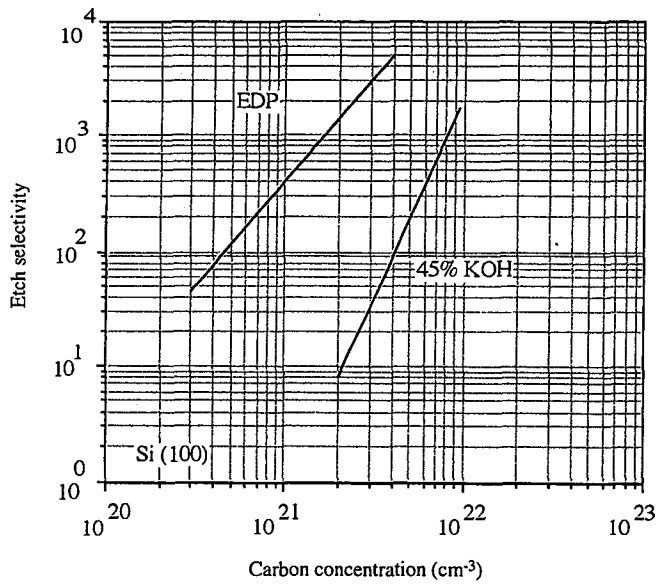

Fig. 6.13 Etch selectivity of (100) silicon to carbon-implanted silicon layer as a function of carbon concentration.

45% KOH at 85°C as a function of the carbon peak concentration (12). The etch selectivity reaches 1000 in EDP at a carbon peak concentration of 1.5×10^{21} cm^{-3}.

Since the carbon concentrations are not sufficient to form a continuous SiC layer (13), the etch-stop effect of the carbon-doped silicon layer appears to arise from the chemical characteristics of the nonstoichiometric Si_xC_{1-x} alloy formed by randomly distributed implanted carbon atoms with the host silicon atoms (7). It should be mentioned that CVD silicon carbide (SiC) layers as well as SiC layers formed by implantation show almost no etching in KOH, EDP, or any other alkaline solutions (14).

*6.2.2.4 **Germanium-Doped Silicon*** Germanium-doped silicon forms a Si_xGe_{1-x} alloy which also exhibits an etch-stop effect. An MBE (molecular beam epitaxy) $Si_{0.7}Ge_{0.3}$ layer grown at 500°C showed an etch selectivity of 17 relative to normal (100) silicon before annealing at 850°C (15). The germanium concentration in the layer was 1.5×10^{22} cm^{-3}. After annealing, the etch selectivity was reduced to 10–12. The etch-stop effect is believed to be associated with the strain induced by the relatively larger atom size of germanium.

Si_xGe_{1-x} layers formed by germanium implantation in silicon show higher etch selectivities than MBE or CVD grown Si_xGe_{1-x} layers (7). When (100) silicon is implanted with a dose of 5×10^{15} cm^{-2} Ge at 200 keV, which corresponds to a peak Ge concentration of 3.1×10^{20} cm^{-3}, the etch selectivity reaches 12. This result indicates that amorphization of the implanted layer is a factor in determining the etch-stop efficiency in germanium-implanted samples (15).

*6.2.2.5 **Nitrogen-Implanted Silicon*** Nitrogen implanted into silicon with a dose of 1×10^{17} cm^{-2} at 140 keV can form an etch-stop layer. These implantation conditions lead to a nitrogen peak concentration of 6×10^{21} cm^{-3}, which is 10 times lower than necessary for forming a continuous silicon nitride (Si_3N_4) layer (10). High annealing temperatures tend to degrade the etch-stop efficiency, indicating that the electron traps introduced by the nitrogen implantation may play an important role in recombining the four electrons necessary for the silicon etching. The CVD silicon nitride (Si_3N_4) layers show no measurable etch rate in KOH, EDP, and any alkaline solutions. Therefore, it can be considered as a perfect masking material for practical applications.

6.2.3 Silicon Anisotropic Etching

The alkaline solutions described above etch silicon anisotropically. The experimental results of the etch rates of (100), (110), and (111) silicon in EDP solution as a function of temperature are shown in Fig. 6.14. Similar curves

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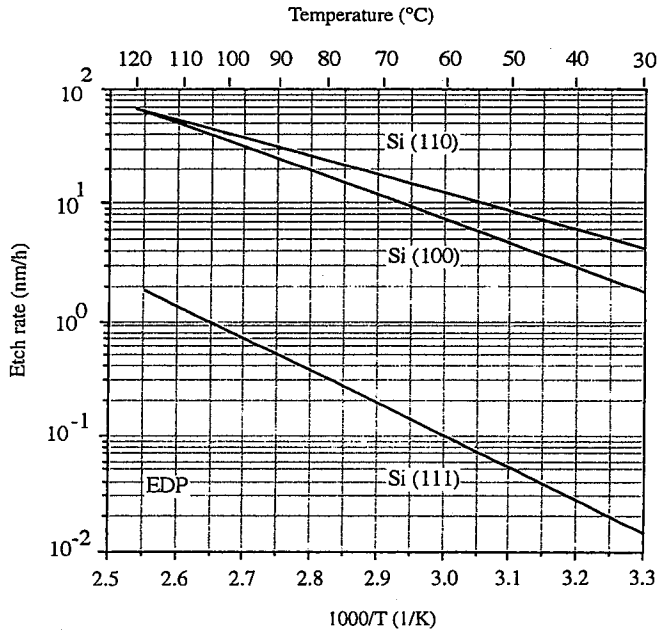

Fig. 6.14 Etch rates of (100), (110), and (111) silicon as a function of temperature in EDP.

are available for KOH solutions. For EDP the following etch rate ratios hold:

The etch rate ratio of (110):(100):(111) = 50:30:1 at 100°C
The etch rate ratio of (110):(100):(111) = 160:100:1 at 30°C

The anisotropy results from the fewer surface Si–OH bonds per unit cell on (111) compared to that on (100) and (110) surfaces, leading to a higher energy to break the backbonds of the (111) surface silicon atoms in the etchant (8). The anisotropic etch effect can be employed to generate V-grooves with a self-adjusting depth in (100) silicon wafers based on openings in an appropriate mask such as an oxide layer. The formation of V-grooves in silicon is the basis of dielectric isolation technology for high-voltage devices. We discuss this topic in Section 11.2. The (111) planes in silicon form an angle of 54.7° with the (100) plane. If we neglect the etching of the (111) planes, the width W of the oxide window of the pattern approximately determines the final depth of the etched groove d (see Fig. 6.15):

$$d \cong \frac{w}{2} \tan 54.7 \cong 0.7W \tag{6.7}$$

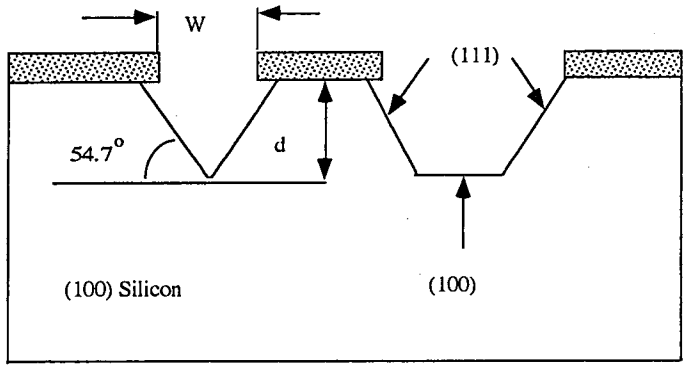

Fig. 6.15 Anisotropic etching in (100) silicon to form V-grooves.

6.2.4 Silicon Isotropic Etching

The most commonly used isotropic silicon etch solution is HF–HNO_3 solution in acetic acid (CH_3COOH) (17). The nitric acid oxidizes silicon to form silicon oxide, which is then dissolved by HF:

$$Si + 4HNO_3 \longrightarrow SiO_2 + 2H_2O + 4NO_2 \tag{6.8}$$

$$SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O \tag{6.9}$$

The H_2SiF_6 is removed by dissolving it in the solution. Acetic acid is a buffering agent which reduces the dissociation of nitric acid.

The etch solution, commonly termed "1-3-8" etch, can be used to etch heavily doped silicon (p^{++} or n^{++}) about 100 times faster than normal silicon:

$$HF(49\%):HNO_3(30\%):CH_3COOH\ (100\%) = 1:3:8 \text{ (in volume)}$$

The etch rate of silicon with a boron concentration greater than 7×10^{18} cm^{-3} is 2 μm/min (18). It decreases to ~ 0.02 μm/min at a concentration of 3×10^{17} cm^{-3}. The etch rate of silicon with a phosphorous concentration greater than 8×10^{18} cm^{-3} is 2.9 μm/min. It decreases to 0.16 μm/min at a concentration of 5×10^{17} cm^{-3}.

Since oxidation of lightly doped silicon is much slower than that of heavily doped silicon, the rate-determining step in the etching of lightly doped silicon by the 1-3-8 etch appears to be the oxidation. In heavily doped silicon the rate-determining step becomes the HF diffusion, which is fast (18).

6.3 LAYER TRANSFER

Thinning of entire silicon wafers of bonded pairs for device layers to submicron thickness with a variation of less than 10% is usually achieved by a layer-transfer approach in which a predetermined thin and uniform, epitaxial

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single crystalline silicon layer on a silicon device wafer is transferred onto a desired substrate (handle wafer). The wafer to which the silicon layer is transferred does not necessarily have to be a bare or oxidized silicon wafer, but can consist of some other material such as quartz, sapphire, or diamond. The predetermined thin and uniform silicon layer can be created, for example, by epitaxial layer growth or ion implantation. Layer transfer is commonly realized by bonding and subsequent chemical etch-back of the device wafer in which the predetermined thin and uniform silicon layer is on the top of a built-in etch-stop. The most popular etch-stop layers include B/Ge, C, and oxide. Recently, another layer-transfer method has been demonstrated in which a hydrogen-implanted wafer is bonded to a handle wafer and the implanted layer is split from the handle wafer during annealing (4).

6.3.1 Layer Transfer by Bonding and Etch-Back

6.3.1.1 B and B/Ge Etch-Stop As described above, heavily boron-doped silicon exhibits a significantly lower etch rate than that of normal lightly doped n- or p-type silicon in alkaline aqueous solutions. Therefore, the use of a B etch-stop is the most frequently used method for thinning the device wafer in a bonded silicon pair. However, there are problems associated with heavy doping of boron in silicon, mainly, boron outdiffusion and misfit dislocations.

Boron is an electronically active impurity in silicon and has a relatively high diffusivity at normal heat-treatment temperatures. The thermal budget for bonding, annealing, oxidation, or activation of implanted boron is therefore limited.

The size of a boron atom is smaller than that of a silicon atom: when in tetrahedral covalent bonding conditions, the radii of silicon and boron are 1.17 and 0.88 Å, respectively. Substitutional boron in silicon causes a tensile stress locally and a shrinkage collectively. The equilibrium lattice constant of the boron-doped layer becomes mismatched with the silicon substrate and stress along the interface increases with dopant concentration. If the highly boron-doped layer is sufficiently thin, the mismatch strain can be accommodated elastically such that the lattice parameters parallel to the interface with the substrate remain unchanged. The critical thickness t_c is given by (19, 20):

$$t_c = \frac{b(1 - \nu \cos^2 \theta)[\ln(t_c/b) + 1]}{8\pi(1 + \nu) f \cos \lambda} \tag{6.10}$$

where b is the length of the Burger's vector (3.84 Å for 60°-type dislocations in silicon), θ is the angle between the dislocation line and its Burger's vector, λ is the angle between the slip direction and that line in the interface plane which is normal to the line of intersection between the slip plane and the interface ($\theta = \lambda = 60°$), and f is the misfit (21):

$$f = \alpha N_B / a_{si} \tag{6.11}$$

where α is an experimental constant equal to -1.49 Å, N_B is the boron concentration in dimensionless atomic fractions (obtained by multiplying the volume concentration by the atomic volume of silicon: 2×10^{-23} cm^{-3}), and a_{si} is the silicon lattice constant (5.4307 Å at 25°C).

However, if the doped layer is thicker than t_c, the stress will be partly released by a plastic deformation of the silicon crystal in the form of misfit dislocations. Consequently, the device layer epitaxially grown on top of the etch-stop layer will be defective owing to threading dislocations.

The strain and thus the stress may be compensated for by codoping with germanium, which has a covalent radius (1.22 Å) larger than that of silicon and which is electrically inactive. Under the assumption that the total strain can be represented by a linear superposition of the individual strains caused by germanium and boron, the misfit f is derived to be (21):

$$f = 0.0425 N_{Ge} - 0.274 N_B \tag{6.12}$$

The strain is fully compensated for ($f = 0$) when the ratio of the two-dopant concentration in silicon reaches:

$$N_{Ge} : N_B = 6.45 \tag{6.13}$$

where N_B and N_{Ge} are atomic concentrations of B and Ge in silicon, respectively.

The following is an example of SOI preparation using device wafers with a B/Ge etch-stop layer (22). Wafers with an epitaxially grown B/Ge etch-stop layer and a nominally undoped silicon layer on top were bonded to an oxidized silicon wafer. Annealing at 650–800°C was performed. After grinding and polishing to remove most of the substrate from the epi-wafer, EDP was used to etch off the remaining 10–30 μm of the silicon substrate. The etch was stopped when a hole concentration of $\sim 8 \times 10^{19}$/cm^3 in the B/Ge layer was approached. The etch selectivity S_1 is about 100 at this stage. The B/Ge layer was then etched off by an 1-3-8 etch which has also an etch selectivity S_2 of about 100. Therefore, the final thickness variation of the device layer, Δt, is a factor of $S_1 \times S_2$ smaller than the original thickness variation of the silicon layer after grinding, Δt_0:

$$\Delta t = \frac{\Delta t_0}{S_1 \times S_2} \tag{6.14}$$

In this case, $S_1 \times S_2$ greater than 10,000 was obtained. The SOI layer obtained by the strain compensated etch-stop method shows thickness uniformity better than ± 100 Å and excellent smoothness of its surface. A

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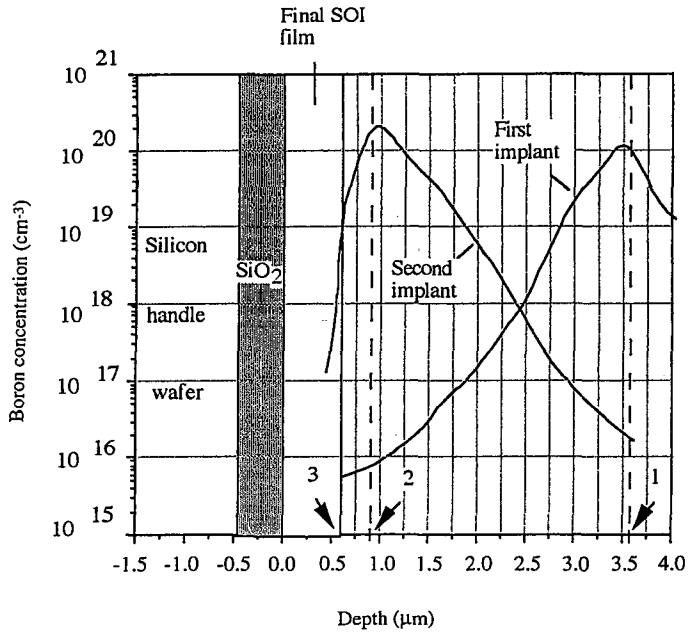

Fig. 6.16 Boron concentration profiles of the two MeV implants in a bonded silicon pair.

low-misfit dislocation density of ~ 1–$20/cm^2$ was achieved. The residual doping in the SOI film was below $5 \times 10^{16}/cm^3$ and excellent carrier lifetimes were measured in these films (22).

Another approach which does not require epitaxial growth for forming a device layer employs MeV boron implantation (23). For high-implant energies, the concentration profile of implanted boron becomes much sharper than in the case of low-energy implantation and the surface boron concentration is reduced. Fig. 6.16 shows the SIMS (secondary ion mass spectroscopy) profile of the boron implant with 6×10^{15} cm^{-2} at 2.5 MeV. In order to have a Si/thermal SiO_2 interface, the implanted wafer was slightly oxidized (250–500 Å oxide). After bonding of the boron-implanted wafer to an oxidized wafer and subsequent annealing (at as low a thermal budget as possible to avoid excess boron outdiffusion, e.g., 800°C, 10 min), the device wafer of the bonded pair was thinned by grinding and EDP etching to reach the etch-stop. The remaining silicon layer was 3.5 μm. The etch-stop was then removed by 1-3-8 etch followed by thermal oxidation and subsequent oxide stripping to further thin the SOI layer to a desired thickness. However, the multiple oxidations generated a substantial density of oxidation-induced stacking faults.

By another MeV boron implantation (6×10^{15} cm^{-2} at 1.6 MeV) into the remaining 3.5 μm, a second etch-stop was created, shown also in Fig. 6.16. The second etch was stopped at location 2 in Fig. 6.16 and the etch-stop was then removed by 1-3-8 etch at location 3 followed by a short wet oxidation and subsequent oxide stripping to thin the SOI layer to $\sim 0.5 \pm 0.004$ μm. Since the defective remaining tail of the second boron implant in the SOI layer was removed by the short oxidation step, a low-defect density was achieved.

*6.3.1.2 **Carbon-Implanted Etch-Stop*** Carbon is an electrically inactive, substitutionally dissolved impurity in silicon. Also, implanted carbon forms strong gettering sites in silicon and can act as sink for implantation-induced excess silicon self-interstitials and thus retard the formation of a dislocation loop (24). As discussed above, Si layers implanted with carbon at conventional energies (≤ 200 keV) and doses (1–3×10^{16} cm^{-2}) act as effective etch-stop layers. The etch-stop efficiency degrades with annealing temperature and virtually disappears at temperatures above 900°C (7). A carbon etch-stop was used for the fabrication of ultrathin SOI layers (25); 4-in., p-type, 5–10 Ωcm, CZ (Czochralski-grown) (100) silicon wafers were used. The wafers were implanted with a carbon dose of 3×10^{16} cm^{-2} at an energy of 190 keV. This implantation process retains 900-Å thick crystalline surface layer along with a deeper amorphous region containing a high carbon concentration. The SIMS measurements revealed that the peak carbon concentration was 1.3×10^{21} cm^{-3} and was located at 0.548 μm below the wafer surface (see Fig. 6.17). It was found that after annealing at 1100°C in argon for 1 h, the carbon concentration in the near-surface region ($\sim$ 913 Å thick) was reduced to below the detection limit of the SIMS measurements (see Fig. 6.17). This low carbon concentration region was termed a "carbon-denuded zone" (25).

The mechanism for the formation of the carbon-denuded zone is as follows: carbon diffuses from the region near the silicon surface into the originally high carbon concentration region where a high concentration of carbon precipitates has formed during the 1100°C annealing. The as-implanted material has a deeper buried amorphous layer, while the near-surface Si layer remains single crystalline. Therefore, after recrystallization at 1100°C, there is an abundance of low-energy carbon precipitate nucleation sites in the recrystallized region, since the Si crystal contains a high density of point defects. This factor, in addition to the high carbon supersaturation in the region, lead to rapid carbon precipitate nucleation and growth. In the near-surface layer, the carbon supersaturation is much lower and the material is crystalline in the first place, leading to a negligible carbon nucleation rate. As annealing time elapses, the supersaturated carbon in the deeper region will be depleted by carbon precipitate growth. Supersaturated carbon from the surface region will diffuse into the deeper region where the carbon atoms are incorporated in growing carbon precipitates.

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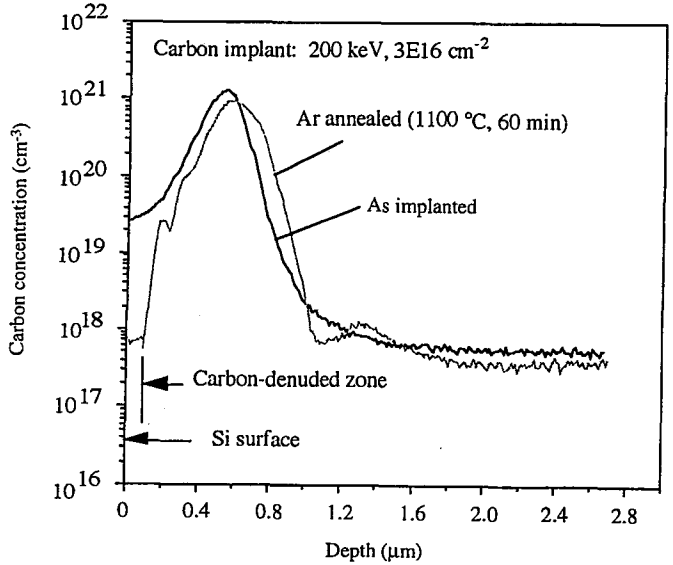

Fig. 6.17 SIMS profiles of carbon concentration in (100) silicon before and after annealing at 1100°C.

The carbon-implanted silicon wafer was bonded to an oxidized silicon wafer. Because of the degradation of the etch-stop efficiency of the carbon-implanted layer with temperature, the post-bonding annealing to increase the bonding strength was performed at 300°C for 42 h. The surface energy after annealing was found to be higher than 800 mJ/m^2 and was adequate for grinding and etching for removal of most of the silicon bulk of the device wafer* to leave the silicon layer with a thickness of 1.5 ± 0.5 μm. The wafer was then etched in EDP at 90°C, resulting in an SOI layer of 5275 ± 14 Å in thickness. Thermal oxidation was employed to oxidize about 4400 Å of silicon containing carbon precipitates. The thermally grown oxide was then removed by a dip in HF aqueous solution. The ultrathin (less than 900 Å) SOI layer with a thickness variation of ±50 Å was finally realized in which the carbon concentration was at or below the SIMS measurement limit.

6.3.1.3 Oxygen-Implanted Etch-Stop To exploit the excellent etch selectivity of silicon to silicon oxide in alkaline aqueous solutions, an oxygen-implanted layer in silicon has been employed as an etch-stop in preparations of SOI

*In the actual experiment, the grinding and polishing was bypassed by using a bonded SOI wafer with a silicon layer thickness of 1.5 ± 0.5 μm as a device wafer. The buried oxide was used as an etch-stop to simulate the grinding and polishing procedures. The outcome, namely a silicon layer of 1.5 ± 0.5 μm thickness containing the implanted carbon etch-stop, was the same as for a conventional grinding and polishing process.

materials. Commercially available SIMOX (Separation by IMplanted OXygen) wafers provide a BOX (Buried Oxide) layer as the etch-stop (26).

Standard SIMOX (oxygen dose of 1.8 × 10^{18} cm^{-2}, energy of 190 keV) can provide ultrathin uniform (0.23 ± 0.005 μm) SOI films in volume but suffers from high defect densities (> 1 × 10^5/cm^2), limited thickness of both SOI (0.03–0.5 μm unless followed by additional epitaxial growth) and BOX (0.05–0.6 μm) layers, limited process flexibility, and poor quality of BOX layers and their interfaces. Among them the most difficult and complicated problems are related to the BOX layer. The coalesced oxide from implanted oxygen appears to behave quite differently from thermal oxide. The BOX layer of SIMOX has silicon inclusions, conducting pipes and pinholes, charge traps and defects distributed through the BOX bulk as well as located at its interfaces, contaminations, low oxide breakdown voltage, and nonuniform thickness. The problems become worse for thinner BOX layers. However, the BOX layer is still adequate as an excellent etch-stop.

Transfer of commercially available SIMOX layers onto thermally oxidized Si wafers by SIMOX wafer bonding and etch-back with the BOX/SIMOX as an etch-stop layer can produce high-quality SOI, combining advantages of SIMOX and bonding technologies and avoiding some of their respective problems (26). In particular, the ability to process the thermal oxide on the handle wafer prior to bonding is very attractive for applications such as radiation-hard SOI materials.

With this technique, there is no problem associated with outdiffusion and degradation of etch-stop efficiency of the BOX layer, therefore, high-temperature (e.g., 1100°C) annealing can be done to strengthen the bond. To reduce the dislocation density in the SOI layer and lower the fabrication cost, low-dose SIMOX can be used (27). For example, oxygen implantation at an energy of 120 keV with a dose of 4 × 10^{17} cm^{-2} can form a continuous BOX of 800 Å thick and a 2150-Å SOI layer after 1320°C, 6 h annealing in a gas mixture of argon and oxygen. The dislocation density is reduced to less than 10^3 cm^{-2}. A comparison of the standard and typical low-dose SIMOX is listed in Table 6.3.

6.3.1.4 SiC Etch-Stop for Transfer of SiC Layers Single- or polycrystalline β-SiC (3C-SiC) layers can be produced on silicon substrates by chemical vapor deposition (28). The SiC is an inert material in silicon etchants;

TABLE 6.3 Comparison of Standard and Typical Low-Dose SIMOX

	Implant Energy (keV)	Implant Dose (cm^{-2})	Si Thickness (Å)	BOX Thickness (Å)	Dislocation Density (cm^{-2})
Standard SIMOX	190	1.8 × 10^{18}	2300	4000	> 1 × 10^5
Low dose SIMOX	120	4 × 10^{17}	2150	800	~ 10^3

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therefore, it can be transferred onto oxidized silicon or other desired substrates by bonding and etch-back using the surface device layer of SiC itself as an effective etch-stop (29). An example is as follows.

Silicon wafers covered with SiC are termed "SiC/Si wafers." After standard RCA cleaning, the SiC/Si wafers were oxidized at 1050°C in dry oxygen to grow 250–1000 Å oxide on the SiC layers. To enhance the hydrophilicity of mating wafer surfaces, both the oxidized SiC/Si wafers and the oxidized handle Si wafers were boiled in nitric acid at 100°C for 10 min and rinsed in deionized water. The oxidized SiC/Si wafers were then bonded at room temperature to Si wafers covered with 1 μm thermal oxide.

Atomic force microscope (AFM) measurements have shown that the mean surface roughness (R_a) of the SiC layer covered with 500 Å oxide is about 23 Å and is much higher than the maximum value of ~ 5 Å required for bubble-free spontaneous room-temperature bonding. The maximum peak-to-valley value of the SiC surface roughness is about 226 Å. It has been found that even with the mating oxidized Si surface with an R_a of 1.5 Å, the wafers require external force in order to bond at room temperature. A Teflon bar was used to press the back side of the room temperature contacted pairs together to allow bonding to occur.

The bonded wafers were then annealed in air at 900°C for 2 h. After annealing the wafer pairs were lapped to remove silicon oxide (and some SiC) from the back of the silicon substrate with the SiC layer. Finally, the silicon substrate of the SiC layer was etched in 13.5% KOH at 75°C for ~ 12 h while the oxidized Si wafer was protected by 1 μm oxide from KOH etching. The etching was stopped when the SiC layer was reached and the SiC layer was transferred onto the oxidized wafers.

6.3.1.5 Porous Silicon Etch-Release Layer This method makes use of the possibility of epitaxial growth of a single crystalline silicon layer on top of a porous silicon surface and the high etch selectivity between the porous and the epitaxial silicon layers in a $HF—H_2O_2—H_2O$ solution (30). The process flow is schematically shown in Fig. 6.18.

In a solution of HF (49%):C_2H_5OH (100%) = 2:1 at 7 mA/cm^2, a p-type silicon (100) wafer with a resistivity of 0.01–0.02 Ωcm was anodized to form a ~ 12-μm thick porous silicon layer on the surfaces. After oxidizing the porous silicon in O_2 at 400°C for 1 h to passivate the pore walls and removing the oxide from the surface, a ~ 0.5-μm thick single-crystalline silicon layer was epitaxially grown on the porous surface with a mixture of SiH_2Cl_2 and H_2 at 900°C and 80 Torr. This device wafer was thermally oxidized to grow 1000 Å oxide and was bonded to an oxidized handle silicon wafer covered with 5000 Å oxide (Fig. 6.18*a*). After annealing at 800°C for 2 h in N_2, the device wafer was thinned by grinding to expose the porous silicon on the entire wafer surface. Finally, the porous silicon layer was selectively etched off by HF (49%):H_2O_2 (30%) = 1:5 solution (Fig. 6.18*b*). The etch selectivity of porous silicon to bulk silicon was ~ 10,000 in the solution. The extremely

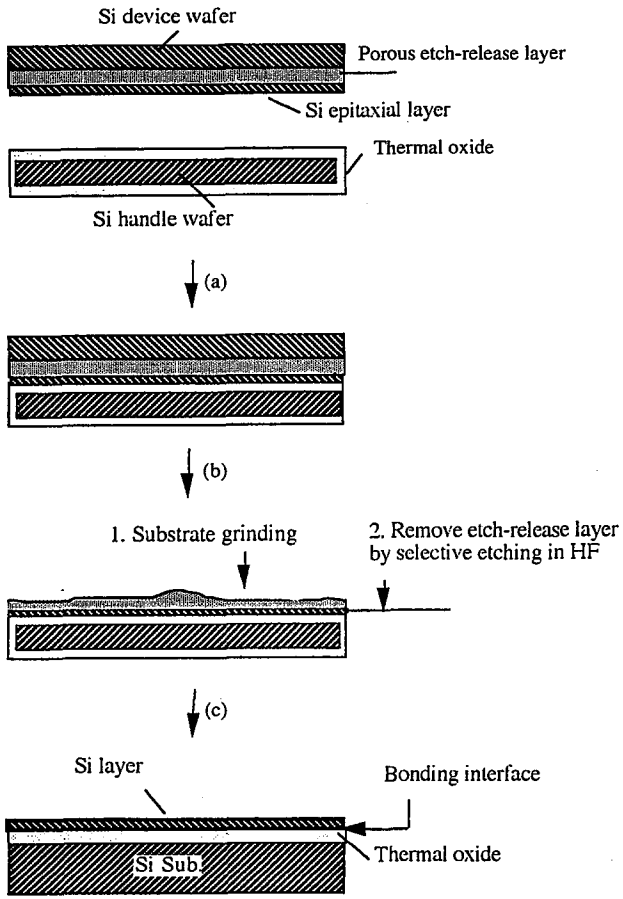

Fig. 6.18 Schematic BESOI process using a porous silicon etch-release layer in the device wafer of a bonded silicon pair. (*a*) Bonding and annealing; (*b*) grind and etch-back; (*c*) layer transferred.

high etch selectivity leads to variation in thickness of the transferred silicon layer of about 280 Å using this one etch-stop method (Fig. 6.18*c*). This method can also be used to transfer epitaxial silicon layers onto other desired substrates.

6.3.2 Layer Transfer by Bonding and Layer Splitting

Recently, another layer-transfer technology was reported (4). The basic process flow, as already shown in Fig. 1.6 of Chapter 1, is reproduced for convenience in Fig. 6.19. The first step (Fig. 6.19*a*) is to implant hydrogen

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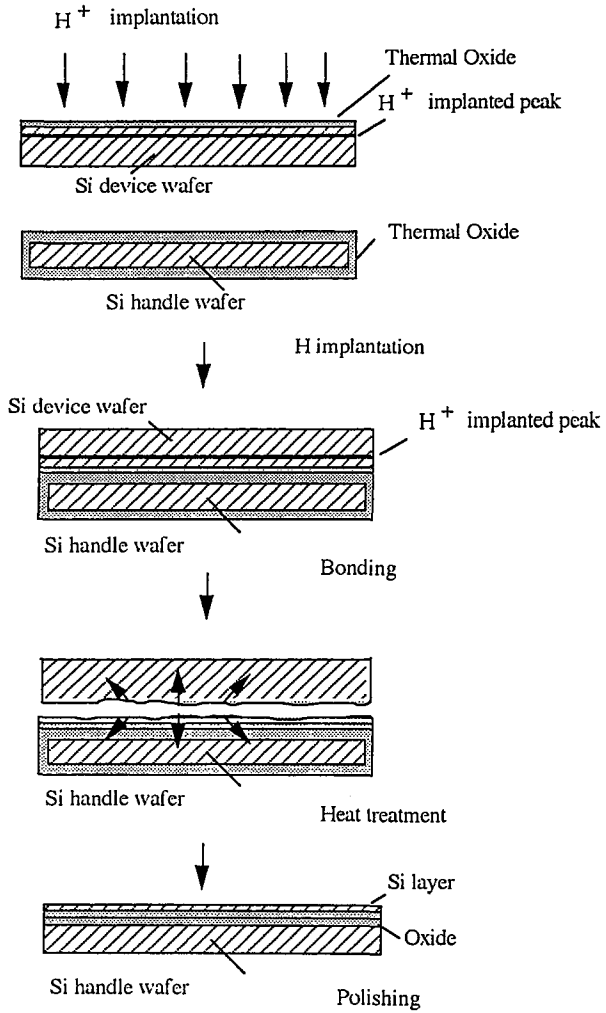

Fig. 6.19 Schematic of layer-transfer process by bonding and layer splitting.

ions into the device silicon wafer. Typical implantation doses are 3.5×10^{16} to 1×10^{17} cm^{-2}. The implant energy is determined by the required final device layer thickness. The thickness depends only on the implant energy with about 90 Å/keV in silicon and silicon oxide. Table 6.4 lists the thickness of the device layer as a function of the hydrogen ion implant energy (31).

To obtain a high-quality Si/SiO_2 interface in the final SOI structure, the device wafer is thermally oxidized before implantation. The implanted device

TABLE 6.4 Relationship of the Device Layer Thickness and the Hydrogen Ion Implant Energy

H^+ Implant Energy (keV)	10	50	100	150	200	500	1000
Device layer thickness (μm)	0.1	0.5	0.9	1.2	1.6	4.7	13.5

wafer and a handle silicon wafer with or without oxide are cleaned in modified RCA solutions and the surfaces of both wafers become hydrophilic. The wafers are then bonded at room temperature (Fig. 6.19*b*). The bonded pair is first annealed at a low temperature ranging from, for example, ~150 to ~400°C to enhance the bond strength, followed by a higher temperature anneal (typically at around 500°C) to split the hydrogen-implanted Si layer from the device wafer.

During implantation, hydrogen ions collide with the host atoms to generate displacement damage (denoted as X) in the form of vacancies and interstitials (Frenkel pairs) and their agglomerates. In addition to generating displacement defects, the implanted hydrogen atoms can interact with the existing defects created by previously implanted hydrogen ions to form hydrogen complexes (X-H). In addition to X-H complexes, platelets (which are separated, H-terminated adjacent crystalline planes over a finite area) on (100) and (111) planes are formed. Platelets are believed to result from a supersaturation of hydrogen and hydrogen passivation of broken Si–Si bonds (32). Platelets are essential because they are likely to act as nucleation sites for microcrack formation when hydrogen atoms diffuse into the platelets to form molecular hydrogen gas. The driving force for this process is the 1.6 eV gained in H_2 molecule formation from two dissociated neutral interstitial hydrogen atoms in a silicon crystal. Also, 0.78 eV are gained by H_2 gas formation from H_2 in Si solid solution (32). During annealing, some trapped hydrogen will dissociate from X-H complexes and diffuse into the platelets forming H_2 molecules, leading to an increase of the internal pressure and formation of microcracks. After annealing for a sufficiently long time, the hydrogen-implanted layer bonded to the handle wafer is split off from the device wafer around the mean hydrogen ion penetration depth during the annealing (Fig. 6.19*c*). The remaining device wafer can be recycled for use as a handle wafer. During another thermal treatment at 1100°C, the bonding strength between the transferred silicon layer and the handle wafer is further enhanced, and the residue of the implanted hydrogen and related defects are almost totally removed. Figure 6.20 is a cross-sectional TEM picture of a microcrack in hydrogen-implanted, oxidized silicon (not bonded) after annealing at 375°C.

Because the mean surface microroughness of the split silicon layer surfaces is in the range of 100 to 120 Å, a final light CMP polishing is necessary to remove a few hundred angstroms from the top surface, resulting in a

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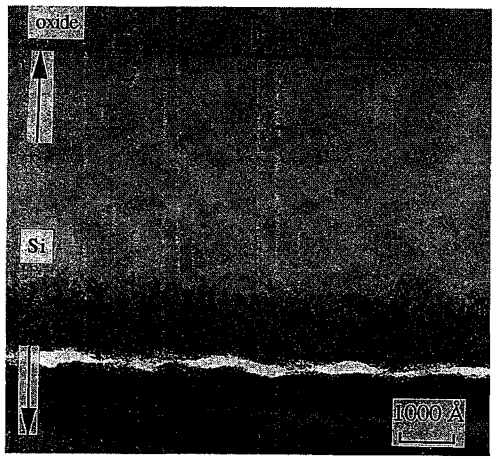

Fig. 6.20 Cross-sectional TEM picture of a microcrack in hydrogen-implanted, oxidized silicon (not bonded) after annealing at 375°C.

smooth surface with a mean surface microroughness of < 1.5 Å and with a thickness variation of ~ 100 Å (Fig. 6.19*d*).

The growth of the microcracks that causes blistering and splitting is probably due to the combined effects of increased internal pressure (33), thermal energy (34), and chemical reaction (35) between hydrogen and the Si—Si bonds. On H-implanted unbonded silicon wafers, hydrogen-induced, optically detectable surface blisters form during annealing at elevated temperatures. Figure 6.21 is an IR transmission picture of blisters on hydrogen-

Fig. 6.21 Infrared transmission picture of blisters on hydrogen-implanted silicon after annealing (magnification: × 200).

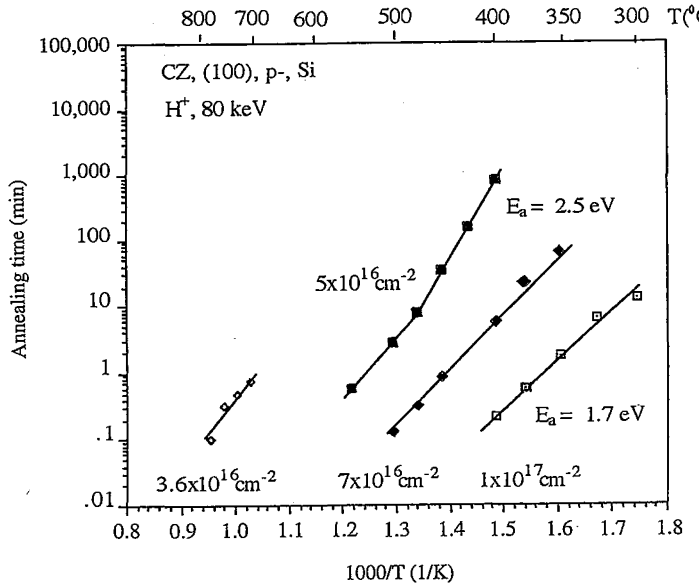

Fig. 6.22 Time required to form optically detectable surface blisters in hydrogen-implanted Si with various hydrogen doses as a function of annealing temperature.

implanted silicon after annealing. Since the times required to form hydrogen-induced optically detectable blisters are a measure of the required splitting time (36), the blistering times on the H-implanted unbonded silicon wafers with various hydrogen doses were determined at various temperatures, as shown in Fig. 6.22.

If the internal pressure dominates the splitting process, the following reaction may be responsible: the internal pressure causes the edge of the microcracks to open slightly where Si—Si bonds are broken, which react with H_2 molecules to form Si—H, that is,

$$2\text{Si}— + \text{H}_2 \longrightarrow 2(\text{Si}—\text{H}) \qquad (6.15)$$

In order to grow, the internal pressure in the microcracks must be kept constant when their volume expands. This implies that H release from the trapped sites or H diffusion into the microcracks would be the rate-limiting step. However, the effective activation energy derived from Fig. 6.22 is about ~ 1.7 eV, which is close to the Si—Si bond energy of 1.9 eV, indicating that Si—Si bond breaking may be the rate-limiting step.

The Si—Si bonds at the edges of the microcracks are highly strained owing to the high internal pressure and therefore have much higher chemical reactivity than strain-free bonds. The H atoms released from their traps

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diffuse into the microcracks. In addition to forming H_2 molecules, at the edges of the microcracks the H atoms are likely to react with the strained Si—Si bonds to form Si—H:

$$\text{Si—Si} + 2\text{H} \xrightarrow{K_h} 2(\text{Si—H}) \tag{6.16}$$

where K_h is a reaction rate constant. We can calculate the time (t) dependence of reaction (6.16) by solving the following equation for the radius R of the microcracks:

$$\frac{dR}{dt} \approx K_h C_H \tag{6.17}$$

$$K_h = K_h^o \exp(-E_a/k_B T) \tag{6.18}$$

where C_H is the concentration of hydrogen in the microcracks, k_B is the Boltzmann constant, and T is the absolute temperature. As long as C_H does not yet change appreciably, Eq. (6.17) has the solution

$$R \approx K_h^o \exp(-E_a/k_B T) C_H t \tag{6.19}$$

To generate an optically detectable blister, the radius of the microcrack should reach a certain size R_{det} (which is assumed to be independent of temperature). For different temperatures this leads to different times required to detect bubbles t_{det}, given by

$$t_{det} \propto \frac{1}{C_H} \exp(E_a/k_B T) \tag{6.20}$$

Equation (6.20) holds only if C_H is sufficiently large to reach R_{det} without being depleted. The activation energy, E_a, is the Si—Si bond-breaking energy from the interaction with H atoms. The activation energy of ~ 1.7 eV derived from the results shown in Fig. 6.22 supports the argument that among hydrogen dissociation, hydrogen diffusion, and the Si—Si bond breaking involved in the blistering process, Si—Si bond breaking is the rate-limiting step over the temperature range in Fig. 6.22. Hydrogen-implantation-induced layer splitting works not only for silicon but also for germanium, diamond, and SiC (36).

Silicon on oxidized silicon (SOI), silicon on glass (37) and silicon carbide on glass (38) or on oxidized silicon (39) have been realized by the bonding and layer-splitting method. However, except in the cases above in which only a small difference in the thermal expansion coefficients between the silicon and the respective substrates is present, other material combinations usually suffer from excessive thermal stresses due to thermal mismatch between the silicon and the dissimilar substrate during annealing for layer splitting. For

example, single-crystalline silicon on quartz is an interesting material combination for high-resolution, flat-panel displays. However, at room temperature, the thermal expansion coefficient of fused quartz is only 0.5×10^{-6}/°C while that of silicon is 2.56×10^{-6}/°C. A bonded 4-in. standard Si/quartz pair (both of ~ 525 μm in thickness) will therefore crack if the temperature considerably exceeds 200°C. Since the splitting temperature of silicon in the process above is typically around 500°C, the process is virtually not applicable for realizing layer transfer onto dissimilar substrates which exhibit a large difference in thermal expansion coefficients.

Recently, a low-temperature silicon layer-splitting technology was developed (40). It was found that for a given annealing time, the splitting or blistering temperature in H-implanted silicon decreases with boron (B) doping concentration in silicon. The blistering times for H-implanted silicon wafers uniformly doped with various B concentrations as a function of temperature are shown in Fig. 6.23. N-type silicon with phosphorous (P) doping concentration of $1-5 \times 10^{18}$ cm^{-3} does not show the same effect, as can also be seen in Fig. 6.23.

Since most device applications require lightly doped Si layers, the B-doping effect has to be realized by B implantation followed by a depth-aligned H

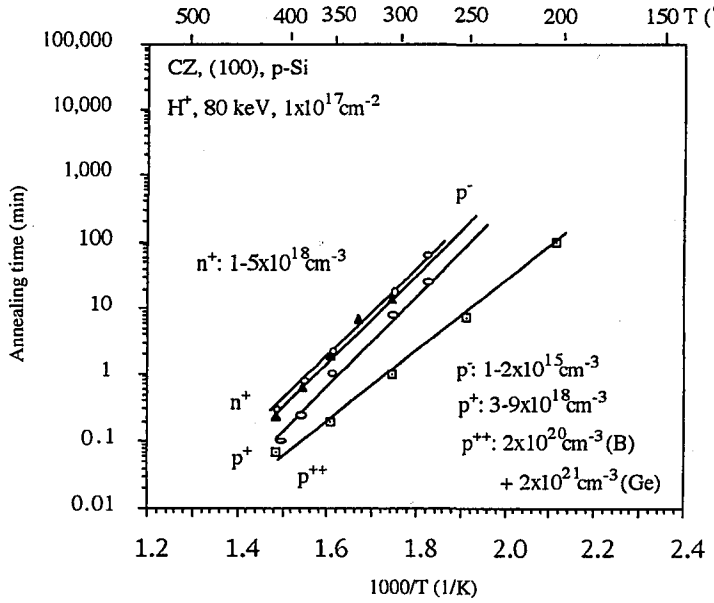

Fig. 6.23 Time required to form H implantation-induced optically detectable surface blisters on hydrogen-implanted, uniformly doped Si wafers (with phosphorous or boron concentrations as indicated) as a function of annealing temperature.

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implantation. After splitting, the boron concentration in the transferred silicon layer can be reduced to a normal level by a thermal oxidation and/or a light polishing step. Silicon wafers were first implanted at room temperature by B^+ with 5.0×10^{12} to 5.0×10^{15} ions/cm^2 at 180 keV, and subsequently implanted by H_2^+ with 5.0×10^{16} ions/cm^2 at an energy which locates the H-peak concentration in the silicon wafers at the same position as that of the implanted boron peak. Compared to the H-only implanted samples, the temperature for the B + H coimplanted silicon layer to split from its substrate after wafer bonding during a heat treatment for a given time is reduced significantly. Surprisingly, when the thermal treatment to electrically activate the implanted B atoms had NOT been performed, a much greater reduction of the temperature required to form optically detectable surface blisters for a given annealing time (termed blistering temperature) was observed, even at a B dose as low as 5×10^{12} ions/cm^2 (see Fig. 6.24). It is speculated that, in addition to generating a high number of point defects per implanted B ion, which are strong gettering sites for hydrogen, B atoms themselves may trap a cluster of hydrogen atoms. Both processes are likely to assist platelet nucleation and microcrack growth.

For a further reduction of the splitting temperature, preannealing of the unbonded B + H coimplanted silicon wafers was performed at a higher temperature (e.g., 250°C) than the splitting temperature (e.g., 200°C) without

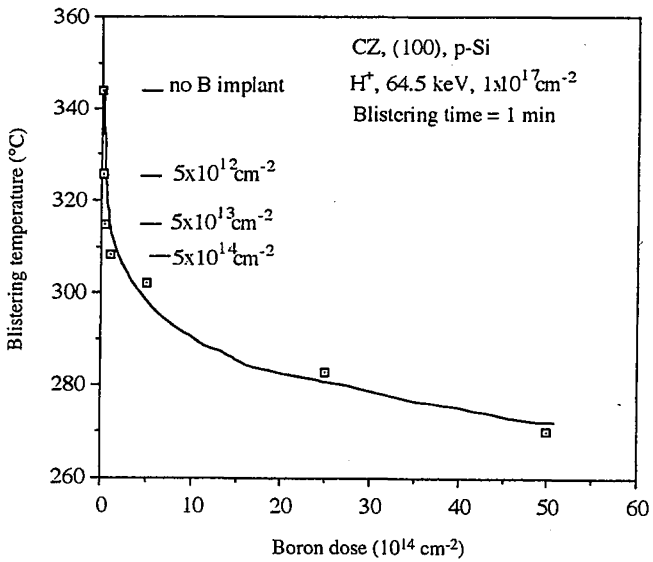

Fig. 6.24 Temperature required to form optically detectable surface blisters in hydrogen-implanted silicon for a fixed annealing time of 1 min as a function of dose of boron implanted before the hydrogen implantation.

generation of optically detectable blisters on the silicon surface. The time needed at 200°C for the generation of optically detectable surface blisters on the preannealed (10 min) samples is only ~10% of that required by silicon wafers without the preannealing. Combining these two effects allows the transfer of a silicon layer from a silicon wafer onto a severely thermally mismatched substrate such as quartz and sapphire at a temperature as low as 200°C.

Recently, transfer of a 3-in. GaAs layer on an oxide-covered silicon substrate was realized by hydrogen implantation and layer splitting (41). The GaAs wafers were 3-in. in diameter, (100) and semiinsulating, covered by a submicron-thick PECVD SiO_2 layer, and implanted by hydrogen (H^+) at 100 keV with a dose in the 5.0×10^{16} ions/cm^2 to 1.0×10^{17} ions/cm^2 range. The PECVD oxide layer was polished to achieve a smoothness suitable for bonding. After cleaning, both GaAs and Si wafers have a hydrophilic surface and were bonded at room temperature. The bonding energy was about 250 mJ/m^2 and was increased to about 900 mJ/m^2 after annealing at 350°C for 0.5 h. Splitting of the hydrogen-implanted GaAs layer of 0.8 μm thick from the GaAs wafer onto the silicon substrate took place during a thermal treatment at 400–700°C. The split surface showed a RMS roughness of about 150 Å. A final polishing was performed to smooth the split surface. It is not clear how thermal stress problems related to the severe thermal mismatch between GaAs and silicon (thermal expansion coefficient of GaAs is 6.8×10^{-6}/°C while that of silicon is 2.56×10^{-6}/°C) were circumvented during the splitting process.

6.3.3 Layer Transfer by Bonding and Lateral Etching

The etch selectivity of the AlAs layer to $Al_xGa_{1-x}As$ film is as high as 10^8 (for $x \leq 0.4$) in a 10% aqueous HF solution. This extremely high etch selectivity has been employed to release an epitaxial film from its growth substrate by undercutting an AlAs layer (42).

The typical process is schematically shown in Fig. 6.25. A multilayer $Al_xGa_{1-x}As$ film was epitaxially grown on an AlAs layer on a GaAs substrate. The AlAs release layer is lattice matched to GaAs and typically 500 Å thick. A black wax (Apiezon W) was applied to the epitaxial film, which is a strip with a width less than 20 mm, by melting a pellet onto its surface at 125°C and flattening it to a thickness of 0.1–0.5 mm by pressing at 75°C. After removing the wax from the edges of the buried AlAs layer, the sample was immersed in a 10% aqueous HF solution at 0°C (Fig. 6.25*a*). The epitaxial film was undercut and released completely from its substrate by lateral etching of the AlAs layer. After rinsing in DI water, the wet epitaxial film was then placed on a desired substrate which was treated to be hydrophilic. After squeezing out the excess water from the bonding interface, the remaining water escaped to the edges by Poiseuille flow and the gap between the film and the substrate decreased until short-range van der Waals

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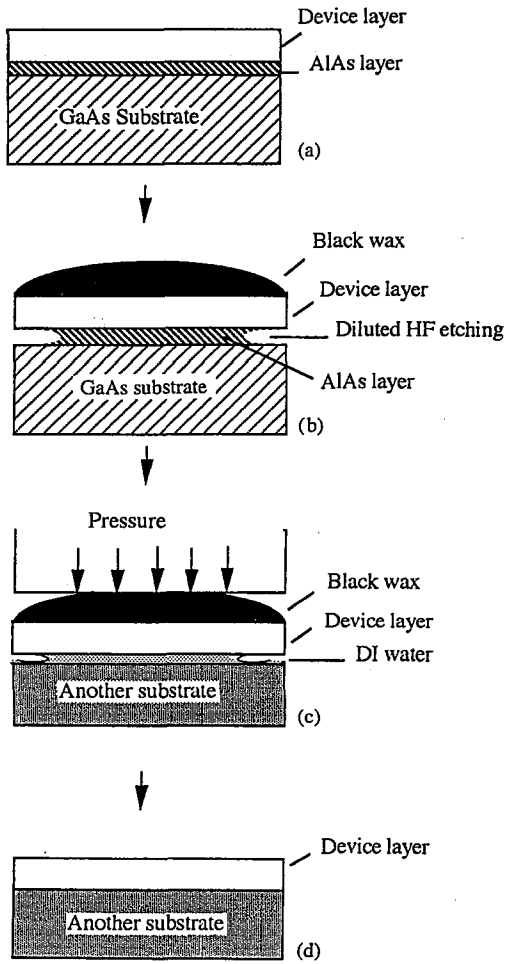

Fig. 6.25 Schematic of layer-transfer process by bonding and lateral etching. (*a*) Epitaxial structure; (*b*) lateral etching and lift-off; (*c*) water bonding; (*d*) wax removal and drying.

forces and hydrogen bridge bonds hold the two pieces together (Fig. 6.25*b*). The wax was then removed by rinsing in trichloroethylene, leaving the epitaxial film bonded to the substrate.

As long as the film–substrate interfacial energy $2\gamma_{fs}$ is less than the sum of the substrate–water (γ_{sw}) and the water–film (γ_{wf}) surface energies, the water will tend to be forced out as the film and substrate surfaces coalesce together:

$$2\gamma_{fs} < \gamma_{sw} + \gamma_{wf} \tag{6.21}$$

Only relatively narrow strips (<20 mm) of epitaxial films have been transferred to new substrates with more favorable properties than the growth substrates. The main reason is the difficulty of the gas product of the undercut etching reaction to diffuse through the extremely narrow gap. The etch rate decreases drastically as the strips get wider. It is conceivable that an entire epitaxial film on a substrate wafer may be transferred by bonding and lateral etching of a release layer with the help of thermal mismatch stresses between the new substrate of the film and the growth substrate, causing the corners of the epitaxial film to lift up during undercutting. Alternatively, a method has been developed in which a system of sufficiently densely spaced grooves allows lateral access for the etching solution so that layers over whole wafers can be transferred in the form of many small areas separated by the grooves (43).

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7

Electrical Properties of Bonding Interfaces

The interface of bonded silicon wafers is generally not perfect even though the common contaminants may have been removed from the surfaces prior to initial bonding. In addition to the difficulty of fabricating two surfaces of exactly the same surface orientation and then aligning them properly during the initial bonding (which prevents defect-free interfaces in the case of hydrophobic bonding), the bonding surfaces, whether hydrophobic or hydrophilic, normally adsorb species other than silicon atoms when bonding is carried out in any ambient. For hydrophilic silicon surfaces prepared by a wet chemical hydrophilization treatment, OH groups and water molecules are the main terminating species on the native oxide-covered surfaces. For hydrophobic silicon wafers which are HF dipped without DI water rinse, Si—H and Si—F are the dominant species present on the surfaces. As discussed in Chapter 12, both hydrophilic and hydrophobic bonding interfaces are gettering sites for metallic impurities. In practice, it was also found that removal of boron contamination from HF-dipped silicon surfaces needs special attention.

Typically, the bonding interface of wafer pairs is commonly not included in active regions of the devices fabricated in the bonded materials, and it functions usually only as part of a mechanical support. However, the electronic properties of the bonding interface can still influence the performance of the devices, effecting their on-resistance or their thermal conductivity, for example. This chapter describes the electronic properties of bonding interfaces and the possible influence of these interfaces on the performance of devices fabricated on bonded materials.

7.1 ELECTRICAL PROPERTIES OF INTERFACES IN BONDED HYDROPHILIC AND HYDROPHOBIC Si/Si WAFERS

7.1.1 Charges in Bonded Si/Si Interface Region

Room-temperature bonded hydrophilic wafer pairs show a non-ohmic behavior in a current versus voltage (I-V) measurement in which a voltage is

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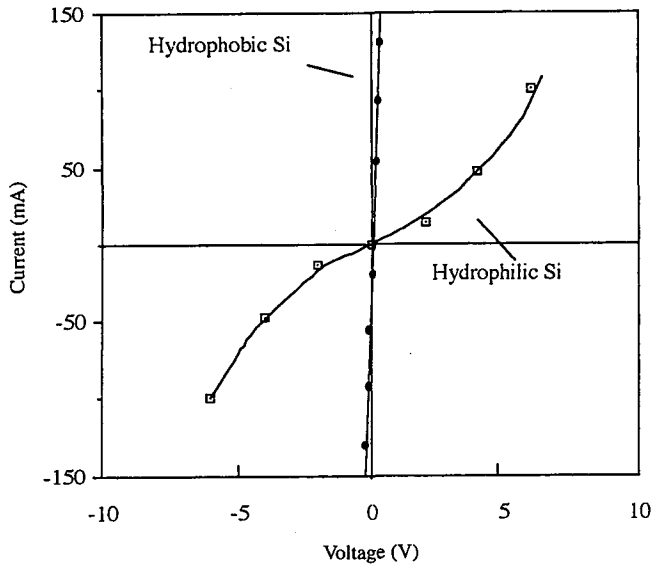

Fig. 7.1 Two typical I-V curves for 1-cm^2 samples cut from 0.1 Ωcm n-type silicon wafer pairs after room-temperature bonding.

applied across the bonded pair and a current passes through the bonded interface. The differential resistance of a room-temperature bonded sample of 1 cm^2 is high and ranges from 60 to 2000 Ω depending on the initial wafer resistivity. However, the influence of a bonded interface of hydrophobic wafers on current transport is significantly lower. A low differential resistance ranging from 0–5 Ω, depending on initial wafer resistivity, and linear I-V characteristics have been observed for the hydrophobic case. Figure 7.1 shows two typical I-V curves after room temperature bonding for 1 cm^2 samples cut from wafer pairs bonded with 0.1 ohmcm n-type silicon wafers (1).

After annealing at 1000°C for 1.5 h, the differential resistance of hydrophilic wafer pairs is drastically reduced to 3–140 Ω and ~1100°C annealing can bring it close to zero (1, 2). For hydrophobic wafer pairs, the differential resistance is always negligibly small after the heat treatment. These phenomena can be understood as follows.

The interface layer in bonded hydrophilic silicon pairs consists of the native oxide layers (the thickness is usually in the range of 10 to 45 Å thick; Fig. 5.19 shows a cross-sectional TEM of a bonded hydrophilic silicon pair) and the possible contaminants from the two bonding surfaces. Similar to the silicon-thermal oxide system (3), charges exist in the interface region of bonded hydrophilic silicon pairs. These charges are shown in Fig. 7.2. The

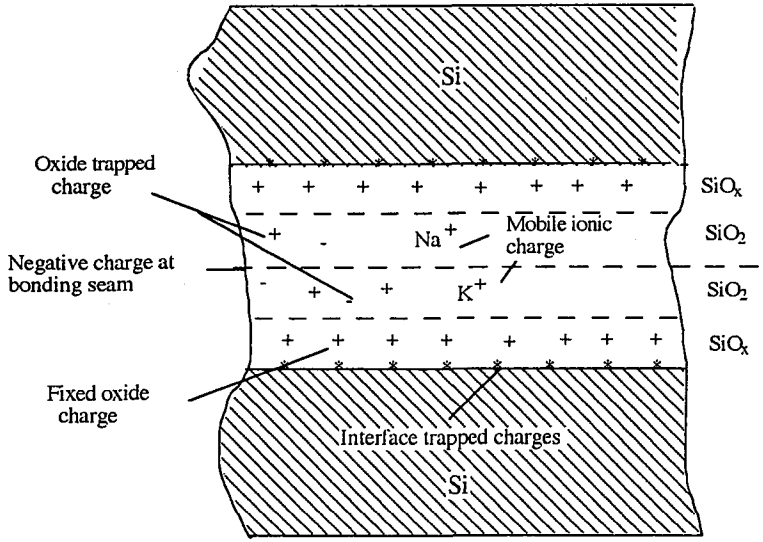

Fig. 7.2 Oxide charges in bonded hydrophilic silicon pairs.

fixed oxide charge in the nonstoichiometric native oxide is believed to be due to unfilled silicon bonds resulting from incomplete oxidation. The interface amorphous layer in a bonded hydrophilic silicon pair after 1100°C annealing for 2 h in nitrogen has been identified as SiO_x ($x = 0.2$–0.3) (4). It can be expected that the fixed-oxide charge density is higher in the interfaces between the interface layer and the two silicon substrates compared to that of thermal oxide/Si interfaces. The termination of the silicon crystal at the interface, the possible misorientation of the bonding wafers, and the impurities trapped and gettered at the bonding interface all result in extra allowed energy states confined to the region very close to the interface. Carriers can be trapped at these interface states of density N_{it} (traps/cm^{-2}). The interface states are distributed with density D_{it} (traps/cm^{-2} eV^{-1}) within the forbidden gap energies.

Assuming that the thin interface oxide layer itself does not present a barrier to the carriers, which can tunnel through it without noticeable restriction, the interface resistance of bonded hydrophilic silicon wafers appears to be caused by the presence of an interface potential barrier resulting from the interface charges. Figure 7.3 is the energy diagram of a bonded n/n silicon pair (1). At thermal equilibrium, the Fermi level is constant throughout the system. Near the bonded interface, the energy states below the Fermi level are filled by electrons, resulting in an energy barrier, qV_0, for free electrons in the conduction band (Fig. 7.3*a*). When a bias, V, is applied, the Fermi levels on the two sides are separated by an energy of qV

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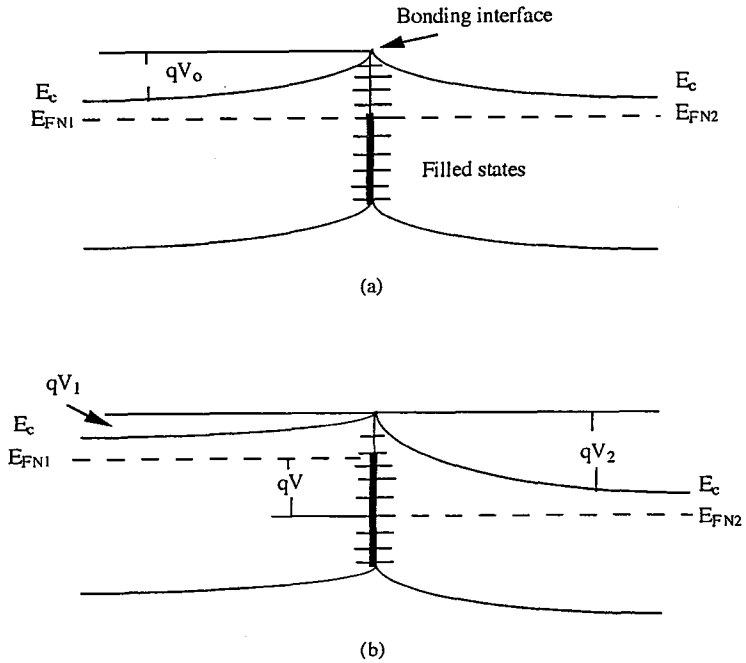

Fig. 7.3 Energy band diagram of a bonded n/n pair (*a*) at thermal equilibrium and (*b*) with an applied voltage V.

corresponding to a nonequilibrium case. The energy barrier for electrons in the conduction band of the negatively biased n-silicon side is reduced to qV_1, leading to a flow of electrons (majority carriers) across the interface. Similarly, on the positively biased n-silicon side, the energy barrier for electrons is increased to qV_2 (Fig. 7.3*b*). As majority carriers, the electrons are supplied to replace recombining electrons at the interface traps by flowing from the negatively biased n-silicon side in picoseconds. On the other hand, the holes are created by thermal emission in the space-charge region on the positive side, a process that takes milliseconds. Therefore, the interface traps between E_{FN1} and E_{FN2} are filled, resulting in an increase of negative charge which counteracts the decrease of the energy barrier. The current density, i, across the interface is limited by thermionic emission over the potential barrier V_1 and can be expressed as (5)

$$i = A^* T^2 \exp(E_{FN1}/kT)\exp(qV_1/kT)[1 - \exp(-qV/kT)] \quad (7.1)$$

$$V = \left(\frac{Q_s}{(2\varepsilon\varepsilon_0 qN)^{1/2}} - V_1^{1/2} \right)^2 - V_1 \quad (7.2)$$

where A^* is the Richardson constant, N is the doping concentration of the silicon of both sides of the structure, Q_s is the interface charge density, and the silicon dielectric constant is ε. As illustrated in Fig. 7.1, compared to hydrophobic bonded samples, wafers bonded with hydrophilic surfaces exhibit a higher resistance owing to higher charge-carrier trap concentrations at the interface and higher interface potential barriers.

Assuming that trapping of electrons is the only source of the change in Q_s during an applied voltage change, the interface state density D_{it} can be obtained from dQ_s/dV_1. By measurement of the response of current to a step voltage, interface state densities of a bonded hydrophilic 50-Ωcm wafer pair after 1000°C, 2 h annealing were found to be in the range of 5×10^{10}–10^{12} $cm^{-2}\,eV^{-1}$. The interface state densities of bonded hydrophobic samples are supposed to be lower, but so far no quantitative data are available.

As discussed in Chapter 5, with a relative rotational misorientation of the crystal axes of less than a critical angle (1°–5°) and after 1000–1200°C annealing for a few hours, the interface oxide layer of bonded hydrophilic silicon wafers is disintegrated, resulting in randomly distributed oxide islands. Between the thin oxide islands, which are typically 500–1000 Å in diameter, the silicon of the two bonded wafers is grown together like that of hydrophobic wafers. This observation explains the drastically reduced interface resistance after high-temperature annealing. When the angles of misorientation are larger, or when the annealing temperatures are below 900°C, the interface native oxide layer does not break up and, therefore, tunneling may limit the current (6).

7.1.2 Boron Contamination at Bonding Interfaces

An interface potential barrier can also be caused by boron contamination on the bonding surfaces prior to bonding (7). The interface boron leads to a p-type layer near the interface of bonded n-type wafers and results in an increase of the spreading resistance there. On the other hand, it gives rise to a decrease of the spreading resistance near the interface of bonded p-type pairs.

The interface boron is chemically adsorbed on the silicon wafer surfaces prior to bonding and is attributed to the boric oxide (B_2O_3) contamination from cleanroom air (8) which passes through hepa-filters:

$$B_2O_3 + SiO_2 \longrightarrow 2B + 3SiO \quad (7.3)$$

Pyrex glass viewports in cleanrooms have been identified as another possible source of boron. Exposure of silicon wafers to a cleanroom environment for 15 min is reported to result in boron contamination on silicon surfaces larger than $10^{12}/cm^2$. Typically, wafers are bonded immediately after cleaning; thus, a boron layer of 5 Å with a dose of $1 \times 10^{11}/cm^2$ can be assumed (9).

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The amount of adsorbed boron per unit surface area is about three times higher for native oxide covered silicon surfaces compared to thermally oxidized silicon surfaces. The adsorbed surface boron can desorb during the high-temperature process steps of conventional device fabrication. In contrast, in the case of wafer bonding, the boron is trapped at the bonding interface and diffuses into the bulk silicon. If wafers are kept wet after cleaning, the boron in the water can be removed by a subsequent rinse. Therefore, when wafers are bonded in water, or remain wet after RCA1 cleaning and DI water rinse followed by room-temperature bonding using the microclean room setup described in Chapter 4, the bonding surfaces will not be exposed to the cleanroom air, resulting in a drastically reduced interface boron concentration. It is also possible to avoid boron contamination by using a hydrophobic clean before bonding the wafers (10). This result indicates that the native oxide layer adsorbs significant amounts of boron.

7.1.3 Recombination Centers at Bonded Interface

As mentioned above, the bonding interfaces of wafer pairs are not usually included in active regions of devices fabricated from bonded materials. The bonded handle wafer commonly functions only as a mechanical support in the pair. However, in some power-device structures, the bonded interface is embedded in a region where minority carriers play an important role in the device performance.

In some power devices the bonded interface is located in the lightly doped side of a pn junction. An example (11) of the cross-sectional structure and the impurity profile is shown in Fig. 7.4. To obtain both mechanically and

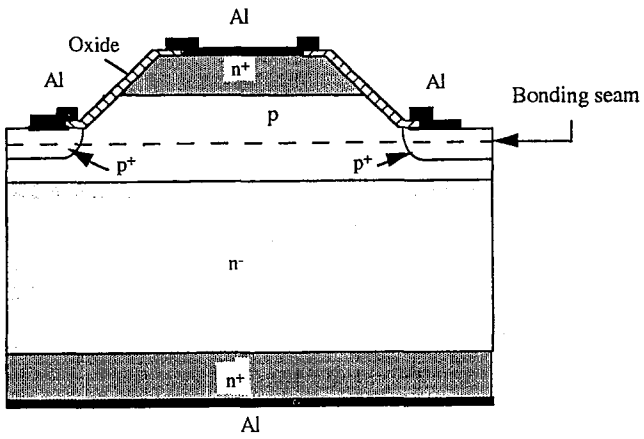

Fig. 7.4 Cross-sectional structure and the impurity profile of a bonded npn power device.

electrically stable bonded interfaces, hydrophilic bonding was performed with a subsequent annealing at 1200°C. The bonded interface was located in the p-base of the 4-kV high-voltage npn transistor. The distance W_{be} between the bonded interface and the emitter junction ranged from 6 to 14 μm and was adjusted by a lapping procedure. A common-emitter current gain I_c/I_b of 10 was achieved for the transistor at $W_{be} = 6$ μm. The loss of carriers to recombination in the base region α can be calculated to be less than 10% by

$$I_c/I_b = \alpha/(1 - \alpha) \tag{7.4}$$

The minority carrier lifetime, τ, in the base region was estimated from the change of α as a function of W_{be}. When the p-base region was doped to a concentration of $1 \times 10^{16}/\text{cm}^3$, τ was about 0.5 to 1 μs, corresponding to 10% of that of the p-base region without a bonded interface. It is believed that the recombination centers in the defective bonded interface region play a critical role in shortening the carrier lifetime.

The effect of carrier lifetime reduction by bonded interfaces can be employed beneficially for switching time control in power devices. When a bonded interface is placed inside an emitter region, the carrier injection can be controlled by adjusting the interface position with respect to the emitter/base junction (11).

7.2 ELECTRICAL PROPERTIES OF BONDED Si/SiO$_2$ AND SiO$_2$/SiO$_2$ BONDING INTERFACES

7.2.1 Charges in Bonded Si/SiO$_2$ Interface Region

The electrical properties of bonded Si/SiO$_2$ interfaces can be evaluated by using capacitance–voltage (C-V) measurements (1, 11) on MOS capacitors. After high-temperature annealing of bonded bare silicon/thermally oxidized silicon pairs, the bulk of the silicon substrate is removed by a selective etch (e.g., EDP or TMAH), from the oxidized wafer of the pair to expose the thermal oxide layer. Aluminum is evaporated and patterned on the top of the oxide layer to form the MOS structures. It has been found that the midgap interface state density is about 5×10^{11} cm^{-2} eV^{-1} while that of the reference samples with thermally grown Si/SiO$_2$ interfaces oxidized in the same furnace as the wafers used in the bonded pairs is in the range of 10^{10} to 10^{11} cm^{-2} eV^{-1}. The properties of the bonded Si/SiO$_2$ interfaces appear to be not sensitive to the chemical treatments prior to bonding. The comparable interface quality of bonded interfaces to thermally oxidized interfaces indicates that proper cleaning and Si/SiO$_2$ bonding procedures prevents additional charges to the bonding interface.

Oxygen-related donors in crystalline silicon can impact device performance. Electron paramagnetic resonance (EPR) was used to identify an

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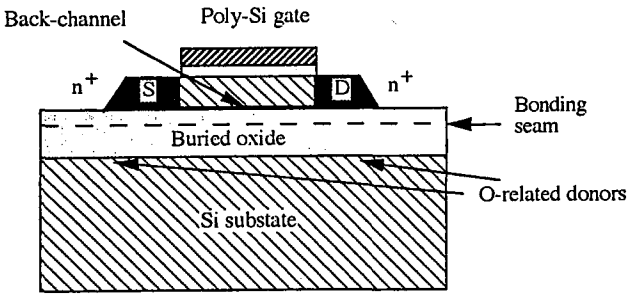

Fig. 7.5 Schematic diagram showing the position of oxygen-related donor defects in a bonded SOI substrate.

oxygen-related donor defect in the silicon substrate, near the bottom Si/SiO_2 interface in a bonded SOI structure, as illustrated in Fig. 7.5 (12). The donor is axially symmetric and is preferentially aligned along the [100] direction. Since these donor defects can be activated during thermal treatment at temperatures in the range of 300 to 850°C, they can effect the intentional doping of the substrate during device fabrication. The origin of the donors appear to be oxygen related. It is suggested that the oxygen-related donors are generated during annealing and the oxygen comes from the diffusion of the buried oxide. Because the donors are related to the annealing during the bonding process, it is expected that the donors could also be present in the top Si/SiO_2 interface, which would impact the device performance significantly in the bonded SOI materials. Presently, no experimental evidence for the presence of oxygen-related donors in the actual SOI layer of bonded wafer is available,

7.2.2 Charges in Bonded SiO_2/SiO_2 Interface Region

In the case of bonding between two oxidized silicon wafers, it was reported that about 1×10^{11} cm^{-2} of negative fixed charges were present at the bonding seam (13) after annealing at 1100°C. To determine the charge, C-V measurements of either MOS or SIS (silicon–insulator–silicon) structures can be used (14).

The MOS structure is formed by etching off the silicon substrate of one wafer in the pair, leaving its oxide bonded to the oxide of the other wafer, followed by aluminum evaporation and patterning. The SIS structure is created by lapping one wafer of the bonded pair to about 10 μm thickness, doping both sides of the structure, and patterning the thin silicon layer to form small measuring dots. The SIS structures are employed to minimize the influence of chemicals used to remove the silicon substrate. The SIS capacitance is a series connection of the oxide capacitance and the interface capacitances at the two Si/SiO_2 interfaces.

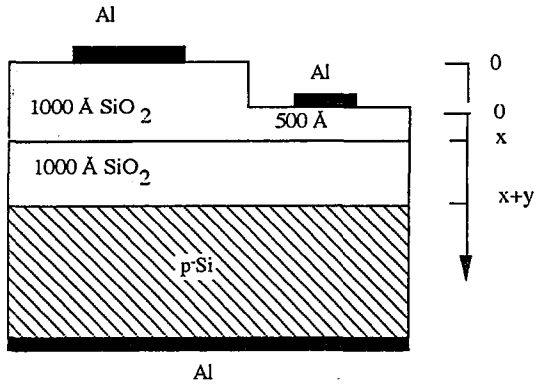

Fig. 7.6 Schematic diagram of a possible MOS capacitor test structure for evaluating interface charges.

The schematic diagram of a possible MOS capacitor test structure is shown in Fig. 7.6 (15). Assuming the interface charge in the MOS structure is due to the presence of two effective fixed-charge sheets (one at the bonding seam with density of Q_i and another at the Si/SiO_2 interface with density of Q_f), we may use the following relationship (15):

$$\frac{xqQ_i}{\varepsilon_0 \varepsilon_{0x}} + \frac{(x+y)qQ_f}{\varepsilon_0 \varepsilon_{0x}} + V_{FB} + |\phi_{FB}| = 0 \qquad (7.5)$$

where x and y are the thickness of two oxide layers; q, ε_0, and ε_{0x} are electron charge, vacuum permittivity, and oxide dielectric constant, respectively; V_{FB} is the flat band voltage; and ϕ_{FB} is the work function difference between aluminum and the silicon wafer. Different thicknesses of the top oxide layer on the same wafer can be obtained by oxide etch after the silicon substrate of the top wafer has been removed. The values of x and V_{FB} can be derived from the maximum capacitance from C-V measurements, and the values of y and ϕ_{FB} are known. The C-V measurements are made at different locations on the same wafer and should be fit to the same values of Q_i and Q_f. The C-V measurements can also be done on different wafers with MOS or SIS structures in which the bonding seam is at different distances from the Si/SiO_2 interface while the combined thickness of the MOS or the SIS capacitor oxide remains constant (13–14).

The origin of the negative charge at the bonding seam is believed to involve reactions between the water and the Si—O—Si bonds at the bonding interface of two bonded oxidized wafers (15). During annealing at 800–1000°C, the interface water can react with Si—O—Si to form Si—OH in the oxide (16):

$$HOH + \equiv Si—O—Si = \Leftrightarrow 2(=Si—OH) \qquad (7.6)$$

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Upon the adsorption of an electron, the Si–OH then produces a hydrogen atom and a nonbridged oxygen bond in the oxide:

$$=\text{Si}-\text{OH} + e^- \Leftrightarrow (=\text{Si}-\text{O}-)^- + \text{H} \qquad (7.7)$$

The nonbridged oxygen bond is a negative charge center. The negative oxide charge is originally located close to the bonding seam. The charge density is reduced with annealing temperature and duration, probably owing to the reverse reaction of Eqs. (7.7) and (7.6). Only a small number of negative charges can be found in the bulk of the buried oxide (9, 17).

7.3 ELECTRICAL PROPERTIES OF BONDED OXIDE

It is known that even nominally dry oxides contain hydrogen with a value of 2×10^{19} H/cm^3 being present in the form of Si—H (Si traps) and O—H (O traps) (18). The hydrogen impurity in oxide is expected to affect the electrical properties of bonded oxides greatly. For samples prepared by bonding of two dry-oxidized hydrophilic FZ silicon wafers and annealing at 1100°C in oxygen, it has been found that the bonding procedure introduces regions in the buried oxide with enhanced etching rate in HF, indicating local changes in the oxide structure (19, 20). Generally, the increased etch rate in HF is one of the features of CVD oxides in which hydrogen is present at significant concentrations. The bonded oxide usually contains more hydrogen than the original oxides because of the reaction of the water monolayers at the bonding seam with the Si—O—Si bonds in the oxide to generate Si—OH during annealing, as described in Eqs. (7.6) and (7.7). The nonuniformity of HF etching can be attributed to the fact that either water molecules react more rapidly with Si—O—Si bonds at the sites in the bonded oxide with preexisting defects, or the excess water cannot be accommodated by the oxide network without localized disruption.

Atomic hydrogen can passivate interface charge traps by attaching to dangling bonds on silicon at the Si/SiO_2 interface. This occurs during annealing of MOS structures at about 400°C in forming gas, a mixture of hydrogen and nitrogen. However, in contrast to the beneficial effect, hydrogen can be quite detrimental when located in the oxide layers. When the oxide is subjected to electron injection or irradiation, mobile hydrogen ions or atoms can be released from weakly bonded hydride in the oxide, which then migrates to the Si/SiO_2 interface where it reactivates silicon dangling bonds, resulting in the creation of interface states (21):

$$\text{Si}_3{\equiv}\text{Si}-\text{H} + \text{H} \longrightarrow \text{Si}_3{\equiv}\text{Si}- + \text{H}_2 \qquad (7.8)$$

The interface state $\text{Si}_3{\equiv}\text{Si}-$ has been termed a P_b center. Its density of states generally has a U-shaped distribution in the band gap. The P_b centers in the upper part of the gap are electron traps and those in the lower part are hole traps (22). Much higher numbers of P_b centers in bonded oxides than

thermal oxides can be attributed to a much higher availability of H after wafer bonding.

Moreover, according to Eq. (7.7), Si—O—H groups in the oxide are electron traps which become negatively charged upon electron trapping. Compared with normal thermal oxides, which show an accumulation of less than 5×10^{10} electrons/cm^2 after electron injection, more than 3×10^{11} electrons/cm^2 are trapped in a bonded oxide (19). The result can be explained by the fact that bonded oxides contain more Si—O—H groups than normal thermal oxides. Since incorporation of hydrogen in the thermal oxide network can also produce oxygen vacancies ($\text{O}_3{\equiv}\text{Si}-$, the E′ center) which are responsible for hole trapping in the oxide (21), a significant enhancement of hole trapping in the bonded oxide is also observed.

To improve radiation hardness of MOS devices, it is beneficial to perform a vacuum annealing at 1000°C or higher following growth of the oxide. This process step can reduce the hydrogen content in the oxide and then minimize hydrogen-mediated reactivation of interface charge traps which occurs under irradiation or charge injection (18). Since preprocessed wafers can be bonded, other advanced oxide-hardening techniques can also be employed during formation of the thermally grown oxide and its interface with silicon prior to bonding. The resultant buried oxide can be favorable for achieving radiation hardness of MOS devices. We discuss radiation-hard SOI devices in Section 12.1.2.

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8

Stresses in Bonded Wafers

Since wafer surfaces are not perfectly flat and smooth, to achieve conformity, the attraction forces between the two bonding surfaces must elastically deform each wafer, resulting in stresses in the bonded pair. The inclusion of trapped gas or particulate bubbles, the changes in interface structure, and the interface composition can also introduce stresses in the bonded pair. When bonding wafers of dissimilar materials, the difference in their thermal expansion coefficients causes excess mechanical stresses in the bonded pair after annealing at elevated temperatures and subsequent cooling. Severe stresses can lead to deformation, debonding, and even fracture of the pair. In this chapter, we discuss the origins of the stresses in bonded pairs and present equations to predict these stresses.

8.1 STRESSES CAUSED BY SURFACE WAVINESS

As described in Chapter 3, the deformation of wafers in a bonded pair can be detected by X-ray topography (XRT). Wafer deformation results in a contrast change of XRT images. A roughness-like pattern throughout the bonded area of a pair has been experimentally observed (1). By comparing the XRT image of the bonded pair and the original optical topograph of the bonded surface after the bonded wafer was separated from its mate, it was determined that the XRT contrast is related to the local flatness variation of the wafers. When two surfaces of similar topography mate together, the periodicity of the strain pattern resulting from the pushing forces at the asperities and the pulling forces in the valleys should be comparable to that of the original surface flatness periodicity (waviness). For bonding of 4-in. oxidized or bare silicon wafers, the amplitude and spatial frequency distribution of the waviness sinusoidal components in the optical topograph indicate that the dominant component has a spatial wavelength on the order of 1 mm, comparable to the strain contrast observed in XRT topography.

Figure 8.1 shows the schematic geometry of the bonding surfaces used in the calculation of local stress. The analysis of the stress caused by bonding of nonflat surfaces embodies the following assumptions: (1) the asperities and valleys are part of a sinusoidal surface topography, which may partly be

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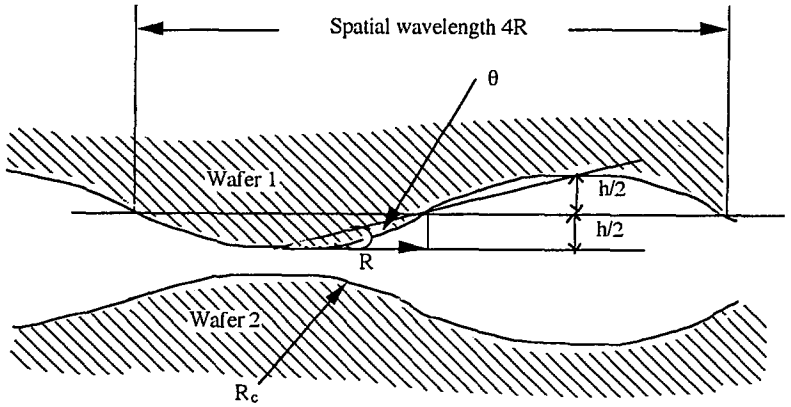

Fig. 8.1 Schematic geometry of the bonding surfaces used in the calculation of local stress.

approximated by a spherical geometry, so that the theory of deformation of elastic spheres can be employed; (2) the asperities of the two surfaces are aligned with respect to each other so that the highest stress is estimated; (3) the two bonding wafers are of equal thickness, and are of the same material. In Fig. 8.1, the asperities and the valleys displace a distance $h/2$ onto a plane located halfway between those containing the tips of the asperities and the bottoms of the valleys, respectively. The resulting maximum stress, which is normal to the surface and averaged over the asperity base area, is given by (2)

$$\sigma_{max} = 4Eh/[\pi R(1 - \nu^2)] \tag{8.1}$$

where E is Young's modulus of the bonding wafers, ν is Poisson's ratio, and R denotes 1/4 of the spatial wavelength. For 4-in. silicon wafers, the typical values of $R = 0.25$ mm and $h/2 = 100$ Å result in a maximum stress of $\sigma_{max} \cong 1 \times 10^7$ N/m^2. The radius of curvature of these asperities and the valleys is $R_c \cong R^2/h \approx 3$ m for the parameters above. The average slope angle θ is about 0.002°.

When one wafer (device wafer) of the pair is thinned, it becomes more deformed because the thick substrate relaxes. If the device layer is sufficiently thin, the stress in the substrate relaxes almost completely and the device layer has to deform in the vertical direction a distance of another $h/2$ at the extremities of the flatness profile. Since the thickness of the film t_f is much smaller than the diameter $2R$ of the deformed area, the elastic spheres approach is not valid; instead, a bending of a uniformly loaded thin circular plate model is used in evaluating the stress (3). When the edge of the pair is not allowed to move freely, the maximum stress occurs at the edge, and we get

$$\sigma_{max} = 2Eht_f/[R^2(1 - \nu^2)] \tag{8.2}$$

The expression

$$\sigma_{max} = Eht_f(3 + \nu)/[R^2(5 + \nu)(1 - \nu)] \tag{8.3}$$

is valid for the case when edge movement is allowed. In this case, the maximum stress is present at its center.

The stress in a silicon film of thickness of 0.5 μm is about 1.2×10^5 N/m^2 using Eq. (8.2) and 4.4×10^4 N/m^2 using Eq. (8.3). The actual stress is expected to be somewhere between the two values. The value is much less than that required to spontaneously nucleate dislocations and plastically deform silicon (2.5×10^9 N/m^2), and should not affect structural properties of the silicon film on the bonded pairs. However, the residual stress in silicon film has a remarkable effect on the dependence of SOI wafer warpage on film thickness (4). We discuss this effect in Section 8.2.4.

8.2 STRESSES IN BONDED DISSIMILAR MATERIALS

8.2.1 Basic Analytic Equations

There are basically two approaches to evaluate stresses in a composite structure. One is to calculate the stresses by analytic equations. Assumptions have to be made to simplify the equation and the solution is approximate in nature. The second approach is to use numerical techniques such as finite element methods. In this section, we describe a typical set of basic equations that can be used to predict the stresses in a bonded pair.

The theoretical distribution of stresses in bimetal strips subjected to uniform heating or cooling has been reported (5). When bonding dissimilar materials, we assume that the difference in thermal expansion coefficients, $\Delta\alpha = (\alpha_2 - \alpha_1)$, is independent of temperature. We also assume that no bubbles, debonding, sliding, or structural or compositional changes occur during temperature changes. The bonding pair has the following material parameters: E_1 and E_2 are Young's modulus of wafer 1 and wafer 2, respectively; t_{w1} and t_{w2} are the respective wafer thicknesses; ν_1 and ν_2 are the respective Poisson ratios; R is the radius of the circular wafers (see Fig. 8.2). The elastic bimetallic strip theory may be adopted approximately to circular wafers. The normal stresses (tension and compression, parallel to the interface) are maximum on the interface and their lateral distributions, $\sigma_1(x)$ and $\sigma_2(x)$, at the interface of wafer 1 and wafer 2 are given by (9.6)

$$\sigma_1(x) = \frac{\Delta\alpha\Delta T}{\lambda t_{w1}}\left[1 + \frac{3t_w D_1}{t_{w1} D}\right][1 - \exp[-K(R - x)]] \tag{8.4}$$

$$\sigma_2(x) = -\frac{\Delta\alpha\Delta T}{\lambda t_{w2}}\left[1 + \frac{3t_w D_2}{t_{w2} D}\right][1 - \exp[-K(R - x)]] \tag{8.5}$$

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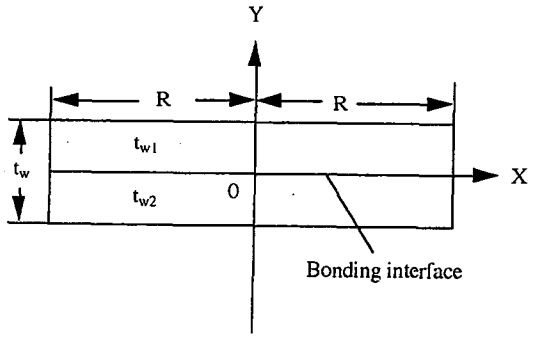

Fig. 8.2 Schematic bonding structure for stress analysis.

where x is the distance from the center at the interface, the plus sign is used for tensile stresses and the minus sign is used for compressive stresses, $\Delta\alpha = (\alpha_2 - \alpha_1)$, ΔT is the temperature change, $t_w = t_{w1} + t_{w2}$, and

$$\lambda = \left(\frac{1-\nu_1^2}{E_1 t_{w1}} + \frac{1-\nu_2^2}{E_2 t_{w2}} + \frac{3(t_{w1}+t_{w2})^2(1-\nu_1^2)(1-\nu_2^2)}{E_1 t_{w1}^3(1-\nu_2^2) + E_2 t_{w2}^3(1-\nu_1^2)} \right) \tag{8.6}$$

$$D_1 = \frac{E_1 t_{w1}^3}{12(1-\nu_1^2)} \tag{8.7}$$

$$D_2 = \frac{E_2 t_{w2}^3}{12(1-\nu_2^2)} \tag{8.8}$$

$$D = D_1 + D_2 \tag{8.9}$$

$$K^2 = \frac{\lambda}{[2t_{w1}(1+\nu_1)/3E_1] + [2t_{w2}(1+\nu_2)/3E_2]} \tag{8.10}$$

Equations (8.4) and (8.5) indicate that the normal stresses drop rapidly at the edges of the bonded wafers.

The vertical distribution of the normal stresses within the two bonding wafers at the center of the wafers can be expressed as (7)

$$\sigma_1(y) = \frac{1}{\rho}\left[(y - t_{w1}/2)E_1' - \frac{2}{t_{w1}(t_{w1}+t_{w2})}\left(\frac{E_1' t_{w1}^3 + E_2' t_{w2}^3}{12} \right) \right] \tag{8.11}$$

and

$$\sigma_2(y) = \frac{1}{\rho}\left[(y - t_{w2}/2)E_2' + \frac{2}{t_{w2}(t_{w1}+t_{w2})}\left(\frac{E_1' t_{w1}^3 + E_2' t_{w2}^3}{12} \right) \right] \tag{8.12}$$

where y is the distance measured from the bonding interface of the bonded pair, and is positive for wafer 1 and negative for wafer 2, and ρ is the radius of curvature of the bonded pair which can be expressed as (4)

$$\rho = \frac{(E_1' t_1^3 + E_2' t_2^3)(E_1' t_1 + E_2' t_2) + 3E_1' E_2' t_1 t_2 (t_1 + t_2)^2}{6E_1' E_2' t_1 t_2 (t_1 + t_2)[\Delta\alpha\,\Delta T]} \tag{8.13}$$

where $E' = E/(1-\nu)$ is the biaxial modulus.

The specific elastic biaxial strain energy (unit area elastic energy) E_{el} based on pure bending in a beam is approximately given by (7)

$$E_{el} = \int_0^{t_w} \frac{\sigma^2(y)}{2E'}\,dy \tag{8.14}$$

For the bonded pair we get

$$E_{el} = \int_0^{t_{w1}} \frac{\sigma_1^2(y)}{2E_1'}\,dy + \int_{-t_{w2}}^{0} \frac{\sigma_2^2(y)}{2E_2'}\,dy \tag{8.15}$$

If the specific elastic biaxial strain energy is larger than the bonding energy 2γ, interface sliding or even complete debonding can occur.

Close inspection of the stresses involved in the bonded pair reveals that in addition to the normal stresses of the two bonding wafers that are parallel to the bonding interface, shear stresses and peeling stresses (that are vertical to the bonding interface) are also present. The shear and peeling stresses are concentrated near the edges of the bonding pair and vary exponentially along the interface from the center ($x = 0$) to the edges ($x \cong R$). The shear stress, τ, at the bonding interface ($y = 0$) can be expressed by the formula

$$\tau = \tau_{max} \exp[-K(R-x)] \tag{8.16}$$

where

$$\tau_{max} = \Delta\alpha\,\Delta T K/\lambda \tag{8.17}$$

The peeling stress has a similar expression:

$$p = p_{max} \exp[-K(R-x)] \tag{8.18}$$

where

$$p_{max} = \frac{\mu K^2}{\lambda}\Delta\alpha\Delta T \tag{8.19}$$

$$\mu = \frac{1}{2}\frac{E_1 t_{w1}^3 t_{w2}(1-\nu_2^2) - E_2 t_{w2}^3 t_{w1}(1-\nu_1^2)}{E_1 t_{w1}^3(1-\nu_2^2) + E_2 t_{w2}^3(1-\nu_1^2)} \tag{8.20}$$

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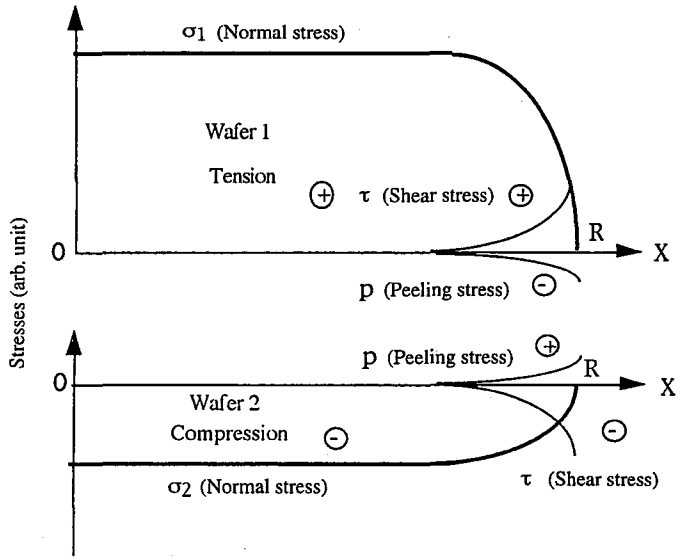

Fig. 8.3 Schematic stress distributions of the interface of a bonded and heated pair with $\alpha_1 < \alpha_2$, $E_1 > E_1$ at the elevated temperature.

Usually, the peeling stresses are responsible for initiating debonding of bonded pairs. From Eq. (8.20) it can be seen that if

$$\frac{t_{w1}}{t_{w2}} = \sqrt{\frac{E_2(1-\nu_1^2)}{E_1(1-\nu_2^2)}} \tag{8.21}$$

then the peeling stresses are zero at any temperature. This feature can be used to alleviate debonding problems of bonded pairs of dissimilar materials undergoing temperature cycling, provided the thickness ratio of the wafers to be bonded can be chosen based on Eq. (8.21).

Equations (8.4)–(8.22) are essentially the same as those derived by Suhir (5). Figure 8.3 is a schematic of the stress distributions at the interface of a bonded pair (with $\alpha_1 < \alpha_2$, $E_1 > E_2$) heated uniformly.

8.2.2 Stresses in Thin Films

If one wafer of the bonded pair is thinned sufficiently, the stresses in the substrate relax almost completely. The stresses are then concentrated in the thin film. Based on the results of the calculations in reference 6, the three main stresses existing in bonded thin films are given by the following expressions, where we use the subscripts "f" for the thin film and "s" for the substrate.

1. The normal stress, σ_f, which is parallel to the bonding interface, is given by

$$\sigma_f = \frac{E_f}{1-\nu_f}(\alpha_f - \alpha_s)\Delta T\{1 - \exp[-K(R-x)]\} \tag{8.22}$$

where $K = \sqrt{\frac{\lambda}{k}}$; $\lambda = \frac{1-\nu_f}{E_f t_f}$; $k = \frac{2}{3}\left\{\frac{(1+\nu_f)t_f}{E_f} + \frac{(1+\nu_s)t_s}{E_s}\right\}$; origin 0 of the rectangular coordinates x, y is in the middle of the wafer on the interface; x is parallel to the bonding interface ($y = 0$) and from the center ($x = 0$) to the edges ($x = R$).

2. The shear stress, τ_f, which is parallel to the bonding interface, is given by

$$\tau_f = \tau_{max} \exp[-K(R-x)] \tag{8.23}$$

$$\tau_{max} = -\frac{E_f}{1-\nu_f}(\alpha_f - \alpha_s)\Delta T t_f K \tag{8.24}$$

3. The peeling stress, p_f, which is vertical to the bonding interface, is given by

$$p_f = p_{max} \exp[-K(R-x)] \tag{8.25}$$

$$p_{max} = \frac{1}{2}Kt_f\tau_{max} \tag{8.26}$$

From Eqs. (8.22)–(8.26) it is clear that the normal stress in thin films is independent of film thickness as long as $t_f \ll t_s$ and locations not too close to the rim are considered. However, the shear and peeling stresses increase with film thickness and depend, via K, on material properties of both the thin film and substrate. The normal stresses drop rapidly to zero at the edge of the film. In contrast, the shear and peeling stresses concentrate near the edge of the film and decrease exponentially away from the edge.

If the thickness of the first wafer of the bonded pair is much smaller than that of the second (substrate) wafer, the stress in the thin film (except the areas very close to the edge) can be determined from the measured radius of curvature, ρ, of the bonded substrate via

$$\sigma_f = \frac{E_s t_s^2}{6\rho t_f(1-\nu_s)} \tag{8.27}$$

Equation (8.27) allows experimental determination of σ_f even if no information is available on $\Delta\alpha$ and the elastic constants of the film. Under these circumstances, the expression (Eq. 8.13) for ρ becomes

$$\rho = \frac{E_s' t_s^2}{6E_f' t_f[(\alpha_f - \alpha_s)\Delta T]} \tag{8.28}$$

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In addition to elastic deformation, plastic deformation is also possible when the stress in the film exceeds the critical yield stress of the material. However, even if σ_f exceeds the yield stress, dislocations do not necessarily form in very thin films on a substrate because the introduction of thermal misfit dislocations is not energetically favorable below a critical thickness, t_c. Similar to Eq. (6.10), this critical thickness can be derived based on a balance between strain energy and thermal misfit dislocation energy as (7)

$$t_c = \frac{b(1 - \nu\cos^2\theta)[\ln(t_c/b) + 1]}{8\pi(1 + \nu)f\cos\lambda} \tag{8.29}$$

where b is Burger's vector ($a/\sqrt{2}$ for Si, where a is Si lattice constant), θ is the angle between the dislocation line and its Burger's vector, λ is the angle between the slip direction and that line in the interface plane which is normal to the line of intersection between the slip plane and the interface (for Si, $\theta = \lambda = 60°$), and f is the thermal misfit given by $\Delta\alpha\Delta T$. Equation (8.29) predicts that for a thin silicon film on a quartz glass substrate, the critical thickness of the silicon film is about 0.1 μm to allow dislocation-free processing up to 1000°C.

8.2.3 Stresses in Bonded GaAs/Si Structures

Employing a numerical analysis approach, the stress distribution in composite structures can be obtained more accurately than by using the analytical approach, especially for complex geometries. Using a numerical analysis method, the stress distribution in GaAs directly bonded to silicon has been reported (8). The analysis was performed with a finite element program using axisymmetric models of the wafers.

As a standard procedure in a finite element technique, the bonded structure is decomposed into a mesh of triangles, with smaller triangles in high-stress gradient regions (at the edges of the bonded pair). Typically, there are six nodes ($i = 6$) at the corners and along the sides in each triangle element. Assuming the displacement u has a parabolic distribution and the bonding wafers are isotropic with Young's modulus E, Poisson's ratio ν, thermal expansion coefficient α, and temperature change ΔT, the derivative of small displacements u in the x direction is related to the various components of the stress tensor by

$$\frac{\partial u}{\partial x} = (\sigma_{xx} - \nu\sigma_{yy} - \nu\sigma_{zz})/E + \alpha\Delta T \tag{8.30}$$

For each triangle with the nodal displacement vector $\mathbf{u}_i$, the force vector $\mathbf{f}_j$ has to be applied to each node to balance the stresses:

$$\mathbf{f}_j = \mathbf{k}_{ij}\mathbf{u}_j \tag{8.31}$$

where $\mathbf{k}_{ij}$ is the stiffness matrix.

TABLE 8.1 Fracture or Debonding Temperature of GaAs/Si Bonded Pairs

GaAs/Si Thickness Ratio	Total Thickness (μm)	Si Thickness (μm)	Fracture or Debonding Temperature
1.00	1273	635	160°C
0.652	537	325	250°C
0.614	234	145	> 350°C
0.089	588	540	200°C

The displacements must be the same and the force must be balanced at each node for all the triangles that share the node. A uniform thermal expansion is added to each triangle. By matching nodes at the boundaries to the boundary conditions and minimizing the overall energy, the nodal displacements are obtained. Together with the parabolic displacement functions, the displacements and their derivatives can be calculated, resulting in approximate stress distributions within each element.

The calculations indicate that the shear and peeling stresses at the interface increase rapidly close to the wafer edge. The stresses are reduced by thinning just the GaAs wafer or both the GaAs and the Si wafers. These results were experimentally verified (8). It was also found that a tapered edge of the top GaAs wafer in a bonded pair reduces the stresses at the edge of the wafer. Table 8.1 lists the experimental results of fracture or debonding temperature for GaAs wafers bonded to silicon wafers covered by a 2500-Å thick oxide as a function of GaAs to Si thickness ratio and total thickness of the bonded pairs. Both reduced thickness ratios between GaAs and Si and tapered edges increase the maximum processing temperature and grinding durability.

8.2.4 Stresses in Bonded SOI and Multilayered Structures

The SOI wafers are three-layer structures. Stresses involved in the structure and changes that occur during their processing for device fabrication have a significant impact on deformation of the structures and therefore on the stress in the silicon device layer. Deformation (warpage) of SOI wafers is an obstacle for wafer handling as well as focus and alignment in photolithographic processing. Excessive stress in the structure can even cause permanent plastic deformation during high-temperature processing steps and delamination of the device layers. Therefore, stress analysis in SOI structures is important in the design of SOI materials to minimize the deformation and the stresses in the device layers for a given device-processing sequence.

Similar to the two-layer structures discussed above, when a mutilayered heterostructure, fabricated on a thick substrate (shown in Fig. 8.4) is subject to temperature change, stresses will be induced owing to differences in thermal expansion coefficients. The stresses will cause the structure to bend

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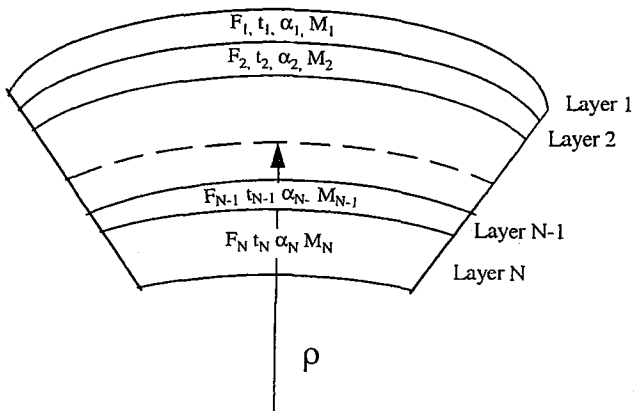

Fig. 8.4 Schematic of bending of a mutilayer heterostructure due to thermal mismatch.

with a radius ρ which is assumed to be much larger than the film thickness, so that the theory of small deflection is valid. The stresses in the films and substrate must satisfy force and momentum balance (9, 10):

(1) Force balance:

$$\sum_{i=1}^{N} F_i = 0 \tag{8.32}$$

where F_i is the normal force for each layer and, N is the number of layers in the structure.

(2) Moment balance:

$$\sum_{i=1}^{N} M_i + \sum_{i=1}^{N} F_i \left(\sum_{j=1}^{i-1} t_j + t_i/2 \right) = 0 \tag{8.33}$$

where $M_i = [E_i t_i^3 / 12\rho(1 - \nu_i)]$ is the bending moment and t_i is the thickness of each layer.

(3) Interface strain continuity for any two adjacent layers:

$$\alpha_i \Delta T_i + \frac{F_i}{E_i' t_i} + \frac{t_i}{2\rho} = \alpha_{i+1} \Delta T_i + \frac{F_{i+1}}{E_{i+1}' t_{i+1}} + \frac{t_{i+1}}{2\rho} \qquad (i = 1, 2, \ldots, N-1) \tag{8.34}$$

where $E_i' = E_i/(1 - \nu_i)$ is the biaxial modulus, α_i, ν_i, and E_i are the thermal expansion coefficient, Poisson's ratio, and Young's modulus for the ith layer,

and ρ is the radius of curvature of the structure. The first term in this equation is from the thermal expansion, but other strain terms should be added if there are other strain sources involved in the thin-film formation. The second term accounts for the elastic deformation caused by the normal force. The third term originates from the geometrical constraint at the interface.

The $N + 1$ equations above can be solved by using a Gaussian elimination technique. The $(N + 1)$ unknowns $F_1, F_2, F_3, \ldots, F_N, \rho$ can thus be determined. The stress for each layer is calculated by (8)

$$\sigma_i = \frac{F_i}{t_i} + \frac{E_i \left(\sum_{j=1}^{i-1} t_j + t_i/2 \right)}{\rho} \tag{8.35}$$

The equations above were derived based on the following assumptions: (1) the substrate and surface films are isotropically elastic, (2) the stresses are in-plane stresses, (3) no chemical reactions between layers occur, (4) no net forces are present at free surfaces or edges, and (5) no shear and peeling stresses are considered at this point. The analysis of shear and peeling stresses in a two-layer structure is described in Section 8.2.1 and that in mutilayered elastic films can be found in the literature (6).

The simulation of bonded SOI deformation as a function of layer thickness using the equations above was reported (4). It indicates that: (1) reducing the buried oxide thickness or increasing the substrate thickness can effectively reduce the total deformation when the structure cools to room temperature after thermal treatments, (2) the warpage of bonded SOI wafers can be reduced by retaining an oxide layer on the back of the substrate (if the oxide thickness on the back of the substrate is identical to that of the buried oxide, warpage will essentially be avoided); (3) if the thickness of the silicon device layer is more than 10 μm, the warpage will be reduced as the silicon layer becomes thicker.

8.3 BONDING OF PRESTRESSED WAFERS

During room-temperature bonding, two wafers can be supported at the rim by posts in the bonding machine described in Section 4.5. If an external pressure is exerted on the wafers at the center of one side to initiate the bonding, bonded wafer pairs can be deformed with a defined vertical stress distribution which is dependent on the imposed curvature (see Fig. 8.5) (11). During the pressing procedure, the wafers bond and debond several times.

When a single wafer is bent by an external force, the convex side is put under tension while the concave side is put under compression. The stresses decrease with increasing distance from the wafer surface until they disappear

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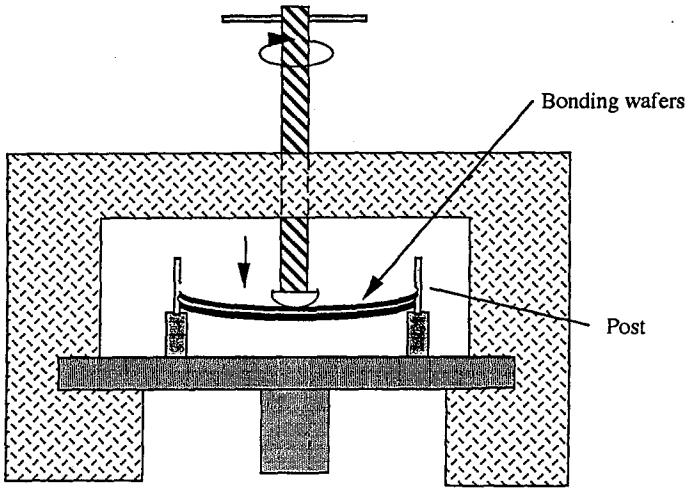


Fig. 8.5 Front view of bonding machine with attached pressing device for prestressed wafer bonding.

in a neutral plane. If the wafers are bonded in the bent state, the bonded surfaces cannot move against each other once the external force is removed. Therefore, the wafers cannot assume their original shape, but retain some curvature and stress. A simplified model has been developed to estimate the stresses in wafers bonded with an imposed curvature (11).

Assuming (1) biaxial stresses and strain that are linearly dependent on the thickness of both wafers, (2) balance of forces and momentums, and (3) equal strain at the bonded interface, the expressions for the vertical stress distribution $\sigma(y)$ and the radius of curvature ρ can be obtained. The quantities $\sigma(y)$ and ρ are functions of the initial radius of curvature after bonding ρ_0, the thickness of the wafers, t_w, and the final thickness, $t_f < t_w$, of the top wafer after thinning. The stresses at the surface of the top (convex side) and bottom (concave side) wafers, σ_{s1} and σ_{s2}, are

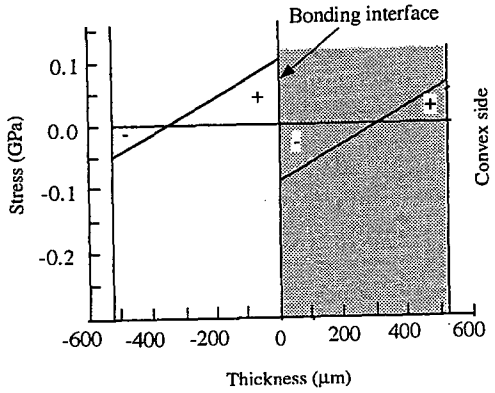
$$\sigma_{s1}(t_f) = \frac{E}{1-\nu}\frac{4t_w^2(2t_f - t_w)}{3\rho_0(t_f + t_w)^2} \tag{8.36}$$

$$\sigma_{s2}(t_f) = \frac{E}{1-\nu}\frac{-4t_w(2t_f - t_w)}{3\rho_0(t_f + t_w)^2} \tag{8.37}$$

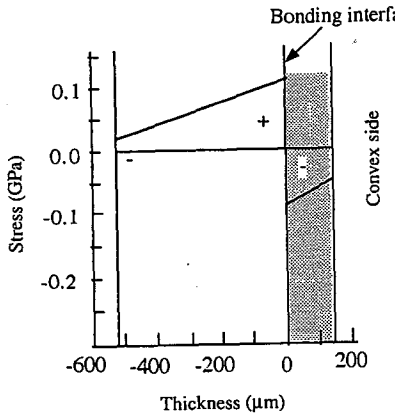
The stresses at the interface of the top and bottom wafers, $\sigma_{if1}(t_f)$ and $\sigma_{if2}(t_f)$, are given by

$$\sigma_{if1}(t_f) = \frac{E}{1-\nu}\frac{4t_w^2(-4t_f^2 + t_w t_f - t_w^2)}{3\rho_0(t_f + t_w)^3} \tag{8.38}$$

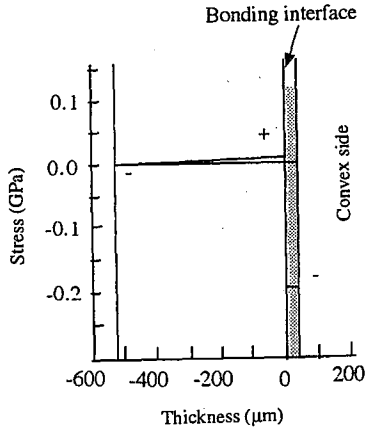
$$\sigma_{if2}(t_f) = \frac{E}{1-\nu}\frac{4t_w t_f(t_f^2 - t_w t_f + 4t_w^2)}{3\rho_0(t_f + t_w)^3} \tag{8.39}$$



(a)



(b)



(c)

Fig. 8.6 Calculated results of vertical distribution (*a*) for as-bonded wafers with a radius of curvature of 1 m and a thickness of 525 μm, (*b*) after thinning the convex side to one fourth of the initial thickness, and (*c*) after thinning to 0.1 μm. The thickness of the layer in the 0.1-μm layer is not shown to scale.

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The radius of curvature can be expressed as

$$\rho = \rho_0 \frac{(t_f + t_w)^3}{8 t_f t_w^2} \tag{8.40}$$

The model predictions are as follows. Both wafers with thickness t_w of an as-bonded pair show a distribution of tensile and compressive stresses. The stress values are higher at the bonded interface than at the surfaces. When the convex side of the wafer is thinned, the unthinned wafer is able to bounce back, resulting in a high compressive stress in the thin layer while stresses have almost disappeared in the unthinned handle wafer. An analogous situation with a high tensile stress in the remaining thin layers may be obtained by thinning the concave part of the wafer pair.

Figure 8.6 shows the calculated results of vertical stress distribution (*a*) for as-bonded wafers with a radius of curvature of 1 m and a thickness of 525 μm, (*b*) after thinning the convex side to one fourth of the initial thickness, and (*c*) after thinning to 0.1 μm. The surface and interface stresses change as a function of the thickness of the thinned wafer. The surface stress at the convex side changes from tensile to compressive and tends toward a maximal value while the stresses in the thick wafer decays drastically. A maximal compressive stress of -0.20 GPa is achieved when two 525-μm thick, 4-in. silicon wafers are bonded with a radius of curvature of 1 m. The curvature decreases rapidly when the thinned down wafer approaches a thickness of 100 μm or less. For a silicon layer thickness of 0.1 μm, a radius of 657 m is obtained, corresponding to a bow of 2 μm.

Prestressing of bonded wafers allows production of SOI layers under compression for enhanced mechanical stability, increased hole mobility and decreased electron mobility (12). The method could also be employed to compensate for wafer bow caused by a buried layer.

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9

Bonding of Dissimilar Materials

9.1 BONDING OF WAFERS OF DISSIMILAR MATERIALS

One of the main advantages of direct wafer bonding technology is its ability to integrate two or more dissimilar materials into one composite. As pointed out by Haisma and co-workers (1), almost all materials investigated can be directly bonded to themselves or to oxidized silicon at room temperature provided the materials are properly polished and prepared as shown in Table 1.1.

As discussed in Chapter 8, the major concern in bonding of dissimilar materials is the thermal stress originating from a mismatch in thermal expansion coefficients. Usually, when the two bonded wafers of dissimilar materials are both relatively thick and a high-temperature anneal is used to strengthen the bond, the pair will severely bend. If the thermal stresses become sufficiently high, they may be released by debonding, sliding, cracking, plastic deformation, or misfit dislocation generation. However, once one of the wafers in the pair is thinned sufficiently, the stresses in the thick wafer almost disappear as it is able to bounce back while the thin film on its top is under a high stress.

If the temperature is below a critical value, the thermal stress is smaller than the critical yield stress of the material, and plastic deformation of the thin film can be avoided. In addition, when the thickness of the thin film is below a critical value, even if the thermal stress exceeds the yield stress, misfit dislocations can still be prevented because the formation of thermal misfit dislocations at the thin film/substrate interface would lead to an increase of the total energy. Therefore, for bonding of dissimilar materials, the general practice is to anneal the bonded pair at a temperature that is as low as possible to achieve a bonding strength as high as possible, which must be sufficiently high to allow subsequent thinning. The thickness of the resultant film should be below the critical value at the maximum device processing temperature to avoid dislocation generation.

Silicon is the most important material for the microelectronics industry. It has superior and well-controlled electronic properties, can be grown in high purity, is easy to dope, and has a high crystal perfection, a suitable band gap and breakdown field, and low interface states. Silicon is also a reliable,

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TABLE 9.1 Some Important Properties of Si and Other Materials at 25°C

Properties	Si	GaAs	InP	SiO_2	Sapphire
Crystal	Diamond	Zncblende	Zncblende	Amorphous	Rhombohedral
Polarity	Nonpolar	Polar	Polar	Nonpolar	polar
Atomic or molecular density (cm^{-3})	5.02×10^{22}	2.21×10^{22}	4.42×10^{22}	2.20×10^{22}	5.6×10^{22}
Lattice constant (Å)	5.4307	5.6532	5.8687	N/A	a = 4.758 c = 12.991
Covalent radius (Å)	1.17	Ga:1.26 As: 1.18	In:1.44 P: 1.10	Si: 1.17 O: 0.66	Al: 1.26 O: 0.66
Band gap (eV)	1.12	1.424	1.344	~ 8.0	5.0
Melting temperature (°C)	1412	1237	1062	1700	2030
Thermal conductivity (W/cm.K)	1.5	0.455	0.7	0.015	0.5
Koop hardness (kg/mm^2)	850	750		820	2100
Yield strength (dyn/cm^2)	7.0×10^{10}			8.4×10^{10}	15.4×10^{10}
Density (g/cm^3)	2.33	5.3176	4.81	2.27	3.98
(100) Young's modulus ($dyne/cm^2$)	1.30×10^{12}	1.19×10^{12}	1.01×10^{12}	0.66×10^{12}	5.3×10^{12} ($1\bar{1}02$)
(110) Young's modulus ($dyne/cm^2$)	1.69×10^{12}	1.207×10^{12}			
(111) Young's modulus ($dyne/cm^2$)	1.87×10^{12}				
Thermal expansion coefficient (K^{-1})	2.6×10^{-6}	6.8×10^{-6}	4.8×10^{-6}	0.56×10^{-6}	5.8×10^{-6}
Dielectric constant	11.7	13.1	12.6	3.9	4.8–9.1
Refractive index	3.51	3.3	3.22	1.46	1.77
Breakdown field (V/cm)	3×10^5	3.5×10^5		1.2×10^7	3×10^5
Electron mobility (cm^2/Vs)	1450	8800	5370		
Hole mobility (cm^2/Vs)	500	360	150		
Bond density (10^{15} cm^{-2})					
(100)	1.355				
(110)	1.9189				
(111)	1.564				
Poisson's ratio	0.29	0.29		0.17	0.24

high-strength, and high-precision mechanical material. Some important properties of silicon and other commonly used materials at 25°C are listed in Table 9.1. Silicon-compatible materials and technologies are therefore highly desirable for successful new products. For optoelectronics, electroacoustics, nonlinear optics, or other applications, it is also desirable to combine silicon with appropriate materials with superior optical, acoustic, or other application-specific properties. This chapter describes some important examples of dissimilar material integration by wafer bonding.

9.1.1 GaAs/Si Bonding

The objective of GaAs/Si bonding is to produce a material system in which a thin, bulk quality GaAs layer is monolithically integrated on a silicon substrate. In contrast to the case of epitaxial growth of GaAs on silicon, the wafer-bonding approach can avoid the generation of threading dislocations in the GaAs layer caused by the 4.1% difference in the lattice constants of silicon and GaAs. The composite has the advantage of combining the properties of Si and GaAs to realize the integration of GaAs optical devices with Si-signal-processing devices on the same chip. Moreover, the GaAs film on Si substrate can be used as a buffer layer for the growth of other compound semiconductors.

For comparison, some important properties of GaAs at 25°C are listed together with those of silicon in Table 9.1. The table implies that the superior thermal and mechanical properties of Si compared to those of GaAs constitute another important advantage of the combination of Si and GaAs. The GaAs devices fabricated on Si substrates dissipate higher power than those on GaAs substrates owing to the more than three times higher thermal conductivity of Si. Thinner bonded GaAs/Si wafers can achieve the same mechanical strength as thicker GaAs substrates, resulting in lower cost and weight. Moreover, GaAs/Si wafer pairs can be handled basically like Si wafers.

As seen in Table 9.1, Si is a nonpolar semiconductor while GaAs is a polar one. There is a 4.1% lattice mismatch between Si and GaAs. These differences between the two materials are the major obstacles for heteroexpitaxial growth of GaAs on Si, but pose no difficulty for bonding. However, the 160% mismatch in thermal expansion coefficients presents a major challenge for GaAs/Si bonding because of thermal stresses induced in the bonded pair when subjected to a heat treatment. Thermal expansion coefficients of Si and GaAs as a function of temperature are shown in Fig. 9.1.

Bonding of GaAs to Si or oxidized Si has been reported (1–3). The as-received GaAs (638 μm thick) and Si (525 μm thick) wafers were bonded at room temperature in a microcleanroom setup (3). The bonding procedures were identical to those described in Chapter 4. Unless small pieces of GaAs and Si are used, the GaAs/Si pair may debond during annealing at temperatures higher than 160°C owing to the large difference in their thermal expansion coefficients. The surface energy of the Si/GaAs pair after 140°C annealing was ~ 220 mJ/m^2.

Using the lift-off method (see Section 6.3.3), 1μm GaAs/InGaAs/AlGaAs quantum-well films grown on GaAs (1 × 1 cm^2) were also transferred to oxidized Si or glass substrates (2). Prior to bonding, the oxidized Si or glass wafers were briefly etched in dilute HF. The quantum-well films were separated from the GaAs substrate by lateral etching of the AlAs layer in a 10% HF aqueous solution for several hours. Measurement of the change of lattice constant perpendicular to the bonding interface plane with respect to temperature for the 1-μm film revealed that for small temperature changes (< 50°C), the film remains rigidly attached to the oxide and the thermal stress is accommodated by a tetragonal distortion of the film. At higher temperatures (up to 350°C), the stress exceeds the bonding shear strength

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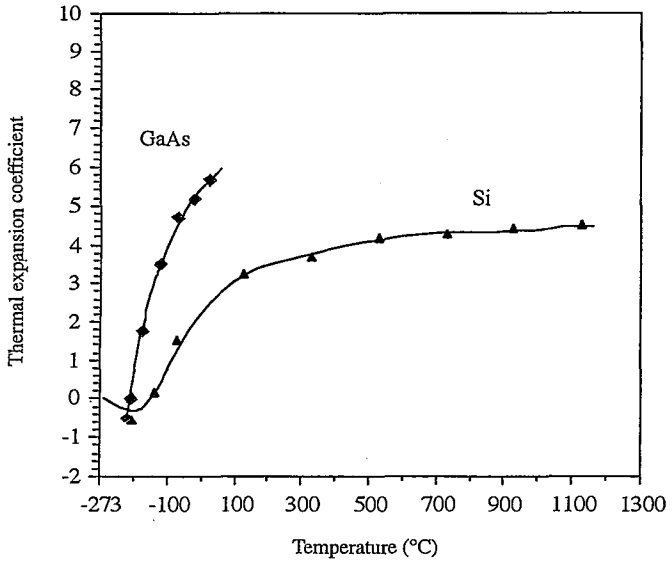

Fig. 9.1 Thermal expansion coefficients of Si and GaAs as a function of temperature. (*a*) Wafer preparation; (*b*) bonding and annealing (650°C in H_2); (*c*) polishing and etch-back; (*d*) final structure.

and the film slips at the bonding interface without generation of dislocations. This fact indicates that the bonding strength is relatively weak.

During annealing at higher temperatures, such as 600°C in hydrogen with a weight on the top of the bonded pair, the inferior oxide on the GaAs is removed by hydrogen and covalent bonds form at the bonding interface similar to those in heteroepitaxial growth (4). The microgaps originated by the surface roughness at the interface vanish owing to the high surface self-diffusion of Ga atoms (5).

The transfer of a small area of a thin GaAs layer to the Si substrate can be realized by an etch-stop method. Figure 9.2 shows the schematic process flow of the transfer process. The GaAs device layer is grown on the etch-stop layer of $Al_{0.8}Ga_{0.2}As$, which is epitaxially grown on the GaAs substrate. After room-temperature bonding and 650°C annealing in hydrogen, the GaAs substrate is lapped down and finally etched in NH_4OH:H_2O_2 solution with a pH value of 8.4 until etching stops at the $Al_{0.8}Ga_{0.2}As$ layer. The etch-stop layer is then selectively removed by buffered HF.

It has been recognized that deposition of a thin SiO_2 (6) or InP layer (4) on the GaAs surface makes the bonding of GaAs wafers to Si much easier. This effect can be explained as follows: a CVD oxide surface has properties similar to a thermal silicon oxide surface, while indium atoms have a higher surface mobility than gallium atoms during the same thermal treatment.

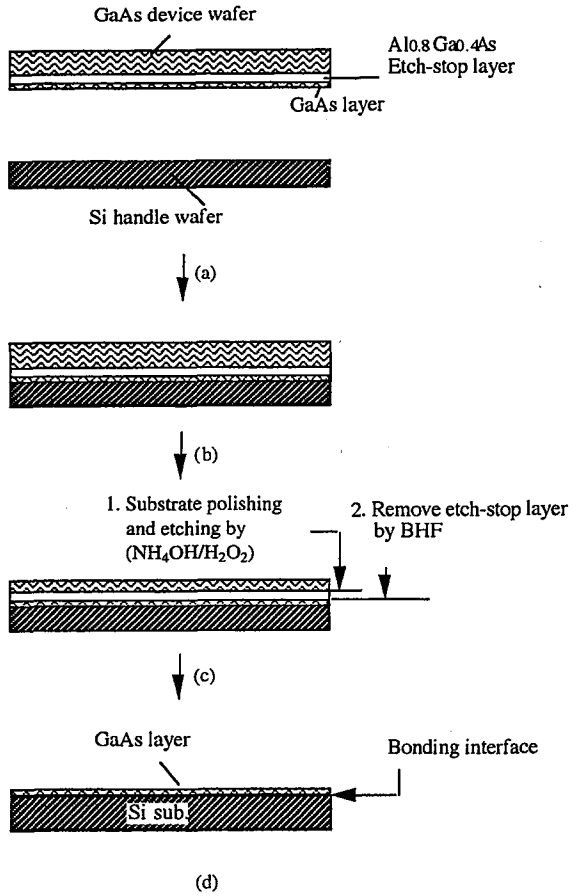

Fig. 9.2 Process flow of fabrication of a GaAs layer on Si by bonding and etch-back. (a) Wafer preparation; (b) bonding and annealing (650°C in H_2); (c) polishing and etch-back; (d) final structure.

Recently, transfer of a thin, single-crystalline (100) GaAs layer from hydrogen-implanted 75 mm (3 in.) diameter wafers onto 75 mm diameter silicon substrate was realized by wafer bonding and layer splitting (7). The process details are given in Section 6.3.2.

9.1.2 InP/Si Bonding

The compound InP is a semiconductor with direct band gap. Some properties of InP related to wafer bonding are also listed in Table. 9.1. Figure 9.3 gives thermal expansion coefficients of InP and Si as a function of temperature. It has been bonded to a Si substrate to integrate InP photonic devices with Si

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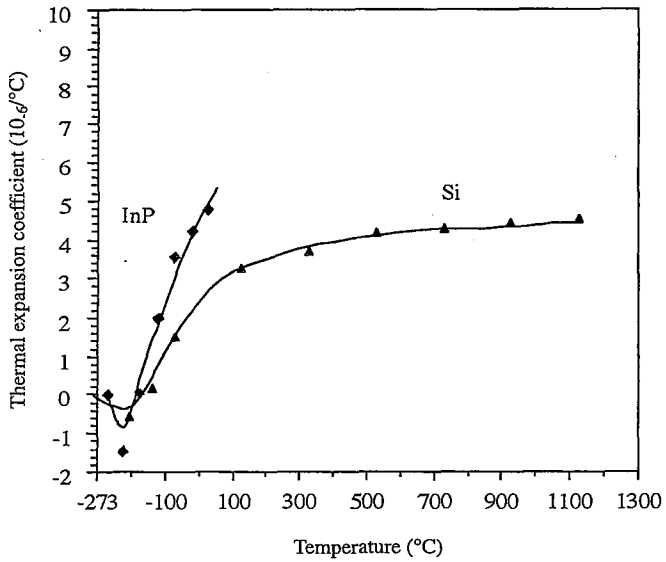

Fig. 9.3 Thermal expansion coefficients of Si and InP as a function of temperature.

electronic circuits on the same chip. The Si substrate is transparent at the wavelength of InP-based lasers, making optical interconnects between devices possible.

Similar to SOI, thin InP layer-on-Si substrate materials are realized by layer transfer using bonding and etch-back as described in Chapter 6. However, room-temperature bonding is difficult, because, like other III-V compound semiconductors, InP lacks an adequate native oxide. A recent report noted that exposing the III-V compounds, such as AlGaAs, to water vapor in a furnace at 400–425°C for 1 h can produce ~ 0.2 μm stable native oxide (8). Bonding experiments on that oxide have yet to be done.

The common practice for InP/Si wafer bonding (3, 9) is to start with epitaxial growth of an ~ 0.2-μm thick etch-stop layer of n^+-InGaAs and a device layer on the InP substrate (Fig. 9.4*a*). Next, the InP wafer is cleaned in H_2SO_4:H_2O_2:H_2O (3:1:1) solution followed by a dip in dilute HF, which removes the poor-quality native oxide, resulting in a hydrophilic InP surface. The Si wafers are cleaned in RCA solution and dipped in HF to remove the native oxide. The room-temperature bonding is usually not spontaneous, probably because of the high surface roughness of the InP surface. An external pressure of about 4 kg/cm^2 is required to press the InP and the Si wafers together. The bonded pair is annealed in hydrogen at 550°C for

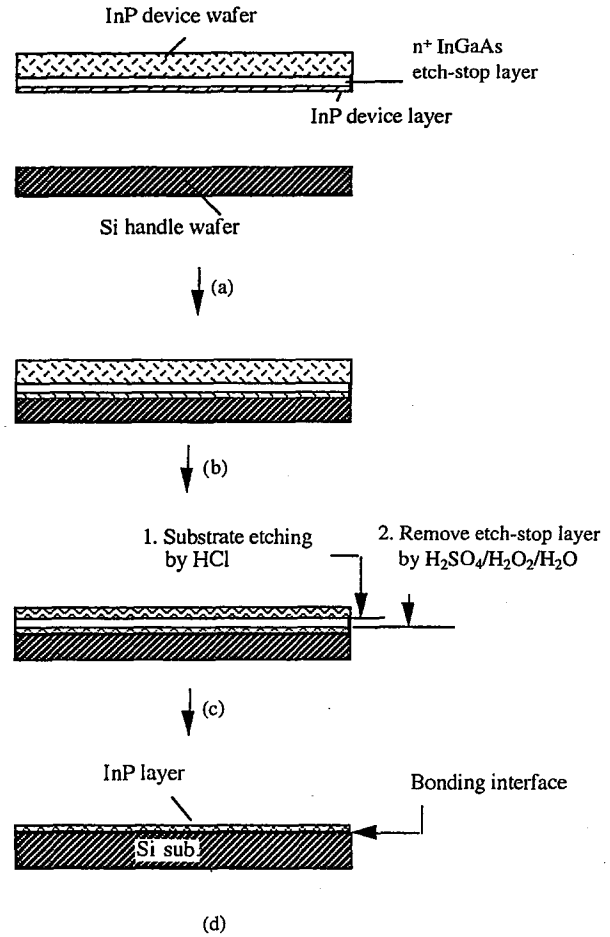

Fig. 9.4 Process flow of by bonding and etch-back. (*a*) Wafer preparation; (*b*) bonding and annealing (550°C in H_2); (*c*) etch-back; (*d*) final structure.

30 min with a weight on the top of the pair to produce a pressure of about 30 g/cm^2 (Fig. 9.4 *b*). For small InP samples up to 5×10 mm^2 in size with a thickness of 350 μm and a 300-μm thick Si substrate, the bonding strength increases with annealing temperature. Strong bonds at the InP/Si interface were found to be formed after annealing at 400°C with a ~ 50 Å thick amorphous oxide layer (9) which disappears at 650–700°C due to removal of the oxide from the interface by hydrogen. At these temperatures, the high surface mobility of In atoms which fill up the microgaps at the interface leads to a complete bond. However, threading dislocations are usually observed

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after annealing at temperatures higher than 550°C owing to the difference in thermal expansion coefficients. Therefore, the optimized annealing temperature is ~550°C. The InP substrate is removed by HCl etching that stops at the n^+-InGaAs etch-stop layer, which is then selectively removed by a H_2SO_4:H_2O_2:H_2O (3:1:1) solution (Fig. 9.4 *c*). The InP device layer is finally transferred onto the Si substrate (Fig. 9.4 *d*).

When transferring an InP layer onto a Si substrate, the 85% difference in their thermal expansion coefficients often causes cracking of the InP film during the thinning process. Low-temperature adhesive bonding (such as wax) (8) technology can be used instead to overcome the problem. A low-temperature direct bonding approach appears to be more desirable, but has yet to be developed.

9.1.3 Quartz Crystal/Si Bonding

Combining crystalline quartz and silicon on the same chip is attractive because it can lead to the integration of electroacoustic devices such as quartz crystal resonators with silicon oscillators and filters for mobile communication systems (10). Quartz crystal resonators have high Q-values combined with small temperature coefficients. The process of bonding quartz crystal to silicon is similar to that of bonding oxidized silicon wafers except that a much lower annealing temperature—between 300 and 450°C—is used to accommodate the large difference in their thermal expansion coefficients (AT-cut quartz crystal: 14.3×10^{-6}, Si: 4.9×10^{-6} at 300°C). As described in Chapter 5, a low-temperature bonding technology can be used for the quartz crystal/Si bonding. After annealing, the quartz crystal of the pair is mechanically thinned to the desired thickness (e.g., 15 μm), to fabricate a resonator.

9.1.4 Si/Quartz Glass Bonding

High quality quartz glass (synthetic or fused quartz) wafers are commercially available. High carrier mobility in single-crystalline Si films on an insulating quartz glass substrate (SOQ) allows microwave devices to be realized. The use of quartz as an optically transparent substrate is also very attractive in image sensors, electroluminescence displays, solar cells, and optical waveguides. The integration of an active pixel matrix with peripheral circuits on the same SOQ substrate would reduce interconnections drastically and increase operation speed for high-resolution and high-frequency liquid-crystal displays. Single-crystalline Si films with thicknesses of 0.5-2 μm (11) and also 2000 Å on thermally mismatched quartz substrates have been fabricated by a wafer-bonding approach (12). Some important properties of quartz glass (SiO_2) are listed in Table 9.1. Figure 9.5 shows the thermal expansion coefficients of quartz glass and silicon as a function of temperature.

To avoid debonding of the severely thermally mismatched Si/quartz pairs during annealing, the temperature difference between initial bonding and

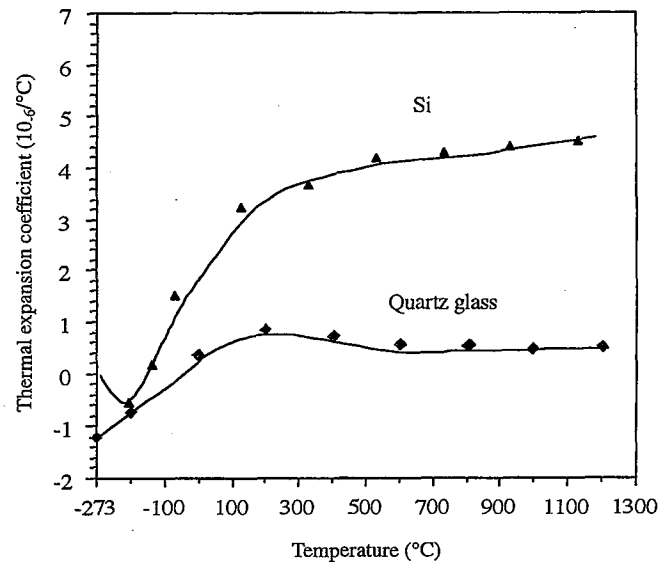

Fig. 9.5 Thermal expansion coefficients of Si and fused quartz as a function of temperature.

annealing should be as small as possible. In this respect, initial bonding at a temperature T_i higher than room temperature T_r will help to reduce the shear and peeling stresses at the interface at annealing temperature T_a. To minimize the thermal stresses in the bonded pair at room temperature as well as at T_a, the optimal temperature for initial bonding T_i should be

$$T_i = \frac{1}{2}(T_a - T_r) + T_r \tag{9.1}$$

Based on low-temperature silicon wafer bonding results (13) in this study, T_a has been determined to be 150°C. Therefore, T_i = 86.5°C is most desirable. Although there is a stress present in the contacting pairs when they are cooled to room temperature, this hot-bonding schedule effectively alleviates the stress in the pairs during annealing at 150°C and prevents debonding. Moreover, the bonded pairs are in an almost stress-free state during 75°C KOH etching which effectively reduces the possibility of KOH penetration into the bonding interface.

Multitemperature (maximum 150°C) consecutive annealing with 1°C/min ramping rate has been adopted to strengthen the bond and to prevent debonding at the edge of the bonded pairs during annealing and etching where thermal shear and peeling stresses are maximum. Final etching by

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EDP or TMAH effectively reduces the peeling failure of the highly stressed thinned Si layer mainly because of a reduced lateral oxide etching rate along the interface.

As discussed in Section 6.3.3, single-crystal silicon thin layers can be transferred onto quartz wafers by wafer bonding and B + H coimplanted silicon layer splitting at temperatures around 200°C. No excessive lapping or etching to remove most of the silicon substrate is required for transferring the thin silicon layers. The quartz wafers as well as the silicon wafers are perfectly preserved during splitting owing to the low thermal stresses involved in the low-temperature splitting process.

9.1.5 Si/Glass Bonding

Silicate glass sheets are widely used as a basic material in various products such as flat panel displays. Silicate glass is less expensive than quartz glass and larger sizes are available. Single-crystalline Si layers on glass (SOG) are very attractive for high-resolution and high frequency displays. Formation of thin single-crystalline Si layers on glass by direct bonding has been reported (14, 15). Both BESOI and layer-splitting methods were used. Depending on the extent of mismatch in their thermal expansion coefficients, the annealing temperatures chosen were from 150 to 500°C.

However, a variety of glasses is available, all of which, except quartz glass, have complex compositions, making the glass surface unpredictable after chemical cleaning, or even after storage in air at room temperature, owing to reactions with the moisture in the ambient. The PECVD TEOS [$Si(C_2H_5O)_4$] oxide (PETEOS) can be deposited at low temperature ($\sim$350°C) on the glass to act as the bonding layer as well as the protection layer during etching (16). Using CMP to improve smoothness of the TEOS oxide surface is necessary to achieve an adequate bonding strength for the thinning and etching operations.

For the bonding and etch-back processes, owing to the extremely low etch rate of silicon oxide in TMAH ($\sim$100 Å/h), etchant penetration into the bonding interface during etching can be effectively prevented by using an oxidized Si wafer instead of bare Si in the bonded pair, even though the bonding energy is very low (surface energy of $\sim$350 mJ/m^2).

Interface bubbles develop during annealing at temperatures higher than 300°C at the bonding interface involved with TEOS layers. These bubbles originate from the outgassing of the TEOS oxide. A proper prebonding annealing step can prevent the formation of bubbles during annealing.

9.1.6 Si/Sapphire Bonding

Sapphire is an electrical insulator and has a much higher thermal conductivity than quartz or glass. It is therefore useful in preparation of bulk-quality thin, single crystalline Si layers on sapphire (SOS) for such applications as high-power microwave monolithic integrated circuits and radiation-hard devices (17, 18). Some important properties of sapphire are listed in Table 9.1.

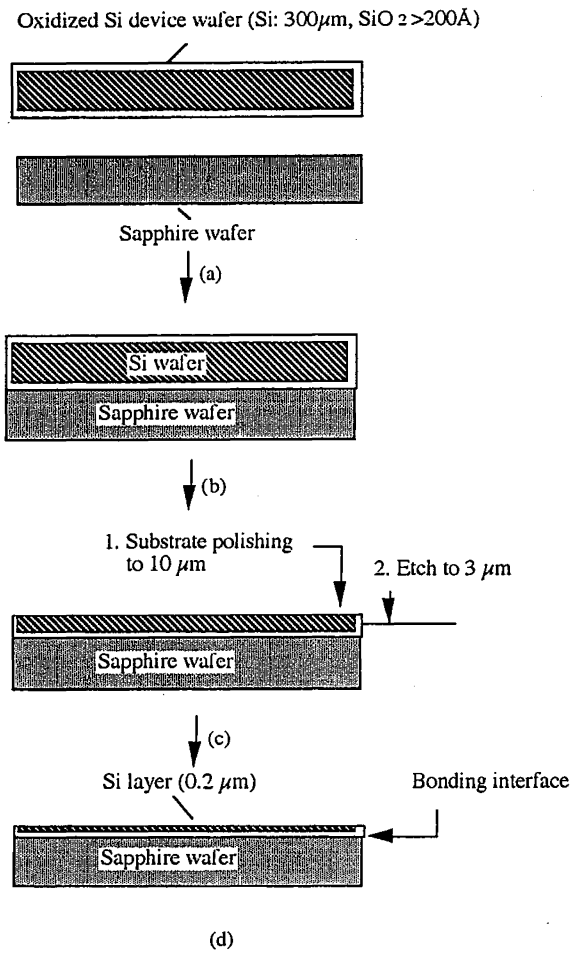

Fig. 9.6 Process flow of fabrication of a Si layer on sapphire by bonding and etch-back. (*a*) Wafer preparation; (*b*) bonding and annealing (270°C); (*c*) polishing and etch-back (KOH); (*d*) final polishing.

An SOS bonding process was suggested as shown in Fig. 6 (16). A 300-μm thick silicon wafer covered with 200 Å thermal oxide was bonded to a $(1\bar{1}02)$-oriented sapphire wafer. The thinner silicon wafer had to be used because of a large difference in the thermal expansion coefficients. To avoid cracking the silicon, the maximum annealing temperature was 270°C. Since silicon oxide has an open structure which can absorb excess gases, a minimum thickness of oxide on the silicon wafer of 200 Å was required to prevent interface bubble generation during annealing. The silicon wafer was then mechanically thinned to 10 μm and etched in KOH to 3 μm followed by

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annealing at 450°C for 2 h. Finally, the silicon layer was polished to the desired thickness. The silicon layer had to be thinner than 0.2 μm to prevent the formation of thermal misfit dislocations during 900°C annealing.

Single-crystal silicon thin layers can also be transferred onto sapphire wafers by wafer bonding and B + H coimplanted silicon layer splitting at temperatures around 180°C, as discussed in Section 6.3.3. In this case, no excessive lapping or etching to remove most of the silicon substrate is required for transferring the thin silicon layers and the split-off silicon wafer can be reused after proper polishing.

9.1.7 SiC on Insulator

The SiC technology provides the possibility of realizing electronic devices that are able to operate at extreme conditions in terms of temperature, speed, power, and radiation. In addition, since the lattice mismatch of (0001) GaN (basal-plane lattice constant = 3.189 Å) to (0001) 6H-SiC (3.080 Å) is only 3.4% compared to ~14% to (0001) c-plane sapphire (2.73 Å), SiC has also become an attractive alternative to sapphire as a substrate in the epitaxial growth of GaN layers for the development of high intensity GaN-based blue-light-emitting diodes and lasers.

One obstacle to the use of bulk SiC single crystals is the extremely high price. The active layers of many SiC devices are only a few microns thick and the epitaxial growth of GaN layers requires only a surface SiC layer on an appropriate substrate. Therefore, it would significantly reduce the cost, as well as allow much wider application, if a technology could be found for fabricating a thin, single-crystalline SiC layer on an inexpensive substrate such as silicon, sapphire (which is more than 10 times cheaper than SiC), or glass, which is transparent to visible light and one of the cheapest possible substrate materials.

There are three approaches to realizing single-crystalline SiC on an insulator, such as oxidized silicon: (1) SiC layers grown by CVD on silicon and subsequent transfer onto oxidized silicon (19), as described in Section 6.3.1.4; (2) direct carbonization conversion of SOI substrates (20); (3) SiC layer transfer by wafer bonding and hydrogen-implanted SiC layer splitting (21, 22). The SiC layers prepared by the first two methods consist of 3C-SiC, which is not always a favorite polytype for device applications. Moreover, the SiC layers still suffer from a high density of defects (up to $10^7/cm^2$) due to a nearly 20% lattice mismatch with silicon. The third approach is more promising because the quality of the 6H- or 4H-SiC layers should resemble that of the corresponding bulk single-crystalline SiC wafers. Thus far, SiC wafers are only available with diameters up to 2 in. (50 mm). Transfer of 2 in. or smaller SiC layers onto commonly used silicon wafers with a larger diameter allows access to state-of-the art silicon processing lines to fabricate SiC devices.

Owing to the hardness of SiC, surface finishing of SiC wafers close to that of silicon has not yet been achieved and the typical Root Mean Square (RMS) roughness of SiC wafers is ~20 Å. The roughness of SiC wafers is adequate for anodic bonding to glass. However, for direct bonding, the SiC wafers have to be covered with a bonding layer such as CVD oxide or polycrystalline silicon, which can be polished to a surface smoothness of better than 5 Å.

Single-crystalline 6H-SiC wafers with 35 mm in diameter which were implanted by H^+ at 100 keV with 8.0×10^{16} ions/cm^2 were bonded to 100-mm diameter CVD oxide-deposited silicon wafers. The SiC layers were then transferred onto the silicon substrate at 1000°C (21). The transfer of single-crystalline 6H-SiC layers from SiC wafers implanted with H_2^+ at 160 keV with a dose of 5.0×10^{16} ions/cm^2 onto a high-temperature (800°C) glass by anodic bonding (560°C, 1000 V) and subsequent layer splitting at 725°C was also demonstrated (22).

9.2 BONDING LAYERS FOR DIRECT BONDING OF DISSIMILAR MATERIALS

As discussed in Section 2.1, for successful room-temperature bonding, the basic requirements for bonding surfaces is that they are sufficiently clean, smooth, flat, and reactive. These conditions are not always satisfied by bonding materials other than silicon wafers. For instance, generally high-quality surface oxides of III-V compound semiconductors are not available. Their bonding with Si or with themselves is usually done by either depositing a bonding layer on their surfaces or totally removing their original oxide. Since the surface-polishing technology for III-V materials is not as advanced as that of Si, a high-temperature annealing in hydrogen with a weight on the bonding pair is needed to achieve strong covalent bonds at the interface assisted by surface-atomic diffusion process. Bonding layers for direct bonding of materials whose surfaces are not favorable for bonding fall into three categories: (1) insulators (e.g., CVD SiO_2, Si_3N_4, and AlN), (2) semiconductors (e.g., polysilicon and InP), and (3) conductors (TiN and silicides).

TABLE 9.2 Bonding Layers and Their Applications in Direct Wafer Bonding

Bonding Material	Reason for a Bonding Layer	Bonding Layer	Bonded Pair	Ref.
Glass	Unstable Surface	PETEOS SiO_2	Si/glass	16
SiC	Rough surface	Thermal SiO_2	SiC/Si	19
Oxidized and grooved Si	Uneven surface topography	Polysilicon	Si/grooved Si	23
Ge	Inferior oxide	Polysilicon	Ge/SiO_2	6
GaAs	Inferior oxide	CVD SiO_2	GaAs/Si	6
InP	Inferior oxide	CVD SiO_2	InP/Si	6
GaAs	Inferior oxide	CVD Si_3N_4	GaAs/Si	24

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Table 9.2 lists some application examples of bonding layers in direct wafer bonding. The selection of bonding material depends on the specific applications. Since Si and SiO_2 are the most mature bonding materials and are compatible to VLSI technology, SiO_2 and polysilicon have become the most favorable materials for bonding layers in direct wafer bonding technology.

9.2.1 CVD Silicon Oxide

Because of its chemical similarity, CVD silicon oxide direct bonding is expected to be similar to the well-known thermal oxide bonding, making it a desirable bonding layer for materials whose surfaces or surface topographies are not favorable for bonding. Chemical vapor deposition oxide bonding has been reported for preparing small area SOI islands by selective polishing (25) and, for InP/SiO_2 (24), GaAs/Si and InP/Si (24), and Si/glass bonding (16).

The CVD of SiO_2 is usually performed at relatively low temperatures (e.g., < 450°C), which is desirable for bonding materials whose dissociation temperature or thermal budget is low. Silane and oxygen can react at low temperatures (typically 400–450°C) to form oxide, but this oxide is not stoichiometric and has a low electric breakdown field ($\sim 6 \times 10^6$ V/cm as compared to 1.2×10^7 V/cm for thermal oxide):

$$SiH4 + O_2 \longrightarrow SiO_2 + 2H_2 \qquad (9.2)$$

The CVD oxide generally has a rougher surface than thermal oxide and prebonding CMP polishing is usually required. Although low-temperature (350°C), plasma-enhanced CVD TEOS [$Si(C_2H_5O)_4$] oxide (PETEOS) also does not have the stoichiometric composition of thermal oxide, this oxide and the related CMP are rapidly becoming widely used for the planarization process in multilevel interconnects in VLSI circuits owing to excellent uniformity and step coverage:

$$Si(C_2H_5O)_4 + 12O_2 \longrightarrow SiO_2 + 8CO_2 + 10H_2O \qquad (9.3)$$

Therefore, using PETEOS oxide as a bonding layer is compatible with VLSI technology requirements. The oxide contains Si-H, Si-OH, and some other gases. A prebonding heat treatment is required to reduce the concentration of those impurities to avoid bubble formation at the bonding interface of bonded pairs during annealing following room-temperature bonding.

If a high temperature is allowed for the bonding materials, the use of a thermal oxide as a bonding layer is preferred. The SiC wafer bonding can serve as an example (19)—the surface of a SiC layer deposited on silicon was first oxidized and then bonded to an oxidized silicon substrate. After etch-back, the SiC layer was transferred onto an oxidized Si substrate.

TABLE 9.3 Some Important Properties of Polysilicon

Properties	Polysilicon
Refractive index (at 0.6 μm)	4.1 (poly); 4.5 (amorphous)
Dopant concentration (cm^{-3})	Up to 10^{20}–10^{21}
Electron mobility (cm^2/V-s)	30–40
Density (g/cm^3)	2.3
Thermal expansion coefficient (K^{-1})	2.0×10^{-6}
Oxide breakdown field (V/cm)	$\sim$ 4-5 $\times 10^6$
Temperature coefficient of resistance (K^{-1})	1×10^{-3}
Average diameter of as-deposited grains	0.03–0.3 μm
Thermal conductivity (W/cm.K)	0.2 (p-type); 0.3 (n-tye) in CMOS

9.2.2 CVD Polysilicon

Polysilicon can be deposited on a substrate at around 600°C by the pyrolitic decomposition of silane at low pressure (0.2–1.0 Torr):

$$SiH_4 \longrightarrow Si + 2H_2 \qquad (9.4)$$

Polysilicon is composed of many small crystallites termed grains. The grains increase in size with annealing temperature. When the deposition temperature is below 575°C, the Si film is amorphous. The amorphous film can recrystallize on further annealing above 600°C. Amorphous Si has a smoother surface than polysilicon. Some important properties of polysilicon are listed in Table 9.3.

The main challenge for a successful polysilicon bonding is to improve the surface smoothness of polysilicon from a RMS roughness of > 1000 Å to a few angstroms by CMP. A proper CMP technology allows the improvement of the polysilicon surface smoothness required for bonding. Polysilicon as a bonding layer, as well as a groove-filling material, has been employed in bonding of a Si wafer to an oxidized and grooved Si wafer for dielectric isolation in high-voltage IC fabrication (23). Polysilicon has also been adopted as a bonding layer for Ge wafers to allow bonding to oxidized Si wafers (6).

Since a polysilicon layer constitutes a conductive layer with a reasonable thermal conductivity, it is expected that for bonding pairs in which a good electric and thermal conductivity are required at the bonding interface, polysilicon is one of the most promising materials of choice for the bonding layer.

9.2.3 CVD Silicon Nitride

Chemical vapor deposition silicon nitride (Si_3N_4) layers are commonly used in VLSI devices as passivation layers because of their impermeability to water and other impurities, or as a mask layer preventing oxidation of the

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underlying silicon. Silicon nitride can be deposited by reacting silane or dichlorosilane and ammonia:

$$SiH_4 + 4NH_3 \longrightarrow Si_3N_4 + 12H_2 \quad (9.5)$$

at 700–900°C at atmospheric pressure or

$$3SiCl_2H_2 + 4NH_3 \longrightarrow Si_3N_4 + 6HCl + 6H_2 \quad (9.6)$$

at 700–800°C at low pressure (LPCVD). Plasma-enhanced CVD (PECVD) silicon nitride can be produced from the reaction of Eq. (9.5) at 250–350°C or from silane and nitrogen at 300–400°C:

$$2SiH_4 + N_2 \longrightarrow 2SiNH + 3H_2 \quad (9.7)$$

The PECVD silicon nitride films are not stoichiometric and contain a large amount of hydrogen which is bonded to silicon as Si—H or to nitrogen as N—H. The hydrogen and nitrogen can be released during annealing.

Some important properties of LPCVD and PECVD silicon nitride are listed in Table 9.4.

The PECVD silicon nitride has been employed as a bonding layer for GaAs to bond to silicon (24). The GaAs wafer covered with 300°C PECVD-deposited nitride layer was cleaned by a modified RCA1 solution (NH_4OH was reduced to 25% of the standard value), followed by a 10-sec dip in 1% HF. The surface is terminated by N—H groups which are polarized and therefore render the surface hydrophilic. Since polymerization of Si—N—H groups across the two bonding surfaces to form strong Si—N—Si bonds can be realized at low temperatures (90–300°C), PECVD silicon nitride layer can be used as a bonding layer for GaAs or other materials which have low dissociation temperatures or will show other undesirable changes at high temperatures.

TABLE 9.4 Some Important Properties of Silicon Nitride

Properties	LPCVD	PECVD
Deposition temperature (°C)	700–900	250–350
Composition	Si_3N_4	$Si_xN_y(x:y = 0.8–1.2)$
Atom % H	4–8	20–25
Density (g/cm^3)	2.9–3.1	2.4–2.8
Thermal expansion coefficient (K^{-1})	4×10^{-6}	$(4–7) \times 10^{-6}$
Refractive index	2.01	1.8–2.6
Dielectric constant	6–7	6–9
Breakdown field (V/cm)	10^7	6×10^6
Stress (10^9 dyne/cm^2)	10 (tensile)	2 (compressive)–5 (tensile)
Energy gap (eV)	5	4–5

Proper deposition conditions must be established to reduce the stresses (especially tensile stresses) and to avoid cracking of the nitride film. The post-bonding annealing temperature should be kept below 300°C to prevent hydrogen outgassing.

9.2.4 CVD InP and Other Materials

As discussed in Sections 9.1.1 and 9.1.2, indium atoms have a high surface mobility during heat treatment at moderate temperatures (450–750°C). Therefore, a CVD thin InP layer (~ 50–1200 Å) may be used as a bonding layer for GaAs (6), GaN (27), $Gd_3Ga_5O_{12}$ (28), or other materials.

The main consideration when using InP bonding layers are: (1) The low-quality oxide on the InP layer should be removed. If the bonding interface needs to be conductive, the oxide on the mating wafer should also be stripped. (2) Annealing should be performed at temperatures higher than 450°C in hydrogen to further clean the bonding surfaces. (3) An external pressure should be applied if the bonding surfaces are not smooth enough.

There are some other materials for buried layers in bonded pairs that are not used to help realize room-temperature bonding but rather for enhancing performance of the bonded pairs. These materials include AlN (29) as a highly thermally conductive insulator, metal silicides (WSi_2, $CoSi_2$, $TiSi_2$) and TiN (30), and C_{60} (31). We discuss applications of these buried layers in Chapter 11.

A layer with a low melting, softening, or diffusion temperature, such as a glass, polymer, or palladium layer, or a metal layer whose eutectic temperature with the bonding substrate is low, may be used as an intermediate layer for low-temperature bonding. However, these approaches are not considered as direct bonding methods within the context of this book. Therefore, we do not discuss them in any detail.

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10

Bonding of Structured Wafers

Wafer bonding is not only a technology allowing new or improved material combinations, but also a powerful method for the fabrication of unique devices and structures. Examples of applications of wafer bonding in VLSI, power devices, micromechanics, and optoelectronics are described in the next two chapters. In many cases, bonding of patterned or structured wafers is essential.

10.1 DESIGN CONSIDERATIONS FOR PATTERNED WAFERS

As discussed in Chapter 2, the attraction forces between two bonding wafers involve mainly short-range van der Waals intermolecular forces. Therefore, a sufficient surface density of bonding species and an adequate smoothness of the bonding surfaces are mandatory for bonding structured wafers of any thickness.

The basic equations for predicting the gap closing between bonding wafers caused by wafer surface waviness was described in Chapter 3. Since the patterns on mating wafers sometimes can be regarded as equivalent to surface flatness variations, the same equations may also serve as a guideline for the design of pattern dimensions to avoid closing of the gaps, which should remain open for the specific applications considered, by the bonding process. The most useful equations are listed again in Table 10.1 where $2R$, $2h$, and t_w are gap extension, gap height, and wafer thickness, respectively, E is Young's modulus, $E' = E/(1 - \nu^2)$, ν is the Poisson ratio, and γ is the average surface energy, $1/2(\gamma_1 + \gamma_2)$, in the case of bonding of two different wafers.

The following is an example of the application of these equations to the design of pattern dimensions on structured wafers. In the study (1), 50-mm (3-in.) diameter, (100) $\pm 0.5°$, 0.25-mm thick, double-side polished p- or n-Si wafers were used. In each bonding pair, a bare Si wafer was bonded to a patterned Si wafer. The patterned wafers were prepared such that an array of 1×1 mm^2 square oxide islands with a nearest neighbor spacing of 2 mm were present on the Si wafer surface. The thickness (height) of the oxide islands, H, on a given wafer was constant. Five thicknesses of oxide islands

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TABLE 10.1 Useful Equations for Structured Wafer Bonding

Conditions	Equation for Avoiding Gap Closing
(1) Two identical wafers $R \gg h$, $R > 2t_w$	$h > \dfrac{R^2}{\sqrt{\frac{2}{3}E' t_w^3/\gamma}}$
(2) Two different wafers $R \gg h$, $R > R_{crit}$	$h > \dfrac{R^2}{\sqrt{\dfrac{4E'_1 t_{w1}^3 E'_2 t_{w2}^3}{3\gamma(E'_1 t_{w1}^3 + E'_2 t_{w2}^3)}}}$
(3) Two identical wafers $R \gg h$, $R < 2t_w$	$h > 3.5(R\gamma/E')^{1/2}$
(4) Two different wafers $R \gg h$, $R < 2t_w$	$h > 3.5(R\gamma/2)^{1/2}\left(\dfrac{1}{E'_1} + \dfrac{1}{E'_2}\right)^{1/2}$
(5) Change over from (2) to (4) at $R = R_{crit}$	$R_{crit} \cong 2\left(\dfrac{E'_1 + E'_2}{E'_1 t_{w1}^3 + E'_2 t_{w2}^3}\right)^{1/3} t_{w1} t_{w2}$

(0.15, 0.2, 0.3, 0.4, and 0.5 μm) were used for five different wafers. Figures 10.1*a* and *b* are schematic diagrams of a plan view and a cross section of the patterned wafers, respectively. Figure 10.1*c* illustrates the desirable structure after bonding.

It was found that in the room-temperature bonded wafer pairs with oxide island thicknesses of 0.15 and 0.2 μm, the bare Si wafer in each pair was actually bonded to the Si corridors between oxide islands on the mating wafer, instead of forming gaps evenly spaced with a distance H between the two bonded wafers, as shown in Fig. 10.1*c*. In contrast, the collapse effect was not observed in the room-temperature bonded pairs in which the heights of the oxide islands were 0.3, 0.4, and 0.5 μm. A clear contrast between a "collapsed" bonded pair and a "normal" bonded pair can be seen from Fig. 10.2*a* and *b*, respectively, which are IR images of the room-temperature bonded pairs in which the height of the oxide islands is 0.2 and 0.4 μm, respectively. The cross-sectional diagram of the collapsed wafer pair is schematically shown in Fig. 10.2*c*.

If we neglect the flatness variation of the original Si wafers, the bonding of a bare Si wafer to a Si wafer with oxide islands of thickness H and spacing of $2R$ may be approximately equivalent to the wafer bonding of two wavy Si surfaces with resulting interface gaps of a lateral extension $2R$ and a height $2h = H$ (see Fig. 10.1*c*). Here, R is much larger than both h and the wafer thickness, t_w, and therefore Eq. (1) in Table 10.1 may be used. Based on the

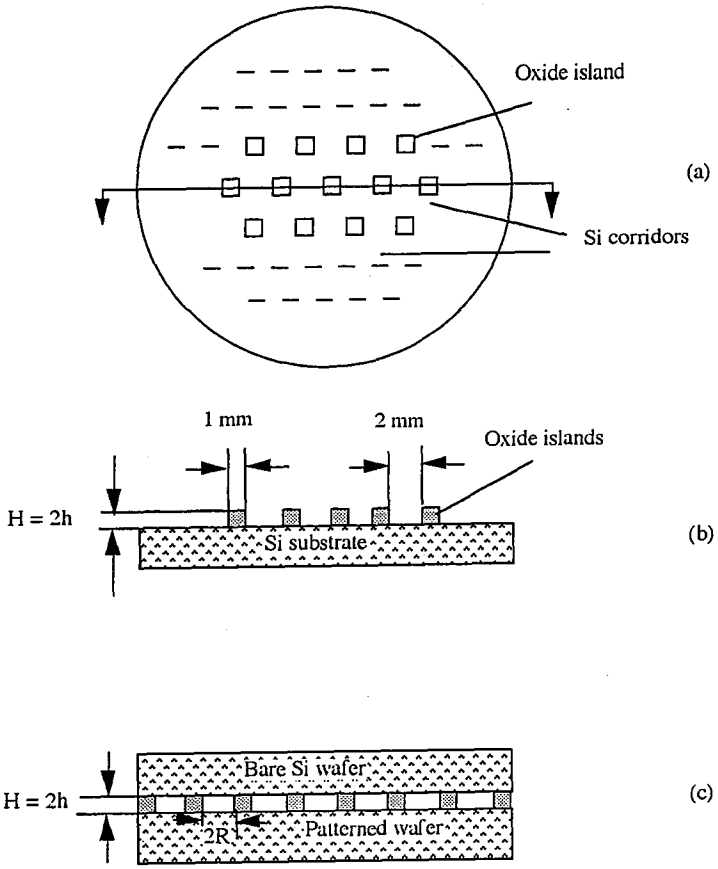

Fig. 10.1 Schematics of (*a*) plan view and (*b*) cross section of a patterned wafer and (*c*) expected bonded structure.

measured surface energy of room-temperature bonded bare Si/oxidized Si pairs, the surface energy g of the room-temperature bonded Si to oxide islands pairs is assumed to be 50–70 mJ/m^2. Although the actual analysis is more complex since two different materials, Si and SiO_2, are involved in the system, Eq. (1) can still be employed to estimate the possibility of the gap closing. Figure 10.3 shows the region of oxide island parameters ($2R$ and H) for which gaps can be closed by the room-temperature bonding process at a given silicon wafer thickness. The figure indicates that the collapse effect will occur in the room-temperature bonded 0.25-mm thick water pairs ($2R = 2$ mm) for oxide island heights of 0.15 and 0.2 μm, while the interface gaps defined by the oxide islands with heights of 0.3, 0.4, and 0.5 μm will remain open. The calculations are in agreement with our experiments, suggesting

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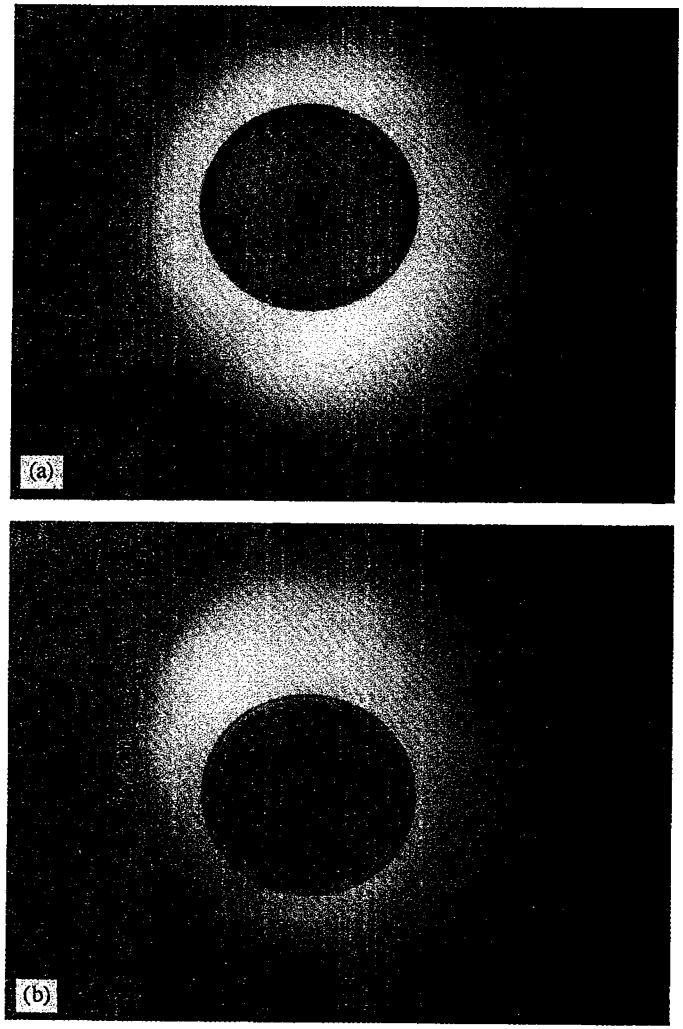
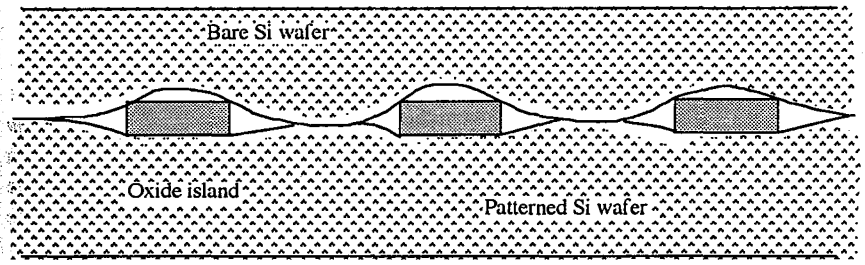


Fig. 10.2 Infrared photos of RT-bonded Si pair with oxide island height of (*a*) 0.2 μm and (*b*) 0.4 μm. In contrast to *b*, the white areas in *a* indicate that the bare Si wafer has bonded to the Si corridors between oxide islands of the patterned wafer.

that Eqs. (1)–(4) in Table 10.1 can serve as design guidelines for patterned-wafer bonding.

This effect can be employed to measure the bonding strength over the whole wafer area of bonded pairs (2). After thermal oxidation, photolithography steps were used to create a sequence of narrow parallel thermal oxide lines with varying spacings between the lines across the silicon wafer. The



(c)

Fig. 10.2 (*Continued*) (*c*) Schematic cross section of the 0.2-μm pair after room-temperature bonding.

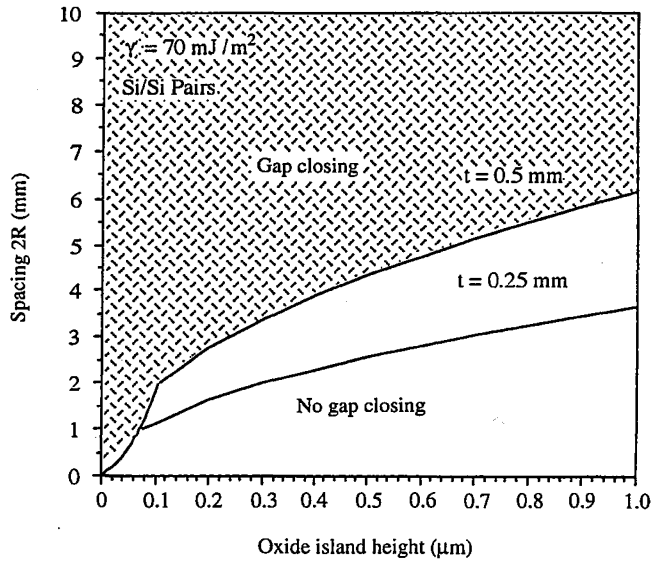


Fig. 10.3 Design curves for pattern dimensions on bonding Si wafers of thickness t_w. The shaded area shows that the interface gaps defined by oxide islands with height H and spacing $2R$ of nearest neighbors will remain after the room-temperature bonding process. The curves are given for two different values of t_w.

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surface energy of the bonding surfaces can be determined by an IR inspection, which indicate that bonding will occur in the location of the pair where the condition relating the line height, line spacing, and wafer thickness is satisfied.

10.2 BONDING OF WAFERS WITH CAVITIES

For micromechanical devices, the formation of sealed cavities is frequently required. Typically, cavities are etched into the surface of the first wafer to a desired depth, followed by bonding a second wafer to the front surface of the first wafer. Often, the second wafer is subsequently thinned back so that the bonded layer is a few microns thick.

During bonding of a silicon wafer with cavities to another silicon wafer in ambient other than high vacuum, gases will be trapped within the sealed cavities. During a subsequent annealing at high temperature, several processes can occur: (1) a reaction between the trapped gases and the silicon inside the cavities may take place, (2) part of the gas may escape from the cavities as the wafers are heated to the annealing temperature, (3) the contaminants on the surfaces of the bonding wafers may desorb, and (4) a plastic deformation may occur if the differential between the pressure in the cavities and the outside pressure increases beyond the yield point of silicon at that temperature.

The inward or outward deflection of the silicon layer over the sealed cavities can be measured with an optical microscope or an optical interferometer system (3). It was found that the silicon layer over cavities bonded in either air or pure oxygen after annealing at 1000°C for 1 h and subsequent cooling to room temperature is deflected into the cavities under atmospheric condition, indicating that the residual pressure is below atmospheric (3, 4). If the wafers are bonded in air (20% oxygen), the initial pressure in the cavities is 1 atm; during annealing at 1000°C for 1 h, the oxygen within the sealed cavities reacts with the silicon and forms SiO_2. This leaves a remaining pressure of approximately 0.8 atm. Wafers bonded in pure oxygen show results close to those bonded in vacuum. If room-temperature bonding is performed in 1 atm pressure of nitrogen, 1 atm is expected as the pressure remaining after annealing. The pressure inside the cavities can be measured as follows: the theory of large deflection of an edge-clamped circular plate can be applied to relate the maximum deflection h at the center of the circular plate to the pressure difference Δp across the plate as (5)

$$h = 0.662\sqrt[3]{\frac{r^4 \Delta p}{Et}} \tag{10.1}$$

where E is Young's modulus, and t and r are the thickness and the radius of the thin circular plate, respectively. The pressure difference Δp between the

atmospheric pressure and the pressure inside the cavities can thus be determined by the measured value of deflection h:

$$\Delta p = \frac{Eh^3 t}{0.29 r^4} \tag{10.2}$$

The reduced residual pressure inside the cavities can also be obtained by differential measurement methods. Two differential techniques are commonly used. The first method determines at which reduced outside pressure at room temperature the silicon layer becomes undeformed. For cases in which the cavities still contain a relatively high percentage of inert gas such as nitrogen, the second technique measures at which elevated temperature the silicon layer over the sealed cavity becomes undeformed ($h = 0$), which indicates that the pressure in the cavity is equal to the outside pressure of 1 atm (4). The differential pressure method is less prone to error since the geometrical parameters of the cavity need not be known to determine the residual pressure in the cavities. Combined measurement methods may also be used for increased accuracy (e.g., on the order of ± 3hPa) (6).

The pressure in the cavities was not always found experimentally to be as predicted. Possible reasons for deviations are as follows (4, 6): (1) If debonding occurs during annealing, the residual pressure will be smaller than expected in the case of nitrogen or air. If the radius of the cavity is limited to less than 3 mm for a typical 0.5-mm thick 4-in. silicon wafer, no debonding will occur since the pressure below 1200°C is not sufficiently high to open a cavity for a surface energy of 80 mJ/m^2. (2) During annealing, hydrocarbons adsorbed at the interface may desorb and be trapped in the cavities, resulting in increased residual pressure in the cavities. (3) Most importantly, hydrogen from the reaction between the water molecules and the silicon at the hydrophilic interface, or release from Si—H bonds at the hydrophobic interface, can diffuse to the cavities, thus leading to an increase in the residual pressure in the cavities. The cavity gas pressure is strongly dependent on the bonded area surrounding each cavity. This effect, described in more detail in Section 5.4.1, is especially undesirable for wafers purposely bonded in high vacuum and designed for absolute pressure sensors. (4) If the pressure in the cavity leads to stresses in the silicon layer exceeding the yield stress of silicon, the silicon layer will be permanently deformed by plastic flow and an outward bow of the layer may result, even if after cooling the residual pressure in the cavity is lower than the outside pressure (2). An application of this effect for a threshold pressure sensor is described in Chapter 11.

10.3 BONDING OF PARTIALLY OR FULLY PROCESSED WAFERS

Wafer-bonding technology can be used to bond partially or fully processed wafers to desired substrates for unique device structures. Examples of such devices are provided in the next two chapters. The major challenges for

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bonding of a processed wafer to a different substrate are: (1) preparing bondable surfaces for nonsilicon materials, (2) reducing thermal stresses in the bonded pair, and (3) limiting annealing temperatures. Generally, nonsilicon wafers have rougher and wavier surfaces than silicon wafers and the surface cleaning and activation technologies for these materials are not as well developed. Using low-temperature CVD SiO_2 or polysilicon on the surfaces of these materials as bonding layers is one to solve the first challenge because the surface can then be flattened and smoothed by conventional CMP technology and the surface cleaned and activated by well-developed silicon-bonding approaches. If glass is the desired bonding substrate, anodic bonding can be adopted because it is more tolerant to the roughness of the bonding surfaces. Since treatment at high temperatures causes undesirable changes and introduces excessive stresses in processed wafers, the application of the low-temperature bonding technologies described in Chapter 5 is essential for the bonding of processed wafers. 'The following is an example of the bonding of processed wafers reported recently (7).

Usually, SOI devices are realized by processing preprepared SOI substrates. In addition to the SOI material fabrication, an optimized SOI device process has to be developed to alleviate stress and wafer-deformation problems. Alternatively, if a processed device layer on a bulk Si substrate can be transferred onto an insulator, the SOI devices may be realized by using the existing mature bulk Si VLSI technology. Wafer direct bonding provides a possible solution to the problem since two dissimilar materials can be bonded with sufficiently high bonding strength after annealing at temperatures lower than the maximum feasible temperature for processed device wafers, that is, 450°C (8). A very strong bond can be achieved even at room temperature when bonding is performed under ultrahigh vacuum conditions (9). Moreover, a wide range of materials can be used as the substrate onto which the device layer is to be transferred by wafer bonding. Using plasma-enhanced CVD TEOS ($Si(C_2H_5O)_4$) oxide (PETEOS) and associated CMP technology, a flat layer on the surface of a processed VLSI bulk Si wafer can be formed for direct bonding. The undoped PETEOS oxide has also been used as a bonding layer for substrates onto which the IC layer is to be transferred and whose surfaces are not favorable for bonding. The PETEOS oxide was deposited on both Si wafers and display-grade glass plates at 350°C. The CMP tools used were a polisher and a single-wafer brush scrubber.

Figure 10.4 shows the surface energy as a function of annealing temperature of a bonded as-deposited TEOS (TEOS/TEOS) pair and a TEOS after CMP and scrubbing (CMP/CMP) pair. It can be seen that CMP significantly improves the bonding quality. The CMP/CMP pair achieves a very high surface energy of 2700 mJ/m^2 after annealing at temperatures as low as 300°C for 100 h, a surface energy that is sufficient for subsequent thinning and etching in the layer-transfer process. As discussed in Section 5.2.1, the maximum surface energy of $\sim$ 4600 mJ/m^2 after 1100°C annealing indicates

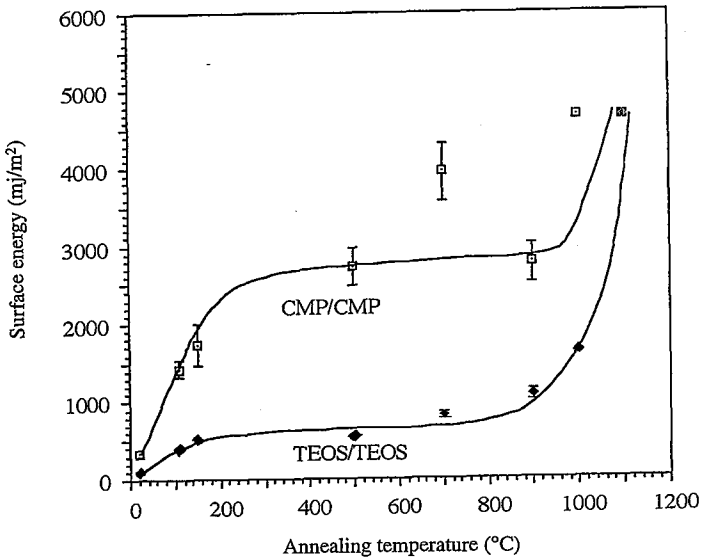

Fig. 10.4 Surface energy as a function of annealing temperature of a bonded as-deposited TEOS (TEOS/TEOS) silicon wafer pair and a silicon wafer pair covered with TEOS and subsequent CMP and scrubbing (CMP/CMP) pair.

that a crack forms inside the bonded oxide layer, not in silicon during the measurement of the surface energy by the crack-opening method.

The PETEOS oxide was also deposited on processed 6-in. VLSI SRAM bulk Si wafers (7). The typical topography height was 1740 Å before CMP and became 120 Å after CMP. The wafers spontaneously bonded to bare Si wafers without any gaps, which is consistent with theoretical predictions based on the measured surface topography.

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11

Mainstream Applications

The flexibility of wafer bonding permits a wide range of applications including, but not limited to, the integration of different materials for optimization of individual functions on the same substrate. Over the last decade, the main driving forces of progress in the area of wafer direct bonding have been its applications in high-quality SOI material fabrication and in the area of silicon-based micromechanics and high-voltage power devices. This chapter focuses on mainstream applications. Emerging applications are the subject of Chapter 12.

11.1 BONDING APPLICATIONS IN VLSI

11.1.1 Competing SOI Technologies

The interest in SOI technology began more than 30 years ago with the demand to increase radiation hardness for applications in space and the nuclear environment (1, 2). However, since SOI devices also circumvent some inherent problems of bulk Si devices associated with junction area, leakage, isolation, and capacitance, SOI became an attractive technology for future generations of mainstream VLSI products. In addition to the DI (dielectric–isolation) technique (3), many approaches to SOI material fabrication were suggested and tested including SOS (silicon-on-sapphire) (4), ZMR (zone-melting-recrystallization) (5), SIMOX (separation by implantation of oxygen), (6) and bonded SOI (7). Table 11.1 provides a comparison of some important properties of bulk silicon and several SOI materials available at the present time.

High-quality ultrathin SOI materials are expected to play a major role in low-voltage and low-power VLSI products. Table 11.2 shows the projected VLSI 8-in. SOI specifications (2).

According to Tables 11.1 and 11.2, only two approaches presently have the potential to meet the SOI requirements for next generation VLSI: bonded SOI and SIMOX. Compared with its main contender, SIMOX (schematically described in Fig. 1.4), wafer bonding offers bulk silicon quality of the SOI layers and thermal oxide properties of the buried oxide layers as well as their

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TABLE 11.1 Comparison of Some Important Properties of 150-mm (6-in.) Diameter Bulk Silicon and Several SOI Materials (2, 8, 9, 10).

Property	Bulk Si	SOS	ZMR	SIMOX	Bonded
Surface roughness (RMS)	~ 1 Å	~ 2 Å	~ 200 Å	~ 3–5 Å	~ 1-2 Å
SOI layer thickness variation	N/A	±10%	±250 Å	±50 Å	±50 Å (depending on thinning procedure)
SOI layer thickness	N/A	0.1–0.2 μm	0.1–2 μm	0.03–0.5 μm	0.05 μm to wafer thickness
Wafer TTV	< 1 μm	8–12 μm	< 3 μm	< 2 μm	< 1.5 μm
BOX thickness	N/A	Up to wafer thickness	Up to several μm	0.05–0.6 μm	From 0 to several micrometers
Bow	< 35 μm	< 60 μm	~ 50 μm	~ 25 μm	< 35 μm
Lifetime	< 150 μsec	< 5 nsec	0.7 μsec	12 μsec	< 150 μsec
Dislocation density (cm^{-2})	< 30	10^8–10^9	10^5 + low-angle grain boundaries	10^5–10^6	< 100

TABLE 11.2 Projected VLSI 300-mm (8-in.) Diameter SOI Specifications

SOI layer	1500 ±75 Å
Surface roughness RMS	< 0.5 Å
Wafer TTV	< 1.5 μm
Defect density	< 0.2 cm^{-2}
BOX pinholes	< 0.1 cm^{-2}
BOX breakdown field	> 10 MV/cm
Interface bubbles	< 0.1 cm^{-2}
SOI layer resistivity	7.5 ±2.5 Ω.cm
Substrate resistivity	7.5 ±2.5 Ω.cm
Surface and silicon metallics	< 1×10^{10} cm^{-2}
Oxygen in SOI layer	12–15 ppma
Edge exclusion	8 mm

interfaces with silicon. In addition, the thicknesses of both the SOI layers and the BOX layers are flexible in bonded SOI. Both technologies presently have difficulty producing 0.1 ± 0.005 μm SOI films in volume at the desired cost of about 2–5 times that of a bulk wafer.

11.1.2 Radiation-Hard SOI Devices

The radiation hardness of the buried oxide strongly influences the hardness of the entire SOI device (11). As discussed previously, preprocessed wafers can be bonded. Therefore, to obtain radiation-hard SOI materials, standard oxide-hardening techniques can be employed to form the thermally grown oxide (which later becomes the BOX in SOI) and Si/SiO_2 interfaces prior to

bonding. The relatively low temperature of the bonding process is also favorable for the radiation hardness. Experimental results suggest (11) that the presence of the SiO_2/SiO_2 bonding interface and associated negative charges do not degrade the radiation-hardness of MOS structures appreciably if process temperatures are kept below 900°C.

It has been found that α-particles with a high energy of a few million electron volts are emitted from IC packaging materials by radioactive elements, such as uranium and thorium atoms, which are present as impurities. Such α-particles can penetrate into the silicon typically in the range of tens of micrometers and cause the generation of electron-hole pairs along the path of the particle. The generated carriers can diffuse in the silicon substrate and reach the devices located at the silicon surface. A 4-MeV α-particle can generate 10^6 electron-hole pairs in silicon, which corresponds to a larger charge than that stored in a typical 16 K DRAM (dynamic random access memory) cell and can cause a change in the state of the cell leading to the random failure of the DRAM. This so-called "soft error" is not associated with physical damages in the device. Since the thin silicon device layer of SOI wafers has a much smaller volume compared with bulk silicon, the number of generated carriers in the SOI layer is much smaller. The electron-hole pairs generated in the bulk of the handle wafer cannot harm the devices in the SOI layer because they are separated by the insulating BOX layer. It was reported that by using 4-μm thick bonded SOI layers, the soft error rate of 64 K DRAMs was reduced by one order of magnitude from that of conventional bulk silicon devices (12). As the SOI layers become thinner, an even lower soft error rate can be expected.

As mentioned previously, only bonded SOI which has a low defect density is adequate for high-performance bipolar transistor fabrication. Experimental results of 1 K ECL RAM (emitter coupled logic random access memory) have shown that, compared with conventional bulk silicon, the soft error rate is reduced by a factor of 400 when bonded SOI material is used. The speed of the integrated circuit has also been found to be 10% faster than that fabricated on a conventional silicon wafer (13).

11.1.3 DRAMs

As VLSI DRAM complexity increases steadily to reach more than 10^7 transistors on each chip and operating frequencies in the giga-Hertz range, the power consumption of each chip, including standby and dynamic power consumptions, has reached the level of a few tens of watts. With various power-management techniques to reduce dynamic power, standby power, which is determined by the leakage current, becomes a relatively important portion of the total power consumption in VLSI chips. Reduction of the leakage current of each transistor is essential because the total leakage current will be multiplied by the number of devices of the chip, which is on the order of 10^7–10^8. Bonded SOI layers have a much lower defect density than SIMOX (~ $10/cm^2$ vs. $10^5/cm^2$). Therefore, lower leakage current and

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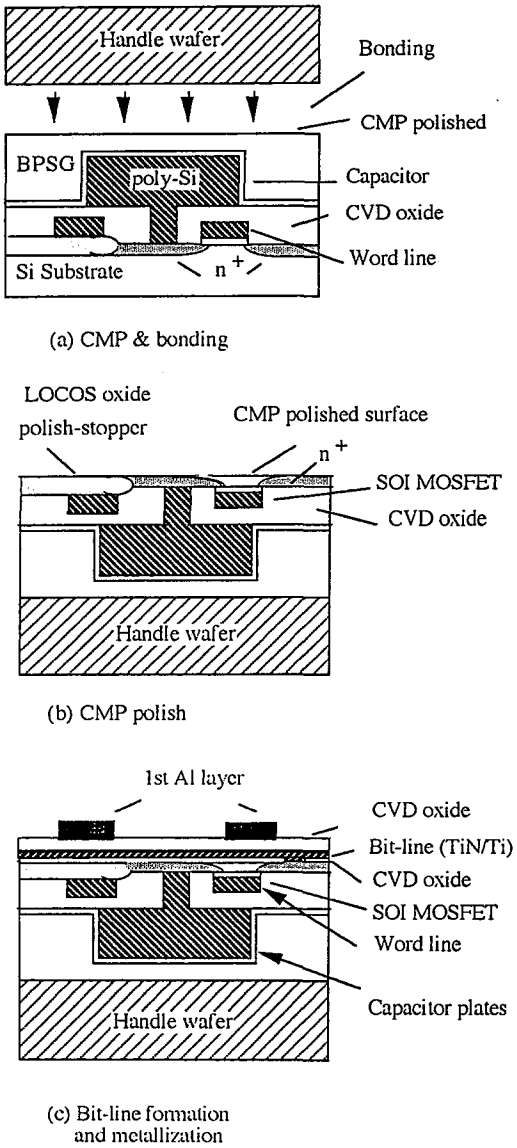

Fig. 11.1 Process flow of a giga-bit DRAM cell structure with a buried storage capacitor (16). (*a*) CMP and bonding; (*b*) CMP polish; (*c*) bit-line formation and metallization.

better VLSI overall performance of bonded SOI as compared to SIMOX may be expected (14).

Bonding technology has been applied to giga-bit MOS DRAMs (15, 16). Giga-bit DRAMs require an extremely small memory cell size ($\sim 0.3\ \mu m^2$), including the MOSFET transistor and the storage capacitor. Low bit-line and word-line capacitances and resistances are also required. An attractive approach for giga-bit DRAMs is to bury the storage capacitor under the MOSFET in the memory cell and, at the same time, keep a small bit-line and word-line parasitic capacitance and resistance. Figure 11.1 shows an example of the process flow of a giga-bit DRAM cell structure with a buried storage capacitor made using wafer bonding (16).

After the fabrication of the MOSFET and the capacitors, CMP is performed on the BPGS (borophosphosilicate glass) top layer of the device wafer. The supporting wafer is then bonded to the polished device wafer and annealed at $\sim 950°C$ (Fig. 11.1*a*). A second CMP is carried out to thin the substrate of the device wafer and the polishing is stopped on the 2200-Å thick LOCOS SiO_2 layer of the chip (Fig. 11.1*b*), resulting in self-aligned SOI areas that are 970 ± 80 Å thick. The bulk MOSFET now has become an SOI MOSFET. The bonded wafer is thermally oxidized to grow 50 Å oxide and 2000 Å CVD oxide is deposited. After opening the contact holes, 500 Å TiN/200 Å Ti is sputtered for the bit-line wiring (Fig. 11.1*c*). This low-resistivity metal is allowed for the bit lines because there are no subsequent high-temperature steps. The sheet resistance and the capacitance of the bit lines are all reduced to half that of conventional structures. The parasitic capacitances of the bit lines are also lowered significantly.

11.1.4 Low-Power, Low-Voltage CMOS

The VLSI chips are continually getting larger and faster, resulting in high power consumption. At the same time, low-power, battery-operated, portable or pocket communication–computer systems are in strong demand. The power consumption of a chip includes dynamic power, P_d ,and standby power, P_s (14):

$$P = P_d + P_s = k_1 C f V^2 + I_s V \tag{11.1}$$

where k_1 is the switching factor, C is the capacitance, f is the operating frequency, V is the power supply voltage, and I_s is the leakage current.

Reduction of power supply voltage without degrading circuit performance becomes an obvious solution. Consequently, the next generation of mainstream VLSI is expected to be low-voltage, low-power, and high-speed CMOS. In addition to reduced soft-error sensitivity, low junction capacitance, and smaller junction area and leakage, various studies comparing SOI and bulk CMOS suggested that ultrathin SOI is a promising candidate for future technology. For bulk Si devices, as supply voltage is reduced, voltage-dependent junction depletion capacitances increase, leading to lower speed.

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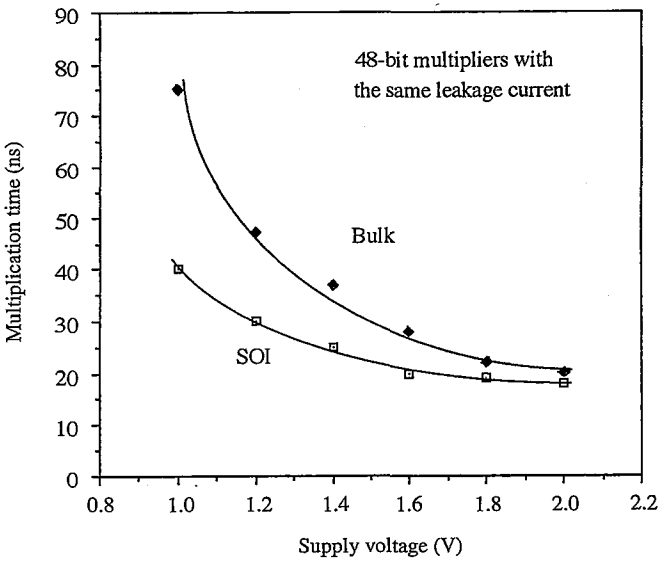

Fig. 11.2 Comparison of 48-bit multiplier performance between SOI and bulk Si using a 0.25 μm CMOS technology (18).

In contrast, for SOI devices, the junctions are essentially bounded by the insulating oxide and thus depletion capacitance is virtually eliminated. The inherent steep subthreshold slopes of SOI devices allow the threshold voltage to be reduced to maintain circuit speed with minimal impact on the standby power. Figure 11.2 illustrates a comparison of SOI and bulk Si 48-bit multiplier performance using a 0.25-μm CMOS technology (17). Some of the differences are (14, 18):

1. For unloaded inverters there is a 3X dynamic power reduction from bulk to SOI for a given gate delay by lowering the power supply voltage.
2. Reducing the power supply from 2.5 to 1.5 V on 64 Kb SRAM bulk Si leads to a 3X power reduction at the price of 70% speed degradation, whereas SOI SRAM achieves a 4X power lowering with only 10% loss of speed.
3. Compared to bulk Si, the speed of microcontrollers using SOI is doubled at sub-1V and the speed-delay product is almost tripled for high density DRAM, SRAM, and frequency dividers.

The leakage current of SIMOX circuits is a major contributor to standby power and the use of bonded SOI could be one of the solutions. Detailed comparisons of bonded SOI and SIMOX in the performance of low-power, low-voltage VLSI CMOS are not yet available.

11.1.5 Body Contacts of SOI MOSFETs

Some of the difficulties associated with SOI MOSFETs, such as the kink effect, single transistor latch-up, low drain breakdown, and back-channel leakage originate from the floating body of MOSFETs since the SOI layer is electrically isolated from the bulk wafer. To eliminate the floating-body effect, the body of MOSFETs must be connected to a fixed potential such as the substrate of the silicon chip. Using the wafer-bonding approach, efficient body-contact schemes can be designed.

An example of the process flow of a body-contact scheme for nMOSFETs is shown in Fig. 11.3 (19). The starting material is a heavily doped p^+ substrate (5×10^{18} cm^{-3}) with a 3-μm thick p^- epitaxial layer (3×10^{15} cm^{-3}). After growth of 250 Å thermal oxide on the p^- epitaxial layer, a 1200-Å silicon nitride layer is deposited. The device-active areas are defined by photolithography. Field areas are dry etched down to the epitaxial layer to a depth of 3500 Å. A second photolithographic step is performed to define the tub areas in the middle of the device-active areas and 3000 Å silicon in the active areas around the tub areas is dry etched off while the field areas are protected. The whole field area is then thermally oxidized to grow 6500 Å oxide. Figure 11.3*a* shows the structure after removal of the nitride and oxide on the top of the tub. A 4000-Å thick LPCVD polysilicon layer is then deposited and boron doped by ion implantation. Layers of 2000 Å LPCVD oxide and 5 μm polysilicon are subsequently deposited. The polysilicon is polished to form a mirror-like surface. The polysilicon surface is then bonded to the handle wafer at 900°C for 1 h (see Fig. 11.3*b*). The p^+ substrate of the device wafer is removed by lapping and selective etching and the p^- epitaxial layer is thinned by polishing using the field oxide as an etch-stop (Fig. 11.3*c*). The nMOSFETs are fabricated on the structure by a conventional process (Fig. 11.3*d*). In these SOI nMOSFETs, the body is connected to the ground via the p^+ polysilicon layer buried under the channel region. To realize the body connect, one extra mask for the tub formation is required. This method can also be adopted to CMOS fabrication.

11.2 BONDING APPLICATIONS IN HIGH-VOLTAGE AND HIGH-POWER DEVICES

Wafer bonding is especially attractive for realizing high-voltage and high-power devices and has been quickly introduced for commercial products. In these applications, two kinds of wafer bonding are adopted: Si/Si and SOI bonding. The former is used to replace the growth of thick epitaxial layers and/or deep diffusion processing steps while the latter is employed for dielectric isolation (DI) between individual devices in high-voltage/high-power ICs. Among the available SOI material technologies, wafer bonding appears to be the most promising option for producing cost-effective DI

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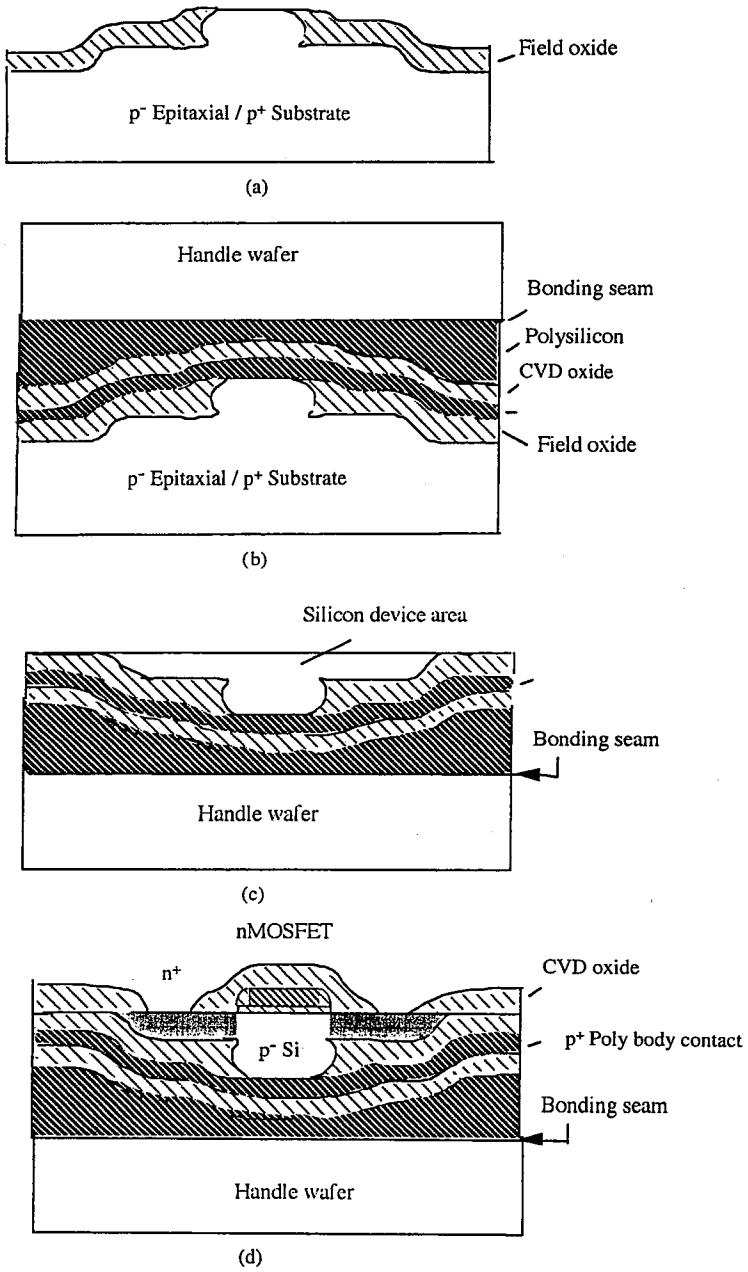

Fig. 11.3 Process flow of a body-contact scheme for nMOSFETs (19). (*a*) Si etch and field oxidation; (*b*) polyoxide-poly dep. and polish; (*c*) Si substrate polish; (*d*) *n*MOSFET fabrication.

structures. In high-voltage and high-power device applications, the buried oxide as well as the silicon layers are relatively thick (>1 μm). The silicon layers are usually in the range of 1.5–100 μm and the thickness uniformity required is on the order of ± 1–2 μm.

11.2.1 Dielectric Isolation

Dielectric isolation (DI) is widely used in analog as well as high-power and high-voltage device integration. Dielectric isolation structures are conventionally produced by thick polysilicon deposition on a grooved, oxidized single-crystal silicon wafer followed by mechanical thinning of the single-crystal wafer to create oxide-isolated silicon islands (tubs) embedded in a polysilicon matrix. The high temperature (~ 1300°C) and long processing time (~ 3 h) required for thick (a few hundred micrometers) polysilicon deposition results in reduced throughput, severe out-diffusion of dopants in buried layers, and wafer warpage.

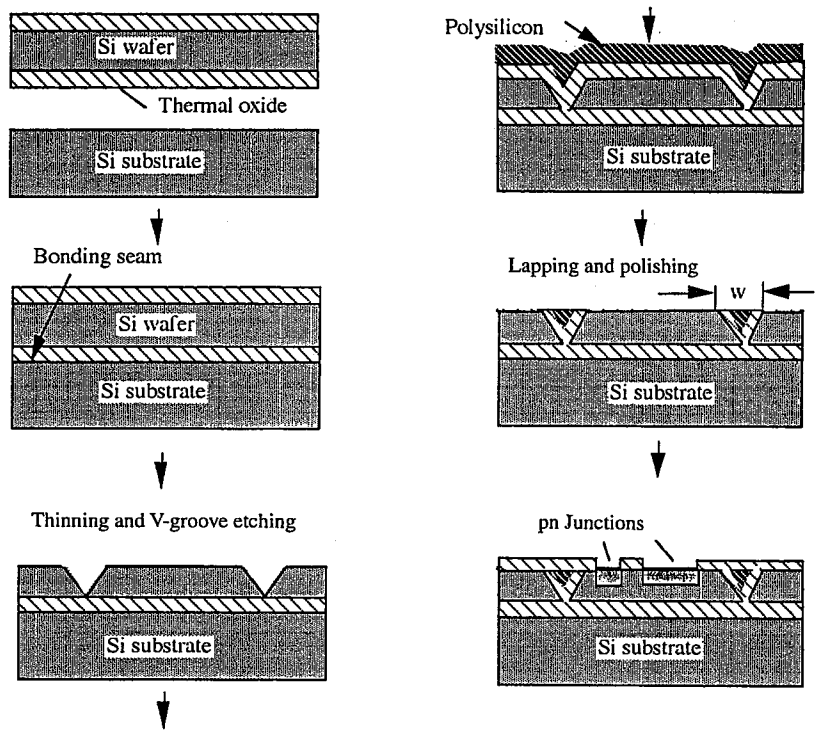

Fig. 11.4 Process flow of "V-groove" dielectric isolation technique (20).

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These drawbacks can be solved by etching V grooves in the silicon layer of a bonded SOI wafer, followed by polysilicon deposition to fill the grooves, and mechanical polishing to obtain a DI structure ("V-groove" technique) (see Fig. 11.4) (20). The available surface area of the tubs is reduced appreciably compared with the conventional DI method because the reverse angle [54.7° for (100) orientation] of the tub sidewall results in a large isolation width w. To overcome this problem, a polysilicon–silicon bonding process has been developed ("poly Si bonding" technique) (21). As shown in Fig. 11.5, after standard V-groove etching and isolation oxidation of a device wafer, a polysilicon deposition to a thickness of twice the V-groove depth was performed. The polysilicon was polished and then bonded to a silicon wafer. The thinning of the device wafer produced the DI structure with the same

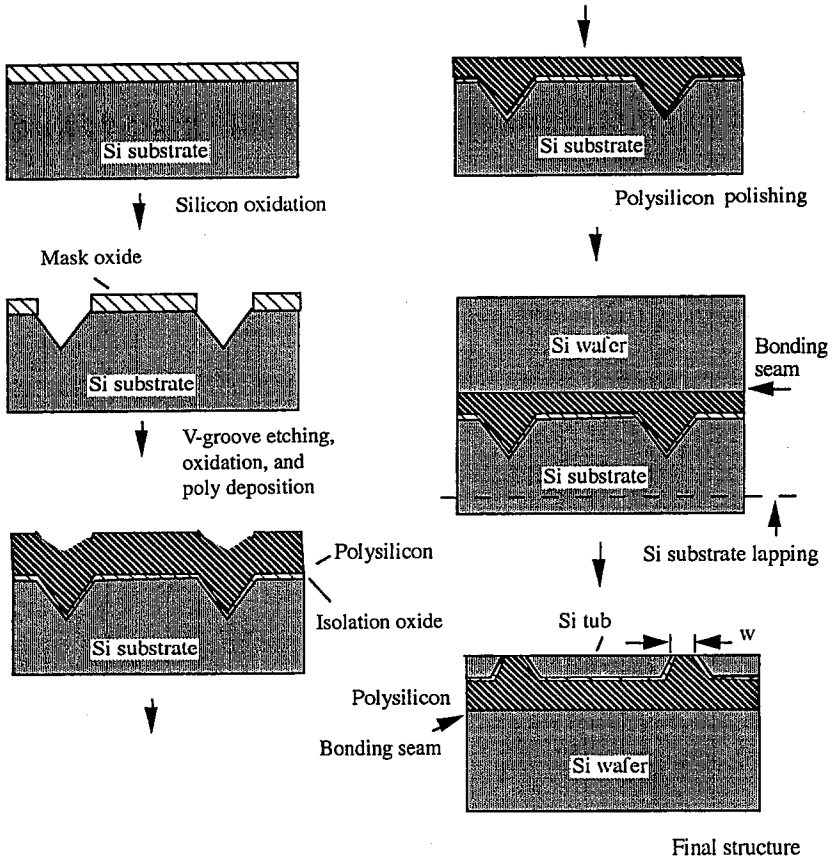

Fig. 11.5 Process flow of "polysilicon bonding" dielectric isolation technique (21).

tub sidewall orientation as a conventional DI structure. The thermal budget was greatly reduced and the stress and thermal resistance were also decreased owing to a thinner polysilicon layer in the structure. High-voltage (600 V) integrated circuits were manufactured by the bonded DI material and a highly accelerated aging test (150°C, biased at 375 V for 12 h) showed no device failure; the conventional devices had a 0.02% failure rate.

Another important DI method involves bonded SOI wafers combined with trench isolation to form fully isolated silicon islands. Figure 11.6 is a process

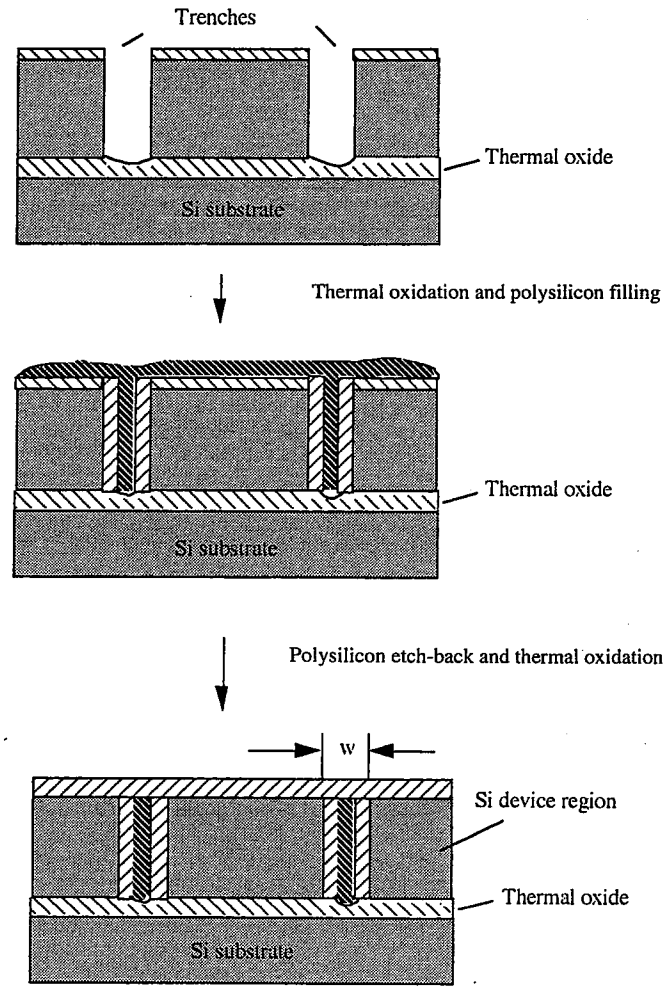

Fig. 11.6 Process flow of "trench isolation" dielectric isolation technique.

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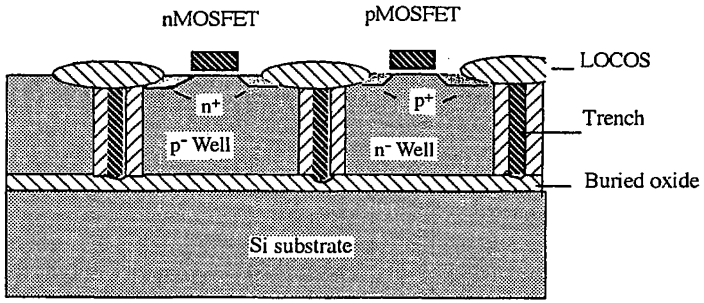


Fig. 11.7 Cross section of a CMOS structure using the trench dielectric isolation technique (22).

flow of the trench DI technique. Higher device-packing density is realized due to the smaller isolation space (w) which is achieved by narrow oxidized trenches filled with polysilicon. The silicon-layer thickness of the SOI substrate is presently limited to ~ 40 μm by currently available trench technology. This DI method ("trench" technique) is compatible with the bulk Si process and has been commercialized in analog CMOS IC production. It may be considered as the most promising DI approach.

Figure 11.7 shows a cross section of a CMOS structure using the trench DI technique (22). In this scheme, trench isolation and LOCOS isolation in the starting bonded SOI wafer with a 5-μm thick silicon layer and a 1-μm thick buried oxide layer are formed by a conventional process. The LOCOS isolation allows more devices to be included in a single tub and serves to eliminate trench parasitic devices. The analog CMOS ICs fabricated by this DI process have demonstrated better isolation features than their bulk pn junction isolation counterparts, including high device-packing density, overvoltage protection, latch-up hardness, low power consumption, low leakage, reduced cross-talk between p- and n-channel devices, and elevated temperature operation.

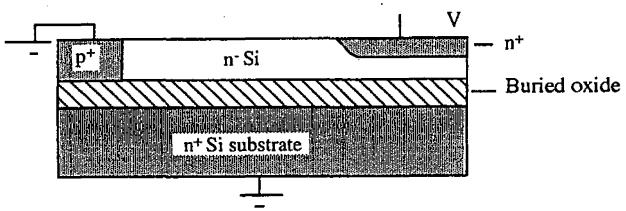
A unique problem associated with bonded SOI substrates is the inability of metallic contaminants introduced during the course of normal device processing to diffuse through the high-quality buried oxide layer to the gettering centers located in the substrate or on the back side of the wafers. The remaining metallic impurities in the SOI layer can lead to more gate oxide defects than would be found in equivalent bulk wafers. This problem does not exist in SIMOX materials, probably because of the gettering function of the defective silicon layer and/or the buried oxide layer. One possible solution to this problem is to introduce gettering sites in the sidewall of the isolation trenches used in the DI process (22). Table 11.3 gives a comparison of the three main DI techniques based on wafer bonding (23).

TABLE 11.3 Comparison of the Three Main DI Techniques Based on Wafer Bonding

Technique	V-Groove	Poly Si Bonding	Trench
Isolation width (w)	~ 57 μm (400 V)	~ 5 μm	~ 3 μm
SOI thickness range	Up to wafer thickness	Up to wafer thickness	< 40 μm
Manufacturability	Good	Good	Fair

11.2.2 High-Voltage Devices

In a pn junction, the applied reverse-bias voltage is totally sustained by the depletion layer. Therefore, a thick silicon layer is needed for realizing (vertical) devices with high breakdown voltage. Since low-cost isolation and high device-packing density can be obtained by the trench isolation on thin SOI substrates, it is of great interest to investigate the possibility of using thin



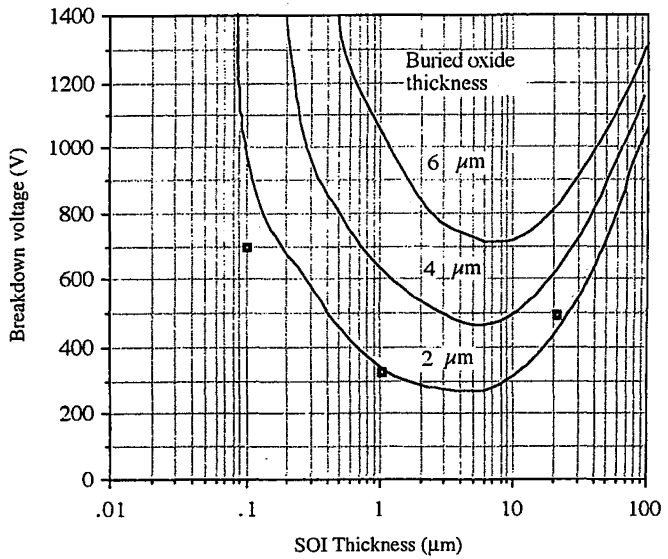


Fig. 11.8 Typical SOI high-voltage device and its calculated breakdown voltage as a function of SOI layer thickness at different buried oxide thicknesses. Several experimental data are also indicated in the plot (24).

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SOI substrates to realize lateral high-voltage devices. It has been found that in an SOI device, the reverse-biased voltage is shared by the silicon layer and the buried oxide layer so that a high breakdown voltage can be obtained by using a thinner silicon layer. Figure 11.8 shows a typical SOI high-voltage device and its calculated breakdown voltage as a function of SOI layer thickness at different buried oxide thicknesses (24). Several experimental data are also indicated in the plot. A linear distribution of the doping concentration from p^+ region to n^+ region in the SOI layer is assumed. It can be seen that the breakdown voltage increases with thickness of the buried oxide and becomes a minimum at SOI layer thickness between 5 and 10 μm. At SOI thickness > 10 μm or < 1 μm, the breakdown voltage increases. By using bonded SOI with a 15-μm thick silicon layer and 3-μm thick buried oxide, high-voltage MOS devices with breakdown voltage greater than 500 V have been realized (25).

There are two unique features of thin SOI substrates: (1) As can be seen in Fig. 11.8, when the silicon layer is thinner than ~ 1 μm, the breakdown voltage of the SOI diode increases significantly, possibly owing to the reduction of the mean free path of carriers, resulting in lower impact ionization. It is predicted that a 1000-Å silicon layer on a 600-μm quartz substrate may allow realization of a 5000-V lateral SOI diode (see Fig. 11.9). (2) The effective lifetime of minority carriers reduces monotonically with reducing SOI thickness, which results from an increasingly dominating role of the surface recombination velocity in determining the lifetime in the SOI layer. Therefore, the turn-off fall time during switching is greatly reduced in

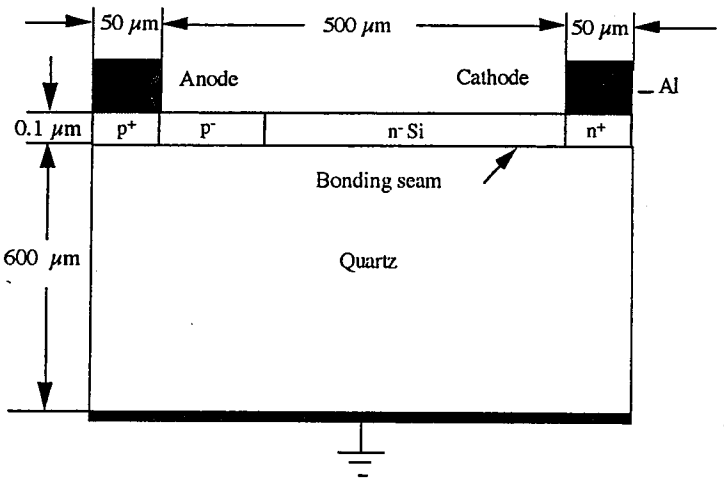

Fig. 11.9 A 5000-V lateral SOI diode with a 1000-Å SOI layer on a 600-μm quartz substrate.

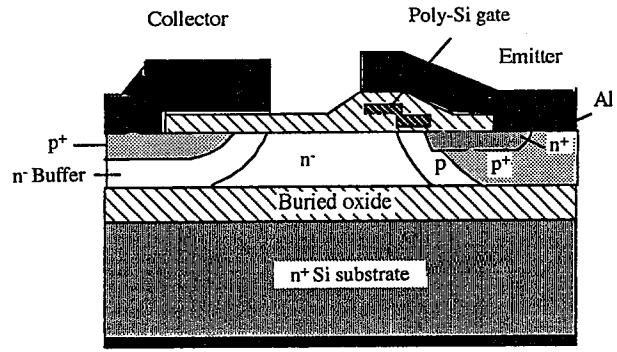

Fig. 11.10 Cross section of a lateral IGBT structure on a 1.5-μm SOI substrate.

high-voltage SOI lateral insulated gate bipolar transistors (LIGBT) without the use lifetime control steps such as Au diffusion or electron irradiation which cause pn junction leakage in devices. Figure 11.10 is a cross section of a lateral IGBT structure on a 1.5-μm SOI substrate. The reverse-bias leakage current of the LIGBT increases with temperature, but decreases as SOI thickness is reduced. It has been reported that LGBTs on 1.5-μm SOI can operate up to 200°C with acceptable leakage current (26).

11.2.3 High-Power Devices

Si/Si bonding has several advantages over the growth of thick epitaxial layers. Besides avoiding autodoping, among the advantages are high crystal quality, low thermal budget, time saving, and flexibility in terms of layer thickness, doping type, and concentration for optimization of device designs. The wafer-bonding technique has been used to fabricate IGBTs to optimize the n^+ buffer thickness and doping to achieve a low on-resistance but high device-breakdown voltage (1800 V) (27).

The minority carrier lifetime in bonded wafers is degraded in the bonding interface region owing to the presence of bonding defects. As discussed in Section 7.1.3 this effect has been used to control the switching time and on-state voltage of IGBTs without the use of conventional lifetime control techniques (28).

If a lightly doped n-type wafer is bonded to a heavily doped p^+-type wafer followed by thinning of the n wafer and subsequent p^+ emitter diffusion, a power transistor with an optimized base thickness can be realized. Processing such a relatively thin n-base (e.g., 30 μm), would not be practical if there was no p^+ wafer to act as a mechanical support, which introduces a small series resistance. Utilizing this approach, a thyristor-like power device was fabricated and an improvement in power-handling capability as high as 250% was obtained (29).

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11.2.4 Smart Power Circuits

As discussed above, high-voltage and high-power ICs can be fabricated with conventional CMOS processes by using an SOI substrate with silicon layers 1–15 μm thick and trench isolation. It is therefore possible that CMOS VLSI CPU and logic and analog circuits can be integrated with high-voltage devices onto the same chip which is then commonly termed a "smart power circuit." At present, the integration level of the smart power circuits is still low; often just some logic circuits and a power device are integrated. The SOI substrates can also offer flexibility to incorporate bulk bipolar, high voltage, low

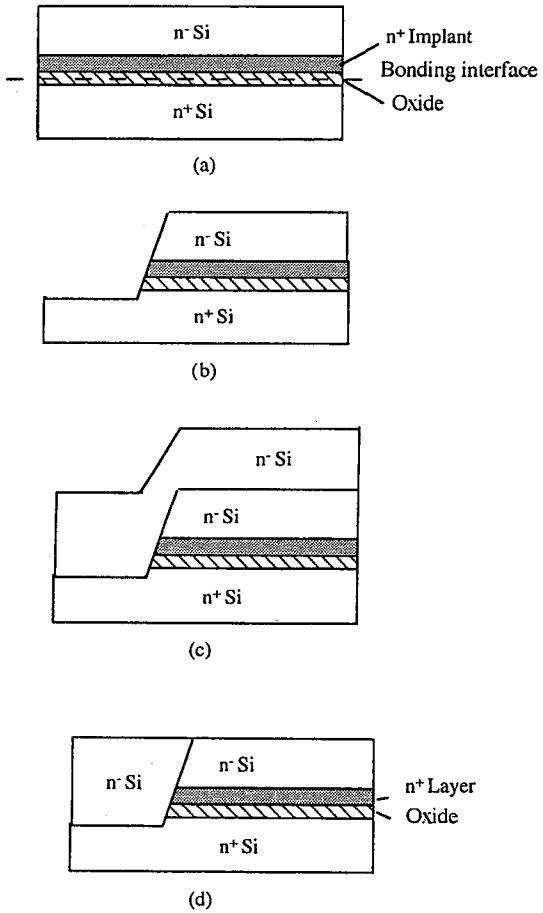

Fig. 11.11 Process flow of a DI substrate in which normal CMOS and bipolar devices are fabricated in the SOI regions and dielectric isolated from high-voltage power devices which are fabricated in the bulk silicon substrate on the same chip (30). (*a*) Bonding; (*b*) Si and oxide etch; (*c*) epitaxial growth; (*d*) polishing.

voltage, SOI or other devices on the same chip. Figure 11.11 shows the process flow of a DI substrate in which normal CMOS and bipolar devices are fabricated in the SOI regions and electrically isolated from high-voltage/high-power devices which are fabricated in the bulk silicon substrate on the same chip (30). The maximum power dissipation of the power ICs fabricated on the substrates is improved by the vertical output (output current passes through the substrate) of the power devices, resulting in reduction of both thermal and electric resistances of the chips.

An improved process for this structure has been reported recently. The process flow of the structure is shown in Fig. 11.12 (31). The starting n^- silicon device wafer is etched locally to form a 3-μm deep pan and n^+ implantation is performed to form the n^+ buried layer in this region.

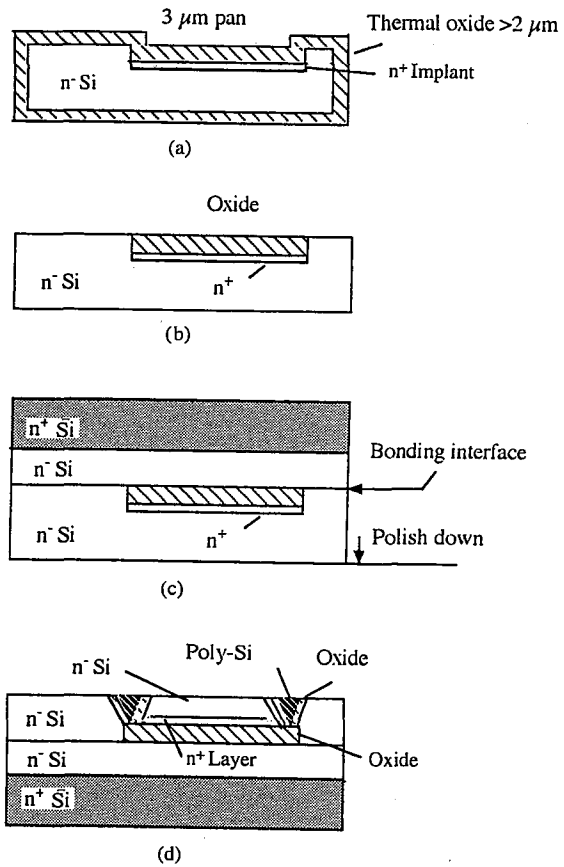

Fig. 11.12 An improved process for SOI/bulk silicon structures (31). (*a*) Pan etch, implantation, and oxidation; (*b*) polishing; (*c*) bonding and thinning; (*d*) trench isolation.

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Subsequently, thermal oxide of more than 2 μm is grown (see Fig. 11.12*a*). The wafer is then polished to have sufficient smoothness and flatness (Fig. 11.12*b*). After removing the native oxide on the silicon region, the wafer is bonded at room temperature with an n^-/n^+ epitaxial silicon handle wafer followed by annealing at 1100°C in nitrogen (Fig. 11.12*c*). It is necessary to anneal in an inert gas to minimize the amount of oxide formed during the annealing process at the bonding interface. The device wafer is thinned by grinding and polishing to a desirable thickness (Fig. 11.12*d*). The dielectric isolation between SOI and bulk regions is formed by a conventional process of groove etching, thermal oxidation, polysilicon refilling, and final polishing (Fig. 11.12*e*). This technique has been employed in the preparation of 600 V, 5 A PWM (pulse width modulation) switching regulator ICs consisting of an output n-DMOSFET with an on-resistance of $\sim 0.6\ \Omega$ and switching frequency of 650 kHz (31).

A bipolar–CMOS–DMOS (BiCDMOS or BCD) technology using trench isolation and bonded SOI substrates with a 2-μm silicon layer and a 0.5-μm buried oxide has been reported. This technology is fully compatible with a conventional 0.8-μm CMOS process and is capable of integrating 60 V low-resistance lateral DMOS, vertical npn and pnp transistors, and a CPU on the same chip with an operation temperature up to 200°C. The CPU operating frequency is 50 MHz at 25°C, a 20% increase over its bulk counterpart (32).

11.2.5 Buried Layer Structures

AlN is an insulator with a high thermal conductivity ($\sim$ 1 W/cmK) comparable to Si (1.5 W/cmK) and much larger than that of SiO_2 ($\sim$ 0.015 W/cmK). Therefore, AlN can be used to replace the SiO_2 in standard SOI structures to form highly thermally conductive SOI structures that allow high-power device applications without significant self-heating effects. AlN films can be deposited on a silicon wafer by reactive sputtering from an Al target in nitrogen and argon at a low pressure of a few milli-Torr. After bonding with a silicon wafer and subsequent thinning, silicon on AlN structures can be formed (33).

Buried highly conductive layers are commonly used in bipolar ICs and power MOS transistors to lower the resistance of the collector/drain of the device and thus to improve its speed and power-handling capability. Since high-quality epitaxial layers cannot be grown on surfaces with a doping concentration in excess of 1×10^{19} cm^{-3}, the resistivity of the buried layer realized by a conventional doping process is limited to $\sim 2000\ \mu\Omega$/cm. This limitation does not exist in wafer bonding. A dielectrically isolated silicon substrate incorporating low-resistivity buried silicide layers can be achieved by wafer bonding. The silicide layer can be formed either prior to room-temperature bonding or during annealing after room-temperature bonding of the wafers in which either one or both wafers are coated with a metal layer. The

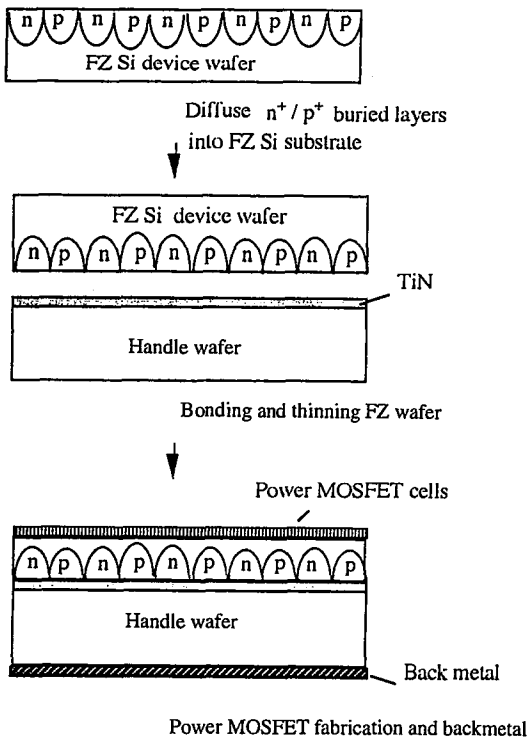

Fig. 11.13 Process scheme used to produce EIGBT (enhanced insulated gate bipolar transistor).

WSi_2, $CoSi_2$, or $TiSi_2$ buried layers with resistivity of 20–30 $\mu\Omega$/cm formed by wafer bonding were reported (34, 35).

An enhanced insulated-gate bipolar transistor (EIGBT) has been reported in which an FZ wafer possessing p^+ (boron) and n^+ (antimony) regions was covered with a TiN conducting layer, forming an ohmic contact to both p^+ and n^+ buried regions, and was bonded to a low-resistivity n^+ wafer (36). Figure 11.13 shows the process flow used to produce the EIGBT. There is a significant lateral diffusion of p^+ and n^+ dopants in the cases where WSi_2 or $TiSi_2$ is used as the conductive bonding layer. At 1200°C, the lateral dopant diffusion coefficients in the silicides are 5–7 orders of magnitude faster than the known diffusion of p^+ and n^+ dopants in silicon. Boron and antimony are also segregated into the silicide layer. Both effects result in a loss of ohmic contact of the silicide layer to both p^+ and n^+ buried regions at the interface. The TiN shows no significant lateral dopant diffusion and is therefore selected as the conductive layer. The FZ wafer was then thinned and power MOSFET cells were fabricated on the top. The TiN layer,

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forming ohmic contact to both n^+ and p^+ regions, enables both low-on-state resistance and fast switching to be achieved simultaneously in the EIGBT.

11.3 BONDING APPLICATIONS IN MICROMECHANICS

Silicon wafer bonding has been found to be a powerful, reliable and versatile technique in fabrication of micromachined devices such as solid-state sensors and actuators, and has quickly been introduced in the fabrication of commercial products. Owing to its application and process compatibility with the VLSI industry, further exploitation of wafer-bonding technology in novel micromechanic structures is promising. Microsensors and actuators of low cost combined with high performance can be realized using VLSI batch-fabrication and device-miniaturization technologies.

11.3.1 Surface Sacrificial Layers

In conventional surface micromachining, a polysilicon layer is deposited on a substrate covered by a sacrificial spacer layer (e.g., oxide), which is then laterally etched off to create a gap between the polysilicon layer and the substrate. The practical thickness of both polysilicon and spacer layers is limited to 2–3 μm. Polysilicon exhibits poor electronic properties, including low piezoresistive coefficients and inferior pn junction characteristics. Moreover, its mechanical behavior is difficult to reproduce. All these drawbacks related to polysilicon can be eliminated by surface micromachining through single-crystal silicon wafer bonding.

A typical example of the process flow for surface micromachining using wafer bonding is schematically shown in Fig. 11.14 (37). After etching shallow

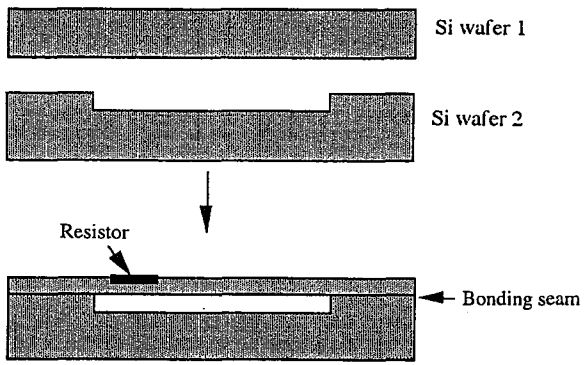

Fig. 11.14 Typical example of the process flow for surface micromachining using wafer bonding (37).

cavities in the silicon substrate, another silicon wafer is bonded to the preetched substrate. A thinning operation is performed to remove most of the silicon from the second wafer to form a layer with a desired thickness (5–25 μm or more) on the substrate. The standard integrated circuit processing can then be employed to fabricate resistors and transistors or to deposit insulating layers and define the metal patterns on the silicon layer. The space between the suspended silicon layer and the substrate surface can be easily adjusted to a desired depth by etching and the silicon suspended layer can be as thick as a full wafer. A number of silicon sensors and actuators have been realized based on this basic process. For example, a resonant-beam pressure sensor (38) was fabricated with long-term overall accuracy of about 0.01% per year.

Figure 11.15 compares some important aspects of polysilicon surface machining combined with bulk etching and wafer bonding for pressure sensors (39). As can be seen from Fig. 11.15, polysilicon surface-micromachined pressure sensors have a nonplanar surface. Polysilicon pressure sensors also suffer from low piezoresistive sensitivity, large thermal mismatch and residual strain. Because the cavities can be etched on one of the wafers before bonding, the area loss due to the 54.7° etch angle on (100) silicon from

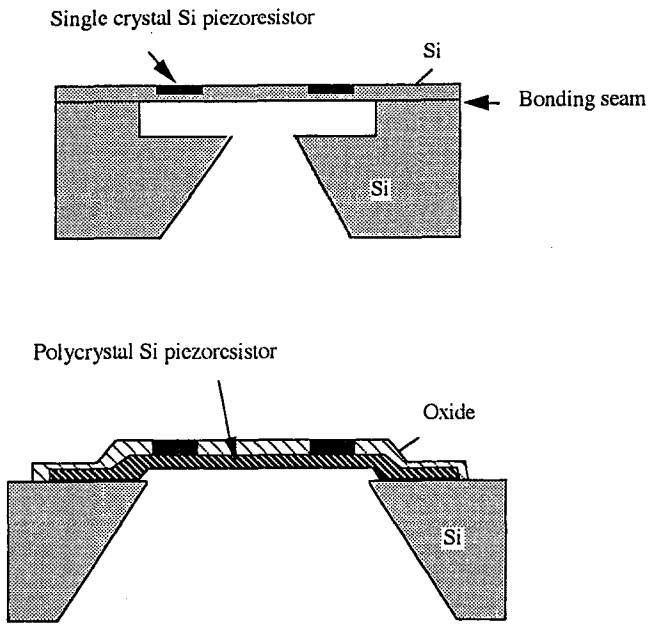

Fig. 11.15 Comparison of some features of pressure sensors fabricated either by wafer bonding or by polysilicon surface micromachining combined with bulk etching from the back side

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the back side of the wafer is significantly reduced. For the same diaphragm dimensions and the same overall thickness of the sensor chip, the bonded sensor used less than 50% of the silicon area of a sensor fabricated by a conventional process.

11.3.2 Pressure Sensors and Accelerometers

Silicon wafer bonding has been widely adopted for the fabrication of pressure sensors and accelerometers, as discussed in previous sections. In addition to low cost, stress free, high performance of the silicon pressure sensors based on single-crystal silicon piezoresistors, wafer bonding has made mass production possible for absolute pressure sensors, high-temperature pressure sensors, high-overrange-tolerance pressure sensors, and very small catheter-tip pressure sensors (40).

The basic process flow for wafer-bonding pressure sensors is shown in Fig. 11.14. If the wafers are initially bonded in vacuum, the pressure in the cavity is close to zero after high-temperature annealing (41), although there may still be small amounts of residual gases such as hydrogen in the cavity. The buried vacuum cavity functions as the vacuum reference pressure and the device is called an absolute pressure sensor. The cavity can be any shape or depth. If the cavity is only a few microns deep, the bottom of the cavity serves as an overpressure stop to prevent the sensors from overrange damage.

Figure 11.16 shows the cross section of a catheter-tip pressure sensor which is very small. Since the cavity has inward-sloping walls, the chip can be only slightly larger than the diaphragm (400 μm vs. 250 μm). To reduce the size of the sensors, the wafer is ground and polished to a thickness of about 150 μm. The cavity is open to the atmosphere and the device used is a gauge-pressure sensor. Since most of the processing is done with a sufficiently thick wafer, the manufacturability is excellent (40).

High-temperature sensors can also be fabricated by wafer-bonding technology. The device wafer is covered with a patterned mask layer, for example, photoresist and implantation is performed to form p^{++} piezoresistors. After removing the photoresist, the device wafer is then bonded to an oxidized silicon wafer. After grinding and selective etching, the p^{++} piezoresistors are

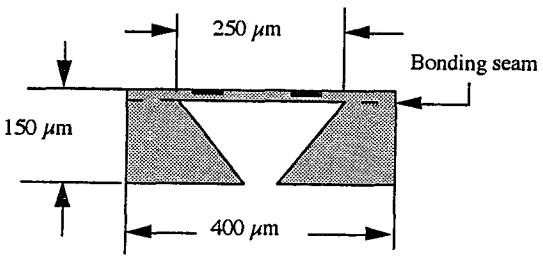

Fig. 11.16 Cross section of a catheter-tip pressure sensor (40).

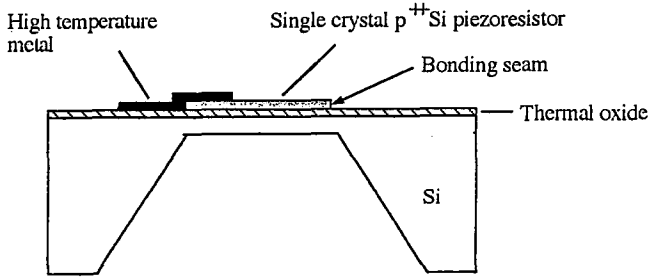

Fig. 11.17 High-temperature pressure sensor fabricated on SOI substrate by wafer-bonding technology (40).

bonded on the oxide followed by a conventional process and etching from the back side to form a pressure sensor (see Fig. 11.17). Because there is no pn junction-associated leakage or resistivity instability induced by ionic contamination, and heavily doped resistors are not sensitive to temperature, an operation temperature higher than 250°C was realized (40).

A silicon threshold pressure switch with mechanical hysteresis has been reported, based on wafer-bonding technology (42). The hysteresis in the behavior of the switch is often desirable to prevent error switching during small fluctuations of the signal being measured. A silicon wafer was bonded to another silicon wafer with cavities in air which was then trapped within the sealed cavity. After annealing at 1000°C for 1 h, the residual pressure inside these sealed cavities was found to be $\sim$0.8 atm owing to the 80% nitrogen remaining after the oxygen had reacted with the silicon. When the first wafer was thinned to $\sim$5 μm and subsequently annealed at 1050°C for 1 h, a spherically shaped cap was formed. The trapped air inside the sealed cavity expanded with increasing temperature and uniformly exerted a force on the thin silicon cap layer beyond its yield point, resulting in plastic deformation of this layer. When the structure was cooled to room temperature, the plastic-deformed silicon capping layer retained its spherical shape. When an external pressure beyond the threshold pressure was approached, the top silicon layer deflected downward and the switch was on. The snapping back of the top silicon layer occurred at a lower pressure than the pressure required to buckle the structure. A schematic diagram of the processing steps and operation is shown in Fig. 11.18 (42). The extent of the permanent deformation is dependent on the cavity depth and diameter, the capping layer thickness, and the deformation temperature.

Accelerometers with high sensitivity, high overrange capability, small size, low cost, and high reliability are key components for active suspension control in automobiles and for crash detectors in air-bag deployment systems. Wafer bonding has made it possible to mass-produce high-performance accelerometers. Figure 11.19 is an example of a schematic cross section of an silicon accelerometer based on wafer bonding (40).

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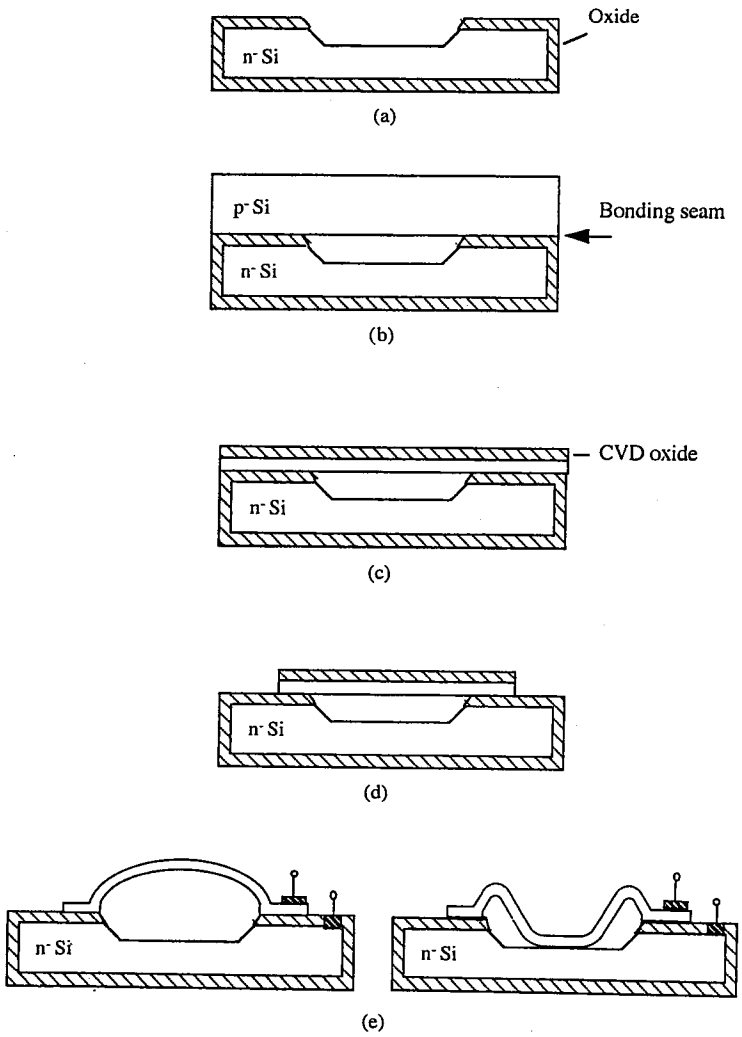

Fig. 11.18 Threshold pressure switch fabrication sequence: (*a*) cavity and oxide etch; (*b*) wafer bonding; (*c*) thinning and CVD oxide deposition; (*d*) oxide and silicon plasma etch; (*e*) pattern, etch contact windows, deposit and pattern Al (42).

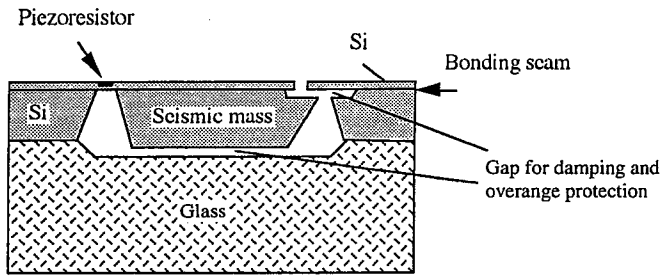

Fig. 11.19 Schematic cross section of an accelerometer fabricated by silicon wafer bonding (40).

11.3.3 Microchannel and Microvalve Systems

An important application of wafer bonding in micromechanics has been the fabrication of microchannel coolers in packages for semiconductor laser diode arrays to achieve a low thermal impedance. Bonding and etch-back has also been employed in vacuum microelectronic devices to precisely control the space of a few microns between the silicon field emitter cathode and the silicon anode (43).

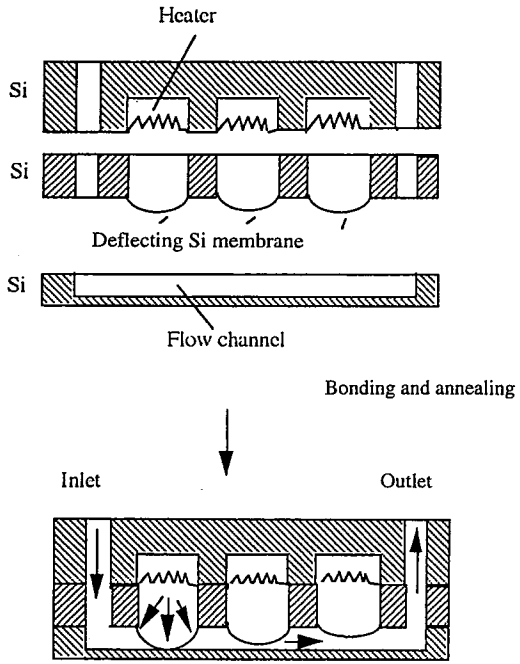

Fig. 11.20 Cross section of a microperistaltic pump (43).

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Micropumps and microvalves can also be fabricated by wafer bonding. Figure 11.20 shows a cross section of a microperistaltic pump. Using the heaters in the device, the three fluid-filled chambers can be sequentially expanded to pump the incoming liquid to the outlet. The three silicon wafers containing the heaters, the silicon membranes, and the fluid channel, respectively, are bonded and annealed (44).

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12

Emerging and Future Applications

Wafer-bonding technology is by no means restricted to silicon wafers. Proper polishing and surface chemistry allow combinations of almost all materials, independent of whether they are crystal or noncrystal solids, their crystal orientation and lattice parameter, their doping type and profile, and their thickness. Optimization of each of the two bonding wafers for a specific application can be realized separately prior to the bonding. Wafer bonding, therefore, opens up new design possibilities not only for mainstream applications, as described in Chapter 11, but also for such other areas as optoelectronics, electroacoustics, nonlinear or X-ray optics, and even metrology.

This chapter introduces some of the recent nonmainstream applications of wafer bonding. It is likely that a better understanding of the physics and chemistry involved in wafer bonding will allow further innovative utilization of the potential provided by wafer bonding in areas of which we are presently not even aware.

12.1 BONDING APPLICATIONS IN OPTOELECTRONICS

12.1.1 Optoelectronic Integrated Circuits

The integration of optical devices with silicon-integrated circuits leads to optoelectronic integrated circuits (OEIC). The OEIC technology is highly desirable for optical-fiber communications and optical interconnects. Since III-V compound semiconductors are the dominating materials for light emission, optical amplification, and other photonic functions, the integration of III-V semiconductors with silicon by wafer bonding is of interest for realizing optoelectronic integrated circuits. Wafer bonding allows us to circumvent the problem of threading dislocations caused by the lattice mismatch between silicon and the relevant III-V compounds when heteroepitaxial growth is performed. As discussed in Chapter 10, successful GaAs/Si, InP/Si, and InP/GaAs bonding has been demonstrated for lasers, detectors, and waveguides. To reduce the optical-fiber loss, long-wavelength lasers are highly desirable. With InP as substrate, InGaAsP is commonly employed to fabricate long-wavelength (1.5–1.55 μm) lasers. At the wavelength of InP-based

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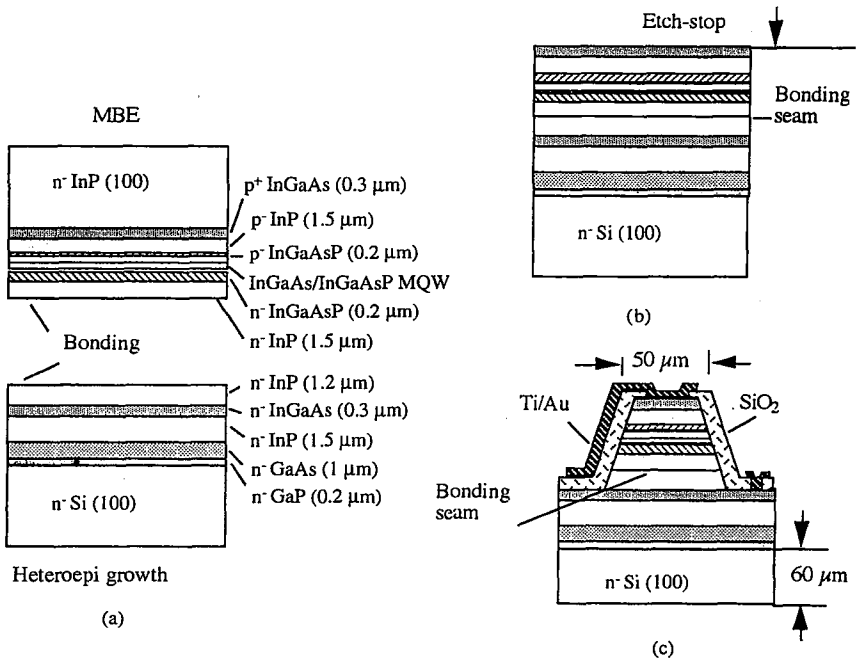

Fig. 12.1 Key process steps of a 1.55-μm laser fabricated by wafer bonding. (*a*) Preparation and bonding substrates; (*b*) bonding (700°C, 1 h, H_2); (*c*) device formation.

lasers, the Si substrate is transparent, making optical interconnects between the devices through the silicon substrate possible.

Figure 12.1 shows the process flow of a 1.55-μm laser fabricated by wafer bonding (1). The InP substrate is a (100), n-type wafer on which a 0.3-μm thick p^+-InGaAs etch-stop layer is grown first. This layer also serves as the metal contact layer in the device. A 1.5-μm thick p-InP cladding layer, an undoped InGaAs/InGaAsP (50 Å/100 Å × 4) 1.55-μm multiquantum-well active layer sandwiched between two 0.2-μm thick InGaAsP optical guide layers and a 1.5-μm thick n-InP layer are consecutively grown. The Si substrate is a (100), 2° off ⟨110⟩, n-type wafer on which buffer layers consisting of a 0.2-μm n-GaP layer, a 1-μm GaAs layer, a 1.5-μm thick n-InP layer, a 0.3-μm thick InGaAs layer, and a 1.2-μm thick n-InP layer are heteroepitaxially grown. The buffer layers are adopted to relax the thermal stress, which may cause the threading dislocations at the bonding interface to propagate into the device layer at high temperatures. The two wafers are carefully mirror polished, cleaned in H_2SO_4:H_2O_2:H_2O solution (3:1:1), rinsed in DI water, and dried. After room-temperature bonding, a weight is

put on the top of the pair to produce a pressure of ~300 g/cm^2 and the pair is annealed at 700°C for 1 h in a hydrogen ambient. The InP substrate is removed by HCl selective etching, which stopped at the top of the p^+-InGaAs etch-stop layer. A 50-μm wide mesa with strip lasers is formed by wet etching and contact windows are opened and Ti/Au contacts are formed. The Si substrate is lapped to 60 μm and cleaved into laser-array bars with the cleaved surfaces as the two mirror facets. The lasers show excellent pn-junction characteristics and no highly resistive layer is observed at the bonded interface. The threshold current density of the lasers is 1.7 kA/cm^2 under room temperature pulsed conditions (300 ns, 1 kHz) which is comparable to the value for lasers fabricated on InP substrates.

12.1.2 Low-Threshold, Long-Wavelength Lasers

If the active layer is sandwiched vertically between two mirrors, the light output is emitted from the surface of the laser chip. These vertical-cavity surface-emitting lasers (VCSEL) can be fabricated by a monolithic process with densely packed chips on wafers. The lasers are potentially low-cost light sources for optical communications because they can couple with optical fiber easily and can be probe-tested on the wafer level before separating into chips.

A double-bonded VCSEL structure has been suggested and demonstrated (2). The process flow of the fabrication of the laser is schematically shown in Fig. 12.2. A 25-period n-GaAs/AlAs mirror and a 24-period GaAs/AlAs mirror are epitaxially deposited on an n-GaAs substrate and a p-GaAs substrate, respectively. The active layer on the InP substrate (covered with a GaAsP etch-stop layer) consists of seven strained InGaAsP quantum wells with strain-compensating InGaAsP barriers that are sandwiched between two 1836-Å thick confinement layers and two 1222-Å thick InP cladding layers (Fig. 12.2*a*). The n-GaAs wafer with the GaAs/AlAs mirror is bonded to the InP wafer with the active layer at 630°C for 20 min in hydrogen. The InP substrate is removed by selective etching in HCl:H_2O (3:1) which stops at the InGaAsP etch-stop layer. The p-GaAs wafer with the GaAs/AlAs mirror is then bonded to the other side of the active layer at 630°C for 20 min in hydrogen again (Fig. 12.2*b*). The p-GaAs substrate and the AlAs etch-stop layer is removed using wet chemical etchants, for example, H_2SO_4:H_2O_2:H_2O (4:1:1) and a 10% HF aqueous solution, respectively. The mesas are etched down to the bottom of the p-GaAS/AlAs mirror using Cl_2 reactive ion etching. Figure 12.2*c* shows the final laser structure. The vertical-cavity lasers have a room-temperature pulsed threshold current density of 3 kA/cm^2 at 1.52 μm and a low thermal resistance.

12.1.3 Quasi-Phase-Matched Second-Harmonic Generation

Taking advantage of nonlinear optical effects, the second harmonic of input-coherent emission wavelengths can be generated, thus extending the

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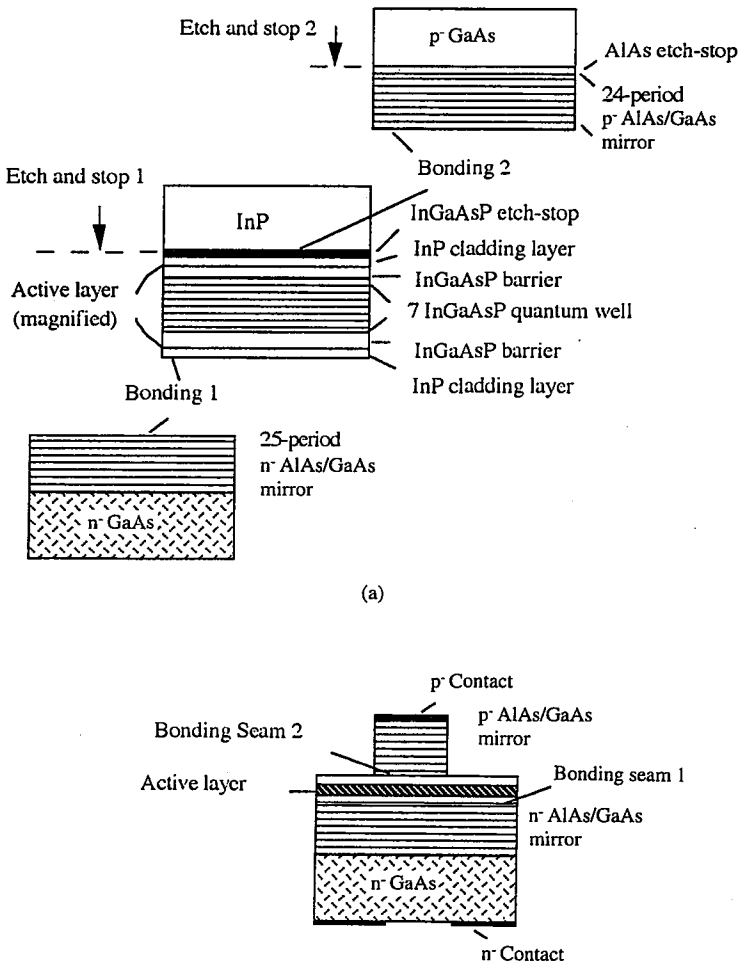

Fig. 12.2 Key process steps of fabrication of a double-bonded vertical-cavity laser structure. (*a*) Double-bonding (both 630°C, 20 min., H_2) and etching; (*b*) laser structure.

available wavelengths of existing lasers. Typical III-V semiconductors have significantly larger second-order nonlinear susceptibilities, higher thermal conductivities, and lower absorption coefficients compared to conventional nonlinear materials. However, the cubic zinc-blende semiconductors have no intrinsic birefringence for phase matching, which is the basic requirement for wavelength conversion. Quasi-phase-matching has been suggested to overcome the difficulty, where a periodic modulation of the nonlinear susceptibility compensates for the phase velocity mismatch between the interacting waves (3). A bonded monolithic stack of GaAs or ZnSe plates as a composite substrate with a designed periodic change of the crystal orientations is considered as a suitable material for that purpose. Wafer bonding of differently oriented crystals to create a monolithic structure also provides a desirable solution to avoid reflection and scattering losses associated with the

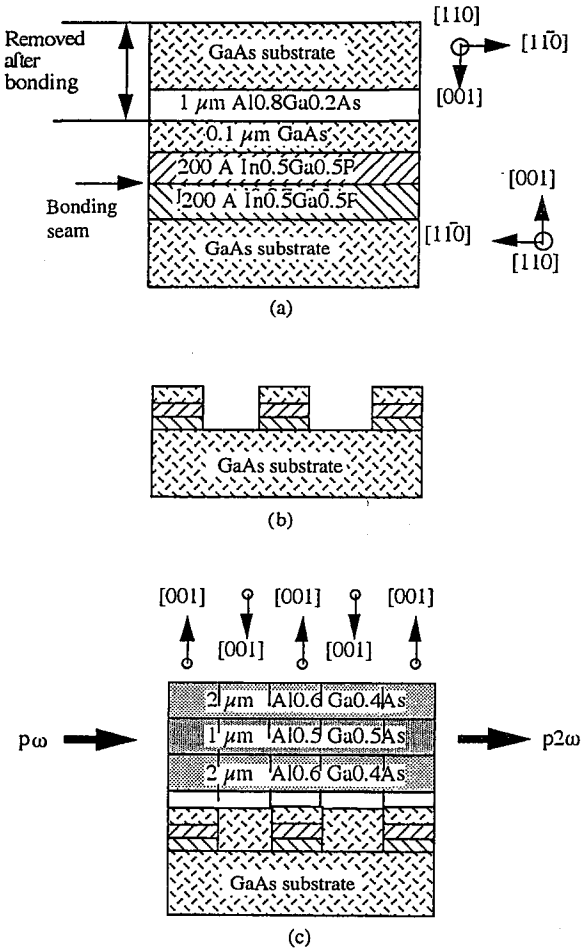

Fig. 12.3 Key process steps of fabrication of an integrated periodically domain-reversed AlGaAs nonlinear optical waveguide. (*a*) MOCVD growth and bonding; (*b*) patterning before epitaxial growth; (*c*) the waveguide with periodic domain inversion.

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many interfaces in the structure. Two to nine bulk (110) GaAs plates were bonded to form a structure in which adjacent wafers were rotated by 180° for second-harmonic (5.3 μm) generation from a 10.6-μm CO_2 laser (4). The bonded nonlinear structure retains the thermal and mechanical properties of the GaAs bulk and the measured wavelength conversion is in agreement with theoretical predictions.

Integrated semiconductor nonlinear optical waveguides with semiconductor lasers on the same chip are desirable for achieving an efficient wavelength conversion. An integrated AlGaAs nonlinear optical waveguide has been demonstrated which is epitaxially grown on a special GaAs substrate. A periodic crystal domain inversion is realized through wafer bonding and MOCVD (MetalOrganic Chemical Vapor Deposition) (5). Figure 12.3*a* shows that two GaAs [001] wafers are bonded at 650°C for 30 min in hydrogen. One of the wafers is covered with a MOCVD grown 200-Å thick $In_{0.5}Ga_{0.5}P$ layer and another has a MOCVD grown layer of 1 μm $Al_{0.8}Ga_{0.2}As$, 0.1 μm GaAs and 200 Å $In_{0.5}Ga_{0.5}P$. In the bonded structure, the [110] crystal orientations of the two wafers are parallel to each other. After annealing of the bonded pair, the substrate of the top GaAs wafer and the 1-μm $Al_{0.8}Ga_{0.2}As$ etch-stop layer are selectively etched away. Figure 12.3*b* shows the substrate structure after patterning of a 3-μm period grating and selective etching. A GaAs surface from the bottom substrate and a GaAs epitaxial layer from the top GaAs substrate are alternatively revealed. Undoped layers consisting of a 0.4-μm GaAs planarization layer, a 2-μm $Al_{0.6}Ga_{0.4}As$ cladding layer, a 1-μm $Al_{0.5}Ga_{0.5}As$ core layer, and a 2-μm $Al_{0.6}Ga_{0.4}As$ cladding layer are MOCVD grown on the patterned GaAs substrate. A vertical arrangement of alternating domains in the epitaxial layers forms the periodically domain-reversed AlGaAs waveguide, (Fig. 12.3*c*). The measurements show a clear quadratic dependence of the second-harmonic power on the input of the fundamental wave.

12.1.4 Cleaved GaN Facet Mirrors on Sapphire Substrates

The GaN lasers are highly desirable for visible light applications and high-density data-storage systems. Improved mirrors are required to reduce the lasing threshold of the GaN lasers. Usually, cleaved mirrors are not useful for GaN grown on sapphire because the natural cleaved planes of (0001) sapphire (c-Al_2O_3) substrates are not perpendicular to the wafer surface. Based on a wafer-bonding approach, cleaved GaN mirrors which are perpendicular to the wafer surface have been achieved (6).

The process flow of the method is schematically shown in Fig. 12.4. The GaN layers with a thickness of 1.5–2.5 μm are MOCVD grown on (0001) sapphire substrates at 1080°C. The RMS surface roughness is $\sim$10 Å. The InP wafers are n-type, (100) orientation. The GaAs and InP samples, 8 × 8 mm in size, are pressed together for bonding after cleaning in solvents and a dip in a 49% HF solution and before the HF evaporated from the surfaces.

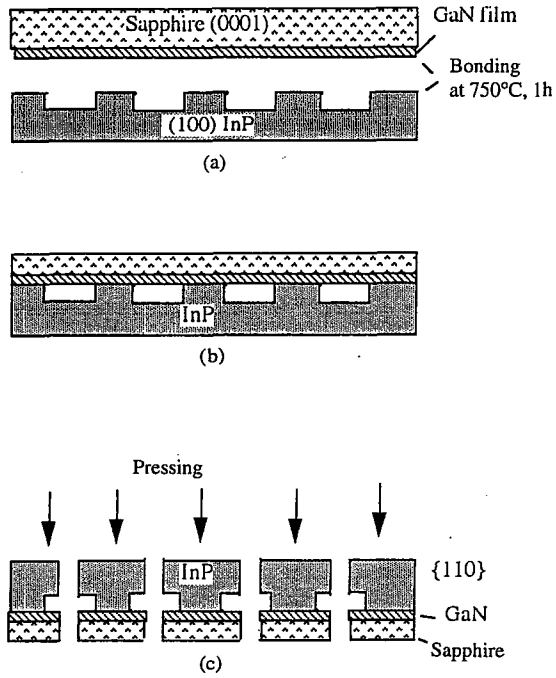

Fig. 12.4 Key process steps of fabrication of a cleaved GaN mirror perpendicular to the sapphire wafer surface. (*a*) InP and sapphire sample preparation; (*b*) thinning of sapphire sample to < 150 μm; (*c*) cleavage to form optically flat GaN faces.

To allow the residual liquid and outgassing gases to escape from the bonding interface during annealing at 750°C for 60 min, the InP samples are etched to form 10-μm wide channels with a period of 150 μm (Fig. 12.4*a*). The bonded interface is bubble-free and has no oxide layer. The defects formed because of the lattice mismatch are contained within only a few monolayers of the bonding interface. The sapphire substrate is lapped by diamond slurry with 15 μm grit to less than 150 μm in thickness (Fig. 12.4*b*). After making a scribe mark on the InP substrate, turning the bonded samples over and pressing on the sapphire, the GaN and thinned sapphire are forced to cleave parallel to the {110} crystal planes of the InP substrate (Fig. 12.4*c*). The cleaved facets appear to be optically flat.

12.2 BONDING APPLICATIONS IN ELECTROACOUSTICS

Direct bonding of silicon to piezoelectric crystals has been investigated to miniaturize surface acoustic wave filters and surface and bulk resonators and to integrate these devices with silicon circuits on the same chip. As described

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TABLE 12.1 Characteristics of Bonding Samples of $LiTaO_3$, $LiNbO_3$, and Silicon

	$LiTaO_3$	$LiNbO_3$	Silicon
TEC (10^{-6}/°C at 300°C)	20.0	18.3	4.9
Sample size (mm^2)	10 × 8	10 × 8	15 × 10
Sample thickness (μm)	50–100	50–100	450
Orientation	x-cut	128° y-cut	(100)
Cleavability	High	High	Low

in Section 9.1.3, the bonding of a quartz crystal to silicon allows the integration of electroacoustic devices such as quartz crystal resonators with silicon oscillators and filters for applications such as mobile communication systems. Bonding of a small quartz crystal with a diameter of 5 mm and a thickness of 30 μm to a silicon piece 10 × 10 mm^2 in size and 350 μm in thickness at 300–450°C for 2 h has been demonstrated. After lapping to thin the quartz crystal to 15 μm after bonding, quartz resonators on silicon substrates have been fabricated (7). By conventional photolithography and wet-etching techniques, the silicon under the quartz crystal is etched away except at the supporting region. Electrodes of 2 mm in diameter are formed on both surfaces of the quartz crystal to generate bulk acoustic waves. With the quartz diameter of 5 mm, a first mode resonant frequency of 112 MHz and a Q-value of 16,000 are obtained. For a further thinned-down quartz crystal, GHz resonators should be possible. Single-chip electroacoustic integrated circuits such as voltage-controlled oscillators and temperature-compensated crystal oscillators can also be realized by bonded-quartz crystal/Si substrates.

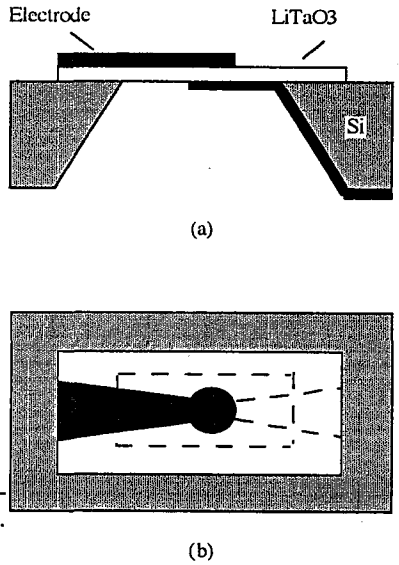

Fig. 12.5 Schematic of a $LiTaO_3$/Si resonator fabricated on a bonded substrate. (*a*) Cross section; (*b*) plan view.

Direct bonding of the piezoelectric crystals $LiTaO_3$ and $LiNbO_3$ to silicon has been demonstrated (8). Table 12.1 lists the thermal expansion coefficients (TEC) of $LiTaO_3$, $LiNbO_3$, and silicon, and the sizes of the bonded samples.

As can be seen in Table 12.1 the large difference in the thermal expansion coefficients and the high cleavability make the bonding of whole wafers of $LiTaO_3$ and $LiNbO_3$ to silicon difficult. The bonding of smaller samples is achieved by RCA1 solution cleaning, DI water rinse and drying, room temperature bonding, and annealing at 200–500°C in N_2. Figure 12.5 shows a schematic of a $LiTaO_3$/Si resonator fabricated on the bonded substrate. The silicon substrate under the $LiTaO_3$ layer is etched away, leaving only the supporting area. The Cr and Au layers are deposited on both surfaces of the $LiTaO_3$ layer to form the electrodes. The diameter of the electrodes is 2 mm. A thickness-shear mode-resonant frequency of 19.07 MHz and a Q-value of 472 are obtained.

12.3 BONDING APPLICATIONS IN ELECTROMAGNETOOPTICS

Magnetooptic devices such as optical isolators are essential to stabilize laser diode oscillation and are fabricated using magnetooptic crystals. Therefore, bonding of III-V semiconductors to magnetooptic crystals are of interest. Bonding between InP and the magnetooptic crystal $Gd_3Ga_5O_{12}$ (GGG) has been demonstrated (9).

The samples to be bonded are mirror-polished (100) or (111) InP and (111) GGG that are 5 × 5 mm in size. The (100) and (111) InP samples are cleaned in H_2SO_4:H_2O_2:H_2O solution (3:1:1) and H_2SO_4:H_2O_2:H_2O solution (1:1:10), respectively. The GGG samples are slightly etched in H_3PO_4 at 150°C. The surfaces of the samples are all hydrophilic. After DI water rinse, the (100) or (111) InP and GGG samples are bonded at room temperature followed by annealing at 450–650°C for 10–60 min in hydrogen at 380 Torr. During the annealing, a weight is placed on top of the bonding pair to produce a pressure of ~150–250 g/cm^2. It has been found that (111) InP can form strong bonds with GGG at temperatures as low as 450°C, while (100) InP needs annealing temperatures higher than 600°C.

The bonding of small samples (5 × 5 mm^2) of InP to GGG covered with GaInSb or a rare earth garnet $(LuNbBi)_3(FeAl)_5)_{12}$ layer at 675–750°C has also been reported (10).

12.4 SURFACE PROTECTION OF SEMICONDUCTOR WAFERS

Silicon wafers are generally transported and stored in plastic wafer boxes. The plastisizers in these boxes may lead to unacceptable organic contamination (i.e., hydrocarbons) of the polished silicon surface (11) and undesirable device properties. Reversible room-temperature bonding of bare silicon

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wafers has been suggested as a method to prevent contamination associated with transport and storage in plastic boxes (12). Room-temperature bonding of dissimilar materials can also be used to protect the respective surfaces against contamination. Moreover, bonding brittle compound semiconductor wafers to silicon wafers can protect them from brittle fracture due to mechanical shock during transport (12).

The wafer surface protection should best be obtained through bonding of wafers with *hydrophobic* surfaces because the bonded interface is stable up to at least 200°C and the surface energy is only in the range of 20 mJ/m^2, which is desirable for easy debonding immediately before device processing (13). If wafer bonding is prepared by hydrophilic surfaces, as discussed in Chapter 5, after storage at room temperature for a certain period of time, both an increase in surface energy and interface bubble generation may occur. A fairly high temperature (around 100°C) and long storage period could unintentionally occur during the transport of reversibly bonded wafers from manufacturers to wafer users. An increased surface energy and interface bubbles are obviously undesirable. Fortunately, as described in Chapter 5, a safe region of storage exists, as shown in Fig. 5.15. Storage at below 110°C can keep wafer pairs basically in the hydrogen-bonding mode and storage time less than a critical period can prevent bubble generation.

The bonded wafers have to be separated again immediately before use in device processing. The wafer pairs can be separated by inserting a blade or a wedge into the edge of a wafer pair. As discussed in Section 4.9, inserting a wedge into the bonding pair in water can increase the crack length significantly, leading to an easy debonding in the case of bonded hydrophilic wafer pairs. Another possible way to separate bonded hydrophobic silicon wafers without the insertion of a wedge appears to be the following: After placing a tiny water droplet on the two hydrophobic silicon wafers, the wafers are bonded while including the water in a small area at the interface. For debonding, the bonded wafers are heated by microwaves to over 100°C so that the enclosed water evaporates and opens up the two wafers. The reliability and the detailed technical handling of this method still have to be investigated.

12.5 NEW MATERIAL COMBINATIONS

12.5.1 Infrared Window Protection Using Si on ZnS Bonding

The compound ZnS is widely used as an IR-transmitting window for airborne imaging and sensing applications. Although the material is capable of withstanding moderately harsh environments, severe surface and substrate damage occur when ZnS is subjected to high-speed rain and sand impacts, as are encountered in military airplanes that operate in the high subsonic and supersonic regimes. The cost of frequently replacing or repairing these

windows is significant. Direct bonding of silicon to ZnS offers a simple solution to the problem (14).

Prime-grade 2-in. (100), 0.25- to 0.5-mm thick silicon wafers and 2-in. polycrystalline 1-mm-thick ZnS wafers were used. The ZnS wafers were polished to a RMS microroughness of ~ 5 Å and a flatness of less than 1.3 μm. Prior to bonding, the silicon wafers were cleaned in RCA1 and RCA2 resolutions and the ZnS wafers were treated in a succession of acetone, isopropyl alcohol, and DI water. The surfaces of both the silicon and ZnS wafers were hydrophilic and room-temperature bonding was spontaneous.

The surface energy of a Si/ZnS bonded pair increases with both time and increasing annealing temperature. Figure 12.6 shows that at 65°C the surface energy of a bonded Si/ZnS pair takes about 100 h of annealing time to approach a saturated value. The saturated surface energy as a function of annealing temperature is shown in Fig. 12.7. The reduction in surface energy at temperatures above about 65°C is due to the gradual buildup of elastic strain energy associated with the large difference in the thermal expansion coefficients between silicon (2.6×10^{-6}/°C at room temperature) and ZnS (6.7×10^{-6}/°C at room temperature). The Si/ZnS bonded pairs started to debond at around 150°C and separated at 400°C without apparent surface damage. The separated wafers can be rebonded. The IR transmittance in the wavelength range 2.5–50 μm mainly resembles that of ZnS since the absorption of silicon at wavelengths above about 6 μm is very weak.

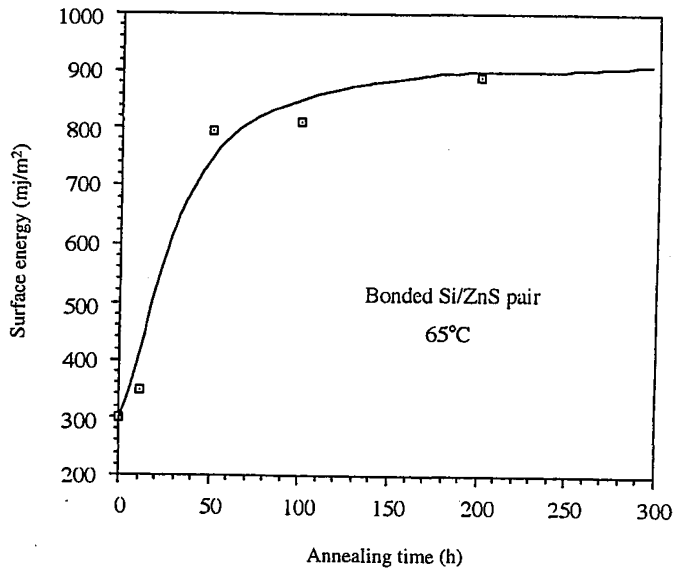

Fig. 12.6 Surface energy of a bonded Si/ZnS pair as a function of annealing time at 65°C.

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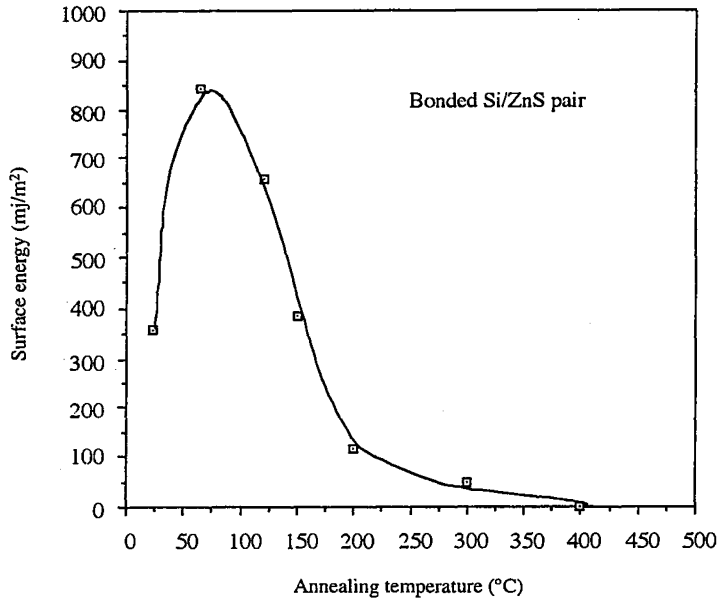

Fig. 12.7 Effect of annealing temperature on the surface energy of a directly bonded Si/ZnS pair.

12.2.2 Buried C_{60} Layers

The C_{60} molecules have received close attention in the research community because of their high symmetry and unusual properties. In combination with other elements they can be used for superconductors, ferromagnets, and photoconductors, and it is expected that a broad range of applications may be possible. It has been demonstrated that silicon wafers covered with a C_{60} layer can be bonded to silicon or oxidized silicon wafers (15).

In the study, 3-in., (100), p-type, 10–30 Ωcm polished Si wafers were used as the substrates for depositing C_{60} films by thermal sublimation of pure C_{60}. Deposition rates were in the range of 5–20 Å/min and the source temperature was ~300°C in vacuum. The C_{60} films were ~600 Å thick and were polycrystalline, consisting of randomly oriented grains with sizes of ~60 Å. The crystalline grains comprise closed-packed C_{60} molecules with a face-centered cubic (fcc) structure having a lattice constant of 12.1 Å. It is believed that van der Waals attraction is the bonding force between these C_{60} molecules, while there are covalent bonds between C atoms in the C_{60} molecules. Atomic force microscopy measurements revealed that the RMS roughness of the C_{60} surface was around 10 Å, which is a much higher RMS value than the silicon wafer. These C_{60}-covered wafers were bonded with hydrophilic bare silicon wafers (termed C_{60}/Si bonding) or thermally oxidized silicon wafers (termed C_{60}/SiO_2 bonding). During room-temperature

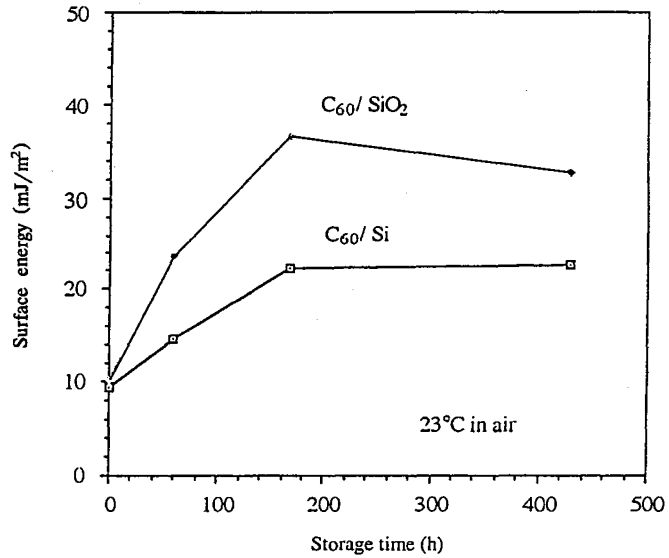

Fig. 12.8 Surface energy of C_{60}/Si and C_{60}/SiO_2 pairs as a function of the storage time at room temperature in air.

bonding, the bonded area initialized by pressing by a tong with Teflon tips did not radially spread over the entire wafer quickly. Some areas of the pair did bond spontaneously while a slight pressure on some other areas was required to help the process.

It has been found that the surface energies of both C_{60}/Si and C_{60}/SiO_2 pairs increase with the storage time at room temperature in air and approach saturated values ~200 h after room-temperature bonding. Figure 12.8 shows the surface energy of C_{60}/Si and C_{60}/SiO_2 pairs as a function of the storage time at room temperature in air. The graph reveals that the saturated interface energy of ~40 mJ/m² for the C_{60}/SiO_2 pair is higher than the value of ~20 mJ/m² for the C_{60}/Si pair. Since C_{60} and higher fullerene films can be deposited on a variety of substrates, it can be expected that mirror-polished materials covered with a C_{60} or higher fullerene layer can also bond to Si or other materials with a smooth and reactive surface. Such unique integrated materials could possibly find a wide range of applications.

12.6 BONDING INTERFACE AS A GETTERING LAYER

Because of inevitable metallic impurity contamination, an effective gettering scheme to remove impurities from the device area during device processing is vital for improving the yield in VLSI production. To control the dopant profiles as devices are scaled down to the deep submicron regime, the

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thermal budget in the VLSI fabrication has to be severely limited. Since the diffusion length of metal impurities is reduced owing to the limited thermal budget, the reduced effectiveness of the conventional wafer back-side external gettering schemes becomes an obstacle in deep submicron VLSI fabrication. Although intrinsic gettering can introduce gettering sites consisting of oxygen precipitates and associated extended defects much closer to the device regions than the back side of the wafer, the distance is difficult to control because of the required extended thermal processing, especially for n^+ wafers. Several alternative proximity gettering schemes have been suggested which can be realized by (1) high-energy implantation (16) of carbon, oxygen, boron, or silicon ions, or (2) Si epitaxial overgrowth either on a low-energy oxygen-implanted Si layer or on a germanium-doped Si layer containing misfit dislocations (17).

These gettering approaches have their own specific disadvantages, for example, the flexibility in the location of the implanted gettering layer is limited. The interface between the device layer and the implanted layer is usually not abrupt and, therefore, the potential use of implanted layers for gettering in the deep submicron range appears to be an unresolved issue. On the other end of the depth scale, even for million-electron-volt implantation, the ion penetration depth is still limited to less than 4 μm. Moreover, the defects related to ion implantation can cause an increased junction leakage. In the case of the use of epitaxial layers grown on defective surfaces, as required in approach (2), the quality of these layers is usually inferior to bulk Si. In addition, the maximum thickness of epi-layers is also restricted.

Recently, the interface of bonded hydrophilic silicon pairs has been demonstrated to provide gettering sites (18, 19). For the device layer of the bonded pairs, the sharp interface with the handle wafer, the wide range of available thicknesses (from the thickness of a wafer down to about 500 Å) and the bulk quality of the device layer are attractive features of this gettering scheme. Float-zone grown (100), hydrophilic p-type silicon wafers of 525 μm in thickness were bonded together and annealed at 1100°C for 2 h in nitrogen. The wafers were bonded with a rotational misorientation of 1° or 25°. The 1° samples had native oxide islands at the bonding interface while the 25° samples contained a continuous native oxide layer at the bonding interface. Both bonded interfaces of the silicon pairs act as gettering sites for gold. Gold atoms diffuse during the annealing step at 950–1000°C for 3 h in vacuum from one side of the bonding wafers and are gettered near the bonding interface. A continuous oxide layer effectively acts as a gettering site for gold, as did the bonding interface region consisting of oxide islands and a network of screw dislocations. Gettering of gold at temperatures as low as 700°C was observed in the interface region (20).

However, the native oxide layer at the interface of bonded hydrophilic Si pairs leads to a high concentration of charge carrier traps ($\sim 5 \times 10^{10}$–10^{12} $cm^{-2}eV^{-1}$) and high potential barriers at the interface (21). To circumvent these problems, a flexible built-in gettering layer formed by the interface of bonded hydrophobic Si pairs has been suggested and demonstrated (20). As described in Section 5.2, stable bonded hydrophobic interfaces can be obtained after only 700°C annealing. No interfacial oxide layer is present and a negligibly small series resistance is obtained even after room-temperature bonding. All silicon wafers for bonding are CZ-grown with (100) orientation. A significant segregation of gold to the hydrophobic bonding interface is found after 900°C annealing. SIMS and simulation results suggest that Si—F groups at the hydrophobic bonding interface are most likely responsible for the gettering effect via Au—F ion pairing.

12.7 RESEARCH APPLICATIONS

12.7.1 Room-Temperature UHV Bonding

Wafer bonding of commercially available 4-in. (100) silicon wafers at room temperature under ultrahigh vacuum (UHV) has been demonstrated (22). The silicon wafers are cleaned in RCA solution followed by a dip in diluted HF to remove the native oxide, resulting in hydrophobic surfaces. The silicon surfaces are covered with mostly hydrogen and a small amount of fluorine. Two hydrophobic silicon wafers are bonded at room temperature. The bonded wafer pair is transferred into a UHV chamber which is subsequently pumped down to about 3×10^{-9} Torr. The two wafers are separated in the UHV chamber and are heated at 300–800°C to desorb the hydrogen from the wafer surfaces. After cooling the two separated wafers are pressed locally by a tong operated from outside of the UHV chamber to initiate a bonded area and the bonded region spreads at very high speed ($\gg 1$ m/s) over most of the wafer area. The bonded pair cannot be separated by inserting a razor blade without breaking, indicating that strong covalent bonds have formed at

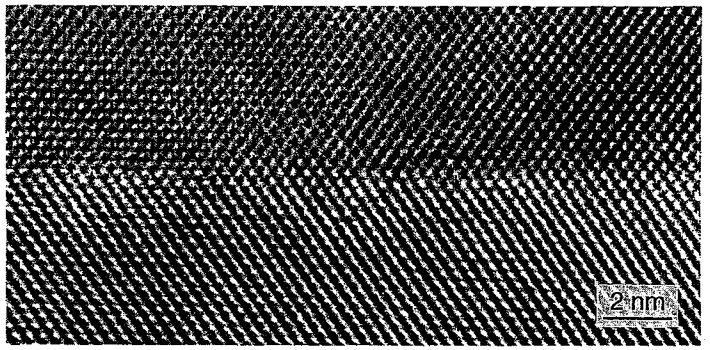

Fig. 12.9 Cross-sectional TEM picture of the interface of (100) silicon wafers bonded at room temperature in UHV without any further heat treatment.

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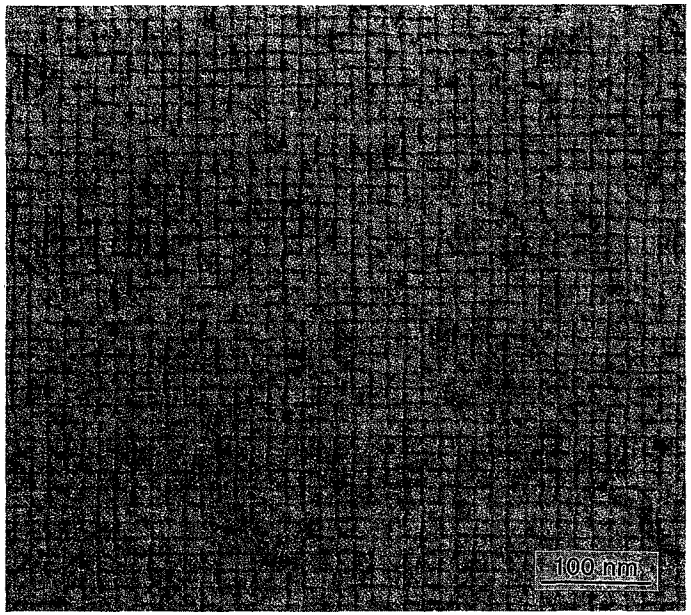

Fig. 12.10 Plan view TEM picture of the interface of (100) silicon wafers bonded at room temperature in UHV without any further heat treatment. The twist angle is around 1°.

room temperature. Figure 12.9 is a cross-sectional TEM image showing that the bonded interface contains no noticeable intermediate layer (23). Plan view images (Fig. 12.10) show the presence of a cross grid of screw dislocation, which is required to adopt the slight rotational misorientation (23). In the meantime, room-temperature UHV bonding has not only been repeated for silicon pairs but also for Si/GaAs and Si/InP pairs, although only small areas were used and a high mechanical pressure had to be applied (24).

12.7.2 Very Abrupt pn Junctions

Bonding of two lightly doped silicon wafers can produce deep and lightly doped pn junctions which are not possible to obtain by other techniques. A very abrupt and narrow impurity profile in a pn junction, such as that shown in Fig. 12.11, is highly desirable in variable capacitance diodes because of a high capacitance change efficiency. Moreover, abrupt pn junctions can increase the injection efficiency in bipolar transistors and enhance the tunneling probability of tunnel diodes. Fabrication of a pn junction with a very abrupt impurity profile based on low-temperature wafer bonding has been reported (25).

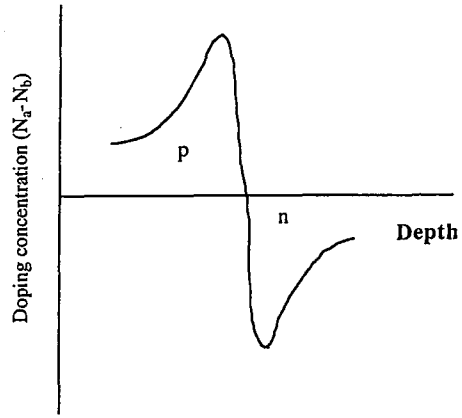

Fig. 12.11 Schematic of a very abrupt and narrow impurity profile in a pn junction.

Figure 12.12 shows the process flow for preparing such an abrupt pn junction. The silicon wafers are p- and n- type, (100), CZ, 6-in., 625-μm thick with a resistivity of 3–5 Ωcm. To avoid bubble generation at the bonding interface during annealing, trenches that are 5-μm deep and 80-μm wide are etched on the p-silicon wafer surface (Fig. 12.12*a*). The interval between two trenches is 2.5 mm. The p-silicon wafer is then oxidized to grow 1000-Å thick oxide and implanted with boron at an energy of 30 keV with a dose of $1 \times 10^{14}/\text{cm}^2$ followed by annealing at 900°C for 30 min. To shift the pn junction to be formed by wafer bonding away from the bonding interface, a lightly doped arsenic layer is implanted into the boron-doped layer with a dose of $2 \times 10^{13}/\text{cm}^2$ and an energy of 50 keV through 250 Å oxide followed by annealing at 900°C for 30 min. The small amount of arsenic doping does not form a pn junction at this stage. The n-silicon wafer is oxidized to grow a 430-Å thick oxide and is implanted with arsenic at an energy of 60 keV with a dose of $5 \times 10^{13}/\text{cm}^2$ followed by annealing at 1000°C for 30 min (see Fig. 12.12*b*). After removal of oxide layers from the silicon wafer surfaces, cleaning in RCA solution and a dip in ~49% HF for 3 min, the wafers are immersed in DI water for 30 min to replace the surface F atoms with OH groups. The wafers are dried and bonded at room temperature followed by annealing at 600°C for 30 min (see Fig. 12.12*c*). The p-silicon wafer is ground and polished to 3 μm, as shown in Fig. 12.12*d*. The wafer pair is etched in TMAH solution to form 100 × 100 μm mesa structures, (Fig 12.12*e*).

The resultant pn junctions show a very abrupt doping profile with only 420 Å from p^+-peak to n^+-peak compared with the 1200-Å pn junction formed by conventional ion implantation and diffusion under similar processing conditions. The distance from 1×10^{18} cm^{-3} to 1×10^{17} cm^{-3} is only 810 Å, which characterizes the abruptness of the doping concentration decrease

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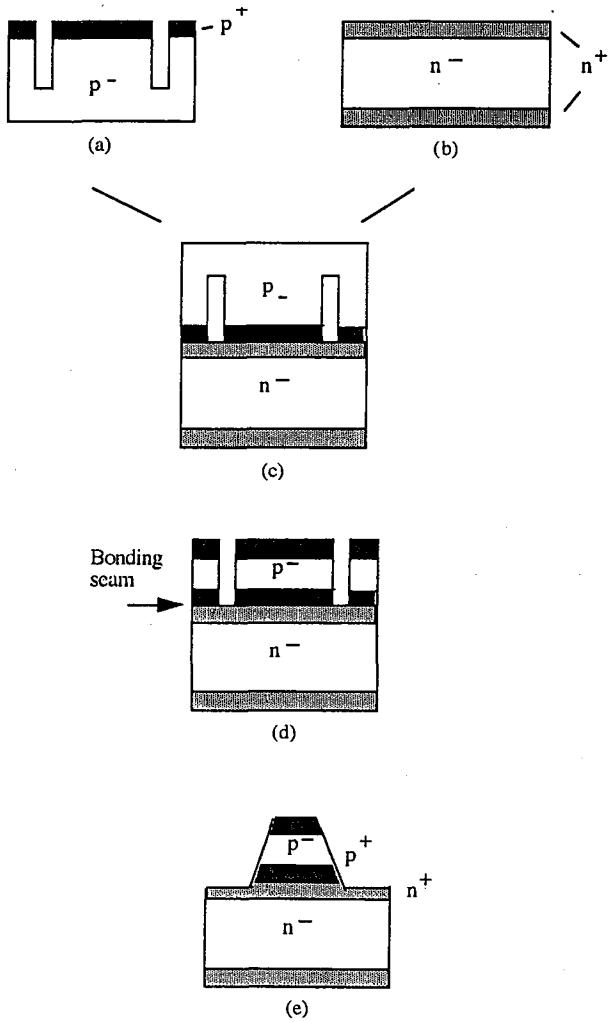

Fig. 12.12 Key process steps for preparing a very abrupt pn junction. (*a*) Trench etch + B^+ implant; (*b*) As^+ implant; (*c*) bonding + 600°C annealing; (*d*) thinning + B^+ implant; (*e*) mesa etching.

from the peak to the bulk. The distance is far smaller than the 1460 Å of conventional pn junctions.

12.7.3 Self-stressed Semiconductor Structures

During room-temperature bonding, two silicon wafers can be supported at the rim by posts in a bonding machine, as described in Section 8.3. If an external pressure is exerted on the wafers at the center of one side to initiate

the bonding, bonded wafer pairs can be formed with a defined vertical stress distribution which is dependent on the imposed curvature (see Section 8.3) (26). If the room-temperature bonding is performed while pressing the wafer pair between a stamp and a bed with a bow, the resulting wafer pair is prestressed and shows a bow which amounts to about a half that of the bed (19).

Prestressing of bonded wafers allows one to produce SOI layers under compression for enhanced mechanical stability, increased hole mobility, and decreased electron mobility (26). The method can also be employed to compensate wafer bow caused by a buried layer. It has been reported that the gettering efficiency of the prestressed hydrophilic silicon wafer pairs for copper is increased (19).

A flat CZ, (100), boron-doped, ~10 Ωcm hydrophilic silicon device wafer is bonded to a handle wafer which is bent into a convex shape and then annealed at 1100°C for 2 h in oxygen. After thinning the device wafer to 5–10 μm in thickness, residual stress is introduced at the bonding interface. The device layer is under compressive stress and the substrate is under tensile stress. The residual stress is observed as ring patterns by x-ray topography. The tensile stress appears to enhance the boron diffusion in the handle wafer around the bonding interface and the compressive stress in the device layer is relaxed somewhat by the aggregation of boron (27).

12.7.4 Fabrication of Grain Boundary Structures

Transfer of dislocation-free silicon layers from commercially available bonded SOI wafers to silicon wafers allows convenient generation and investigation of misfit dislocations at the newly formed bonding interface. In this case, hydrophobic bonding after an HF dip has to be used to avoid the presence of a native oxide at the interface. The small thickness (about 2 μm) of the transferred layer allows a much easier investigation of the misfit dislocations by TEM and EBIC (electron beam induced current) than would be possible for a bonding interface located in the middle of two wafers.

The layer-transfer procedure involving two 100-mm (4-in.) diameter silicon wafers (which are rotated against each other by a couple of degrees in order to generate a twist boundary) is similar to that for SIMOX layer transfer as described in Section 6.3. The main difference in this case is that the handle wafer is not thermally oxidized and thus would not be protected by a thermal oxide during KOH etching for removing the substrate of the bonded SOI wafer. Therefore, a thermal oxide was grown on the already bonded wafer pair during a 1100°C annealing step. The oxide on the front surface was then removed by HF before KOH etching. Because of the intentional misorientation between the two bonded wafers, the development of a square array of screw dislocations has been observed, analogous to what is shown in Fig. 12.10 for UHV room-temperature bonded silicon wafers (28). Similar observations have been also made for unthinned, bonded silicon wafers.

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12.7.5 Investigation of Surface Contamination

The detection of very small amounts of residual impurities on wafer surfaces becomes difficult because of evaporation of the impurities from the surfaces being measured during the stabilization period of the measuring beam, such as that in SIMS systems. In addition, hydrocarbons detected by SIMS on the surface may be either actual surface contaminants on the wafer or artifacts from the vacuum-pumping system. These difficulties may be circumvented by wafer bonding and thinning of identical test samples before the SIMS measurement (29).

The two wafers have to be cleaned by identical procedures and bonded to each other at room temperature followed by annealing of the bonded pair at elevated temperatures. After one wafer of the pair is mechanically or chemically thinned to about 3–18 μm in thickness, the wafer pair is cleaned again. Since the contaminants are encapsulated at the bonding interface, the primary beam has sufficient time to be stabilized before it hits the bonding interface. Therefore, those impurities on the wafer surfaces before bonding that are not significantly affected by the annealing at an elevated temperature can be detected with a much higher sensitivity.

12.7.6 Determination of Surface Topology and Surface Energy

As described in Chapters 3 and 4, 5, even small particles between two wafers may lead to large unbonded interface areas. In the situation that two wafers are identical and $h \ll t_w$, the particle size (radius h or height $H = 2h$) is (for $R > 2t_w$)

$$h = \frac{R^2}{\sqrt{\frac{2}{3}\frac{E' t_w^3}{\gamma}}} \tag{12.1}$$

where t_w is the wafer thickness, γ is the surface energy of each wafer in the pair when partially debonded, $E' = E/(1 - \nu)$, E is the Young's modulus, and ν is Possion's ratio. Since a particle of about 1 μm diameter ($2h$) leads to an unbonded area with a diameter ($2R$) of about 0.5 cm for typical 4-in. silicon wafers with a thickness of 525 μm, the amplification of particle diameter by a factor of 5000 is achieved by wafer bonding. Therefore, tiny particles may be detected.

For $R < 2t_w$, instead of Eq. (12.1) we get

$$h = 3.5\sqrt{(R\gamma/E')} \tag{12.2}$$

provided there is no elastomechanical instability, as described in Section 3.2.

For an IR image, the highest resolution for measuring the diameter of a particle is $\lambda/4$, corresponding to about 0.25 μm for the IR light used for silicon. According to Eq. (12.1), the diameter of the bubble which is caused by such a particle is about 3 mm for standard 4-in. silicon wafers. Half of this value (i.e., 1.5 mm) may be considered as the approximate lateral resolution for measuring particle size by the IR method. The resolution can be improved if a visible light-transparent wafer such as a quartz or glass wafer is used to replace one of the silicon wafers in the pair. The resolution of the particle height is $\lambda/4$, which for visible light is about 0.13 μm. The bubble diameter which is caused by the smallest detectable particle will be about 2 mm, corresponding to a lateral resolution of 1 mm.

As described in Section 3.2, the surface energy of wafers may be determined by the crack-opening method when the bonded wafers are partially separated by inserting, for example, a razor blade into the bonding interface. Therefore, wafer bonding can be used to determine the surface energy of a wafer by bonding it at room temperature to an identical wafer.

12.7.7 Formation of Uniformly Spaced Silicon Wafers

Wafer bonding has been applied to achieve a silicon wafer pair with well-defined and uniform spacing between them over the full wafer area (30). Spacings between 0.1 and 3.9 μm have been obtained and have been used to confine liquid helium in a well-defined geometry at low temperature to study the finite-size effects on the superfluid density as a function of confinement spacing. As described in Section 10.1, the size effects of cavities in wafer bonding must be taken into account in designing the spacing of the two wafers.

A desired form of confinement can be realized by bonding a silicon wafer to another silicon wafer covered with a patterned oxide layer whose thickness can accurately be controlled in the oxidation process. When the first wafer has a filling hole which is spark-cut through the wafer in the center, the bonded pair can be fed with liquid helium via the hole into the space between the two bonding wafers. The superfluid density of He at temperatures below 2.176 K can then be measured by a high-Q torsional oscillator (30).

12.7.8 Curved Single-Crystal Silicon X-Ray Analyzer

Since excellent energy resolution for scattered X-rays can be achieved by Bragg scattering from high-quality single crystals, X-ray analyzers may be made from widely available silicon single crystals. The use of analyzer crystals as focusing optics is essential for inelastic X-ray scattering. When a bent silicon crystal is used, the collection and focusing of the scattered X-rays can be realized.

To achieve high-energy resolution, earlier efforts on fabrication of a bent silicon X-ray analyzer concentrated on minimizing bending-induced strain to reduce broadening of the backscattered X-ray spectrum. A strain-free diffraction volume was obtained by grooving the crystal so that a thin back

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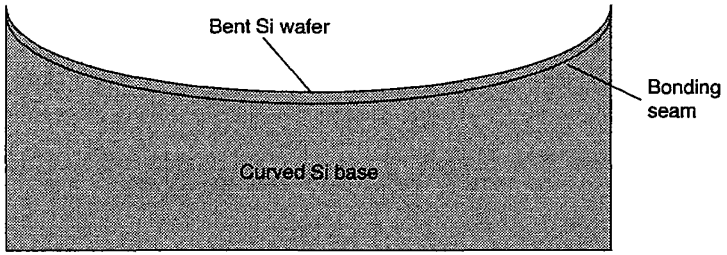

Fig. 12.13 A possible configuration of a directly bonded full-wafer spherically focusing silicon X-ray backscattering analyzer.

wall takes up the strain and leaves strain-free columns (31). However, the available front surface area for X-ray diffraction is significantly reduced. By epoxy gluing and pressing a full Ge (111) wafer 90 mm in diameter into a concave glass form having a radius of curvature of nearly 1 m, a full-wafer spherically focusing Ge backscattering analyzer was realized. An overall inelastic scattering resolution of 0.3 eV using (444) reflection was demonstrated (32). The reliability, stability, outgassing, and thermal stress concerns associated with the intermediate glue layer has pointed toward the use of a wafer direct-bonding approach. Figure 12.13 shows a possible configuration of a directly bonded full-wafer, spherically focusing silicon X-ray backscattering analyzer. Direct bonding of 3- and 4-in. diameter silicon wafers to curved silicon blankets is under active investigation, but so far no report has been published.

12.7.9 Double-Gate SOI MOSFETs

The double-gate SOI MOSFET is an attractive device structure to enhance the performance of SOI MOSFETs. The key process steps of the p^+ double-gate SOI MOSFET fabricated by wafer bonding (33) are shown in Fig. 12.14. After completing a conventional p^+ poly gate structure, a CVD oxide is deposited and polished, followed by a deposition of BPSG film (Fig. 12.14*a*). A handle silicon wafer is then bonded to the BPSG surface of the device wafer at 900°C in nitrogen. The silicon substrate of the device wafer is polished and the field oxide acts as the polish-stopper (Fig. 12.14*b*). The front gate and the source and drain are formed by conventional process steps to realize a double-gate SOI MOSFET (Fig. 12.14*c*).

The drain current, the transconductance, and the short-channel behavior are all improved remarkably. With a 600-Å thick SOI silicon layer, 110-Å thick gate oxide, and 0.17-μm gate length, the maximum transconductance of the double-gate SOI MOSFETs is over 400 mS/mm, which is about three times that of the conventional single-gate SOI MOSFETs and is comparable to that of bulk MOSFETs with 45-Å gate oxide.

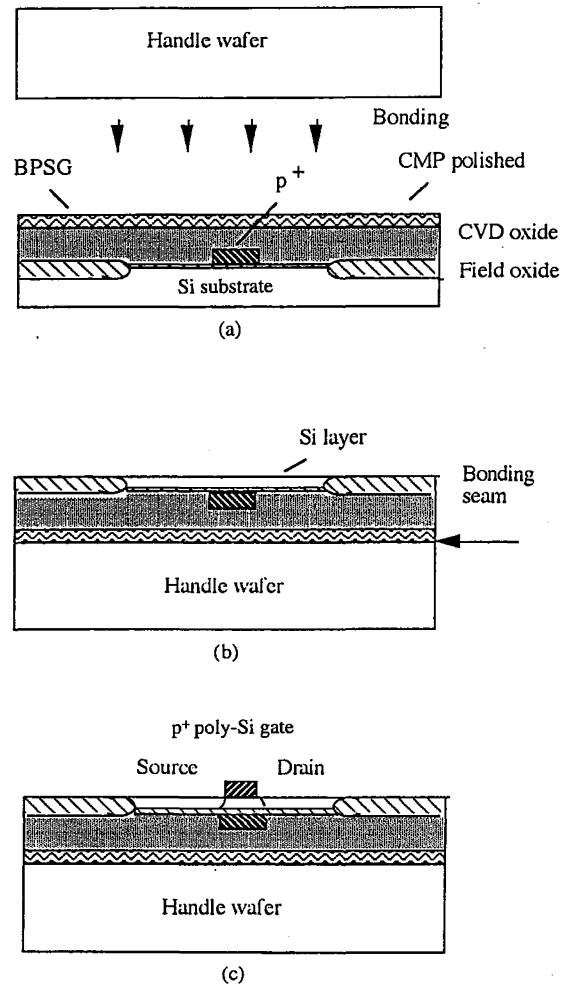

Fig. 12.14 Key process steps for preparing a double-gate SOI MOSFET. (*a*) P^+ poly Si gate, CVD oxide, and BPSG formation; (*b*) bonding and thinning; (*c*) second poly Si gate and source/drain formation.

12.7.10 "Compliant" Substrates for High-Quality Heteroepitaxial Growth

As discussed in Chapter 1, substrates consisting of a fixed thin film on a handle wafer have been used to produce high-quality heteroepitaxial films recently (34). The "compliant" layer was a single-crystalline (100) GaAs film with a thickness of 100 Å, grown on an etch-stop layer of AlAs which was grown on a (100) GaAs substrate. The ultrathin compliant layer was formed

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by wafer bonding at a rotation angle between 9° and 32° to a single-crystalline (100) GaAs wafer which produced a relaxed twist boundary consisting of a screw-dislocation network (34). After annealing to strengthen the bond at 550°C in hydrogen, the GaAs substrate with a built-in AlAs etch-stop layer was removed by a selective chemical etch in diluted NH_4OH solution. The AlAs etch-stop layer was then removed by etching in a diluted HF solution. A 3000-Å thick $In_{0.35}Ga_{0.65}P$ film was epitaxially grown on top of the 100-Å twist-bonded GaAs compliant layer at 640°C with no misfit dislocations. The thickness (3000 Å) is about 30 times the usual critical thickness. The possible interpretation of the role of the fixed-film substrate for growing high-quality lattice mismatched epitaxial films is that the screw dislocation network at the twist boundary can getter away contaminants which would otherwise generate growth-stacking faults. The screw dislocation network could also provide confined regions for the nucleation of lattice mismatch-relieving dislocations to occur without the need to leave threading dislocation segments in the heteroepitaxial film bulk (35). Such compliant substrates could possibly be fabricated based on other substrates such as InP and Si and could lead to the formation of substrates on which compound semiconductors of nearly any lattice constant and crystal structure can be grown without misfit dislocations.

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