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**Systematic Low Temperature Bonding And Its Application To The  
Hydrogen Ion Cut Process And Three-Dimensional Structures**

By

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**Dissertation**

Submitted in partial satisfaction of the requirements for the degree of

**Doctor of Philosophy**

in

Electrical Engineering

in the

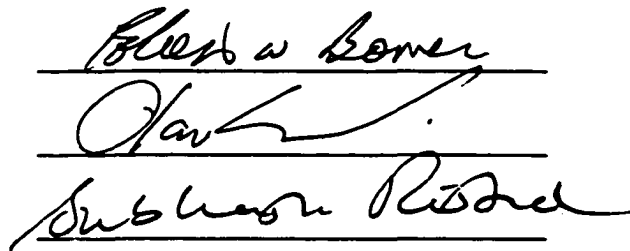
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## **Abstract**

A systematic low temperature process is demonstrated in this work. This process is improved from the earlier wafer bonding technology. It can be reproduced consistently therefore it can be implemented in the modern semiconductor industry to produce three-dimensional structures. A brief review of the revolution of modern semiconductor device, especially metal-oxide-semiconductor (MOS) device, is given. Three-dimensional electronic devices are considered the next generation in the IC industry. Low temperature bonding technology is a necessary approach to produce this multi-layer, multi-function electronic device. To stack the electronic devices, as well as vertical integration of different other microstructures, such as III-V based photo-electro devices, microwave devices and Micro-Electro-Mechanical-Structure (MEMS), into one single silicon based IC chip, to achieve so-called system-on-chip structure, is critical for the further development of the ultra-large-scale-integration (ULSI) technology. Some necessary approaches, such as systematic low temperature wafer bonding, reversible bonding, layer splitting and thin film transferring, copper to copper low temperature direct bonding, etc. are demonstrated, in order to make it possible for the vertical integration. Low temperature direct bonding together with reversible bonding, are the key steps to stack different pre-fabricated active device layer into one single chip. Ion-cut technology, also referred as Smart-cut<sup>®</sup> technology, demonstrated a excellent way to form thin films that can be further processed in the conventional IC microfabrication laboratory. The development of this technology, especially using boron and hydrogen co-implantation instead of using hydrogen implantation only, as of the conventional Smart-cut<sup>®</sup> technology, reduced both the implantation dose and the cutting temperature to

an acceptable level for the active device layer. Copper (Cu), considered as the key candidate of the interconnection metal for the next generation of ultra-large-scale-integrated circuit (ULSI) and giga-scale-integrated circuit (GSI), is receiving more and more attention. Cu to Cu low temperature direct bonding technology may be critical in some of the ULSI applications, not only due to its mechanical properties (e.g., high thermal conductivity for heat dissipation), but also due to the possibility of vertical integration of the multi-layer microelectronics structures for the next generation of faster ULSI and GSI devices. An easy way of Cu-Cu low temperature bonding is demonstrated in this work. Following the summary, some further work also critical for the vertical integration is discussed, such as the thin film transfer, or so-called low temperature modular lift-off technology, the possibility of implementing B-H co-implantation layer splitting in partially or fully processed device layers, etc.

**Dedicated to My Parents - Qingchang and Weihe**

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# CONTENTS

## CHAPTER 1

### **Introduction** **1**

1.1 VLSI Technology in the Past 25 Years

1.2 Three-dimensional Microelectronics

1.3 Vertical Integration Multi-layer Microstructure

References

## CHAPTER 2

### **Low Temperature Direct Bonding** **8**

2.1 Brief History of Wafer Bonding

2.2 Aligned Wafer Bonding

2.3 Mechanical Considerations of Wafer Bonding

2.4 RCA Clean

2.5 Optimization of Plasma Activation Process

2.6 Plasma Treatment and Surface Activation Energy

2.7 Three-step Systematic Low Temperature Wafer Bonding Process

## References

### **CHARTER 3**

#### **Reversible Bonding 39**

3.1 Importance of the Reworkability in Three-dimensional Integration

3.2 Possible Ways to Reverse the Bond

3.3 Analysis of the Reversible Bonding for Two Typical Cases

## References

### **CHARTER 4**

#### **Layer Splitting and Thin Film Transfer 51**

4.1 A Brief Review of Smart-cut® Technology

4.2 Hydrogen-Silicon System and Basic Mechanism of Smart-cut®

4.3 Low Temperature and Smoother Thin Film Transference

4.4 Lower Hydrogen Dose and Lower Temperature Layer Splitting

## References

## **CHARTER 5**

### **Low Temperature Copper Direct Bonding 82**

5.1 Comparison of Possible Interconnect Metal

5.2 Low Temperature Copper to Copper Low Temperature Direct Bonding

5.3 Bond Strength Test

5.4 Specific Contact Resistance Measurement

References

## **CHARTER 6**

### **Summary and Future Work 92**

6.1.Overall Scheme for the Vertical Integration of Multi-layer Microstructure

6.2.Future Work

References

## **Appendix**

### **Bonding Classification 97**

## List of Tables

Table 1.1	A few major changes for MOSFET in the past 25 years	7
Table 2.1	Optimized recipes for different plasma activation process in the low temperature direct bonding	27
Table 2.2	Experimental evidence of the effects for different plasma activation process in low temperature direct bonding	27
Table 2.3	Initial bonding results with pressure only	27
Table 2.4	Bonding samples after pressure and temperature	28
Table 2.5	Bond types before and after the third (200 °C anneal) step with or without the intermediate step (second step with both temperature and pressure)	28
Table 4.1	Monte Carlo simulation results for hydrogen implants into silicon by SRIM	68
Table 4.2	Implant boron as the catalyst material may greatly reduce both the hydrogen implantation dose and the splitting temperature.	69
Table 5.1	Comparison of properties of possible interlayer metals (ref. 3 and 4)	88
Table 5.2	Contact resistance measurement for Cu-Cu direct bonding, the contact area is 18 mm <sup>2</sup> for this sample	88
Table A.1	Bond classification, only type 4 or 5 bonds shown in IR can produce strong bonding where the bond strength is measured >1,000 ergs/cm <sup>2</sup>	99

## List of Figures

Figure 2.1 The experimental setup for aligned wafer bonding (after Bower et al., 1991)	29
Figure 2.2 Some mechanical considerations for the wafer bonding - radius of curvature, waviness and microroughness (after Bower et al., 1995)	30
Figure 2.3 AFM surface measurement shows, for commercial (100) silicon wafer, the microroughness is much below the mechanical criteria for achieving a successful wafer bonding	31
Figure 2.4 Cross sectional SEM image of aligned bonded commercial SRAMs (after Bower et al., 1993)	32
Figure 2.5 Reduction of the surface activation energy ( $E_a$ ) by applying the plasma treatment to the attempted bonded samples	33
Figure 2.6 Pressure fixture built for applying the pressure in three-step low temperature direct bonding process	34
Figure 2.7 Average initial type of bond with pressure only	35
Figure 2.8 Likelihood of Good Bond with Pressure only	36
Figure 2.9 Average type of bond after pressure and temperature treatment	37
Figure 2.10 Likelihood of Good Bond after Pressure and Temperature Treatment	38
Figure 3.1 Cross section of wafers or chips stacked in a three-dimension array with an offset when aligned bonded, so that a force can be applied along the edge	49
Figure 3.2 Rectangular chip of dimensions $d$ by $w$ , with line force $F_d$ applied	49
Figure 3.3 Circular wafer of diameter $D$ , with angular force $F_D$ applied	49

Figure 3.4 Force needed to debond a 100mm circuit bonded sample, from the calibration measurement of a 2cm × 2cm square bonded sample, where 0.5 lb force is applied on the side (Note $\alpha = 2\theta$ , can change from 0 to 90°, they represent the total length of the arc at the edge that a force is applied).	50
Figure 4.1 Smart-cut <sup>®</sup> technology to produce silicon-on-insulator material	70
Figure 4.2 Four possible hydrogen configurations in silicon (1) bond - centered (BC); (2) antibonding (AB); (3) H <sub>2</sub> <sup>+</sup> ; (4) silanic	71
Figure 4.3 Blisters at the silicon surfaces after hydrogen ion implantation.(a) $4.5 \times 10^{16}$ H <sup>+</sup> into (100) Si, 40 KeV, 425 °C, 6 hours; (b) $4.9 \times 10^{16}$ H <sup>+</sup> into (100) Si, 40 KeV, 425 °C, 2 hours; (c) $5.3 \times 10^{16}$ H <sup>+</sup> into (100) Si, 40 KeV, 425 °C, 25 minutes; (d) $5.7 \times 10^{16}$ H <sup>+</sup> into (100) Si, 40 KeV, 425 °C, 20 minutes	72-75
Figure 4.4 Proposed basic mechanism of Smart Cut <sup>®</sup> process	76
Figure 4.5 Monte Carlo TRIM-95 simulation for H <sup>+</sup> implantation into silicon	77
Figure 4.6 A 10cm diameter SOI wafer produced with a hydrogen ion cut at 420 °C after low temperature wet SRD direct bonding	78
Figure 4.7 The surface roughness of smart-cut <sup>®</sup> layers created with a normal direct bond after an Atomic Force Microscopic (AFM) picture published in a recent article (after M. Bruel et al)	79
Figure 4.8 AFM of the surface roughness low temperature bonded hydrogen cut wafer (vertical scale is 0 - 12.49 nm)	80
Figure 4.9 Process of layer splitting and thin film transfer	81
Figure 5.1 AFM surface roughness measurement. Scan range is 1 μm × 1 μm; the vertical scale is 0 to 11 nm	89

Figure 5.2 Specific contact resistance measurement experimental setup	90
Figure 5.3 I-V measurement shows very good linear relation indicates no extra contact barrier exists for this Cu-Cu direct bond	91
Figure 6.1 Overall process flow for the vertical integration of multi-layer microstructure	95
Figure A.1 Type1 bond	97
Figure A.2 Type2 bond	97
Figure A.3 Type3 bond	98
Figure A.4 Type4 bond	98
Figure A.5 Type5 bond	99



# CHAPTER 1

## Introduction

### 1.1.VLSI Technology in the Past 25 Years

The electronics industry has been experienced phenomenal growth in the past few decades. It is now become the largest industry in the world with global sales over one trillion ( $10^{12}$ ) dollars! It never has such an impact to the people in their day-to-day life. Low power, fast speed, high packaging density, high yield and low cost are always the key driven forces in the evolution of this industry. The most important device for ultra-large-scale-integration (ULSI) may be the enhancement mode metal-oxide-semiconductor field-effect transistor (MOSFET). Although reported as early as in the early 1960's (by Kahng and Atalla [1], Bower and Dill [2], etc.), it could not be fabricated properly and reliably until the early 1970's. However, since then, lots of changes happened to this simple device, Table 1.1 just listed a few major ones.

R. W. Bower summarizes one simple relation between the manufacturing fabrication cost and the device feature size in the early 1990's as following:

$$\text{Fabrication Cost} \propto 1/(\text{Feature size})^2$$

It is not surprising that the manufacturing fabrication cost is in the range of two billions nowadays when the device feature size reaches one-quarter micron. One can further easily predict that the fabrication cost will be in the range of 10-13 billion dollars when the feature size decreases to 0.1 micron in the very near future.

However, the feature size is no longer the pre-dominant parameter for the speed, performance and packaging density in the ULSI and giga-scale-integration (GSI) technology. As S. J. Hilenius stated in *Modern Semiconductor Device Physics* (Wiley-Interscience, 1998), "... we have seen various technologies become more integrated into a single chip and more and more functionality incorporated into these 'system on a chip' architectures. The future of these systems will be in the increased integration of these different structures with an ever-increasing dependence on the **three-dimensional** nature of these devices..." [3].

Should we keep on squeezing the near-saturated devices in two-dimensional as we did in the past 25 years, or should we move to the three-dimensional scheme for the next generation of ULSI and GSI? What are the advantages for the three-dimensional integration? What are the necessary approaches to achieve the vertical integration? These are the questions to be answered in this work.

## **1.2.Three-dimensional Microelectronics**

The aluminum based two-dimensional networks has been found inadequate in ULSI and GSI technology, because of the unacceptable high values of the interconnection delay (or so-called  $RC$  delay) [4, 5]. One can reduce the  $RC$  delay either by reducing  $C$  associated with the dielectric or by reducing  $R$ , while only the latter will be considered in this work. According to the simple relationship of  $R = \rho L/A$ ,  $R$  can be reduced by reducing the resistivity  $\rho$  and the length  $L$  of the interconnection metal or by increasing the cross-sectional area of the interconnections, with geometry factors also affecting  $C$ . Increasing the interconnection area has little appeal, since (a) the area occupied by interconnection lines is already an extremely large fraction of the chip area

and (b) the fabrication requirements limit the thickness of the metal (in the matter of fact, however, using other interconnect metal with higher electromigration resistance, such as copper, to replace aluminum, may be also possible to reduce the cross sectional area  $A$ , this issue will be addressed briefly in Chapter 5 of this work). Therefore, a vertical structure integrating the multi-layer is proposed in this work, the lowering of  $L$  in such schemes is achieved by using vertical interconnections that span shorter horizontal distances on selected planar levels.

The industrial standard integrated circuits (ICs) are usually two-dimensional. However, huge gain can be achieved when expand the device into three-dimensional. Take static random-access-memory (SRAM) as a simple example. Although the device dimension is kept on shrinking in the last few years, the most significant structural change is the accomplishment of extensive usage of the thin-film transistors (TFT) to allow the  $p$ -channel load transistor to be put on top of the  $n$ -channel transistor to produce a cell stacked in the third dimension. Dynamic random-access-memory (DRAM), as another example, the incredible volume increase comes from the expanding the device properly in the third dimension also, either using a deep-trench capacitor deep under the MOS transistor or using a crown type of capacitor structure above the MOS transistor.

Besides modifying the processing technology and producing the single device in three-dimensional directly, the post-single-device-fabrication three-dimensional packaging is also proposed. Packaging the conventional two-dimensional IC into three-dimensional microelectronics is always a challenging issue in the semiconductor field. The gain is huge, e.g., a two-dimensional conventional IC is about 500  $\mu\text{m}$  thick (for 10cm wafer), the active layer of this IC is only about 1 to 2  $\mu\text{m}$  thick. Thus, three-

dimensional stacked aligned bonded chips would have a density of 250 to 500 times denser than conventional chips. Moreover, the conventional IC is also mounted in a package that increases its thickness to the order of  $\geq 2$  mm. Thus, ideally speaking, the density ratio of three-dimensional to two-dimensional chips is as great as 1000 to 1!

Overall, three-dimensional microelectronics devices, comparing to their two-dimensional counterparts, have faster speed at a given feature size, much higher packaging density at a given feature size. Therefore, the cost per function is reduced and the performance is increased. Smaller manufacturing capital cost can then eventually be accomplished.

### **1.3. Vertical Integration Multi-layer Microstructures**

Silicon based integrated circuit technology has been a major factor for the semiconductor industry evolution in the past few decades. Some other important developments are those of micro-electro-mechanical structure (MEMS), III-V based photonic devices and microwave devices, etc. The integration of these technologies is a goal whose impact will be far reaching. Unfortunately, different processing lines are required for fabricating different type of devices. Thus, packaging the processed devices into one chip turns out to be the main approach for this issue.

Wafer bonding is considered the major approach for stacking different active device layer into one single chip. A systematic low temperature silicon/SiO<sub>2</sub> wafer bonding technology is developed in this work [6, 7]. The re-workability of this wafer bonding technology is also discussed and a reasonable re-work method is proposed and analyzed [8, 9]. Ion-cut technology for layer splitting and thin film transferring is developed [10], the basic mechanism of Smart-cut<sup>®</sup> is discussed [11]. A brand new

boron/hydrogen co-implantation compared with low temperature direct wafer bonding ion-cut technology, allowing a lower implantation dose and more importantly, at much lower cutting temperature, is developed [12]. Finally, copper metallization is discussed and a copper to copper low temperature direct bonding process is demonstrated [13].

## **References**

1. D. Kahng and M .M. Atalla, "Silicon-silicon dioxide surface device", *in IRE Device Research Conference*, Pittsburgh, 1960.
2. R. W. Bower and H. G. Dill "INSULATED GATE FIELD EFFECT TRANSISTORS FABRICATED USING THE GATE AS SOURCE-DRAIN MASK", Paper 16.6 International Electron Device Meeting, Washington, D.C., 1966.
3. "Modern Semiconductor Device Physics", Edited by S. M. Sze, published by Wiley-Interscience, 1998.
4. S. P. Murarka, R. J. Gutmann, A. E. Kaloyeros and W. A. Lanford, "Advanced multilayer metallization schemes with copper as interconnection metal", *Thin Solid Films*, 236 (1993) 257-266.
5. Ronald J. Gutmann, T. Paul Chow, William N. Gill, Alain E. Kaloyeros, William A. Lanford and Shyam P. Murarka, "COPPER METALLIZATION MANUFACTURING ISSUES FOR FUTURE ICs", *Mat. Res. Sco. Symp. Proc. Vol. 337*, 1994.
6. Y. Albert Li and Robert W. Bower, "Low temperature direct bonding using pressure and temperature", *Proceedings of SPIE*, Vol. 3184, June 1997, 124-128.

7. Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March), 1998.
8. Robert, W. Bower and Y. Albert Li, "Reversible low temperature direct bonds for fabrication of three-dimensional microelectronic structures", Proceedings of SPIE, Vol. 3184, June 1997, 120-123.
9. Robert W. Bower and Y. Albert Li, "Analysis of Rectangular Chip and Circular Wafer Debonding Applied to Reversible Low Temperature Bonding", to be published, 1998.
10. Robert W. Bower, Y. Albert Li and Frank Y-J Chin, "The hydrogen ion cut technology combined with low temperature direct bonding", Proceedings of SPIE, Vol. 3184, June 1997, 2-4.
11. Y. Albert Li and Robert W. Bower, "Surface Conditions and Morphology of Hydrogen Ion Cut Low Temperature Bonded Thin Film Layers", submitted to Journal of Applied Physics, August 1998.
12. Robert W. Bower, Louis LeBoeuf, and Y. Albert Li, "Transposed Splitting of Silicon Implanted With Spatially Offset Distributions of Hydrogen and Boron", IL NUOVO CIMENTO, Vol. 19, D, N. 12, 1871-1879, December 1997.
13. Y. Albert Li Robert W. Bower and Izak Bencuya, "Low Temperature Copper to copper Direct Bonding", Jpn. J. Appl. Phys. Vol.37(1998) pp.L1068-L1069, Part 2, No. 9A/B, 15 September 1998.

Issue	From	To	By	Why
Feature Size	10 $\mu\text{m}$	< 0.25 $\mu\text{m}$	Hard Work	Speed and Packaging Density
Wafer Size	10 mm	> 200 mm	Growing	Yield
Devices per Chip	25	> $2 \times 10^7$	Scaling	Speed and Packaging Density
Fab Cost (in US \$)	$10^6$	$2 \times 10^9$	Money	Money

Table 1.1. A few major changes for MOSFET in the past 25 years.

## **CHAPTER 2**

# **Low Temperature Direct Bonding**

### **2.1 Brief History of Wafer Bonding**

Wafer bonding, in order to create novel structures, is not a new technology. As early as in 1969, Wallis and Pomerantz first introduced their work on anodic bonding of glass to metal or silicon to quartz, which is also known as field-assisted bonding [1]. This process is based on electrostatic forces pulling materials together and is applicable only when at least one of the materials is insulating or covered with an insulator. The materials brought into mechanical contact are heated to an elevated temperature and an electric field is applied across the boundary. This method is used extensively in fabricating sensors and actuators especially for creating a hermetic sealed cavity. However, this method is limited to the materials, at least one of the wafers must be insulator as mentioned above. In addition to the material limitations, anodic bonding requires high voltage (200 - 2000 Volts) which is generally detrimental for use with pre-fabricated electronics devices.

Gluing is another natural, simple bonding method. Two attempted pairs are joined together with a thin adhesive “glue” layer, which usually is low temperature melting glass such as boron glass, BPSG glass, or spin-on-glass, polymer (PMMA, e.g.) glue, sometimes even low melting point metal for conductive bonding [2-7]. The intermediate layer gives good adherence between two wafers after an annealing step. Applications of gluing include an epitaxial film transfer technique for producing single



crystal silicon film on an insulating substrate [8]. The drawbacks are that the adhesive may produce a layer of unnecessary material with temperature restrictions that may impose unnecessary limitations on the composite structures.

Direct bonding, which does not require any adhesive or electrostatic field, was first performed by two independent groups in the mid 1980's. Lasky et al. reported the bonding of silicon dioxide and silicon dioxide to silicon dioxide, and Shimbo et al. reported the silicon to silicon direct bonding in 1985 and 1986 respectively [9, 10]. Direct bonding usually consists of room temperature bonding of clean and particle free, mirror-polished, flat wafer surface (either hydrophilic or hydrophobic). The initial weak room temperature bond is followed by an anneal cycle to create a permanent strong bond. The temperature of the thermal anneal cycle dictates the type of direct bonding. An anneal cycle above 700°C is usually required for this category of direct bonding, which is also called fusion bonding, thermal bonding or high temperature direct bonding [11-13].

Plasma activated low temperature direct bonding was first introduced by Bower et al in the early 1990's [14-17]. Where the attempted samples were first received a plasma treatment prelude the room temperature initial contact, following a thermal anneal at a temperature of only 90-300°C. As a well known fact, that silicon has a 0.5-1 percent solid solubility in aluminum at a temperature of 450-500°C, therefore, during heat treatment, Si will diffuse into Al, forming Al spikes in the Si. These spikes may destroy the operation of the transistor. This phenomenon is particularly severe in the LSI scheme and beyond since the junction is designed shallower and shallower. To bond pre-processed electronics device with metal line already in place, a low temperature process is required. Since the year of 1993, independent research groups developed different

methods of low temperature wafer bonding, either by sufficiently long time subsequent low temperature anneal ( $\sim 200$  hours is required at anneal temperature of  $150\text{ }^{\circ}\text{C}$ ), or by ultrahigh vacuum ( $\sim 3 \times 10^{-9}$  Torr) room temperature bonding, or by all means of plasma treatment for low temperature direct bonding [18-32]. In our research group at UC Davis, ammonia, oxygen and argon plasmas were used for the surface activation, different materials such as bare silicon,  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{TiN}$ , etc. were successfully bonded [15-17, 33-36]. Our recent experimental data (1996-97) shows that oxygen plasma activated  $\text{Si}/\text{SiO}_2$  wafers have the best bonding results (uniformity and strength), the bond strength of a uniform bonded sample usually in the range of greater than  $1,000\text{ ergs}/\text{cm}^2$ , which is as strong as that of high temperature direct bonding.

## **2.2 Aligned Wafer Bonding**

It is critical to have an aligned wafer bonding process in making the three-dimensional microstructures. Bower et al. described a mechanical fixture to implement the aligned wafer bonding process (Fig. 2.1) in 1991, where the wafer alignment of an accuracy of  $5\text{ }\mu\text{m}$  was obtained [14]. This fixture consisted basically of an infrared (IR) wafer-mask aligner system, where the two vacuum chucks hold the two attempted wafers in place, face-to-face and parallel respect of each. An infrared source generated the infrared beam shining on the etched grooves, which were used to obtain the contrast for the alignment. The monitoring system consisted of a microscope, a CCD camera and TV monitor. By monitoring the transmitted IR image, one could adjust the positions of the two wafer holders and achieve a good alignment.

## **2.3 Mechanical Considerations of Wafer Bonding**

To achieve a successful wafer bonding, the wafers have to be 1) clean and free of particles, 2) flat, where the radius of curvature should be at least 60 meters, 3) smooth, where the waviness should be less than  $10^{-6}$  and the microroughness should be less than 1nm. Several articles presented the investigations of the surface variations, and the above criteria are concluded by Bower et al. in 1995 [37]. The definitions of the radius of curvature, waviness and microroughness are shown in Fig. 2.2.

For a commercial (100) silicon wafer, an atomic force microscopy (AFM) was used to measure the surface variations [38]. The results indicate that the surface roughness  $R_a = 0.2383$  nm and the root-mean-square ( $RMS$ ) = 0.3035 nm, both of them are much below the mechanical criteria for a successful wafer bonding (Fig. 2.3). The flatness and the waviness can be measured by a DekTak 3030 Profilometer, usually the radius of curvature is  $> 100$  m, and the waviness is  $< 10^{-6}$ . Both of them are within the range for a good bonding.

A question will be immediately raised, which is "Is the fully processed IC chip with circuits good enough to do a wafer bonding?" Fortunately, the multi-layer interconnection metallization scheme in the modern IC industry (5 layers for 0.25- $\mu$ m feature size device, e.g.) requires smoother and smoother surfaces of the device after each layer in order to add the next layer and complete the whole structure. Fig. 2.4 shows a cross sectional scanning electron microscopy (SEM) image for aligned bonded two commercial SRAMs (donated by Advanced Micro Device Inc.). This picture indicates clearly that 1) the industry standard devices are flat and smooth enough for direct wafer bonding, without any extra post-planarization, and 2) only the low temperature direct

bonding process can be used in bonding the pre-fabricated devices with the metal line already in place.

## **2.4 RCA Clean**

Considering the strict mechanical criteria for the direct wafer bonding, all of the experiment in this work was completed in the cleanroom environment (Class-100) at UC Davis. RCA clean is required before any plasma activation in the low temperature direct bonding process (to all the semiconductor surfaces). The standard RCA process consists of:

1. Base bath ( $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:6$ ) at  $75^\circ\text{C}$  for 10 minutes
2. De-ionized (DI) water rinse
3. Acid bath ( $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:7$ ) at  $75^\circ\text{C}$  for 10 minutes
4. DI water rinse
5. Buffered-oxide-etcher (BOE) dip for 1 minute
6. DI water rinse
7. Spin dry

The organic contaminants can be removed in the base bath, where the acid bath can get rid of the metallic contaminants on the surface of the wafer. DI water rinse not only can rinse off the activation residues but may also be useful in getting rid of the loose particles. BOE dip is usually used for stripping off the native oxide layer. This may convert the wafer surface from hydrophilic into hydrophobic. However it was found that the native oxide layer did not necessarily affect the bonding results in this work, our plasma activated low temperature process can be applied to both hydrophilic and hydrophobic surfaces. This is because after the plasma activation process, the wafers are

always converted to hydrophilic in spite of its original state. Therefore, BOE dip may be skipped in this work. The fact of the equivalent effect of this low temperature bonding process to both hydrophilic and hydrophobic materials plays very important role in the ion-cut technology, the detailed results will be given in Chapter 4.

## **2.5 Optimization of Plasma Activation Process**

Following the RCA clean, as mentioned before, different plasmas, such as  $\text{NH}_3$ , O and Ar, were used for the surface activation process prelude the low temperature direct bonding. Either a Technics PECVD 900 series chamber for generating  $\text{NH}_3$  plasma or a Technics RIE 800 series chamber for generating O or Ar plasma was used in this work. While all the plasmas succeeded somewhat, however, one has to adjust the operation parameters such as the gas flow rate, the chamber pressure (output mass flow controller, for RIE 800 only), the power of plasma, and the activation time, to obtain the best combination in order to accomplish the best activation effect for the bonding. Table 2.1 lists the optimized activation recipes for all the three kinds of plasmas used in this work.

## **2.6 Plasma Treatment and Surface Activation Energy**

Plasma activation process changes the kinetics of strong bond formation. Possible effects of the plasma activation process to the surface includes 1) chemical reaction of the plasma and the surface material, 2) electronic charge deposition onto the surface, 3) plasma induced surface damage, which may further cause re-arrangement of the atoms on the wafer surface, and the combinations of the above three items. A set of experiment is completed, with a) both reactive plasma gases ( $\text{NH}_3$  and O) and inert plasma gas (Ar), b) initiate the bonding immediately after the plasma treatment and apply another wet surface clean (DI water rinse, in order to remove the possibly deposited charge). Table 2.2 shows

the experimental evidence of different treatment. The surface damage is obviously the common effect for all processes. It is believed that the diffusion coefficient ( $D$ ) at the bonded interface is increased by the plasma induced surface damage, which can further increase the surface activation energy ( $E_a$ ). However, although Ar gas may not directly react with Si (comparing with O and  $\text{NH}_3$ , they may chemically react with Si to form a thin layer of  $\text{SiO}_x$  or  $\text{Si}_x\text{N}_y$ ), it is possible that Ar ions remove chemisorbed water from the surface, rearrange the dangling bonds on the surface, and/or remove other contaminants on the surface, hence to introduce some sort of a chemical change to the bonding material. It is still an open question whether the physical damage or the chemical change to the surface is most critical for bonding mechanism, more experimental evidence is required before any explicit conclusion is drawn.

Figure 2.5 shows the reduction of the surface activation energy by using plasma treatment for the attempted bonded samples. It is found the bonded area of the plasma activated direct bond after initial contact of the two substrates appears to slowly grow, till the bond strength to be saturated at a certain value, e.g.  $\sim 1,000$  ergs/cm<sup>2</sup>. The rate of the growth of the bonded area is linearly related to anneal time and temperature. To produce a bond strength at the saturation value, one can either fix the anneal temperature and increase the anneal time, or fix the anneal time but use a higher anneal temperature. It is found that the anneal time follows straight lines when plotted on a semilogarithmic scale versus reciprocal anneal temperature. This type of behavior is similar to many other natural systems (e.g., diffusion rate versus temperature) and can be referred to Arrhenius expression to the relationship. Therefore, the following model is used to describe this behavior:  $\ln(t) = E_a/(kT) + C$ , where  $k$  is Boltzman's constant and  $C$  is an arbitrary

constant. Experimental data set are presented in Figure 2.5. At each data point, the bond strength is measured to be  $\sim 1,000$  ergs/cm<sup>2</sup>. The horizontal axis represents  $1000$  over anneal temperature  $T$  (in Kelvin), while the vertical axis shows anneal time  $t$  (in hours). A simple relationship between  $t$  and  $T$  is then presented as:

$$t = t_0 \text{Exp}(-E_a/kT) \quad (2.1)$$

One can easily obtain the surface activation energy ( $E_a$ ) by calculating the slope of the  $1000/T$  vs.  $t$  curve. The experimental data indicates that, in the earlier high temperature direct bonding,  $E_a$  is about 0.72 eV, it is reduced gradually in different plasma activation process for treating different bonded surfaces, and the latest results (1996-97) show that  $E_a$  is only  $\sim 0.3$  eV for oxygen plasma activated Si/SiO<sub>2</sub> surfaces.

Conclusively, the surface activation energy is greatly reduced by plasma activation the bonded surfaces, much less energy is required to enhance the strong bond formation, therefore, the final thermal anneal temperature can be also greatly reduced.

## **2.7 Three-Step Systematic Low Temperature Wafer Bonding Process**

To implement a technology into the semiconductor industry, it has to be (1) able to fabricate reproducibly with a consistent high yield, and (2) reliable after long enough period of time after the fabrication. Earlier work of direct wafer bonding is always initiated by a pair of tweezers, and it was very dependent of a good deal of artistic talent of the operators and hard to reproduce consistently. Furthermore, it is hard to imagine that this tweezers-initiation can be applied in making a mass production in the IC industry. Therefore, a systematic method must be developed in order to make it possible to adopt this low temperature direct bonding technology into the daily routine IC fabrication [35, 36].

A systematic three-step process to low temperature direct bond silicon and/or SiO<sub>2</sub> surfaces was developed. The process activates the surface with ammonia, argon or oxygen plasma. While these activation processes allow a very strong low temperature bond to be created, they require techniques distinctly different from those found in previous work for reproducible results. The plasma processes do not result in a bond that propagates as a wave resulting from a point source initiation. A substantial pressure is required to initiate the bond. It is found that a three-step process using pressure and temperature results in very strong, reproducible bonds.

As mentioned above, the processes used to create strong, direct bonds differ considerably by various researchers. Work that is reported in several articles describes a process where a wafer bond with H<sub>2</sub>O precursor is initiated from pressure applied at a point source that propagates across the surface, as if a wave spreads out from the initial contact point across the entire surface. This point source initiation is also reported to produce void free bonds for sodium silicate bonded surfaces. It has also been the experience in our research group that bonds formed with an H<sub>2</sub>O precursor can be effectively initiated at a point that generates a wave that propagates across the surface. However, a number of papers that describe direct bonds to silicon make no reference to propagation of a surface wave propagating from a point. The bonds reported in these articles, however, do not result from an initial water bond. No reference to contact waves is found in the initiation of bonds that form after plasma activation. Plasma activated low temperature bonds have been described in earlier publications, without the initial bond forming from a wave propagating across the surface. While plasma activated low temperature bonds do not propagate as a wave, this technique does require the application



of considerable pressure applied over a substantial portion of the surface. In past plasma activated low temperature bonding work this pressure has been applied with tweezers and involved a good deal of artistic talent to generate successful bonds. Here, a systematic procedure has been developed that results in reproducible strong bonds after a low temperature anneal.

The bond is initiated by the application of a uniform pressure to the samples being bonded. It is known from earlier work that the initial plasma activated low temperature bonds are weak and require substantial pressure to initiate. In fact, the initial bond produced in the plasma activated low temperature bonding process is much weaker than generally found in a conventional process with water bonds. As a result of this weak initial bond the pair has often debonded due to the shear forces during the thermal shock of the final anneal step before a strong bond can develop. Therefore, a systematic three-step process was developed using plasma activation to avoid:

- 1) The artistic nature of the tweezers pressure application.
- 2) The debonding of the initial plasma activated pair due to thermal shear fracture of the weak bond.

In order to accomplish:

- 1) Possible mass production with consistent high yield in the IC industry.
- 2) Good reliability for a long period of time.

The following three-step systematic process has been developed for oxygen plasma activated low temperature bonding. It is found that the application of pressure in the first two steps of this process is essential for the generation of a uniform strong bond on clean semiconductor surfaces. The three-step process consists of:

1. **Pressure.** A pressure of greater than  $2.1 \times 10^5$  N/m<sup>2</sup> applied for 10 minutes was found to be necessary for a high likelihood of a uniform bond.
2. **Pressure with temperature.** The application of a pressure of greater than  $4 \times 10^5$  N/m<sup>2</sup> at a temperature of 200 °C, for a period of 30 minutes was found to overcome the tendency of the pieces to debond during a final anneal process. It was found that while this intermediate pressure and temperature step did not produce a strong bond, it was strong enough avoid debonding when followed by a final anneal.
3. **Temperature.** While the intermediate (step 2) pressure and temperature anneal produced a high likelihood of a uniform bond, the strength of this bond was weak. A final anneal of 200 °C for 10 hours increased the bond strength greater than that of a normal high temperature direct bond or  $>1,000$  ergs/cm<sup>2</sup>.

Similar three-step process has also been found appropriate for both ammonia and argon plasma activated low temperature bonding, with variations in the required pressures for step 1 and 2.

The following process is completed in a class-100 cleanroom of UC Davis to reduce the particle count to the lowest level. 100-mm commercial Czochralski (CZ) (100) silicon wafers are used in this work. The wafers are n-type with a resistivity of 1-2 ohm-cm and thickness of 500-550  $\mu$ m. The wafers are then cut into 2cm  $\times$  2cm square samples. All attempted bonding samples receive a regular RCA clean, as described in the previous section (2.4). BOE dip produces no observable difference in bonding results, which implies that this process works for both bare silicon and SiO<sub>2</sub> surfaces. The samples are dried in a N<sub>2</sub> gun after the final DI water rinse. A Technics 800 series Micro Reactive Ion Etcher (RIE) is used for the surface plasma activation process. The

samples, which are handled by vacuum tweezers only during the whole process (this prevents any unnecessary damage on the wafer surface), are put into the chamber, bonding face up. The chamber is pumped to 6 mTorr, backfilled by oxygen at a flow rate of 10 sccm, the mass flow controller is adjusted till the pressure is at 135 mTorr. The activation proceeds at the power of 100 watts for a period of 10 minutes.

After the plasma surfaces treatment, a pair of samples is placed face-to-face into a pressure fixture shown in Fig. 2.6, where the spring is well calibrated and well controlled by turning the two knobs. The pair to be bonded is held between two perfectly flat gauge blocks, where there is a little hole in the center of each, and the pressure is applied through a stainless still ball which sits on the hole of the top gauge block. This plate is thus gimbaled by the still ball to keep the plates parallel during the application of pressure. A uniform pressure is therefore applied to the whole surface of the bonded pair.

The experimental results in Tables 2.3 through 2.5 for oxygen plasma activated samples classify the results by the nature of the infrared interference patterns seen in the bonded pairs at various stages of the three-step process. The bond type classification system rates the bond quality on a scale of 1 to 5, with the type 5 most likely to form a high quality strong bond after the final anneal (step 3) and a type 1 the least likely to form such a bond. Details of the bond type classification scheme are given in the Appendix.

Experimental results are shown in Tables 2.3, 2.4 and 2.5, they represents the results of step 1, 2, and 3 respectively in this three-step process. The raw bond type is given for each applied pressure, the average types of bond and the likelihood of producing uniform (type 4 or 5) bonds are calculated. Statistical descriptions appropriate

for the small sample sizes and the discrete, subjective bond classification system has been employed.

Table 2.3 represents the bond rating for the initial bond found as a function of pressures ranging from  $1.1 \times 10^5 \text{ N/m}^2$  to  $5.3 \times 10^5 \text{ N/m}^2$ . Column (I) gives the applied pressure, column (II) shows the classification types of bond corresponding to that pressure for each sample analyzed. The average type of bonds is calculated in column (III), and column (IV) gives the likelihood of forming a type 4 or 5 bonds, where the likelihood defined as the ratio of type 4 or 5 bonds produced compared with the total number attempted. Figure 2.7 shows a graph of these data where the bond classification improves only slightly for pressures greater than  $3.5 \times 10^5 \text{ N/m}^2$ . Figure 2.8 plots the likelihood of producing a type 4 or 5 bond and shows that a pressure of  $2.1 \times 10^5 \text{ N/m}^2$  is a pressure that has a likelihood of greater than 50% of producing a type 4 or 5 bond, while pressures greater than  $4.3 \times 10^5 \text{ N/m}^2$  have a likelihood of 80% of producing a type 4 or 5 bond.

Table 2.4 depicts the experimental data describing the intermediate step where both pressure and temperature are applied to strengthen the bond without shearing the pair. Column (I) through (IV) in Table 2.4 have the same parameters as in Table 2.3. The average type of bond corresponding to different pressure is also plotted in Figure 2.9. In this case the average bond type improves approximately linearly with pressure requiring greater than  $4 \times 10^5 \text{ N/m}^2$  for bonds better than type 4. Figure 2.10 then plots the likelihood of producing a type 4 or 5 bond with various pressures. These data illustrate that a dramatic improvement in this likelihood occurs for pressures greater than  $4 \times 10^5 \text{ N/m}^2$ .

Table 2.5 shows the type of bond produced at various points with variations in the three-step process described in this paper. Column A) is the normal process, while column C) shows the data where the second step is removed. The pairs of numbers in each column indicate the type of bond before and after the third step anneal. The final bonds in columns A) are of good quality when the bond at the intermediate step was good. Final results in column C) are uniformly poor indicating that step 2 (pressure and temperature) is of critical importance.

A systematic low silicon and/or SiO<sub>2</sub> direct bonding process using pressure and temperature is developed. Oxygen, Argon or Ammonia plasma activation was used to initiate the process. For the case of an oxygen plasma activation it was found that a pressure greater than  $2.1 \times 10^5$  N/m<sup>2</sup> is needed for step 1. A pressure greater than  $4 \times 10^5$  N/m<sup>2</sup> at 200 °C, 30 minutes was found necessary for step 2. After appropriate pressures and temperatures in steps 1 and 2 an anneal of 200 °C for 10 hours is required for the final anneal. After the plasma activates the wafer surface, the first two steps create uniform bonds, while the third step will increase the bond strength to  $> 1,000$  ergs/cm<sup>2</sup>, which is as strong as in the high temperature direct bond. The results of this investigation clearly indicate that the tweezers push can be replaced with a well-defined application of uniform pressure, provided a combination of pressure and temperature is subsequently applied. The standard three-step process follows the pressure and temperature step with a standard anneal; this is found to produce an acceptable process. However, the three-step process may be collapsed into two-step process where a relatively long anneal under pressure is found to produce an excellent bond. The bond strength was measured after a

long period storage time in air (> 6 months), no difference was found from the as-bonded samples.

As a conclusion of this chapter, the three-step process can be used in mass production with a consistent high yield (~ 80%), and the bonds are reliable after only 10 hours of 200 °C thermal anneal.

## **References**

1. George Wallis and Daniel T. Pomerantz, "Field Assisted Glass-Metal Sealing", *Journal of Applied Physics*, Vol. 40, No. 10, September 1969, 3946-3949
2. M. Kimura, K. Egami, M. Kanamori and T. Hamaguchi, "Epitaxial film transfer technique for producing single crystal Si film on an insulating substrate", *Appl. Phys. Lett.* 43 (3), August 1983, 263-265
3. Leslie A. Field and Richard S. Muller, "Fusing Silicon Wafers with Low Melting Temperature Glass", *Sensors and Actuators A21-23* (1990) 935-938
4. A. Yamada, T. Kawasaki and M. Kawashima, "SOI BY WAFER BONDING WITH SPIN-ON-GLASS AS ADHESIVE", *Electronics Letters*, 2<sup>nd</sup> January 1987, Vol. 23, No. 1, 39-40
5. A. Yamada, T. Kawasaki and M. Kawashima, "BONDING SILICON WAFER TO SILICON NITRIDE WITH SPIN-ON GLASS AS ADHESIVE", *Electronics Letters*, 2<sup>nd</sup> January 1987, Vol. 23, No. 1, 314-315
6. W. P. Eaton, S. H. Risbud, R. L. Smith, "Wafer bonding by low temperature melting glass", *Proceedings of the First International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications*, 13-18, 1991, p. 146-52

7. W. P. Eaton, S. H. Risbud, R. L. Smith, "Silicon wafer-to-wafer bonding at  $T < 200^{\circ}\text{C}$  with polymethylmethacrylate", *Applied Physics Letters*, Vol. 65, Iss. 4, p. 439-41, 25 July 1994
8. Jayant K. Bhagat and David B. Hicks, "Bonding of silicon by solid-phase epitaxy", *J. Appl. Phys.* **61** (8), 15 April 1987, 3118-20
9. Goran S. Matijasevic, Chen Y. Wang and Chin C. Lee, "Void Free Bonding of Large Silicon Dice Using Gold-Tin Alloys", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 13, No. 4, December 1990, 1128-33
10. J. B. Lasky, "Wafer bonding for silicon-on-insulator technologies", *Appl. Phys. Lett.*, **48** (1), 6 January 1986, 78-80
11. Stefan Bengtsson, "Semiconductor Wafer Bonding: A Review of Interfacial Properties and Applications", *Journal of Electronic Materials*, Vol. 21, No. 8, 1992, pp841 - 862
12. W. P. Maszara, G. Goetz, A. Caviglia and J. B. McKittrick, "Bonding of silicon wafers for silicon-on-insulator", *J. Appl. Phys.* **64**, 4943 (1988)
13. Takao Abe, Tokio Takei, Atsuo Uchiyama, Katsuo Yoshizawa and Yasuaki Nakazato, *Japanese Journal of Applied Physics*, "Silicon Wafer Bonding Mechanism for Silicon-on-Insulator Structures", Vol. 29, No. 12, December, 1990, pp. L 2311-L 2314
14. R. W. Bower, M. S. Ismail, and S. N. Farrens, "Aligned Wafer Bonding: A Key to Three Dimensional Microstructures", *Journal of Electronic Materials*, Vol. 20, No. 5, 1991

15. R. W. Bower and M. S. Ismail, "Nitrogen Based Low Temperature Direct Bonding", US patent No. 5,503,704, filed June 23, 1992, issued April, 1996.
16. Robert W. Bower, Mohd S. Ismail and Brian E. Roberds, "Low temperature  $\text{Si}_3\text{N}_4$  direct bonding", Appl. Phys. Lett. **62** (26), 28 June, 1993, 3485-87
17. V. H. C. Watt, R. W. Bower, "Low temperature direct bonding of nonhydrophilic surfaces", Electronics Letters, Vol. 30 (9), p. 693-5, 29 April 1994
18. Gudrun Kissinger and Wolfgang Kissinger, "Void-free silicon-wafer-bond strengthening in the 200-400 °C range", Sensors and Actuators A, 36 (1993) 149-156
19. Qin-Yi Tong, G. Cha, R. Gafiteanu, U. Gosele, "Low temperature wafer direct bonding", Journal of Microelectromechanical Systems, Vol. 3 (1), p. 29-35, March 1994
20. Q.-Y. Tong, U. Gosele, "Process design of low temperature wafer bonding", Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications, P. 78-95, 1995
21. Q.-Y. Tong, U. Gosele, "A model of low-temperature wafer bonding and its applications", Journal of the Electrochemical Society, Vol. 143 (5), p. 1773-9, May 1996
22. U. Gosele, H. Stenzel, T. Martini, J. Steinkirchner, D. Conrad, and K. Scheerschmidt, "Self-propagating room-temperature silicon wafer bonding in ultrahigh vacuum", Appl. Phys. Lett. **67** (24), 11 December 1995, 3614-16
23. H. Takagi, K. Kikuchi, R. Maeda, T.R. Chung, T. Suga, "Silicon wafer direct bonding at room temperature in a vacuum", Journal of Mechanical Engineering Laboratory, Vol. 50 (3), p. 53-8, May 1996



24. James a. Folta, Charles E. Hunt and Shari N. Farrens, "Low-Temperature Wafer Bonding of Surfaces Using a Reactive Sputtered Oxide", J. Electrochem. Soc., Vol. 141, No. 8, August 1994
25. Shari N. Farrens, James R. Dekker, Jason K. Smith, and Brian E. Roberds, "Chemical Free Room Temperature Wafer To Wafer Direct Bonding", J. Electrochem. Soc., Vol. 142, No. 11, November 1995, 3949-55
26. B. Roberds and S. Farrens, "An AFM study on the roughness of silicon wafers correlated with direct wafer bonding", Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications, p. 326-41, 21-26 May 1995
27. B. Roberds and S. Farrens, "An atomic force microscopy study on the roughness of silicon wafers correlated with direct wafer bonding", Journal of Electrochemical Society, Vol. 143 (7), p. 2365-71, July 1996
28. R. Stengl, K.-Y. Ahn and U. Gosele, " Bubble-free silicon wafer bonding in a noncleanroom environment", Jpn. J. Appl. Phys. 27, L2364 (1988)
29. H. J. Quenzer and W. Benecke, "Low-temperature silicon wafer bonding", Sensors and Actuators A, 32 (1992) 340-344
30. Takao Abe, Tokio Takei, Atsuo Uchiyama, Katsuo Yoshizawa and Yasuaki Nakazato, "Surface Impurities Encapsulated by Silicon Wafer Bonding", Japanese Journal of Applied Physics, Vol. 29, No. 12, December, 1990, pp. L 2315-L 2318
31. Stefan Bengtsson and Olof Engstrom, "Interface charge control of directly bonded silicon structures", J. Appl. Phys. 66(3), 1 August 1989, 1231-1239

32. H. Takagi, K. Kikuchi, and Maeda, "Surface activated bonding of silicon wafers at room temperature", Appl. Phys. Lett. 68(16), 15 April 1996, 2222-2224
33. R.W. Bower, W.Chan, L.Hong, L. LeBoeuf, Y.A. Li, and J. Lee, "Optimization of Low Temperature NH<sub>3</sub> Plasma Activated Direct Bonding", Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head, SC, June 1996
34. Robert W. Bower and Frank Y.-J. Chin, "Low Temperature Direct Silicon Wafer Bonding Using Argon Activation", Jpn. J. Appl. Phys. Vol. 36 (1997) Pt. 2, No. 5A, L527-L528
35. Y. Albert Li and Robert W. Bower, "Low temperature direct bonding using pressure and temperature", Proceedings of SPIE, Vol. 3184, June 1997, 124-128
36. Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March), 1998
37. R. W. Bower, W. Chan, L. Hong, V. H. C. Watt, "Mechanical considerations for direct bonding of semiconductor materials", Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications, p. 107-14, 21-26 May 1995
38. V. H. C. Watt, M. Moinpour, R. Bower, and R. Sundararaman, "Atomic force microscopy: a key to direct wafer bonding technology", Journal of Materials Science Letters, Vol. 14 (2), p. 96-8, 15 Jan. 1995

Gas	Power	Time	Flow Rate	Pressure	Activation Chamber
NH <sub>3</sub>	50 W	5 min	75 sccm	430 mT	Technics PECVD 900
O	200 W	10 min	10 sccm	135 mT	Technics RIE 800
Ar	100 W	10 min	10 sccm	150 mT	Technics RIE 800

Table 2.1 Optimized recipes for different plasma activation process in the low temperature direct bonding.

Plasma	Surface	Chemical	Charge	Damage
NH <sub>3</sub>	Dry	×	×	×
NH <sub>3</sub>	Wet clean after activation	×		×
O	Dry	×	×	×
Ar	Dry	?	×	×
Conclusion		?	No	Yes

Table 2.2. Experimental evidence of the effects for different plasma activation process in low temperature direct bonding

Pressure ( $\times 10^5$ N/m <sup>2</sup> ) (I)	Bond Type Data (II)	Average Type of Bond (III)	Likelihood of a 4 or 5 bonds (%) (IV)
1.1	1, 3, 3, 1, 4, 4, 3, 2, 3	2.67	22.2
2.1	5, 5, 4, 5, 4, 5, 4, 4, 4, 2.5, 1, 3, 2, 2.5, 3.5, 4, 3,	3.62	52.9
3.2	5, 5, 5, 3, 5, 4, 2, 2,	3.86	62.5
4.3	5, 4, 2, 4, 5, 5	4.17	83.3
5.3	3, 4, 4, 4, 4.5, 4, 4.5, 4, 3, 4.5, 5, 5, 5	4.19	84.6

Table 2.3. Initial bonding results with pressure only

Pressure ( $\times 10^5$ N/m <sup>2</sup> ) (I)	Bond Type Data (II)	Average Type of Bond (III)	Likelihood (%) (IV)
1.516	3.5, 3, 2.5, 2	2.75	0
2.067	2, 2.5, 2.5, 3.5, 2.5, 3.5, 3	2.8	0
2.549	3, 2, 5	3.3	33.3
3.101	4, 3.5, 3, 3, 2.5, 5, 4.5, 3.5	3.63	37.5
4.134	4, 3.5, 5, 4.5, 4.5, 5,	4.25	83.3
5.168	4, 5, 5, 5, 5, 5, 5, 4.5, 5, 5, 4.5, 4.5	4.8	100

Table 2.4 Bonding samples after pressure and temperature

Anneal results w/ step 2 (before/after) (A)	Anneal results w/o step 2 (before/after) (B)
2/3, 4/5, 2/2.5, 5/5, 5/5, 4/5, 2/2, 3/5, 5/5, 3/3, 2/3, 5/5, 2/2.5, 5/5, 4/4.5, 3/3, 5/5, 5/5, 3/4, 5/5, 4/4, 5/4, 5/5, 5/5, 2/2, 4/3.5, 2/2, 4/4, 2/4, 2/2, 2/2, 3/3, 4/4, 3/3, 4/4, 5/5, 5/5, 5/5, 2.5/2.5	5/1, 5/1, 4/1, 5/1, 5/1, 5/1, 3/2, 3/2, 2/1, 2/1, 5/1, 4/2, 4/3, 3/2, 2/3, 3/1, 5/1, 4/1, 5/1, 3/1, 5/1, 3/1, 2/2, 5/1, 5/1, 3/1, 3/3

Table 2.5 Bond types before and after the third (200 °C anneal) step with or without the intermediate step (second step with both temperature and pressure)

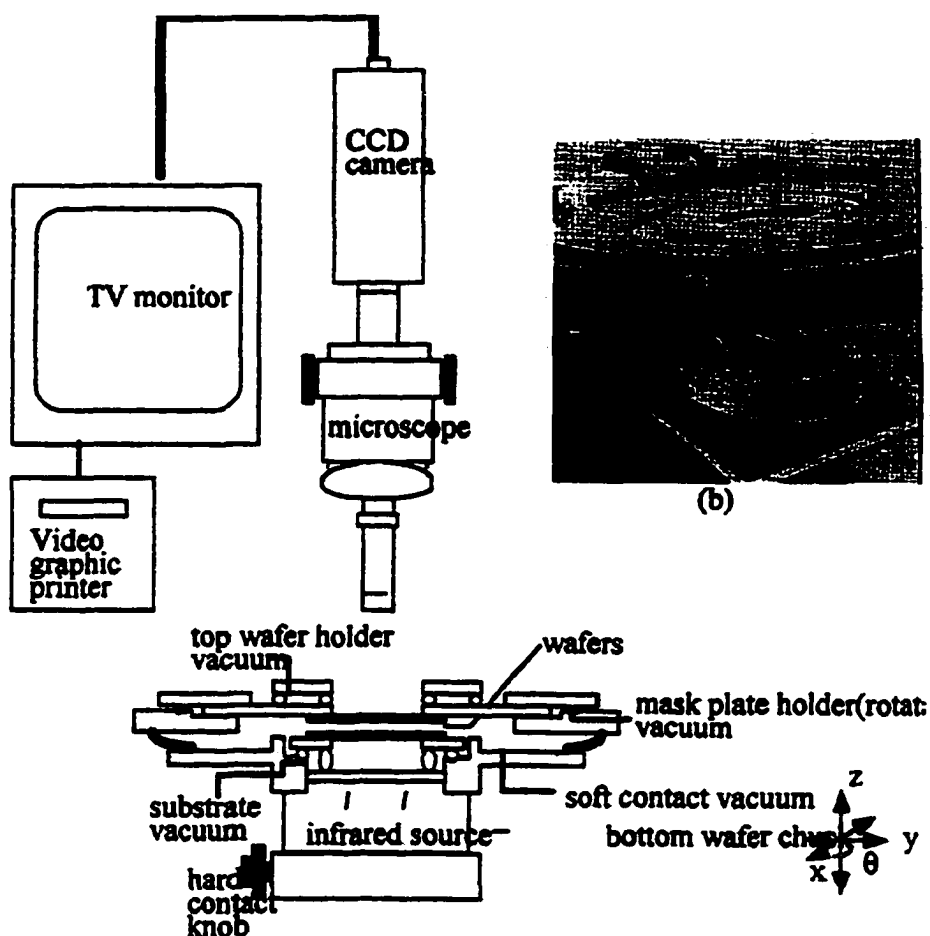


Fig. 2.1. The experimental setup for aligned wafer bonding (after Bower et al., 1991)

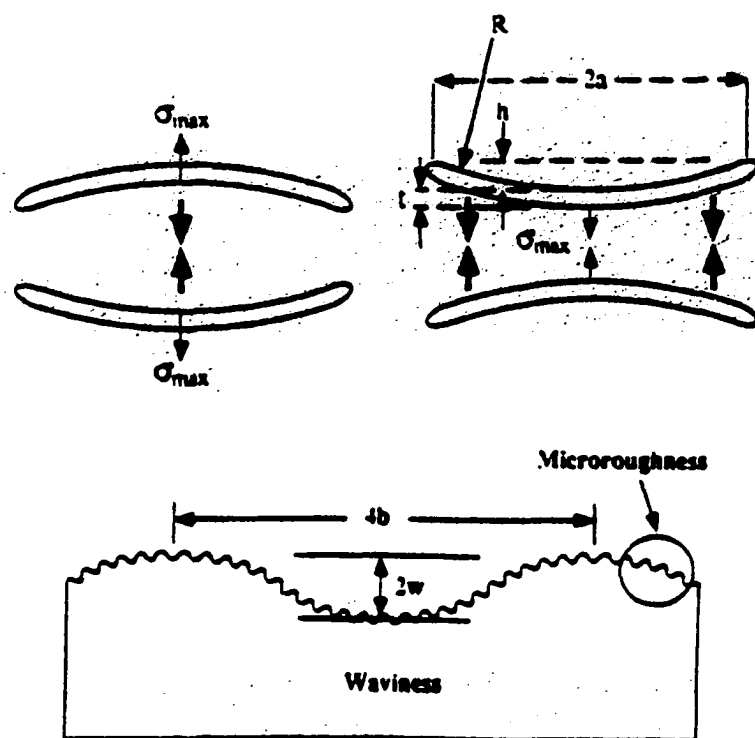
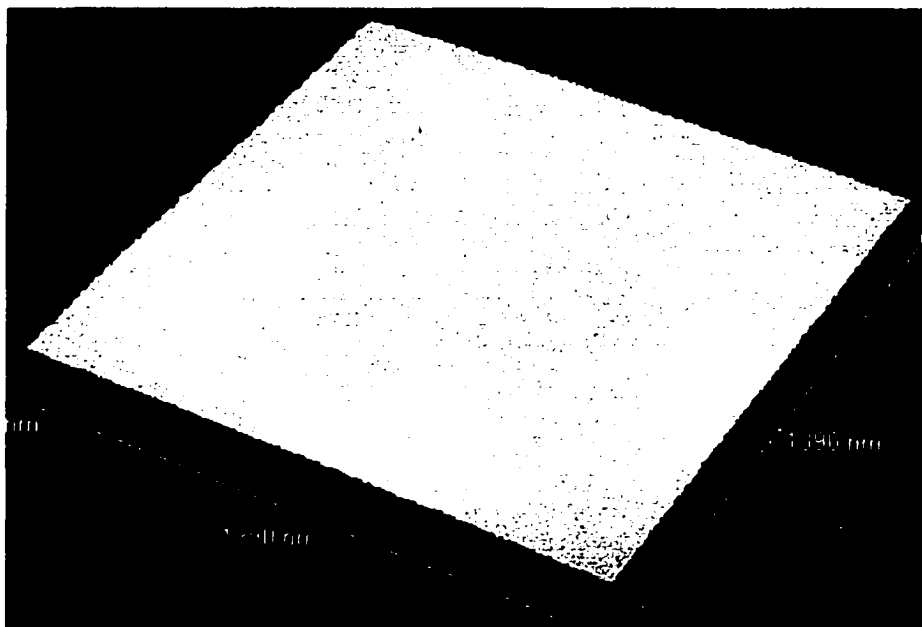
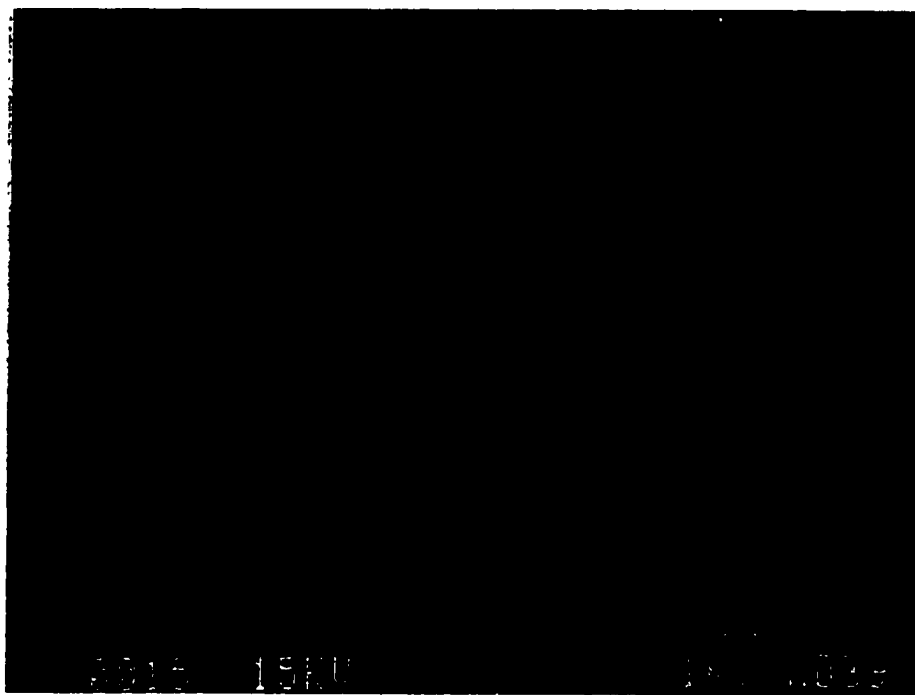


Fig. 2.2. Some mechanical considerations for the wafer bonding - radius of curvature, waviness and microroughness (after Bower et al., where the microroughness should be less than 1nm; waviness should be less than  $10^{-6}$ ; and radius of curvature should be greater than 100m for a successful direct bonding.



**Fig. 2.3. AFM surface measurement shows, for commercial (100) silicon wafer, the microroughness is much below the mechanical criteria for achieving a successful wafer bonding**



**Fig. 2.4. Cross sectional SEM image of aligned bonded commercial SRAMs (after Bower et al., 1993)**



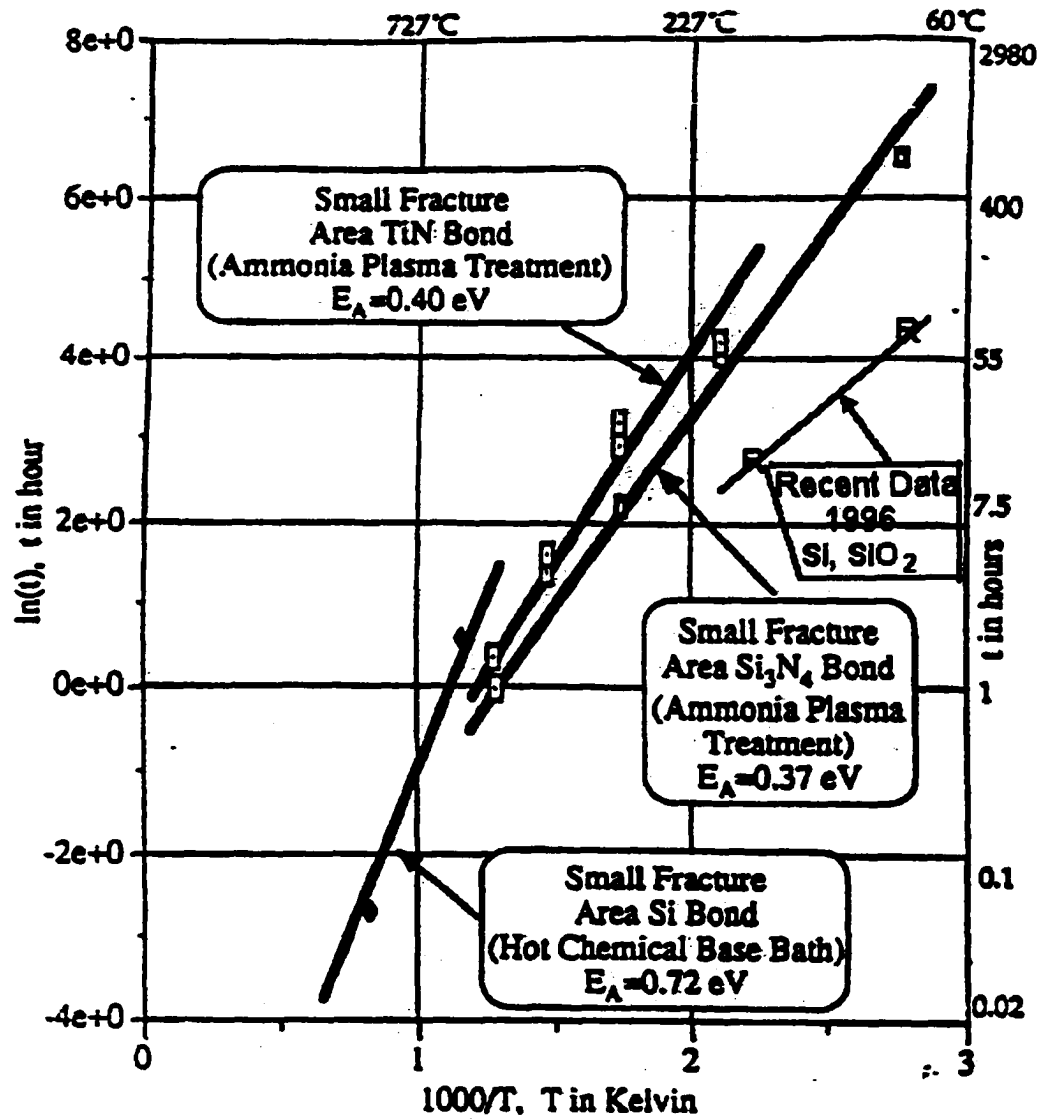
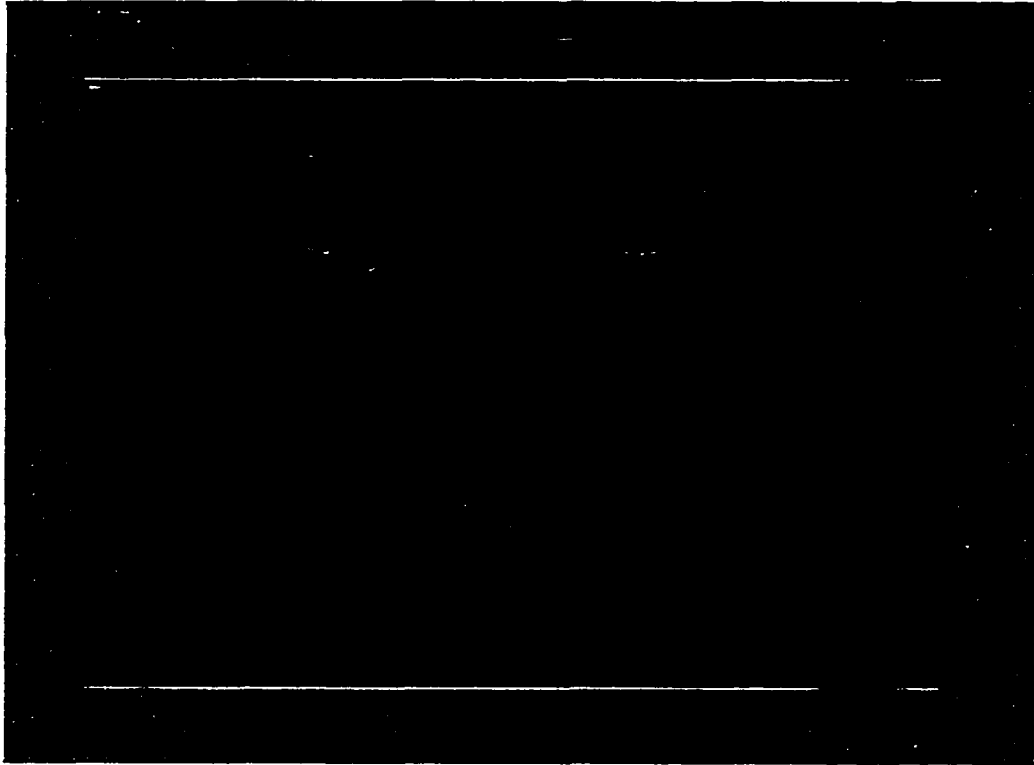


Fig. 2.5. Reduction of the surface activation energy ( $E_a$ ) by applying the plasma treatment to the attempted bonded samples



**Fig. 2.6. Pressure fixture built for applying the pressure in three-step low temperature direct bonding process.**

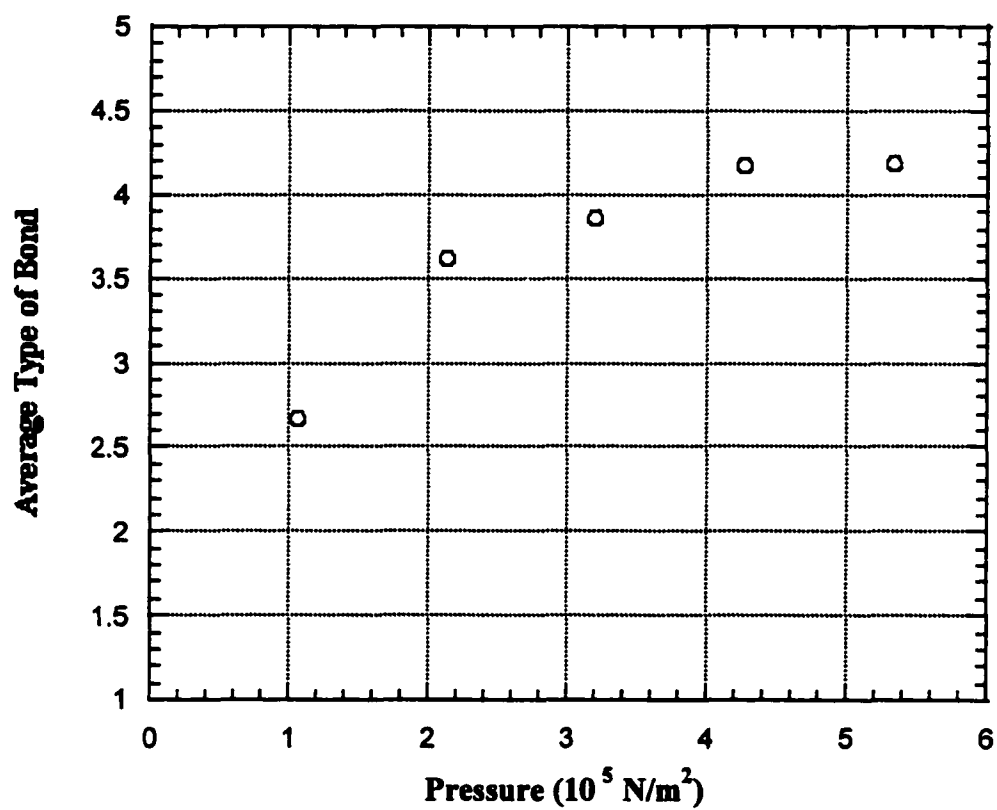


Fig. 2.7. Average initial type of bond with pressure only

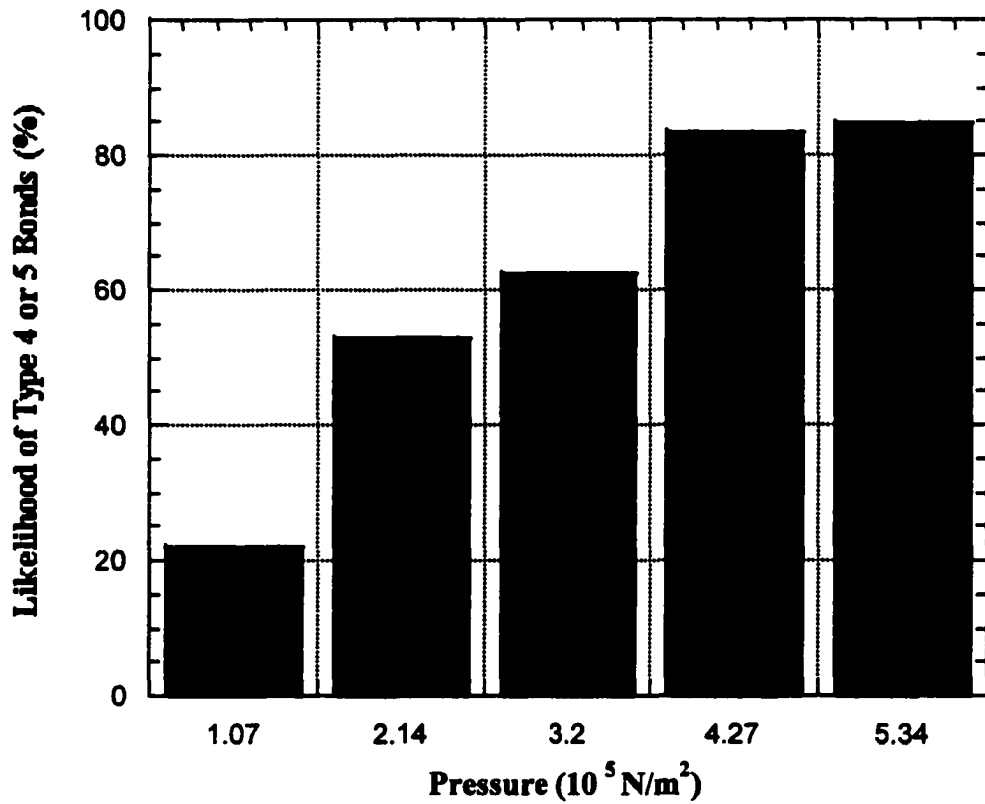


Fig. 2.8. Likelihood of Good Bond with Pressure only

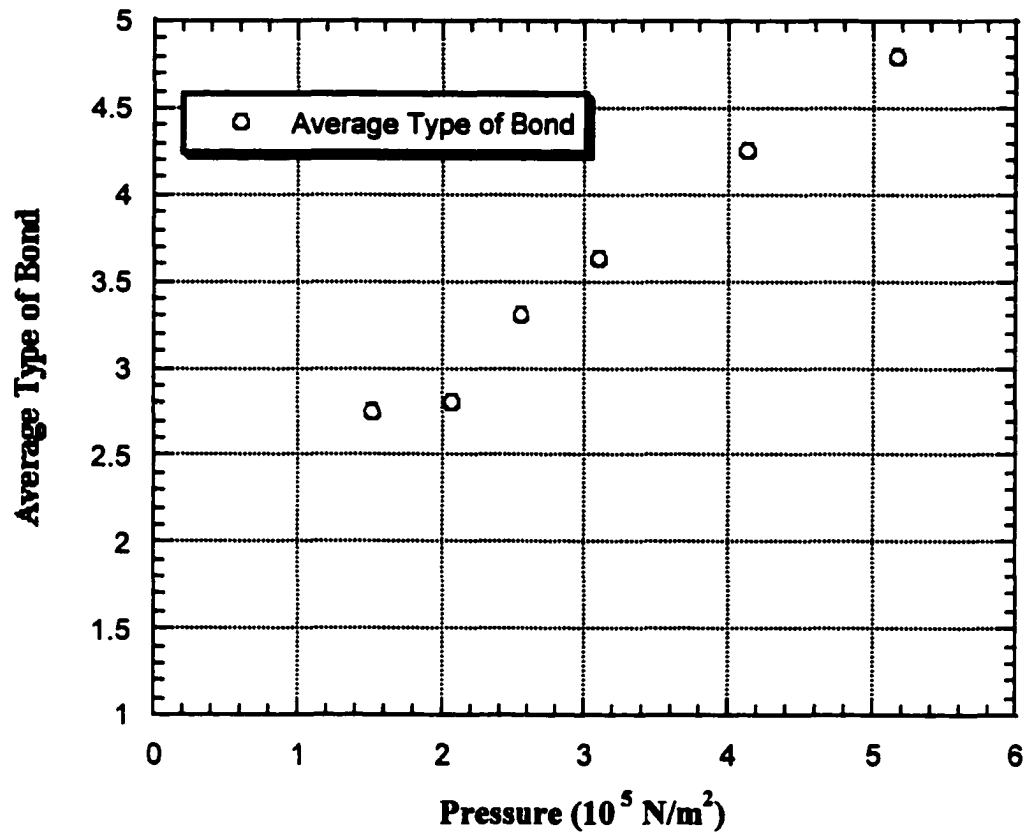


Fig. 2.9. Average type of bond after pressure and temperature treatment

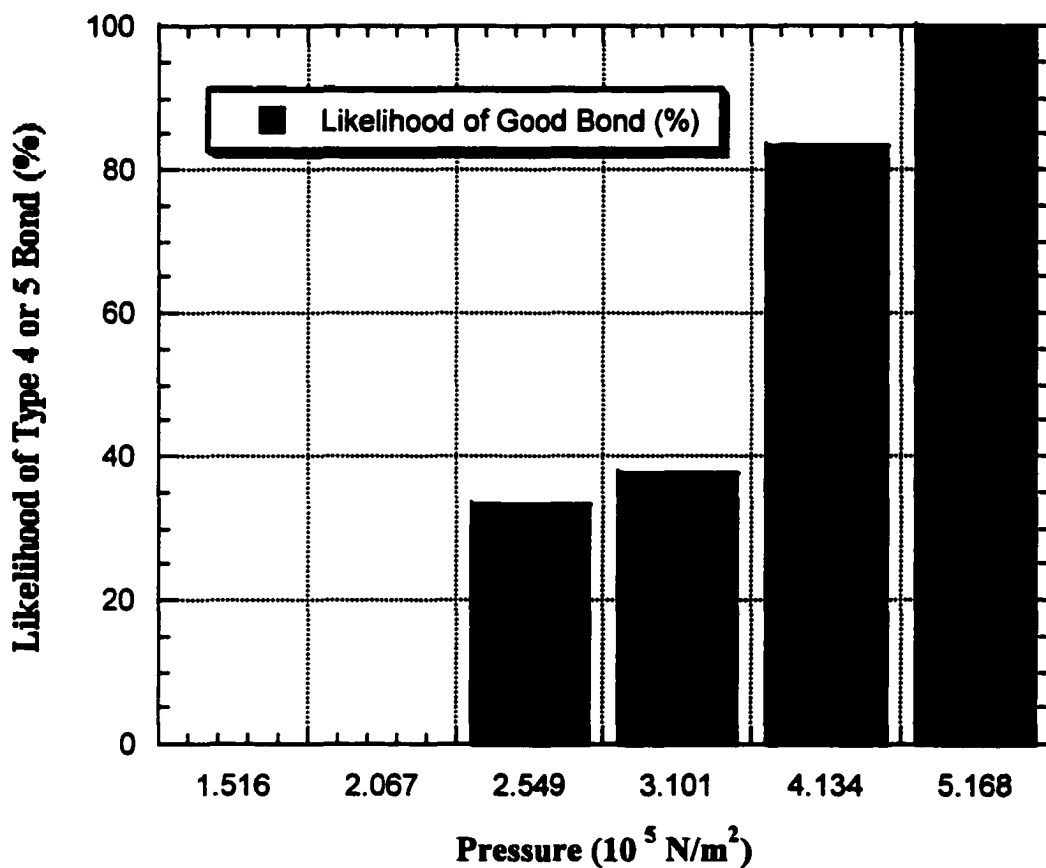


Fig. 2.10. Likelihood of Good Bond after Pressure and Temperature Treatment

## CHAPTER 3

# Reversible Bonding

### 3.1 Importance of the Reworkability in the Three-dimensional Integration

This chapter describes the formation and application of reversible low temperature bonds for fabrication of three-dimensional microelectronic structures. The basis of this reversible bond is that a partially formed low temperature bond is strong enough to be tested, but may be debonded without significant damage to the surface so a new bond may be subsequently formed. The three-step low temperature bonding process has provided an excellent approach to form this partial bond [1, 2]. This three-step process, as described in detail in the last chapter, consists of 1) pressure, 2) pressure and temperature, and 3) temperature. The first and second steps of this process create a uniform, void free, weak bond of strength less than  $100 \text{ ergs/cm}^2$  that can be easily severed. The third step consists of a long anneal (10 hours) at  $200^\circ\text{C}$  that creates a bond of strength greater than  $1,000 \text{ ergs/cm}^2$ . A thin layer of silicon (or other semiconductor such as Ge, SiC or diamond, etc) is then to be used to fabricate the various structures that will comprise the three-dimensional layered structure. A planarized layer of bondable material is then formed on the surface of the structured thin silicon-on-insulator (SOI) layer. The processed thin layer is then reversibly bonded to a conformable transfer membrane. The thin layer of processed material is then released from the bulk wafer. The thin layer of processed material is then reversibly align-bonded to the three-dimensional microstructure. The resulting composite structure is then tested. If the

system tests good the reversible bond is made permanent by completing the third step of the process and the process is repeated for the next layer. If the test fails, the top layer is removed at the reversible bond and reworked [3, 4].

Direct bonding of silicon and related semiconductor fabrication materials such as  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  and  $\text{TiN}$  has been studied extensively for the past decade [5-12]. In the early 1990's, the concept of low temperature direct bonding was introduced [13-20]. Later, in the 1996-97 period, the concept of a three-step low temperature direct bonding methodology was also introduced [1, 2]. This low temperature direct bonding process, together with the evidence of a low temperature hydrogen ion cut technology for creating silicon-on-insulator (SOI) material and capable of producing transferable thin layers of a variety of bare and processed micro-electro-mechanical structure (MEMS) and optical materials is presented. In order to utilize this technology for the formation of three-dimensional microstructures and multichip modules, it is extremely important to have a rework procedure that allows a bonded part that proves defective to be removed and replaced so that the entire structure is not rendered inoperable. This concept is important in three-dimensional structures and multichip modules because the value of the entire item becomes larger as each new element is added. Thus, near the end of the process it is very costly to allow the entire module to fail as a result of adding one new defective element. Thus, we developed a rework procedure in the form of a reversible low temperature bond into our process. The three-step low temperature direct bonding process lends itself perfectly to this concept since a weak, uniform bond is formed after the first and second steps of the process that can be easily severed.

### **3.2 Possible Ways to Reverse the Bond**



The rework requirements using a low temperature direct bond must include the following:

- a) The reversible bond must be strong enough to hold the materials together in alignment during ordinary handling.
- b) The reversible bond must be easily severed by a standardized procedure that does not damage the surfaces, so that rebonding may be accomplished with a replacement chip.
- c) The reversible bonded sample must be able to be tested *in situ* to determine whether rework is necessary.

The following three methods of reversing a bond were studied experimentally with the following results:

***1) The straight pull normal to the plane of the bonded pair.***

A force applied normal to the bonded pair was first investigated as a method to reverse a bond. It was found that this straight pull method of reversing a direct bond after step 1 or step 2 of the three-step process required forces ranging from 2 to 8 lbs/in<sup>2</sup>. The forces required were also found to be difficult to control by process variations. It was therefore decided that the straight pull method would not be used in this procedure.

***2) A twisting or sliding force in the plane of the bonded pair.***

The application of a sliding or twisting force in the plane of the bonded pair was found to be unacceptable because the surface damage caused by this action prevented rebonding of the materials.

***3) Side torque applied on the edge of the material.***

The application of a side torque to the bonded parts was found to allow the surfaces to be easily and reproducibly debonded without noticeable surface damage. Fig. 3.1 shows the bonded sample with multiple layers of active devices already in place, they are bonded with an offset upon aligned bonding. Therefore, a force can be easily applied along the edge of each layer.

In summary of the experimental analysis it is found the side torque method to be an acceptable method to debond low temperature direct bonded oxygen plasma activated samples at the conclusion of step 1 or 2 of the process. It is also found that debonded samples were not damaged and could be rebonded. Finally, it is found that these reversible bonds provided suitable electrical conduction to allow in situ testing of the bonded layer.

A number of possible manufacturing methods for applying a side torque to debond a reversible pair are possible. One such method would be to generate a notch on the top or bottom edge of each wafer or chip. A simple tool could then be inserted into the notch whereby a force normal the bonded plane could be applied by a twist or pull of the tool that applies a normal force to one side of the pair perpendicular to the bonded plane.

### **3.1 Analysis of Reversible Bonding for Two Typical Cases**

The most interesting geometries for wafer bonding are circular for wafers and rectangular for chips. The force required for debonding with a side torque applied to these geometries is considered in detail.

Fig. 3.2 illustrates the geometry of a line side torque applied to a rectangular bonded chip of dimension  $d$  by  $w$ . The line force  $F_d$  (in the unit of force/length, e.g., N/m, etc.) is applied over a length  $2h$ .

The total torque generated by force  $F_d$  can be expressed as  $2d \int_0^h F_d dy$ . By equating this integration, also note that  $h = d(\tan \alpha_1)$ , to the opposite couple of the bonded pair,  $\int_0^d w f_d x dx$ , where  $f_d$  is force generated by bonding per unit area (in the unit of force/area, e.g. N/m<sup>2</sup>, etc.), then it is easily found that the line force  $F_d$  necessary in terms of the bonding force per unit area,  $f_d$ , is given by

$$F_d = \frac{w f_d}{4 \tan \alpha_1} \text{ or } F_d = \frac{d w f_d}{4 h} \quad (3.1)$$

or the total applied force is

$$F_d 2h = \frac{h w f_d}{2 \tan \alpha_1} \text{ or } F_d 2h = \frac{d w f_d}{2} \quad (3.2)$$

Fig. 3.3 illustrates the geometry of a circular arc side torque applied to a circular wafer of diameter  $D$ . Noting that  $D=2r$ , where  $r$  is the radius of the circular wafer and  $x=D\cos^2\theta$  and  $y=D\cos\theta\sin\theta$ , similarly, we may again equate the applied force  $F_D$  per unit length to the bonding force per unit area,  $f_D$  by the integrals of their associated couple

$$\int_{-h}^h x(y) F_D dy = \int_0^D x f_D y(x) dx \quad (3.3)$$

Where LHS of Eq. 3.3 represents the torque introduced by the line force  $F_D$  on the arc of the wafer at the edge, and RHS of Eq. 3.3 is again the total torque generated by the

bonding force per unit area  $f_d$ . The integral on the left when written in polar coordinates becomes

$$2 \int_0^{\theta} D^2 F_D \cos^2 \theta (\cos^2 \theta - \sin^2 \theta) d\theta \quad (3.4)$$

which has an analytical solution

$$\frac{1}{2} D^2 F_D (\theta + \sin 2\theta + \frac{1}{4} \sin 4\theta) \quad (3.5)$$

The integral on the right when written in polar coordinates becomes

$$2 f_D \int_0^{\frac{\pi}{2}} (D \cos^2 \theta)(D \sin \theta \cos \theta)(2D \sin \theta \cos \theta) d\theta \quad (3.6)$$

which has an analytical solution  $\frac{\pi}{4} f_D D^3$ . Thus, the force necessary to balance the couple is

$$F_D = \frac{\pi D}{4\theta + 4 \sin 2\theta + \sin 4\theta} f_D \quad (3.7)$$

and since  $f_D = f_d$ , because the bonding force per unit area is a constant, we can write a relationship between  $F_D$ , the force per unit length of arc, and  $F_d$ , the line force per unit length of the rectangular case. The relationship is

$$F_D = \pi \frac{4hD}{dw(4\theta + 4 \sin 2\theta + \sin 4\theta)} F_d \quad (3.8)$$

After the debonding process, the surfaces of the materials were examined carefully under a microscope using bright light spectroscopy and found to have no visible signs of damage. The debonded materials were then RCA cleaned, reactivated in oxygen plasma and found to successfully rebond.

Fig. 3.4 shows the force conversion from a  $2\text{cm} \times 2\text{cm}$  square sample with  $0.5\text{ lb}$ . applied on one side ( $h = 2\text{cm}$ ) to a  $100\text{ mm}$  circular wafer. It is derived that by varying the total length of the force applied on the edge of the circular wafer (it can be represented by the angle  $\theta$ , or  $\alpha$ , with  $\alpha = 2\theta$ ), the force required to debond this circular bonded wafer can be significantly different, the total arc of  $\geq 60^\circ$  is preferred if we want to apply a total force  $\leq 5\text{ lb}$ .

Overall, the work described in this chapter has demonstrated conclusively that the three-step Low Temperature Bonding Procedure may be incorporated into a methodology for producing reworkable three-dimensional microstructures or multichip modules. The method of applying side torque has proven successful in debonding structures after the first or second step in the Low Temperature Bonding process. The debonded materials have been shown to have undamaged surfaces that have been successfully rebonded. A proposed tool that allows this procedure to be incorporated into a scheme for making three-dimensional structures has been described. The techniques developed in this chapter provide the basis for cost effective manufacture of direct bonded multichip modules three-dimensional structures.

## References

- 1) Y. Albert Li and Robert W. Bower, "Low temperature direct bonding using pressure and temperature", Proceedings of SPIE, Vol. 3184, June 1997, 124-128
- 2) Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March), 1998

- 3) Robert, W. Bower and Y. Albert Li, "Reversible low temperature direct bonds for fabrication of three-dimensional microelectronic structures", Proceedings of SPIE, Vol. 3184, June 1997, 120-123
- 4) Robert W. Bower and Y. Albert Li, "Analysis of Rectangular Chip and Circular Wafer Debonding Applied to Reversible Low Temperature Bonding", to be published, 1998.
- 5) Stefan Bengtsson, "Semiconductor Wafer Bonding: A Review of Interfacial Properties and Applications", Journal of Electronic Materials, vol. 21, No. 8, 1992, pp 841-862
- 6) W. P. Maszara, G. Goetz, A. Caviglia and J. B. McKitterick, "Bonding of silicon wafers for silicon-on-insulator", J. Appl. Phys. 64, 4943 (1988)
- 7) R. Stengl, K.-Y. Ahn and U. Gosele, "Bubble-free silicon wafer bonding in a noncleanroom environment", Jpn. J. Appl. Phys. 27, L2364 (1988)
- 8) H. J. Quenzer and W. Benecke, "Low-temperature silicon wafer bonding", Sensors and Actuators A, 32 (1992) 340-344
- 9) Takao Abe, Tokio Takei, Atsuo Uchiyama, Katsuo Yoshizawa and Yasuaki Nakazato, Japanese Journal of Applied Physics, "Silicon Wafer Bonding Mechanism for Silicon-on-Insulator Structures", Vol. 29, No. 12, December, 1990, pp. L 2311-L 2314
- 10) Takao Abe, Tokio Takei, Atsuo Uchiyama, Katsuo Yoshizawa and Yasuaki Nakazato, "Surface Impurities Encapsulated by Silicon Wafer Bonding", Japanese Journal of Applied Physics, Vol. 29, No. 12, December, 1990, pp. L 2315-L 2318

- 11) Stefan Bengtsson and Olof Engstrom, "Interface charge control of directly bonded silicon structures", J. Appl. Phys. 66(3), 1 August 1989, 1231-1239
- 12) H. Takagi, K. Kikuchi, and Maeda, "Surface activated bonding of silicon wafers at room temperature", Appl. Phys. Lett. 68(16), 15 April 1996, 2222-2224
- 13) R. W. Bower and M. S. Ismail, "Nitrogen Based Low Temperature Direct Bonding", US patent No. 5,503,704, filed June 23, 1992, issued April, 1996.
- 14) R. W. Bower, M. S. Ismail, B. E. Roberds and S. N. Farrens, 'One-Step Direct Bonding Process of Low Temperature Si<sub>3</sub>N<sub>4</sub> and TiN Technology'. Conference on Solid-State Sensors and Actuators (Transducers 93), Yokohama, Japan. Published in the Journal of Transducers 93 June (1993).
- 15) R. W. Bower, M. S. Ismail and B. E. Roberds, "Low Temperature Si<sub>3</sub>N<sub>4</sub> Direct Bonding", Appl. Phys. Lett., 28 June 1993 pp. 3485-3487.
- 16) Victor H. C. Watt and Robert Bower, Electronic Letts., April 1994, Vol. 30, No. 9, 693-695
- 17) R. W. Bower, V.H.C. Watt, R. Sundararaman and W. Chan, 1994 ISHM Symp., Boston., MA, Nov. 15-17.
- 18) R. W. Bower, W. Chan, L. Hong and V. H. C. Watt, "Mechanical Properties Of Low Temperature Bonded Materials", Electrochem. Soc, 1995. p. 107-14, special issue: Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications
- 19) R.W. Bower, W.Chan, L.Hong, L. LeBoeuf, Y.A. Li, and J. Lee, "Optimization Of Low Temperature O Plasma Activated Direct Bonding", Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head, SC, June 1996

- 20) Robert W. Bower and Frank Y.-J. Chin, "Low Temperature Direct Silicon Wafer Bonding Using Argon Activation", Jpn. J. Appl. Phys. Vol. 36 (1997) Pt. 2, No. 5A, L527-L528





Fig. 3.1. Cross section of wafers or chips stacked in a three-dimension array with an offset when aligned bonded, so that a force can be applied along the edge.

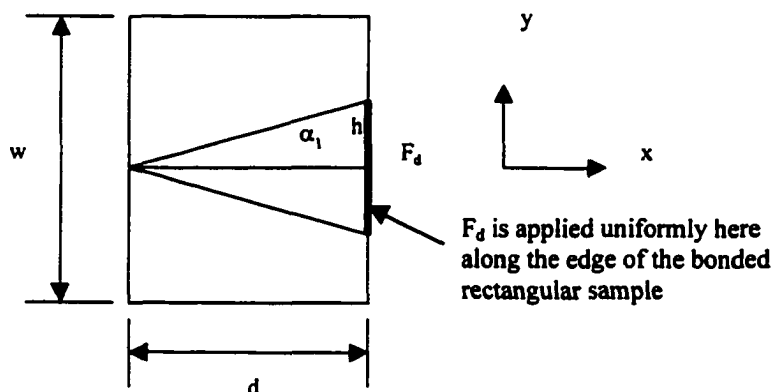


Fig. 3.2. Top view of the rectangular chip of dimensions  $d$  by  $w$ , with line force  $F_d$  applied inside the notch of the bonded sample, the force may be applied uniformly by the length of  $2h$  as shown in this figure.

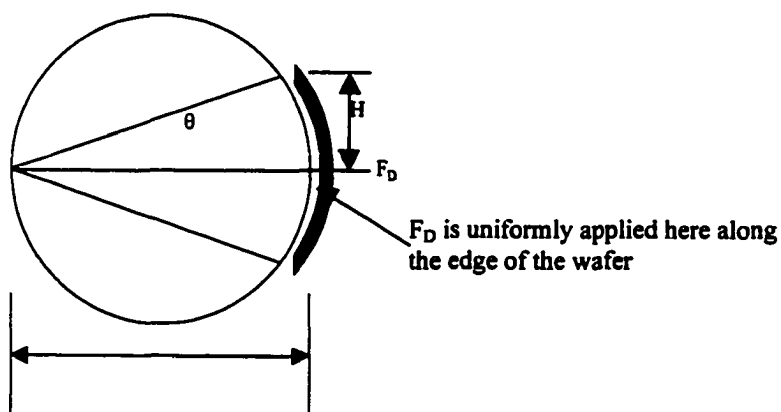


Fig. 3.3. Top view of a circular wafer of diameter  $D$ , with angular force  $F_D$  applied on the edge of the wafer,

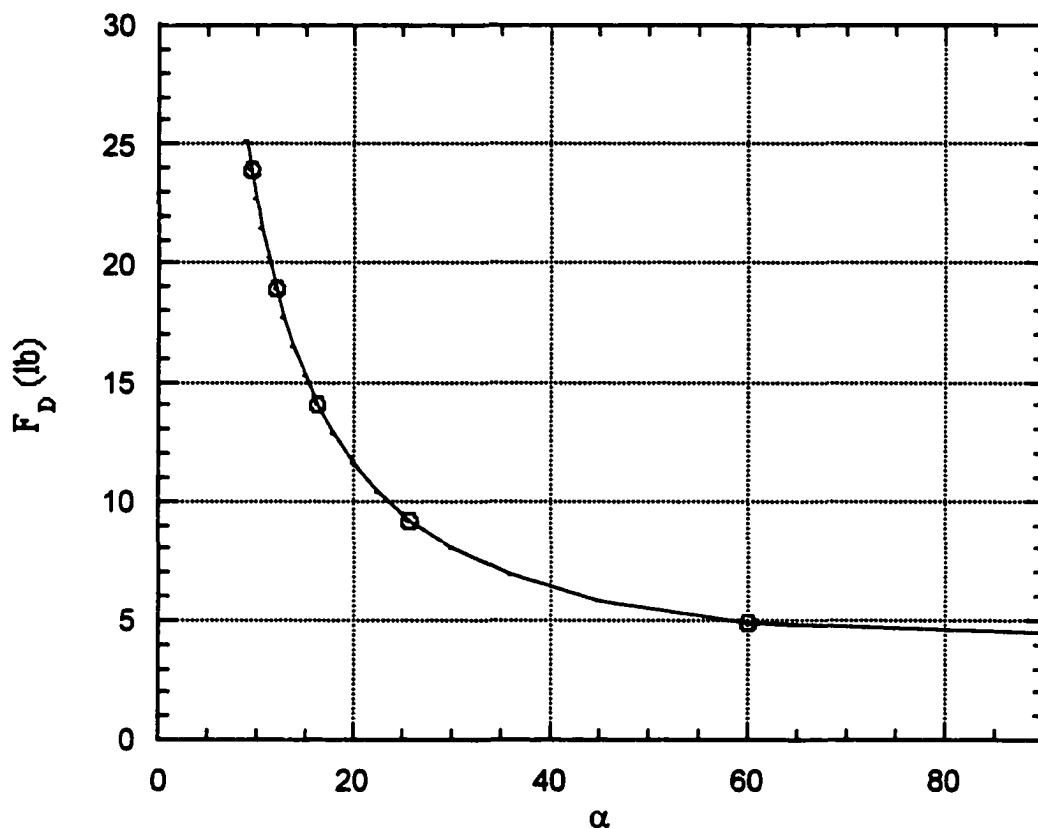


Fig. 3.4. Force needed to debond a 100mm circular bonded sample, from the calibration measurement of a 2cm  $\times$  2cm square bonded sample, where 0.5 lb force is applied on the side (Note  $\alpha = 2\theta$ , can change from 0 to 90°, they represent the total length of the arc at the edge that a force is applied).

## CHAPTER 4

# Layer Splitting and Thin Film Transfer

### 4.1. A Brief Review of Smart-cut® Technology

As described in the previous chapters, the active device layer is only in the thickness of 2-3  $\mu\text{m}$ . Therefore, it is critical to develop a method to stack the thin, single crystalline, partially or fully processed device layers onto a target substrate, where this target substrate material can be the same or different material, amorphous, polycrystalline or single crystalline, in order to provide a mechanical support or heat dissipation for the final structure.

Smart-cut® is a newly developed fabrication process for silicon-on-insulator (SOI) wafers. The advantages of the Smart-cut® technology are clearly pointed out by M. Bruel [1]. This process takes advantages of the two technologies: wafer bonding and ion implantation. The implantation enables a high uniformity of the top silicon layer thickness to be obtained whereas the wafer bonding step is intended to keep the original crystalline quality of the silicon layer unchanged. The Smart-cut® process can be detailed in the following four steps (the schematics are shown in Fig. 4.1) [2-8]:

- 1)  $\text{H}^+$  implantation (dose in mid  $10^{16}$  to  $10^{17}$  ions/ $\text{cm}^2$ ) into silicon wafer A, where this wafer is capped with a dielectric layer (e.g., thermally grown  $\text{SiO}_2$ ) before the implantation.

- 2) Hydrophilic bonding wafer A and another silicon wafer B (either bare or capped).  
Wafer B plays a key role in the Smart Cut<sup>®</sup> process as a stiffener and provides the bulk silicon under the buried oxide in the SOI structure.
- 3) Two-phase heat treatment of the bonded wafers. During the first phase (400-600 °C) the implanted wafer A splits into two parts: a thin layer of single crystalline silicon remaining bonded to wafer B; and the remainder of wafer A (which can be recycled and used as wafer A again). The second high temperature treatment phase (> 1,000 °C) strengthens the chemical bonds between the transferred layer and wafer B;
- 4) Final polishing. A chemical mechanical planarization (CMP) is necessary due to the increased surface microroughness after the splitting. A touch polishing step to smooth the top silicon surface and decrease the surface roughness value from ~100 angstroms as splitting to <1.5 angstroms is reported [5].

This Smart-cut<sup>®</sup> process is currently used in fabricating the so-called Unibond<sup>®</sup> SOI wafers in the semiconductor industry. However, it is also very promising to implement this technology into the three-dimensional electronics scheme, to produce and transfer the controlled thin film layer onto the desired target substrate and make the vertical multi-layer device structure. The following few issues should be investigated, understood and/or developed:

- 1) Hydrogen implantation induced silicon defect or the mechanism of the Smart-cut<sup>®</sup> technology;
- 2) To produce an as split smoother surface;
- 3) To reduce the hydrogen implantation dose in order to reduce the fabrication cost in order to implement this technology into mass production; And

- 4) To reduce the splitting temperature ( $>1,000\text{ }^{\circ}\text{C}$ ) in order to integrate this technology into stacking partially or fully processed device layers.

#### 4.2. Hydrogen-Silicon System and Basic Mechanism of Smart-cut<sup>®</sup>

It is summarized in a review article by G. F. Gerofolini et al. that hydrogen usually is in one of the four following configurations in single crystal silicon (Fig. 4.2) [9]:

- 1) The bond-centered (BC) configuration, typical of intrinsic or *p*-type silicon.
- 2) The antibonding (AB) configuration, where hydrogen is kept close to an interstitial tetrahedral ( $T_d$ ) position by an antibonding state of silicon.
- 3) The  $\text{H}^*_2$  configuration, resulting from pairing of close, ionized, AB ( $\text{H}^-$ ) and BC ( $\text{H}^+$ ) hydrogen atoms.
- 4) The silanic Si-H configuration, resulting from hydrogen reaction with a silicon dangling bond.

In their work, CZ (100), *p* type, with resistivity of 30-50  $\Omega\text{ cm}$  silicon wafer was used. It is pointed out, that annealing in the range 200-400  $^{\circ}\text{C}$  induces the formation of a strong displacement field (detected by RBS), quite irrespective of the target temperature during the implantation. While heat treatment at  $T < 400^{\circ}\text{C}$  does not produce appreciable hydrogen out-diffusion, heat treatment at  $T \geq 400^{\circ}\text{C}$  produce a fast hydrogen loss, terminating at saturation value. As hydrogen is gradually lost, the displacement field is progressively reduced. Once the displacement field has reached its maximum value (around 400  $^{\circ}\text{C}$ ), heat treatments at higher temperature simultaneously produce a loss of hydrogen and a reduction of the displacement field. The displacement field decreases

with  $T$  approximately like the amount of hydrogen, thus suggesting that they be strictly correlated.

It is also reported in this article, as well as quite a few others [9-13], that the extended defects in the implanted samples are  $\{100\}$  and  $\{111\}$  platelets, often observed in high-fluence hydrogen implantation, and  $\{113\}$  platelets, usually detected in silicon-implanted layers. The shape and size of the hydrogen-related platelets vary with annealing temperature, ranging from a diameter of about 7 nm in as-implanted samples (300K) to an average diameter of approximately 12 nm after annealing at 400 °C. Furthermore, by increasing the hydrogen implantation dose (the dose is low  $\sim 1.6 \times 10^{16}$  cm<sup>-2</sup>, 31 KeV H<sup>+</sup> used in their article) one can see a clear change of these bubbles in size when annealed in an elevated temperature. Fig. 4.3 shows four scanning electron microscopic (SEM) images of H<sup>+</sup> implantation induced silicon wafer surface blistering. A set of 3" commercial (100) silicon wafers is used for H<sup>+</sup> implantation. The implantation energy is fixed at 40 KeV, the H<sup>+</sup> dose are varied starting from  $2.9 \times 10^{16}$  ions/cm<sup>2</sup>, with the increasing step of  $0.4 \times 10^{16}$  ions/cm<sup>2</sup>, up till to  $5.7 \times 10^{16}$  ions/cm<sup>2</sup>. Then the samples are put onto a hot plate where the temperature can be well controlled. The surface blister becomes visible for H<sup>+</sup> implantation with a dose of greater than  $4.9 \times 10^{16}$  ions/cm<sup>2</sup>, 2 hours anneal with temperature  $\geq 425$  °C. The surface blister appears in shorter time with the same temperature anneal for higher H<sup>+</sup> dose. The size of the flaking increases from  $3.8 \mu\text{m} \times 7.5 \mu\text{m}$  for the  $4.9 \times 10^{16}$  ions/cm<sup>2</sup> H<sup>+</sup> dose sample to  $6.3 \mu\text{m} \times 8.8 \mu\text{m}$  for that of  $5.7 \times 10^{16}$  ions/cm<sup>2</sup> H<sup>+</sup> dose sample. With regard to the hydrogen bubble observation, it suggests an interaction of the higher peak concentration with more extensive damage.

Although no detailed model of hydrogen platelet structure or formation in silicon has been completely accepted, the lack of a central vacancy loop structure, known to exist in the other examples is generally accepted in the silicon case. It is suggested that platelets arise from hydrogen passivation of Si-Si bonds broken during implantation damage processes. Calculations have previously established that the bond-centered site is the most stable configuration for atomic hydrogen in a relaxed silicon lattice. Since, however, one broken Si-Si bond requires two hydrogen atoms to passivate it, we can expect a pairing effect, perhaps with the two interstitial hydrogen atoms displaced to opposite sides of the original Si-Si bond. The resulting structure of Si-H bonds could produce "planes" of hydrogen atoms. These could cause a relatively small amount of bowing in the neighboring matrix planes, resulting in the low strain contrast observed. As S. Romani and J. H. Evans pointed out in their article, that there are only about one-eighth of the implanted hydrogen would be trapped in platelets [13]. Clearly many other trapping sites must be available within the lattice for the remaining hydrogen. These traps presumably must include displacement damage defects and small vacancy-hydrogen clusters precursors to the bubbles seen at higher doses. Such structures could involve hydrogen-passivated mono, di-, and tri-vacancy centers, and with help of the elevated temperature, the microcavities grow and eventually form surface blisters.

However, when adding a stiffener on top of the hydrogen implanted silicon wafer, this blistering phenomenon does not take place locally, but instead these microcavities propagate laterally and cause the layer to split near the hydrogen implantation peak (or so-called projection range,  $R_p$ ) [14-22]. Therefore, the mechanism is proposed for the Smart-cut® process (Fig. 4.4):

- 1) Hydrogen implants into silicon wafer and form H-Si bond formation;
- 2) A damage layer centered on the damage peak is formed; this damage involves with H bubbles, and has been denoted as the interstitial loop. If the damage is enough to form an amorphous layer (which means the hydrogen fluence is high enough), certain amount of hydrogen may diffuse into the many localized platelet bubbles;
- 3) When the wafer is annealed above 400 °C, more hydrogen starts to diffuse into the already formed bubbles and cause these bubbles to grow rapidly;
- 4) High stress drives the cracks propagate laterally with the help of a bonded wafer as a stiffener. This void-free strong uniform bond is very important for the lateral crack propagation, otherwise the localized bubbles may only pop locally, and then a uniform crystalline silicon film may not be transferred to the other wafer (wafer B).

#### **4.3. Low Temperature and Smoother Thin Film Transference**

Past literature on the hydrogen ion cut technology (Smart-Cut<sup>®</sup>) has followed a procedure where hydrophilic materials are bonded at room temperature to form a weak bond [1-8]. The weakly bonded pair is then heated to 400 to 600 °C to transfer a thin film to a new host substrate, and finally the bond is strengthened with an anneal temperature of > 1,000 °C to form SOI. Later work does not explain how the bond can be strengthened without the subsequent high temperature anneal. However, to implement this layer splitting and film transferring technology into the three-dimensional electronics scheme, it is necessary to constrain the entire process under low temperature, so that partially or fully processed device layers can be cut and transferred onto the target substrate without affecting the device performance.



As pointed out in Bruel's work it is desirable to affix the hydrogen implanted thin region strongly to a bonded substrate during the transfer step. This is not accomplished with a normal high temperature bond at the cutting temperature of 400 to 600 °C. However, it is possible to form the SOI layers by using hydrogen ion cut followed by a Low Temperature Direct Bond which is described in the previous chapters of this work. In this case a bond of greater than 1,000 ergs/cm<sup>2</sup> is produced with a temperature process that does not exceed 200 °C. Thus, we have a strong bond in place before the cut process is completed and our entire process is accomplished with temperatures below 420 °C, which is the temperature for the hydrogen to start out-diffusion and bubble growth.

Hydrogen of  $5 \times 10^{16}$  to  $1 \times 10^{17}$  ions/cm<sup>2</sup> was ion implanted at room temperature with energies ranging from 22 to 100 KeV. The layer cut is produced near the penetration depth,  $R_p$ , of the hydrogen implanted layer when the dose is sufficient to cause a structural failure in the H-Si plane during this process, where  $R_p$  can be calculated and well controlled by adjusting the hydrogen implantation energy (Table 4.1 and Fig. 4.5). It is reported that the damage peak must reach a threshold value large enough to capture the implanted hydrogen in the defect structure and prevent its rapid diffusion so that H bubbles can subsequently form near the damage peak plane. In this work, hydrogen ion cut is used with a variety of plasma activated low temperature bonding procedures. The hydrogen was implanted into both bare silicon and SiO<sub>2</sub> capped samples. Low temperature bonding was induced by surface activation with ammonia, argon and oxygen plasma processes that produced bonds with surface energies greater than 1,000 ergs/cm<sup>2</sup> with anneals of 200 °C for 10 hours [23-28].

A wet and Spin, Rinse, Dry (SRD) process is successfully incorporated into the previously described low temperature plasma activated bonding processes [29, 30]. Figure 4.6 illustrates a 10cm diameter SOI wafer produced with a hydrogen ion cut at 420 °C after low temperature wet SRD direct bonding. The surface roughness as measured with an 80nm DecTak 30-30 line scan ranged from 0.9 to 1.3 nm. The center of this wafer transferred without voids, while some voids are seen on the parameter of the wafer where some hydrogen masking occurred due to the wafer holders used during the ion implantation. This wet SRD process has eliminated the voids often present in dry plasma activated processes bonded without special void reducing tools.

When the temperature is raised above 420 °C hydrogen is released from the silicon defects allowing localized platelet bubbles to grow rapidly. The high stress of the bubbles causes the cracks to propagate laterally with the help of a bonded wafer as a stiffener. This uniform stiffener is very important in the ion cut process, otherwise the H bubbles will be cracked locally instead of propagating and form a uniform thin film. A conventional direct bond that has not had a surface activation process and is not bonded at ultra high vacuum will be relatively weak with surface energies  $<500 \text{ ergs/cm}^2$  at the cut temperature of 400 to 600 °C. Since the microcavities are not located in one atomic plane but a layer with thickness corresponding to the simulated projected range straggling ( $\Delta R_p$ ), this weak, conventional bond at the cut temperature is not strong enough to prevent the bubbles to break locally. This is why a rough surface is always obtained after splitting in the conventional smart-cut® process (~100 angstroms Root-Mean-Square, RMS). However in the low temperature plasma activated bonding process, a strong, uniform bond is already in place when the temperature is elevated to above 400 °C, hence

the bond can hold till the bubbles grow laterally and split in the entire wafer. Figure 4.7 illustrates the roughness of ion cut layers created with a normal direct bond after an Atomic Force Microscopic (AFM) picture published in a recent article [5]. Figure 4.8 shows a similar AFM of low temperature bonded hydrogen cut wafer. The RMS roughness of the structure measured in Fig. 4.7 with a normal bond was reported to be ~ 10 to 13 nm, while the low temperature bonded structure in Fig. 4.8 averaged a RMS roughness of ~0.96 nm. Both of these AFM scanned a  $1\mu\text{m}$  by  $1\mu\text{m}$  area to generate the RMS roughness values given [31, 32].

The conventional Smart-Cut<sup>®</sup> process uses a normal direct bond to form the stiffener for the cut process. The cut process is preformed at a temperature under 500 °C where the surface energy is expected to be the order of 500 ergs/cm. It is suggested that this surface energy may not be enough to prevent local delamination at the bonded interface during the stage where aggregates of hydrogen atoms create regions of localized stress. It is further suggested that this would then lead to a film with a partially stiffened complainant layer resulting from the cut process. In the case of the plasma enhanced low temperature bond used in the work described in this paper the stiffener has reached a surface energy of  $>1,000 \text{ ergs/cm}^2$  by the point where the cut is formed. It is further speculated that a surface energy of  $1,000 \text{ ergs/cm}^2$  is large enough to prevent the bonded stiffener from delaminating locally during the cut process. Thus, the higher surface energy of the stiffener produced by the plasma activated low temperature bond would tend to prevent stress relief of the hydrogen perpendicular to the surface and would have more of a tendency to relieve the stress along the weakened plane of the hydrogen aggregates. This would tend to produce a cut that is smoother than the conventional

Smart-Cut®. In fact, this is exactly what is found experimentally and is reported in this work.

In order to obtain a smooth surface, a post splitting CMP step is always necessary in the conventional smart-cut® process, this may remove up to a few hundred angstroms of the transferred film. Therefore, the combination of low temperature plasma activated direct bonding and ion cut induced layer splitting is significant because it allows:

- 1) Ultra thin (<500 angstroms) SOI needed for a fully depleted technology
- 2) It is smooth enough to be directly used without Chemical-Mechanical Polishing (CMP) for integration of three-dimensional nanostructures, and is essential to incorporation in the development ion cut to form thin films of preprocessed microelectronic and MEMS structures.

Therefore, the low temperature layer splitting and film transference includes (Fig. 4.9):

- 1) Hydrogen implantation into wafer A at a controlled energy, where wafer A can be either hydrophilic or hydrophobic;
- 2) Plasma activates wafer A and target substrate (motherboard) and low temperature bonding to produce a permanent structure of the two. The temperature is restricted under 200 °C for this step;
- 3) Phase-two heat treatment the bonded structure at 420 °C, hydrogen out-diffusion into the already existed microcavities and cause these bubbles to grow laterally, eventually cause the layer to split;

- 4) A fine polishing step may apply to the transferred film, or, since the surface of the transferred film is smooth enough, this step may be removed then the layer splitting and film transference can be collapsed into three steps.

#### 4.4. Lower Hydrogen Dose and Lower Temperature Layer Splitting

It is clear that within a certain dose range, hydrogen implanted into silicon can precipitate in platelets basically on two sets of planes, namely {001} and {111} [13]. At higher doses bubbles generally form instead of platelets. The lack of strain field around these platelets suggests that they may arise from the passivation of broken Si-Si bonds and essentially contain little or no gas pressure component, in contrast to other cases of platelets in materials. A comparison of the calculated hydrogen content within typical platelets indicates that only a relatively small amount of the implanted hydrogen remains trapped within them. This implies by introducing other species into silicon, which can trap more hydrogen atoms during the implantation, but in a lower energy bond, then it is possible that it releases the hydrogen to cause the bubbles growth and layer splitting at a lower temperature.

A. D. Marwick et al pointed out in their early publication, that Ga in silicon is found to attract hydrogen implanted into silicon [33-35]. The Marwick paper suggests that ionized  $Ga^-$  in silicon attracts  $H^+$  ions and at temperatures of  $\sim 200^\circ C$  may attract quantities of H much in excess of the density of Ga. The process can be summarized by the following overall equation:



where  $nH_{imm}^0$  represents an immobile neutral cluster of  $n$  hydrogen atoms. The equation represents a process in which the H-Ga pair dissociated, and then the hydrogen diffuses to a cluster.

However, Ga is not appropriate in the layer splitting and film transference because it is too heavy and may cause too much damage to the surface layer. Boron, on the other hand, as another group III element but much lower atomic mass, is investigated in this work, as the catalyst material in lower both the hydrogen implantation dose and the layer splitting temperature.

A boron implantation, rapid thermal annealed (RTA) and followed by hydrogen implantation, significantly decreased the surface blistering temperature (or the layer splitting temperature). Monte Carlo simulation indicates that each boron atom generates  $\sim 400$  displacement defects and may trap a cluster up to 12 hydrogen atoms. Moreover, the Si-H bond appears to be weakened by the presence of boron next to it. Therefore the boron pre-implantation can enhance platelet creation after the subsequent hydrogen implantation, and the microcavities can grow at a lower temperature due to the diffusion of released hydrogen atoms which may form  $H_2$  molecules in the microcavities which eventually lead to the layer splitting. Boron RTA is critical in this B-H co-implantation induced layer splitting, because otherwise the boron may not incorporated into the crystal lattice points and electrically active. Experimental results show that with RTA, B-H co-implantation may produce surface blistering as low as 200 °C, while an anneal has to be performed at a temperature of 420 °C for the B-H co-implanted samples without boron RTA.

To reduce the hydrogen implantation dose not only critical for reducing the fabrication cost but also can reduce the implantation damage. With the help of boron pre-implantation ( $1 \times 10^{15}/\text{cm}^2$ ), it is observed that the hydrogen implantation dose can be reduced to as low as  $2 \times 10^{16}/\text{cm}^2$ , less than one half of the dose used in the smart-cut® process ( $5 \times 10^{16}/\text{cm}^2$  to  $1 \times 10^{17}/\text{cm}^2$ , see Table 4.2).

Other methods were also introduced in reducing the splitting temperature, both thermally and mechanically. Among them, using liquid nitrogen to give the annealed sample a "cooling" shock seemed a very promising way. We have reduced the splitting temperature for hydrogen implanted only bonding sample down to 390 °C, which is 30 °C lower than the "normal" cutting temperature.

#### References

- 21) Michel Bruel, "Application of hydrogen ion beams to Silicon On Insulator material technology", Nuclear instruments and Methods in Physics Research B 108 (1996) 313-319.
- 22) M. Bruel, "Silicon on insulator material technology", Electronics Letters, 6th July 1995, Vol. 31, No. 14, 1201-1202.
- 23) M. BRUEL, B. ASPAR, B. CHARLET, C. MALEVILLE, T. POUMEYROL, A. SOUBIE, A. J. AUBERTON-HERVE, J.M. LAMURE, T. BARGE, F. METRAL, S. TRUCCHI, "SMART CUT": A PROMISING NEW MATERIAL TECHNOLOGY", Proceedings 1995 IEEE International SOI Conference, Oct. 1995, 178-179.
- 24) L. Di Cioccio, Y. Le Tiec, F. Letertre, C. Jaussaud and M. Bruel, "Silicon carbide on insulator formation using the Smart Cut process", Electronics Letters, 6th July 1996, Vol. 32, No. 12, 1144-1145.

- 25) A.J. AUBERTON-HERVE, Michel BRUEL, Bernard ASPAR, Christophe MALEVILLE, and Hubert MORICEAU, "SMART-CUT<sup>®</sup>: The Basic Fabrication Process for UNIBOND<sup>®</sup> SOI Wafers", IEICE TRANS. ELECTRON. VOL. E80-C, NO.3 MARCH 1997. 358-363.
- 26) B. Aspar, M. Bruel, H. Moriceau, T. Poumeyrol, A.M. Papon, "Basic mechanisms involved in the Smart-Cut<sup>®</sup> process", Microelectronic Engineering 36 (1997) 233-240.
- 27) Christophe Maleville, B. Aspar, T. Poumeyrol, H. Moriceau, M. Bruel, A.J. Auberton-Herve, T. Barge, "Wafer bonding and H-implantation mechanisms involved in the Smart-cut<sup>®</sup> technology", Materials Science and Engineering B46 (1997), 14-19.
- 28) Michel BRUEL, Bernard ASPAR and Andre-Jacques AUBERTON-HERVE, "Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding", Jpn. J. Appl. Phys. Vol. 36 (1997) pp. 1636-1641, Part 1, No. 3B, March 1997.
- 29) G.F. Cerofolini, L. Meda, R. Balboni, F. Corni, S. Frabboni, G. Ottaviani, R. Tonini, M. Anderle and R. Canteri, "Hydrogen-related complexes as the stressing species in high-fluence, hydrogen-implanted, single-crystal silicon", PHYSICS REVIEW B, VOLUME 46, NUMBER 4, 15 JULY 1992-II, 2061-2070.
- 30) G.F. Cerofolini, R. Balboni, D. Bisero, F. Corni, S. Frabboni, G. Ottaviani, R. Tonini, R.S. Brusa, A. Zecca, M. Ceschini, G. Giebel, and L. Pavesi, "Hydrogen Precipitation in Highly Oversaturated Single-Crystalline Silicon", phys. Stat. Sol. (a) 150, 539-585 (1995).



- 31) M.K. Weldon, V.E. Marsico, Y.J. Chabal, M. Collot, Y. Caudano, S.B. Christman, E.E. Chaban, D.C. Jacobson, W.L. Brown, J. Sapjeta, C.-M. Hsieh, C.A. Goodwin, A. Agarwal, V.C. Venezia, T.E. Haynes, and W.B. Jackson, "Mechanism of Silicon Exfoliation by Hydrogen Implantation and He, Li and Si Co-implantation", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, 124-125.
- 32) S. J. Jeng, G. S. Oehrlich, and G. J. Scilla, "Hydrogen plasma induced defects in silicon", Appl. Phys. Lett. **53** (18), 31 October 1988, 1735-37.
- 33) S. Romani, and J. H. Evans, "Platelet defects in hydrogen implanted silicon", Nuclear Instruments and Methods in Physics Research B44 (1990) 313-317.
- 34) Tohru Hara, Takayuki Onda, Yasuo Kakizaki, Sotaro Oshima and Ira Kltamura, "Delamination of Thin layers by High Dose Hydrogen Ion Implantation in Silicon", J. Electrochem. Soc., Vol. 143, No. 8, August 1996, L166-L168.
- 35) X. Lu, S. S. K. Iyer, J. Min, Z. Fan, P. K. Chu, C. Hu and N. W. Cheung, "PLASMA IMMERSION ION IMPLANTATION FOR SOI SYNTHESIS: SIMOX AND SMART-CUTTM", Proc. SOI conference, 1996.
- 36) Xiang Lu, S. Sundar Kumar Iyer, Chenming Hu, and Nathan W. Cheung, Jing Min, Zhineng Fan, and Paul K. Chu, "Ion-cut silicon-on-insulator fabrication with plasma immersion ion implantation", Appl. Phys. Lett. **71** (19), 10 November 1997, 2767-2769.
- 37) Xiang Lu and Nathan W. Cheung, Michael D. Strthman, Pail K. Chu, Brian Doyle, Appl. Phys. Lett. **71** (13), 29 September 1997, 1804-1806.
- 38) Paul K. Chu, "SYNTHESYS OF SOI MATERIALS USING PLASMA IMMERSION ION IMPLANTATION", MRS, Fall, 1996.

- 39) L.B. Freund, "A lower bound on implant density to induce wafer splitting compliant substrate structure", Appl. Phys. Lett. 70 (26). 30 June 1997.
- 40) Q.-Y. Tong, K. Gutjahr, S. Hopfe, and U. Gosele, T.-H. Lee, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates", Appl. Phys. Lett. 70 (11), 17 March 1997, 1390-1392.
- 41) T.-H. Lee, Q.-Y. Tong, Y.-L. Chao, L.-J. Huang and U. Gosele, "Semiconductor Layer Transfer By Anodic Wafer Bonding", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, 40-41.
- 42) Q.-Y. Tong, T.-H. Lee, L.-J. Huang, Y.-L. Chao and U. Gosele, "Low Temperature Si Layer Splitting", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, 126-127.
- 43) R. W. Bower, M. S. Ismail and B. E. Roberds, "Low Temperature  $\text{Si}_3\text{N}_4$  Direct Bonding", Appl. Phys. Lett., 28 June 1993 pp. 3485-3487.
- 44) Victor H. C. Watt and Robert Bower, "Low Temperature direct bonding of non-hydrophilic surfaces", Electronic Letts., April 1994, Vol. 30, No. 9, 693-695.
- 45) R.W. Bower, W.Chan, L.Hong, L. LeBoeuf, Y.A. Li, and J. Lee, "Optimization Of Low Temperature  $\text{NH}_3$  Plasma Activated Direct Bonding", Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head, SC, June 1996.
- 46) R. W. Bower & F. Y. -J. Chin, "low Temperature Direct Silicon Wafer Bonding Using Ar Activation", Japanese Journal of Applied Physics, vol.36, No.5A, pp.L527-L528.
- 47) Y. Albert Li and Robert W. Bower, "Low temperature direct bonding using pressure and temperature", Proceedings of SPIE, Vol. 3184, 124-128, June 1997.

- 48) Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March), 1998.
- 49) Robert W. Bower, Y. Albert Li, Wade Xiong, Jimmy Kieue, Bryon Washoe, "Low Temperature Plasma Activated Water Bonded Wafers", To be published 1998.
- 50) Bryon Washoe and Robert W. Bower, "Voidless Plasma Activated Low Temperature Bonding of Wafers", To be published 1998.
- 51) Robert W. Bower, Y. Albert Li and Frank Y-J Chin, "The hydrogen ion cut technology combined with low temperature direct bonding", Proceedings of SPIE, Vol. 3184, June 1997, 2-4.
- 52) Y. Albert Li and Robert W. Bower, "Surface Conditions and Morphology of Hydrogen Ion Cut Low Temperature Bonded Thin Film Layers", to be published, 1998.
- 53) D. Marwick, G. S. Oehrlein, and M. Wittmer, "High hydrogen concentrations produced by segregation into  $p^+$  layers in silicon", Appl. Phys. Lett. 59 (2), 8 July 1991, 198-200.
- 54) Robert W. Bower, Louis LeBoeuf, and Y. Albert Li, "Transposed Splitting of Silicon implanted with Spatially Offset Distributions of Hydrogen and Boron", IL NUOVO CIMENTO, Vol. 19, D, N. 12, 1871-1873, December 1997.
- 55) Adiya Agarwal, T. E. Haynes, and V. C. Venezia, D. J. Eaglesham, M. K. Weldon, Y. J. Chabal, "Efficient production of Silicon-on-Insulator Films by Co-implantation of  $He^+$  with  $H^+$ ", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, 44-45.

Ion Energy	dE/dx Elec.	dE/dx Nuclear	Projected Range	Longitudinal Straggling	Lateral Straggling
10.00 keV	2.196E-01	4.222E-03	1689 A	740 A	682 A
11.00 keV	2.333E-01	3.994E-03	1835 A	770 A	718 A
12.00 keV	2.469E-01	3.793E-03	1975 A	797 A	751 A
13.00 keV	2.601E-01	3.615E-03	2110 A	821 A	781 A
14.00 keV	2.729E-01	3.455E-03	2240 A	843 A	810 A
15.00 keV	2.854E-01	3.310E-03	2367 A	863 A	836 A
16.00 keV	2.975E-01	3.179E-03	2489 A	882 A	861 A
17.00 keV	3.092E-01	3.059E-03	2608 A	899 A	884 A
18.00 keV	3.207E-01	2.949E-03	2723 A	915 A	906 A
20.00 keV	3.426E-01	2.754E-03	2946 A	943 A	946 A
22.00 keV	3.632E-01	2.587E-03	3158 A	968 A	982 A
24.00 keV	3.827E-01	2.441E-03	3361 A	989 A	1014 A
26.00 keV	4.010E-01	2.312E-03	3556 A	1009 A	1044 A
28.00 keV	4.182E-01	2.199E-03	3745 A	1026 A	1071 A
30.00 keV	4.343E-01	2.097E-03	3927 A	1042 A	1096 A
33.00 keV	4.565E-01	1.962E-03	4192 A	1063 A	1130 A
36.00 keV	4.764E-01	1.846E-03	4446 A	1082 A	1162 A
40.00 keV	4.996E-01	1.713E-03	4774 A	1104 A	1200 A
45.00 keV	5.236E-01	1.574E-03	5167 A	1128 A	1242 A
50.00 keV	5.424E-01	1.459E-03	5548 A	1150 A	1280 A
55.00 keV	5.568E-01	1.360E-03	5919 A	1169 A	1315 A
60.00 keV	5.672E-01	1.276E-03	6285 A	1186 A	1347 A
65.00 keV	5.741E-01	1.202E-03	6646 A	1201 A	1378 A
70.00 keV	5.782E-01	1.137E-03	7004 A	1216 A	1407 A
80.00 keV	5.793E-01	1.028E-03	7722 A	1245 A	1461 A
90.00 keV	5.738E-01	9.401E-04	8445 A	1272 A	1512 A
100.00 keV	5.640E-01	8.672E-04	9181 A	1297 A	1562 A
110.00 keV	5.517E-01	8.056E-04	9934 A	1322 A	1610 A
120.00 keV	5.380E-01	7.530E-04	1.07 um	1346 A	1658 A
130.00 keV	5.238E-01	7.074E-04	1.15 um	1370 A	1706 A
140.00 keV	5.097E-01	6.675E-04	1.23 um	1393 A	1754 A
150.00 keV	4.958E-01	6.322E-04	1.32 um	1417 A	1803 A
160.00 keV	4.825E-01	6.007E-04	1.40 um	1441 A	1852 A
170.00 keV	4.697E-01	5.725E-04	1.49 um	1466 A	1902 A
180.00 keV	4.576E-01	5.471E-04	1.58 um	1491 A	1953 A
200.00 keV	4.354E-01	5.029E-04	1.77 um	1553 A	2058 A
220.00 keV	4.156E-01	4.659E-04	1.97 um	1617 A	2167 A
240.00 keV	3.979E-01	4.343E-04	2.18 um	1684 A	2280 A

**Table 4.1. Monte Carlo simulation results for hydrogen implants into silicon by SRIM**

	Without Boron co-implantation	With Boron co-implantation ( $1 \times 10^{15} \text{ cm}^{-2}$ )	
		No RTA	RTA
Hydrogen Dose	$5 \times 10^{16}$ to $1 \times 10^{17} \text{ cm}^{-2}$	$5 \times 10^{16}$ to $1 \times 10^{17} \text{ cm}^{-2}$	$2 \times 10^{16} \text{ cm}^{-2}$
Splitting Temperature	420 °C	420 °C	200 °C

Table 4.2 Implant boron as the catalyst material may greatly reduce both the hydrogen implantation dose and the splitting temperature.

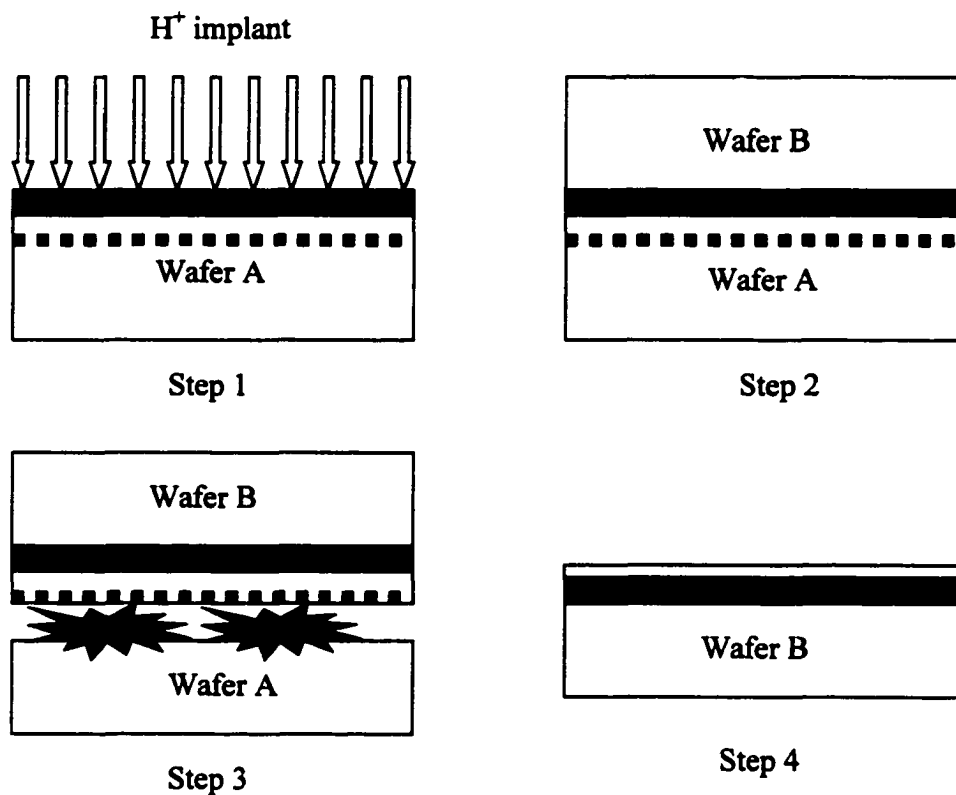


Fig. 4.1. Smart-cut<sup>®</sup> technology to produce silicon-on-insulator material. Including 1) hydrogen implantation to oxide capped silicon (wafer A); 2) hydrophilic bond wafer A to a stiffener wafer (wafer B); 3) two-phase thermal anneal, 400 - 600 °C for wafer A to delaminate and >1000 °C for enhance the wafer bond strength; 4) polish the surface from ~100 angstroms as-splitting RMS roughness to ~ 5 angstroms to complete the SOI structure

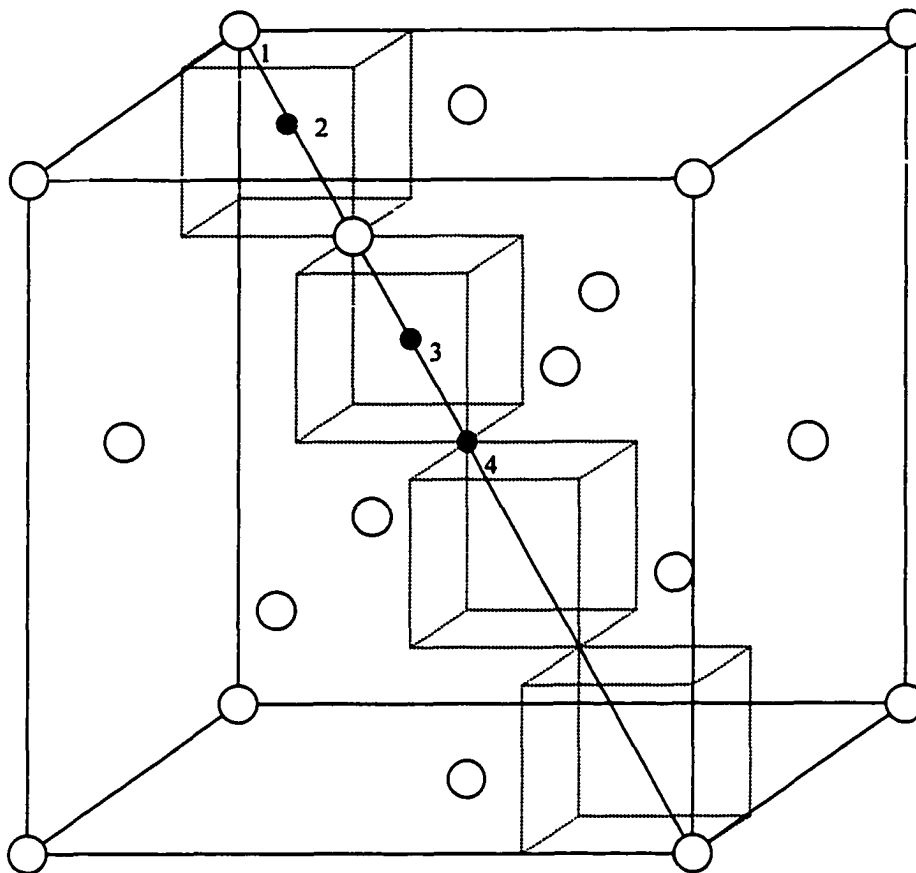


Fig 4.2 (a) The conventional unit cell in the silicon lattice in 3-dimension. Different impurity sites are indicated that 1. Substitutional, 2. Bond center (BC), 3. Antibonding (AB) and 4. Tetrahedral (T)

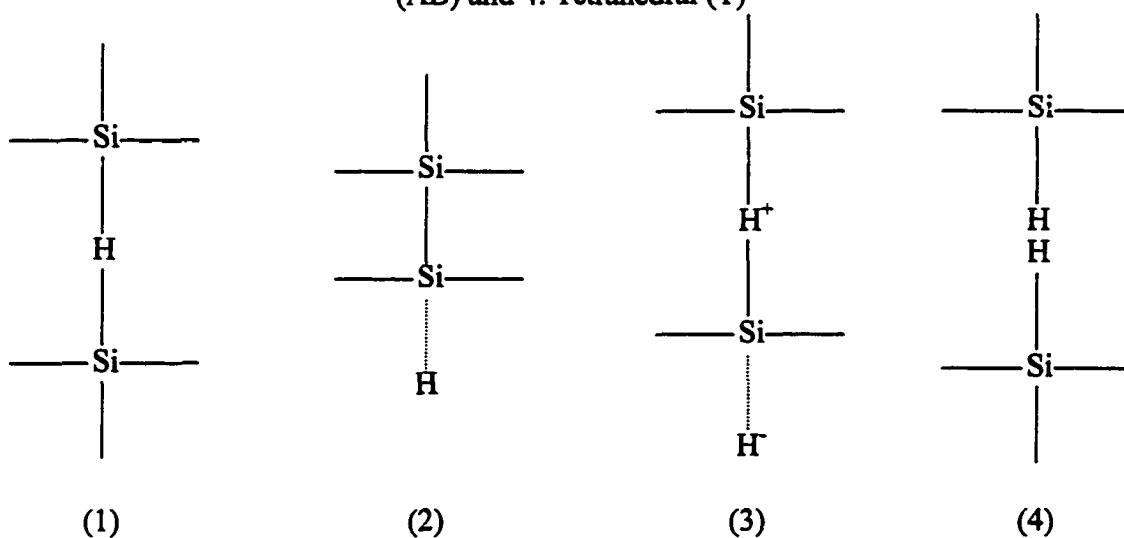
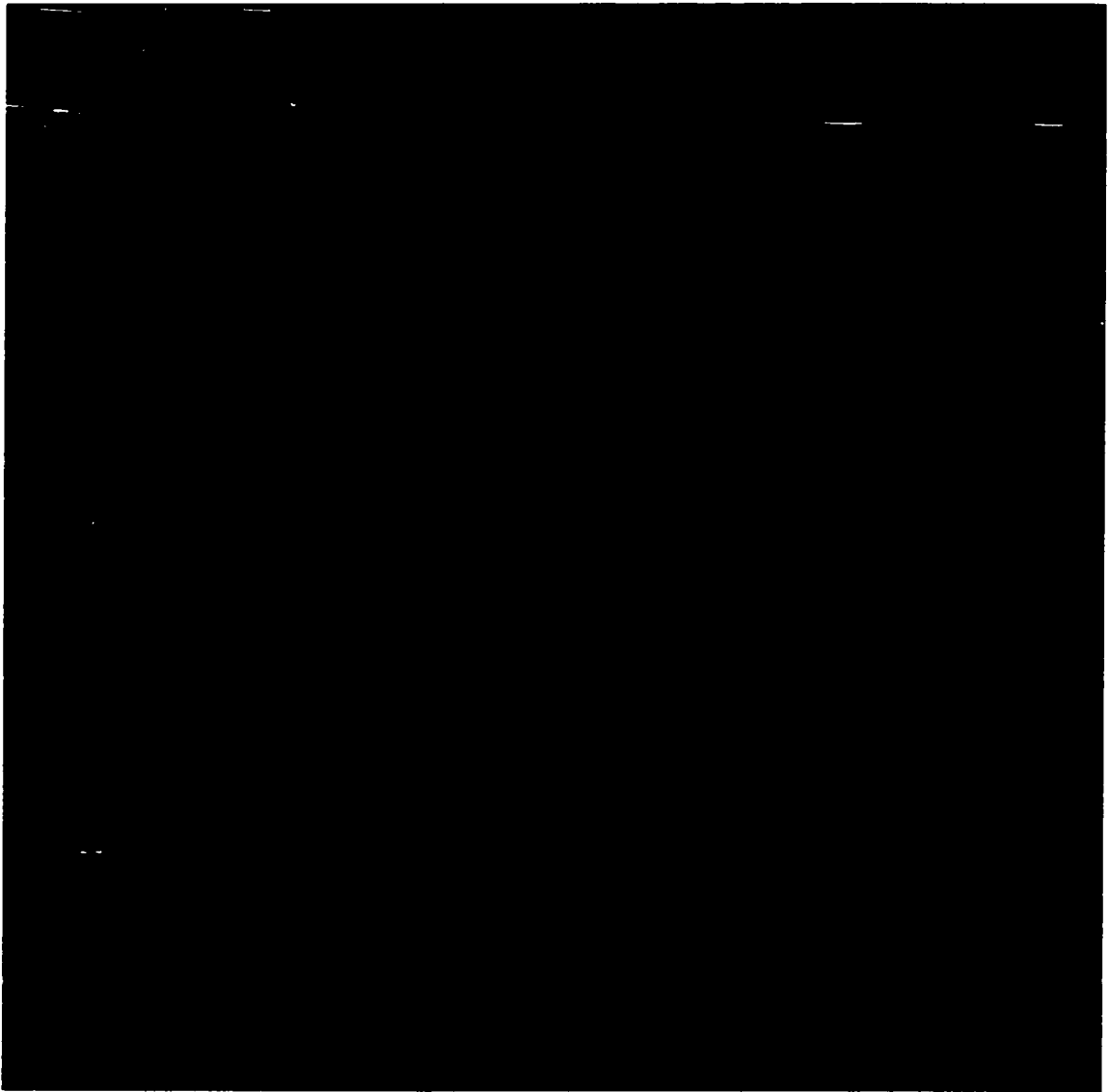
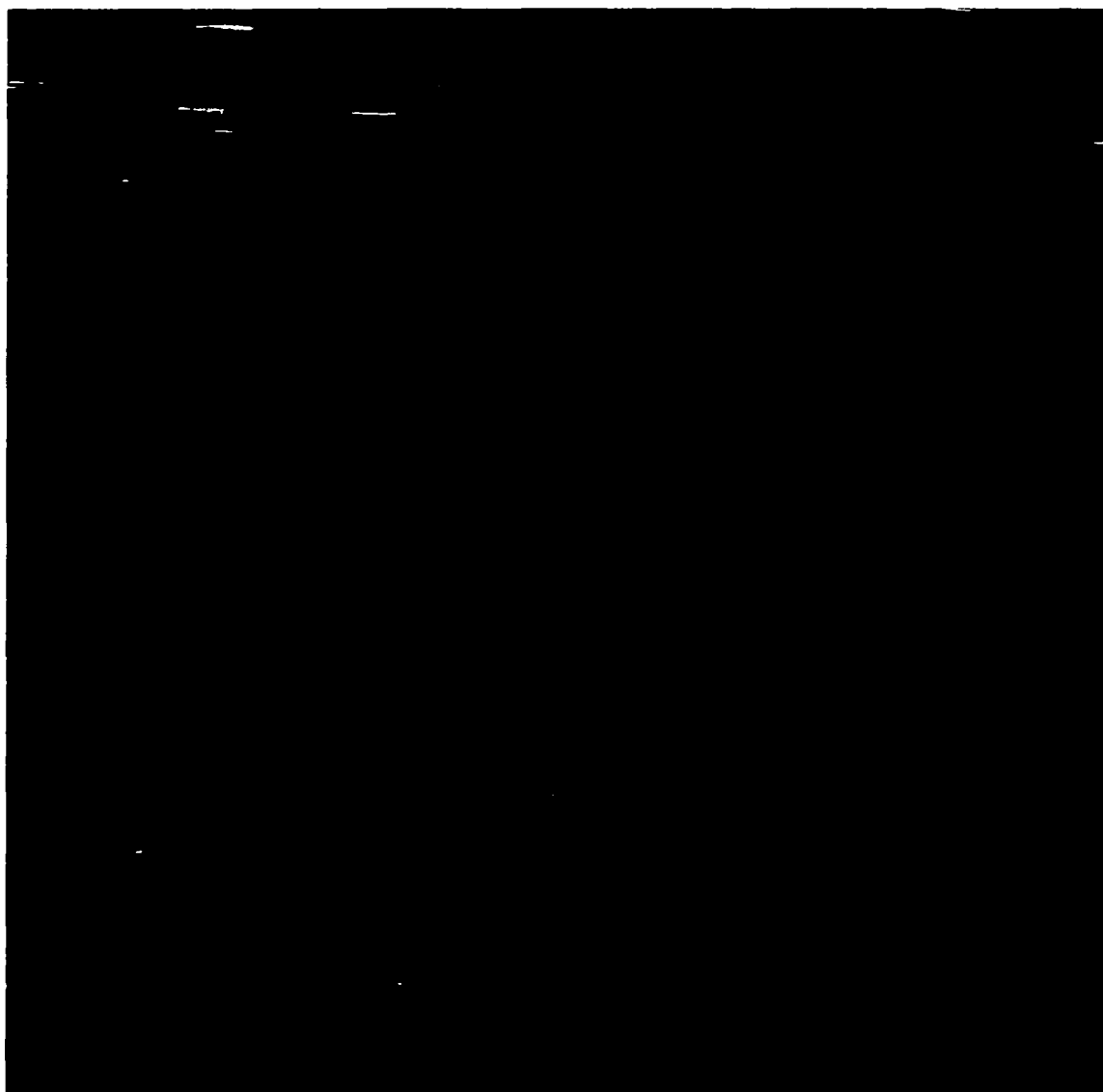


Fig. 4.2 (b). Four possible hydrogen configurations in silicon (1) bond – centered (BC); (2) antibonding (AB); (3)  $H_2$ ; (4) silanic

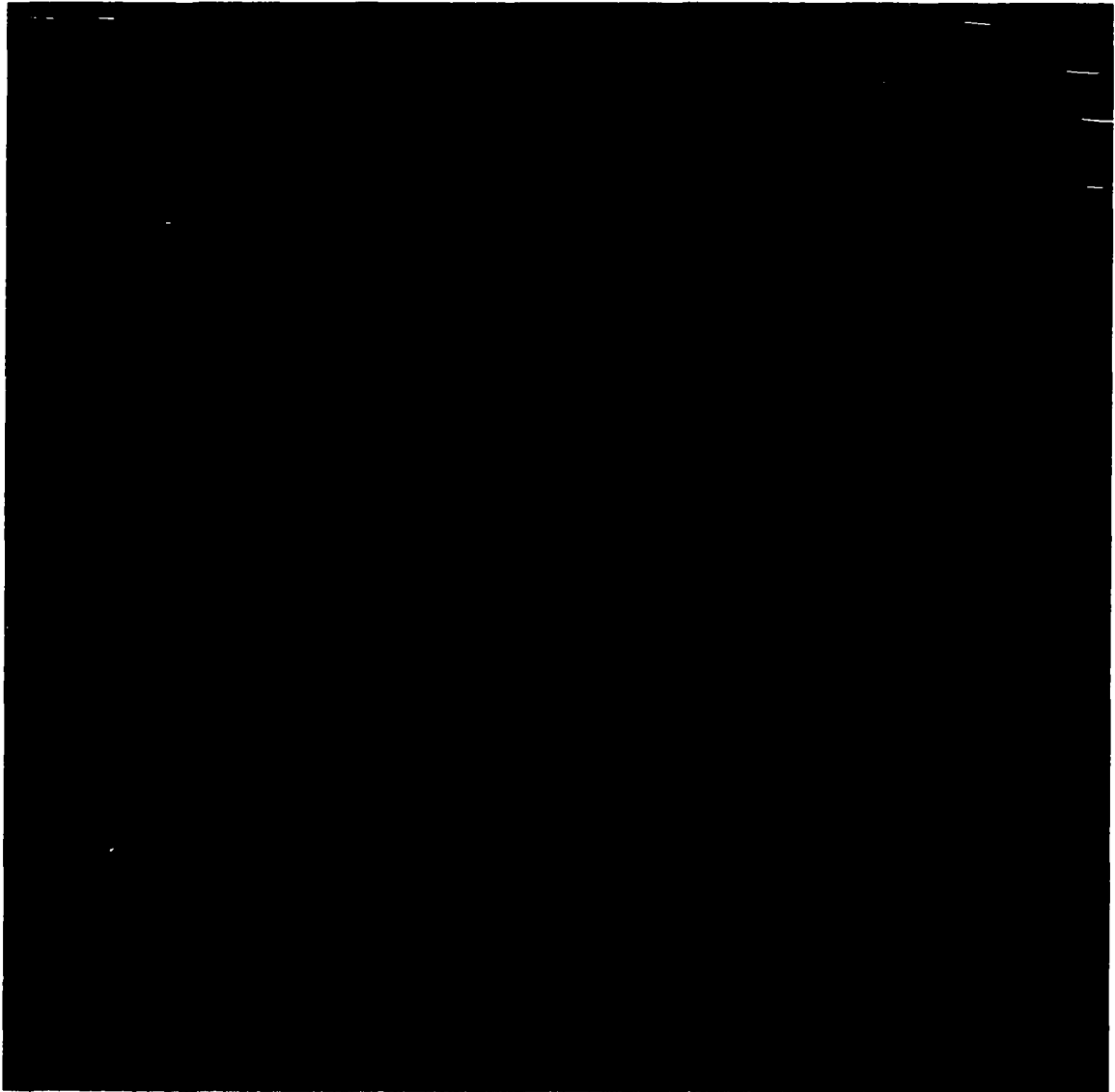


**Fig 4.3. Blisters at the silicon surfaces after hydrogen ion implantation.**  
**(a)  $4.5 \times 10^{16} \text{ H}^+$  into (100) Si, 40 KeV, 425 °C, 6 hours**





**Fig. 4.3. Blisters at the silicon surfaces after hydrogen ion implantation  
(b)  $4.9 \times 10^{16} \text{ H}^+$  into (100) Si, 40 KeV, 425 °C, 2 hours**



**Fig. 4.3. Blisters at the silicon surfaces after hydrogen ion implantation.  
(c)  $5.3 \times 10^{16}$  H<sup>+</sup> into (100) Si, 40 KeV, 425 °C, 25 minutes**



**Fig. 4.3. Blisters at the silicon surfaces after hydrogen ion implantation.  
(d)  $5.7 \times 10^{16} \text{ H}^+$  into (100) Si, 40 KeV, 425 °C, 20 minutes**

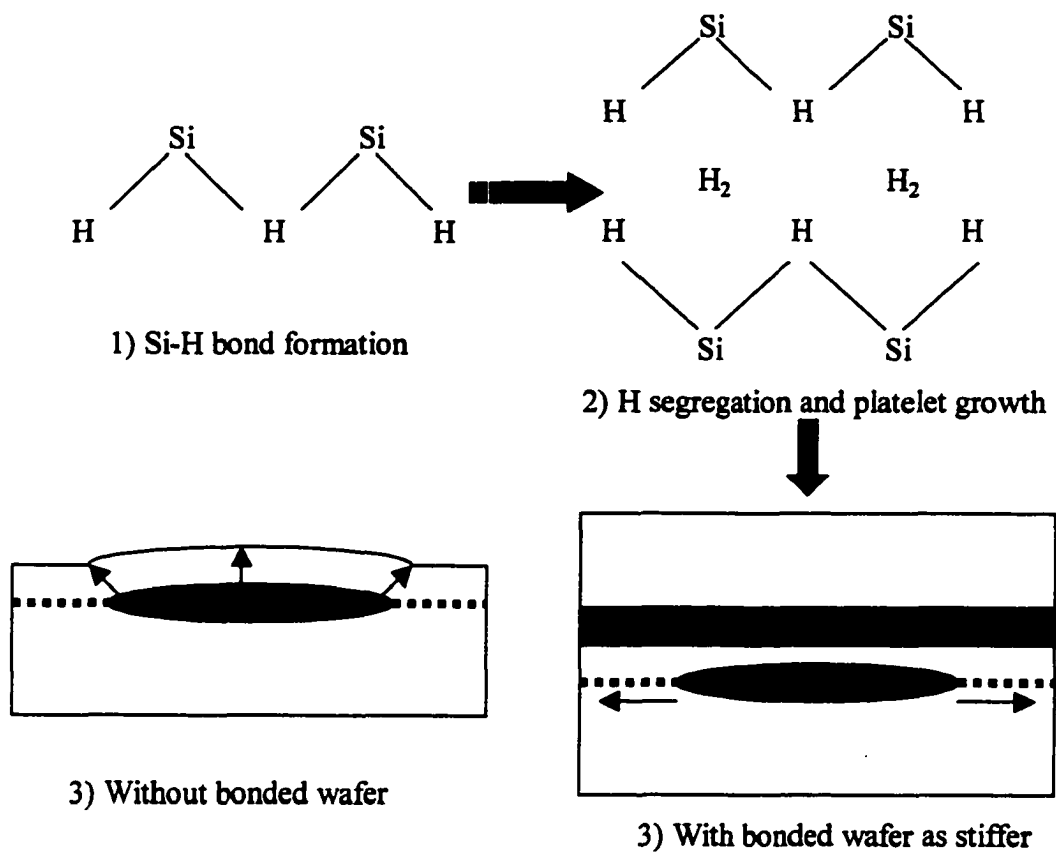


Fig. 4.4. Proposed basic mechanism of Smart Cut<sup>®</sup> process

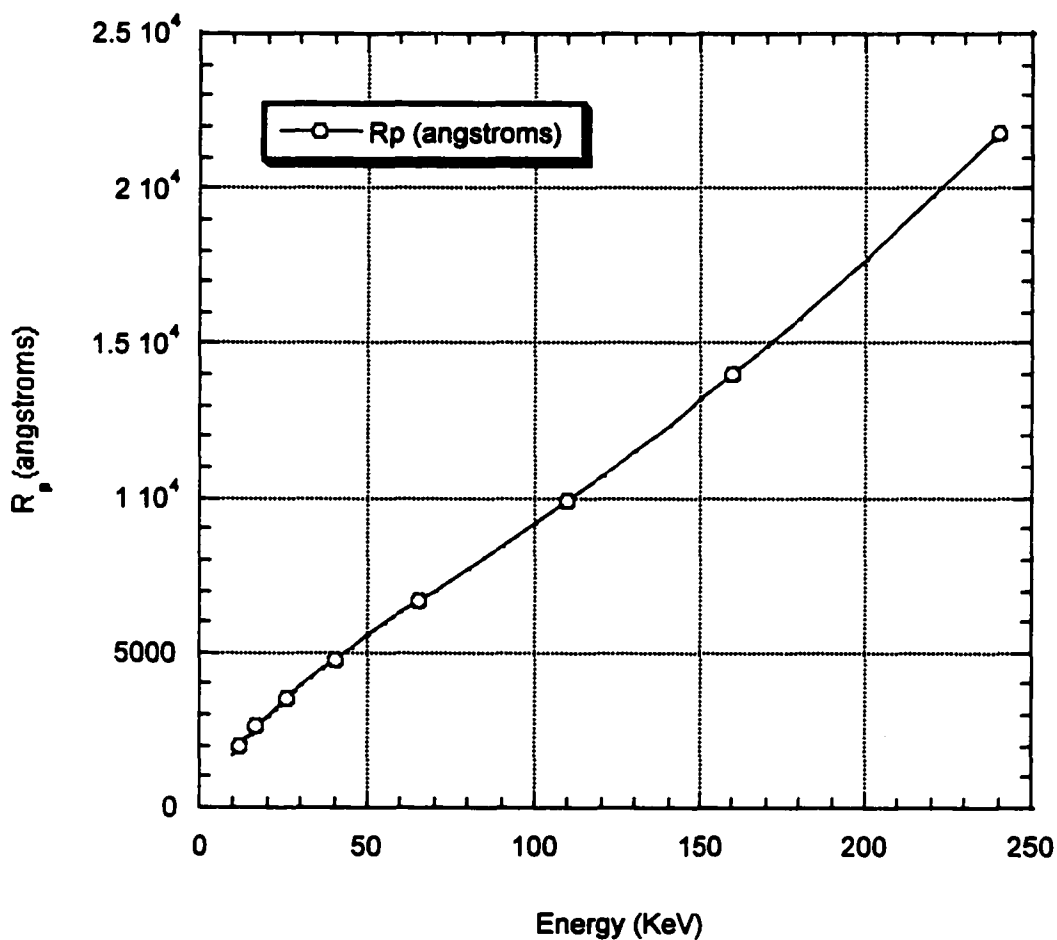


Fig. 4.5. Monte Carlo simulation shows the hydrogen projected range implanting into silicon can be predicted by adjusting the implantation energy.



**Fig. 4.6. A 10cm diameter SOI wafer produced with a hydrogen ion cut at 420 °C after low temperature wet SRD direct bonding.**

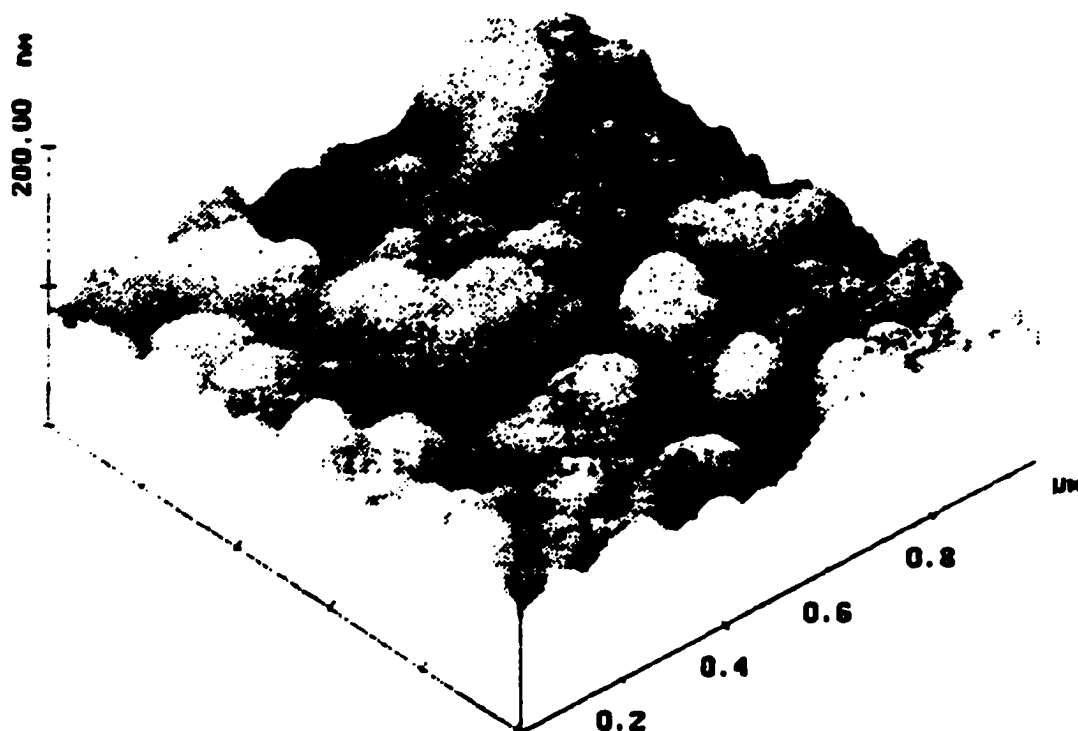
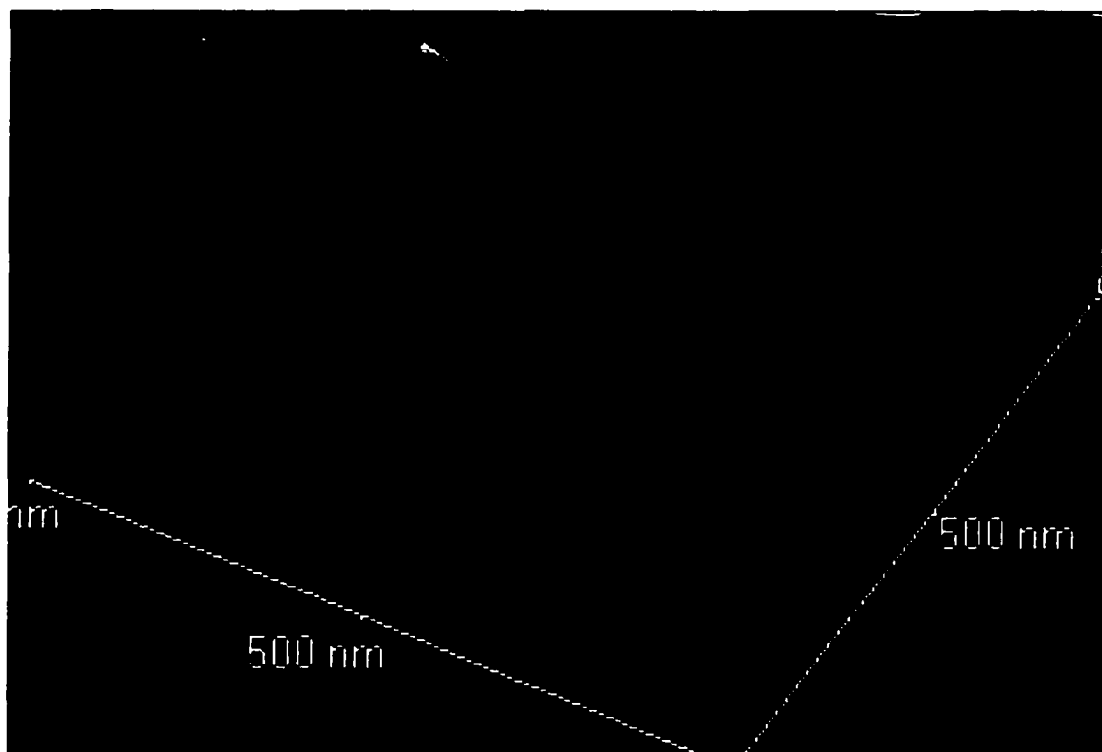


Fig. 4.7 The surface roughness of smart-cut<sup>®</sup> layers created with a normal direct bond after an Atomic Force Microscopic (AFM) picture published in a recent article (after M. Bruel et al)



**Fig. 4.8 AFM of the surface roughness low temperature bonded hydrogen cut wafer  
(vertical scale is 0 - 12.49 nm)**



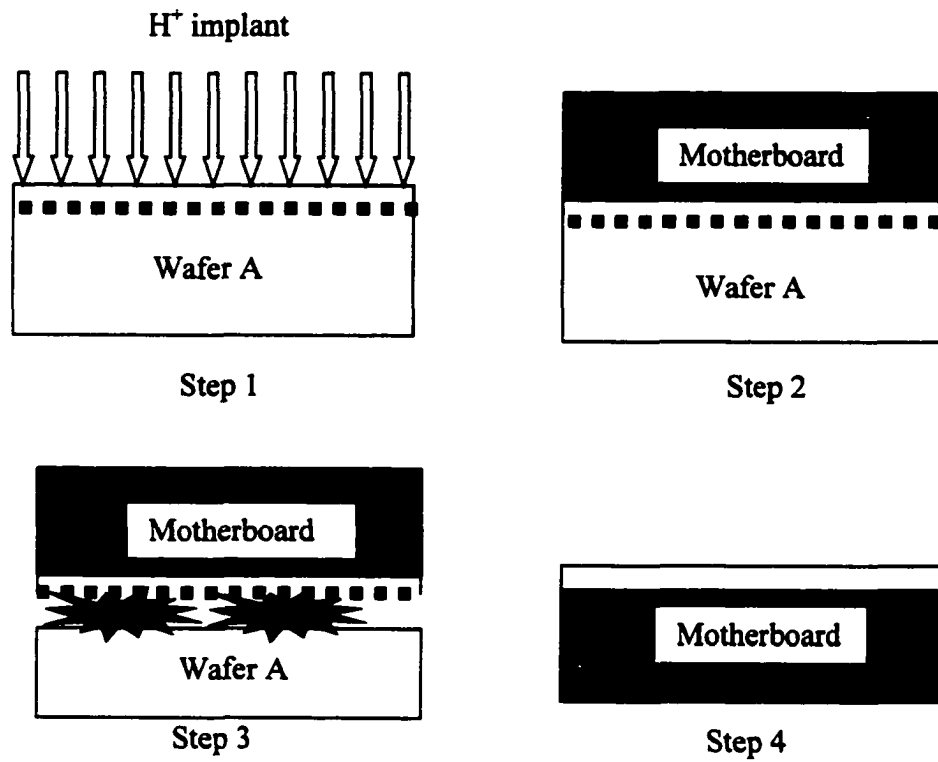


Fig. 4.9 Process of layer splitting and thin film transference

## **CHAPTER 5**

# **Low Temperature Copper to Copper Direct Bonding**

### **5.1 Comparison of Possible Interconnect Metal**

Interconnect technology is currently an area of considerable interest in integrated circuits. The basic material technologies as well as the structure and number of layers of interconnect are subjects of concern. The work described in this chapter addresses both of these issues. Low temperature direct bonding of copper to copper provides a metal superior to aluminum in many ways and provides a novel new method of forming multi-layer interconnect structures of this material.

Aluminum and its alloys are found to be inadequate for ultra-large-scale integrated circuits (ULSI) and giga-scale integrated circuits (GSI). Two main problems cause aluminum to be inadequate. The relatively high resistivity of aluminum, causes an unacceptable high value of RC delay, especially in microprocessors and application-specific integrated circuits (ASIC) [1, 2]. And secondly, Electromigration of aluminum power devices is a major problem where the current density is often greater than  $10^5$  amp/cm<sup>2</sup> [3].

The use of copper interconnects, on the other hand, is receiving increasing attention for future generations of ICs, with advantages of low line resistance, low interconnect delay, high electromigration resistance and, possibly, overall back-end

simplicity. In addition, copper can be more readily deposited by chemical vapor deposition (CVD) techniques, thereby offering the possibility of a high performance interconnection technology with complete filling of high aspect-ratio vias and trenches. Finally, copper is also superior to aluminum because of its high thermal conductivity. Some physical parameters for possible interconnect metals are listed in Tables 5.1 [1, 2].

Therefore, Cu to Cu low temperature direct bonding technology becomes critical in some of the ULSI applications, not only due to its mechanical properties (e.g., high thermal conductivity for heat dissipation), but also due to the possibility of vertical integration of the multilayer microelectronics structures for the next generation of faster ULSI and GSI devices.

## **5.2 Low Temperature Copper to Copper Direct Bonding**

Direct bonding of semiconductors and insulators now have a considerable history where covalent bonds of these materials can be produced at temperatures ranging from  $\sim 100$  °C to over 1000 °C [4]. Direct low temperature bonding of metals has not been previously described [5]. The metal to metal bond is much simpler than the covalent bond established in the earlier work and only intimate contact and reduction of intermediate layers of oxide appear necessary to create a low temperature bond.

In this chapter, a simple, low temperature direct Cu bonding technique is presented, which produces a strong bond with a uniform pressure at a temperature of only 100 °C for a period of 3 hours [6].

In this work, 6-inch commercial n type (100) silicon substrates with very low resistivity ( $\rho \sim 1\text{-}3\text{ m}\Omega\text{-cm}$ ) were used. The wafers were dipped in high concentration HF (100:1) first. Then the materials were placed in a sputter chamber, where an in situ Ar

ion etch was applied at 300 °C to remove the top few hundred angstroms of substrate. Finally, a 500 nm copper film was sputtered onto the surface at a temperature of 350 °C.

Surface roughness is always an important concern in direct wafer bonding [7]. In Fig. 5.1, for a Cu sample without any chemical mechanical planarization (CMP), the area  $R_a$  and root-mean-square (RMS) roughness were measured by AFM, and found to be 0.9927 nm and 1.2911 nm respectively. Therefore, the roughness of this deposited Cu is only slightly greater than required (1 nm) for direct silicon wafer bonding. However, since Cu surface is much softer than that of silicon, it is no surprising that a Cu-Cu bond was found to be more tolerant of roughness than that found for silicon.

The Cu samples were cut into 2 cm × 2 cm square pieces. After the initial contact, a pressure was applied uniformly throughout the whole surface ranging from 0 to  $10^7$  N/m<sup>2</sup>. Then the samples were moved into an oven with temperature ranging between 70 to 200 °C. The oven was first pumped to a high vacuum then back-filled with nitrogen gas to about 0.3 atm. It was found that both temperature and pressure are required for a successful bond. Threshold pressures of  $10^7$  N/m<sup>2</sup> and 100 °C for a minimum of 3 hours were measured in this work to produce a successful bond.

### 5.3 Bond Strength Test

A straight pull test was performed to measure the bonding strength. The bonded sample was glued to a fixed smooth platform. A well-calibrated spring scale was glued to the other side of the bonded sample. It was found that > 35.6 N is required to separate the bonded sample. It was observed that for a Cu sample sputtered directly on top of silicon substrate without any adhesion promotion layer, the bonded sample always separated at the Cu-Si interface, rather than at Cu-Cu bonding interface. This indicates

(a) the Cu-Cu bonding strength is actually greater than the measured value; and (b) that an adhesion promoter (e.g., Ti, TiN, Ta, TaN, etc.) is required even for depositing Cu directly onto bare silicon surfaces. The specific contact resistance ( $\rho_c$ ) was also measured. The value of contact resistance is currently under investigation, the initial results suggest that the electrical conduction will be acceptable for IC applications.

#### 5.4. Specific Contact Resistance ( $\rho_c$ ) Measurement

Specific contact resistance is a very important parameter for Cu-Cu direct bonding, which is a theoretical quantity referring to the metal-metal interface only. The  $\rho_c$  measurement setup is shown in Fig. 5.2a, the silicon substrate is highly doped and the resistivity is very low (n type,  $\sim 1\text{-}3\text{ m}\Omega\text{-cm}$ ). The substrate is then HF dipped and a thin layer of 500-nm Cu film is sputtered. After bonding, a HF clean on the backsides of the sample is performed to prevent any native oxide. A current at different fixed values is forced through the bonded sample from the backsides of the silicon substrate (contacts 1 and 2), the voltage drop is measured across the Cu-Cu contact (contacts 3 and 4). Then the specific contact resistance can be calculated as  $\rho_c = A V_{34}/I_{12}$ , where  $A$  is the contact area.

This experiment setup is similar to the well-known vertical Kelvin test structure [8]. Fig. 5.2 shows both the Cu-Cu contact resistance measurement setup (Fig 5.2a) and vertical Kelvin test structure (Fig. 5.2b). There are two major reasons that cause the apparent contact resistance larger than the actual value. In Fig. 5.2a, comparing with Fig. 5.2b, there is no isolation PN junction to confine the current flow  $I$ , therefore, the actual current is flowing across the whole contact area, which is considerably large (in the order of  $\text{mm}^2$ ). Furthermore, although there is very little lateral voltage drop along the

interface during the voltage measurement because essentially no current is drawn, the lateral effect also plays a role in this structure. This comes about not because of the current flows laterally to reach a collecting contact but because of current spreading. The current does not flow strictly vertically. It has a lateral spreading component, which makes the voltage at the sensing contacts (contacts 3 and 4) not exactly equal to the voltage under the contact metal. The additional spreading causes the measured contact resistance to be higher than the true contact resistance.

Fig. 5.3 shows linear current-voltage characteristics. The calculation of specific contact resistance also shows that the Cu-Cu bonded sample can supply the necessary device current, and the voltage drop across the contact is small enough comparing to the voltage drop of the active device regions.

It is demonstrated that with the help of pressure and temperature treatment, low temperature direct bonding technology can be extended to metal surface, especially for copper. This metal is currently thought to be the next key interconnect metal in ULSI and GSI. Low temperature direct bonding Cu to Cu may be useful in the formation of multilayer copper metallization technology.

## References

1. S. P. Murarka, R. J. Gutmann, A. E. Kaloyeros and W. A. Lanford, "Advanced multilayer metallization schemes with copper as interconnection metal", Thin solid Films, 236 (1993) 257-266.
2. Ronald J. Gutmann, T. Paul Chow, William N. Gill, Alan E. Kaloyeros, William A. Lanford and Shyam P. Murarka, "Copper Metallization Manufacturing Issues for

- Future ICs", Symposium Proceedings of Materials Research Society, Vol. 337, 41-57, 1994.
3. Semiconductor Technology Handbook, pp9.8 – 9.12, 1985.
  4. Stefan Bengtsson, "Semiconductor Wafer Bonding: A Review of Interfacial Properties and Applications", Journal of Electronic Materials, vol. 21, No. 8, 1992, pp 841-862.
  5. R. W. Bower, M. S. Ismail and B. E. Roberds, "Low Temperature  $\text{Si}_3\text{N}_4$  Direct Bonding", *Appl. Phys. Lett.*, 28 June 1993 pp. 3485-3487.
  6. Y. Albert Li, Robert W. Bower and Izak Bencuya, "Low Temperature Copper to copper Direct Bonding", Jpn. J. Appl. Phys. Vol.37(1998) pp.L1068-L1069, Part 2, No. 9A/B, 15 September 1998.
  7. R. W. Bower, W. Chan, L. Hong and V. H. C. Watt, "Mechanical Properties Of Low Temperature Bonded Materials", Journal of the Electrochemical Society, Oct. 1995.
  8. D. K. Schroder, "Semiconductor Material and Device Characterization", pp127-128, 1990.

	Cu	Al	W
Resistivity ( $\mu\Omega\text{-cm}$ )	1.67	2.66	5.65
Young modulus $\times 10^4$ (MPa)	12.98	7.06	41.1
Thermal conductivity ( $\text{W m}^{-1}$ )	398	238	174
Corrosion resistance in air	Poor	Good	Good
Melting point (K)	1358	933	3660
Specific heat capacity ( $\text{J kg}^{-1} \text{K}^{-1}$ )	386	917	138
Delay ( $\text{ps mm}^{-1}$ )	2.2	3.7	7.8
Thermal stress on Si ( $\text{MPa K}^{-1}$ )	2.5	2.1	0.8
Adhesion to $\text{SiO}_2$	Poor	Good	Poor
Deposition			
Sputtering	√	√	√
Evaporation	√	√	√
CVD	√	√?	√
Etching			
Dry	?	√	√
Wet	√	√	√
Electromigration Resistance	$10^3$ better than Al	Poor	

Table 5.1. Comparison of properties of possible interlayer metals (after ref. 3 and 4).

Current (mA)	Voltage (mV)	$\rho_c$ ( $\Omega\text{-cm}^2$ )
100.00	0.40000	7.2000e-04
200.00	0.89000	8.0100e-04
300.00	1.3500	8.1000e-04
400.00	1.8100	8.1450e-04
500.00	2.2700	8.1720e-04
602.00	2.7000	8.0731e-04
50.000	0.17000	6.1200e-04
-50.000	-0.24000	8.6400e-04
-100.00	-0.49000	8.8200e-04
-200.00	-1.0100	9.0900e-04
-300.00	-1.5300	9.1800e-04
-400.00	-2.0700	9.3150e-04
-500.00	-2.6500	9.5400e-04
-600.00	-3.2500	9.7500e-04

Table 5.2 Contact resistance measurement for Cu-Cu direct bonding, the contact area is  $18 \text{ mm}^2$  for this sample.



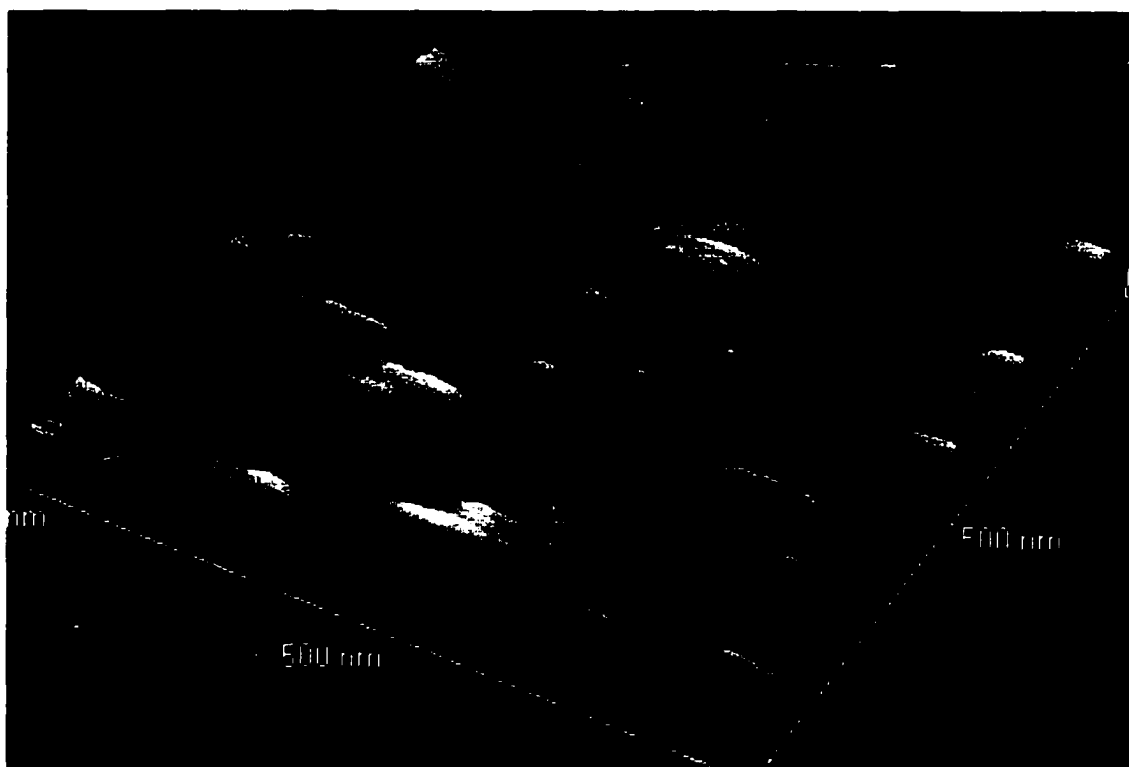


Fig. 5.1. AFM surface roughness measurement. Scan range is  $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$ ; the vertical scale is 0 to 11 nm.

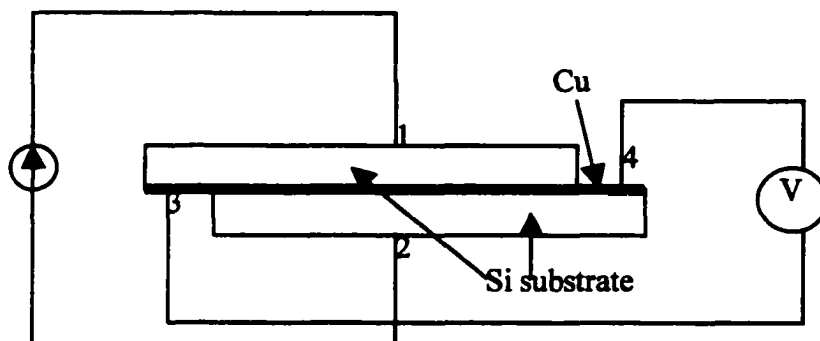


Fig. 5.2a. Cu-Cu contact resistance measurement experimental setup.

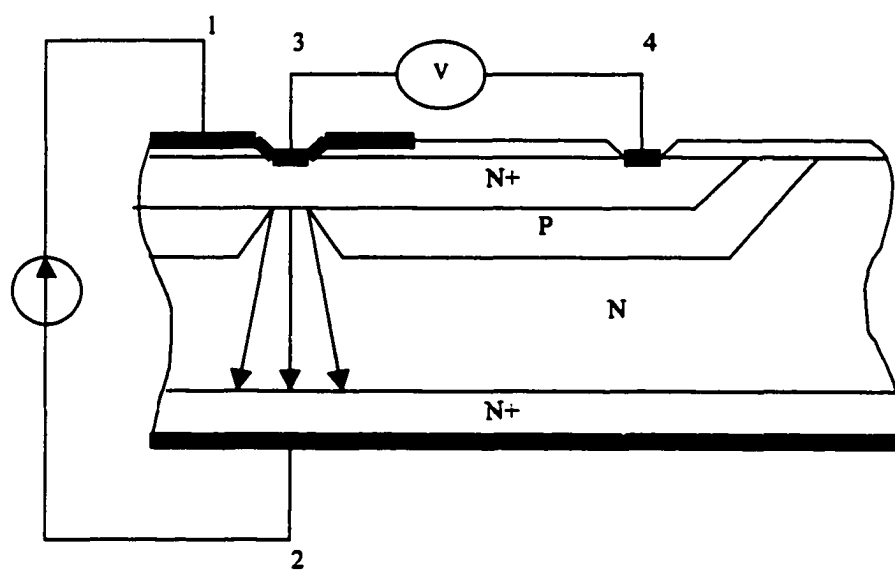


Fig. 5.2b. Cross section of the vertical Kelvin structure to measure the contact resistance

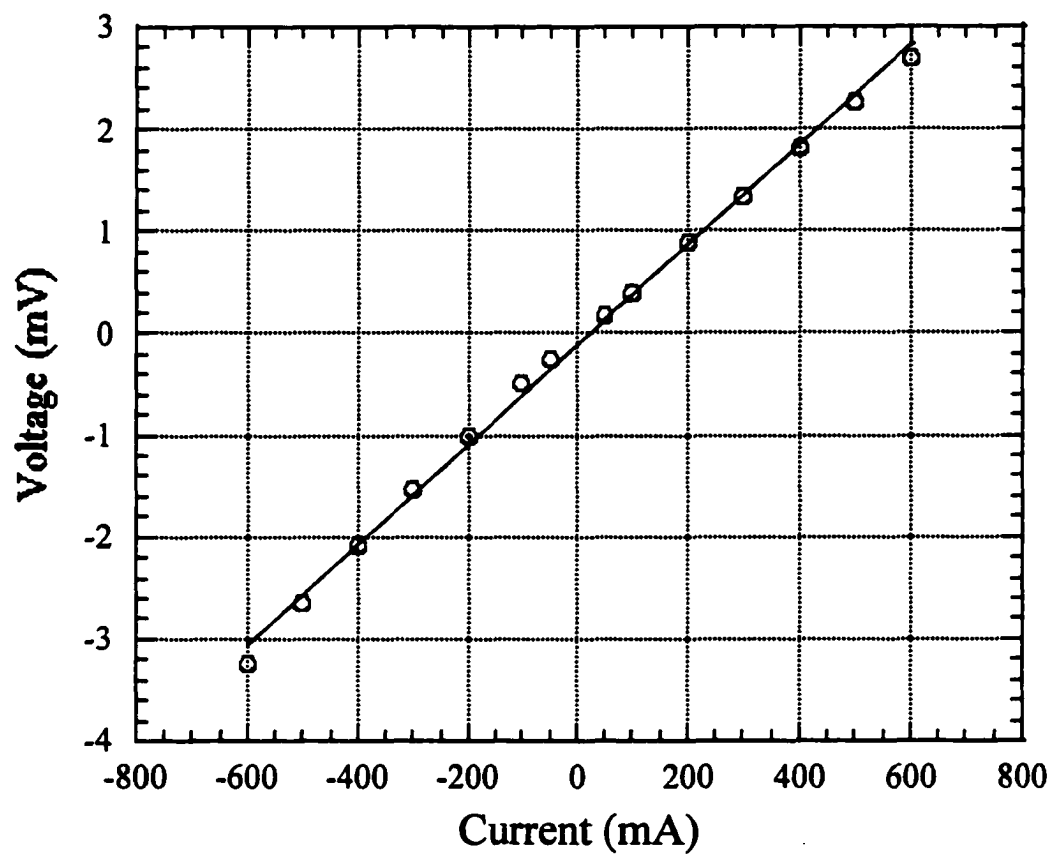


Fig. 5.3. Measured Cu-Cu specific contact resistance, the contact area in this figure is 18 mm<sup>2</sup>.

## CHAPTER 6

### Summary and Future work

#### 6.1. Overall Process Flow for the Vertical Integration of Multilayer Microstructure

A new vertical integrated multi-layer microstructure is proposed in this work. Necessary approaches such as low temperature wafer direct bonding, reversible bonding, ion cut for processible thin films and copper direct bonding are demonstrated [1-7]. These processes make the vertical integration of multi-layer structure possible. Figure 6.1 illustrates the overall process flow for the vertical integration of multilayer microstructure.

A number of technologies described in this work are the keys in forming the stacked three-dimensional structure. The technologies are all compatible with the current environment required stacking processed structures. Aligned wafer bonding, low temperature direct bonding copper and silicon based semiconductor, and reversible bonding technologies are presented in this work. Techniques for material extraction and transfer are the keys in creating the multilayer microstructures. Extended smart-cut technology or hydrogen implantation induced silicon layer splitting and film transfer is developed and discussed. The process described shows the reduced the cutting time and temperature, reduced hydrogen implantation dose by pre-implanting boron as the catalyst material to trap hydrogen cluster, and improved as-splitting surface roughness [8]. These extended methods of ion cut technology will be very useful in creating three-dimensional structures with partially or fully processed device layers.

## 6.2.Future Work

Two issues should be investigated, fully understood, and developed in the future work.

Transportation of the extracted thin film is a critical issue in this process needs to be developed. Up to date, a modular lift-off process, or peel-off process, is under development. The idea is very similar to the work published by E. Yablonovitch et al in the early 1990's, where they grew  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  on a very thin layer of AlAs on top of GaAs substrate, all lattice matched, then lift off the top  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  by etch away the sacrificial AlAs layer, and finally van der Waals bond it to a target substrate [9, 10]. Unfortunately, the lift-off is an extremely slow process because the total time is limited by etching away the AlAs thin layer, and it is diffusion limited process, therefore only very small piece of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  films were lift off in the previous experiment. In peel-off process, on the other hand, by temporarily bond the device layer to a transportation structure, etching away the sacrificial layer process is speed up by bending the wafer from the edge. It is demonstrated in an experiment that it is possible to bend a 10cm silicon wafer to a radius of 2m!

Another issue is the possibility to implement this layer splitting and film transfer technique into a processed device wafer. The boron-hydrogen co-implantation indicates a great flexibility to do so. Experimental results show that upon co-implantation, it is not necessary to superimpose the boron penetration depth exactly on top of the hydrogen penetration depth. Up to a few thousand angstroms offset may still produce surface blisters, even layer splitting, for a reduced hydrogen implantation dose ( $\sim 2 \times 10^{16} / \text{cm}^2$ , with boron co-implantation at  $1 \times 10^{15} / \text{cm}^2$ ) and at a reduced cutting temperature ( $\sim 200$

°C) [11]. Although quite a few publications demonstrated that hydrogen had the tendency to diffuse in boron-doped silicon, pairing with B<sup>-</sup> at the lattice sites, or even to be trapped in cluster at the dopant sites [12]. The movement of hydrogen and/or boron in the silicon should be investigated and fully understood.

## **References**

14. Y. Albert Li and Robert W. Bower, "Low temperature direct bonding using pressure and temperature", Proceedings of SPIE, Vol. 3184, June 1997, 124-128.
15. Robert, W. Bower and Y. Albert Li, "Reversible low temperature direct bonds for fabrication of three-dimensional microelectronic structures", Proceedings of SPIE, Vol. 3184, June 1997, 120-123.
16. Robert W. Bower, Y. Albert Li and Frank Y-J Chin, "The hydrogen ion cut technology combined with low temperature direct bonding", Proceedings of SPIE, Vol. 3184, June 1997, 2-4.
17. Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March).
18. Y. Albert Li, Robert W. Bower and Izak Bencuya, "Low Temperature Copper to copper Direct Bonding", Jpn. J. Appl. Phys. Vol.37(1998) pp.L1068-L1069, Part 2, No. 9A/B, 15 September 1998.
19. Robert W. Bower, Y. Albert Li, Wade Xiong, Jimmy Kuei and Bryon Washoe, "Low Temperature Plasma Activated Water Bonded Wafers", To be published 1998.
20. Bryon Washoe and Robert W. Bower, "Voidless Plasma Activated Low Temperature Bonding of Wafers", To be published 1998.

21. Y. Albert Li and Robert W. Bower, "Surface Conditions and Morphology of Hydrogen Ion Cut Low Temperature Bonded Thin Film Layers", to be published, 1998.
22. E. Yablonovitch, T. Gmitter, J.F. Harbison, and R. Bhat, "Extreme selectivity in the lift-off of epitaxial GaAs films", Appl. Phys. Lett. **51** (26), 28 December 1987, 2222-2224.
23. E. Yablonovitch, D.M. Hwang, T.J. Gmitter, L.T. Flirez, and J.P. Harbison, "Van der Waals bonding of GaAs epitaxial liftoff films onto arbitrary substrates", Appl. Phys. Lett. **56** (24), 11 June 1990, 2419-2421.
24. Robert W. Bower, Louis LeBoeuf, and Y. Albert Li, "Transposed Splitting of Silicon Implanted With Spatially Offset Distributions of Hydrogen and Boron", IL NUOVO CIMENTO, Vol. 19, D, N. 12, 1871-1879, December 1997.
25. Jeffrey T. Borenstein, James W. Corbett and Stephen J. Pearton, "Kinetic model for hydrogen reactions in boron-doped silicon", J. Appl. Phys. **73** (6), 15 March 1993.

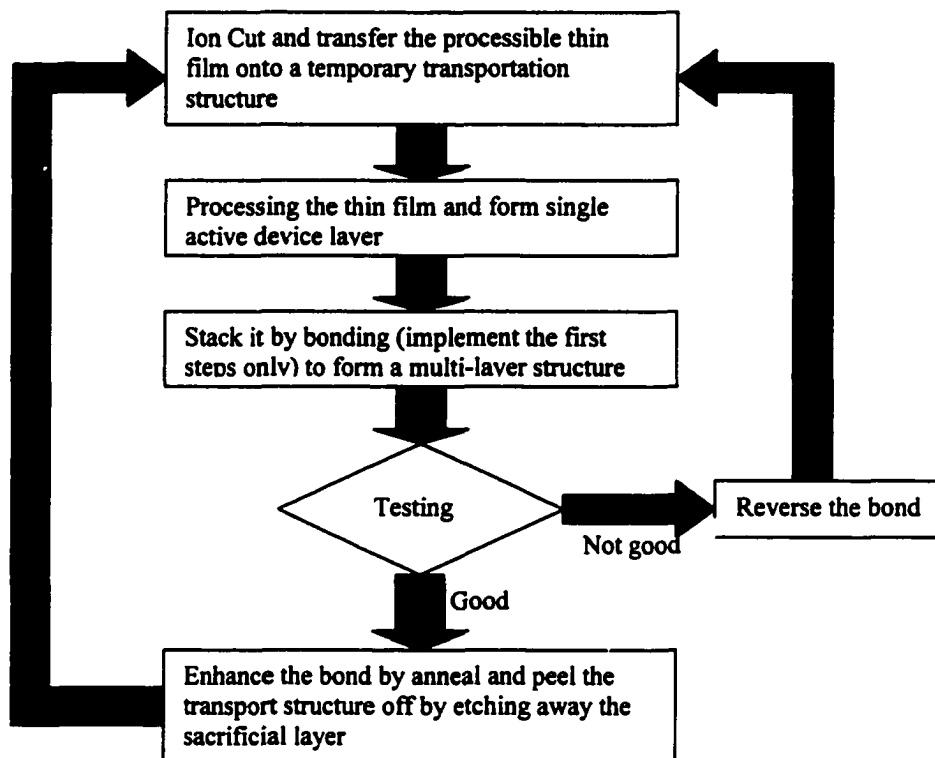


Fig. 6.1. Overall process flow for the vertical integration of multi-layer microstructure



## Appendix

The bonds are rated using a classification of 1 to 5 described in an earlier publication <sup>6)</sup> with 5 being a bond without any voids under IR detector. See Table A.1 below for a detailed description of the classification system. Only type 4 or 5 bonds are found to form strong bonds after long time anneal, the strength of the bond is tested after the final anneal to be greater than 1,000 ergs/cm<sup>2</sup>. Samples of each bond type are shown in figures A.1 through 5.

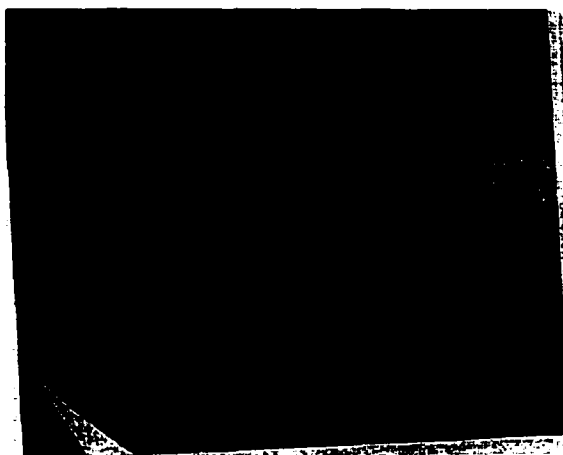
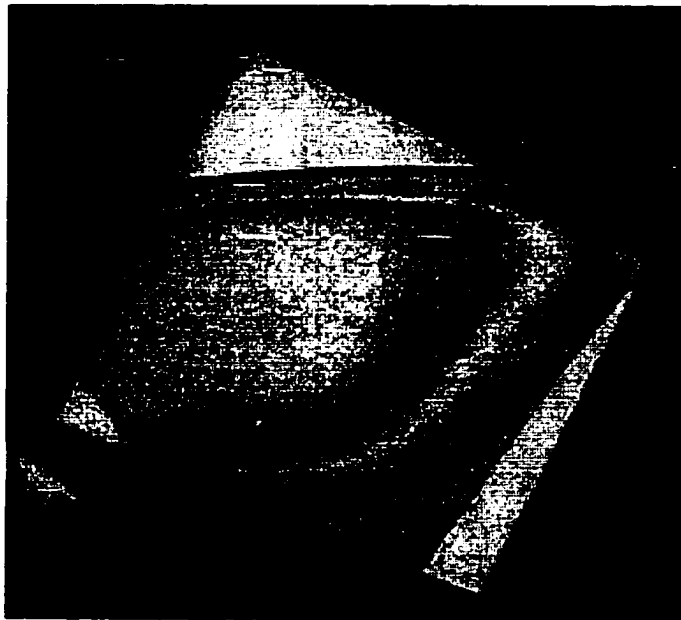


Figure A.1. Type 1 Bond



Figure A.2. Type 2 Bond



**Figure A.3. Type 3 Bond**



**Figure A.4. Type 4 Bond**

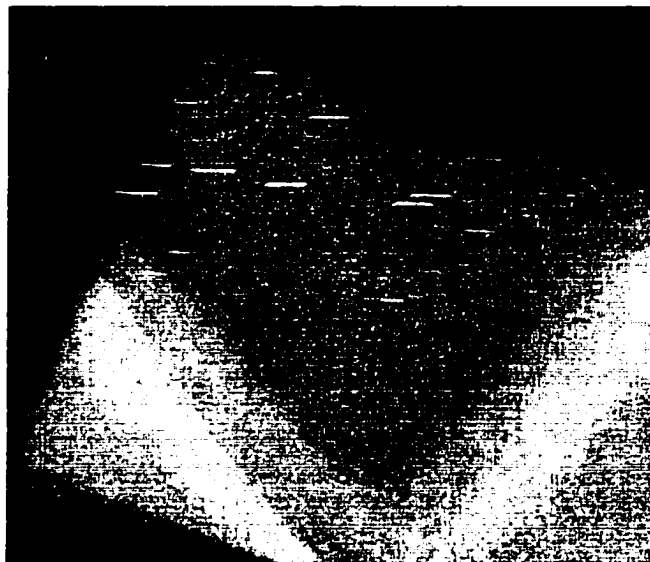


Figure A.5. Type 5 Bond

Rating	Description
1	No bond or very weak bond easily to be broken
2	Soft bond, or small region (spot) of solid bond
3	Solid bond to 1/3 of contact area, soft elsewhere
4	Solid bond to 2/3 of contact area, fringe patterns at edges
5	99.9% bonded area, void free

Table A.1. Bond classification, only type 4 or 5 bonds shown in IR can produce strong bonding where the bond strength is measured  $>1,000$  ergs/cm<sup>2</sup>.

## References

1. R.W. Bower, W.Chan, L.Hong, L. LeBoeuf, Y.A. Li, and J. Lee, "Optimization of Low Temperature NH<sub>3</sub> Plasma Activated Direct Bonding", Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head, SC, June 1996
2. Y. Albert Li and Robert W. Bower, "Systematic Low Temperature Silicon Bonding using Pressure and Temperature", Japanese Journal of Applied Physics, Vol. 37, No. 3, 737-741 (March), 1998