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# Low temperature Si<sub>3</sub>N<sub>4</sub> direct bonding

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Extremely strong bonds can be formed between smooth, clean layers of Si<sub>3</sub>N<sub>4</sub> at temperatures ranging between 90 and 300 °C. These bonds have been formed between Si<sub>3</sub>N<sub>4</sub> layers deposited on various substrates with deposition temperatures as low as 300 °C. The bond is initially formed at room temperature and subsequently annealed at temperatures ranging between 90 and 300 °C. Thus, the materials bonded in this manner are never exposed to temperatures higher than 300 °C. This low temperature bond greatly expands the range of applications of direct bonding which had heretofore been restricted by the temperatures of 700 to 1000 °C required by conventional wafer bonding.

Direct wafer bonding between layers of silicon and SiO<sub>2</sub> have been studied and applied successfully to a variety of applications including bond and etch back for silicon-on-insulator devices (SOI),<sup>1</sup> sensors and actuators,<sup>2,3</sup> and aligned wafer bonded structures.<sup>4-6</sup> Although these bonding techniques have proven useful the high anneal temperature required by this technique has limited the applications. Previously, it has been reported that Si<sub>3</sub>N<sub>4</sub> is not a bondable surface,<sup>1,7</sup> although an oxidized surface of nitride was reported to bond at high temperatures consistent with silicon fusion bonding.<sup>8</sup> Direct bonding of low-pressure metalorganic chemical-vapor deposition (LPCVD) of Si<sub>3</sub>N<sub>4</sub> at temperatures greater than 800 °C has also been reported.<sup>9</sup> The Si<sub>3</sub>N<sub>4</sub> bonding technique described here allows the fabrication of microstructures with materials that are able to withstand temperatures of 100 to 300 °C. The applications which are possible with this procedure include a variety of optoelectronic and high frequency devices that require materials such as GaAs and InP. This low temperature bonding technique reduces the problems of thermal mismatch in bonding dissimilar materials. Thus, materials such as GaAs and InP may be bonded to silicon to combine the power and economy of silicon integrated circuits to these high performance optoelectronic materials. Diamond heat sinks may also be bonded to a variety of materials to improve heat dissipation or mechanical durability. It also follows that combinations of III-V and II-VI materials or devices may be combined with low temperature bonding that are otherwise difficult to merge with conventional heteroepitaxial techniques. Van der Waals bonding of GaAs using epitaxial lift-off has been successfully accomplished to bond GaAs to a number of substrates.<sup>10</sup> The strength of this epitaxial lift-off bond has subsequently been improved by using an interfacial layer of Pd.<sup>11</sup> However, the cited literature does not report the capability of producing electrically conducting and insulating regions, nor can prefabricated structures be critically aligned and bonded with the epitaxial lift-off process.

Additionally, low temperature bonding can be applied to planarized surfaces of "completed" integrated circuit

chips and wafers which include the conventional Al metalization. Normally, the Al metalization would limit bonding steps to temperatures of 400 to 450 °C, which again precludes conventional high temperature bonding. Completed integrated circuits have only been bondable using organic glues or indium bumps. Both of these types of bonds have limitations compared with a clean, low temperature Si<sub>3</sub>N<sub>4</sub> bond.<sup>12,13</sup> To complete this discussion we should add that we have found a companion electrically conducting material, TiN, to complement Si<sub>3</sub>N<sub>4</sub> to provide both insulating and conducting surfaces which may be align bonded at low temperature. TiN coated silicon wafers have been activated and found to produce strong bonds at temperatures as low as 90 °C. The combination of Si<sub>3</sub>N<sub>4</sub> and TiN surfaces align bonded provide electrical, insulating, and optical connections between the joined layers for three dimensional optoelectronic elements.<sup>14</sup>

Material preparation for low temperature Si<sub>3</sub>N<sub>4</sub> bonding has many similarities to other wafer bonding.<sup>15</sup> Wafer flatness and surface roughness have been found to be important physical considerations in bonding other thin film deposited materials.<sup>16</sup> Deposition of about 500 Å thick Si<sub>3</sub>N<sub>4</sub> was achieved using plasma enhanced chemical deposition at 300 °C. The wet chemical cleaning of the nitride requires a controlled time treatment of a modified RCA clean where the NH<sub>4</sub>OH is diluted to 25% of that used in a standard RCA clean. The reduced NH<sub>4</sub>OH in the base cleaning agent offers the effectiveness of a standard RCA clean with less silicon nitride surface roughening.<sup>17</sup> The final step in the surface preparation includes a 10 s dip in 1% HF which renders the surfaces hydrophilic and enables bonding immediately after rinsing and spin drying. A one step process of bonding Si<sub>3</sub>N<sub>4</sub> has also been developed. A NH<sub>3</sub> plasma activation for several minutes immediately after Si<sub>3</sub>N<sub>4</sub> deposition without breaking the plasma renders the surface for direct bonding. The utilization of NH<sub>3</sub> plasma treatment in high temperature direct bonding of silicon and silicon dioxide has been reported previously.<sup>18</sup>

We have successfully bonded silicon to silicon, silicon to SiO<sub>2</sub>, and Si to GaAs using Si<sub>3</sub>N<sub>4</sub> as the intermediate bonding layer. The bonded area of the Si<sub>3</sub>N<sub>4</sub> direct bond

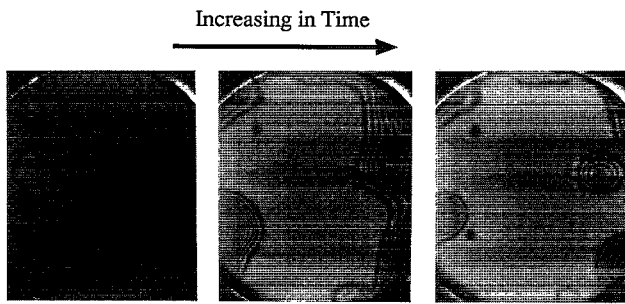


FIG. 1. Infrared images of the spread in the bonded area of  $\text{Si}_3\text{N}_4$  surfaces at room temperature upon initial contact of the two substrates.

after initial contact of the two substrates appears to slowly grow as illustrated in the infrared micrograph in Fig. 1. The rate of growth of the bonded area is not as rapid as in the silicon direct bonding. The  $\text{Si}_3\text{N}_4$  direct bond has been found to be strong enough to result in three dimensional fracture in tensile strength tests conducted on samples annealed for various lengths of time at temperatures ranging from 90 to 300 °C. These data are presented in Fig. 2 which plots  $\ln(t)$  versus  $1000/T$ , where  $t$  is the annealing time leading to a given fracture morphology as indicated in this figure, and  $T$  is temperature in Kelvin. This figure plots data for low temperature  $\text{Si}_3\text{N}_4$  bonds and also for high temperature silicon bonds.<sup>19</sup> These sets of data have been analyzed and fit to the relationship  $\ln(t) = E_a/K(1/T) + C$ , where  $C$  is a constant.  $E_a$  is found from this analysis to be equal to approximately 0.37 eV for  $\text{Si}_3\text{N}_4$  direct bonds and 0.73 eV for Si direct bonds where the time  $t$  was determined for the onset of three-dimensional fracture for a tensile pull that resulted in fracture of the bonded couple.

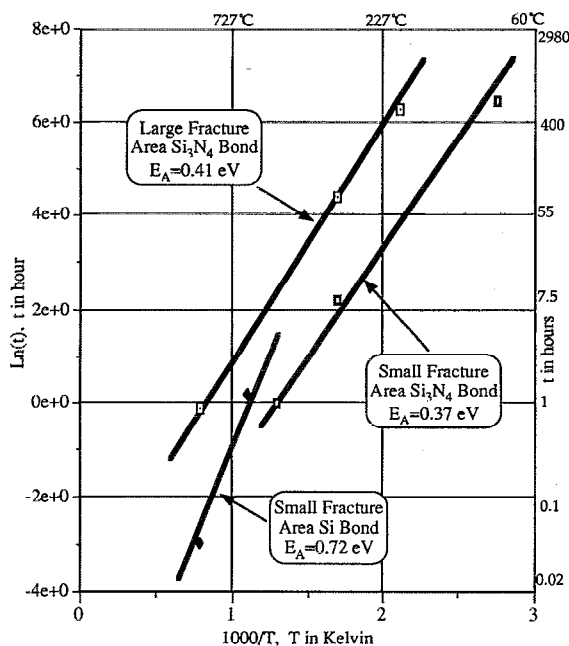


FIG. 2. Graph plot of  $\ln(t)$  vs  $1/T$ , where  $t$  is the annealing time to give the indicated fracture-type and  $T$  is temperature in Kelvin. Data for  $\text{Si}_3\text{N}_4$  direct bond and silicon direct bond were plotted on the same graph for comparison.

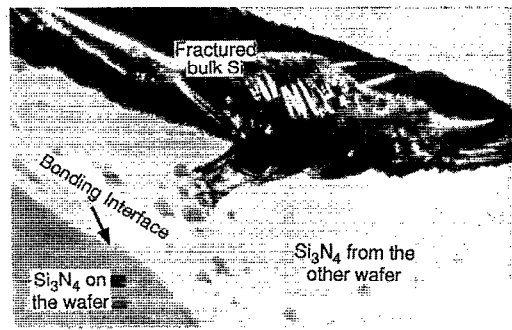


FIG. 3. A photomicrograph of one of the tensile test samples that shows an example of the three-dimensional fracture of  $\text{Si}_3\text{N}_4$  direct bonds. Both substrates are silicon.

The time  $t$  required to create a large area three dimensional fracture for  $\text{Si}_3\text{N}_4$  direct bonds was also determined and found to fit a linear plot of  $\ln(t)$  versus  $1000/T$  over temperatures ranging from approximately 200 to 1000 °C. For the large area fracture case an approximate value of  $E_a = 0.41$  eV was determined for the  $\text{Si}_3\text{N}_4$  direct bonds. Thus, the values for  $E_a$  for the onset of fracture and large area fracture for  $\text{Si}_3\text{N}_4$  direct bonds are found to be within 10% of each other indicating that a common limiting process may control bond development over temperatures ranging from 90 to 1000 °C. Fracture occurs at about 2 MPa for  $\text{Si}_3\text{N}_4$  direct bonds. This value may be compared to the bulk silicon fracture of approximately 10 MPa.<sup>19</sup> The lower value for the fracture of  $\text{Si}_3\text{N}_4$  may be related to the fact that three-dimensional fracture may be initiated by defects in the substrate induced by internal stress caused by the deposited  $\text{Si}_3\text{N}_4$  film. This conjecture tends to be corroborated by the examination of the bond fracture shown in Fig. 3. It should be noted in this photomicrograph that the bonded interface between the  $\text{Si}_3\text{N}_4$  layers appears to be intact while fracture has occurred in the bulk of the bonded silicon substrates. Figure 4 is a photomicrograph that shows the fractured surface of Si bonded to GaAs with  $\text{Si}_3\text{N}_4$  as the intermediate layer. This photomicrograph reveals that fracture occurred in the relatively more brittle GaAs rather than the silicon or silicon nitride interface.

The significant difference in activation energy between the  $\text{Si}_3\text{N}_4$  direct bond and the silicon direct bond would

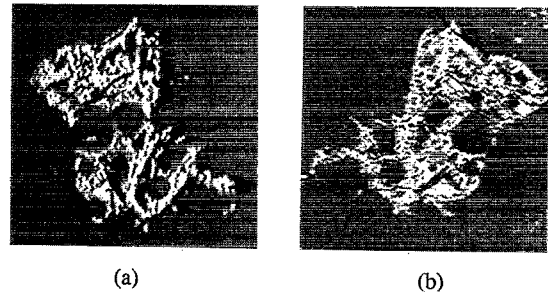
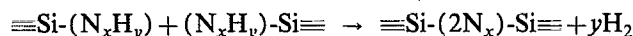


FIG. 4. A photomicrograph of the fractured surface of a small sample of Si bonded to GaAs via  $\text{Si}_3\text{N}_4$  direct bonding, where (a) is the silicon substrate and (b) is the GaAs substrate.

suggest that a considerably different surface chemistry is involved for the  $\text{Si}_3\text{N}_4$  direct process than that proposed by Stengl for the silicon direct bond.<sup>20</sup> The final stage of the cohesive bond in silicon direct bonding has been described in many articles including Stengl's as a covalent Si-O-Si chemical structure.<sup>20</sup> The Si—O—Si bond is suggested to form via the interaction between two radicals of SiOH at temperatures higher than 700 °C.<sup>20</sup> We suggest that surface free radicals of Si-N-H may be responsible for the formation of direct bonds at the  $\text{Si}_3\text{N}_4$ - $\text{Si}_3\text{N}_4$  interface. The cohesive direct bond of the Si-(N)-Si-type has been achieved at temperatures as low as 90 °C. The activation energies of 0.37 and 0.41 eV for  $\text{Si}_3\text{N}_4$  direct bonding are found to be comparable with the activation energy of the permeability of  $\text{H}_2$  in vitreous silica of about 0.38 eV reported by Lee *et al.*<sup>21</sup> Based on this result we speculate that a chemical reaction as follows:



may be responsible where the released hydrogen diffuses from the bonding interface. The surface chemistry of treated  $\text{Si}_3\text{N}_4$  layers using both processes described in this letter are currently under investigation.

This letter has described the technique to achieve low temperature  $\text{Si}_3\text{N}_4$  direct bonding. Successful direct bonding of the coated  $\text{Si}_3\text{N}_4$  layer has been applied to silicon, silicon dioxide, and GaAs substrate wafers. The activation energy for  $\text{Si}_3\text{N}_4$  direct bonding was found to range from 0.37 to 0.41 eV which is approximately half of the value found for silicon direct bonding. This low activation energy allows bonding of optoelectronic materials and completed integrated circuits with Al metalization in place. We suggest that the surface chemistry of  $\text{Si}_3\text{N}_4$  bonding may differ from that found in direct silicon bonding. Two methods of a wet chemical process and a one-step plasma process for surface preparation prior to initial  $\text{Si}_3\text{N}_4$  direct bonding has been established.

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