

**IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF NEW JERSEY**

INVENSAS BONDING TECHNOLOGIES, INC.,

Plaintiff,

v.

SAMSUNG ELECTRONICS AMERICA, INC., and  
SAMSUNG ELECTRONICS CO., LTD.,

Defendants.

Civil Action No.: 17-7609-RMB-KMW

**JURY TRIAL DEMANDED**

Magistrate Judge Karen M. Williams

**DECLARATION OF THE ELECTROCHEMICAL SOCIETY**

I, Elizabeth Craanen, am over twenty-one (21) years of age. I have never been convicted of a felony, and I am fully competent to make this declaration. Under penalty of perjury, I declare the following to be true to the best of my knowledge, information, and belief:

1. I am Director of Publications for The Electrochemical Society, Inc. ("ECS").
2. Among my responsibilities as Director of Publications, I act as a custodian of certain records for ECS.
3. I make this declaration based on my personal knowledge, information contained in the business records of ECS, or confirmation with other responsible ECS personnel with such knowledge.
4. ECS received a subpoena in the above-captioned matter requesting the production of documents.
5. It is the regular practice of ECS to publish articles and other writings and make them available to the public. ECS maintains copies of publications in the ordinary course of its regularly conducted activities.

6. The articles listed below, along with their abstracts, are attached as Exhibits to this declaration:

Exhibit	Reference	Date of Public Availability
A	M. Reiche et al., <i>The Effect of a Plasma Pretreatment on the Si/Si Bonding Behaviour</i> , 97-36 Electrochemical Society Proceedings 437 (1997).	February 23, 1998
B	Amirfeiz et al., <i>Formation of Silicon Structures by Plasma-Activated Wafer Bonding</i> , Journal of the Electrochemical Society, Vol. 147 (2000) pp. 2693-2698.	July 11, 2000
C	Karin Ljungberg et al., <i>Modification of Silicon Surfaces with H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:HF and HNO<sub>3</sub>:HF for Wafer Bonding Applications</i> , Journal of The Electrochemical Society, Vol. 143 No. 5 (1996) pp. 1709-1714.	May 14, 1996
D	W. P. Maszara, <i>Silicon-on-Insulator by Wafer Bonding: A Review</i> , Journal of The Electrochemical Society, Vol. 138, No. 1 (1991).	January 3, 1991
E	E. Bertagnolli, et al., <i>Interchip Via Technology - Three Dimensional Metallization or Vertically Integrated Circuits</i> , Electrochemical Society Proceedings, v. 97-36, 509-520 (1997).	February 23, 1998

7. I obtained a copy of each of the attached Exhibits by downloading the contents from the ECS Digital Library, [www.ecsdl.org](http://www.ecsdl.org), and Google Books, [www.books.google.com](http://www.books.google.com), where they are maintained in the ordinary course of ECS's business.
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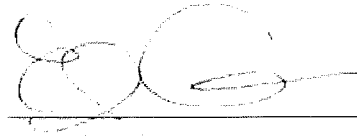
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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct and that the foregoing is based upon personal knowledge and information and is believed to be true.

Dated: September 20, 2018

By:

A handwritten signature in black ink, appearing to read 'Elizabeth Craanen', written over a horizontal line.

Elizabeth Craanen

## EXHIBIT A

## THE EFFECT OF A PLASMA PRETREATMENT ON THE Si/Si BONDING BEHAVIOUR

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The effect of plasma treatments (reactive ion etching in oxygen- and/or fluorine-containing plasmas) on Si/Si wafer bonding was investigated. Etching in SF<sub>6</sub> caused a bonding behaviour generally known from hydrophobic (HF etched) samples, whereas adding O<sub>2</sub> to the feed gas caused the Si(100) surfaces to become hydrophilic and spontaneous bonding was achieved. Plasma treatments in mixtures of oxygen with SF<sub>6</sub> or CHF<sub>3</sub> result in higher interface bond energies than for hydrophilic bonded wafer pairs already after annealing at  $T \geq 400^\circ\text{C}$ . Very strong bonds, however, are even obtained by lower temperature annealing ( $T \leq 400^\circ\text{C}$ ) after plasma treatments in O<sub>2</sub>

### INTRODUCTION

Silicon wafer direct bonding is a technology promising for VLSI, semiconductor power and sensor device applications [1]. For most applications, an additional annealing step at higher temperatures is required after the initial room-temperature bonding in order to increase the bonding strength. There are, however, numerous applications such as the bonding of processed wafers for sensor fabrication, which allow only short postannealing at relatively low temperatures such as 400°C. Therefore, an activation process of the bonding surfaces is desirable, which causes high interface energies already at relatively low temperatures. One possibility of such an activation process is the preparation of interface layers of glass or TMOS (hydrolyzed tetramethoxysilane) which increase the interfacial energy by a factor of 2, or more, with respect to bonded hydrophilic wafer pairs (e.g. [2]). In some cases, however, interface layers are not compatible with device requirements, or their preparation cannot be integrated into the device fabrication process. Another possibility is the modification of surface bonds by plasma processes. Analyses of the bonding behaviour of silicon surfaces exposed to oxygen [3], Ar [4], or Ar/H<sub>2</sub> [5] plasmas showed an appreciable increase in the bonding strength. Treatments in oxygen plasma cause the formation of a thin oxide layer at the bonding interface, whereas surfaces cleaned (etched) in an Ar/H<sub>2</sub> plasma are bondable only after a thermal desorption of hydrogen at temperatures between 400°C and 600°C. Interfaces prepared by the latter procedure are atomically flat, showing no intermediate interface layers. But the bonding strength after room temperature bonding is about the same as for normal hydrophilic wafer bonding. Therefore, other plasma pretreatments compatible with modern device processes are required. Fluorine compounds such as SF<sub>6</sub>, CHF<sub>3</sub>, or CF<sub>4</sub> and



their mixtures with O<sub>2</sub>, N<sub>2</sub>, or H<sub>2</sub> are widely applied. All these gases are characterized by a different selectivity of etching silicon or SiO<sub>2</sub>. Therefore, the present paper is concerned with the application of pretreatments in fluorine-containing plasma to wafer bonding. Results of these experiments are compared to pretreatments in an oxygen plasma.

## EXPERIMENTAL

Czochralski-grown silicon wafers (diameter 4 in., p-type,  $\rho = 30 - 50 \Omega\text{-cm}$ ) were used for the experiments. After cleaning in standard RCA1,2 solutions, the wafers were plasma treated and subsequently bonded under dry conditions, or by an additional water flushing using the microcleanroom set-up [6]. For the plasma treatment (reactive ion etching, RIE) at 13.56 MHz the following processes were used:

- etching in SF<sub>6</sub> (100%) at a pressure of 25 Pa for 20 sec, a flow rate of 64 sccm SF<sub>6</sub>, and a rf power of 220W,
  - etching in SF<sub>6</sub>/18.9%O<sub>2</sub> mixtures (SF<sub>6</sub> : O<sub>2</sub> = 60 : 14) at a pressure of 1.4 Pa for up to 160 sec, and a rf power of 80W,
  - etching in CHF<sub>3</sub>/O<sub>2</sub> (25sccm/10sccm) at a pressure of 20 Pa for up to 20 sec, and a rf power of 200 W,
  - etching in O<sub>2</sub> at a pressure of 150 Pa for up to 15 min, and a rf power of 600 W.
- All processes were carried out under cleanroom conditions.

The bond energy was measured by the crack opening method in air. Some treatments (especially with oxygen plasma), however, cause the bond energy to increase and the crack opening method to fail. Therefore, the fracture stress was measured by tensile tests. The morphological variations of the plasma-treated surfaces and the structure of the bonding interface were characterized by different microscopic and spectroscopic methods.

## RESULTS

### Analysis of plasma treated surfaces

Treatments in fluorine-containing plasmas cause the surface roughness to increase (table 1). For instance, due to a plasma process in SF<sub>6</sub>/O<sub>2</sub> for 40 sec the surface roughness increased by a factor of more than 2 with respect to an otherwise identical RCA-cleaned wafer. An analogous roughness results from chemical etching in 1% HF solutions for 10 min [7]. The roughness is associated with first indications of a granular structure, which however, is substantially less pronounced than for etching in a CF<sub>4</sub>/O<sub>2</sub> plasma for the same time.

Results of spectroscopic ellipsometry (VASE) are shown in fig. 1 for a sample etched in SF<sub>6</sub>/O<sub>2</sub>. For modelling the plasma-etched surface, a 2-layer model is assumed on top of bulk silicon consisting of a disturbed silicon layer, about 5.2 nm thick, and an oxide layer. Other common models such as the Bruggeman effective-medium approximation (EMA layer) used for interpreting HF-etched surfaces [8] fail. For the disturbed silicon layer (Si-V), the silicon data for refractive index  $n$  and extinction coefficient  $k$  are fitted. But as fig. 1 also

shows, the differences of both are very small. The physical meaning of the disturbed layer is that it represents a layer damaged by plasma etching. This interpretation is supported by other investigations demonstrating that plasma etching causes Si lattice defects [9,10]. Furthermore, VASE measurements on surfaces analogously etched in other gases ( $\text{CF}_4/\text{O}_2$ ,  $\text{CHF}_3/\text{O}_2$ ) are interpreted on the basis of the same model. The thickness of the disturbed (damaged) layer and the data for  $n$  and  $k$  are slightly different, indicating the different degree of damage due to the etching by different gases. As other authors showed (e.g. [11]), the damage is annihilated by an appropriate postannealing.

Furthermore, etching in pure  $\text{O}_2$  causes the formation of a thin oxide layer on the surface. Its thickness mainly depends on the process time. A logarithmic dependence is observed. After long exposure times, however, a damaged layer is also detected by VASE measurements. Measurements of the contact angle of samples treated in an oxygen plasma show that they are strongly hydrophilic. Contact angles of  $2^\circ$  or less (detection limit of the method) are observed. In contrast, measurements on samples treated in a fluorine-containing plasma show that the hydrophilicity is strongly affected by the concentration of oxygen added to the gas phase. Processes with a pure fluorine plasma cause hydrophobic surfaces (especially  $\text{SF}_6$ ).

#### Wafer bonding

Wafers pretreated with the various plasmas mentioned, except those pretreated in  $\text{CF}_4$ , show a more or less spontaneous bonding. The bond energy, measured after room-temperature bonding and additional annealing, is increasing with annealing temperature, and with the oxygen concentration increasing in the fluorine-containing gases (figure 2). Wafers treated with pure  $\text{SF}_6$  show a bonding behaviour generally known from hydrophobic (HF-etched) samples (fig. 3). The dependence of the bond energy on the annealing temperature and the structure of the interface are also analogous. In contrast to that, wafers treated in a  $\text{SF}_6/\text{O}_2$  plasma bond spontaneously. All data measured after bonding at room temperature show that the interface energy  $\gamma$  is significantly higher than for bonded hydrophilic wafer pairs. Moreover,  $\gamma$  clearly increases if the wafers are etched in the  $\text{SF}_6/\text{O}_2$  plasma for up to 40 sec. Further prolonging the plasma treatment causes  $\gamma$  to decrease again. The data showed appreciable differences of  $\gamma$  between the bonding under dry conditions, and with a preceding water flushing. After bonding under dry conditions at room temperature  $\gamma$  varies by a factor of about 2 for plasma treatments up to 40 sec, whereas after more extended treatments there is no difference. The increased value of  $\gamma$  at room temperature (as compared to that of normal hydrophilic bonding) indicates a change of the surface structure, i.e. the treatment in the  $\text{SF}_6/\text{O}_2$  plasma increases the number of active sites. Assuming OH-groups as the active sites for bonded hydrophilic wafers, the differences in  $\gamma$  measured between bonding under dry conditions and with a preceding water flushing suggest that especially under room-temperature conditions the active sites produced by the plasma treatment are characterized by a higher affinity for bonding  $\text{H}_2\text{O}$  molecules via OH-groups on the surface, resulting in an increased surface energy  $\gamma$  during bonding. The complexity of the mechanism is demonstrated by the dependence of  $\gamma$  on the annealing temperature (figure 4). For  $T < 400^\circ\text{C}$ , plasma-treated wafer pairs bonded with a preceding water flushing yield values of  $\gamma$  similar to those of bonded hydrophilic wafers. After annealings above  $400^\circ\text{C}$ ,  $\gamma$  is higher than for bonded hydrophilic wafers. Moreover,  $\gamma$  values measured after annealing plasma-treated wafers bon-

ded under dry conditions, are substantially lower than for a bonded hydrophilic wafer pairs (fig. 3).

There is an analogous behaviour also with respect to the interface defect generation (bubble generation) between  $\text{SF}_6$ (100%) etched wafers and hydrophobic ones on the one hand, and  $\text{SF}_6/\text{O}_2$  etched wafers and hydrophilic ones, on the other. Figure 4 shows infrared microscope images of the same wafer pair after room-temperature bonding and after annealings at 200, 400, and 600 °C, respectively, for 1 hour. Here, plasma etching in  $\text{SF}_6/\text{O}_2$  and a preceding water flushing before bonding were applied. The generation of bubbles seems to be similar to that observed in bonded hydrophilic wafer pairs. Further annealing at higher temperatures reduces the bubble density. Interfaces without bubbles may be realized after single-step annealing at high temperatures. The same holds true also for  $\text{SF}_6/\text{O}_2$  etched and dry-bonded wafer pairs as well as for samples etched in pure  $\text{SF}_6$ , only.

Wafers bonded after being treated with an oxygen plasma result in bond energies of 0.1 to 0.2 J/m<sup>2</sup> after bonding at room temperature. The bond energy increases, however, substantially with increasing temperature (fig. 2). Strong bonds arise already after annealing at 300°C for short times. The generation of interface defects (bubbles) during annealing is mainly affected by the duration of the plasma treatment and the water flushing before bonding. Infrared microscopy did not reveal any bubbles on the samples plasma-treated before being water flushed. In contrast to that, bubbles appear in dry-bonded wafer pairs after the same annealing. This suggests that treatments in an oxygen plasma also crack residual carbon hydrogen compounds on the wafer surface, which are removed by water flushing.

#### Interfacial structure

Cross-sectional samples were prepared for high-resolution electron microscopy after annealing wafer pairs at 1100°C for 5 hours. Typical images of the interface structure are shown in figure 5. For instance, etching in pure  $\text{SF}_6$  and  $\text{SF}_6/\text{O}_2$  causes an interface structure analogous to that after chemical etching in HF solutions. Moreover, there are no differences in the interface structure of  $\text{SF}_6/\text{O}_2$ -etched samples between wafer pairs bonded with a preceding water flushing, and without. The oxide layer on the surface is always removed and both Si surfaces are directly bonded to each other. The bonded interfaces are not atomically flat as for etching in  $\text{Ar}/\text{H}_2$  plasma [5]. Instead, the interface represents a 1 to 2 nm thick defective layer. Most of the defects within the layer are of a rod-like morphology and oriented parallel to {111} lattice planes. They cannot be observed in plan-view samples due to their 1-dimensional extension. Rod-like defects were shown to consist of silicon self-interstitials rather than of foreign phases composed of impurities detected by SIMS [11]. The reason for such a defective interface layer is assumed to be the same for  $\text{SF}_6$  or  $\text{SF}_6/\text{O}_2$  etched wafer pairs as described for HF-etched ones. For the latter, an accommodation process of two rough surfaces during annealing was suggested [7].

Furthermore, etching in  $\text{CHF}_3$  causes a completely different interface structure. Here, an amorphous layer is detected in the interface. The intermediate layer is assumed to consist of fluorocarbons and/or hydrocarbon compounds, forming residual layers on the silicon surface during the plasma treatment [12]. Note that the interface is not atomically flat. In some cases cavities, which are more than 10 nm deep, are observed. In contrast, bonded interfaces

of wafer pairs treated with oxygen plasma are atomically flat and characterized by a thin ( $d \approx 2n$ ) oxide layer.

## CONCLUSIONS

Wafers pretreated with various plasmas show a more or less spontaneous bonding. The bond energy, measured after room-temperature bonding and additional annealing, is increasing with the temperature of annealing and with the oxygen concentration increasing in the fluorine-containing gases. Treatments in  $SF_6/O_2$  mixtures caused a hydrophilic bonding behaviour, but a higher interface bond energy than for hydrophilic bonded wafer pairs. There is, however, no intermediate (oxide) layer at their Si/Si interface. The highest bond energies are measured for wafer pairs pretreated in an oxygen plasma already after annealing at  $T < 400^\circ C$ .

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Table 1: Results of roughness analysis on plasma-etched Si(100) surfaces.

Data were collected from AFM measurements (analyzed area  $1 \times 1 \mu m^2$ ).

	Rms (Rq) [nm]	Ra [nm]	Rmax [nm]
RCA cleaned sample	0.128	0.102	1.176
$CHF_3/O_2$ , 40 sec	0.317	0.255	2.778
$SF_6/O_2$ , 40 sec	0.268	0.215	2.116
$O_2$ , 5min	0.157	0.125	1.523
$CF_4$ , 40 sec	1.114	0.898	9.423

2	SiO <sub>2</sub>	22.461 Å
1	Si V4	52.57 Å
0	Si Jell	0.5 mm

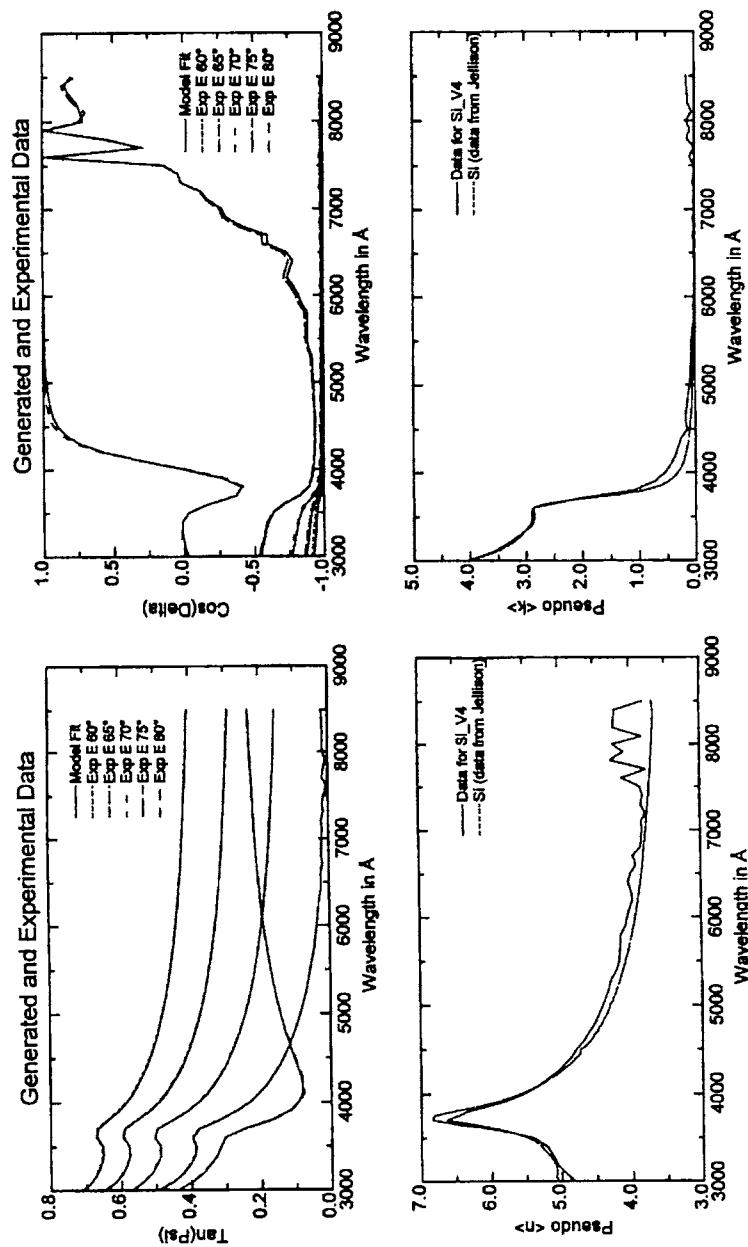
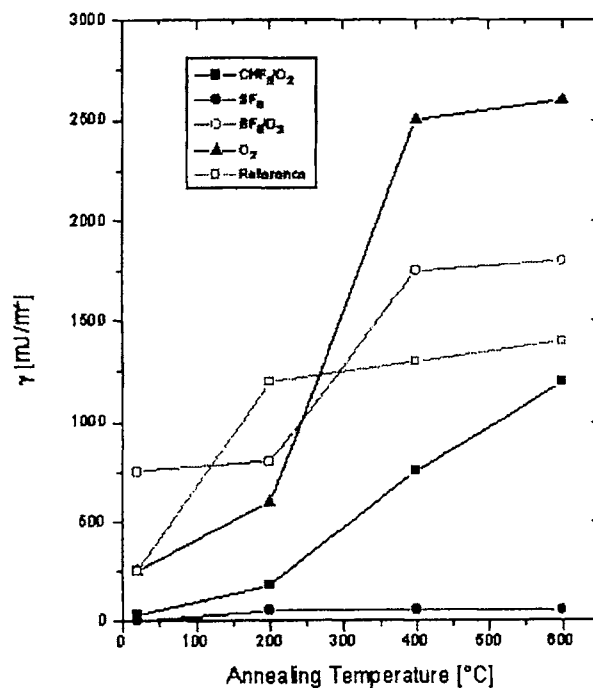
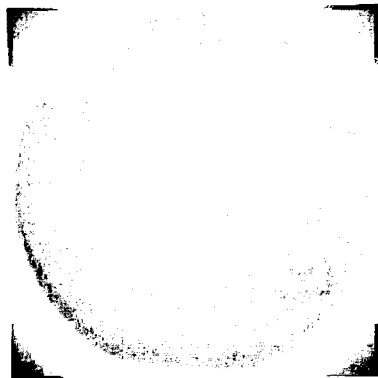


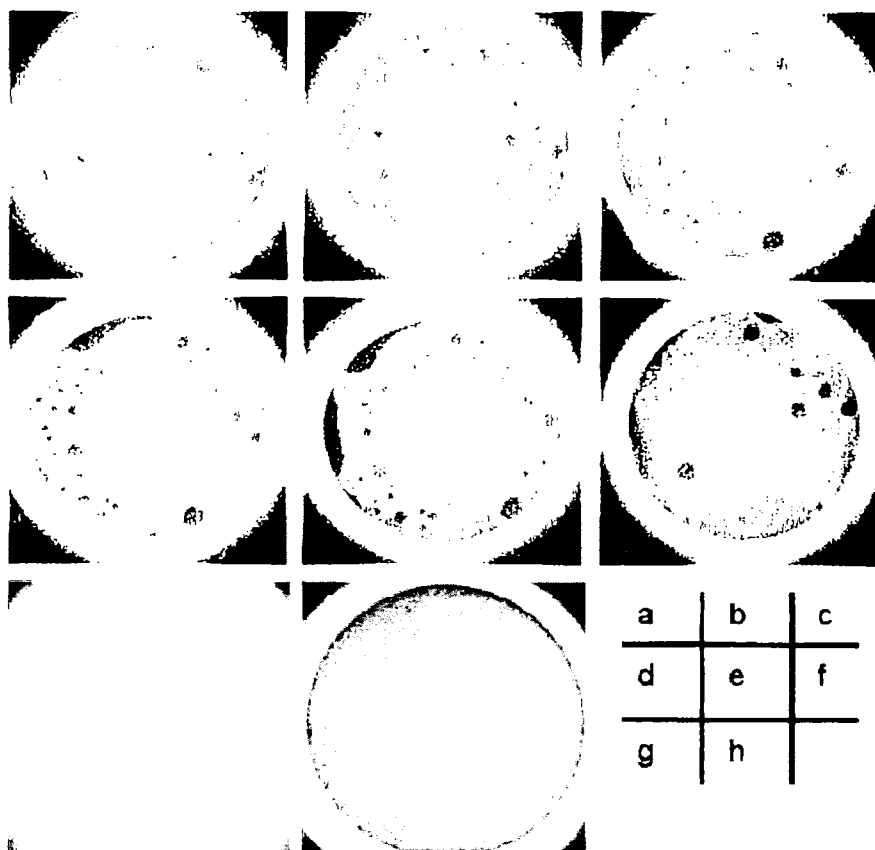
Figure 1: Ellipsometric analysis of a Si(100) surface etched in a SF<sub>6</sub>/18.9%O<sub>2</sub> plasma for 40 sec. The model used for data fit (a), the experimentally generated data for the amplitude ratio  $\Psi$  (b) and the phase shift difference  $\Delta$  (c) as well as the data used for refractive index  $n$  (d) and extinction coefficient  $k$  (e) for modeling the disturbed layer (Si-V).



**Figure 2:** Dependence of the interface bond energy  $\gamma$  on the plasma pretreatment and on the temperature during additional annealing for 1 hour after bonding. The figure shows a bonded hydrophilic wafer pair as reference (data for equilibrium conditions). Measurements by the crack propagation method.



**Figure 3:** Plasma-treated (SF<sub>6</sub>, 1min) and subsequently bonded wafer pair. Infrared microscope image after room-temperature bonding.



**Figure 4:** Infrared transmission images of bonded wafer pairs pretreated by etching in an  $\text{SF}_6/\text{O}_2$  plasma (a – f) and an  $\text{O}_2$  plasma (g,h).

a – f - Images of a wafer pair after room-temperature bonding (a) and after annealing for 1 hour at 200°C (b), 400°C (c), 600°C (d), 800°C (e), and 1100°C (f).  
g,h - Image of a wafer pair after room-temperature bonding (a) and after annealing at 300°C for 5 hours.



**Figure 5:** Electron microscope image of the interface of a bonded wafer pair pretreated in a  $\text{SF}_6/\text{O}_2$  plasma for 40 sec. After bonding the wafer pair was annealed at 1100°C for 5 hours.

## EXHIBIT B



## Formation of Silicon Structures by Plasma-Activated Wafer Bonding

P. Amirfeiz,<sup>a</sup> S. Bengtsson,<sup>a,\*</sup> M. Bergh,<sup>b</sup> E. Zanghellini,<sup>c</sup> and L. Börjesson<sup>d</sup>

<sup>a</sup>Microtechnology Centre at Chalmers and Solid State Electronics Laboratory, Department of Microelectronics, <sup>c</sup>Department of Experimental Physics, and <sup>d</sup>Department of Applied Physics, Chalmers University of Technology, SE-412 96 Göteborg, Sweden

<sup>b</sup>Celsius Consultants AB-MicroTech, SE-412 88 Göteborg, Sweden

A room temperature wafer bonding process based on oxygen plasma treatment or argon plasma treatment has been studied for surfaces of silicon, silicon dioxide, and crystalline quartz. The surface energy of the bonded samples was observed at different storage times. Atomic force microscope measurements, multiple internal reflection infrared spectroscopy, electrical characterization, secondary ion mass spectroscopy, and post-processing steps were performed to evaluate the plasma-treated surfaces and the formed bonded interfaces. Electrical measurements were used to investigate the usefulness of plasma-bonded interfaces for electronic devices. The bonded interfaces exhibit high surface energies, comparable to what can be achieved with annealing steps in the range of 600-800°C using normal wet chemical activation before bonding. The high mechanical stability obtained after bonding at room temperature is explained by an increased dynamic in water removal from the bonded interface allowing covalent bonds to be formed. © 2000 The Electrochemical Society. S0013-4651(99)12-076-7. All rights reserved.

Manuscript received December 21, 1999.

Wafer bonding is used in industry for manufacturing silicon-on-insulator (SOI) materials and sensors. In most cases the bonding procedure involves high annealing temperatures around 1000°C, while in many applications high-temperature steps are unacceptable. This may be the case when dissimilar materials are to be bonded or in sensor manufacturing when metal wires are already present on the structures to be bonded. Hence, there is a clear need of low-temperature, preferably room temperature, bonding techniques.

Plasma-assisted wafer bonding has recently attracted attention as a room temperature bonding method.<sup>1-4</sup> The bonded interfaces exhibit very high surface energies, comparable to what can be achieved with annealing steps in the range of 600-800°C using normal wet chemical activation before bonding.

When designing SOI materials and sensors it is of great importance to know how the plasma-assisted bonding technique affects the properties of the component to be manufactured. However, the bonding mechanism and the features of the bonded interface are still unclear. Therefore, this paper is aimed at finding a mechanism for the plasma activation, the driving forces for the speculated formation of covalent bonds at room temperature, and the electrical characteristics for future electronic devices.

### Experimental

n-Type, 3 in. (100) float-zone silicon wafers of 1-10  $\Omega$  cm resistivity and 1 in. crystalline quartz (AT cut) wafers were used for the bonding experiments. Some of the silicon wafers were thermally oxidized to an oxide thickness of 100 or 600 nm before bonding. All silicon wafers were cleaned for 10 min in SC1 ( $\text{NH}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ , 1:4:20) at 60°C, rinsed in deionized (DI) water, dipped in 2% HF for 20 s, rinsed in DI water, and dried before plasma exposure. The plasma exposure was made in an STS multiplex inductively coupled plasma (ICP) reactive ion etcher using a coil power of 800 W and a platen power of 20 W or 15 W for oxygen plasma, or 12 W for argon plasma. The chamber pressure was in the range of 33-39 mTorr during the plasma processing. For most experiments a plasma exposure time of 30 s was used. After plasma exposure quartz and thermally oxidized wafers as well as most of the silicon wafers were rinsed in DI water and dried. All wafers were brought into contact at room temperature in clean room ambient. After bonding, the surface energy was measured for different storage times. Each sample was only measured once. The surface energy of the interfaces was measured by the crack opening method.<sup>5</sup> For plasma processing the 1 in. crystalline quartz wafer, it was fixed to a 3 in. silicon carrier wafer by a photoresist layer. Then the quartz wafer was exposed to oxygen plas-

ma, dipped in DI water, and bonded to a 3 in. silicon wafer. After at least 24 h of storage the quartz wafer was released from the carrier by use of acetone and ultrasonics.

To characterize the roughness of silicon surfaces exposed to oxygen plasma, atomic force microscopy (AFM) (Parc Scientific Instruments model SFM-BD2-210) was used. Before measurement the wafers were stored in a container in a clean room ambient.

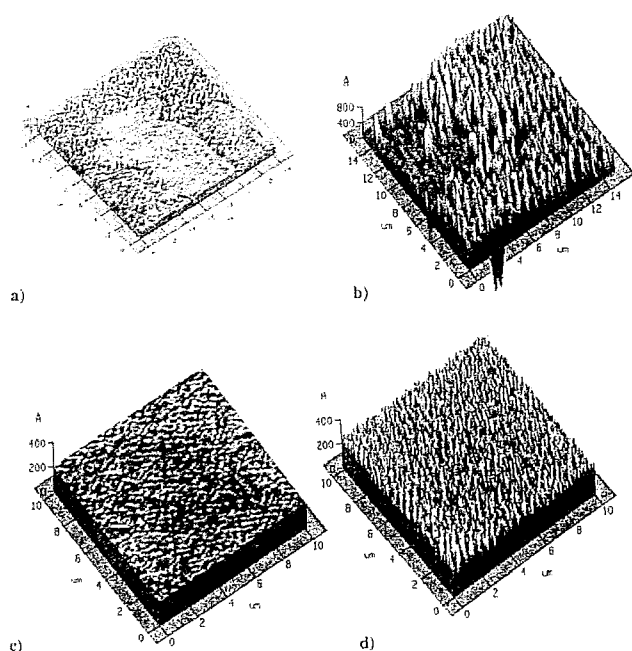
Electrical characterization was used to reveal the presence of oxide charge in the plasma oxide and to investigate the usefulness of the bonded silicon/silicon structures for electronic applications. To achieve this, two types of structures were made. Aluminum contacts were formed on top of the plasma oxide and, for the second substrate, on both sides of the bonded samples to measure oxide charge, respectively, for applications for electronic usefulness. The current vs. voltage characteristics were measured using an HP 4156B parameter analyzer and the capacitance vs. voltage characteristics were measured using an HP 4284A LCR meter.

Infrared measurements were performed in the multiple internal reflection geometry-Fourier infrared spectroscope (MIRS-FTIR). The configuration of the spectrometer is similar to that described in Ref. 6. One sample bonded after oxygen plasma treatment and dipped in water and one sample bonded immediately after oxygen plasma treatment were studied. Samples bonded after SC1 cleaning and annealing 120°C for 30 min, 200°C for 60 min, 500°C for 30 min, and 800°C for 60 min were also measured. The bonded samples were cut into rectangular pieces of about 20  $\times$  15 mm. Two optical windows were obtained by polishing the sample edges to an angle of 45°. A bulk silicon wafer was shaped in a similar fashion, and the measured spectrum was included for reference. Two flat, uncoated aluminum mirrors were fit into the sample compartment of a Bruker IFS 66v/S FTIR spectrometer to obtain the desired optical path.

### Results

The oxygen plasma creates a silica surface. The surface was shown to be reactive to an additional water rinse when it was characterized by AFM measurements. Si wafers that had been treated in oxygen plasma, dipped in water, and dried could not be properly measured immediately after the treatment, since the produced AFM data (picture) was not informative in a topographical sense. It seemed as if the probe had stuck onto the surface of the wafers. Such samples, exposed to plasma and water, could only be measured after storage. On the other hand, wafers which had not been rinsed in water were measurable. Figures 1a and b show the oxygen plasma and water-dipped surfaces after different storage times. Figures 1c and d show a surface exposed to oxygen plasma only. Similar observations concerning water-rinsed surfaces treated with Ar plasma were made.

\* Electrochemical Society Active Member.

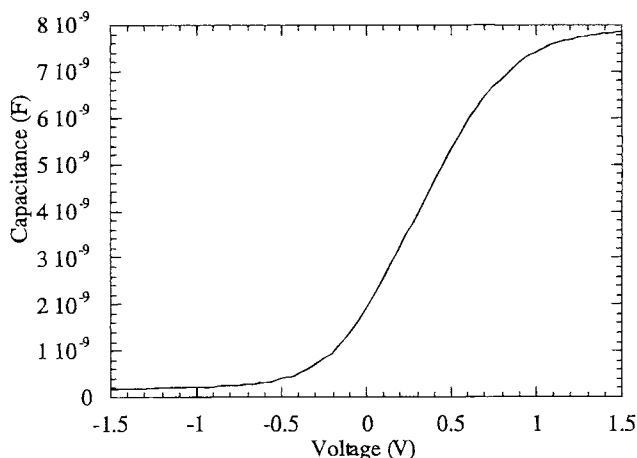


**Figure 1.** AFM scan over a surface treated in oxygen plasma for 30 s (a) dipped in water and stored for 24 h, a platen power of 20 W was used; (b) dipped in water and stored for 2 h, a platen power of 15 W was used; (c) a platen power of 15 W was used; and (d) a platen power of 20 W was used.

The surface roughness of the wafers exposed to oxygen plasma depends on the platen power of the ICP as can be seen in Fig. 1c and d. Comparison shows that the surfaces created with platen power of 20 and 15 W have different roughness, the rms values are, respectively, 37.6 and 1.07 Å.

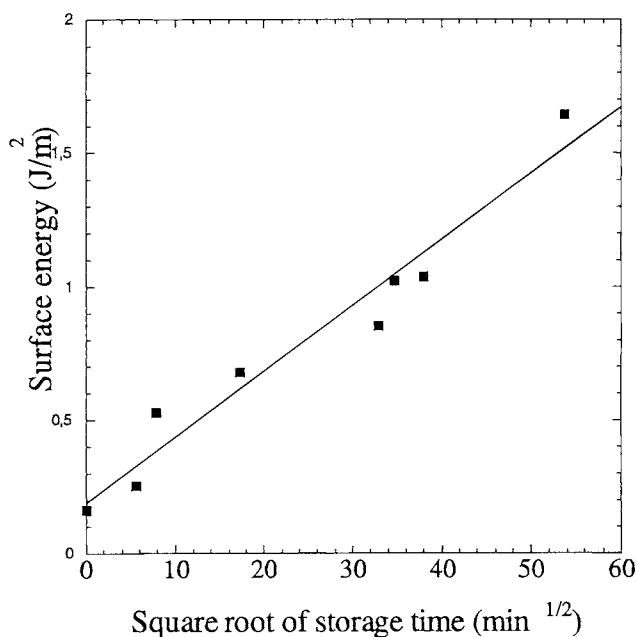
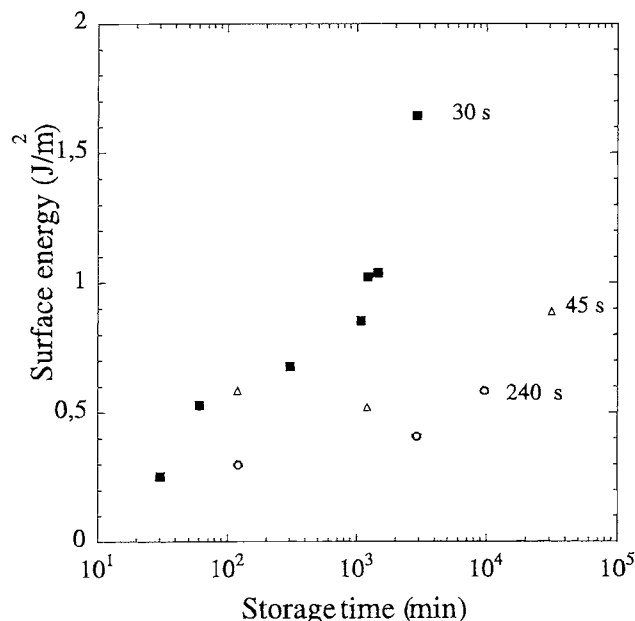
No sign of a large oxide charge was found in the oxide created by plasma. A capacitance vs. voltage curve for the silicon/plasma oxide/aluminum metal oxide semiconductor (MOS) structure is shown in Fig. 2. The flatband voltage of about  $-0.25$  V can be due to the difference in work function between the aluminum gate and the n-type silicon material. The oxide thickness of 8–10 nm obtained from the capacitance vs. voltage curve contrasts with the thickness of 5 nm obtained from ellipsometric measurements.

It was found that long plasma exposure times degrade the bonding properties. Surface energies obtained after storage of the bonded



**Figure 2.** Capacitance vs. voltage characteristic measured on a MOS capacitor made by oxygen plasma exposure of silicon for 30 s followed by aluminum evaporation. The thickness of the plasma oxide was found to be approximately 50 Å from ellipsometry.

wafers in a clean room are shown in Fig. 3a for three different plasma exposure times. Surface energies corresponding to what can be achieved by activation in SC1 followed by annealing at 600–800°C have been obtained at room temperature by using a plasma exposure time of 30 s. Using argon plasma followed by a DI water dip gave roughly the same surface energies as for oxygen-plasma-treated samples. Silicon wafers exposed to oxygen or argon plasma showed strongly hydrophilic properties when dipped in DI water. If the surface energy data of Fig. 3a corresponding to an oxygen plasma exposure of 30 s is plotted against the square root of the storage time an



**Figure 3.** (a, top) Surface energy vs. storage time at room temperature for bonded interfaces formed using oxygen plasma and DI water dip as surface preparation before bonding. The results are shown for three different oxygen plasma exposure times. (b, bottom) Surface energy vs. the square root of the storage time at room temperature for silicon wafers bonded after plasma exposure for 30 s followed by a short DI water rinse.

approximately linear relationship is found. This is demonstrated in Fig. 3b.

Oxygen plasma was successfully used also for bonding of crystalline quartz to silicon, for bonding of thermal  $\text{SiO}_2$  to silicon, and for bonding of thermal  $\text{SiO}_2$  layers. No surface energy measurement was possible on the bonded silicon/quartz sample since the bond was too strong to allow the insertion of a metal blade at the bonded interface. Figure 4 shows a 1 in. quartz wafer bonded to a 3 in. silicon wafer. A sample consisting of two bonded wafers with 600 nm oxide each was found to withstand post-processing steps like the water rinse, photoresist developer, Au/Cr etch solutions, acetone, fuming nitric acid, buffered oxide etch, and ethylenediamine-pyrocatechol-water (EPW) etch.<sup>7</sup> The bonded sample was not subject to any heat-treatment before the post-processing, but was stored for more than 24 h.

MIRS-FTIR spectra for some different bonded samples are presented in Fig. 5. For our samples four main regions are to be considered: 1000-1500  $\text{cm}^{-1}$ , 1500-1800  $\text{cm}^{-1}$ , 1800-2500  $\text{cm}^{-1}$ , and 2500-4000  $\text{cm}^{-1}$ . The region 1000-1500  $\text{cm}^{-1}$  has been attributed to Si-O stretching. For the SC1 set of samples, a weak band at 1240  $\text{cm}^{-1}$  shifts toward higher energies with increased annealing temperature, the peak position being at about 1230, 1235, 1240, and 1247  $\text{cm}^{-1}$  for specimens annealed at 120, 200, 500, and 800°C, respectively. The oxygen-plasma-treated samples with or without water rinse show no difference with regard to this band, the peak position being at about 1250  $\text{cm}^{-1}$ .

The region 1400-1800  $\text{cm}^{-1}$  has been attributed to  $\text{H}_2\text{O}$  bending. A main band around 1600  $\text{cm}^{-1}$  is observed. It is present also for the silicon bulk wafer. This band is shifted for the oxygen-plasma-treated samples, the peak being at around 1620  $\text{cm}^{-1}$ . The intensity is almost the same for samples within each set, a little higher for the oxygen-plasma-treated samples than for the SC1 ones.

The region 1800-2500  $\text{cm}^{-1}$  has been attributed to Si-H stretching. The features in this energy range are very weak and the tails of much stronger bands peaked elsewhere giving rise to a varying background-like signal. Therefore, this spectra in Fig. 5 is plotted without a reference line. The relative intensity has been left unchanged. The spectrum for silicon bulk wafer presents three main bands centered at around 1940, 2110, and 2250  $\text{cm}^{-1}$ . For the oxygen-plasma-treated samples two more bands are present, a sharp peak at 2350  $\text{cm}^{-1}$  and a broad bump centered at around 1800  $\text{cm}^{-1}$ . These two samples present most of their differences in this region.

The region 2500-4000  $\text{cm}^{-1}$  has been attributed to C-H and O-H stretching. In this region the spectra present one very broad band peaked around 3370  $\text{cm}^{-1}$ . The broad band is much stronger for the oxygen-plasma-treated samples, the peaks are at about 3270  $\text{cm}^{-1}$  and have some quite clear structures. In the SC1 set the band is fea-

tureless, the shape being similar to that for silicon bulk wafer. It shows a marked decrease in intensity with increasing annealing temperature.

Silicon/silicon structures bonded at room temperature using oxygen plasma activation were characterized electrically. Since exposure to oxygen plasma results in an oxide layer on the silicon surfaces one should expect the current to be restricted by the bonded interface. Indeed this was also found from the current vs. voltage measurements as is shown in Fig. 6. The sample area was 25  $\text{mm}^2$ . The slope of the curve in Fig. 6 corresponds to a large signal resistance of about 4 k $\Omega$ . This should be compared to be series resistance due to the silicon itself, which can be estimated to be of the order of a few ohms. Capacitance vs. voltage measurements of samples made simultaneously with the sample of Fig. 6 are shown in Fig. 7. The peak of the capacitance curve demonstrates the presence of space-charge regions surrounding the bonded interface. The capacitance measurement shown in Fig. 7 was performed using a test signal frequency of 100 kHz.

To further investigate the electrical properties of the bonded interfaces, spreading resistance measurements were made on bonded samples prepared using oxygen plasma and room temperature bonding. Figure 8 shows the peak in the spreading resistance when the probes passed the bonded interface. The peak shown in Fig. 8 is attributed to a space-charge region at the interface.

Wafer bonding has earlier been shown to encapsulate impurities that are present on the wafer surfaces before bonding.<sup>8-11</sup> To investigate the encapsulated impurities after oxygen plasma treatment, secondary ion mass spectroscopy (SIMS) analysis was made on a bond-

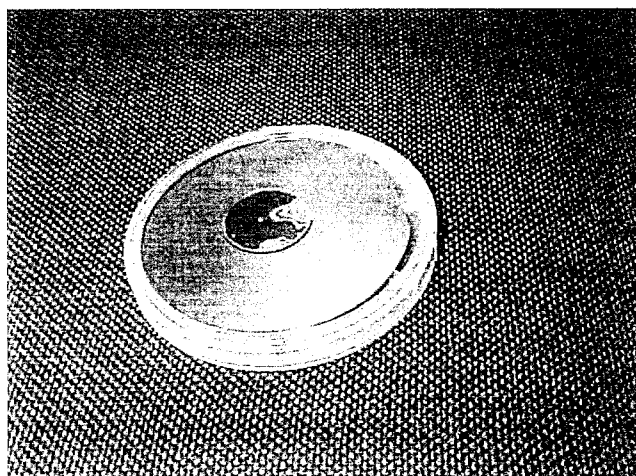


Figure 4. Crystalline quartz wafer bonded to silicon wafer after exposure to oxygen plasma.

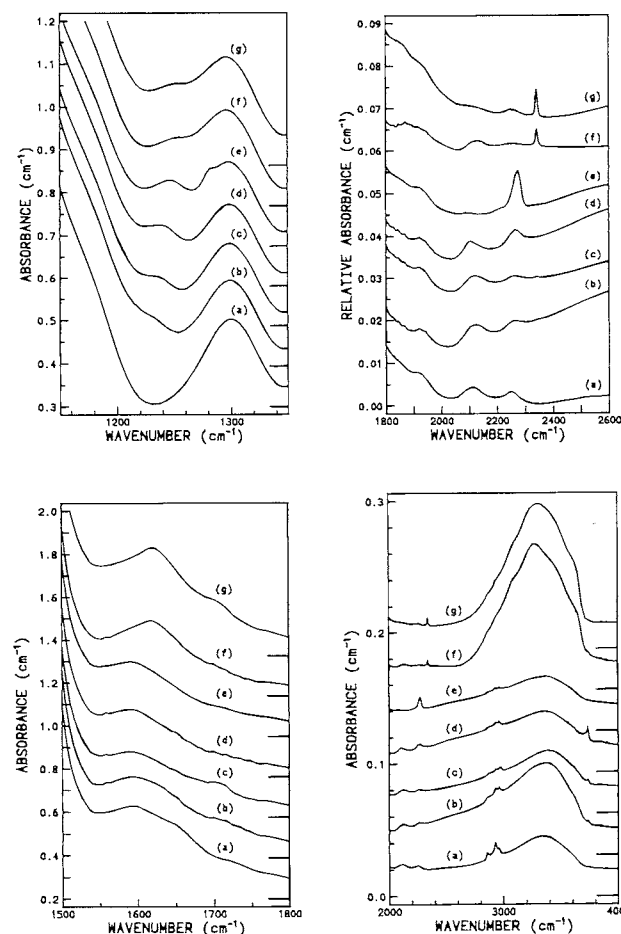
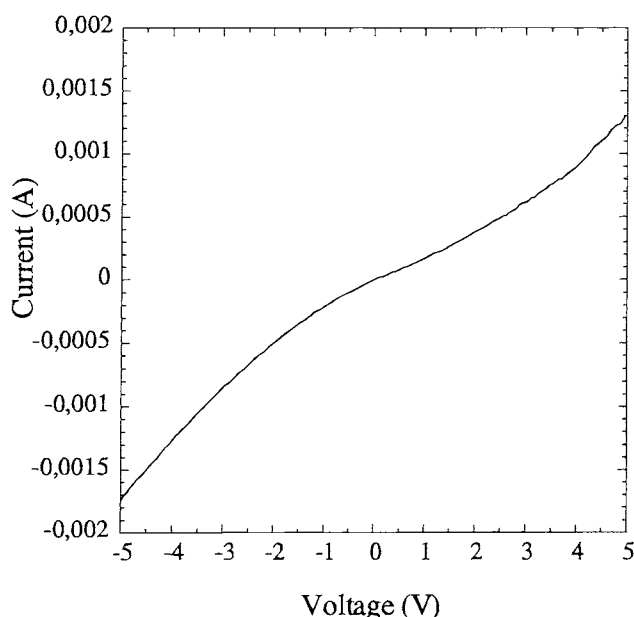


Figure 5. MIRS spectra for (a) silicon bulk wafer, (b) SC1 (120°C), (c) SC1 (200°C), (d) SC1 (500°C), (e) SC1 (800°C), (f) oxygen plasma, and (g) oxygen plasma and water rinsed samples. The values on the intensity axis are to be referred to the reference line on the right for each spectrum. For the measurements to the upper right the values on the intensity axis are on a relative scale.

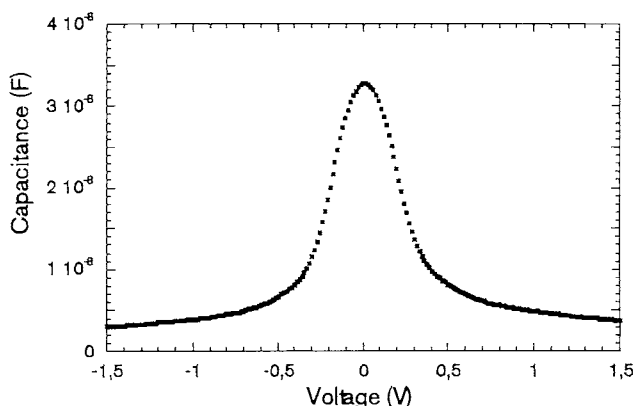


**Figure 6.** Current vs. voltage characteristic for a silicon/silicon structure formed by wafer bonding at room temperature following oxygen plasma exposure and DI water dip.

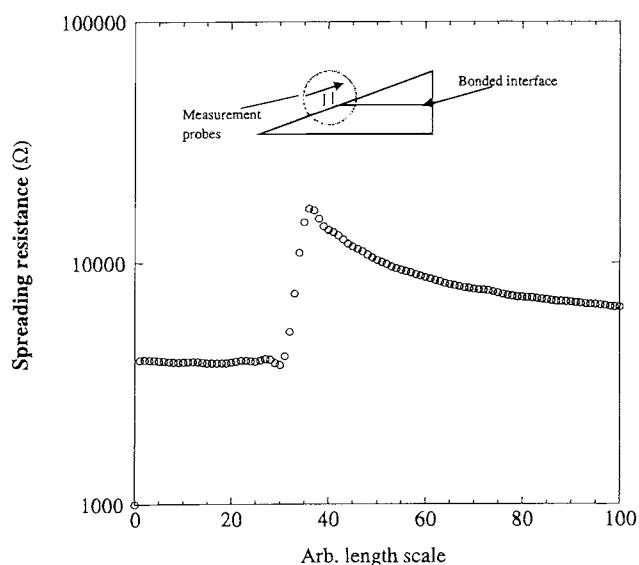
ed silicon/silicon sample. In Fig. 9a and b traces across the bonded interface of some impurities are shown. Using  $\text{Cs}^+$ , primary ions, increased concentrations of hydrogen, carbon, oxygen, and fluorine were found as compared to bulk silicon. Using  $\text{O}_2^+$ , primary ions, peaks of boron, carbon, calcium, and aluminum were found at the bonded interface. The found impurities, C and F, are residues from the etching and passivation sequences run in the plasma system. The increase in oxygen concentration at the interface is expected since the wafers were covered with a thin oxide film formed during the plasma exposure. The peak of H, is attributed to H passivation of dangling bonds, pointing at the presence of a defective region at the bonded interface. Two of the found impurities, B and Ca, are common contaminants in clean room and vacuum environments. The distinct aluminum peak occurs because of the aluminum containing ceramics used in the interior of the plasma system.

#### Discussion

No satisfactory explanation of the influence of the plasma activation on the bonding properties has yet been proposed, but the importance of rapid removal of interfacial water after plasma exposure for

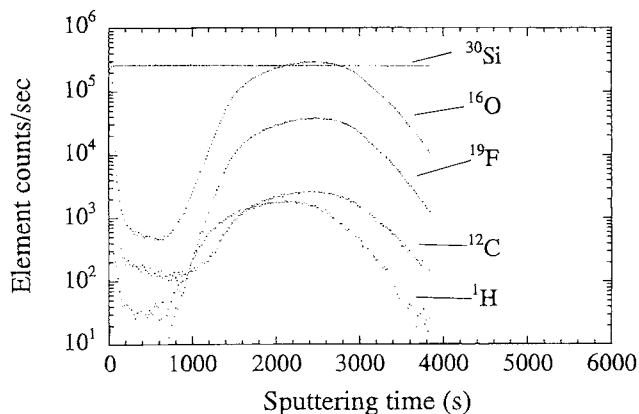
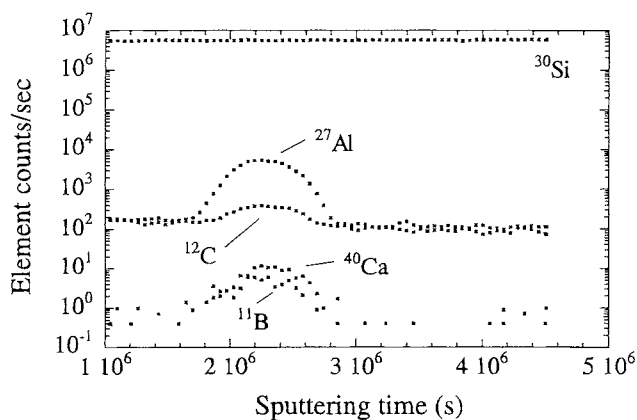


**Figure 7.** Capacitance vs. voltage characteristic for a silicon/silicon structure formed by wafer bonding at room temperature following oxygen plasma exposure and DI water dip.



**Figure 8.** Spreading resistance across a bonded interface formed after oxygen plasma exposure and room temperature bonding. The inset of the figure shows the measurement geometry. The measurements were made by stepping the probes across the interfacial region on a sample which had been lapped to an angle of approximately  $11^\circ$ .

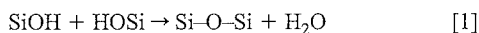
stronger bonds to be formed has been pointed out.<sup>1,4</sup> When bonding is achieved using wet chemical activation, the water removal takes



**Figure 9.** SIMS result where (a, top)  $\text{Cs}^+$  ions are used for detecting concentrations of impurities and (b, bottom)  $\text{O}_2^+$  ions are used for detecting concentrations of impurities in plasma bonded sample.

place during the annealing step subsequent to wafer contacting.<sup>12</sup> Plasma exposure may affect a silicon surface in different ways. chemical reactions may take place, charges may be injected into the oxide or the semiconductor, and the plasma bombardment may cause structural changes. It is obvious that the oxygen plasma gives rise to chemical reactions at the silicon surface since it is oxidized. However, since the use of argon plasma also results in formation of bonded interfaces with high surface energies, the chemical reaction (oxidation) does not seem to be the crucial step. Furthermore, we did not find any direct evidence for a large charge content in the formed plasma oxide after oxygen plasma exposure (Fig. 2). It has been speculated that an increased oxidation rate driven by a strong electric field could be responsible for the water removal.<sup>1,4</sup> We do not find any evidence in our experiments for this speculation. From the discussion above the most important effect of the plasma exposure seems to be the formation of a disordered surface structure.

When the wafers are brought into contact after plasma immersion and DI water dip, they bond to each other with hydrogen bonds between the adsorbed water and hydroxyl groups. Immediately after bonding the surface energy of oxygen-plasma-treated samples dipped in water is about the same as the surface energy expected for SC1 bonded samples (see Fig. 3b). When the bonded sample is stored at room temperature the surface energy increases due to the formation of Si–O–Si bonds according to the reaction



Hence the increase in surface energy is a result of water transport away from the interface. As shown in Fig. 3b, the surface energy increases roughly with the square root of storage time at room temperature. This dynamic shows similarities to the growth of oxides in the parabolic diffusion-limited regime.<sup>13</sup> This result supports the hypothesis that the increase in surface energy upon storage is controlled by the diffusion of water away from the interface. If non-negligible amounts of water diffuse from the interface over short periods of time at room temperature, the diffusion of water must be very much enhanced compared to diffusion of water in silicon dioxide. It is not possible to find the reason for the enhanced water diffusion entirely based on the presented results, but one can speculate that enhanced diffusion will occur in a porous structure.

The broad band at about  $3400 \text{ cm}^{-1}$  is associated with the symmetric stretching mode of water and at about  $1600 \text{ cm}^{-1}$  to its bending mode.<sup>14</sup> These bonds can shift significantly, depending on the interaction of the molecule via hydrogen bonds with its surrounding.<sup>15</sup> Based on the spectra concerning these regions, the oxygen-plasma-treated samples present stronger hydrogen bond interactions than do the SC1 set. Not only is the amount of water in the oxygen-plasma-treated samples greater, as the measured intensity of the bending mode testifies, but the overall amount of hydroxyl groups is also. The structures of the broad band around  $3400 \text{ cm}^{-1}$  for these samples are to be associated to hydrogen-bonded silanols and water molecules either connected to the crystalline silicon or to the glassy silica layer. In contrast, very small amounts of silanols are present in the SC1 set. Although huge amounts of water are indicated by MIRS measurements, this water is likely to be trapped in the claimed porous system.

Results of MIRS measurements, in the region of lower wavenumbers, also support the hypothesis of a porous surface structure. The spectral features present at about  $2110$ ,  $2260$ ,  $2350 \text{ cm}^{-1}$  are associated with stretching modes for hydride groups of the type  $\text{Si-H}$ .<sup>16-18</sup> In this case the role of hydrogen bonds is important, but an additional consideration is related to the high mobility of hydrogen in silicon. Freely oscillating hydride groups are supposed to be present at the surface of pores inside the oxygen-plasma-treated samples. They are associated with the sharp peak found at  $2350 \text{ cm}^{-1}$ .<sup>16</sup> It should be mentioned that peaks at  $2350 \text{ cm}^{-1}$  may also be due to  $\text{CO}_2$ . The band at  $2110 \text{ cm}^{-1}$  is associated with hydrogen-bonded hydride groups connected to silicon and the band at  $2260 \text{ cm}^{-1}$  can be associated with hydrogen-bonded hydride

groups connected to silica.<sup>16-18</sup> In the spectra, evidence of hydrogen-bonded hydride groups can be found for the SC1 set of samples but is almost missing in the plasma-treated samples. An explanation for the latter can be that possibly water oxidizes the walls in the cave, and this reaction would instead lead to the production of a wall terminated by silanols. Hence, the measurements show silanol groups rather than hydrogen-bonded hydrides.

Another reason to believe that the surface of plasma-exposed samples is porous is the observed discrepancy between the different methods for determining the oxide thickness. From ellipsometric measurements the thickness of the oxide formed was found to be  $5 \text{ nm}$ , while the capacitance vs. voltage measurement revealed a thicker oxide of  $8\text{--}10 \text{ nm}$ .

MIRS results agree with the formation of Si–O–Si bonds. The IR band at about  $1240 \text{ cm}^{-1}$  may be related to a silicon oxide structure that forms at the interface.<sup>19</sup> The increase of the energy of this mode with annealing temperature agrees with previous results on, for example, silica glass prepared by sol-gel route.<sup>20</sup> It has been suggested that a shift of this mode toward higher energies is associated with changes in the Si–O–Si bond lengths and angle. It seems likely that the shifting in the samples is due to the evolution of the silica layer at the bonding interface.<sup>21</sup> Hence, the progress toward a stronger network with increased annealing temperature or oxygen plasma treatment is in agreement with the high surface energy achieved.

AFM measurements were not possible after plasma exposure, a rinse in water, and drying, since the probe of the instrument was incompatible with the surface for making a proper characterization. The surface can be described as a thin layer of silicon material which sticks to the AFM probe. However, it was observed that the thin layer of material, perhaps superfine grained silica, forms small aggregates after some storage time. After  $2 \text{ h}$  of storage there were holes in the thin layer of silica and after an additional  $10 \text{ h}$ , the surface beneath the silica was almost revealed except for some places where there were aggregates of silica. Such wafers that had been stored for  $4 \text{ h}$  were not possible to bond.

The double-barrier model earlier proposed for the bonded interfaces can explain the electrical properties of the results obtained from electrical characterization of the bonded silicon/silicon junctions.<sup>22</sup> Surface states in the disordered interface give rise to depletion regions surrounding the interface. The energy band diagram of the structure is shown in Fig. 10. A negative interfacial charge gives rise to depletion regions surrounding the bonded interface. The energy barrier at the bonded interface restricts the majority carrier current in the conduction band of the semiconductor. Using a simple theory of the bonded structure the capacitance vs. voltage curve gives an approximate energy barrier height of  $0.2 \text{ eV}$ .<sup>22</sup> The electrical properties of the room-temperature-bonded structures show similarities to structures bonded after hydrophilic surface preparation followed by high-temperature annealing. The energy barrier height of  $0.2 \text{ eV}$  is somewhat lower than what is most often found after

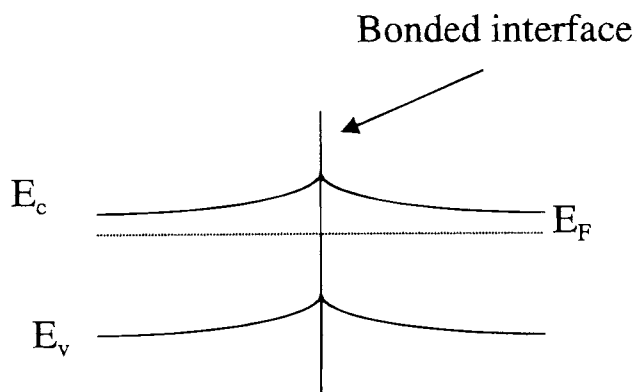


Figure 10. Energy band diagram of a bonded silicon/silicon structure.

bonding using hydrophilic surfaces.<sup>22</sup> On the other hand, the energy barrier is still considerably larger than that obtained when bonding hydrophobic surfaces. Also, although an at least 5 nm thick oxide was found from ellipsometry after plasma exposure, the current seems not to be limited by an oxide layer at the surface. This again indicates a disordered nature of the interfacial oxide layer.

The spreading resistance peak shows the presence of a space-charge region surrounding the bonded interface. However, the band bending which can be related to this peak is considerably smaller than what can be derived from the capacitance vs. voltage curve. The reason for this is not understood, but may be related to inhomogeneities at the bonded interface.

The SIMS analysis showed that plasma-bonded interfaces exhibit increased concentrations of various impurities as compared to bulk silicon. No fundamental differences exist between the impurity profile found for these interfaces prepared by plasma exposure and bonding and earlier studied interfaces prepared using wet chemical activation of the surfaces followed by wafer bonding<sup>8-10</sup> or samples prepared by ultrahigh vacuum (UHV) bonding.<sup>11</sup> However, we believe that the peaks of C and F are related to the gases used for reactive ion etching in the system we used for oxygen plasma exposure. The aluminum peak also seems to be related to the particular piece of equipment used. The oxygen peak indicates an oxide in the interface and the hydrogen peak indicates the hydride groups, water, and hydroxyl groups, which were detected by MIRS in the porous structure of the interface.

### Conclusion

Oxygen plasma activation of silicon, silicon dioxide, and crystalline quartz surfaces has been used to form bonded structures at room temperature. Also, argon plasma activation of silicon surfaces has been used to form bonded structures. The bonded structures, oxygen-plasma-activated as well as argon-plasma-activated, exhibit very large surface energies. It seems that the most important effect of the plasma exposure is the formation of a disordered surface structure. The mechanism behind the high mechanical stability at room temperature for oxygen-plasma-bonded samples is explained by an increased dynamics in water removal from the bonded interface allowing covalent bonds to be formed. Although huge amounts of water in the oxygen-plasma-treated samples were indicated by MIRS measurements, the water is likely trapped in a porous system. A discrepancy in the characterization of the oxide thickness supports a speculated porous system. MIRS measurements indicate the formation of a silica layer at the bonding interface of oxygen-plasma-treated samples comparable to that obtained for SC1 bonded sam-

ples annealed at about 1000°C. Electrical characterization of bonded structures shows properties similar to those obtained using conventional wet chemical activation and high temperature annealing.

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## Formation of Silicon Structures by Plasma-Activated Wafer Bonding

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### Abstract

A room temperature wafer bonding process based on oxygen plasma treatment or argon plasma treatment has been studied for surfaces of silicon, silicon dioxide, and crystalline quartz. The surface energy of the bonded samples was observed at different storage times. Atomic force microscope measurements, multiple internal reflection infrared spectroscopy, electrical characterization, secondary ion mass spectroscopy, and post-processing steps were performed to evaluate the plasma-treated surfaces and the formed bonded interfaces. Electrical measurements were used to investigate the usefulness of plasma-bonded interfaces for electronic devices. The bonded interfaces exhibit high surface energies, comparable to what can be achieved with annealing steps in the range of 600–800°C using normal wet chemical activation before bonding. The high mechanical stability obtained after bonding at room temperature is explained

by an increased dynamic in water removal from the bonded interface allowing covalent bonds to be formed. © 2000 The Electrochemical Society. All rights reserved.

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## May be of interest

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Mechanisms for Room-Temperature Fluorine Containing Plasma Activated Bonding

Chenxi Wang et al., *IEEE Journal of Solid State Circuits and Technology*

The Role of Mobile Charge in Oxygen Plasma-Enhanced Silicon-to-Silicon Wafer Bonding

B. Tzeng et al., *Fluorine-Activated and Fluorinated Polymers*

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## Modification of Silicon Surfaces with $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:HF}$ and $\text{HNO}_3\text{:HF}$ for Wafer Bonding Applications

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## ABSTRACT

Two combinations of oxidizing and etching agents,  $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:HF}$  and  $\text{HNO}_3\text{:HF}$ , have been used to modify silicon surfaces prior to wafer bonding. The chemical oxide thickness can be adjusted between 0 and 10 Å by tuning the HF content of the mixtures. Using x-ray photoelectron spectroscopy it was found that the chemical composition of the surfaces can also be affected. Hydroxyl groups, fluorine, and hydrogen are terminating species that can be obtained by the described procedures. Both the described cleaning procedures permit hydrophilic bonding, giving a high room temperature bond strength with a minimum of interfacial oxide. The bond between a mainly fluorine-terminated or a mainly OH terminated surface and a hydrogen-terminated surface is no stronger than the bond between two hydrogen-terminated surfaces.

## Introduction

Despite the fact that direct bonding of silicon wafers is now quite commonly used in microelectronics and for micromechanical applications, opinions are still divided about how different parameters influence the bonding behavior.<sup>1-3</sup> Known important properties are roughness and waviness of the surface and particle density. In addition, control of the surface chemistry is desirable. In this work we have investigated the chemistry of silicon surfaces treated in two different cleaning mixtures and studied their bonding behavior.

A strong room temperature attraction between the wafers is desirable to make handling, e.g., polishing and cleaning, of the bonded wafers easier. A high bond strength also increases the probability of closure of the gap between wafers that are rough on a microscopic scale. For electronic applications it is not only important to control the bonding behavior in terms of bond strength and void generation, but also to minimize the influence of the bonded interface on the electrical performance. Hence, it is important to control the interfacial oxide, which leads to the choice of hydrophobic bonding,<sup>4</sup> using an HF-last process as surface preparation. On the other hand, the bond strength at room temperature is considerably larger (up to about three times larger) for hydrophilic than for hydrophobic wafers.<sup>5,6</sup> This is due to the hydroxyl (OH) termination of the surface of the thin oxide present on hydrophilic wafers. A good starting material would thus

be an oxide-free silicon surface terminated by hydroxyl groups to achieve hydrophilic bonding with a minimum of interfacial oxide.

Different combinations of oxidizing and oxide-etching agents are widely used in semiconductor wafer cleaning technology. One of the most well known is the RCA1 (or SC1 or APM) mixture, i.e.,  $\text{NH}_4\text{OH:H}_2\text{O}_2\text{:H}_2\text{O}$ .<sup>7</sup> Oxidizing/etching mixtures are very well suited to particle removal thanks to continuous oxidation and etching of the silicon substrate under the particles. Moreover, using an oxidizing cleaning mixture in combination with an oxide etchant could make careful control of the surface oxide possible. In principle, it would make it possible to tune the thickness of the interfacial oxide very carefully by varying the mixing ratios.

The so-called SPM cleaning (sulfuric peroxide mixture, i.e., a mixture of  $\text{H}_2\text{SO}_4$  and  $\text{H}_2\text{O}_2$ ) is known to produce a chemical oxide of good quality in terms of large thickness<sup>8,9</sup> and a low etching rate in HF solutions.<sup>10</sup> It has also been shown to be effective for passivation and protection of the Si surface prior to gate oxidation.<sup>10</sup> However, due to the high viscosity of the sulfuric acid, SPM is difficult to rinse.<sup>11, 12</sup> Recently it was demonstrated that a small amount of HF in the SPM solution results in higher rinsing efficiency.<sup>11</sup> This mixture is referred to as SPFM (sulfuric peroxide hydrofluoric mixture). The suggested explanation of the higher rinsing efficiency is that the SPFM cleaning causes fluorine-passivation of the silicon surface, turning it hydrophobic. However, rinsing the surface in water gives the surface hydrophilic properties.<sup>11</sup> This is probably due to

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substitution of fluorine by OH-groups, which has been observed by several researchers.<sup>13-15</sup> The HF-modified SPM solution acts as an oxidizing/etching mixture on silicon, which potentially could be used for control of the thickness of the chemical oxide. Furthermore, by adding HF to the standard SPM solution, the concentration of sulfur on the wafer surface is considerably reduced.<sup>11</sup> This is of importance for wafer bonding applications since contaminants are encapsulated into the structure by the wafer contacting.

Another oxidizing/etching mixture suggested for cleaning is  $\text{HNO}_3:\text{HF}$  in which the HF concentration is kept very low. This etch is referred to as SE, slight etch, as in Ref. 16. Nitric acid is a strong oxidizer, known to produce thick chemical oxides. Addition of HF results in simultaneous oxide etching. The SE cleaning always gives a thin chemical oxide on the surface, since the etch reaction of the oxide is the etch rate-determining step.<sup>16, 17</sup> This means that the etch rate is highly dependent on HF concentration.<sup>17</sup> Thus, as with the SPFM cleaning solution, the HF concentration in the SE mixture should be tunable to control the thickness of the chemical oxide. Thicknesses of chemical oxides produced in SPM and nitric acid ( $\text{HNO}_3$ ) can be found in the literature.<sup>18, 19</sup> The absolute values differ due to different measurement methods or data interpretation. Important is that  $\text{HNO}_3$  is known to give a thick oxide as compared to, e.g.,  $\text{NH}_4\text{OH}:\text{H}_2\text{O}:\text{H}_2\text{O}_2$ , while SPM gives a thinner oxide.

The aim of this study is to investigate the influence of surface termination on the bondability of silicon surfaces and to evaluate the use of oxidizing/etching mixtures for manufacturing controlled chemical oxides for wafer bonding purposes. From the discussed observations, we suggest that a combination of an oxidizing solution and an etching agent, HF, can also be used to prepare Si surfaces with a controlled surface chemical composition. This makes it possible to investigate the influence of different species on the bonding properties. In addition, these mixtures also make it potentially possible to control the thickness of the thin chemical oxide, which may be useful in advanced device applications. In the present work, surface analysis with XPS (x-ray photoelectron spectroscopy) has been used to investigate how varying amounts of HF in an SPFM or an SE mixture can be used to modify Si surfaces. The bonding behavior of the surfaces is observed by inspection in transmitted IR to study the speed of the contact wave and by measurement of bond strengths. The influence of surface conditions on bonding properties is discussed.

## Experimental

In the experiments mainly 3 in. Si wafers (Wacker, p(100) FZ, 1 to 10  $\Omega$  cm) were used. For some experiments with differently terminated surfaces, 2 in. wafers were used. Prior to cleaning in SPFM or SE some wafers were dipped for 1 min in dilute HF to remove the native oxide, while others were used as-received. Preparation of the wafers in the SPFM and SE solutions was according to one of the following methods: (i) 2 min in SPFM, i.e.,  $\text{H}_2\text{SO}_4(97\%):\text{H}_2\text{O}_2(30\%)$ , 1:4, with a small amount of HF added. The temperature was about 120°C due to the reaction heat. (ii) 5 min in SE, i.e., hot (80°C)  $\text{HNO}_3(70\%)$  with HF added.

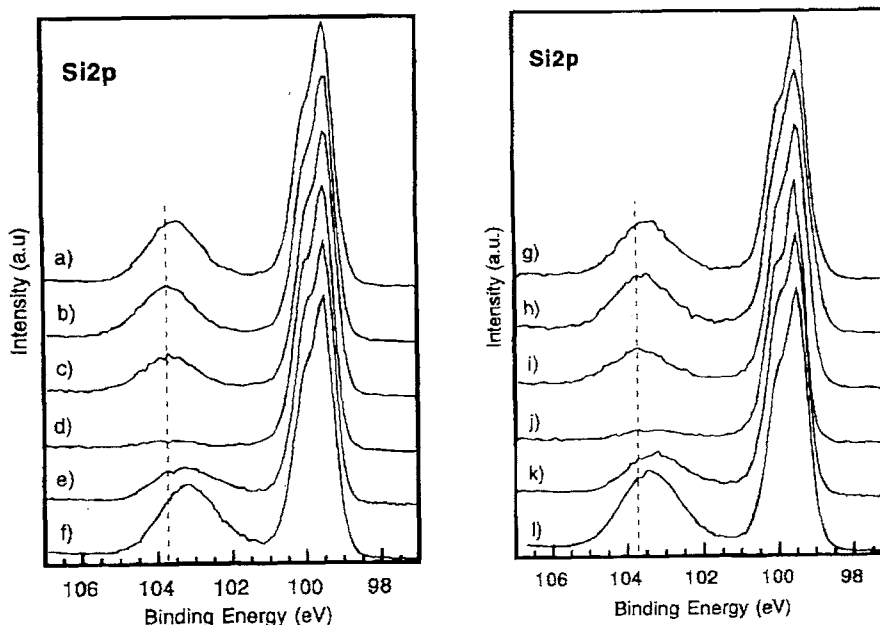
The HF concentrations ranged from 10 to 1000 ppm. Higher HF concentrations gave nonbondable surfaces. Subsequential rinsing was performed in DI water (18 M  $\Omega$  cm), after which the wafers were blow-dried in  $\text{N}_2$ . After room temperature bonding some samples were annealed in  $\text{N}_2$  ambient for 1 h.

## Characterization of Silicon Surfaces

The silicon surfaces were analyzed with XPS using monochromatic Al  $K_{\alpha}$  radiation. Charging was corrected for using an arbitrary value of 284.8 eV for the C 1s peak of adsorbed hydrocarbons. The hydrophilicity of the surfaces was determined by measuring the contact angle to water in a standard contact angle microscope. Atomic force microscopy (AFM) was used to analyze the surface roughness. The data was recorded in air. The scanned area was  $0.2 \times 0.2 \mu\text{m}$  which was analyzed as a  $256 \times 256$  matrix.

**Oxide formation.**—The XPS results clearly show that the oxide thickness can be controlled by cleaning the wafer in an oxidizing/etching mixture. The oxide thickness after cleaning depends on several parameters, including choice of acid, HF concentration, and rinse time. This can be seen in Fig. 1 which shows the Si 2p peaks from silicon surfaces cleaned in SPFM or SE. The spectra show two features at about 99.7 and 103.4 eV which can be attributed to elemental silicon and silicon in  $\text{SiO}_2$ , respectively. The thickness of the oxide cleaned in pure SPM without HF, spectrum 1a, can be estimated as about 10 Å by measuring the intensity of the Si 2p peak and using the procedure described by Namiki *et al.*<sup>20</sup> The intensity,  $I$ , follows an exponential law according to

Fig. 1. Si 2p spectra from Si (100) surfaces after cleaning. To the left are shown spectra obtained immediately after treatment in: (a) SPM (no HF), (b) SPFM (10 ppm HF), (c) SPFM (100 ppm HF), (d) SPFM (1000 ppm HF), (e) HF dip + SPM, and (f) HF dip +  $\text{HNO}_3$ . The right side shows spectra obtained from the surfaces after 2 min subsequent  $\text{H}_2\text{O}$  rinse: (g) SPM (no HF), (h) SPFM (10 ppm HF), (i) SPFM (100 ppm HF), (j) SPFM (1000 ppm HF), (k) HF dip + SPM, and (l)  $\text{HNO}_3$ . The dashed line marks 103.7 eV.



$$I = I_0 \left( 1 - e^{-\frac{d_{ox}}{\lambda \sin \theta}} \right) \quad [1]$$

where  $I_0$  is the intensity of the Si 2p peak when no oxide is present on the surface,  $\theta$  is the take-off angle of the emitted electrons, and  $\lambda$  is the mean free path for the Si 2p electron in the  $\text{SiO}_2$  film ( $\lambda = 30 \text{ \AA}$ ). From this the oxide thickness,  $d_{ox}$ , can be derived. As can be seen in Fig. 1, comparison of the relative heights of the peaks from elemental silicon and from silicon in  $\text{SiO}_2$  shows that the addition of HF to the SPM mixture reduces the oxide thickness. In fact, 1000 ppm HF yields an essentially oxide-free surface, illustrated by spectrum 1d. An interesting observation is that the oxide peak at about 103.4 eV (spectrum 1a) is slightly shifted toward higher binding energies when HF is added to the solution, as in spectra 1b-d. This shift is caused by the presence of Si-F bonds in the oxide. It is likely that most of the fluorine originates from adsorbed atoms terminating the surface. However, some fluorine is probably also embedded in the oxide. A subsequent water rinse shifts the oxide peak back to normal binding energies due to the removal of Si-F bonds and the formation of Si-O bonds, as illustrated in spectra 1h-i.

The final oxide thickness is also dependent on the surface condition prior to cleaning. Spectra 1 a-d were obtained from samples which were not HF-etched prior to cleaning in the SPM mixture. This means that they were initially covered by a thin native oxide about 10 to 15 Å thick. In contrast, SPM cleaning of initially oxide-free surfaces (obtained by HF-etching prior to the cleaning step) yielded considerably thinner oxides for a given HF concentration (cf. spectra 1a and e). The oxides produced in a SE mixture exhibit the same behavior as those obtained in a SPM mixture. In general, the SE solution produced thicker oxides (cf. spectra 1e and f). An interesting observation is that the binding energy of the oxide peak of the fluorine-free surface is dependent on the cleaning solution. This was also observed for oxides with identical thicknesses and can probably be attributed to structural differences between the oxides, giving rise to a structure-induced shift, as discussed by Grunthaner *et al.*<sup>21</sup>

It should also be noted that carbon was observed in all XPS spectra obtained from SPM and SE-cleaned surfaces. The carbon peak can be assigned to contaminants adsorbed on the surfaces during transport in air to the analysis chamber. In addition, a clear sulfur (S 2p) peak

was observed in spectra from SPM-cleaned surfaces. This peak is due to adsorption of residual species on the surface during cleaning. A rough quantitative analysis, based on elemental standards, shows that the sulfur amount is about 1 to 2 atom percent (a/o). No reduction in sulfur content was observed after water rinse. This shows that some sulfur is still present on the surfaces in spite of the hydrophobic silicon surface lowering the carry-over of etch solutions to the rinse bath. Nitrogen, which may have been present on the SE-cleaned surfaces, was not observed.

The results above show that cleaning in SPM and SE solutions can be used to prepare silicon oxides with thicknesses ranging from essentially zero to about 10 Å. This behavior can be explained by the chemical properties of the mixtures. Pure  $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ , as well as hot  $\text{HNO}_3$ , forms oxides on silicon, while HF etches  $\text{SiO}_2$ . It is likely to assume that a competition between oxidation and etching takes place in the solutions when HF is added. The final thickness of the oxide is then determined by a "steady-state" value determined by the HF concentration.

**Surface termination.**—The XPS results also showed that the termination of the silicon surface could be modified by the cleaning procedure. It was found that SPM- and SE-cleaned surfaces contained large amounts of adsorbed fluorine (Fig. 2, spectra 2a-c). From this it can be concluded that the cleaning procedures give oxidized silicon with a mainly fluorine-terminated surface. The results also showed that essentially oxide-free silicon surfaces with high concentrations of adsorbed fluorine could be obtained with 1000 ppm HF in the cleaning solution (spectrum 2c). The XPS analysis of this surface showed a clear O 1s peak, suggesting a partial termination by, *e.g.*, OH groups. However, contact angle measurements showed that all SPM and SE-treated surfaces were hydrophobic with contact angles ranging from 40 to 50°. These large contact angles show that the concentration of OH groups must be relatively low and that the surfaces should instead be mostly terminated with fluorine. An interesting observation is that the fluorine content decreased slightly for HF concentrations above 100 ppm. This is probably due to increasing hydrogen termination of the surface. This is supported by the fact that HF concentrations above 100 ppm yielded even more hydrophobic surfaces with contact angles of about 50-55°.

Rinsing in DI water for 2 min strongly reduced the intensity of the F 1s peaks (spectra 2d-f), again supporting

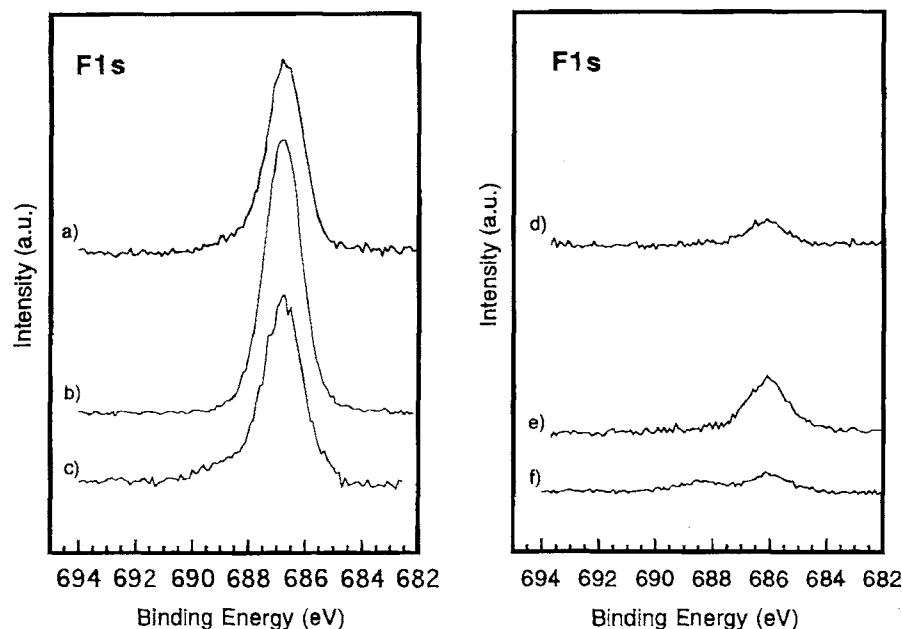


Fig. 2. F 1s spectra obtained from Si (100) surfaces prior to water rinse: (a) SPM (10 ppm HF), (b) SPM (100 ppm HF), and (c) SPM (1000 ppm HF); and after a 2 min rise in  $\text{H}_2\text{O}$ : (d) SPM (10 ppm HF), (e) SPM (100 ppm HF), and (f) SPM (1000 ppm HF).

the conclusion that most of the fluorine is present at the surface. No fluorine could be detected by XPS analysis after a rinsing time of 15 min. It is generally accepted that this is due to a substitution of fluorine atoms by OH groups producing an OH-terminated surface.<sup>13-15</sup> The assumption that such a substitution takes place is supported by the observation that the surfaces became hydrophilic with a contact angle reduced to less than 5° after the water rinse. An interesting observation was that the "oxide-free" silicon surface, obtained with 1000 ppm HF in the cleaning solution, was quite hydrophobic also after the water rinse (contact angle 30°). This is explained by the high degree of hydrogen-termination of the oxide-free surface.

The XPS results show that SPFM and SE cleaning can be used to prepare oxide-free as well as oxidized silicon surfaces with controllable oxide thickness and different surface terminations. In addition, a conventional HF dip can be used to obtain completely oxide-free hydrogen-terminated surfaces. The different types of surfaces are summarized in Table I.

**Surface roughness.**—SPFM with 1000 ppm HF dissolved about 100 Å Si/min during 10 min etching, which is at least 20 times more than SPFM with 10 ppm HF. This was measured by weighing the samples before and after etching using a balance gravimeter capable of measuring changes of mass down to 10 µg. This indicates a strongly increasing etch rate with HF concentration in SPFM.

AFM showed no large increase in the microscopic roughness with HF concentration. The wafers were dipped in diluted HF and rinsed in water before cleaning in the different SPFM solutions. The AFM analysis was made after subsequent water rinsing for 4 min. The calculated rms roughness values are 0.62 Å for SPFM with 10 ppm HF, 0.80 Å for SPFM with 100 ppm HF, and 0.58 Å for SPFM with 1000 ppm HF. An as-received silicon (100) surface has an rms roughness of 0.3 to 0.4 Å.

These results show that although the etch rate is considerably higher in SPFM with relatively high HF contents, i.e., 1000 ppm, the surface microroughness seems not to increase significantly as judged from the rms value.

### Bonding Results and Discussion

Wafer bonding was done immediately after each treatment and the bonding process was recorded in transmitted infrared light using a video setup. Thus the velocity of the contact wave, i.e., the growing bonded area, could be measured. This method has been presented elsewhere.<sup>22</sup> The bond strengths, i.e., surface energies, were measured using the crack opening method introduced by Maszara *et al.*<sup>23</sup> The surface energy,  $\gamma$ , of the bond is calculated using Young's modulus,  $1.66 \cdot 10^{11}$  Pa, the wafer thickness 381 µm, and the blade thickness 50 µm.

**Direct bonding.**—In Fig. 3 contact wave velocities and room temperature surface energies vs. HF content in SPFM are given. It can be seen that 100 ppm of HF gives a significantly higher wave velocity than 10 ppm, while a

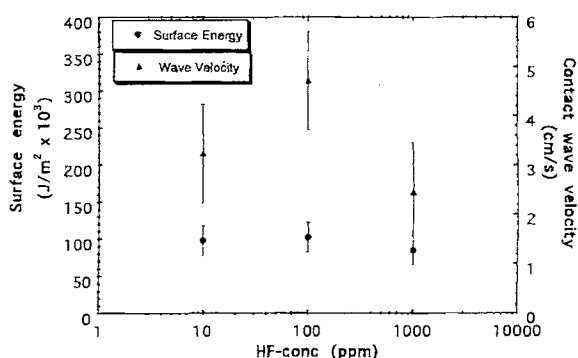


Fig. 3. Mean values of measured contact wave velocities and room temperature bond strengths of Si (100) surfaces vs. the HF concentration in SPFM.

mixture with 1000 ppm HF gives velocities comparable to the 10 ppm case. The higher velocities measured for the 100 ppm samples correlate to the higher F content on this surface, giving a high OH concentration after rinsing. No large differences in bond strength were observed between the samples, as is evident from Fig. 3. This is in agreement with the fact that all these surfaces are mainly OH terminated. The surface produced with 1000 ppm HF is partly terminated with H as previously described. It is known that HF-etched, hydrogen-terminated, silicon surfaces show a lower contact wave velocity and bond strength than hydrophilic ones.<sup>1,22</sup> The decrease in contact wave velocity for the highest HF concentration in Fig. 3 can be explained by this. It might be suspected that the higher etch rate in the solution containing 1000 ppm HF would cause a larger surface roughness leading to a slower contact wave. However, as the AFM results showed, the microscopic roughness did not increase with increased HF concentration. Hence the increasing hydrophobicity of the surface seems to be the most probable reason for the observed bonding behavior.

No significant differences in bonding behavior were seen between samples that were HF dipped prior to cleaning and those which were not. Even if the resulting oxide became thinner when the native oxide is etched off before SPFM treatment, as indicated by the XPS analysis, the surface was still passivated by a thin chemical oxide after the SPFM treatment. The only possible exception is the surface treated with the 1000 ppm solution.

Figure 4 shows how the bond strength increases with anneal temperature for SPFM surfaces with varying HF concentration. The differences in surface energies corresponding to the different concentrations are small, and no clear correlation with the HF concentration can be found.

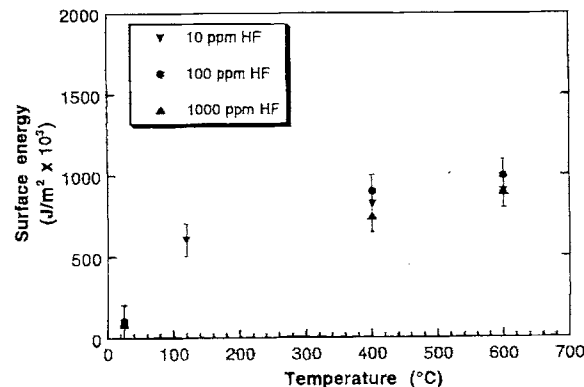


Fig. 4. Mean values of measured surface energies vs. annealing temperature (1 h in N<sub>2</sub>) for Si (100) surfaces treated in SPFM with varying concentrations.

Table I. Summary of the resulting silicon surface condition, i.e., presence of oxide and main atomic termination of the surface after different cleaning procedures. Note that small amount of absorbed OH are probably also present on all SPFM and SE surfaces (see text).

Mixture	Subsequent water rinse	Surface oxide	Main Termination
SPFM or SE (10-100 ppm HF)	No	Yes	F
SPFM or SE (10-100 ppm HF)	Yes	Yes	OH
SPFM or SE (1000 ppm HF)	No	No	F and H
SPFM or SE (1000 ppm HF)	Yes	No	OH and H
Aqueous HF	No	No	H

The increase with temperature follows the previously reported surface energies for RCA1(NH<sub>4</sub>OH:H<sub>2</sub>O:H<sub>2</sub>O<sub>2</sub>)-treated samples quite well,<sup>5</sup> but with slightly higher values. The agreement of the results for RCA1-treated surfaces regarding the dependence of bond strength on anneal temperature is not surprising, since both the SPFM- and RCA-cleaned surfaces are OH terminated.

**Combinations of differently terminated surfaces.**—Since these chemical preparation procedures make it possible to control the termination of the silicon surface and to choose among H, F, and OH for the termination, we decided to study the influence of H-atoms, F-atoms, and OH-molecules on the bonding behavior systematically by bonding combinations of the differently terminated surfaces. SPFM or SE cleaning followed by water rinsing was used to produce OH-terminated surfaces. An aqueous HF solution (10%) was used to give hydrogen termination. Since the nonrinsed, SPFM-cleaned wafers were found to be very difficult to blow-dry, the SE clean was used to achieve mainly fluorine-terminated surfaces. Surfaces treated in SE mixtures were easily blown dry even before a water rinse. The HF concentrations used for these experiments were 100 ppm in SPFM and 500 ppm in SE.

The results are summarized in Fig. 5 showing the room temperature bond strengths for the different combinations. As can be seen, OH-OH, *i.e.*, hydrophilic bonding, gave a considerably higher surface energy than H-H, *i.e.*, hydrophobic bonding, as expected from earlier experiments<sup>5</sup> and from the literature.<sup>6</sup> It has been suggested that strong attractive forces (*i.e.*, hydrogen bonding) between electronegative F atoms and H terminating the Si surface would give rise to high surface energies of bonded wafers.<sup>2,6</sup> However, as illustrated in Fig. 5, the bonding behavior of this combination of surfaces is fairly similar to that of two hydrogen-terminated surfaces. In fact, the surface energies obtained in the present investigation are somewhat lower than those found for the H-H bonding case. Furthermore, bonding one H- and one OH-terminated surface also gives about the same surface energy as purely hydrophobic bonding. This may not be too surprising since the higher surface energy obtained for purely hydrophilic room temperature bonding, OH-OH, originates from the dipolar properties of the terminating species on both surfaces. The Si-H bond is only weakly polarized, since Si is not a very electronegative atom. Hence the attractive force cannot be as strong between Si-H and Si-OH. We conclude that the bonding between a hydrogen-terminated and an OH-terminated or fluorine-terminated surface includes hydrogen bonding only to a very small degree. This results in surface energies of the order of those obtained for purely hydrophobic bonding, H-H.

**Void formation.**—Voids may occur at the bonded interface both during wafer contacting and during subsequent

annealing. The voids formed during wafer contacting are caused by particle encapsulation or surface damage. Void formation during low-temperature annealing may be caused by vaporization of water<sup>24</sup> or hydrocarbons.<sup>25</sup> The presence of voids after bonding of different combinations of surfaces was monitored after room temperature bonding as well as after annealing at 400 to 600°C for 1 h. With a few exceptions, the purely hydrophilic bonding, OH-OH, did not give rise to void formation during the annealing at these low temperatures. In the case of purely hydrophobic bonding, H-H, large voids were seen after the annealing in agreement with earlier reports.<sup>26, 27</sup> It can be speculated that these voids are due to adsorbed hydrocarbons<sup>25, 28</sup> on the surfaces. Bonding a fluorine-terminated or OH-terminated surface to a hydrogen-terminated surface also caused void formation during the anneal. These voids showed many similarities to those obtained after purely hydrophobic bonding, again showing the similarity between the three combinations H-H, F-H, and OH-H. A link between the hydrophobic silicon surface and the occurrence of large voids during low-temperature annealing can be seen. Hence, it is not very probable that vaporization of water is the cause of these voids. However, in some of the H-OH bonded samples, small point-shaped voids were generated during the anneal, in contrast to the dominating large "gas-bubble" type of voids that were most often observed. This deviating behavior of some of the H-OH samples may be due to the combination of hydrophilic and hydrophobic surface properties.

## Conclusions

A method for controlling the thickness of chemical oxides on silicon, between 0 and 10 Å, using a combination of an oxidizing and an etching agent has been presented. H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:HF (SPFM) and HNO<sub>3</sub>:HF (SE) mixtures with low HF contents were investigated. The preparation methods were used to modify the chemical oxide on silicon surfaces for bonding purposes. Both the SPFM and the SE cleaning methods permit hydrophilic bonding giving a high room temperature bond strength with a minimum of interfacial oxide.

The described method makes it possible to control not only the thickness of the chemical oxide but also the atomic composition of the wafer surfaces. This means that the termination of the surface dangling bonds can be controlled, which makes it possible to create "custom-made" silicon surfaces. OH, F, and H are terminating species that can be obtained by the described procedures.

Different bonded combinations of terminated surfaces were investigated. Neither the bond between a fluorine-terminated surface and a hydrogen-terminated surface nor the bond between an OH-terminated surface and a hydrogen-terminated surface gave any higher bond strength than the bond between two hydrogen-terminated surfaces. In these cases the room temperature adhesion is probably due to the same mechanism as in the case of two hydrogen-terminated surfaces.

Applications of these oxidizing/etching mixtures can be found also outside the area of wafer bonding. Both solutions are very well suited for cleaning and particle removal from the silicon surface due to the slow dissolution of the silicon. The possibility of controlling the thickness, and possibly also the porosity, of thin chemical oxides may be interesting also for other applications. For instance, one may be able to control the thickness and thereby the transmission probability of tunneling barriers very accurately.

## Acknowledgments

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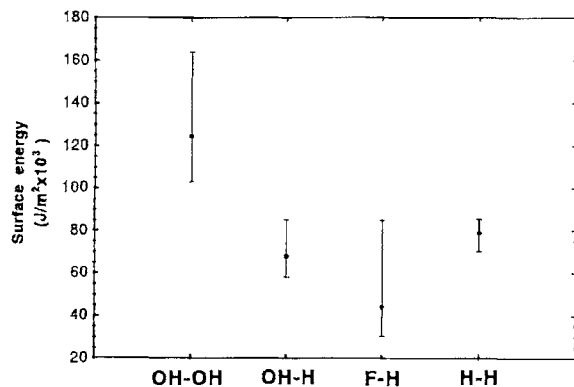


Fig. 5. Measured surface energies for bonded combinations of differently terminated surfaces. The error bars represent the spread in recorded data from the lowest to the highest value, and the large markers are mean values.



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## Modification of Silicon Surfaces with $H_2SO_4 : H_2O_2 : HF$ and $HNO_3 : HF$ for Wafer Bonding Applications

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### Abstract

Two combinations of oxidizing and etching agents,  $H_2SO_4 : H_2O_2 : HF$  and  $HNO_3 : HF$ , have been used to modify silicon surfaces prior to wafer bonding. The chemical oxide thickness can be adjusted between 0 and 10 Å by tuning the HF content of the mixtures. Using x-ray photoelectron spectroscopy it was found that the chemical composition of the surfaces can also be affected. Hydroxyl groups, fluorine, and hydrogen are terminating species that can be obtained by the described procedures. Both the described cleaning procedures permit hydrophilic bonding, giving a high room temperature bond strength with a minimum of interfacial oxide. The bond between a mainly fluorine-terminated or a mainly OH terminated surface and a hydrogen-terminated surface is no stronger than the bond between two hydrogen-terminated surfaces.

## Key Words

silicon surface phenomena oxidation etching wafer bonding  
X-ray photoelectron spectra bonds (chemical)

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## EXHIBIT D

# Silicon-On-Insulator by Wafer Bonding: A Review

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## ABSTRACT

Various approaches to wafer bonding technology are reviewed. Bonding kinetics are discussed as well as different mechanical and chemical thinning techniques. The structural and electrical qualities of state-of-the-art bonded SOI silicon films and devices built in them are detailed. Problems faced by this technology are evaluated.

Silicon device isolation by wafer-to-wafer bonding without any glue layer has been known for more than a quarter of a century, since Kenney applied for a United States patent in 1964 (1) (although the bonding process he used was meant to only transfer the device layer, rather than provide a semiconducting substrate). The bonding was assisted by very high temperature, 1225°C, and pressure, 2000 psi. A somewhat less cumbersome technique was introduced by Wallis and Pomerantz (2) for bonding silicon wafer to fused quartz, and investigated for silicon-on-insulator (SOI) applications by Anthony (3) and Frye *et al.* (4). This technique used lower temperatures, 850°-950°C (2, 3), and an externally applied electric field, which replaces hydrostatic pressure in providing the pulling force needed to achieve intimate contact of the wafer surfaces. The applied voltages ranged from 20 to 50V (3, 4). The major drawback of the field-assisted techniques is the need for electrical contact to the wafers at high temperature, making the process incompatible with batch processing and prone to contamination.

The potential of the wafer bonding technique became widely recognized after the first reports of SOI substrates produced by bonding without an externally applied electric field or pressure were published in 1985-1986 by Lasky *et al.* (5-7) and Shimbo *et al.* (7). The bonding process, followed by the removal of most of one of the wafers by mechanical and/or chemical means, creates a generic (non-mask-specific) SOI wafer. This technique provides an insulating oxide and a high-quality silicon device layer (comparable to bulk), as well as thermal oxide interfaces between the buried SiO<sub>2</sub>, the device layer, and the silicon substrate. It inherently permits the use of a wide range of thicknesses of both the insulating oxide and the device layer, which allows for more design flexibility. Applications, including pressure sensors (8), improved dielectric isolation (DI) wafers (9), complimentary metal-oxide-semiconductor (CMOS) transistors in a very thin (30 nm) silicon film (10), and 256 K static random access memory (SRAMs) (11), have been reported.

In this paper we review and discuss various aspects of wafer-bonding SOI technology and summarize the status of the art.

## Process Steps

The SOI wafer is created in four basic process steps: (i) Formation of an etchstop (by implantation or epitaxy) or polish-stop (an imbedded grid of slow polishing material, e.g., SiO<sub>2</sub>) in one of the wafers (the seed wafer). In the case of a nonselective polish-back approach, a plain oxidized wafer is used. (ii) Contacting the polished face of the seed wafer with that of another wafer (the handle wafer), oxidized or not, in ambient temperature and atmosphere. (iii) Bonding the pair at an elevated temperature. (iv) Grinding and etching or lapping and polishing the pair from the seed wafer side to the desired thickness of the silicon device layer.

## Room Temperature Bond (Contacting)

Two flat, smooth, hydrophilic surfaces can be bonded at room temperature (or "contacted") without using external force. The bonded materials can be metallic, semicon-

ducting, or insulating in nature. The contacting forces are believed to be caused by attraction between hydroxyl groups (—OH) (5, 7, 10, 11) and possibly some water molecules (13, 14) adsorbed on the two surfaces. The attraction can be significant enough to cause the spontaneous formation of hydrogen bonds across the gap between two wafers. The spontaneity in the initiation of the contacting occurs only between exceptionally flat, smooth, and clean surfaces. Once initiated, this bonding process can spread in a form of "contacting wave" throughout the entire area between two Si wafers with speeds of several cm/s (10, 14).

The hydroxyl groups are usually attached to the surface through the reaction of a clean surface oxide with the moisture from the air or atomized water source. Numerous other surface treatments can be used, if needed, to improve the hydrophilic properties of oxide surface. Ammonium hydroxide soaks (4, 10), sulfuric acid (7), NH<sub>3</sub> plasma (15), and other treatments (16, 17) were proposed. After treatment, the wafers are usually washed in DI water and dried in N<sub>2</sub> at room temperature before contacting.

## Bonding

Although room temperature bonds can withstand grinding and etchback processes (18), it is customary to strengthen the bonds by annealing at temperatures ≥800°C.

Kinetics of bonding have been extensively investigated for temperatures ranging from 20 to 1400°C, and times from 10s to 6h (10, 12). The bond strength was measured in terms of surface energy  $\gamma$  by a technique based on the theory of crack propagation in linear elastic solids (10). The energy is plotted vs. bonding temperature in Fig. 1 for a bonding time of 10 min.

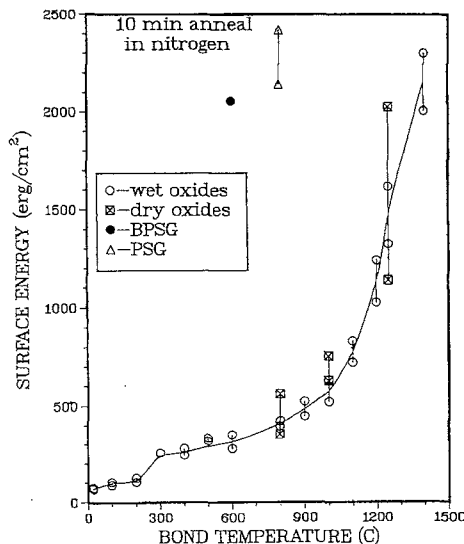


Fig. 1. Surface energy vs. bonding temperature for bonds between wet oxides 300 nm thick (3 in. Si wafers). Also shown are energies for dry oxides (3 in. wafers), BPSG (4 in.), and PSG (4 in.).

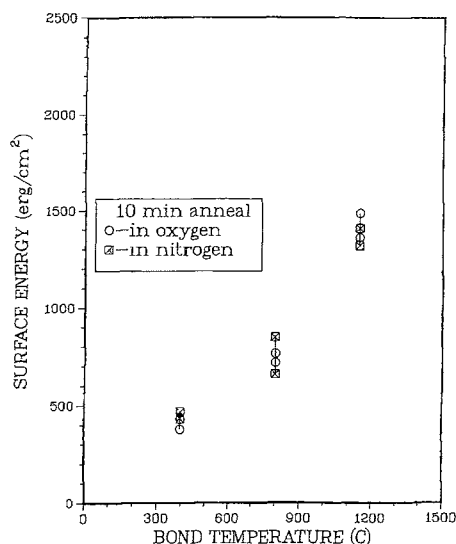


Fig. 2. Surface energy vs. bonding temperature; 4 in. wafers with wet 300 nm thick oxide bonded in  $N_2$  and  $O_2$ .

The bond strength increases monotonically with temperature and exhibits three distinct phases. The first phase, hydrogen bonding between hydroxyl groups (OH) on one surface with the oxygen atoms of either the  $SiO_2$  or OH groups on the other, begins at room temperature and starts being replaced by the second phase, the Si—O—Si bond, around 300°C. This phase involves elastic deformation of the wafers in the locally unbonded microareas and dominates through temperatures up to about 1100°C. Finally, in the third phase, viscous flow of the oxide around and above 1100°C leads to complete bonding. The surface energies of bonds between dry oxidized wafers are similar to those of bonds between oxides grown in steam.

Several researchers have chosen bonding in an oxygen atmosphere, explicitly (6) or implicitly (15, 23), indicating that it produces bonds superior to those formed in nitrogen gas. It is rather unlikely that, for the times and temperatures used in typical bonding, oxygen gas can diffuse through the crack, at best one or two monolayers wide, for distances comparable to the radius of the wafer. We have conducted an experiment to test this hypothesis. Figure 2 shows bond strengths measured for the oxidized (300 nm thick oxide) 4 in. wafers contacted in air and bonded in dry oxygen or nitrogen, respectively. Temperatures of 400°, 800°, and 1150°C were used. There is no difference, within

experimental error, between bond strengths corresponding to the two bonding ambients.

### Wafer Parameters vs. Bonding

It should be noted that although the model discussed above describes the general kinetics of wafer bonding, the values of the surface energies observed in our experiments represent only those particular sets of wafers tested. In accordance with the model, higher densities of  $\equiv Si-OH$  groups, smoother and more planar surfaces, lower softening points of the oxides, or thinner wafers, will all contribute to a stronger bond, i.e., parts of or the whole  $\gamma$  vs. temperature curve will shift toward the lower temperatures. The effect of these properties on bonding will be briefly discussed below. It was an inadequate quantity of any of the above parameters that forced earlier researchers to facilitate bonding with the assistance of an external force (hydrostatic pressure, electric field).

**Hydrophilic surfaces.**—Stengl *et al.* (14) measured the speed of the contacting wave between two silicon wafers at different temperatures and found it to decrease monotonically to zero as the temperature increased to 320°C. This reflects the loss of the source of the attractive force, presumably due to the thermal decomposition of the silanol group and desorption of the freed OH group.

**Surface roughness and flatness.**—The range and strength of the hydrogen bond forces are sufficient to elastically deform wafers, whose macroscopic flatness deviates over many micrometers, to achieve conformity of the two surfaces in room temperature bonding. The deformation also happens microscopically, accommodating some of the surface roughness. Both types of deformation are illustrated in the x-ray transmission topographs of the bond in Fig. 3. The change of the x-ray image contrast reflects the strain in the lattice due to the global (Fig. 3a) and local (Fig. 3b) deformations. The “roughness” of the latter has a spatial wavelength on the order of 0.1–1 mm. The areas at the edge of the wafer and in the large void of Fig. 3a that were not bonded exhibit smooth appearance indicating lack of local strain clearly in support of the postulated bonding-caused deformation. The roughness imaged by the x-ray topography does not appreciably change in the temperature range up to 1200°C, indicating that most of the deformation of the wafers happens during contacting.

In light of the above discussion, one should expect that wafers with a rougher surface, which require more deformation to conform to each other, should produce weaker bonds at a given temperature, all other conditions kept equal. The microroughness of a thin film surface would depend on both the original wafer surface topography and the film formation process. In particular, the roughness of

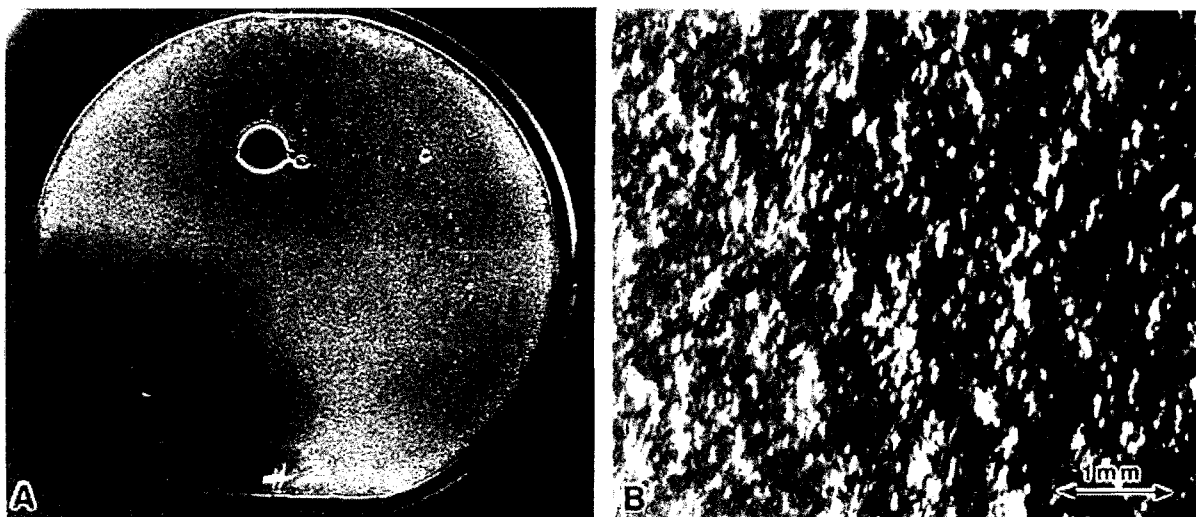


Fig. 3. X-ray topography of an interface between two 4 in. Si wafers bonded at 800°C: (a) shows macroscopic deformation (warpage), the darkening in the lower left corner of the image, (b) shows microscopic deformation (roughness) in this 20 $\times$  image.

the insulating layers (thermally grown or deposited) utilized in the wafer-bonding SOI wafers affects their bond strength.

**Thermal oxides.**—Thermal oxides are very smooth and, unlike most of the deposited films, their microroughness is not detectable by stylus profilometry or Nomarsky optical microscopy. Hahn *et al.* (20) have found, using light scattering and low energy electron diffraction (LEED) methods, that the roughness of silicon surface increases with the thickness of  $\text{SiO}_2$  layer grown on it (for a given growth temperature). We reason then that the oxide surface should also become rougher with the increasing thickness, at least for some small thicknesses, where the topography of the oxide surface can be affected by the local  $\text{SiO}_2$  volume changes at the growth (*i.e.*, Si— $\text{SiO}_2$ ) interface. It would be expected, then, that at least for thin oxides, the bond strength would decrease with increasing thickness of the thermal oxides of bonded wafers.

Silicon wafers with oxides of different thicknesses, all grown in steam at  $850^\circ\text{C}$ , were bonded in pairs and their surface energy measured. Figure 4a shows two surface energy vs. oxide thickness curves for wafers bonded at  $800^\circ$  and  $1200^\circ\text{C}$ , respectively. Both curves exhibit a rapid decrease of surface energy with increasing oxide thickness for thicknesses up to 200 nm. The energies for the wafers with 1–2 nm thick (native) oxides were unmeasurable, because the bonds were so strong that the wafers cracked upon the insertion of a blade used in the energy measurement technique. The curve for the  $800^\circ\text{C}$  bond levels off for oxides thicker than about 200 nm. Both the initial drop-off of the energy and its subsequent leveling off are in accordance with the postulated change of the oxide surface roughness. We believe that the increase in surface energy (after the initial drop-off) with increasing oxide thickness for the samples bonded at  $1200^\circ\text{C}$  is caused by easier oxide flow in the thicker oxides at that temperature.

An attempt was made to verify the model by evaluating the roughness of the five oxides used in the above bonding experiment. Long, linear scans of the surface profile with a stylus profilometer (60  $\mu\text{m}$  scan) and an optical profilometer (660  $\mu\text{m}$  scan) were used, as well as local two-dimensional ( $1 \times 1 \mu\text{m}$ ) scans with two different atomic force microscopes (AFM) to assess the roughness. Figure 4b shows the relationship between the root-mean-square (rms) roughness of the thermal oxide surfaces and their thickness as measured by the four instruments. The scatter of the data from sample to sample, as well as for

any given sample (the latter partially caused by the difference in the scan size), is too large to draw any conclusions in support or against the proposed model. The main reason for the inconsistency is believed to be the very high level of smoothness of the samples, comparable to the resolution limit of the measurement technique.

**Deposited films.**—The chemical vapor deposited (CVD) films are usually rough and fail to contact and bond to even very smooth silicon wafer surfaces without an externally applied force. Smoothing the surface by chemomechanically polishing the hard (undoped) oxides or annealing (flowing) soft (phosphosilicate [PSG] or borophosphosilicate glasses [BPSG]) oxides significantly improves their bonding capability. In particular, annealing previously nonadhering wafers, covered with a BPSG (4% of B, 4% of P) film, at  $950^\circ\text{C}$  for 15 min caused the two wafers to subsequently bond very well. Also, because of the lower viscosity of the BPSG, bonding was completed at lower temperatures. A  $600^\circ\text{C}$ , 10 min process was sufficient to increase the bond strength about sixfold over that measured for two thermal oxides bonded at the same temperature. PSG films showed similar performance (Fig. 1). If the high content of boron or phosphorus in those films can be ignored (*e.g.*, in some sensor applications) or dealt with (using diffusion barriers such as  $\text{Si}_3\text{N}_4$ ), these glasses can be used as adhesion layers when wafer bonding at low temperatures is required.

**Wafer thickness.**—Thicker wafers, being stiffer, are expected to yield less to the local pulling forces of the bonds forming across the gap between them. A weaker bond should result in bonding at a given temperature. It has been shown that thinner (more flexible) wafers bonded more strongly at a given temperature (10). The practical aspect of this phenomenon is that due to the very high flexibility of a seed wafer after it is thinned to about 1  $\mu\text{m}$  or so for SOI applications, normal processing temperatures should suffice to further increase bond strengths.

We have found that, contrary to the above, the bond strength for 4 in. wafers was consistently higher than that for the 3 in. ones, although the latter are thinner. A possible explanation is that the surface smoothness of the larger wafers is sufficiently better to offset the disadvantage of their increased thickness.

## Voids

The single most important problem faced by bonding technology is the lack of local bonding, leading to delamination and subsequent loss of the device film in the unbonded region. Two types of voids can be discerned: "extrinsic," formed during the contacting process, and "intrinsic," which are generated at elevated temperatures.

Particulate contamination or, more rarely, other residue present on the surface of either wafer is responsible for the former. An extreme lack of flatness and/or poor local hydrophilization of the surface may also lead to void formation. The voids are formed when the advancing contact wave surrounds the contaminated area, trapping ambient gas in it. For a given size of particle, the thicker (stiffer) the wafer, the larger the void will become. One might expect that the oxygen gas trapped in the void during contacting would be locally consumed by chemical reaction of the Si—O—Si bond formation, or outdiffusion into the two substrates during bonding at elevated temperatures. This in turn would lead to the collapse and rebonding of the void. We have not observed any appreciable void reduction. The change in the void sizes in the wafers annealed up to  $1100^\circ\text{C}$  for 30 min is negligible (some slightly increase or decrease) for pairs contacted in air or oxygen. Similar findings for the samples contacted in air, oxygen, and vacuum were reported by Black *et al.* (21) and for samples contacted in air by Stengl *et al.* (17). Much of the particulate contamination is of organic origin and it is likely that upon its decomposition at higher temperatures reaction products interact with the void surface, rendering it unbondable. We have seen a condensation-like decoration of some voids in bonded quartz-silicon wafer pairs, which supports this possibility.

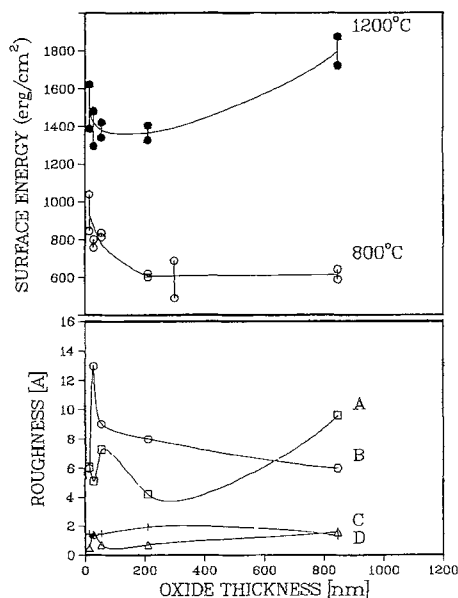
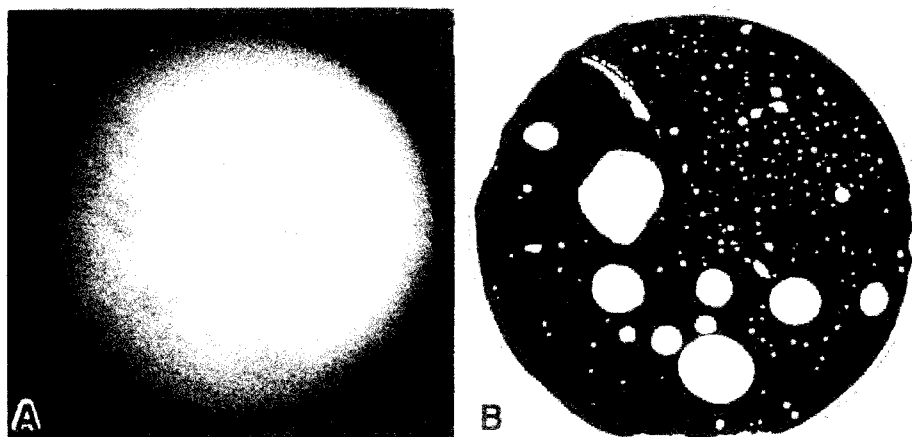


Fig. 4. (a) Surface energy vs. wet oxide thickness after bonding at  $800^\circ$  and  $1200^\circ\text{C}$ , (b) surface roughness (rms) vs. wet oxide thickness by optical (curve A) and stylus (B) profilometry, and 2-D imaging with different atomic force microscopes (C and D).



Fig. 5. Bonded 4 in. wafers imaged with: (a) infrared, and (b) ultrasound.



Intrinsic voids can be generated at elevated temperatures. Ohashi *et al.* (9) has reported void generation at and above 200°C, followed by disappearance of the voids around 700°–800°C for wafers with native oxides. Similar behavior has been observed by Bengtsson and Engstrom (22) and Lehmann (23). No such voids were reported for thermal oxide bonds. Outgassing of hydrocarbons adsorbed at the wafer surface has been proposed as the cause of these voids (23). Thermally-generated voids in bonded sputtered oxides were also observed (24). In this case gas incorporated into the film during sputtering outgassed during bonding. Void generation was strongly suppressed by annealing sputtered films prior to bonding.

Voids can be visualized by a variety of methods. The bond between silicon wafers can be analyzed by infrared (IR), ultrasonic, or x-ray imaging, or by thinning one of the wafers down to its oxide layer to visually inspect the voids. In the last case, the majority of voids bulge up due to the release of the compressive stress stored in the oxide film, thus becoming more visible. Visible and IR imaging are based on interference effects and thus are limited to voids whose height is more than about 1/4 of the probing wavelength. IR imagers are the most convenient real-time observation tools and can register voids of about 1 mm diam and bigger. X-ray topography (XRT) has the best resolution, tens of micrometers, but is very time consuming (several hours for a 4 in. wafer) and expensive. Reflection ultrasonic imaging relies on the enhancement of the beam energy due to reflections off imperfections at the bond and is found to produce somewhat more detailed images than IR. The image formation, however, takes much longer. Figure 5 shows a side-by-side comparison of full wafer images obtained by IR and ultrasonic methods. Many small voids seen in the latter do not appear in the former. The images in Fig. 6, formed by ultrasound, XRT, and optically (after full etchback), and magnified by factor of about two, show the capability of these methods for imaging small voids.

An external force, hydrostatic or electric, can somewhat remedy the lack of local bond formation in an inferior wafer pair by forcing the opposing surfaces of a void into intimate contact at elevated temperatures (21, 25, 26), particularly when the void is located near the wafer edge and can vent entrapped gas.

Stengl *et al.* (17) introduced a promising concept of water jet cleaning of two wafers in close proximity, which does not require a clean-room environment and contributes to a dramatic reduction of voids.

#### Device Layer Formation

The bonding process is followed by thinning of one of the wafers (the seed wafer) to an appropriate device film thickness. The diagram in Fig. 7 shows various thinning techniques utilized in SOI wafer formation. Two basic approaches have been used. The first is lapping (or grinding) and chemomechanical polishing, and the second, grinding followed by selective etchback (the, so-called, BESOI technique [bonding-and-etchback SOI]). The grinding is primarily a rather crude, time-saving step that can be used to remove all but the last several tens of micrometers of the seed wafer. The polish-back with no polish-stop thinning technique is an excellent choice for thick (>1  $\mu\text{m}$  of Si) SOI applications such as bipolar analog circuits, BiCMOS, high-voltage, high-power, or micromechanical sensors. The etchback with double etchstop formed by B<sup>+</sup> implant and epitaxy, or by double epitaxial layer (p<sup>++</sup> epi and device epi), seems to be the best approach so far for thin-film (<0.5 of Si) SOI. A summary of the parameters for all the thinning techniques is given in Table I.

**The polish-back process.**—The standard polishing method is cheaper than the etchback technique but the thickness uniformity of the device layer is limited by the flatness and parallelism of the handle wafer (the SOI substrate).

A modified version of this thinning method employs a polish-stop layer consisting of a pattern made out of a slow

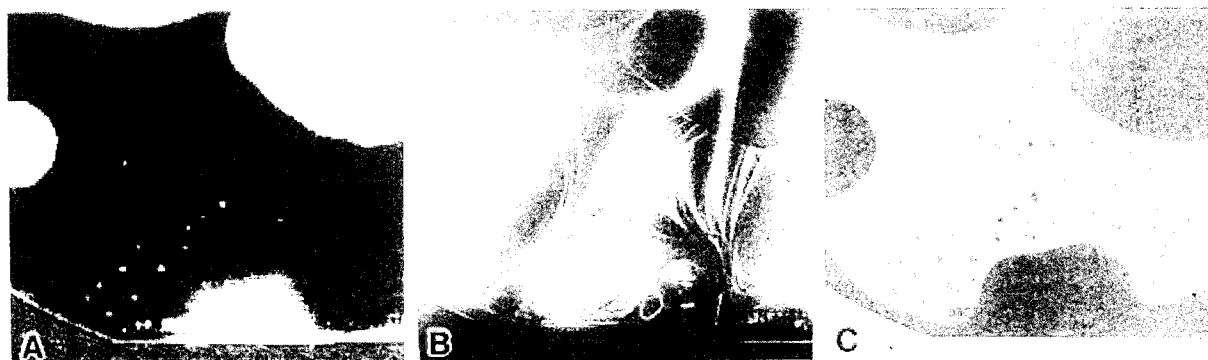


Fig. 6. A part of bonded 4 in. wafers imaged with: (a) ultrasound, (b) XRT, and (c) optically (after full etchback of seed wafer). Magnification about 2 $\times$ . None of the small voids imaged here can be seen with IR.

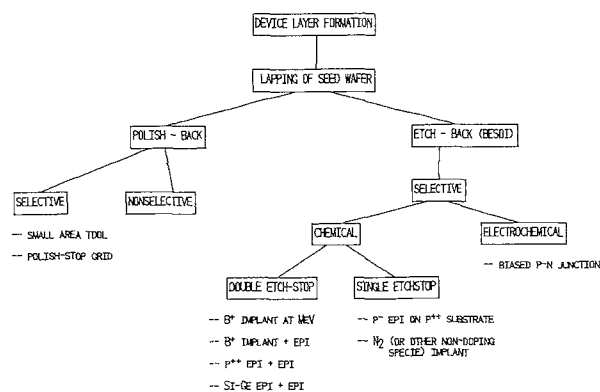


Fig. 7. Thinning techniques for SOI by wafer bonding

polishing material such as SiO<sub>2</sub> buried in the device wafer (28). It is mask-specific and more complex than the no-stop polishing, but can produce layers with much better thickness uniformity.

Another polishing technique has been proposed by Yamada *et al.* (29). Here, local polishing with a small-area tool was combined with thickness mapping in a computer feedback loop. This method seems to have the best potential to produce cheap, generic SOI wafers with highly uniform silicon films for CMOS as well as other, less-demanding applications.

**The etchback process.**—After initial grinding, the remainder of the seed wafer is further thinned by chemical or electrochemical etching. A built-in etchstop is used to reduce the etch rate by several orders of magnitude. Figure 8 shows the structure of the seed wafer for various etchback techniques.

The selective chemical etchback thinning technique has two basic variants: a single or double etchstop. The first involves the selective removal of a p<sup>++</sup> wafer with an HF-based etchant that leaves behind a low-doped epi device film. The etchant is usually a mixture of HF, HNO<sub>3</sub>, and CH<sub>3</sub>COOH in the ratio of 1:3:8 (the 1-3-8 etch) (30). The limited selectivity allowed by this technique results in only moderate silicon film thickness uniformity. Moreover, the etch requires electrochemical control of the oxidizer content to maintain its selectivity (18). The etch abruptly reduces its etch rate upon reaching highly resistive material and produces a passivation layer, a porous SiO<sub>x</sub> that can be

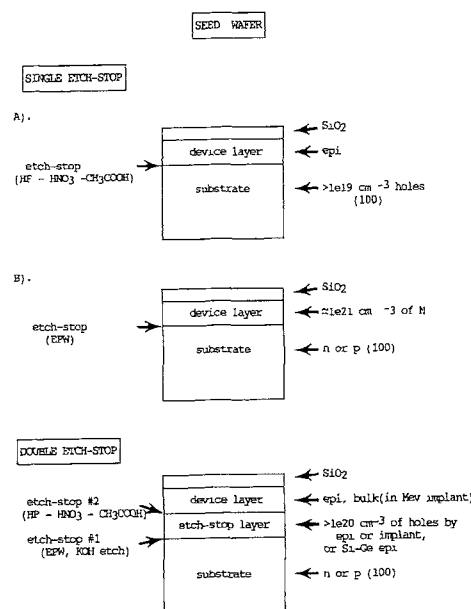


Fig. 8. Seed wafer structure for various etchback thinning techniques

as thick as 70 nm. This layer can be removed by a mixture of HF and an oxidizer such as HNO<sub>3</sub>, KMnO<sub>4</sub>, etc.

The double etchstop technique requires a buried p<sup>++</sup> layer in a low-doped wafer. This structure can be created by implantation of boron alone, or an implant of boron followed by the growth of a low-doped epi film on the seed wafer before bonding (10). In the first case, a high-energy (>1 MeV) implant is required to obtain a device layer with an appropriate carrier concentration (<1e16 cm<sup>-3</sup>). We were also successful in utilizing a double-epi procedure (p<sup>++</sup>, p<sup>-</sup>) which simplifies the technology and avoids a certain amount of surface roughness related to the p<sup>++</sup> implant damage. Two selective etches are used to remove the p<sup>++</sup> wafer and p<sup>++</sup> buried layer, respectively. An ethylenediamine-pyrocatechol-water (EPW) etch (31) is used to remove most of the remainder of the low-doped seed wafer. A 1-3-8 etch removes the p<sup>++</sup> layer. The combined selectivity of the etches is greater than 10,000:1. The final thickness uniformity in this as well as the single etchstop approach depends on the uniformity of the last etchstop

Table I. Summary of wafer thinning techniques for the wafer-bonding SOI, current best results

Method of thinning	Si thickness uniformity (μm)	Roughness	Process complexity	Comments	Reference
Polish-back					
1. Regular	±0.2	Excellent	Low	Si thickness uniformity depends on handle wafer	(27)
2. Small-area tool	±0.4	Excellent	Mod	Si thickness uniformity is independent of handle wafer	(29)
3. Polish-stop	±0.02	Excellent	High	Mask specific, complex	(28)
Etchback					
Chemical					
1. Single etchstop					
a) p <sup>-</sup> epi on p <sup>++</sup> substrate	±0.03-0.07	Good	Low	Difficult etching	(5, 25)
b) N <sub>2</sub> implant into p or n substrate	±0.002	?	Low	Implant damage (?) High N <sub>2</sub> content	(32)
2. Double etchstop					
a) B <sup>+</sup> implant + p <sup>-</sup> epi	±0.005	Very good	Mod	Etchpits ≤10 <sup>3</sup> /cm <sup>2</sup>	(This work)
b) p <sup>++</sup> epi + p <sup>-</sup> epi	±0.012	Excellent	Low	Etchpits ≤3 × 10 <sup>3</sup> /cm <sup>2</sup>	(This work)
c) B <sup>+</sup> implant at MeV	±0.005	Excellent	Low	Expensive implant	(Unpublished)
d) Si-Ge epi + p <sup>-</sup> or n <sup>-</sup> epi	±0.02 <sup>a</sup>	?		MBE growth, misfit dislocations	(34)
Electrochemical					
1. Biased p-n junction etchstop	Good <sup>b</sup>	Poor	High	Complex preparation for biasing	(18)

<sup>a</sup> With diamond machining.  
<sup>b</sup> 1 selectivity.

plane distance from the original surface of the seed wafer, i.e., the top epi thickness and/or boron implant uniformity. The increased total selectivity of the etchback process, in conjunction with a very good epi deposition source, recently produced silicon film thickness uniformity with an average standard deviation  $\sigma = 12$  nm for double-epi SOI wafers, and  $\sigma = 4$  nm for the single-epi ones, across a 4 in. wafer.

A successful attempt to create a buried etchstop by  $N_2$  implantation (32) has been recently reported. A nitrogen dose of  $4 \times 10^{16} \text{ cm}^{-2}$  implanted at 120 keV was found sufficient to significantly reduce the etch rate of the EPW etch. Annealing at high temperatures had little effect on the etch rates. A similar successful etch-stopping property of implanted carbon has been reported by Lehmann (33). It is not clear at this point what causes the etch-stopping action here. Neither the nitrogen nor the carbon implant provides the carrier concentration available in the activated boron etchstop implant. Nor is the concentration of the species high enough to form a continuous stoichiometric  $\text{Si}_3\text{N}_4$  or  $\text{SiC}$  layer that would dramatically alter the EPW etch rate. The quality of the Si films remains to be assessed. Substantial amount of implant damage and implanted species-related precipitation is likely to be present in the film, and an extensive thermal treatment may be required to alleviate these deficiencies. However, the reported Si layer thickness variation of less than 2 nm across the nitrogen-implanted wafer is very impressive and certainly invites further investigation of this technique.

A molecular beam epitaxial (MBE) grown  $\text{Si}_{0.7}\text{Ge}_{0.3}$  layer has been investigated as an etchstop layer by Godby *et al.* (34). Low etch selectivity (17:1), the expense of the MBE process, and misfit dislocations (although mostly confined to the etchstop these may lead to an imprint of their pattern on the device layer after the etchback) are drawbacks associated with this technique.

An electrochemical etchback has been proposed where a reverse-biased p-n junction serves as an etchstop (18). The junction is created by an n-type epilayer deposited on a low-doped p substrate. KOH-based etch is used for the etchback. An elaborate wafer preparation scheme to provide bias through the SOI oxide, and a final orange-peel type of roughness, renders this technique less attractive than the others described above.

### Bonded Wafer SOI Properties

**Structural properties.**—SOI wafers produced by bonding and thinning have thermally grown insulating oxide and Si film- $\text{SiO}_2$  interfaces. There are no traces of a bond in the SOI oxide in fully processed wafers (10). Etch pit densities in the films produced by the etchback of single-epi + boron implant seed wafers were reported below  $1000/\text{cm}^2$  (10, 19). We have obtained counts below  $300/\text{cm}^2$  for the double-epi seed wafers. This suggests that the residual implant damage may not be the sole factor contributing to the defects as proposed earlier (10). The epi growth process is another likely source of some of the observed imperfections. There are no reports, to our knowledge, of defect densities in polish-back wafers, although one would expect them to be very low, comparable to the bulk wafers. No defects were observed in the Si films of BESOI wafers by cross-sectional transmission electron microscopy (TEM).

Silicon layer thickness uniformity, as mentioned above, varies from  $\pm 0.2 \mu\text{m}$  for the best generic polish-back wafers to about  $\pm 0.004 \mu\text{m}$  for the ones obtained through the double etchstop procedure. Wafer warpage was comparable to the source material ( $< 15 \mu\text{m}$  bow in 4 in. wafer).

Roughness of the top surface of the silicon film is difficult to assess quantitatively for these fine surfaces, although it can be discriminated with the help of Nomarsky optical microscopy. The double-etchstop samples with a boron implant are slightly rougher than the ones with a double-epi structure. Those in turn are minimally less smooth than the polished surfaces. However, high-resolution TEM observations could not distinguish among these surfaces.

**Electrical properties.**—The charge density at the bond annealed at  $1100^\circ\text{C}$  was evaluated by a capacitance-voltage

Table II. Hall mobilities and carrier generation lifetimes in the wafer-bonding SOI films

Mobility ( $\text{cm}^2/\text{Vs}$ )		Carrier lifetime ( $\mu\text{s}$ )	Reference
Electrons	Holes		
		15-20 27	Maszara <i>et al.</i> (10) Lasky <i>et al.</i> (5) Spangler and Wise (35) Xu <i>et al.</i> (16) Xu <i>et al.</i> (16)
1096 (1160)	350 409 (420)		

Control bulk data in parentheses.

method (10) and was found to be about  $1 \times 10^{11} \text{ cm}^{-2}$  and negative. Published values of generation lifetimes and carrier mobilities are comparable to bulk material and are listed in Table II. Metal-oxide-semiconductor field effect transistors (MOSFETs) made in bonded SOI had generally better subthreshold slopes and leakage currents than bulk devices. Channel carrier mobilities for SOI and bulk devices are comparable. Table III summarizes n- and p-MOS transistor parameters reported by several workers for bonded SOI materials. We measured a lateral diode ideality factor of  $n = 1.04$  for a 90 nm thick Si film (10). Krull *et al.* (37) reported  $n = 1.15$  for a  $2 \mu\text{m}$  thick Si film. The high-temperature ( $\approx 500^\circ\text{C}$ ) operation of ring oscillators has been achieved (10). As the above results indicate, the bonded SOI wafer technology produces top-quality devices, in many aspects surpassing other competing technologies. The excellent microscopic properties of the wafers extend beyond single transistors and simple circuits, as demonstrated by recently reported working 256k SRAMs fabricated in a  $0.3 \mu\text{m}$  Si film on SOI substrate (11).

### Heterostructures by Wafer Bonding

Wafer bonding techniques can be used to form other semiconductor-on-insulator wafers, where a film of single-crystal semiconductor is formed on a different substrate with an insulating layer between them. A variety of substrate-film combinations allow the use of two different semiconductor material side by side, e.g., InP and Si for optoelectronics with a silicon "brain." The substrate can also be utilized in a passive manner, e.g., a Si wafer providing a mechanical support for brittle GaAs, or a fused quartz substrate allowing optical access to the back of the silicon device layer for optical imaging applications. Successful bonding of GaAs to Si, InP to Si, Ge to Si, and Si to fused quartz, and subsequent thinning, has been demonstrated (39). In some cases, adhesion promoters such as reactively sputter-deposited  $\text{SiO}_2$  layers were used. The bonding was performed at temperatures low enough to avoid any failure due to the mismatch of thermal expansion coefficients, yet the bond strength was sufficient to survive the thinning process. The thinning process, augmented by the etching of a stress-relieving pattern, allowed the thermally mismatched films to withstand subsequent device processing temperatures. High electron mobility transistor (HEMT) devices fabricated on thinned GaAs and InP bonded to silicon show no deterioration of their electrical parameters in comparison with similar devices formed on bulk substrates (39).

### Conclusions

The wafer bonding technique offers a wide range of choices for the thicknesses of the silicon and insulating oxide films. Oxide thicknesses ranging from zero, for bulk silicon power devices, to full substrate thickness (i.e., a fused quartz wafer) for microwave and optoelectronic applications are available. Both silicon and oxide films retain the structural and electrical quality of bulk material and remain superior to that of other SOI materials. Si films can be as thin as 30 nm for fully depleted MOSFETs with high transient radiation hardness, high-temperature performances and high speed, and as thick as tens or hundreds of micrometers for high-power, high-voltage SOI circuits. Bonding without applied electrical or mechanical force appears to be the technology of choice. Approaches to thin-

Table III. MOS device parameters comparison for the wafer-bonding SOI and bulk silicon substrate

Mobility [cm <sup>2</sup> /Vs]	N-MOS		Mobility [cm <sup>2</sup> /Vs]	P-MOS		Silicon film thickness (μm)	References
	Subthreshold slope (mV/dec)	Leakage current (pA/μm)		Subthreshold slope (mV/dec)	Leakage current (pA/μm)		
640	140 <sup>a</sup>	0.05				1.3	Spangler and Wise (35)
	68	<0.1		68	<0.1	0.02-0.1	Mazara et al. (10)
451	65 <sup>a</sup>	<0.001	179	100 <sup>a</sup>	<0.05	0.4	Lasky et al. (5)
(454) <sup>b</sup>	(130) <sup>a</sup>	(<0.001)					Lasky et al. (5)
590	118	1.0	300	90	0.2	0.5	Palkuti et al. (36)
(610)	(112)	(0.8)	(310)	(80)	(0.2)	2.0	Palkuti et al. (36)
451			124				Krull et al. (37)
(468)			(151)				Krull et al. (37)
	70 <sup>a</sup>	<0.1				0.5	Gotou et al. (26)
753						0.18	Caviglia (38)

<sup>a</sup> Evaluated from a plot.<sup>b</sup> Control bulk data in parentheses.

ning are two-pronged. The no-stop polish-back is most promising for thick SOI films (>1 μm) and at this point is near commercialization by one of the major wafer suppliers (40). The etchback of wafers with double-epi layer seems to be the best candidates for thin SOI films (<0.5 μm) for CMOS applications, at least until polishing with small-area tool matures.

Bonded SOI shows excellent electrical performance with film properties comparable to bulk material. All the processing steps lend themselves to automation and/or batch processing and are highly compatible with the bulk wafer production environment, particularly the polish-back techniques.

Bonding techniques also bring the promise of expansion of the standard SOI structure into a broader spectrum of semiconducting and insulating materials combined on a single wafer.

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## Silicon-On-Insulator by Wafer Bonding: A Review

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### Abstract

Various approaches to wafer bonding technology are reviewed. Bonding kinetics are discussed as well as different mechanical and chemical thinning techniques. The structural and electrical qualities of state-of-the-art bonded SOI silicon films and devices built in them are detailed. Problems faced by this technology are evaluated.

### Key Words

wafer bonding    silicon-on-insulator    isolation technology    mechanical properties  
chemical analysis    reviews

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May be of interest

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<p>(Invited) SiGe BiCMOS Heterogeneous Integration Using Wafer Bonding Technologies</p> <p><a href="#">Wolfgang Witschack et al., ECS Meeting Abstracts</a></p>	<p>6 Reasons Why People Skip Their HIV Meds</p> <p><a href="#">HIV 1</a></p>
<p>The Study of the Bonding Energy on Silicon-to-Glass Wafer Bonding</p> <p><a href="#">Yu-Ko Chuan et al., ECS Transactions</a></p>	<p>Vitamin D May Cut Asthma Attacks</p> <p><a href="#">Asthma</a></p>
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## EXHIBIT E



# INTERCHIP VIA TECHNOLOGY- THREE DIMENSIONAL METALLIZATION FOR VERTICALLY INTEGRATED CIRCUITS

E. Bertagnolli, D. Bollmann, R. Braun, R. Buchner, \*M. Engelhardt, T. Graßl, K. Hieber, G. Kawala, \*M. Kleiner, A. Klumpp, \*S. Kühn, C. Landesberger, \*W. Pamler, R. Popp, P. Ramm, \*E. Renner, G. Ruhl, \*A. Säger, \*U. Scheler, \*C. Schmidt, \*S. Schwarzl, J. Weber

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## ABSTRACT

The mainstream planar technology is marked by physical and technological limitations, which have a severe impact on system characteristics. The performance, the multifunctionality and the reliability of microelectronic systems will be mainly limited by the wiring between the ICs and subsystems. The „on-chip“ wiring also leads to a critical performance bottleneck for future IC generations which can be solved only temporarily by the introduction of additional metallization layers and innovative materials (copper, low- $\epsilon$ -dielectrics). 3D IC fabrication creates a basis to overcome these drawbacks and to pave the way for system approaches of an entirely new quality. We realized a three dimensional metallization for Vertically Integrated Circuits (VIC) using a newly developed technology that allows stacking and vertical interchip wiring of completely processed and electrically tested wafers using available microelectronic processes. Wafers are stacked by an aligned bonding process. Vertical electrical connections are formed between the uppermost metal levels of the bonded wafers by fabrication and metall refill of high aspect ratio interchip vias. This interchip via (ICV) concept allows the formation of multiple wafer stacks using CMOS compatible materials and process steps exclusively and avoids wafer back processes. The potential of the ICV technology is the realization of some 100 000 vertical interconnects per  $\text{cm}^2$  with  $1\text{-}4\text{ }\mu\text{m}^2$  interchip vias, arbitrarily selectable.

## INTRODUCTION

The Vertically Integrated Circuits technology was developed [1, 2] to provide an IC stacking technology for the realization of micro-electronic systems with new or highly improved features. Such systems can now be realized with IC stacking technologies utilizing arbitrarily selectable vertical interconnections (Fig. 1). VICs consisting of different ICs such as ASICs, memories, sensors etc. exhibit a new class of multi-

functionality allowing highly parallel signal processing due to a large number of vertical contacts, high performance gain and high spacial packing density. Low power dissipation resulting from short interconnects and both high electrical and mechanical reliability are further advantages of this stacking technique. The key applications of VICs are those where realtime image and signal processing are required e. g. traffic safety, navigation systems and automation. Ultra compact systems as required for medical applications and micro-systems for in-situ control of processes and engines are further candidates to be realized with VIC technology. In contrast to 3D integration approaches e.g. proposed by Y. Hayashi et al [3, 4], VIC technology requires only front side processing of wafers. All of the necessary processes are fully compatible to the requirements of a CMOS line.

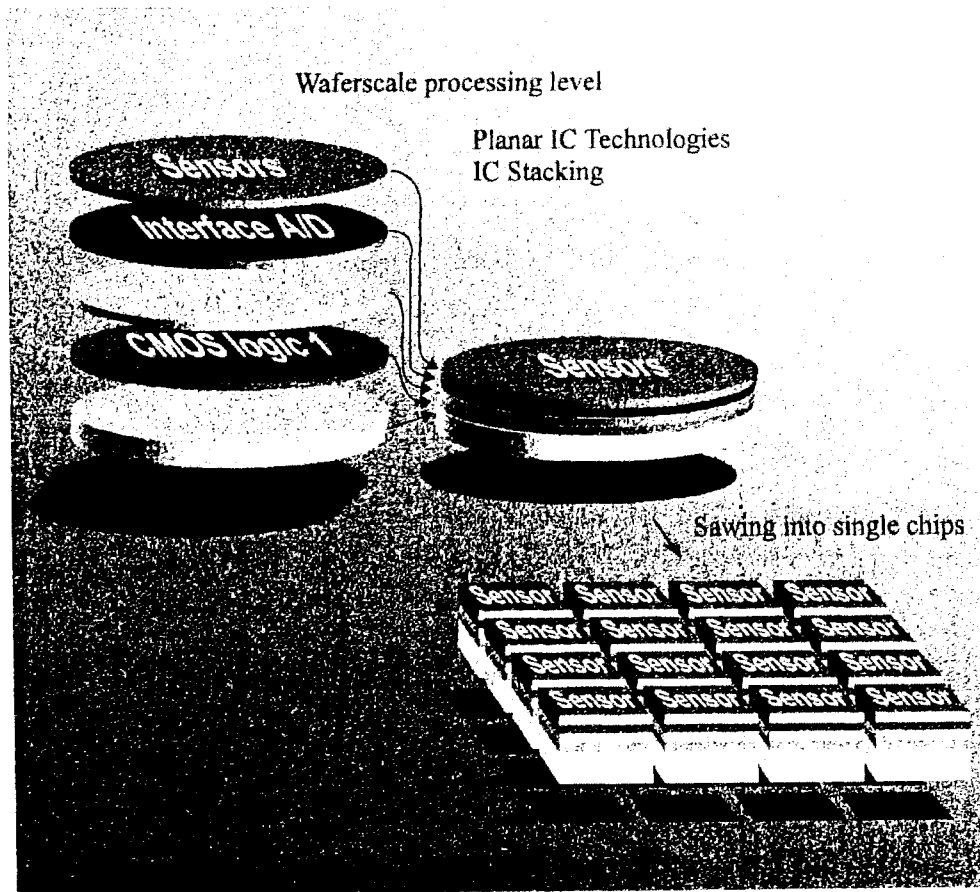


Fig. 1: Combination of different Planar IC Technologies to a Vertically Integrated Circuit. Every planar technology can be optimized to reach maximum yield.

## RESULTS AND DISCUSSION

### The Interchip Via - Concept

We developed the CMOS-compatible interchip via concept that is based on the optically adjusted bonding of a thinned top wafer to a bottom wafer with an organic glue layer in between. The vertical wiring between the uppermost metallization levels of both wafers is accomplished by following steps: The topography of both top- and bottom wafer is planarized by a combination of CVD of oxide and chemical mechanical polishing (CMP). The interchip vias are prefabricated on the top wafer by highly anisotropic plasma etching processes and lead through all intermetal dielectrics (IMD) into the silicon substrate. The etch depth in silicon is typically 10  $\mu\text{m}$ . After thinning the topwafer from the backside to a thickness smaller than the etch depth the vias are opened and can be used as alignment marks at the backside (Fig. 2). After bonding the top wafer onto the polyimide layer of the bottom wafer the cleaned via is used as etch mask for opening the polyimide and subsequent planarisation and passivation layer of the bottom wafer. Filling the vias with tungsten plugs and processing the interconnects between the vertical wiring and the contact pads of the top wafer finishes the processing sequences of the VIC concept (Fig. 3).

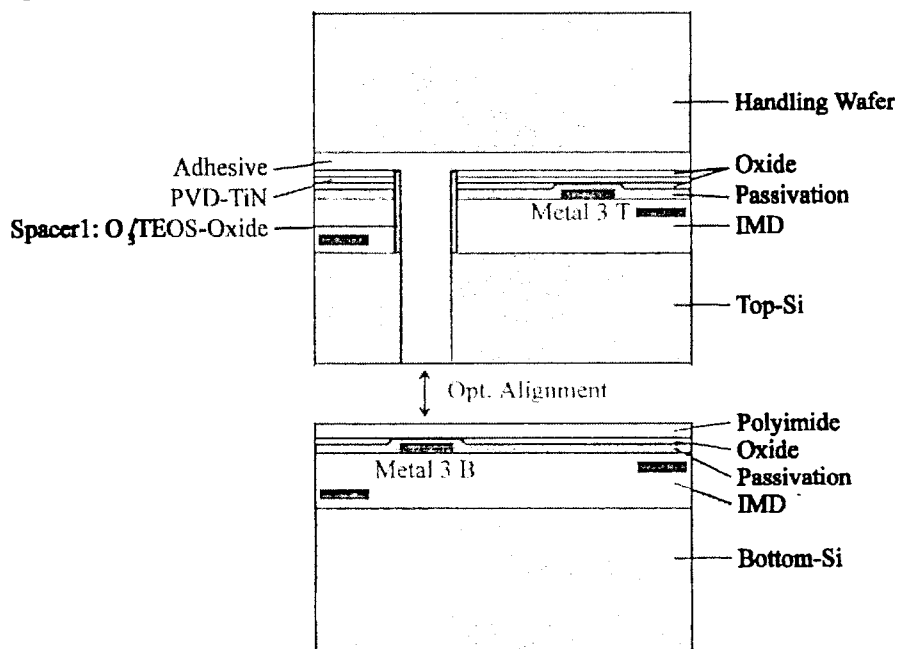


Fig. 2: Optical alignment of the thinned top- to bottom wafer using opened vias

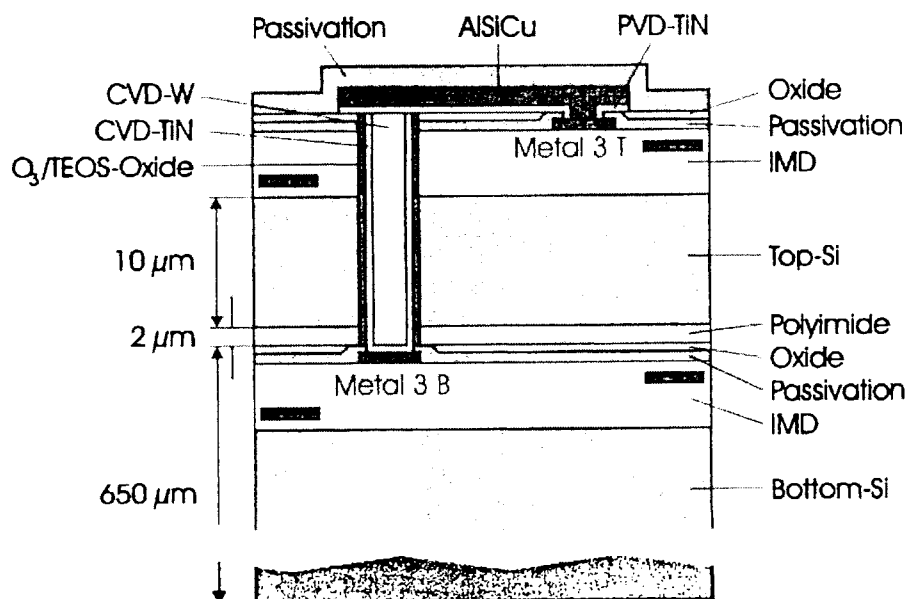


Fig. 3: Interchip via (ICV) concept for Vertically Integrated Circuits

### Trench Etch

For the silicon trench etching and subsequent plasma etching processes, the top wafer requires the deposition of a hard mask bilayer consisting of PVD-TiN and PECVD-SiO<sub>2</sub>. The entire thickness of the hard mask, the planarizing oxide, the passivation films and the IMD of a 3-level metallization is typically 6.5 μm. A single step process (CHF<sub>3</sub>, CF<sub>4</sub>, Ar) was developed for the SiO<sub>2</sub> trench etching without any lateral etching of the individual layers or boundaries [5]. Since the via cleaning requires an HF dip (refer to trench etching), a spacer technique is employed after the resist stripping to protect the BPSG layer of the IMD from etch attack (Spacer 1). This, in turn, prevents the formation of cavities, when the interchip vias are filled (metallization). For the generation of the spacer, an O<sub>3</sub>/TEOS oxide deposition at a wafer temperature of around 400°C has been developed [6]. Even at the high aspect ratios encountered here in the SiO<sub>2</sub> trench, it results in an edge coverage of almost 100%. A spacer etching marked by a high intrinsic anisotropy creates an SiO<sub>2</sub> case in the trench. The subsequent Si trench etching (HBr, NF<sub>3</sub>, He/O<sub>2</sub>) uses the uppermost PECVD-oxide layer as hardmask and results in typically 10 μm deep vias into the substrate [5] as can be seen in figure 4.

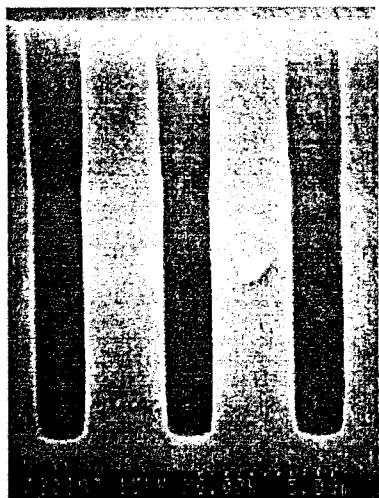


Fig. 4: High aspect ratio ICVs obtained by dielectric trench and subsequent silicon trench etching

### Thinning

The thinning of the top wafer from its back surface is done in three steps: After grinding to a remaining thickness of typically 300 $\mu$ m, the top wafer is adhesively connected to a dummy substrate (handling wafer) for mechanical stabilization. Highly uniform wafer thinning is then achieved by a combination of wet chemical spin etching and chemical mechanical polishing (CMP) that opens the interchip vias from the rear.

### Polyimide bonding

The frontside of the bottom wafer is spin coated with polyimide as glue layer (thickness 2 $\mu$ m). We chose polyimide as intermediate layer for different reasons: It is a CMOS-compatible organic material that can be bought in microelectronic quality. The chosen polyimide is stable up to 500°C and can tolerate particles easier than an inorganic layer as SiO<sub>2</sub>, that is often used for high temperature bonding (silicon fusion bonding). We achieved stable bonding by the following process sequence: The polyimide is spun on the bottom wafer and cured at 380°C. The surface of the polyimide layer is activated in an RF-plasma using water as atmosphere. The surface is hydrophilic after this procedure. The polished back of the top wafer is hydrophobic after CMP. This latter surface is therefore treated with a plasma discharge and additionally with a primer to have a proper bonding between polyimide and silicon surface of the top wafer. Figure 5 shows the results of a proper pretreatment sequence to get the best bonding results. We tested the mechanical stability of the bonded polyimide interface by tearing bonded chips apart. With the appropriate sequence the location of failure is not the bonded interface but the ceramics or the silicon chips itself. Figure 6 shows the model of the chemical state of a polyimide and silicon surface prior to bonding, after the treatment with water plasma, chlorine plasma and primer molecules.

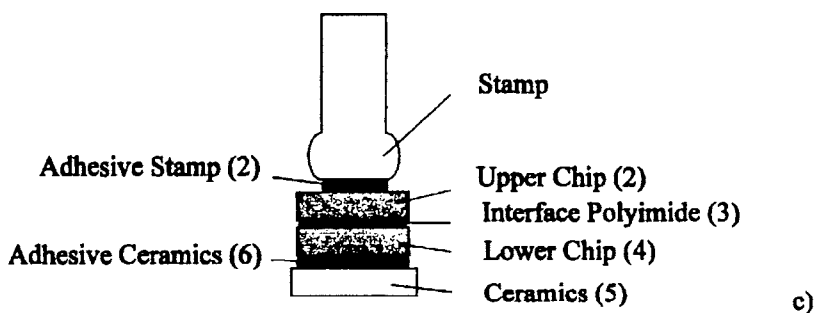
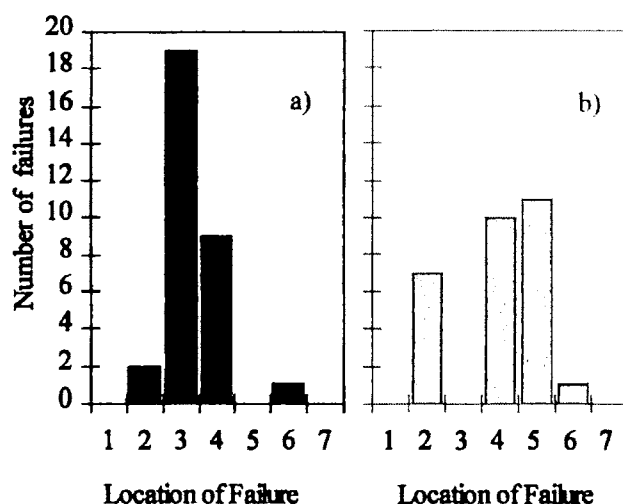


Fig. 5: Results and experimental setup for measuring the stability of bonded polyimide interfaces. The bonded wafer is sawed to single chips. Every chip is mounted to a ceramics plate and a metal stamp by an adhesive layer (c)). The maximum amount of tearing force is documented and the location of failure is analysed. As can be seen in picture a) the location of failure concentrates to the polyimide interface when the pretreatment is not successful. Only with the combination of polyimide and silicon wafer surface treatment including the application of primer molecules succeeds in stable polyimide bonds (fig. b)). The maximum amount of tearing force reaches up to 2000 kp/ cm<sup>2</sup>.

The lithographic levels of the top and the bottom wafers are carefully adjusted to each other (misalignment  $\leq 1\mu\text{m}$ ) using a flip-chip bonder with split beam optics (Fig. 2). After the wafer bonding at 400°C, the handling wafer is removed leaving the actual wafer stack that can be reprocessed as a standard silicon wafer. Specific cleaning processes have to be applied in order to remove the adhesive layer in a residue free way.

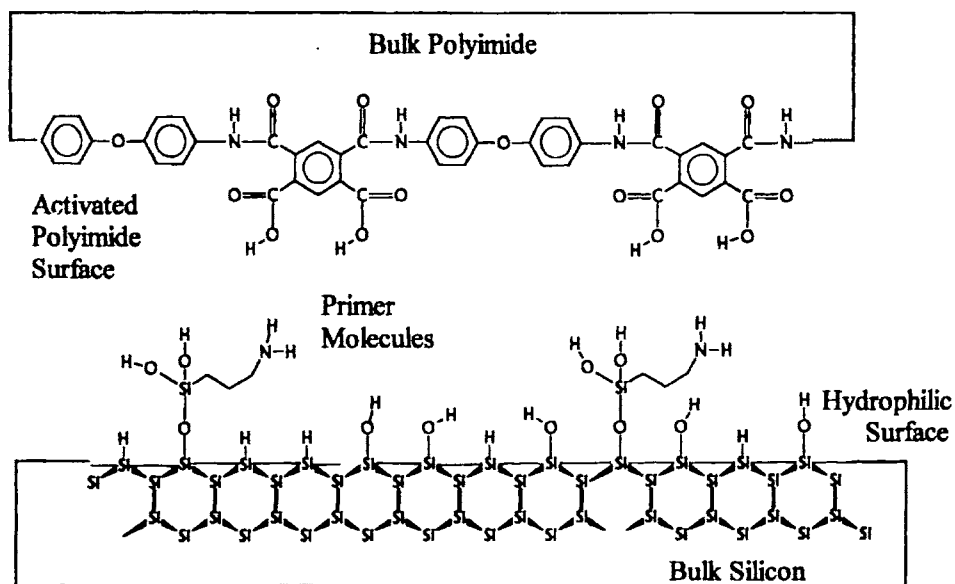


Fig. 6: Model of the chemical state of a polyimide and silicon surface prior to bonding, after the treatment with water plasma, chlorine plasma and primer molecules.

#### Interchip via formation

For interchip via formation, the uppermost metal level of the bottom wafer is exposed by anisotropic plasma etching of the polyimide and the passivation layers. This dielectric etching process uses the TiN layer of the top wafer as hardmask. For lateral electrical via isolation, a dielectric spacer technique is applied involving highly conformal CVD of O<sub>3</sub>/TEOS-oxide (Spacer 2). The interchip vias are metallized by refilling with highly conformal CVD of TiN/W bilayer (25nm/900nm). A subsequent W etch back process is applied for W plug formation.

The lateral electrical connection of the metallized interchip via with the uppermost metal level of the top wafer was realized by opening contact windows on the top wafer followed by a standard TiN/AlSiCu metallization resulting in a 3D metallization of the wafer stack. According to standard IC technologies, the VIC wafer is finally passivated and the bond pads are opened. Fig. 3 shows the schematic cross section of the fully processed VIC.

The requirements on the metallization processes include the void-free filling of vias with extreme aspect ratios in the range of 5 to 10. Due to the underlying aluminum metallization, the interchip via metallization process temperatures have to be kept below

450°C. Therefore, we chose a metallization scheme based on CVD processes. In this scheme we use CVD-tungsten plugs with a CVD-titanium nitride glue layer and PVD-aluminum interconnects.

In order to deposit TiN films with a good step coverage at high aspect ratios, we used a CVD process by the thermal decomposition of the metalorganic precursor TDMAT ( $\text{Ti}[\text{N}(\text{CH}_3)_2]_4$ ) reactor [7]. The process developed allows the deposition of films with an excellent step coverage at a wafer temperature of 390°C. Due to the deposition mechanism, the films contain about 25 at% carbon as incorporated hydrocarbons leading to a relatively high electrical resistivity [8]. Films measured after contact to air show a specific resistivity of about 4500  $\mu\text{Wcm}$ . Without air exposure the resistivity is significantly lower. Thus this resistivity increase due to oxidation was avoided by in situ processing using TiN- and W-CVD process chambers mounted on the same mainframe. In this setup, the titanium nitride film is kept under vacuum prior to tungsten deposition. The amorphous microstructure of the films yields good barrier performance [9] which allows the use of films with thicknesses down to 20 nm. In the case of interchip vias, the contact is formed on the TiN capping layer of the bottom wafer's topmost metal level after passivation opening.

In order to use standard CMOS metallization processes we chose tungsten CVD for the interchip via fill. However, standard W-CVD processes show insufficient step coverages to fill our extreme aspect ratios void free with metal. Thus we modified a standard process to meet our demands [10]. The process is based on the thermal reduction of  $\text{WF}_6$  by  $\text{H}_2$  at wafer temperatures below 450°C. The reaction has to be operated in the surface activated regime to achieve adequate step coverage. The key parameters for the selection of this process regime are a sufficiently high  $\text{WF}_6$  flow rate and a sufficiently low substrate temperature. Prior to the main deposition, a nucleation layer must be grown in order to promote film growth on the TiN glue layer. Although only a few tens of nm in thickness, this layer needs to show a sufficiently high step coverage as well. Otherwise, the nucleation layer would be too thin in the bottom region of the interchip via, and the growth of the main layer would be delayed there resulting in a keyhole in the W plug. In conventional via fill applications, the nucleation layer is formed by reduction of  $\text{WF}_6$  with an  $\text{SiH}_4/\text{H}_2$  mixture. In contrast to the main deposition, the  $\text{WF}_6$  flow rate must be kept low to avoid  $\text{WF}_6$  attack of the contact in case of a diffusion barrier failure. A distinct improvement of the step coverage for our process was found by omitting  $\text{H}_2$  from the reaction gas mixture. The resulting films show properties comparable to those for standard via fill applications as they have a specific resistivity of 10  $\mu\text{Wcm}$  and a tensile stress of 1 GPa. Fig. 7 shows the SEM cross section of a VIC wafer stack after W plug formation.



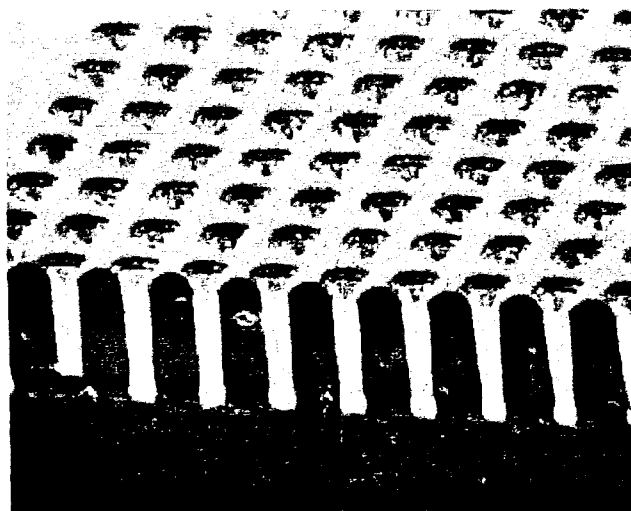


Fig. 7: SEM test structure showing an array of ICVs after via metallization and W etch back. The W-plug at the left side has no contact to the bottom wafer metallization due to a local defect.

#### Electrical and thermal measurements

We performed measurements of electrical conductivities on test structures of interchip vias. The contact resistances obtained and the theoretically calculated values versus the diameter of ICVs with square areas are shown in Fig. 9. The interchip vias were filled with a 200 nm  $\text{O}_3/\text{TEOS-SiO}_2$  spacer, 25 nm MOCVD-TiN and 900 nm CVD-W. The theoretical values for the contact resistance are calculated with specific resistivities of  $3000 \mu\Omega\text{cm}$  and  $10 \mu\Omega\text{cm}$  for TiN and W respectively. The obtained contact resistances for the  $14 \mu\text{m}$  deep interchip vias were, e. g.  $2 \Omega$  for  $2 \times 2 \mu\text{m}^2$  and  $4 \Omega$  for  $1.4 \times 1.4 \mu\text{m}^2$ .

A theoretical and practical thermal analysis was conducted to investigate possible limitations for VIC applications [11]. Fig. 10 shows the permissible range of the power density generated on individual chip layers as a function of the number of chip layers in the stack. The permissible maximum temperature rise of the VIC over ambient is  $50^\circ\text{C}$  and the chip is housed in a high performance PGA package. The temperature difference inside the VIC was accounted for on the basis of a 1-D thermal model and experimentally determined thermal parameters of VICs. It is found that the permissible power density per chip layer decreases only slightly more than proportional with the number of chip layers, since the thermal resistance inside the VIC is small in comparison with that of the package. Fig. 10 shows that the maximum permissible power density per chip layer is  $12 \text{ W/cm}^2$  in case of 2 chip layers and  $1.5 \text{ W/cm}^2$  for 15 chip layers. Our investigations show that, from the thermal point of view, the Vertical Integration of Circuits can be employed for a wide range of applications.

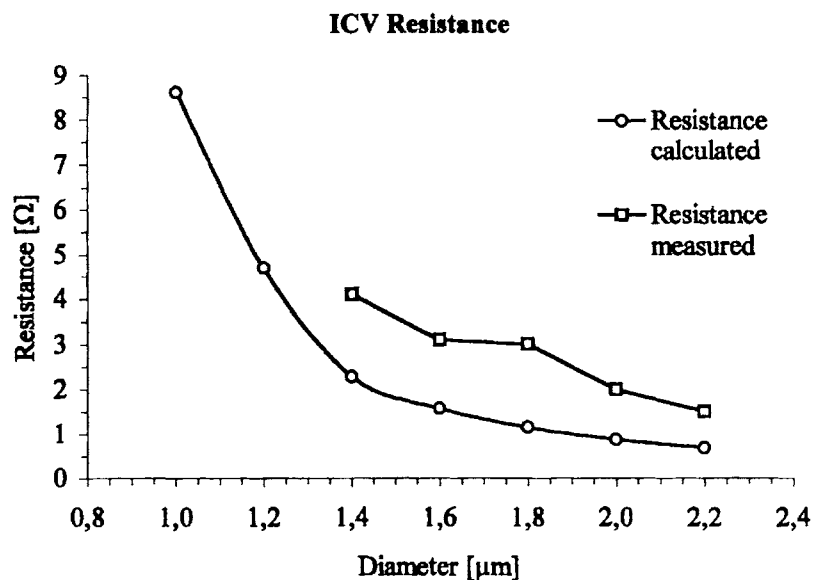


Fig. 8: Contact resistance versus interchip diameter of a VIC-stack (measured and theoretically calculated). The interchip vias are 14  $\mu\text{m}$  deep and filled with CVD-plugs (200 nm  $\text{SiO}_2$  spacers, 25 nm MOCVD-TiN).

### CONCLUSION

A CMOS-compatible process technology for the realization of Vertically Integrated Circuits was developed. The three dimensional metallization technique results in low ohmic contact resistances comparable to conventional multilevel metallization. In conclusion, we have developed a new 3D integration technology which is attractive for a great variety of applications.

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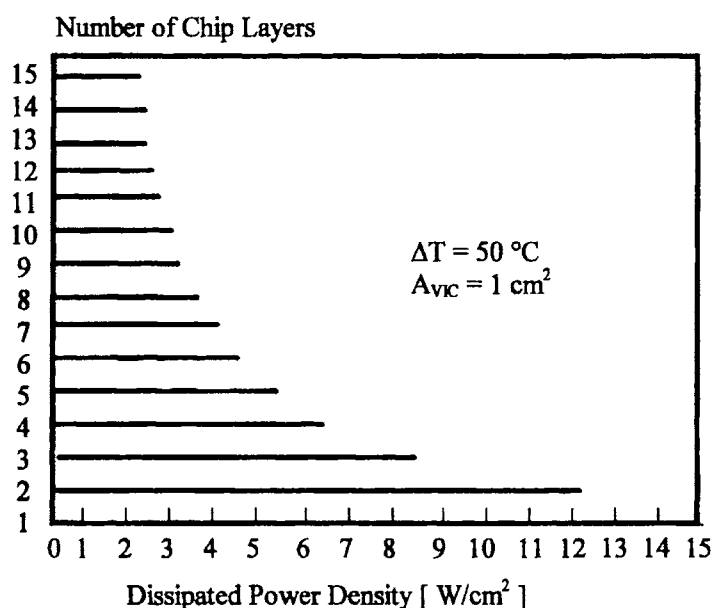


Fig. 9: Range of permissible power density as a function of the number of chip layers in the VIC stack.  $\Delta T$  is the maximum permissible temperature increase of the top chiplayer against ambient.  $A_{vic}$  is the area of the vertical integrated circuit.

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## EXHIBIT F



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(as of 3-1-10)

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I work for a Dutch startup company involved in the development of so-called HBr flow batteries. For our website, I would like to use a graph from the publication "Journal of The Electrochemical Society, 159 (11) A1806-A1815 (2012)".

Can you allow me to use this graph, with the purpose of explaining the fundamental working principles of HBr flow batteries ?

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According to Kathy MacDonald at Cummings, when an issue is printed and bound, they mail it out and ship out the copies and immediately close the ticket. It is the date that the ticket is closed that is sent to the Library of Congress to use as the first available date. It's best to check with Cummings for the date if we have not received any notification yet from the LOC.

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## **Requests for Permission for Summer Fellowship Reports**

as per MEY, email 8/31/15:

Given the summer fellowship reports are only 1-2 pages, the author would have to substantially add to the report to be acceptable as a journal paper for us. If submitting to us, the author should reference the Interface article. If the author wishes to submit to another journal, he/she should ask permission of ECS, because what he/she submits could be, say 80% of what was published in Interface. We would allow it, with proper attribution; however it's likely that the other journal will not accept it. And the author, upon submitting to another journal, should indicate that the material ( and how much) was published elsewhere.

. I assume the author will have to allow ECS to publish the report before the journal article can be published. That is my understanding of our transfer of copyright form. Do you agree?

Correct

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MEY: They are essentially one and the same, so go ahead and give permission. We should also review the MA transfer of copyright.



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As per Mary on 11-4-13:

Hi Annie: The latter part of your e-mail is exactly right. This is the part of the copyright transfer that covers institutional repositories. Mary

I'm still a bit fuzzy on requests to include ECS papers in institutional repositories. Up until now, I have been saying, "ECS does not grant permission for articles published by ECS to be deposited into any institutional repository and made available on an open access basis. ECS will be re-evaluating this issue in the future and may change its policy."

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Posting a PV paper in an IR:

Hi Logan,

Back in the days of PVs we didn't have a strict copyright transfer that spelled out requirements. (I spoke to Mary and we question if there was any copyright agreement that authors signed.) At this point in time, it would be fine to grant permission to the current request with only item #3 from below as the requirement. It will be interesting to see what they do end up posting, if it is just a scanned PDF of the article, of if they do some OCR'ing of the file.

I hope this helps.

-Annie

**From:** Logan Streu

**Sent:** Thursday, November 30, 2017 9:39 AM

**To:** Ann Goedkoop <[Ann.Goodkoop@electrochem.org](mailto:Ann.Goodkoop@electrochem.org)>

**Subject:** FW: Author request to self-archive in an institutional repository

Hey Annie,

We received a request (below) to include a PV article in an institutional repository. I know we allow this provided that the ECS-formatted PDF is not used, but I'm not sure how this would work for a PV article since there's no digital version. This is what I would normally send for a request to self-archive an article:

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Could you please help me with a rewrite that would work better for PVs? i.e. what version can they use, and where (if anywhere) should they link back to?

Thanks in advance for your help!

-Logan

**From:** Richard Dinapoli [<mailto:drichard@sas.upenn.edu>]

**Sent:** Wednesday, November 29, 2017 4:47 PM

**To:** Copyright <[copyright@electrochem.org](mailto:copyright@electrochem.org)>

**Cc:** [kenwhi@upenn.edu](mailto:kenwhi@upenn.edu)

**Subject:** Author request to self-archive in an institutional repository

To whom it may concern:

I am writing on behalf of Dr. Vohs, one of our faculty members at the University of Pennsylvania. Dr. Vohs has requested to self-archive a chapter he wrote for *Solid Oxide Fuel Cells VII* in Penn's openly accessible institutional repository, ScholarlyCommons (<http://repository.upenn.edu>). I was unable to find anything related to this type of reuse for books on your website; would you allow Dr. Vohs to post his work to ScholarlyCommons?

Here is the citation for the work in question:

- Anodes for Direct Oxidation of Hydrocarbons in Solid Oxide Fuel Cells, S. Park, H. Kim, S. McIntosh, W. Worrell, R.J. Gorte, and J.M. Vohs, Solid Oxide Fuel Cells VII, edited by H. Yokakawa and S.C. Singhal, (2001) pp. 712-718.

Please feel free to contact me should you have any questions about this request or ScholarlyCommons. We would really love to include Dr. Vohs' work and thus preserve his contribution to Penn's scholarly community!

Best,

Richard DiNapoli

ScholarlyCommons Digital Publishing Assistant

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Richard DiNapoli

University of Pennsylvania | Class of 2019

Benjamin Franklin Scholar

Candidate for Bachelor of Arts in History and

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