

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner

Case IPR2019-00779
Patent 6,163,492

**PATENT OWNER PROMOS TECHNOLOGIES, INC.'S RESPONSE TO
PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

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I. INTRODUCTION.

Patent Owner ProMOS Technologies, Inc. hereby responds to Samsung's Petition for *Inter Partes* Review seeking cancellation of claims 14-19 of U.S. Patent No. 6,163,492 (Ex. 1001). Samsung's petition presented four grounds challenging the validity of these claims:

- 1) that Fu anticipates claims 14-19;
 - 2) that McAdams anticipates claims 14-19;
 - 3) that Fu in combination with Sugibayashi renders claims 14-19 obvious;
- and
- 4) that McAdams in combination with Sugibayashi renders claims 14-19 obvious. Pet. at 2-3.

The Board instituted trial on all four grounds. Paper 7 at 14, 17, 18.

None of the art relied upon by Samsung is sufficient to meet its burden to show that the challenged claims are invalid. Fu and McAdams do not anticipate the challenged claims, because neither of these references discloses a circuit that includes "a terminal T1 for providing a signal indicating a state of the programmable latch" when that term is properly construed. That phrase should be construed to mean: "a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch." Neither Fu nor McAdams discuss when the circuit is used with regard to

when it is programmed. Samsung cites Sugibayashi in its obviousness combinations for disclosure of a different claim element (constant non-ground voltage), and therefore the combination of Sugibayashi with Fu or McAdams does not cure the deficiencies in the primary references or otherwise render obvious the challenged claims.

Likewise, Fu and McAdams do not anticipate the challenged claims because they do not disclose a circuit that includes “a first terminal for receiving a constant non-ground voltage throughout operation of the latch.” This term, when properly construed, means “at all times during circuit operation without being disabled.” When so construed, neither Fu nor McAdams anticipate the challenge claims because they do not teach that the voltage is provided “without being disabled.” Samsung’s reliance on Sugibayashi also does not cure this deficiency because Sugibayashi is only relied on for the “constant non-ground voltage” aspect of the element, and indeed does not teach that the voltage is applied without being disabled.

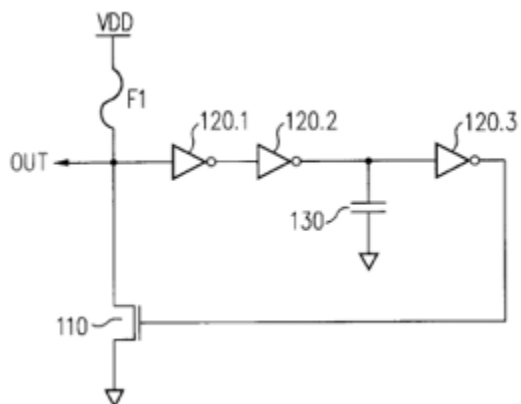
II. RELIEF REQUESTED.

The Board should conclude that Samsung has failed to meet its burden of proof to show that claims 14-19 are unpatentable for each of the instituted grounds.

III. OVERVIEW OF THE '492 PATENT.

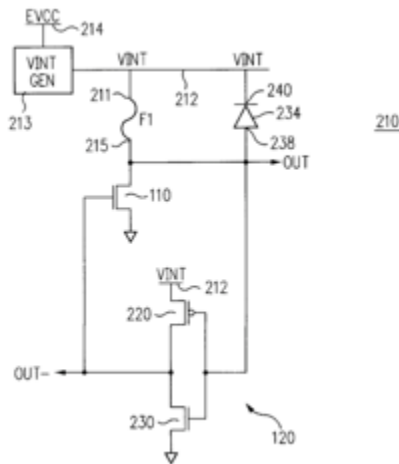
The '492 patent, titled “Programmable latches that include non-volatile programmable elements” was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



Ex. 1001 at Fig. 1.

One aspect of the invention, shown for example in figure 2A below, is that the fuse connects the power source VINT to the output node OUT, whose value is read to indicate the state of the latch.



Ex. 1001 at Fig. 2A.

The fuse is claimed as a “non-volatile programmable element,” and each of claims 1 and 14 require that, when conductive, it connects the claimed “first terminal” (power) to the claimed “terminal T1” (terminal indicating the state of the latch). Ex. 1001 at claims 1, 14. Because of this structure, the fuse directly indicates the state of the latch and is the only device which affects the output. Ex. 1001 at col. 2:22-27, 3:66-4:3.

The '492 invention solved a problem that occurs when the terminal OUT may indicate the wrong state before power is applied to the latch at VDD. Ex.

1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent:

when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal 'may tend to have its potential raised to a logic level '1'.' In addition, the terminal OUT potential may become 'unstable due to the capacitive coupling' in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown.

Id. at col. 1:38-47.

The '492 patent solves these problems by preventing the output node (terminal OUT) from floating above ground when power is off and from destabilizing through capacitive coupling during power up. Ex. 1001 at col. 1:36-47. In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node. *Id.*

One way the '492 patent solves this problem is to require that power be turned off after programming to allow any voltage that accumulated on the output node to dissipate. Ex. 1001 at col. 5:51-6:8. In this way, the risk of a false state caused by capacitive coupling or otherwise is eliminated.

Claim 14 is an exemplary claim that ensures that power is off after programming, using the term "a terminal T1 for providing a signal indicating a state of the programmable latch."

14. A programmable latch comprising:
a first terminal for receiving a constant non-ground Voltage throughout operation of the latch;
a second terminal for receiving a voltage;
a terminal T1 for providing a signal indicating a state of the programmable latch;
a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;
a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable impedance path having a control terminal for controlling the impedance of the variable-impedance path; and
an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the Variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

Ex. 1001 at Claim 14.

IV. PROMOS'S PROPOSED CLAIM CONSTRUCTIONS.

Samsung did not propose any constructions for the claims at issue. Pet. at 15-16.

ProMOS proposes a construction for two terms in claim 14:

- 1) “a terminal T1 for providing a signal indicating a state of the programmable latch;” and
- 2) “throughout operation of the latch.”

In this proceeding, claim construction uses the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); see 83 Fed. Reg. 51340-58 (Oct. 11, 2018).

- A. **“a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”**

Claim 14 includes the term “a terminal T1 for providing a signal indicating a state of the programmable latch.” This limitation should be construed as follows: “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” ProMOS explained that this should be the correct construction in its preliminary Patent Owner’s response.

In its institution decision, the Board did not adopt ProMOS's construction, and provided two reasons that ProMOS's construction was not appropriate on the existing record. Paper 7 at 8-10. First, the Board suggested that ProMOS's construction is incorrect because the term appears in both claims 1 (with a diode) and 14 (without a diode). *Id.* The Board assumed that ProMOS was arguing for a different constructions for the relevant term in the two different claims. Paper 7 at 9. Not so. Claim 1 addresses the stated "false state" problem with two solutions – a diode and "a terminal T1 from which voltage is dissipated after programming . . ." Ex. 1001 at 2:13-21, 2:38-50. In contrast, claim 14 recites a single solution to the problem – embodied in the limitation at issue. That is precisely what the specification states at Ex. 1001 at col. 5:51-6:8, quoted below, and there is no inconsistency.

Second, the Board concluded that ProMOS was seeking to read a specific embodiment into the claim, because the '492 patent discloses a number of embodiments. Paper 7 at 9-10. But as discussed below, terminal T1 must be at ground voltage before power is applied to the circuit because otherwise the element "a terminal T1 for providing a signal indicating a state of the programmable latch" would not be met – the terminal T1 in that case would indicate the wrong state, which is the very problem that the '492 patent is trying to solve.

As explained in ProMOS’s preliminary response, and as set forth below, ProMOS’s proposed construction is supported by the intrinsic record. In particular, the concept that power to the latch is off between programming and use, is necessary because otherwise the terminal will not “indicate[] a state of the programmable latch.” That is, a terminal that does not operate in this way will suffer from the risk of false output that was discussed in the background of the patent. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2003 at ¶24; see e.g., *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1315 (Fed. Cir. 2017) (interpreting an apparatus claim with “presents,” “receives,” and “generates” terms as requiring “capability of the structure” or the “particular capabilities” of the structure) (citing *UltimatePointer, LLC v. Nintendo Co.*, 73 F. Supp. 3d 1305, 1308 (W.D. Wash. 2014)).

The background of the ’492 patent explains that the entire purpose of the invention is to eliminate the risk of a false output because of excess voltage at T1 accumulated from programming or from capacitive coupling at the output. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2003 at ¶24. If this voltage is not dissipated after programming, then the terminal T1 will not necessarily indicate the state of the latch because it may indicate a false state due to this programming voltage. Ex. 2003 at ¶24. Therefore, in order for the terminal T1 to “indicate[] a state of the

programmable latch” as claimed, power must be turned off to allow voltage to dissipate from the output node after programming.

The specification goes on to explain that in the embodiments without a diode (for example claim 14) power must be turned off after programming:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at

zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

Thus, this term should be given ProMOS’s proposed construction.

B. “throughout operation of the latch” means “at all times during circuit operation without being disabled.”

Claim 14 recites “a first terminal for receiving a constant non-ground voltage throughout operation of the latch.” The term “throughout operation of the latch” should be construed to mean “at all times during circuit operation without being disabled.” Ex. 2003 at ¶¶27-29.

This construction is consistent with the specification’s use of the term:

“In some embodiments, the synchronous DRAM includes several generators 213. Each generator is enabled by its own signal EN. Thus, selective generators 213 can be disabled to reduce power consumption (in stand-by mode, for example). However, at least one generator 213 is enabled throughout the circuit operation in order to power circuits that are never disabled, for example, the buffer 386. Hence, the VINT voltage is a constant value throughout the operation of the integrated circuit.”

Ex. 1001 at col. 4:66-5:7 (emphasis added).

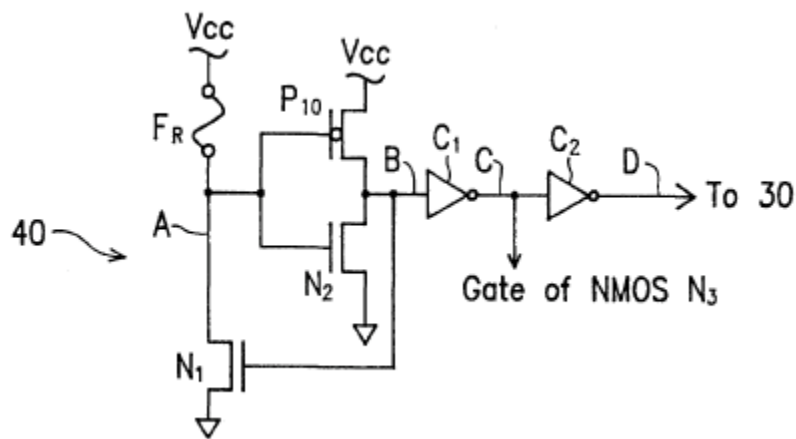
The above paragraph is the only use of the term “throughout operation of the latch” in the specification, and explains that the VINT voltage is supplied without being disabled, for use by circuits that are always operational. Ex. 2003 at ¶¶27-

29. Thus, this claim term “throughout operation of the latch” should be construed to mean “at all times during circuit operation without being disabled.”

V. THE PRIOR ART.

A. Fu

Fu describes a memory redundancy apparatus used for replacing defective memory cells. However, Fu is not directed at reducing false-state transitions and is not directed at problems associated with capacitive coupling or floating voltage increases at the output. Rather, Fu is a circuit aimed at power savings when not in use. Ex. 1005 at col. 1:11-13. Fu Fig. 4 is illustrative and is set forth below:



Ex. 1005 at Fig. 4.

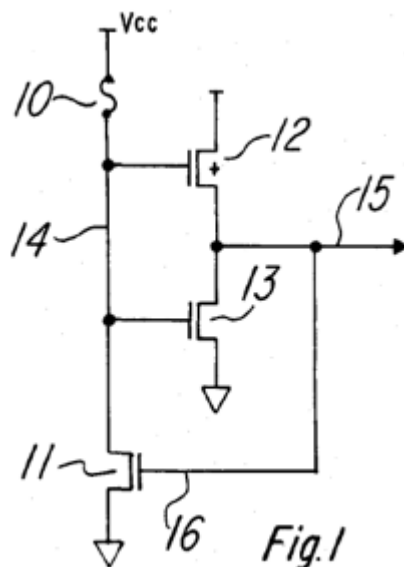
In the above figure, the W/L ratio of N1 is much larger than N2, and this maintains a low voltage at node A and a high voltage at node B, without any electric power consumption. Ex. 1005 at col. 4:35-44. Fu talks about programming the fuse (*Id.* at col 1:57-62), but does not discuss the operation of the

latch, and specifically does not disclose when programming is done with respect to run-time of the latch. Ex. 2003 at ¶33.

Further, Fu discloses a voltage VCC but does not state that the clock is provided at all times to the latch, without being disabled.

B. McAdams

McAdams teaches a fuse circuit for selecting a new memory cell where one is defective. According to McAdams, less power is consumed using its Figure 1 circuit because of feedback transistor 11, which is connected to the output of inverter 12/13.



Ex. 1006 at Fig. 1.

The McAdams circuit above does not discuss operation of the latch at all. More specifically, McAdams does not specify when the latch is operated with

respect to programming and whether power is turned off in order to allow voltage to dissipate after programming. Ex. 1006; Ex. 2003 at ¶39.

Further, McAdams discloses a voltage VCC but does not state that the clock is provided at all times to the latch, without being disabled.

C. Sugibayashi

Sugibayashi teaches a voltage generator circuit for addressing so-called voltage overshoot, shown in Figure 4. Ex. 1011 at col. 3:1-32.

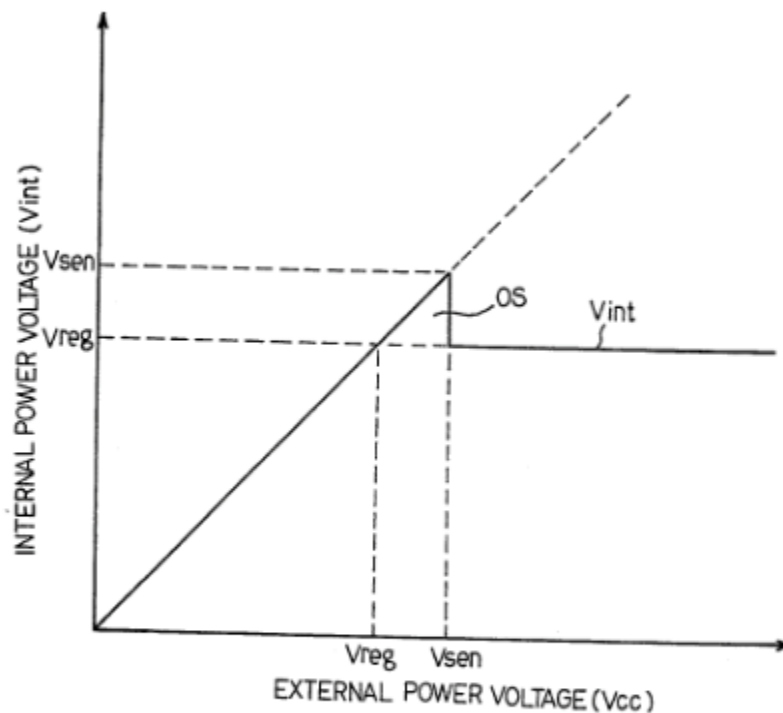


Fig. 4
PRIOR ART

Ex. 1011 at Fig. 4.

In order to prevent any overshoot, Sugibayashi discloses the voltage generation circuitry in Figure 5, which uses a voltage detecting circuit shown in Figure 6.

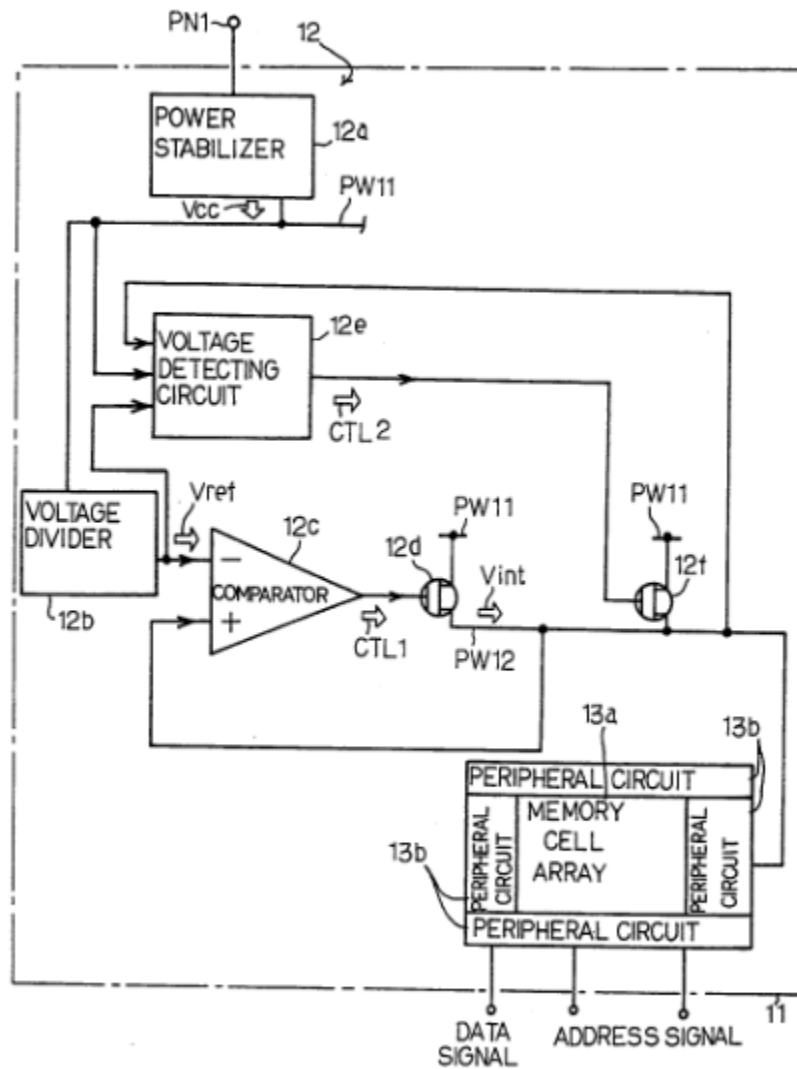


Fig. 5

Ex. 1011 at Fig. 5.

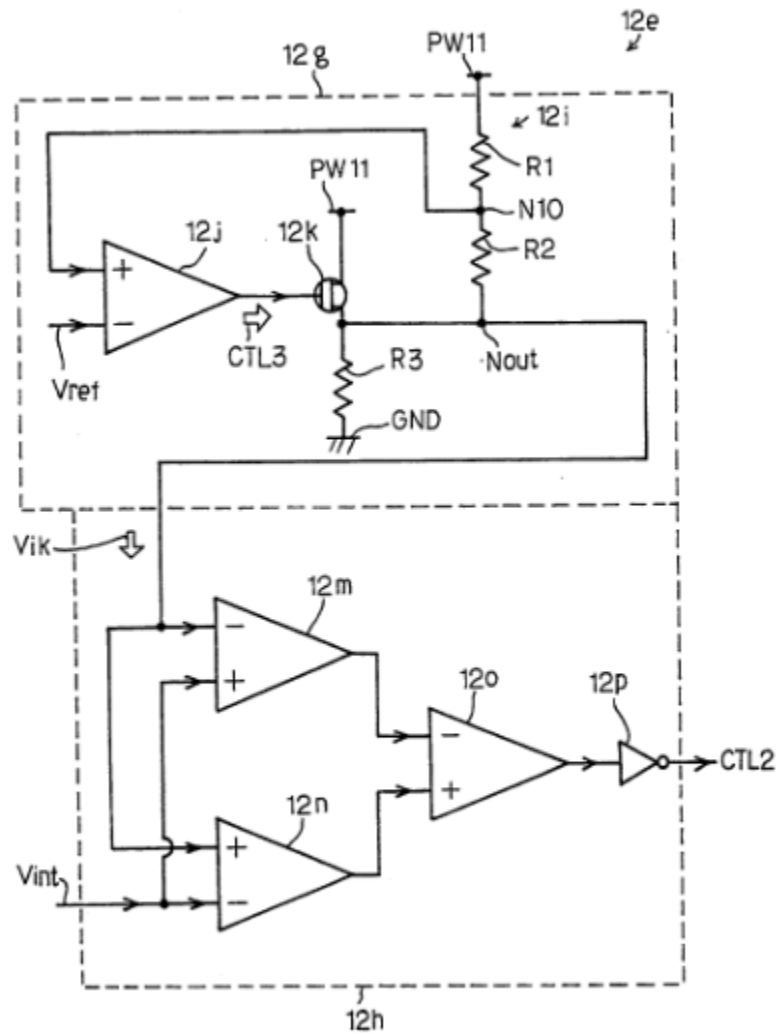


Fig. 6

Ex. 1011 at Fig. 6.

Sugibayashi purports to provide the advantage of limiting the high voltage level to the target voltage (the problem depicted in figure 4), but does not teach how the generator would be used, and in particular whether it would be used in

conjunction with an enable/disable circuit (as typical for voltage generators, Ex. 2003 at ¶46) or whether it would always be active.

VI. INVALIDITY ANALYSIS.

A. Fu Does Not Anticipate Claims 14-19.

To anticipate a claim, a single prior art reference must disclose each limitation of the challenged claims. *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Fu does not anticipate the challenged claims for two reasons: 1) it does not disclose a structure that meets the proper construction of following limitation: “a terminal T1 for providing a signal indicating a state of the programmable latch;” and 2) it does not disclose that power VCC is provided “throughout operation of the latch.”

Fu does not teach any mechanism for dissipating voltage from its internal nodes, and further does not describe the operation of its latch. Therefore, there is no teaching that any voltage buildup at the internal nodes is dissipated *before operation*, as required by a proper construction of this term. Ex. 2003 at ¶33. Thus, the Fu circuit fails to cure the problem that the '492 invention solved – the latch may indicate the wrong state during power up. *Id.* Accordingly, Fu does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Further, Fu is silent as to when the voltage VCC is provided to the latch, and specifically does not teach that VCC is provided without being disabled, as required by a proper construction of the term. Ex. 2003 at ¶35. Samsung cites 4:64-5:6 (during “operation of the memory redundancy circuit 2 . . .”) as its only support for this element, but this passage does not mean that the signal is provided “throughout operation of the latch,” or at all times “without being disabled.” Ex. 2003 at ¶35. Therefore, there is no teaching that the voltage VCC is used without an enable signal, as required by ProMOS’s construction. Ex 1001 at 4:66-5:7. The claim element “receiving a constant non-ground voltage throughout operation of the latch” is therefore missing from Fu.

B. McAdams Does Not Anticipate Claims 14-19.

McAdams also does not anticipate claims 14-19 for two reasons: 1) it does not disclose a structure that meets the proper construction of following limitation: “a terminal T1 for providing a signal indicating a state of the programmable latch”; and 2) it does not disclose that power VCC is provided “throughout operation of the latch.”

McAdams does not state that voltage that accumulates on nodes 14 and 15 is dissipated after programming. Ex. 2003 at ¶39; Ex. 1006 generally. The capacitive coupling downstream from this circuit in McAdams allows the floating node 15 to stray far from its initialization state, and absent any teaching that the

latch is programmed and left unpowered before being read, the McAdams circuit suffers from this capacitive coupling. *Id.* McAdams is silent about whether power is turned off after programming in order to allow power to dissipate, and therefore does not meet the proper construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Further, McAdams is silent as to when the voltage VCC is provided to the latch, and specifically does not teach that VCC is provided without being disabled, as required by a proper construction of the term. Ex. 2003 at ¶41. Therefore, there is no teaching that the voltage VCC is used without an enable signal, as required by ProMOS’s construction. Ex 1001 at 4:66-5:7. The claim element “receiving a constant non-ground voltage throughout operation of the latch” is therefore missing from McAdams.

C. Fu and Sugibayashi Do Not Render Obvious Claims 14-19.

Samsung, in its third proposed grounds, argues that the combination of Fu and Sugibayashi renders the challenged claims obvious under 35 U.S.C. §103. Samsung relies on the Sugibayashi reference only for the element containing the language “constant non-ground voltage.” Pet. at 71-81. The combination of Sugibayashi with Fu, therefore does nothing to cure the fact that Fu does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Regarding the claim element “throughout operation of the latch” which is missing from Fu, discussed above, Sugibayashi is not cited by Samsung as satisfying that language and indeed does not teach that the voltage generator output would be provided to a latch circuit at all times without being disabled. Ex. 2003 at ¶¶45-46.

The combination of references does not disclose or suggest the claimed invention, including this limitation, and therefore the challenged claims are not invalid as obvious.

D. McAdams and Sugibayashi Do Not Render Obvious Claims 14-19.

Samsung, in its fourth proposed grounds, argues that the combination of McAdams and Sugibayashi renders the challenged claims obvious under 35 U.S.C. §103. As with the combination with Fu, discussed above, Samsung cites the Sugibayashi reference only for the element containing the language “constant non-ground voltage.” Pet. at 82-87. The Sugibayashi reference therefore does nothing to cure the fact that McAdams does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Regarding the claim element “throughout operation of the latch,” as with Fu above, Sugibayashi is not cited by Samsung as satisfying that language and indeed does not teach that the voltage generator output would be provided to a latch circuit at all times without being disabled. Ex. 2003 at ¶¶45-46.

Accordingly, the combined references do not render the challenged claims obvious.

VII. CONCLUSION.

For the reasons set forth above, the Board should issue a final written decision that challenged claims 14-19 are patentable over Fu, McAdams, and Sugibayashi.

Dated: December 5, 2019

Respectfully submitted,

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APPENDIX OF EXHIBITS

Exhibit No.	Description
2001	Declaration of Erik de la Iglesia in Support of Patent Owner ProMOS Technologies, Inc.'s Preliminary Response
2002	Exhibit marked at the Deposition of Dr. Baker, October 25, 2019
2003	Declaration of Erik de la Iglesia in Support of Patent Owner ProMOS Technologies, Inc.'s Response to Petition
2004	Deposition Transcript of R. Jacob Baker, Ph.D., P.E., October 25, 2019

CERTIFICATE OF SERVICE

I hereby certify that on December 5, 2019, a true and correct copy of the foregoing *Patent Owner ProMOS Technologies, Inc.'s Response to Petition for Inter Partes Review of United States Patent No. 6,163,492* and all supporting exhibits were served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

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**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION REQUIREMENTS**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned attorney of record, hereby
certifies that:

This brief complies with the type-volume limitation of 37 C.F.R. § 42.24(b).
The brief contains 3,606 words, excluding the parts of the brief exempted by 37
C.F.R. § 42.24.

Date: December 5, 2019

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