

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,163,492

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,163,492**

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 6,163,492 (“the ’492 patent”) (Ex. 1001).¹

2. I am being compensated at a rate of \$615/hour for my work in this proceeding.

3. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

4. I have been asked to consider whether certain references disclose or suggest the features recited in claims 14-19 of the ’492 patent. My opinions are set forth below.

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’492 patent.

II. BACKGROUND AND QUALIFICATIONS

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding circuit design and memory devices referenced in this declaration.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

8. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

9. As described in my CV, I am a licensed Professional Engineer in the state of Idaho and have more than 30 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of flash memory while at Micron. My efforts resulted in more than a dozen flash memory-related patents. Among other experiences, I led development of the delay-locked loop (DLL) in the late 90's so that Micron products could transition to the DDR memory standard. I have worked as a consultant at other companies designing memory chips, including Sun, Oracle, and Contour Semiconductor. I also worked on the design of CISs and memory as a consultant for OmniVision.

10. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, and fiber optics. As a professor, I have been the main advisor to over 85 Master's and Doctoral students.

11. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on 149 granted U.S. patents in integrated circuit designs including flash memory and DRAM.

12. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

13. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

14. I have received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award the four years I have been at UNLV.

15. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

16. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding circuits, including fuse-based circuits used in memory devices.

17. In forming my opinions expressed in this Declaration, I reviewed the '492 patent (Ex. 1001), the prosecution file history for the '492 patent (Ex. 1004); U.S. Patent No. 5,457,656 ("Fu") (Ex. 1005); U.S. Patent No. 4,621,346 ("McAdams") (Ex. 1006); U.S. Patent No. 5,373,477 ("Sugibayashi") (Ex. 1011); U.S. Patent No. 5,592,121 ("Jung") (Ex. 1012); Taur *et al.*, Fundamentals of Modern VLSI Devices, 2009 ("Taur") (Ex. 1015); and any other materials I refer to in this Declaration in support of my opinions.

18. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '492 patent at the

time of the alleged invention, which I have been asked to initially consider was the mid-to-late 1990s (including October 23, 1998, the filing date of U.S. Application No. 09/178,445 (“the ’445 application”) that matured into the ’492 patent). My opinions reflect how one of ordinary skill in the art would have understood the ’492 patent, the prior art to the ’492 patent, and the state of the art at the time of the alleged invention.

19. Based on my experience and expertise, it is my opinion that certain references disclose or suggest all the features recited in claims 14-19 (“challenged claims”) of the ’492 patent, as I discuss in detail below.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the ’492 patent as of what I understand is the filing date of October 23, 1998 for the ’445 application. Specifically, based on my review of the ’492 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in art would have had would have had a B.S. degree in electrical engineering, or equivalent thereof, and at least two to three years of experience in integrated circuit

design. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and become familiar with the prior and current solutions to those problems.

21. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe, i.e., mid-to-late 1990s, including the time preceding the '445 application filing date of October 23, 1998.

V. TECHNICAL BACKGROUND

22. In this section, I present a brief overview of basic circuit concepts that will assist in better understanding the '492 patent and the prior art that I discuss in this declaration. In particular, I cover below the operation of a metal-oxide semiconductor field-effect transistor (MOSFET or MOS transistor), which is the building block of the circuits described in the '492 patent and the prior art.

A. MOSFET

23. A metal oxide semiconductor field effect transistor (MOSFET) was a well-known building block of circuits in various applications long before the alleged time of the invention. In fact, MOSFETs have been known since at least as

early as 1960, *i.e.*, decades before the alleged invention of the '492 patent. As an example, Taur explains some of the known characteristics of MOSFETs. (*See, e.g., Ex. 1015 at 2.*)²

24. The MOSFET was known to be a four-terminal device with the terminals designated as gate, source, drain, and substrate (substrate is sometimes referred to as a body). The substrate was typically a silicon substrate. Although pure silicon is a poor conductor, the electrical conductivity of silicon was known to be increased by introducing impurity atoms, or dopants, into the silicon. Silicon material doped with p-type dopants is called p-type silicon, and silicon material doped with n-type dopants is called n-type silicon. Taur provides an example of the basic structure of a MOSFET in figure 3.1, where the basic structure includes a

² My understanding of such background MOSFET technologies is based on my experience and knowledge, and my reference to Taur is only for exemplary purposes. Taur was published in 2009, and based on my experience and knowledge, the disclosure of MOSFET technologies in Taur that I refer to in this declaration is consistent with what one of ordinary skill in the art would have understood regarding such technologies in the mid-to-late 1990s.

p-type silicon substrate and n-type source and drain regions that are each heavily doped compared to the substrate.

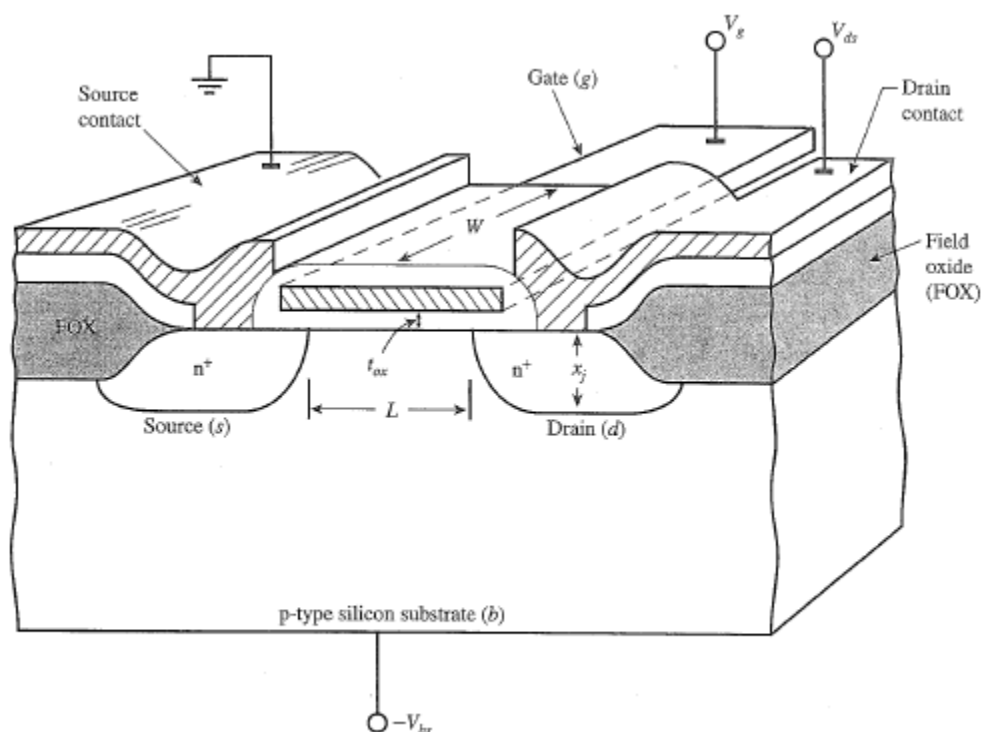


FIGURE 3.1. Three-dimensional view of basic MOSFET device structure. (After Arora, 1993.)

(*Id.* at 149, FIG. 3.1) The configuration shown in Figure 3.1 of Taur was consistent with the basic structure of such a configured MOSFET that one skilled in the art would have understood during the 1990s. (See, *e.g.*, reference to Arora 1993 below the figure).

25. In configurations where the source and drain regions are heavily n-doped, similar to the configuration shown in figure 3.1 above, the MOSFET was typically known as an n-channel MOSFET (or NMOSFET, NMOS transistor, or

simply NMOS). Another type of MOSFET was known as a p-channel MOSFET (or PMOSFET, PMOS transistor, or simply PMOS), in which the dopant types are reversed compared to those of an n-channel MOSFET as I described above (and exemplary shown in figure 3.1.) (*See also id.* at 148.)

B. MOSFET as a Switch

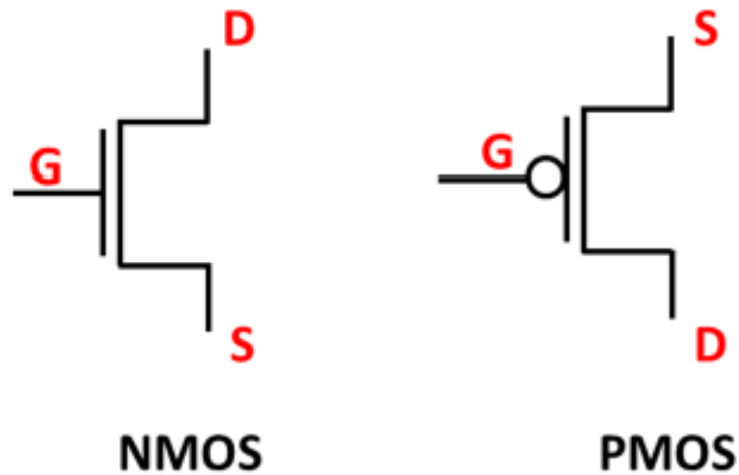
26. In a simplified configuration of a MOSFET in the mid-to-late 1990s (and still today), there was no current flow between the source and drain unless the voltage difference between gate and source terminals exceeds a threshold voltage. When a sufficiently large voltage (typically called the threshold voltage of the transistor or V_T) is applied between the gate and the source, the silicon surface between the source and drain is inverted to n-type, which forms a conductive n-channel between the source and drain. (*Id.*) Where a voltage difference existed between the source and drain, current would then flow between those terminals. In such circumstances, it was known that the MOSFET would operate like a switch and would conduct current depending on the $|V_{GS}|$ (magnitude of voltage between gate and source terminals).³ (*Id.*) For a PMOS, the current flows from source to

³ The MOSFET was also known to operate in what was known as the “subthreshold” region, where a very small amount of current is conducted by the

drain when the gate voltage is below the source voltage by the threshold voltage. On the contrary, for an NMOS, the current flows from drain to source when the gate voltage is greater than the source voltage by the threshold voltage.

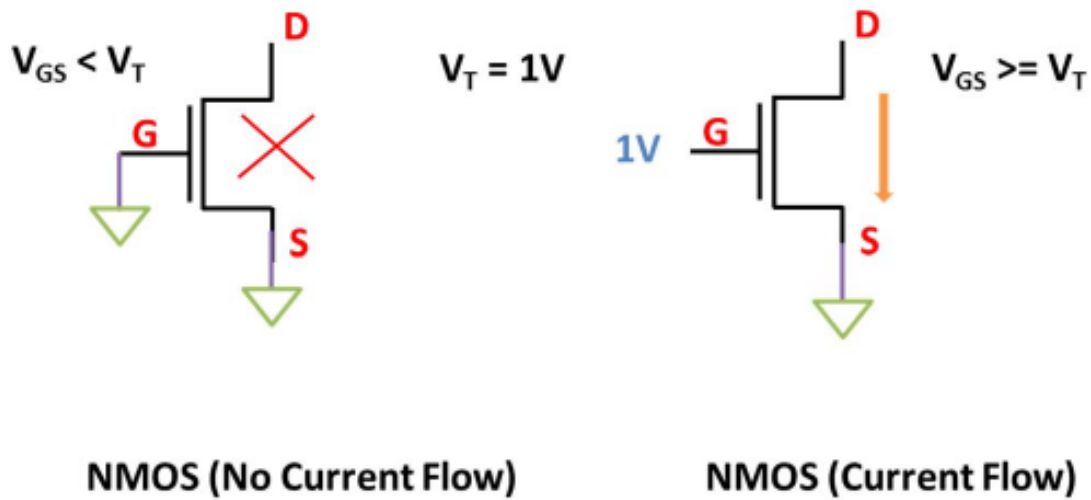
27. The following demonstratives illustrate the above basic concepts that were known to those skilled in the art in the 1998 timeframe. Demonstrative A illustrates the symbols that were commonly attributed to an NMOS and a PMOS in circuit designs at that time. The gate, drain, and source are respectively labeled G, D, and S in these demonstratives.

MOSFET because the gate-source voltage is lower than the threshold voltage. As a result, where the applied voltages result in the gate-source voltage being higher than the threshold voltage, the “sub-threshold” mode is not implicated in the operation of the MOSFET at that state.



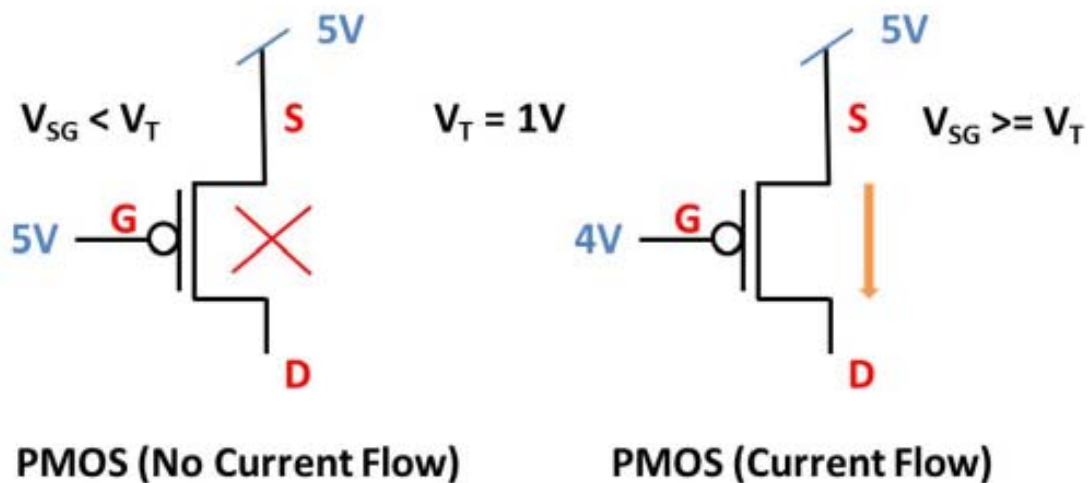
DEMONSTRATIVE A

28. Demonstrative B illustrates an NMOS with a threshold voltage of 1V and describes that when the gate to source voltage (V_{GS}) is less than 1V (*e.g.*, both gate and source are at ground (shown by the green triangles), no current flows through the NMOS (represented by the red “X”), but when the gate to source voltage is greater than or equal to the threshold voltage, current flows from drain to source (shown by the orange arrow).



DEMONSTRATIVE B

29. Demonstrative C similarly illustrates the operation of a PMOS with the difference being that for the PMOS, the gate voltage has to be lower than the source voltage for the PMOS to conduct current. That is, instead of V_{GS} being greater than or equal to V_T , the V_{SG} must be greater than or equal to V_T .



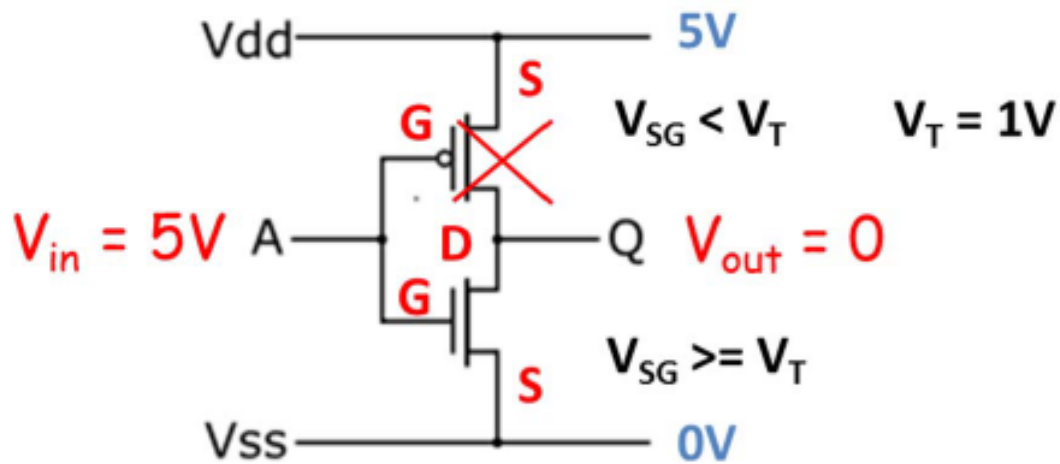
DEMONSTRATIVE C

30. A simple circuit example of an inverter brings together the above basic MOSFET concepts in a scenario using digital logic. It was well known long before the time of the alleged invention to use digital logic in various data processing contexts. For example, it was well known to represent data using two logic values—a logic HIGH (commonly designated ‘1’), and a logic LOW (commonly designated ‘0’). The two logic values HIGH (‘1’) and LOW (‘0’) were called logical complements of each other. A horizontal bar over a digital signal’s name was a common way to designate a logical complement, e.g., $\bar{X}$ would have been the logical complement of X. In the context of circuits, it was known to interpret a relatively low voltage (e.g., 0V) as a logic LOW, and to interpret a relatively high voltage (e.g., 5V) as a logic HIGH.

31. Various circuit devices were known for manipulating digital logic signals. For example, it was well known to use complementary metal oxide semiconductor (CMOS) technology for implementing logic gates that would manipulate such digital logic signals. The simplest example was an inverter, which performed the logic operation of inverting a logic value from LOW to HIGH (i.e., generate a ‘1’ at the output of the inverter when the input to the inverter is ‘0’) and from HIGH to LOW (i.e., generate a ‘0’ at the output of the inverter when

the input to the inverter is '1'). In other words, the output of the inverter had a logic value that was the logical complement of the input of the inverter.

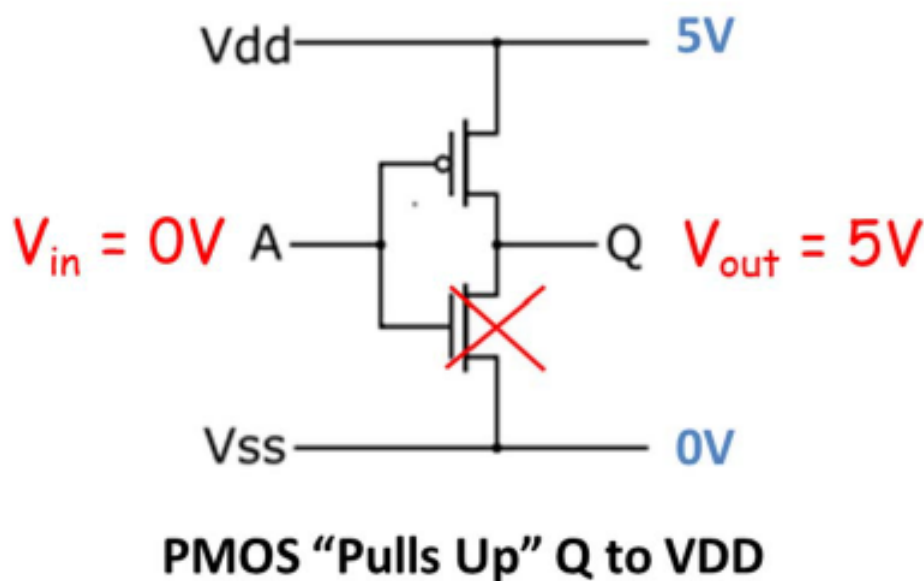
32. As shown below in demonstrative D, an inverter consists of a PMOS and NMOS in series with shared drain terminals. This configuration is consistent with what was known to one of ordinary skill in the art at the time of the alleged invention for the '492 patent. The source of the PMOS is at 5V (High) in this example and the source of the NMOS is at 0V (Low). It is assumed that the threshold voltage for both transistors is 1V. When an input voltage (V_{IN}) of 5V is provided to the gates of both the PMOS and the NMOS, the V_{SG} of the PMOS is 0V (less than V_T) and the V_{GS} of the NMOS is 5V (greater than V_T). Accordingly, the PMOS is turned OFF and the NMOS is turned ON. Because there is no current flowing through the PMOS, the NMOS will "pull down" the voltage at its drain terminal causing an output voltage (V_{OUT}) of 0V, and the NMOS in this configuration was referred to as a "pull-down transistor."



NMOS “Pulls Down” Q to VSS

DEMONSTRATIVE D

33. If, however, in the same example the input voltage is at 0V, the PMOS will turn ON, the NMOS will shut off, and, as a result, the PMOS will “pull up” the voltage at its drain to 5V causing an output voltage of the inverter circuit of 5V. The PMOS in this configuration was referred to as a “pull-up transistor.”



DEMONSTRATIVE E

34. I refer to these basic concepts of “pull up” and “pull down” when I explain the prior art below (see below at Sections VIII, IX).

35. The current-conducting capability of the MOSFET was known at that time to depend on the dimensions of the transistor, *i.e.*, width (W) and length (L). (See also Ex. 1015 at FIG. 3.1 (reproduced above)). It was known that when the MOSFET operates in the above-threshold region (*i.e.*, $|V_{GS}|^4$ is greater than the

⁴ I use the absolute value sign with V_{GS} (*i.e.*, gate-to-source voltage) because for a PMOS, the V_{SG} (*i.e.*, source-to-gate voltage) has to be greater than threshold for the PMOS to conduct current.

threshold voltage), for a given V_{DS} , the MOSFET current (i.e., the drain-source current or the source-drain current) is proportional to $|V_{GS}|$, i.e., a higher $|V_{GS}|$ results in a higher current through the MOSFET.

VI. OVERVIEW OF THE '492 PATENT

36. The '492 patent is entitled "Programmable Latches that Include Non-volatile Programmable Elements." (Ex. 1001, Cover.) Consistent with the title, the '492 patent relates to "programmable latches that include non-volatile programmable elements" where "[e]xamples of non-volatile programmable elements are fuses." (*Id.* at 1:15-17.)

37. As disclosed by the '492 patent, such programmable latches "are used in integrated circuits to enable modification of the circuits without changing the masks used for circuit fabrication." (*Id.* at 1:18-20.) For example, the '492 patent discloses that such programmable latches can be used for replacing defective memory cells with spare memory cells in semiconductor memories. (*Id.* at 1:20-22.) The '492 patent acknowledges that programmable latches using non-volatile programmable elements such as fuses were known in the art before the alleged invention disclosed in the '492 patent. (*Id.* at 1:24-54.)

38. Figure 1 of the '492 patent, replicated below, illustrates one prior art programmable latch that includes a “[f]use F1 connected between the power supply VDD and the latch output terminal OUT.” (*Id.* at 1:24-27.)

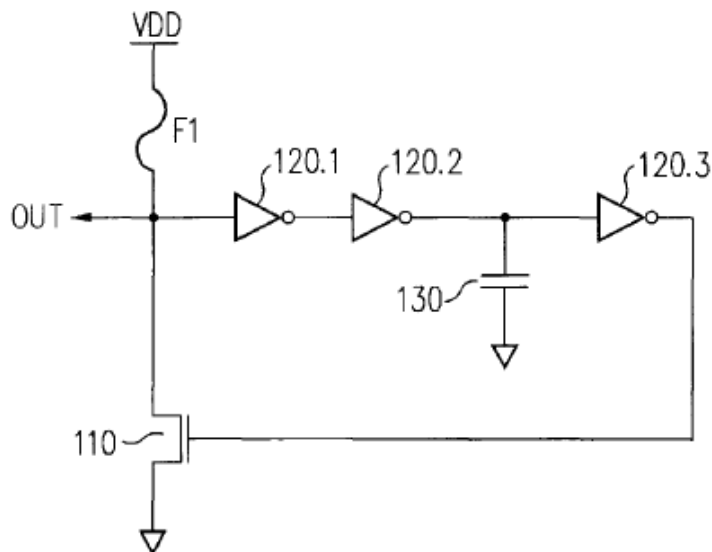


FIG. 1
(PRIOR ART)

(*Id.* at FIG. 1.)

39. The '492 patent describes the operation of the prior art latch circuit of figure 1 as follows:

If fuse F1 is intact, the terminal OUT is pulled to VDD. The inverters 120 keep transistor 110 off. If fuse F1 is blown, the terminal OUT is at the ground voltage. The inverters turn transistor 110 on to keep the terminal OUT at ground.

(*Id.* at 1:32-35.)

40. The '492 patent discloses that the capacitor 130 is included in the circuit of figure 1 above to ensure proper initialization when power is supplied to the circuit. (*Id.* at 1:36-54.) Specifically, the '492 patent, referring to the disclosure in U.S. Patent No. 4,546,455, indicates that a malfunction can occur on power up when the fuse is blown. Specifically, when power is off, transistor 110 is off and the node OUT is floating. (*Id.* at 1:38-40.) A person of ordinary skill in the art would have understood that a “floating” node is a node that is not being pulled to any particular voltage such as ground and that an indeterminate voltage can exist on that node. Because the node OUT is floating, there is a concern that OUT can inadvertently be raised to a logic “1” (High) by capacitive coupling or otherwise. (*Id.* at 1:40-44.)

41. If the fuse F1 is blown, when power is applied to the latch, if the OUT node, which has been floating while the power is off, is at a logic “1” due to charge accumulated on that node, the charge on OUT corresponding to the logic “1” (high) can keep the transistor 110 off. If transistor 110 is kept off, it prevents the charge on OUT from being drained away. (*Id.* at 1:44-46.) Therefore, even if the fuse has been blown, the output of the programmable latch, which should be logic “0” (low), may remain high. (*Id.* at 1:46-47.) According to the '492 patent, “[c]apacitor 130 is intended to avoid such malfunction” and “keeps the input of

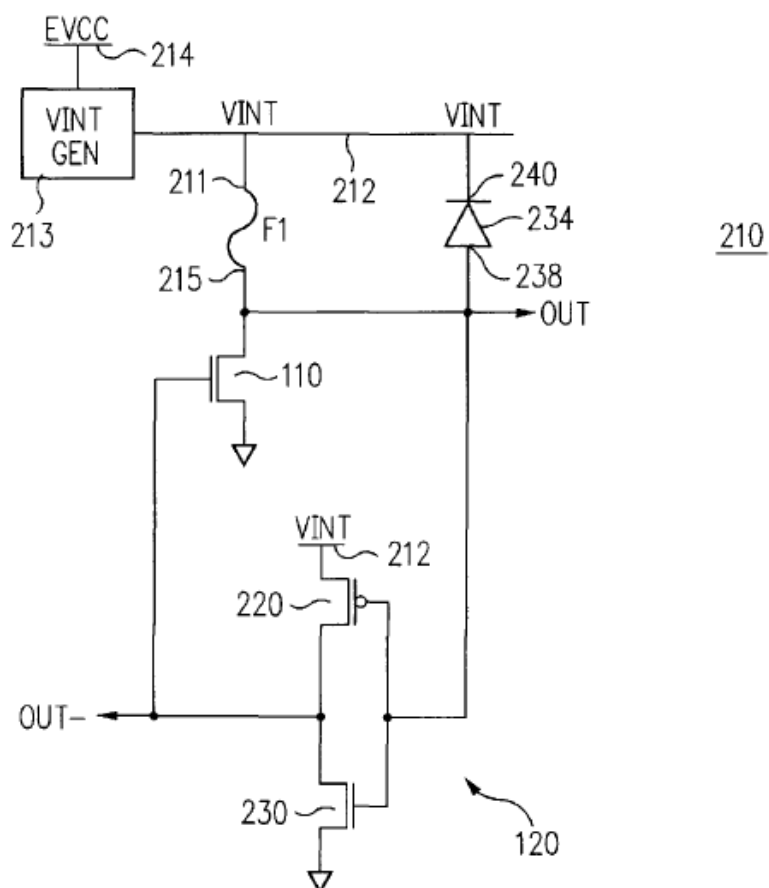
inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown” such that OUT properly reflects the state of the fuse F1. (*Id.* at 1:48-54.) According to the ’492 patent:

Prior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals.

(*Id.* at 2:22-26.)

42. The ’492 patent proposes an alternative programmable latch shown in figure 2A below. (*Id.* at 3:10-11.)

FIG. 2A



(*Id.* at FIG. 2A.)

43. The programmable latch shown in figure 2A above includes a fuse 211, an inverter 120 that includes transistors 220 and 230, and a transistor 110. (*Id.* at 3:10-33, FIG. 2A.) The programmable latch of figure 2A also includes a diode 234. (*Id.* at 3:33-35, “Diode 234 has its anode terminal 238 connected to terminal OUT and its cathode terminal 240 connected to the VINT terminal 212.”) As disclosed by the ’492 patent, the diode 234 holds the OUT node at a voltage not higher than a threshold voltage of the diode 234 when the VINT terminal is

ground. (*Id.* at 3:35-41, “When the power is off, the VINT terminal is at ground. . . . Therefore, the voltage on the terminal OUT is not higher than one threshold voltage of the diode 234.”)

44. The ’492 patent indicates that by maintaining the voltage on OUT low using the diode 234, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on and “connects the terminal OUT to ground,” resulting in a correct output. (*Id.* at 3:41-49.) This happens because terminal OUT is held “not higher than one threshold voltage of diode 234,” and at such a voltage, transistor 230 does not turn on because its threshold voltage (e.g., 1.2V) is greater than the threshold voltage of diode 234. (*Id.*) Per the ’492 patent, the latch can operate correctly even if the diode is omitted. (*Id.* at 5:51-6:7.)

45. The above features were well known as discussed below at Sections VIII and IX.

VII. CLAIM CONSTRUCTION

46. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is mid-to-late 1990s (including October 23, 1998, the filing date of the U.S. Application maturing into the ’492 patent). In considering the meaning of the claims, however,

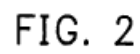
I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

VIII. OVERVIEW OF THE PRIOR ART

A. Fu

47. Fu relates to a “memory redundancy apparatus for replacing defective memory cells in a main memory cell array of a memory device.” (Ex. 1005 at Abstract.) As disclosed by Fu, because the density of memory devices is increasing, there is a higher probability of defects, where those defects can render a memory device useless and lower the manufacturing yield rate for the memory devices. (*Id.* at 1:17-22.) Fu indicates that on-chip redundant memory cells and their control logic are included on memory devices so that “devices with a limited number of defective memory cells can still be used as qualified memory devices, salvaging the device from otherwise being disposed of.” (*Id.* at 1:26-30.)

48. Figure 2 of Fu, reproduced below, illustrates memory redundancy circuitry 2, including a redundancy activation circuit 40. (*Id.* at 3:27-35, 3:47-48, FIG. 2.)



(*Id.* at FIG. 2.)

49. Fu discloses that the “redundancy activation circuit 40” shown in figure 2 is also depicted as a schematic diagram in figure 4, which is reproduced below. (*Id.* at 4:14-17, FIG. 4.)

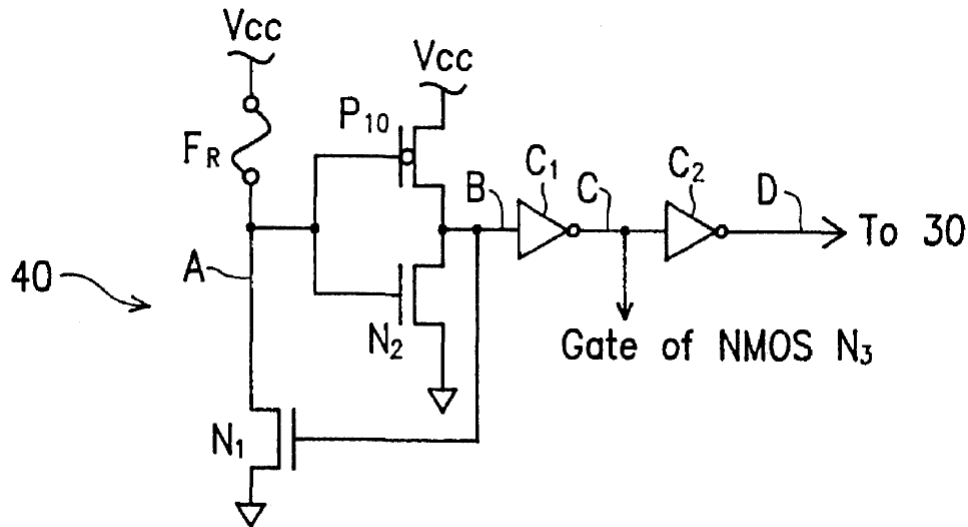


FIG. 4

(*Id.* at FIG. 4.)

50. In figure 4, “the fuse element F_R is connected in series with the NMOS transistor N₁, with the other end of fuse element tied to V_{CC}, and the transistor end tied to ground.” (*Id.* at 4:20-23.) When the redundancy activation circuit 40 of figure 4 is operational, the voltage at node A is influenced by the electrical potentials applied on the V_{CC} and GND terminals and the state of the fuse

F_R . Specifically, F_u describes the operation of the memory redundancy circuit as follows:

When the memory redundancy circuitry 2 of FIG. 2 is not selected, or in other words, not activated, to replace the defective memory cells utilizing the redundant memory cells in circuitry 2, the fuse element F_R is not blown. In this case, the potential of node A is at its high level (V_{CC}), and the NMOS transistor N_2 is in a conduction mode to pull node B to the GND potential. Meanwhile, the other NMOS transistor N_1 is maintained in non-conduction mode, helping to maintain the potential of node A at the high level. In this condition, the electric potential of node C is also at high level, making the third NMOS transistor N_3 go into a conduction mode, which in turn pulls the potential of node E to the GND potential. This inverts the redundancy activation status signal RD into a high level, indicating a non-activated status of the memory redundancy circuitry 2.

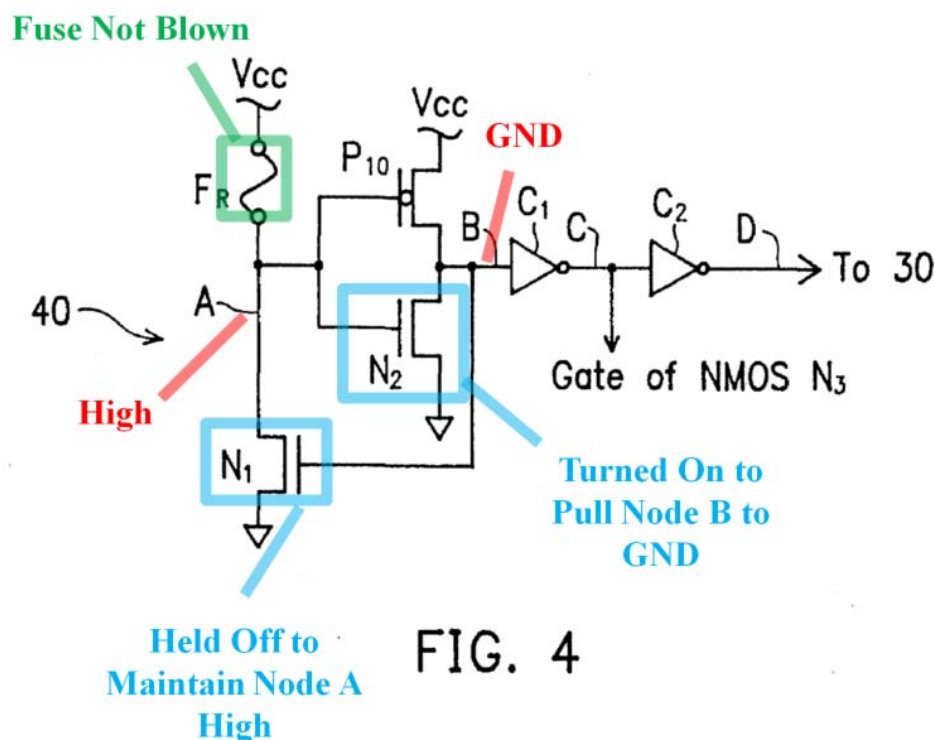
In addition, node D is at a low level, and as a result, the PMOS transistor TP_1 conducts, while the NMOS transistor TN_1 is not conducting, thereby blocking the signal path of the address signal X_1 .

On the other hand, when the memory redundancy circuitry 2 of FIG. 2 is selected and activated, the fuse element F_R is blown open. Each of the fuse elements F_i , say F_2 for example, of the decoder unit 32 in the programmable redundancy decoder logic that correspond to a defective memory cell in the main memory cell array are also blown. At this instant, node A is at a low electric potential, making the PMOS

transistor P_{10} conduct. The conduction of P_{10} brings node B to the high potential level, which also makes the NMOS transistor N_1 conducts, so that node A is ensured to be maintained at a low potential level.

(*Id.* at 4:67-5:29.)

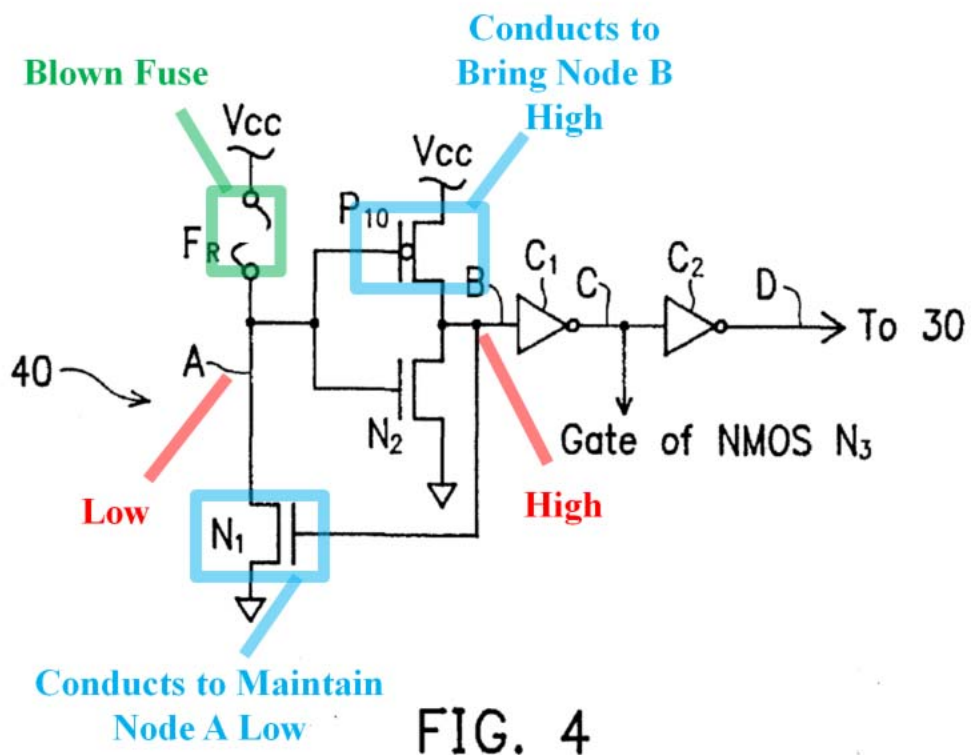
51. I have annotated figure 4 of Fu below to show how the circuit of figure 4 operates when the fuse F_R has not been blown. As shown, when the fuse F_R is not blown, the voltage at node A will be “High.” (*Id.* at 4:67-5:4, “When the memory redundancy circuitry 2 of FIG. 2 is not selected, or in other words, not activated, to replace the defective memory cells utilizing the redundant memory cells in circuitry 2, the fuse element is not blown. In this case, the potential of node A is at the high level (V_{CC}).”, FIGs. 2, 4.) Because node A is at the high level, the NMOS transistor N_2 that is included as the “pull-down” transistor in the inverter formed by P_{10} and N_2 is turned on to “pull node B to the GND potential.” (*Id.* at 5:4-6; *see also* my discussion above in Section V.B.) Fu further discloses that “[m]eanwhile, the other NMOS transistor N_1 is maintained in non-conduction mode, helping to maintain the potential of node A at the high level.” (*Id.* at 5:6-8.)



(*Id.* at FIG. 4 (annotated).)

52. I have also created a demonstrative (below) in order to show how the circuit shown in figure 4 of Fu operates when the fuse F_R has been blown, and, as a person of ordinary skill in the art would have understood, results in an open circuit between V_{CC} and node A. As shown in the demonstrative, the blown fuse is represented by including a break (open circuit) in the conductor included inside the fuse F_R . According to Fu, when the fuse is blown, the node A is at a low potential. (*Id.* at 5:19-25.) Because node A, which is coupled to the gate of PMOS transistor P_{10} , is low, PMOS transistor P_{10} is on and conducting. (*Id.* at 5:25-26; *see also* my

discussion above in Section V.B.) In turn, “[t]he conduction of P_{10} brings node B to the high potential level, which also makes the NMOS transistor N_1 conduct[], so that node A is ensured to be maintained at a low potential level.” (*Id.* at 5:26-29.)



(*Id.* at FIG. 4 (annotated and modified to show blown fuse).)

53. Therefore, based on whether or not the fuse F_R has been blown, node A will be held either high (V_{CC}) or low (GND). (*Id.* at 4:67-5:29.) The state of node A is inverted by the inverter formed by transistors P_{10} and N_2 to produce the state at node B, which is fed back to the input of NMOS transistor N_1 , thereby helping to maintain the state of nodes A and B. Therefore, nodes A and B are

latched at either V_{CC} (“High”) or GND (“Low”) based on whether or not the fuse is blown.

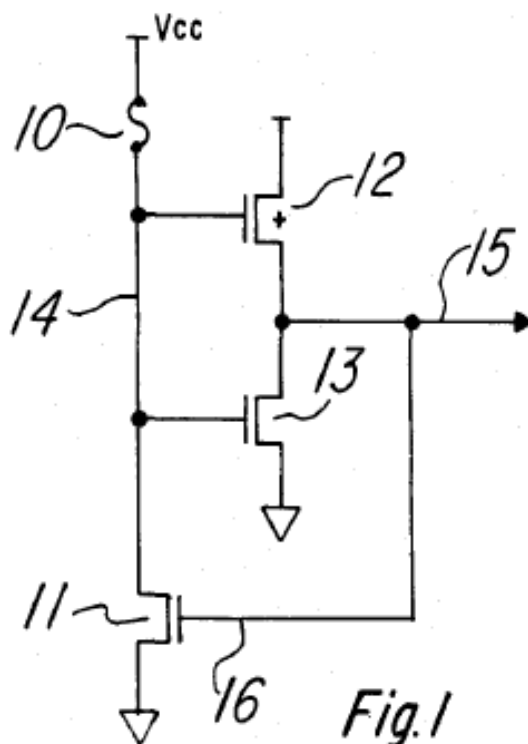
B. McAdams

54. McAdams relates to a “fuse circuit as used in self-repairing memory devices.” (Ex. 1006 at Abstract.) McAdams describes the operation of the fuse circuit as follows:

In self-repairing semiconductor memory device, fuses are used to store the addresses of faulty locations, so redundant cells can be substituted. Or, the fuse may be used to generate an enabling signal. These fuses are usually polysilicon conductor strips that are selectively blown by an indexed laser beam.

(*Id.* at 1:9-14.)

55. McAdams discloses operation of a particular fuse circuit in connection with figure 1. (*Id.* at FIG. 1.)



(*Id.* at FIG. 1.)

56. The fuse circuit shown in figure 1 of McAdams includes “[a] fuse element 10,” “an N-channel feedback transistor 11,” and “[a] CMOS inverter [that] includ[es] a P-channel transistor 12 and an N-channel transistor 13.” (*Id.* at 1:67-2:6.) The fuse circuit of figure 1 “produces an output 15” and “[f]eedback is provided from the output node 15 to the gate of the transistor 11.” (*Id.* at 2:3-7.)

57. McAdams discloses how the fuse circuit operates when power-up occurs and Vcc goes from zero to +5v. (*Id.* at 2:8-26.) For example, when power is applied, “if the fuse has not been blown, the node 14 follows Vcc” (*id.* at 2:8-10), which, as a person of ordinary skill in the art would have understood, results

in the output node 15 of the inverter being pulled low to V_{ss} . If the fuse has been blown, node 14 is at V_{ss} when power is applied, and transistor 12 turns on, causing the output node 15 to follow V_{cc} and be pulled high. (*Id.* at 2:21-24; see my analysis above in Section V.B.) As the output node 15 goes high, transistor 11 turns on, thereby keeping the node 14 at V_{ss} . (*Id.* at 2:24-26.)

C. Sugibayashi

58. Sugibayashi relates to an internal power supply system for use in a semiconductor memory device. (Ex. 1011 at 4:40-45, “[A] dynamic random access memory device embodying the present invention is fabricated on a single semiconductor chip 11, and largely comprises an internal power supply system 12 for producing a step-down power voltage V_{int} ”) Sugibayashi discloses that internal power supply circuits were known to be included in semiconductor memory devices. For example, Sugibayashi states that a “typical example of the dynamic random access memory device” includes “an internal power circuit” such as that shown in figure 1. (*Id.* at 1:16-22, FIG. 1.)

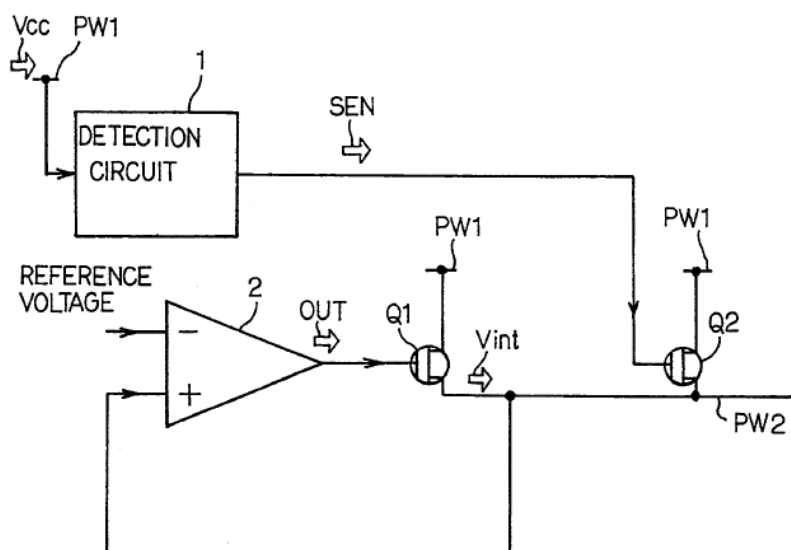


Fig.1
PRIOR ART

(*Id.* at FIG. 1.)

59. According to Sugibayashi, while internal voltage supply generators for memory devices such as DRAMs were known, the internal voltages generated by such prior art voltage supply generators could have non-constant levels and result in malfunctions in the internal component circuits of the memories. (*Id.* at 2:58-3:24.) Therefore, Sugibayashi discloses an internal power supply system 12 depicted in annotated figure 5 below. (Ex. 1011 at 4:40-52, FIG. 5.)

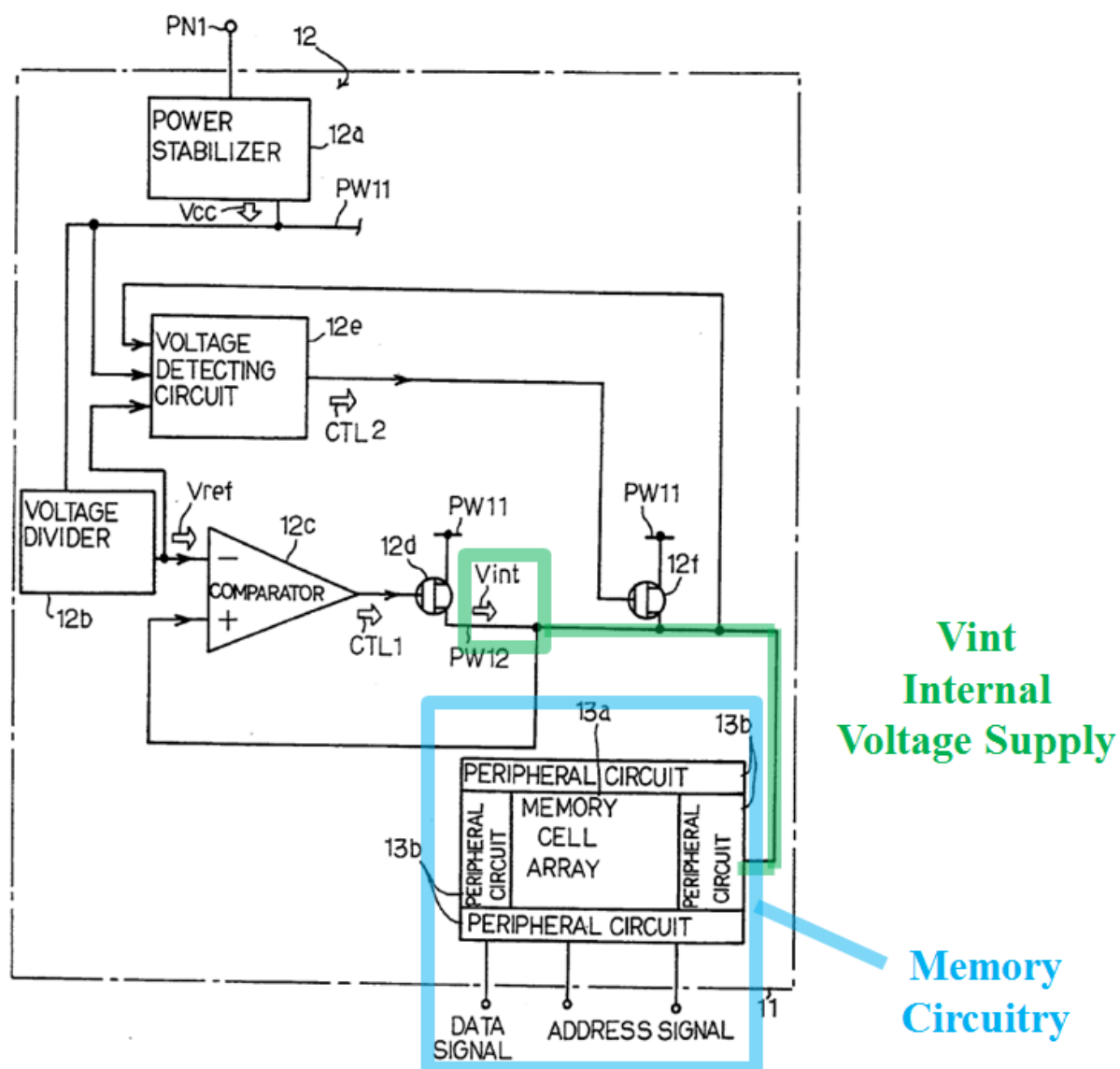


Fig. 5

(Id. at FIG. 5 (annotated).)

60. As shown in annotated figure 5 above, a comparator 12c compares the internal voltage V_{int} with a reference voltage V_{ref} , and, based on whether the internal voltage V_{int} is greater or less than V_{ref} , comparator 12c controls the

transistor 12d to keep V_{int} at the desired reference voltage level V_{ref} . (Ex. 1011 at 5:7-31, FIG. 5.) The internal power supply system 12 shown above also includes voltage detecting circuit 12e, which, in combination with variable load transistor 12f, ensures that variations in the external power voltage V_{cc} do not result in similar variations on the internal voltage supply V_{int} . (*Id.* at 6:48-68 (describing that when there is “turbulence in an external supply system” the “step-down power voltage V_{int} is kept constant as shown in FIG. 8”).)

IX. THE PRIOR ART DISCLOSES OR SUGGESTS ALL OF THE FEATURES OF CLAIMS 14-19 OF THE '492 PATENT

61. I have reviewed Fu, McAdams, and Sugibayashi. As I describe below in Sections IX.A-D, in my opinion, Fu and McAdams each disclose all of the features of claims 14-19 of the '492 patent. As I describe below in Sections IX.C-D, in my opinion Fu in combination with Sugibayashi as well as McAdams in combination with Sugibayashi discloses or suggests all of the features of claims 14-19 of the '492 patent.

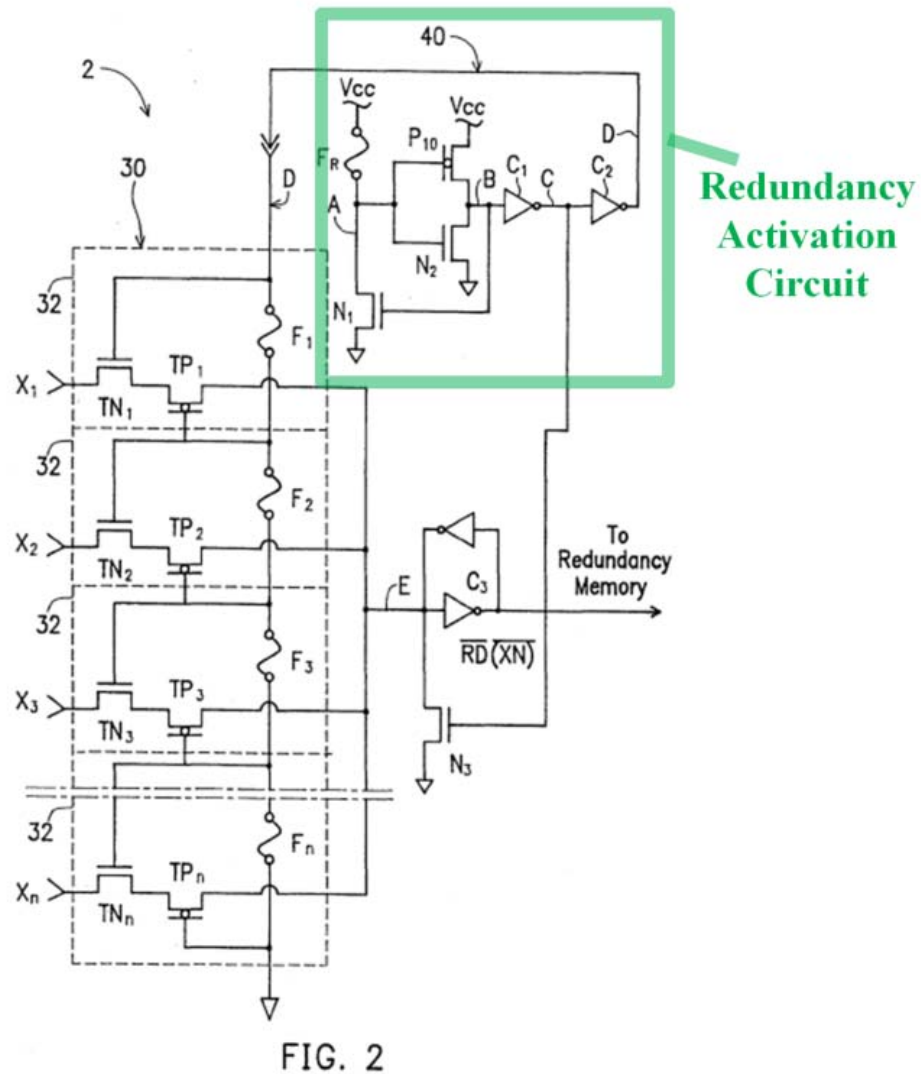
A. Fu Discloses the Features of Claims 14-19

62. In my opinion, Fu discloses all of the features of claim 14 of the '492 patent.

1. Claim 14

a) “A programmable latch comprising,”

63. I understand that “[a] programmable latch comprising” is the preamble of claim 14. I have been asked to assume that the preamble is limiting. In my opinion, Fu discloses this feature. For example, Fu discloses “memory redundancy circuitry 2, which comprises the redundancy activation circuit 40.” (Ex. 1005 at 3:47-48.) Figure 2 (reproduced below) illustrates the memory redundancy circuitry 2, including the redundancy activation circuit 40. (*Id.* at 3:47-48, FIG. 2.)



(*Id.* at FIG. 2 (annotated).) Fu further discloses that the “redundancy activation circuit 40” shown in figure 2 is also depicted in figure 4 (reproduced below). (*Id.* at 4:14-17, FIG. 4.)

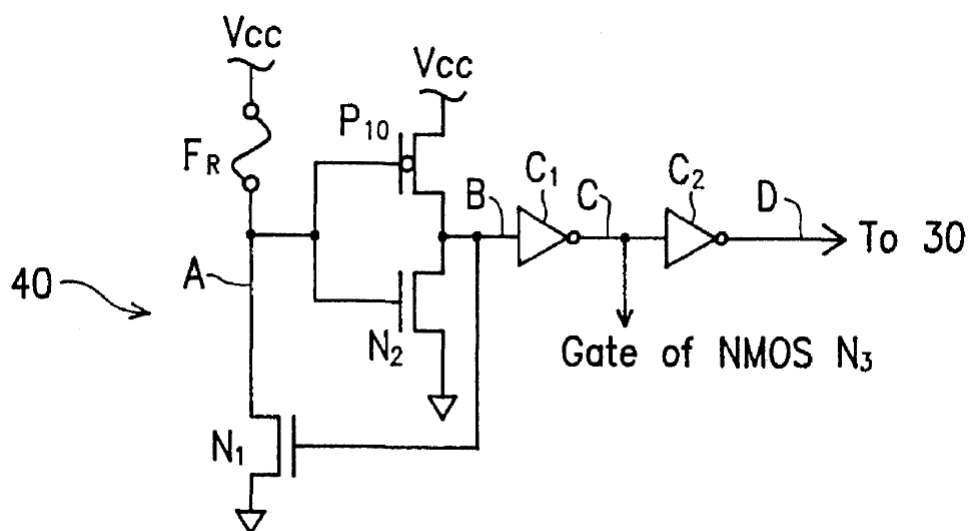


FIG. 4

(*Id.* at FIG. 4.)

64. “The redundancy activation circuit 40 of figure 4 includes a fuse F_R , a PMOS transistor P_{10} , two NMOS transistors N_1 and N_2 , and two inverters C_1 and C_2 .” (*Id.* at 4:17-19.) Fu discloses how the redundancy activation circuit 40 operates to provide control signals to the remainder of the memory redundancy circuitry 2 shown in FIG. 2 as follows:

The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (V_{cc}) and low (GND) levels, together with its host main memory cell array of the entire memory device.

(*Id.* at 3:46-51.)

The following will describe the operation of the memory redundancy circuitry 2 of the present invention shown in FIG. 2.

When the memory redundancy circuitry 2 of FIG. 2 is not selected, or in other words, not activated, to replace the defective memory cells utilizing the redundant memory cells in circuitry 2, the fuse element F_R is not blown. In this case, the potential of node A is at its high level (V_{CC}), and the NMOS transistor N_2 is in a conduction mode to pull node B to the GND potential. Meanwhile, the other NMOS transistor N_1 is maintained in non-conduction mode, helping to maintain the potential of node A at the high level. In this condition, the electric potential of node C is also at high level, making the third NMOS transistor N_3 go into a conduction mode, which in turn pulls the potential of node E to the GND potential. This inverts the redundancy activation status signal RD into a high level, indicating a non-activated status of the memory redundancy circuitry 2.

In addition, node D is at a low level, and as a result, the PMOS transistor TP_1 conducts, while the NMOS transistor TN_1 is not conducting, thereby blocking the signal path of the address signal X_1 .

On the other hand, when the memory redundancy circuitry 2 of FIG. 2 is selected and activated, the fuse element F_R is blown open. Each of the fuse elements F_i , say F_2 for example, of the decoder unit 32 in the programmable redundancy decoder logic that correspond to a defective memory cell in the main memory cell array are also blown. At this instant, node A is at a low electric potential, making the PMOS transistor P_{10} conduct. The conduction of P_{10} brings node B to the high potential level, which also makes the NMOS transistor N_1 conducts, so that node A is ensured to be maintained at a low potential level. Meanwhile, node C is low, cutting off the NMOS transistor N_3 . Since node D is high, and since fuse element F_2 has been blown open, only NMOS and PMOS transistors TN_2 and TP_2 are in their conduction mode, because the gate of TN_2 is high and the gate of TP_2 is low. No other transistor pair are in this condition. This allows only the properly decoded address bit signal X_2 to access the redundant memory cell, replacing its defective original part.

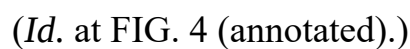
(*Id.* at 4:64-5:37.)

65. The circuitry in Fu operates between two electrical potentials, one of which is a logical high (V_{CC}) and the other is a logical low (GND). Specifically, Fu discloses:

The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (V_{CC}) and low (GND) levels, together with its host main memory cell array of the entire memory device.

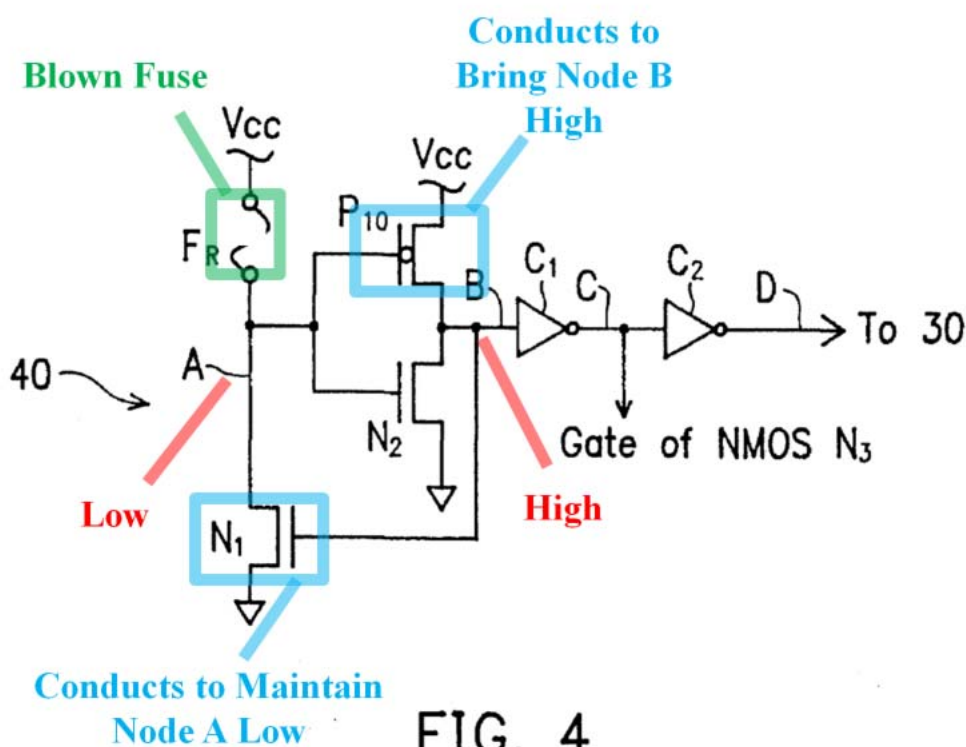
(*Id.* at 3:46-51.)

66. I have annotated figure 4 of Fu below to show how the circuit of figure 4 operates when the fuse F_R has not been blown. As shown, when the fuse F_R is not blown, the node A will be “high.” (*Id.* at 4:67-5:4, “When the memory redundancy circuitry 2 of FIG. 2 is not selected, or in other words, not activated, to replace the defective memory cells utilizing the redundant memory cells in circuitry 2, the fuse element is not blown. In this case, the potential of node A is at the high level (V_{CC})....”; *id.* at FIGs. 2, 4.) Because node A is at the high level, NMOS transistor N_2 , which is included as the “pull-down” transistor in the inverter formed by P_{10} and N_2 , is turned on to “pull node B to the GND potential.” (*Id.* at 5:4-6; *see also* my discussion above in Section V.B.) Fu further discloses that “[m]eanwhile, the other NMOS transistor N_1 is maintained in non-conduction



43

transistor in the inverter formed by P_{10} and N_2 , is on and conducting. (*Id.* at 5:25-26; *see also* my discussion above in Section V.B.) Because P_{10} is turned on and conducting, it pulls the output node B of the inverter high, and the high voltage at node B turns on the NMOS transistor N_1 , which in turn holds the node A “low.” (Ex. 1005 at 5:26-29, “The conduction of P_{10} brings node B to the high potential level, which also makes the NMOS transistor N_1 conduct[], so that node A is ensured to be maintained at a low potential level.”)



(*Id.* at FIG. 4 (annotated and modified to show open circuit in fuse F_R)⁵.)

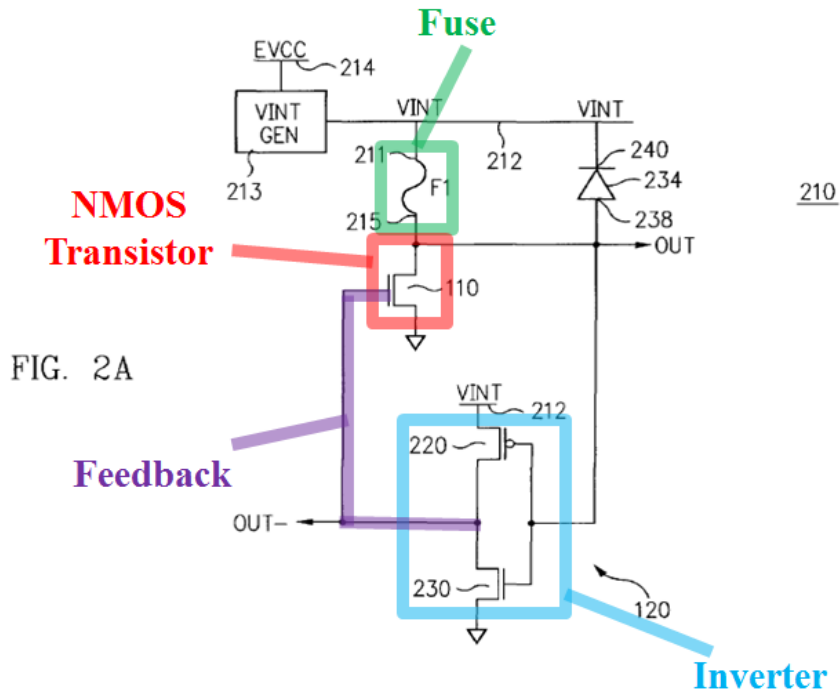
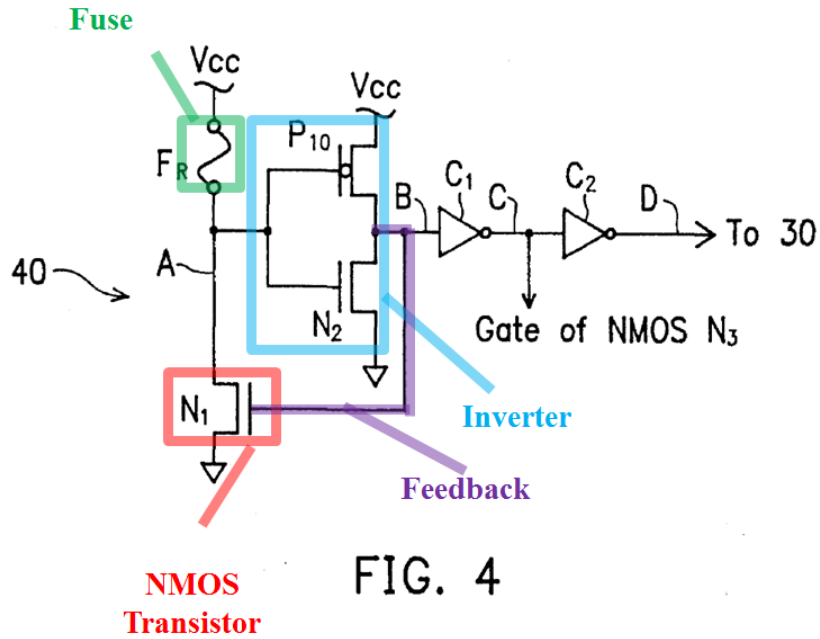
68. Therefore, based on whether or not the fuse F_R has been blown, node A will be held either high (V_{CC}) or low (GND). (Ex. 1005 at 4:67-5:29.) The state of node A is inverted by the inverter formed by transistors P_{10} and N_2 to produce the state at node B, which is fed back to the input of NMOS transistor N_1 , thereby helping to maintain the state of nodes A and B. Therefore, as a person of ordinary skill in the art would have understood, nodes A and B are latched at either V_{CC} or GND based on whether or not the fuse is blown.

69. The outputs of the redundancy activation circuit (i.e., the outputs of inverters C_1 and C_2) are inverted and non-inverted versions of the state of node B, respectively, where the state at node B is the inverse of the state at node A. (Ex. 1005 at FIG. 4.) A person of ordinary skill in the art would have recognized that the redundancy activation circuit 40 shown in figure 4 of Fu is a “programmable

⁵ The demonstrative is a non-limiting and exemplary demonstrative that I have created to help explain the operation of Fu’s circuit. Indeed, all of the demonstratives in this declaration, where I have modified a figure from a prior art or created a drawing to explain basic circuit concepts, are exemplary and should not be viewed as limiting.

latch” where the programming corresponds to the state of the fuse F_R , which determines the latched values at nodes A and B as well as at the outputs C and D.

70. Indeed, a person of ordinary skill in the art would have recognized that the circuit of figure 4 of Fu is a “programmable latch” in the same way that the figure 2A circuit of the ’492 patent is a “programmable latch.” As shown in the annotated figures below, the circuit of figure 2A of the ’492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the corresponding elements in the figure 4 circuit of Fu. (Ex. 1001 at FIG. 2A; Ex. 1005 at FIG. 4.)



(Ex. 1005 at FIG. 4 (annotated) (top); Ex. 1001 at FIG. 2A (annotated) (bottom).)

b) "a first terminal for receiving a constant non-ground voltage throughout operation of the latch;"

71. In my opinion, Fu discloses this feature. As shown in annotated figure 4 below, the “fuse circuit” of Fu includes a “terminal” V_{cc} , where V_{cc} is a “high voltage level.” (Ex. 1005 at 1:67.) Fu discloses that “[t]he memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (V_{CC}) and low (GND) levels together with its host main memory cell array of the entire memory device.” (*Id.* at 3:46-51.)

72. A person of ordinary skill in the art would have recognized that the “two electric potentials” V_{CC} and GND in Fu correspond to the power supply provided to the integrated circuit (e.g. memory device) of Fu. V_{cc} was commonly used to represent one of the power supply terminals (typically a positive voltage), whereas V_{ss} or GND was used to represent the other power supply terminal. A person of ordinary skill in the art would also have recognized that during operation of the circuit, V_{cc} would be “a constant non-ground voltage” as it would be relatively stable (constant) and is a positive potential (non-ground). Indeed, Fu recognizes that V_{cc} is a “non-ground voltage” because it distinguishes V_{cc} from ground (“GND”). (See *id.* at 3:46-51.) A person of ordinary skill would have recognized that V_{cc} is a “constant” non-ground voltage because such a “constant”

voltage is a requirement for the proper operation of the circuit. Indeed, Fu does not state that V_{CC} is not constant when power is applied to the circuit.

73. A person of ordinary skill in the art would have also understood that the triangle symbol shown pointing downward in the annotated figures above corresponds to the ground potential.

74. Fu discloses that “[a]s can be seen in the drawing, the fuse element F_R is connected in series with the NMOS transistor N_1 , with the other end of fuse element tied to V_{CC} , and the transistor end tied to ground.” (*Id.* at 4:20-23.) During “operation of the memory redundancy circuit 2,” “node A is at its high level (V_{CC})” when the fuse is not blown. (*Id.* at 4:64-5:6.) Therefore, a high voltage V_{CC} , which is a constant non-ground voltage, is applied when the circuit of figure 4 operates. Accordingly, the terminal I highlighted in blue below, which receives V_{CC} , is a “first terminal for receiving a constant non-ground voltage throughout operation of the latch” as recited in claim 14.

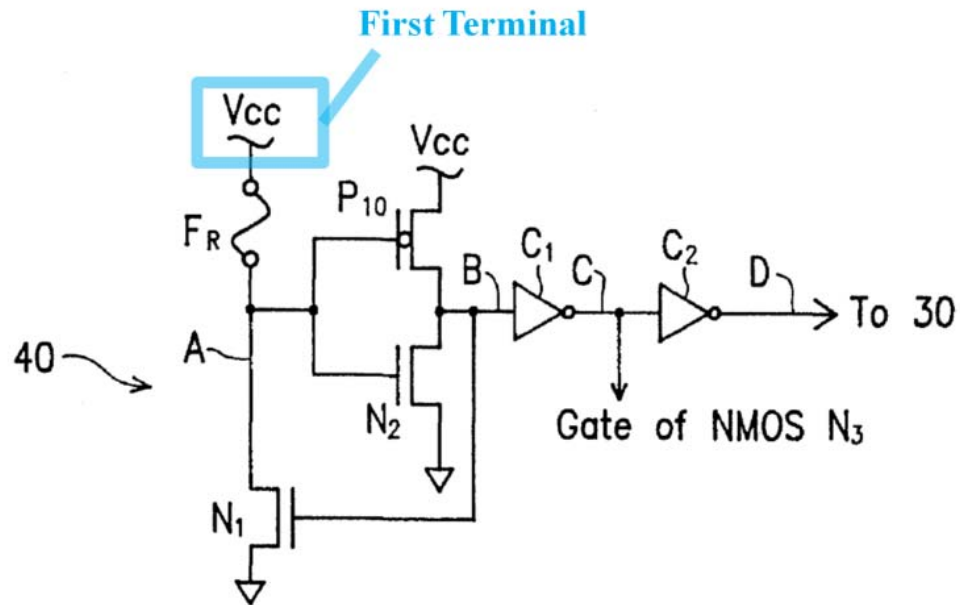
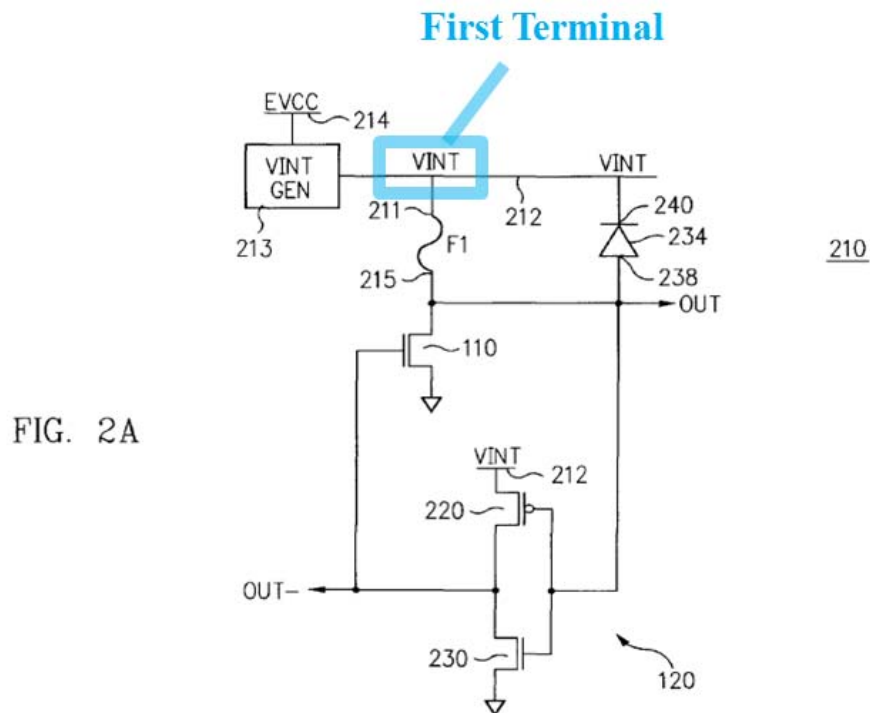


FIG. 4

(*Id.* at FIG. 4 (annotated).)

75. As shown in annotated figure 2A of the '492 patent below, the "first terminal" highlighted in figure 4 of Fu above is consistent with the "first terminal" disclosed by the '492 patent.



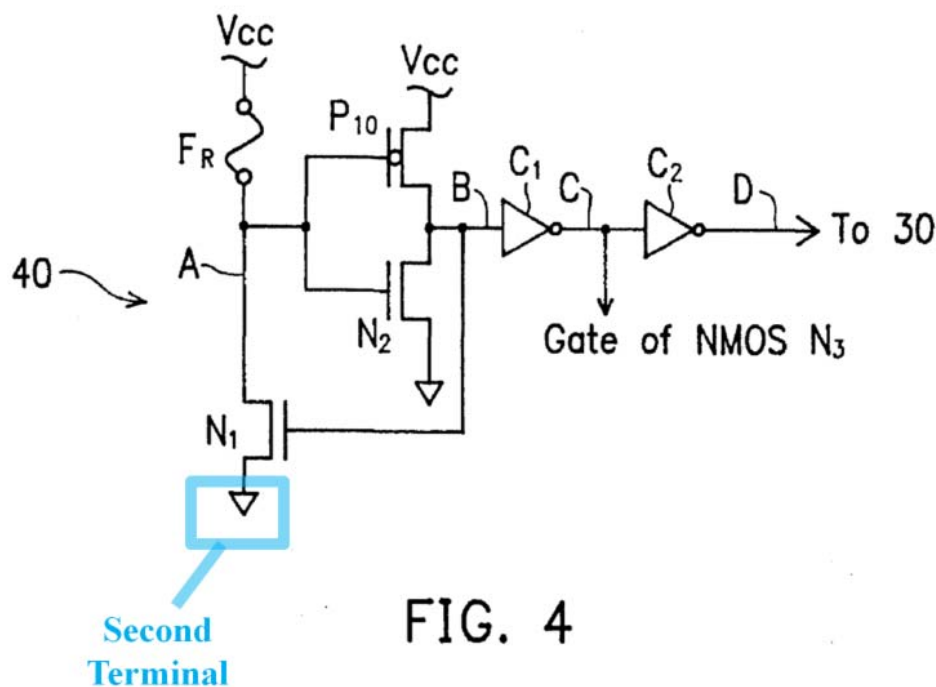
(Ex. 1001 at FIG. 2A (annotated)).

c) “a second terminal for receiving a voltage;”

76. In my opinion, Fu discloses this feature. For example, the programmable latch circuit in figure 4 of Fu includes a second terminal for receiving GND, which, in the example embodiment described in Fu, corresponds to a low voltage. (Ex. 1005 at 3:46-51, “The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (Vcc) and low (GND) levels together with its host main memory cell array of the entire memory device.”, FIG. 4.) Fu discloses that “[a]s can be seen in the

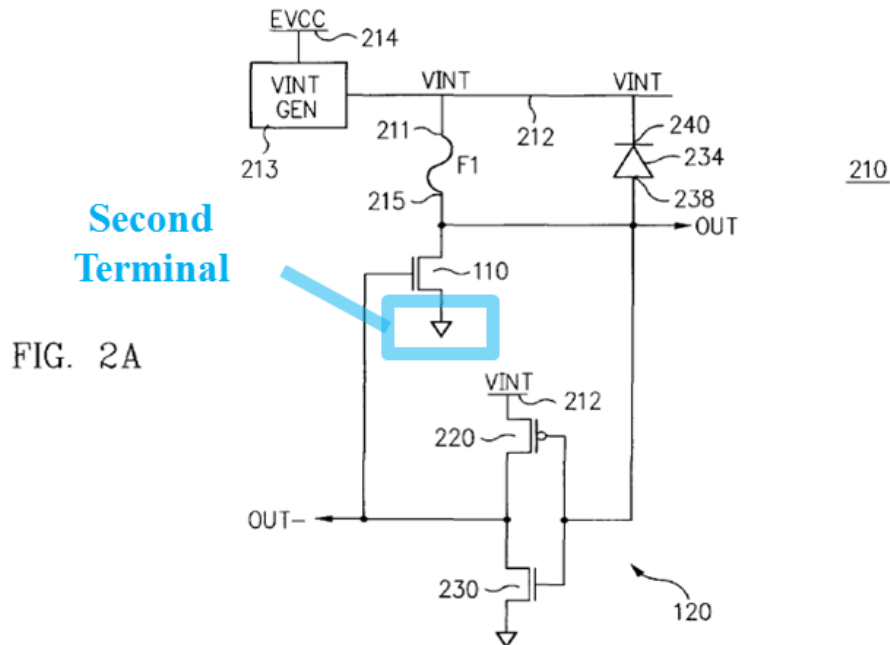
drawing, the fuse element F_R is connected in series with the NMOS transistor N_1 , with the other end of fuse element tied to V_{CC} , and *the transistor end tied to ground.*” (*Id.* at 4:20-23, emphasis added.)

77. Therefore, the terminal that I highlighted in blue below that receives GND is a “second terminal for receiving a voltage” as recited in claim 14. Note that another such terminal that receives GND is shown connected to the drain of transistor N_2 .



(*Id.* at FIG. 4 (annotated).)

78. As shown in annotated figure 2A of the '492 patent below, the “second terminal” highlighted in figure 4 of Fu above is consistent with the “second terminal” disclosed by the '492 patent.



(Ex. 1001 at FIG. 2A (annotated).)

- d) “a terminal T1 for providing a signal indicating a state of the programmable latch;”

79. In my opinion, Fu discloses this feature. For example, as shown in annotated figure 4 below, the node A indicates the state of the fuse, which corresponds to the state of the programmable latch (“a terminal T1 for providing a signal indicating a state of the programmable latch”). As discussed above with respect to claim element 14[a], during operation of the latch, if the fuse is intact,

node A is at V_{cc} (high), but if the fuse is blown, node A is at GND (low). (See my discussion above regarding the operation of the circuit in figure 4 of Fu in Section IX.A.1(a).) Therefore, a person of ordinary skill in the art would have recognized that the voltage at node A indicates a “state of the programmable latch” because it indicates whether the fuse is blown or not.

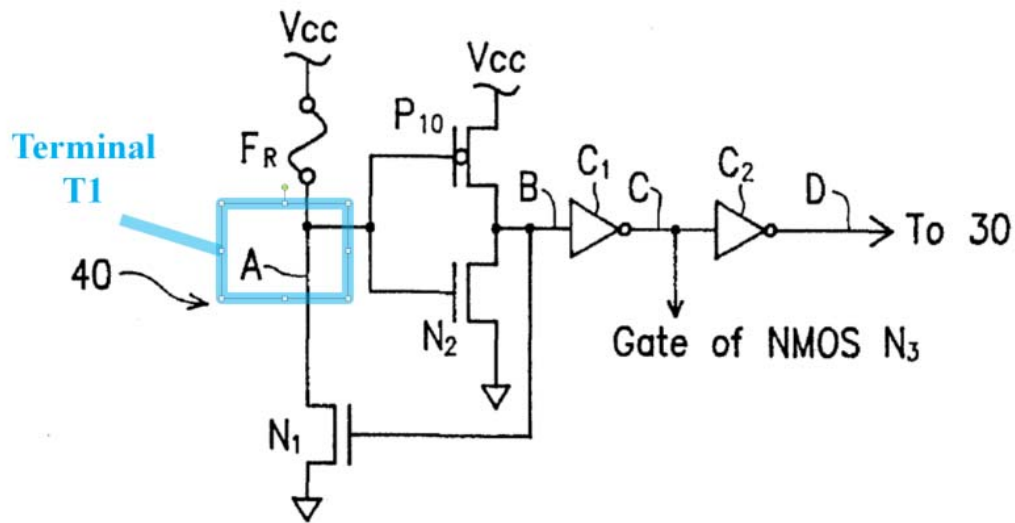
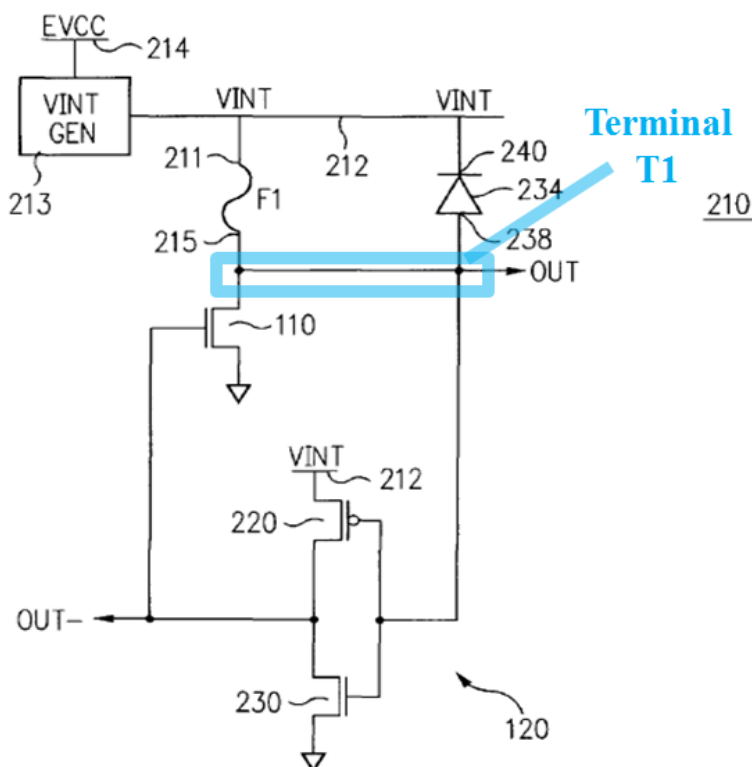


FIG. 4

(Ex. 1005 at FIG. 4 (annotated).)

80. As shown in annotated figure 2A of the '492 patent below, the “terminal T1” highlighted in figure 4 of Fu above is consistent with the “terminal T1” disclosed by the '492 patent.

FIG. 2A



(Ex. 1001 at FIG. 2A (annotated).)

- e) “a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;”

81. In my opinion, Fu discloses this feature. For example, the fuse F_R that I have highlighted in red in annotated figure 4 of Fu below is a “non-volatile programmable element.” Such an understanding is consistent with the disclosure of the '492 patent, which shows a fuse as the “non-volatile programmable element”

in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 3:10-23, 7:24-36.) Moreover, claim 18, which depends from claim 14, recites “wherein the programmable element is a fuse.” Such a recitation in claim 18 makes clear to a person of ordinary skill in the art that a fuse is a “non-volatile programmable element” in the context of claim 14 and the ’492 patent. (*Id.* at 10:38-39.)

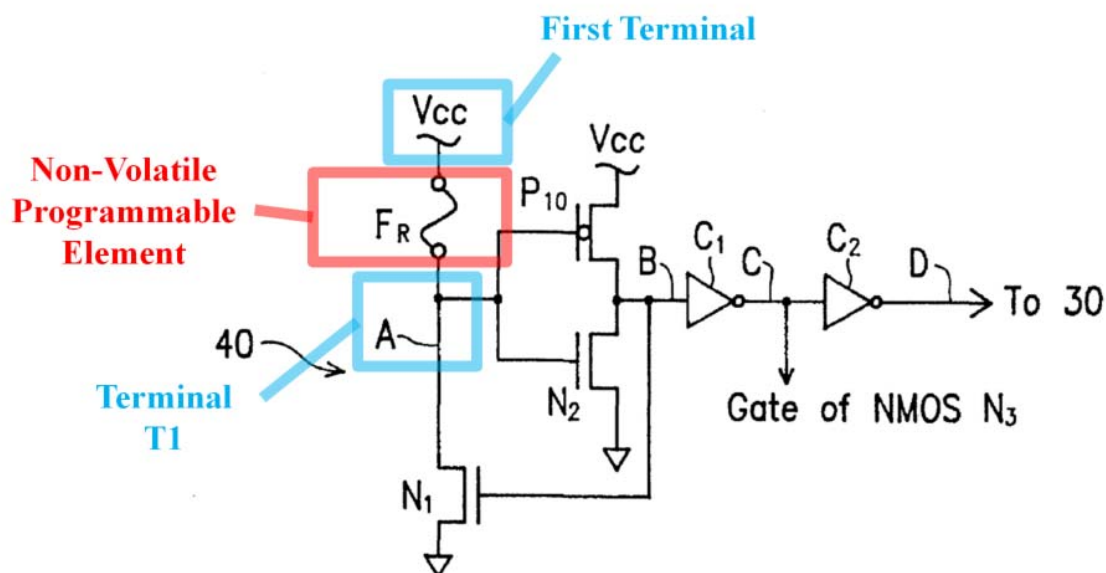


FIG. 4

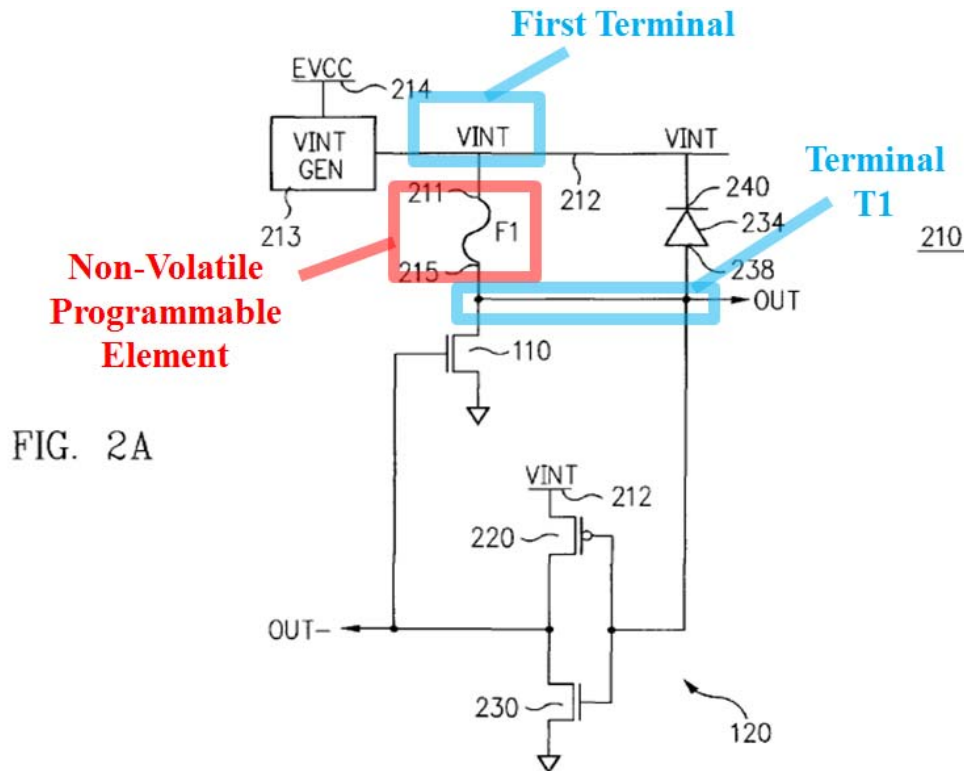
(Ex. 1005 at FIG. 4 (annotated).)

82. As shown in annotated figure 4 above, the fuse F_R (“non-volatile programmable element”) is coupled between V_{CC} (“first terminal”) and node A (“terminal T1”) and therefore constitutes “a non-volatile programmable element connected to the terminal T1 and the first terminal.”

83. If the fuse F_R is not blown such that the conductor within the fuse is left intact, the fuse will allow current to flow between its two terminals (i.e., it is “conductive.”) Therefore, when the fuse is intact and “conductive,” it provides an electrical connection between V_{CC} (“first terminal”) and node A (“terminal T1”). (*Id.* at 5:4-5; *see also* my discussion above regarding the operation of the circuit in figure 4 of Fu in Section IX.A.1(a).) Therefore, in my opinion, Fu discloses “the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive.”

84. If the fuse F_R is blown such that the conductor within the fuse is severed and there is an open circuit between the two terminals of the fuse, the fuse is non-conductive and will not allow current to flow between the terminals. Therefore, when the fuse is blown and “non-conductive,” the fuse does not provide an electrical connection between V_{CC} (“first terminal”) and node A (“terminal T1”). (*Id.* at 5:19-25; *see also* my discussion above regarding the operation of the circuit in figure 4 of Fu in Section IX.A.1(a).) A person of ordinary skill in the art would have understood that the lack of an electrical connection between V_{CC} and node A “isolates” node A from V_{CC} . Therefore, Fu discloses “the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive.”

85. As shown in annotated figure 2A of the '492 patent below, the “non-volatile programmable element” highlighted in figure 4 of Fu above is consistent with the “non-volatile programmable element” disclosed by the '492 patent.



(Ex. 1001 at FIG. 2A (annotated).)

- f) “a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and”

86. In my opinion, Fu discloses this feature. For example, a person of ordinary skill in the art would have understood that the NMOS transistor N_1 highlighted below in annotated figure 4 of Fu is a “variable-impedance electrical

path” as that term is used in the ’492 patent. Indeed, such an understanding is consistent with the disclosure of the ’492 patent, which shows an NMOS transistor as the “variable-impedance electrical path” in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 7:57-66.) Indeed, claim 19, which depends from claim 14, recites “wherein the variable-impedance electrical path is an NMOS transistor.” As such, a person of ordinary skill in the art would have understood that an NMOS transistor is a “variable-impedance electrical path” in the context of claim 14 and the ’492 patent. (*Id.* at 10:40-41.)

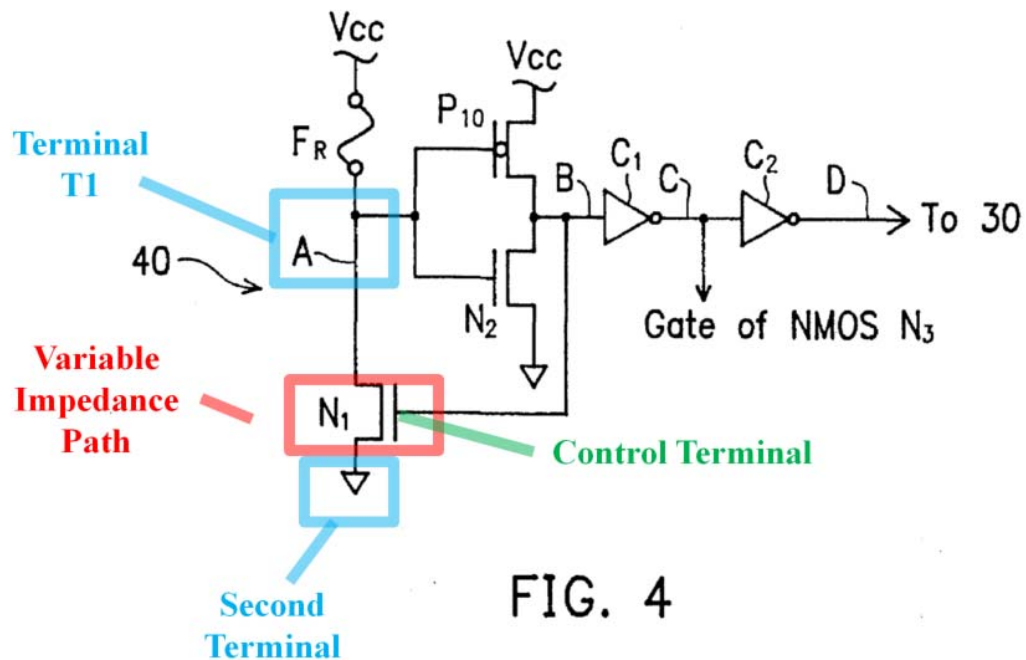


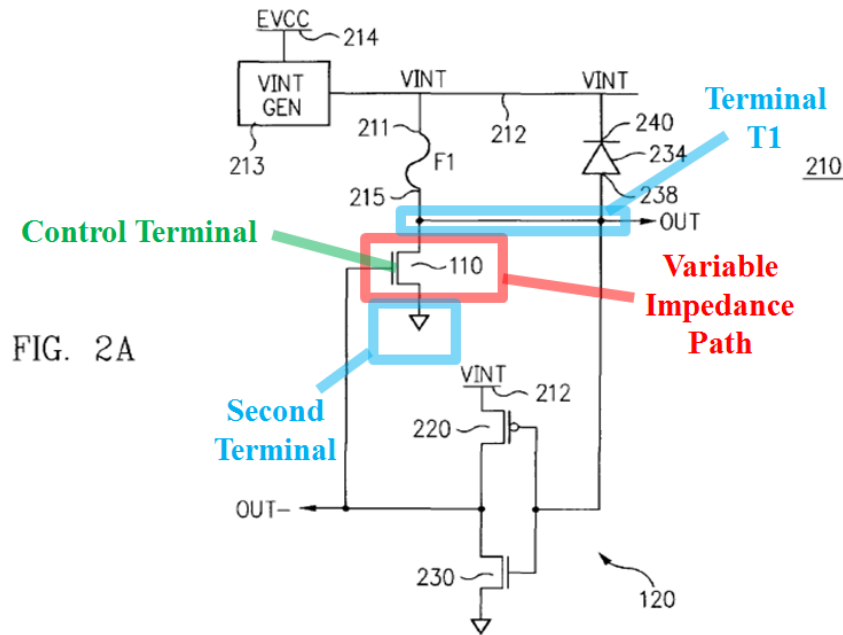
FIG. 4

(*Id.* at FIG. 4 (annotated).)

87. As shown in annotated figure 4 above, the NMOS transistor N_1 (“variable-impedance electrical path”) is coupled between node A (“terminal T1”) and GND (“second terminal”) and therefore constitutes “variable-impedance electrical path connected between the terminal T1 and the second terminal.”

88. The gate terminal of the NMOS transistor N_1 determines whether the NMOS transistor is on or off. (See Section V.B above.) A person of ordinary skill in the art would have understood that the impedance of the transistor N_1 , where the impedance of the transistor includes its opposition to current flow, is less when the transistor is on than when the transistor is off. Therefore, the NMOS transistor N_1 (“variable impedance path”) has a gate terminal (“having a control terminal”) that determines whether the NMOS transistor is on or off, where the impedance of the transistor is different when it is on as opposed to when it is off (“for controlling the impedance of the variable-impedance path”). (Ex. 1005 at 5:5-7, 5:26-28.)

89. As shown in annotated figure 2A of the '492 patent below, the “variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path” highlighted in figure 4 of Fu above is consistent with the “variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path” disclosed by the '492 patent.



(Ex. 1001 at FIG. 2A (annotated).)

- g) “an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.”

90. In my opinion, Fu discloses this feature. For example, as shown in annotated figure 4 of Fu below, transistors P_{10} and N_2 together form an inverter. (Ex. 1005 at FIG. 4, 4:23-30, “The PMOS transistor P_{10} and the other NMOS transistor N_2 are also connected in series, with the PMOS end of this connection tied to V_{CC} and the NMOS end tied to ground. The gates of the P_{10} and N_2 transistors are tied together and are connected to the joint node A of the fuse

element F_R and N_1 series connection. The gate of the transistor N_1 is connected to the joint node B of the P_{10} and N_2 transistor series connection. . . .”; *see also* my discussion in Section V.B.) The gates of transistors P_{10} and N_2 (“the input of the inverter”) are connected to the node A (“terminal T1”). (Ex. 1005 at 4:23-30.)

91. The output of the inverter at node B is connected to the gate of the transistor N_1 (“an output connected to the control terminal of the variable-impedance path”). (*Id.*)

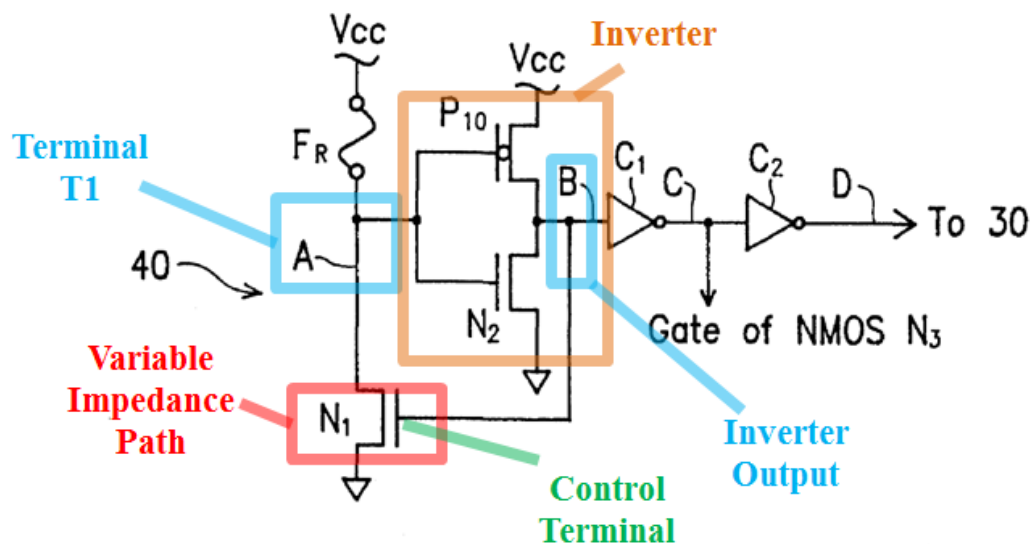
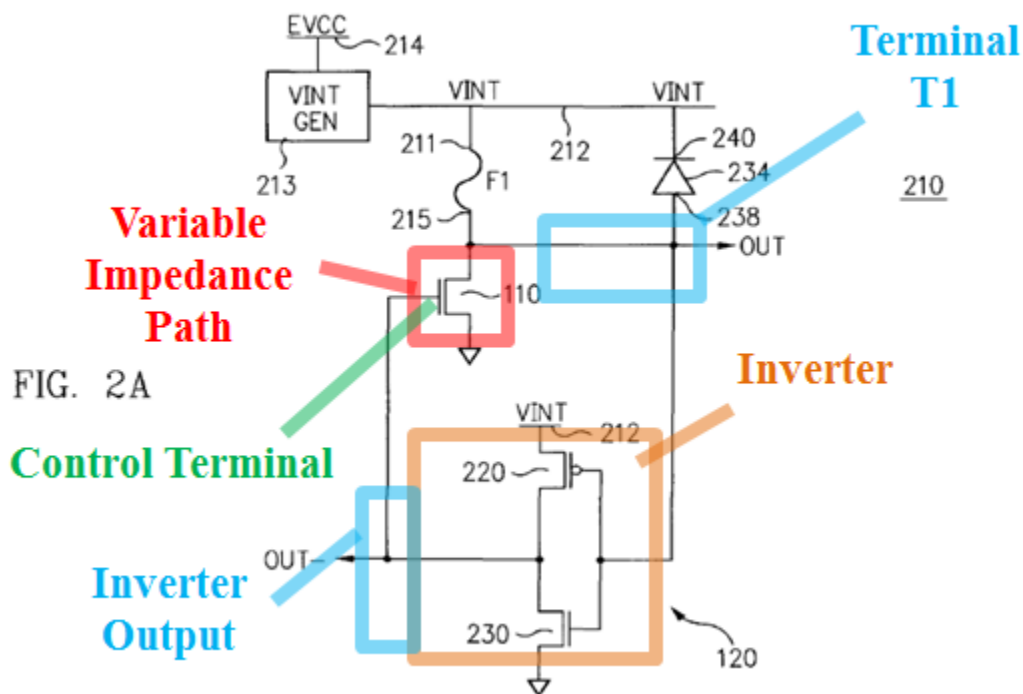


FIG. 4

(*Id.* at FIG. 4 (annotated).)

92. As I discussed above in section V.B, a person of ordinary skill in the art at the time of the invention would have understood that P_{10} and N_2 together form an “inverter.” Indeed, the circuit formed by P_{10} and N_2 is just like the

“CMOS inverter 120 formed by pull-up transistor 220 and NMOS pull-down transistor 230” in the ’492 patent. (Ex. 1001 at 3:24-32, FIG. 2A.)



(*Id.* at FIG. 2A (annotated).)

93. As shown in annotated figure 4 below, the inverter in F_u includes PMOS transistor P_{10} (“pull-up device”) coupled between the inverter output node B and V_{CC} , where, when the PMOS transistor P_{10} is on, it pulls the voltage on the inverter output node B up to V_{CC} and therefore would be understood to operate as a “pull-up” transistor in the inverter. (Ex. 1005 at FIG. 4, 4:23-30; *see also* my discussion above in Section V.B.) Similarly, the inverter includes NMOS transistor N_2 (“pull-down device”) coupled between the inverter output node B and

GND, where, when the NMOS transistor N_2 is on, it pulls the voltage on the inverter output node 15 down to GND and therefore would be understood to operate as a “pull-down” transistor in the inverter. (Ex. 1005 at FIG. 4, 4:23-30; *see also* my discussion above in Section V.B.)

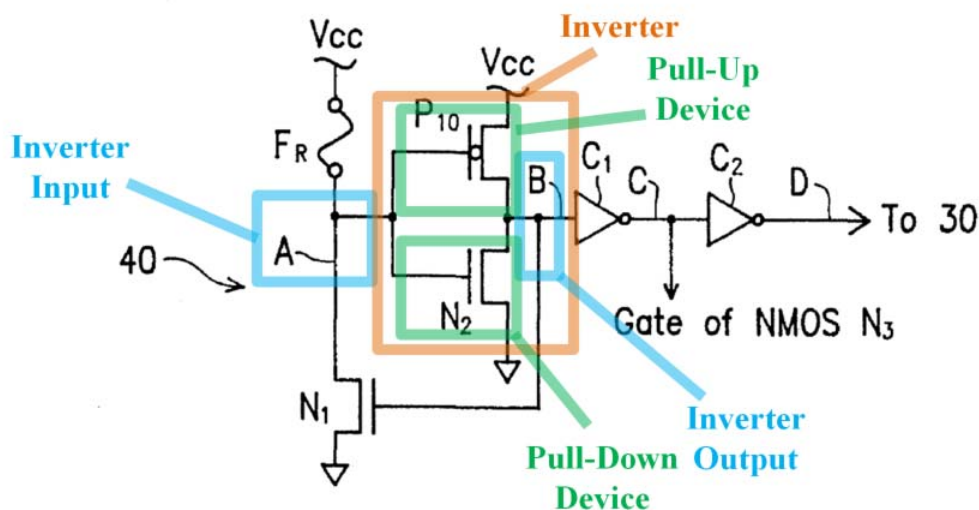
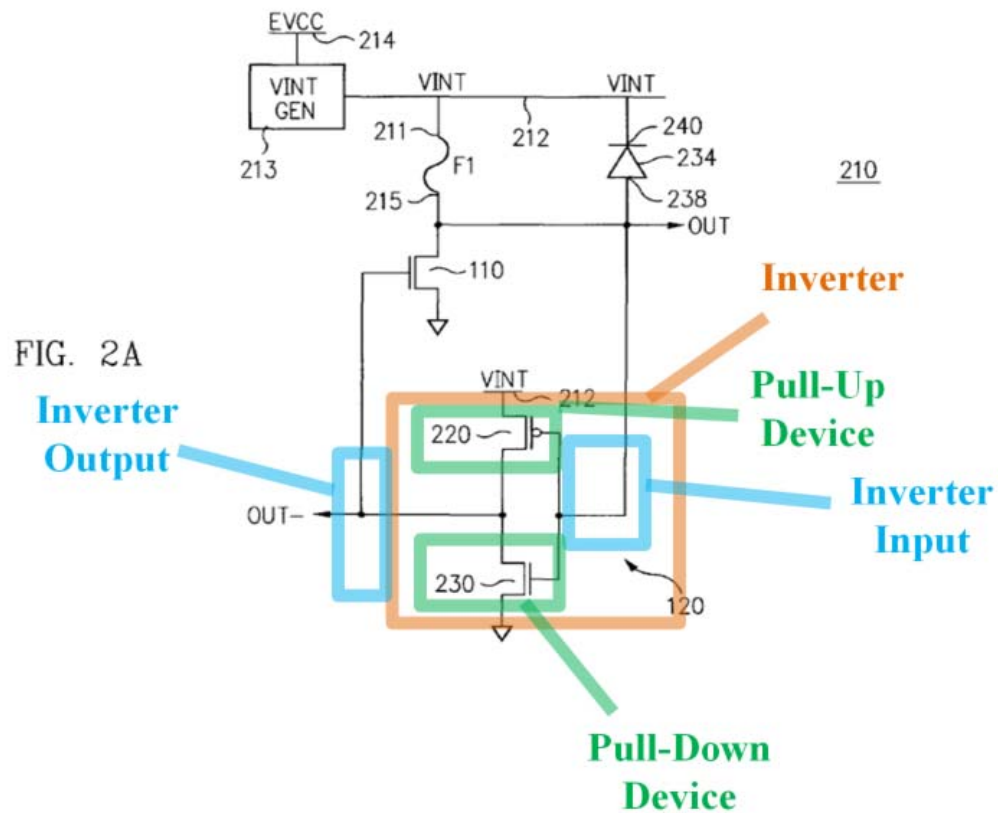


FIG. 4

(*Id.* at FIG. 4 (annotated).)

94. As shown in annotated figure 4 above, both the PMOS transistor P_{10} (“pull-up device”) and the NMOS transistor N_2 (“pull-down device”) are coupled to the inverter input at node A and the inverter output at node B (“at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output”). (*Id.* at FIG. 4, 4:23-30.)

95. The disclosure of P_{10} and N_2 of Fu as “pull-up” and “pull-down” devices, respectively, is consistent with the disclosure of the '492 patent, which shows an inverter including PMOS transistor 220 (“pull-up device”) and an NMOS transistor (‘pull-down device”) in figure 2A. (Ex. 1001 at 3:24-32, FIG. 2A.)



(*Id.* at FIG. 2A (annotated).)

2. Claim 15

- a) “The programmable latch of claim 14 wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.”

96. In my opinion, Fu discloses this feature. As shown in annotated figure 4 of Fu below, the “redundancy activation circuit” (“programmable latch”) of Fu does not receive any inputs from outside of the circuit as illustrated. (Ex. 1005 at FIG. 4.) As discussed above with respect to claim feature 14[a], when the circuit of figure 4 is operational, the voltage at node A (“terminal T1”) is only influenced by the electrical potentials applied on the Vcc and GND terminals (“first and second terminals”) and the state of the fuse F_R (“programmable element”). (*Id.* at 4:67-5:29; *see also* my discussion above in Section IX.A.1(a).)

97. Specifically, if the fuse is not blown, node A is at Vcc, whereas if the fuse is blown, node A is at GND. (*Id.* at 4:67-5:29; *see also* my discussion above in Section IX.A.1(a).)

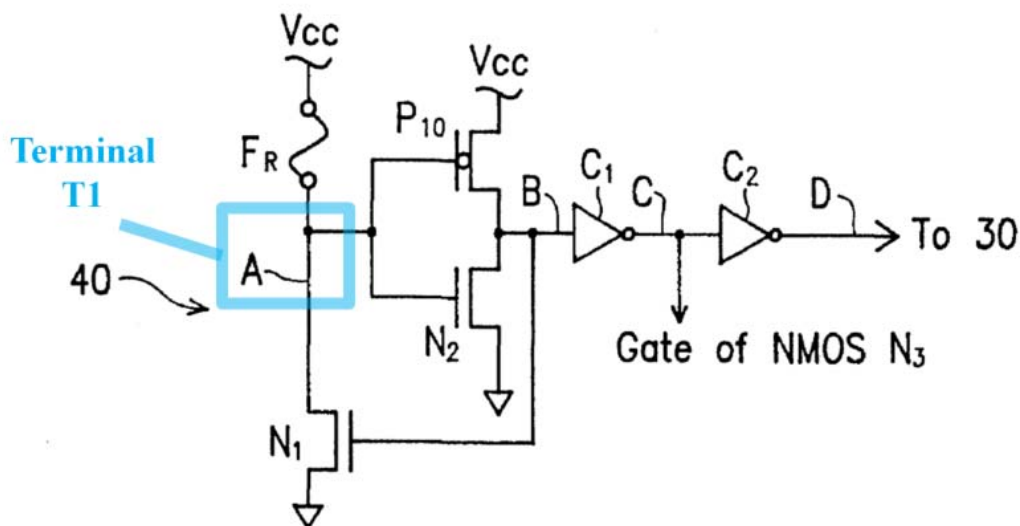


FIG. 4

(Ex. 1005 at FIG. 4 (annotated).)

98. Therefore, Fu discloses “wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.”

3. Claim 16

- a) “The programmable latch of claim 14 wherein the latch does not receive any latch initialization signal from outside the latch.”

99. In my opinion, Fu discloses this feature. As shown in figure 4 of Fu below, the “redundancy activation circuit” (“programmable latch”) of Fu does not receive any inputs from outside of the circuit illustrated and the state of the latch is

completely determined by the state of the fuse F_R and the voltages on the V_{CC} and GND terminals. (Ex. 1005 at 4:66-5:29, FIG. 4; *see also* my discussion above in Section IX.A.2.)

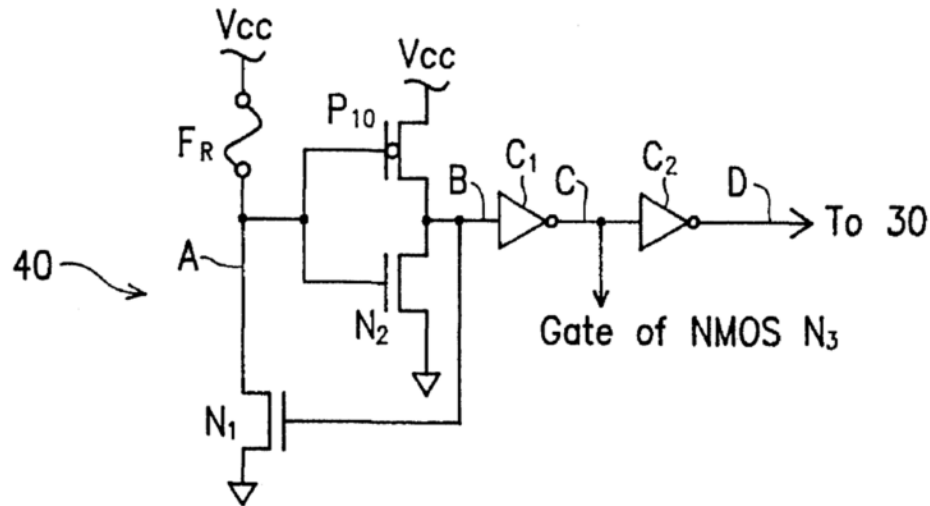


FIG. 4

(Ex. 1005 at FIG. 4.)

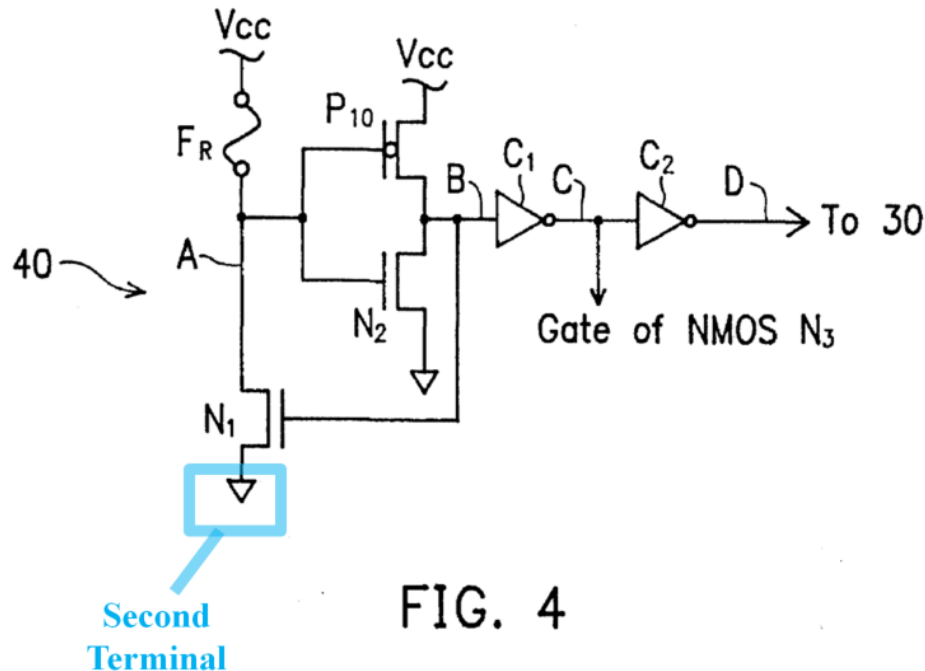
100. Therefore, Fu discloses “wherein the latch does not receive any latch initialization signal from outside the latch.”

4. Claim 17

a) “The programmable latch of claim 14 wherein the second terminal is to receive a ground voltage throughout operation of the latch.”

101. In my opinion, Fu discloses this feature. As discussed above with respect to claim element 14[c], when the “redundancy activation circuit”

(“programmable latch”) is operational, the second terminal is connected to ground (GND). (Ex. 1005 at 3:46-51, “The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (V_{CC}) and low (GND) levels together with its host main memory cell array of the entire memory device.”, 4:20-23, “As can be seen in the drawing, the fuse element F_R is connected in series with the NMOS transistor N_1 , with the other end of fuse element tied to V_{CC} , and the transistor end tied to *ground*.”, emphasis added; see my discussion above in Section IX.A.1(c).)



(*Id.* at FIG. 4 (annotated).)

102. Therefore, Fu discloses that “the second terminal is to receive a ground voltage throughout operation of the latch” as recited in claim 17.

5. Claim 18

a) “The programmable latch of claim 14 wherein the programmable element is a fuse.”

103. In my opinion, Fu discloses this feature. As demonstrated above with respect to claim feature 14[e], the fuse F_R shown in annotated figure 4 below is a “non-volatile programmable element.” (See my discussion above in Section IX.A.1(e).) Therefore, Fu discloses “wherein the programmable element is a fuse.”

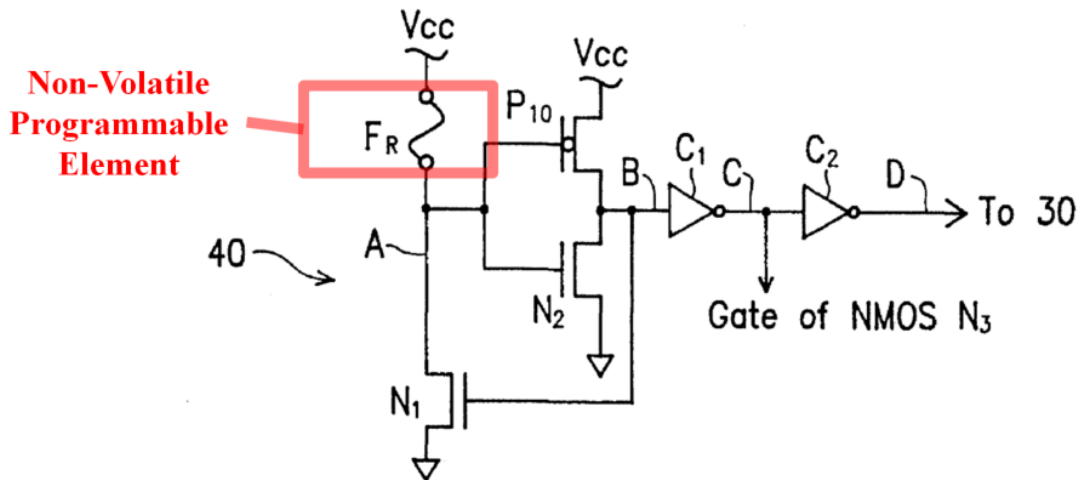


FIG. 4

(Ex. 1005 at FIG. 4 (annotated).)

6. Claim 19

a) “The programmable latch of claim 14 wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.”

104. In my opinion, Fu discloses this feature. As demonstrated above with respect to claim feature 14[f], the NMOS transistor N₁ in annotated figure 4 below corresponds to the claimed “variable impedance electrical path.” (See my discussion above in Section IX.A.1(f).) Therefore, Fu discloses “wherein the variable-impedance path is an NMOS transistor.”

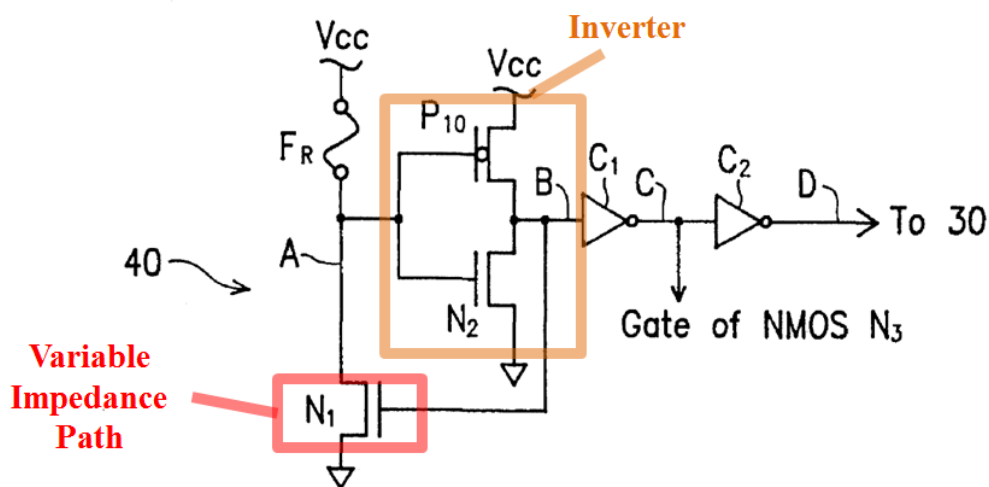


FIG. 4

(Ex. 1005 at FIG. 4 (annotated).)

105. Similarly, as demonstrated above with respect to claim feature 14[g], PMOS transistor P₁₀ and NMOS transistor N₂ together disclose the claimed “inverter.” (See my discussion above in Section IX.A.1(g).) The inverter formed

by PMOS transistor P_{10} and NMOS transistor N_2 is a “CMOS inverter” as it includes both NMOS and PMOS transistors (i.e., complementary MOS “CMOS” transistors). Such an understanding is consistent with the disclosure of the ’492 patent. (Ex. 1001 at 3:24-26, “Terminal OUT is connected to the input of CMOS inverter 120 formed by PMOS pull-up transistor 220 and NMOS pull-down transistor 230.”) Therefore, Fu discloses “wherein . . . the inverter is a CMOS inverter” as recited in claim 19.

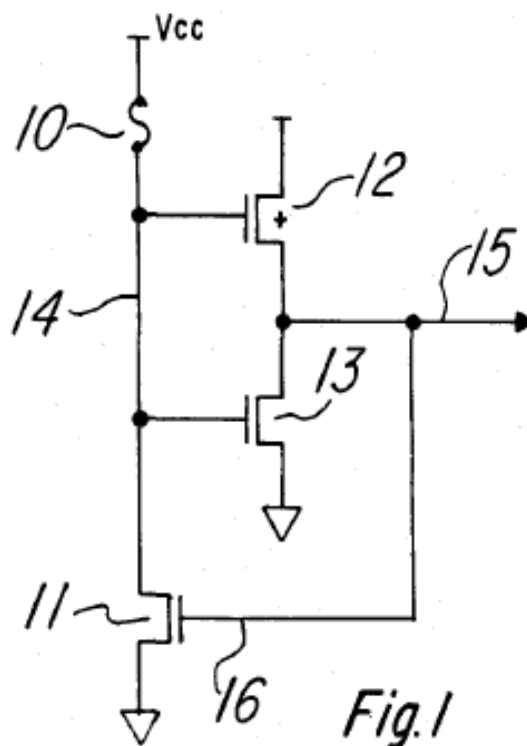
B. McAdams Discloses the Features of Claims 14-19

106. In my opinion, McAdams discloses all of the features of claim 14 of the ’492 patent.

1. Claim 14

a) “A programmable latch comprising:”

107. I understand that “[a] programmable latch comprising” is the preamble of claim 14. I have been asked to assume that the preamble is limiting. In my opinion, McAdams discloses this feature. For example, McAdams discloses a fuse circuit depicted in figure 1.



(Ex. 1006 at FIG. 1.)

108. McAdams describes the operation of the fuse circuit of figure 1 as follows:

Referring to FIG. 1, a fuse circuit constructed according to the invention is illustrated. **A fuse element 10** is connected in series with **an N-channel feedback transistor 11**, and this series circuit is connected between a supply voltage V_{cc} and V_{ss} . **A CMOS inverter including a P-channel transistor 12 and an N-channel transistor 13** has the node 14 as an input and produces an output 15. **Feedback is provided from the output node 15 to the gate of the transistor 11** by a line 16.

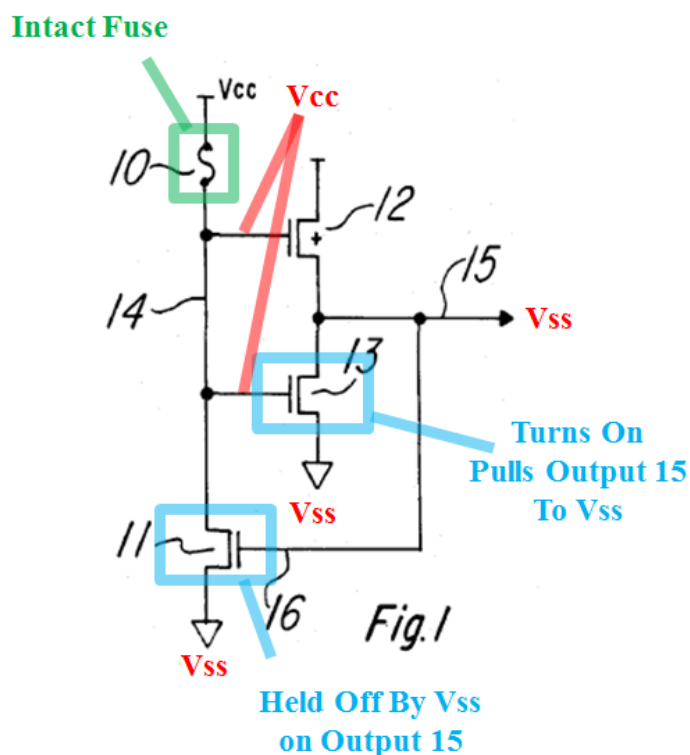
(*Id.* at 1:67-2:7 (emphases added).)

109. I have annotated figure 1 of McAdams below to show how the circuit of figure 1 operates when the fuse has not been blown. As shown, when the fuse 10 is intact and has not been blown when power is applied to the circuit, the node 14 follows the power supply V_{cc} , which turns on transistor 13. McAdams describes the operation of the circuit of figure 1 as follows:

During power-up of the supply voltage V_{cc} , as V_{cc} goes from zero to +5 v, if the fuse has not been blown, the node 14 follows V_{cc} since the node 15 starts at V_{ss} potential and the transistor 11 is off. Since the node 14 follows V_{cc} , the P-channel transistor 12 stays off. As soon as V_{cc} and node 14 reach the N-channel threshold voltage, V_{tn} , the transistor 13 turns on, holding the output node 15 at V_{ss} . This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to the V_{cc} transition, and so the transistor 11 is held off.

(*Id.* at 2:8-18.)

110. When transistor 13 turns on, any charge on the output node 15 is discharged, pulling the output 15 to V_{ss} . (*Id.*; see also my discussion above in Section V.B.) The V_{ss} voltage on the output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state. (Ex. 1006 at 2:8-18.)



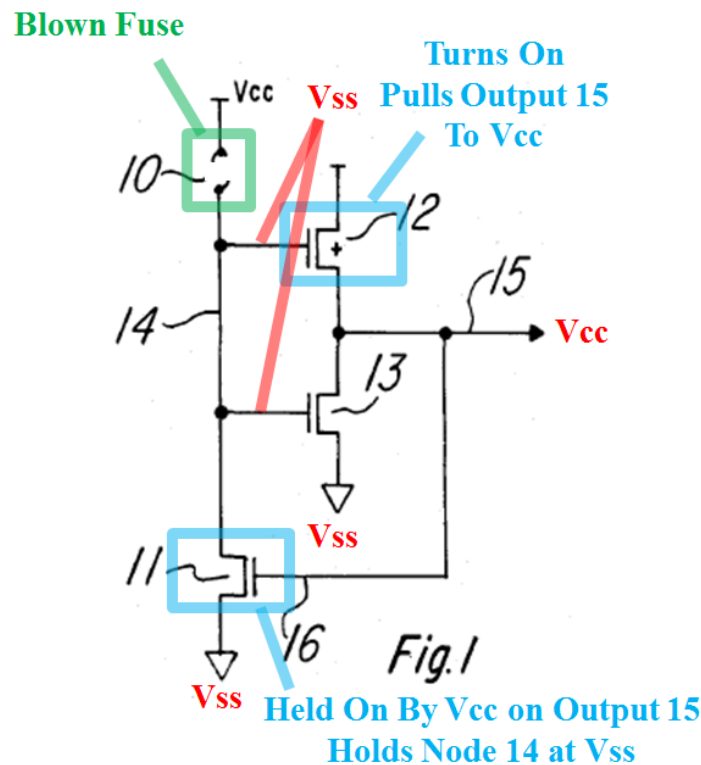
(*Id.* at FIG. 1 (annotated).)

111. I have also created a demonstrative in order to show how the circuit shown in figure 1 of McAdams operates when the fuse has been blown. As shown in the demonstrative below, the blown fuse includes a break (open circuit) in the conductor included inside the fuse 10. According to McAdams, when the fuse is blown, the node 14 is at Vss when power is applied. (*Id.* at 2:21-22.) Because the gate of P-channel transistor 12 is at Vss, transistor 12 turns on and the output node 15 is pulled to Vcc. (*Id.* at 2:22-24.) The Vcc voltage on the output is fed back to the gate of transistor 11, which turns transistor 11 on and holds the node 14 at Vss. (*Id.* at 2:24-26; *see also* my discussion above in Section V.B.) Holding node 14 at

V_{ss} ensures that the P-channel transistor 12 remains on and the output 15 is held is V_{cc}. McAdams discloses:

If the fuse 10 has been blown, as V_{cc} is powered up, node 14 is at V_{ss} and the P-channel transistor 12 turns on as soon as its threshold V_{tp} is reached, causing the output node 15 to follow V_{cc}. Once the node 15 reaches the threshold V_{tn}, the transistor 11 turns on, keeping the node 14 at V_{ss}.

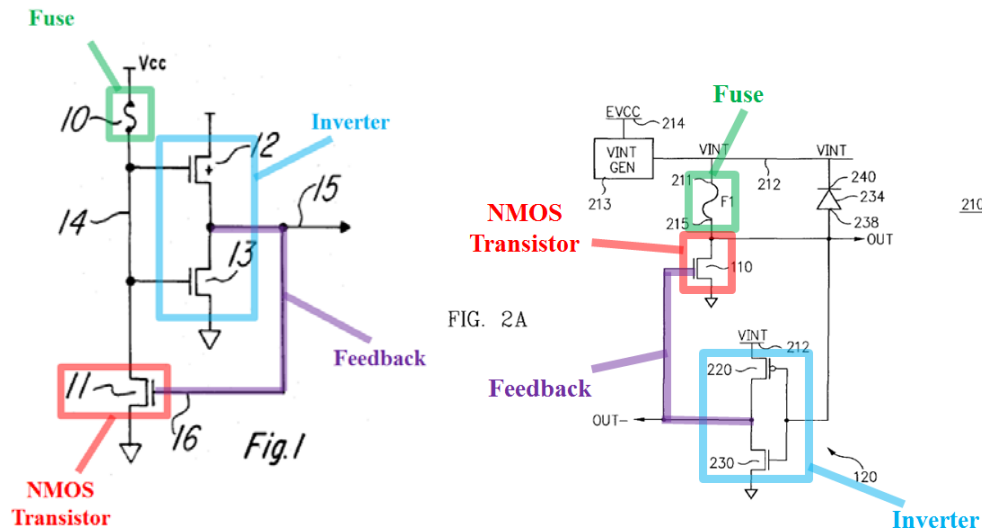
(Ex. 1006 at 2:21-26.)



(*Id.* at FIG. 1 (annotated and modified to show open circuit in fuse 10).)

112. Therefore, based on whether the fuse 10 has been blown or is intact, the output 15 of the fuse circuit shown in figure 1 will be held at either Vcc or Vss. (*Id.* at 2:8-26.) The feedback of the output of the inverter to the transistor 11 holds that output at Vcc or Vss. (*Id.*) Therefore, the output is latched at either Vcc or Vss based on whether or not the fuse is blown. (*Id.*) A person of ordinary skill in the art would have recognized that the fuse circuit constitutes a “programmable latch” where the programming corresponds to the state of the fuse, which determines the latched value at the output.

113. Indeed, a person of ordinary skill in the art would have recognized that the fuse circuit of McAdams corresponds to a “programmable latch” in the same manner as that disclosed in the figure 2A of the '492 patent. As shown in the annotated figures below, the programmable latch shown in figure 2A of the '492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the fuse circuit in figure 1 of McAdams. (Ex. 1001 at FIG. 2A; Ex. 1006 at FIG. 1.)

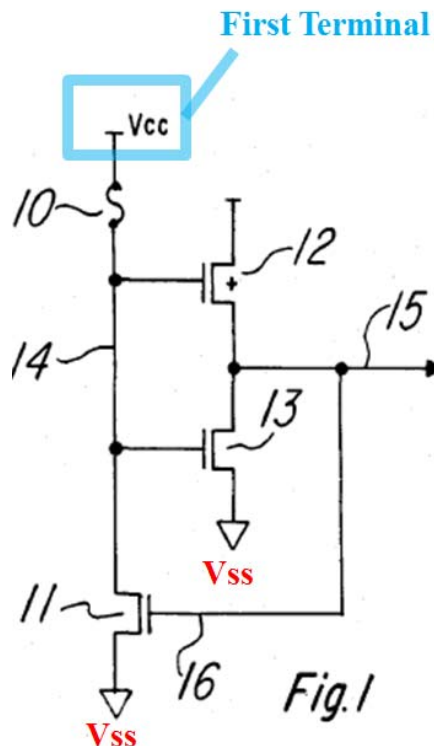


(Ex. 1006 at FIG. 1 (annotated); Ex. 1001 at FIG. 2A (annotated).)

b) “a first terminal for receiving a constant non-ground voltage throughout operation of the latch;”

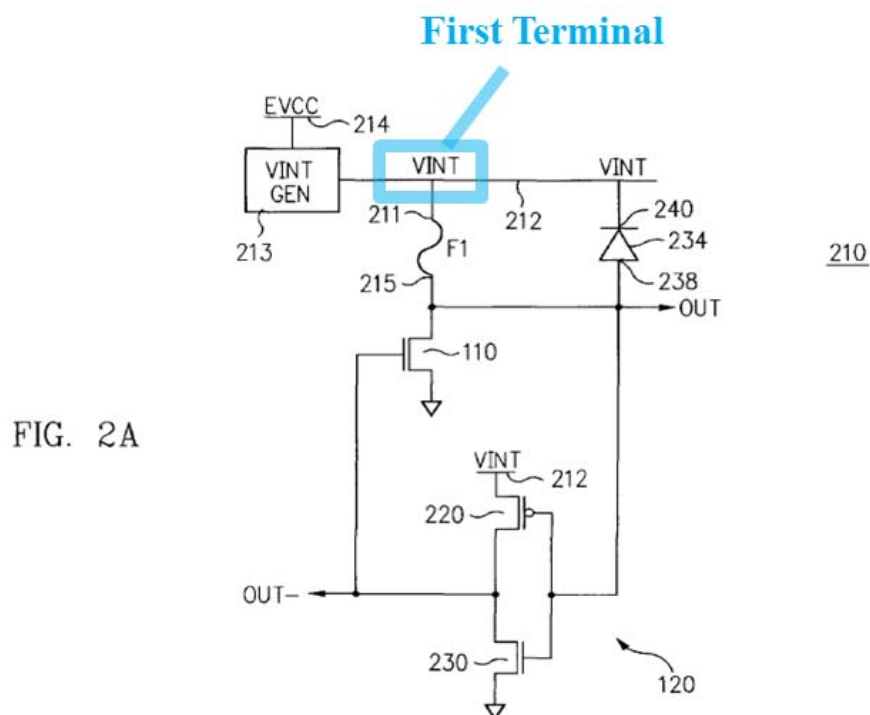
114. In my opinion, McAdams discloses this feature. As shown in annotated figure 1 below, the “programmable latch” of McAdams includes a “terminal” Vcc, where Vcc is a “supply voltage” that is applied when power is applied to the circuit of figure 1. (Ex. 1006 at 2:2-3, “series circuit is connected between a supply voltage Vcc and Vss”, 2:8-9, “During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v”, 3:24-26, “wherein said one of the first and second terminals of said power supply is a positive voltage and said other is ground”, 4:20-22, “a power supply having a first terminal at a positive voltage and a second terminal at a ground potential”). In the example embodiment of McAdams, Vcc is at +5 v after power up of the latch and therefore constitutes “a

constant non-ground voltage throughout operation of the latch.” A person of ordinary skill would have understood that the Vcc voltage of +5 v is a “constant” non-ground voltage because such a constant voltage is a requirement for proper circuit operation. Therefore, the terminal highlighted in blue below constitutes a “first terminal for receiving a constant non-ground voltage throughout operation of the latch.”



(Id. at FIG. 1 (annotated).)

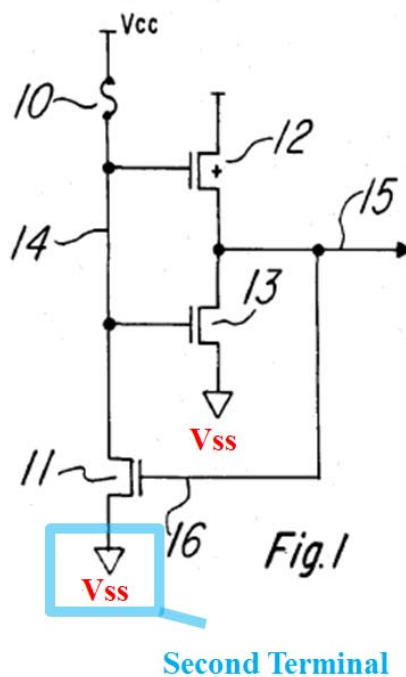
115. As shown in annotated figure 2A of the '492 patent below, the “first terminal” highlighted in figure 1 of McAdams above is consistent with the “first terminal” disclosed by the '492 patent.



(Ex. 1001 at FIG. 2A (annotated).)

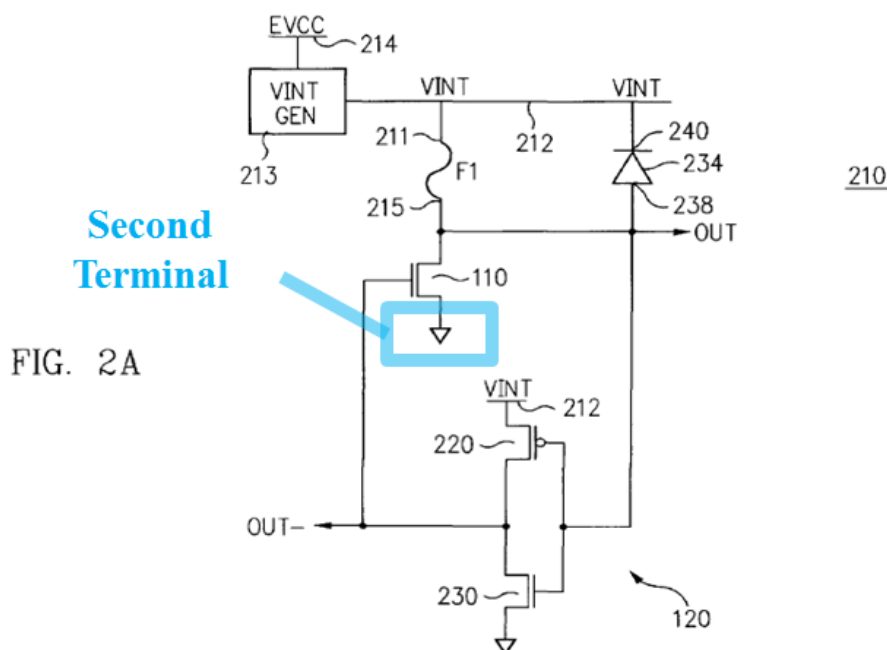
c) “a second terminal for receiving a voltage;”

116. In my opinion, McAdams discloses this feature. For example, the programmable latch circuit in figure 1 of McAdams includes a terminal (“second terminal”) for receiving V_{ss} (“a voltage”). (Ex. 1006 at 2:2-3, “series circuit is connected between a supply voltage V_{cc} and V_{ss} ”, 2:14-17, “[T]he transistor 13 turns on, holding the output node 15 at V_{ss} . This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to V_{cc} transition.”) Therefore, McAdams discloses “a second terminal for receiving a voltage.”



(*Id.* at FIG. 1 (annotated).)

117. As shown in annotated figure 2A of the '492 patent below, the "second terminal" highlighted in figure 1 of McAdams above is consistent with the "second terminal" disclosed by the '492 patent.

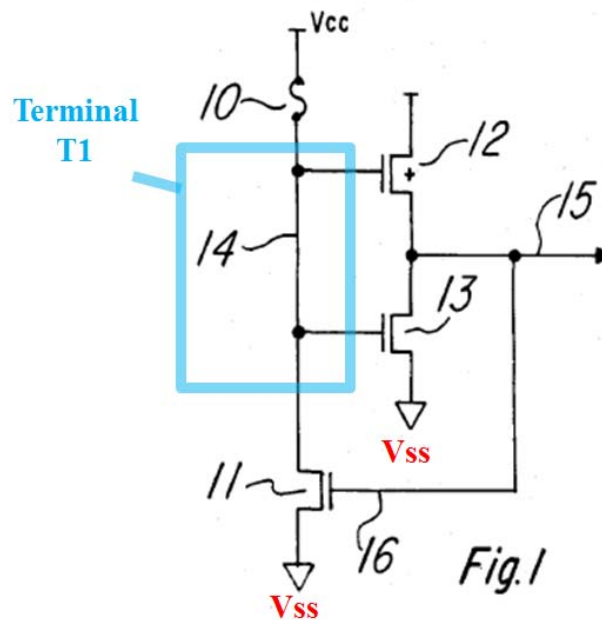


(Ex. 1001 at FIG. 2A (annotated).)

- d) “a terminal T1 for providing a signal indicating a state of the programmable latch;”

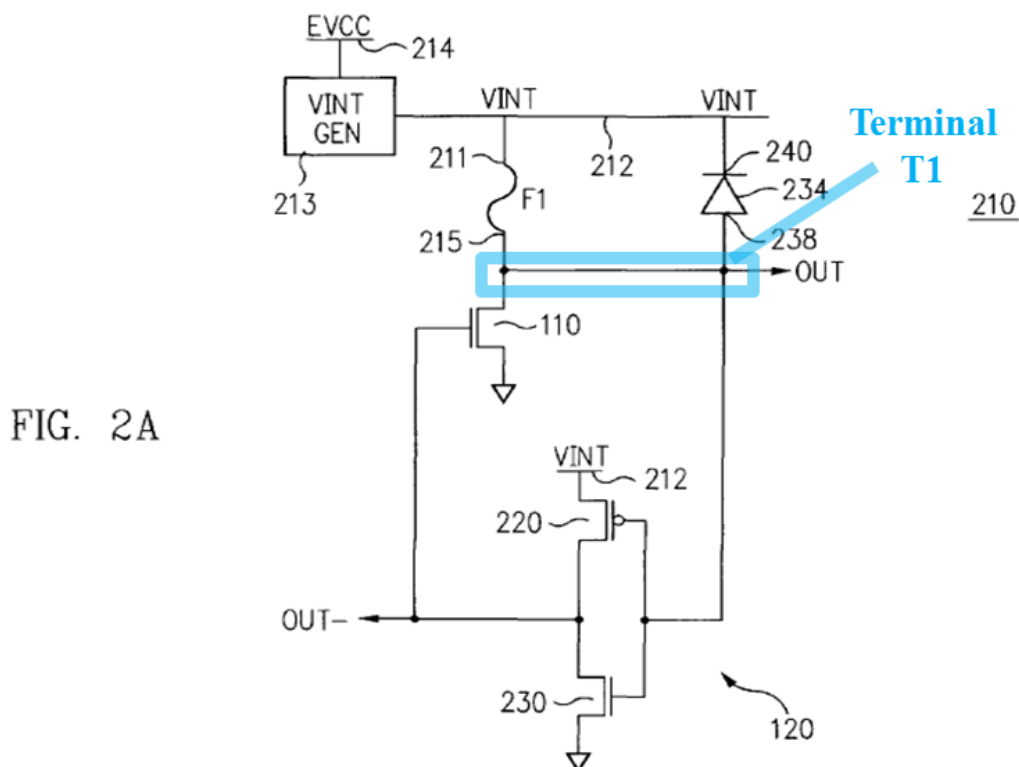
118. In my opinion, McAdams discloses this feature. For example, as shown in annotated figure 1 below, the node 14 indicates the state of the fuse, which corresponds to the state of the programmable latch (“a terminal T1 for providing a signal indicating a state of the programmable latch”). As discussed above with respect to claim element 14[a], when power is applied to the latch, if the fuse is intact, node 14 is at Vcc (high), but if the fuse is blown, node 14 is at Vss (low). (See my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.B.1(a).) Therefore, the voltage at node 14

indicates a “state of the programmable latch” because it indicates whether the fuse is blown or not.



(Ex. 1006 at FIG. 1 (annotated).)

119. As shown in annotated figure 2A of the '492 patent below, the “terminal T1” highlighted in figure 1 of McAdams above is consistent with the “terminal T1” disclosed by the '492 patent.

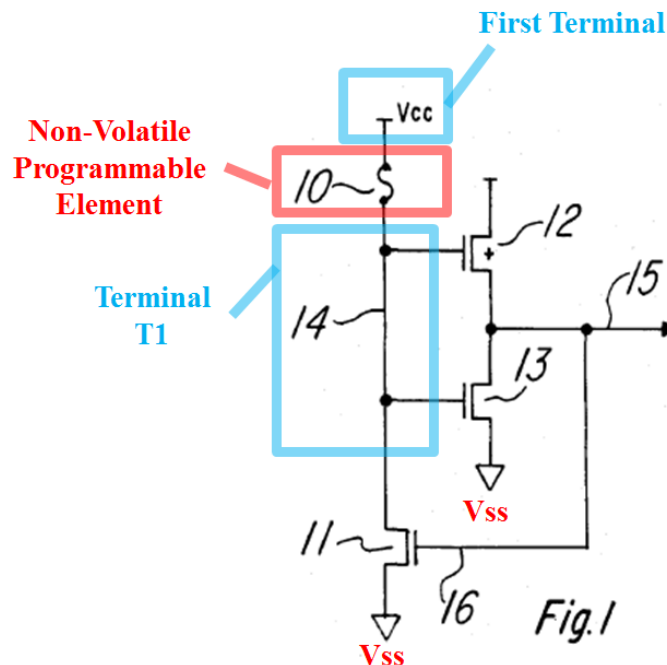


(Ex. 1001 at FIG. 2A (annotated).)

- e) “a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;”

120. In my opinion, McAdams discloses this feature. For example, the fuse 10 that I have highlighted in red in annotated figure 1 below is a “non-volatile programmable element.” Such an understanding is consistent with the disclosure of the ’492 patent, which shows a fuse as the “non-volatile programmable element”

in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 3:10-23, 7:24-36.) Moreover, claim 18, which depends from claim 14, recites “wherein the programmable element is a fuse.” Such a recitation in claim 18 makes clear to a person of ordinary skill in the art that a fuse is a “non-volatile programmable element” in the context of claim 14 and the ’492 patent. (*Id.* at 10:38-39.)



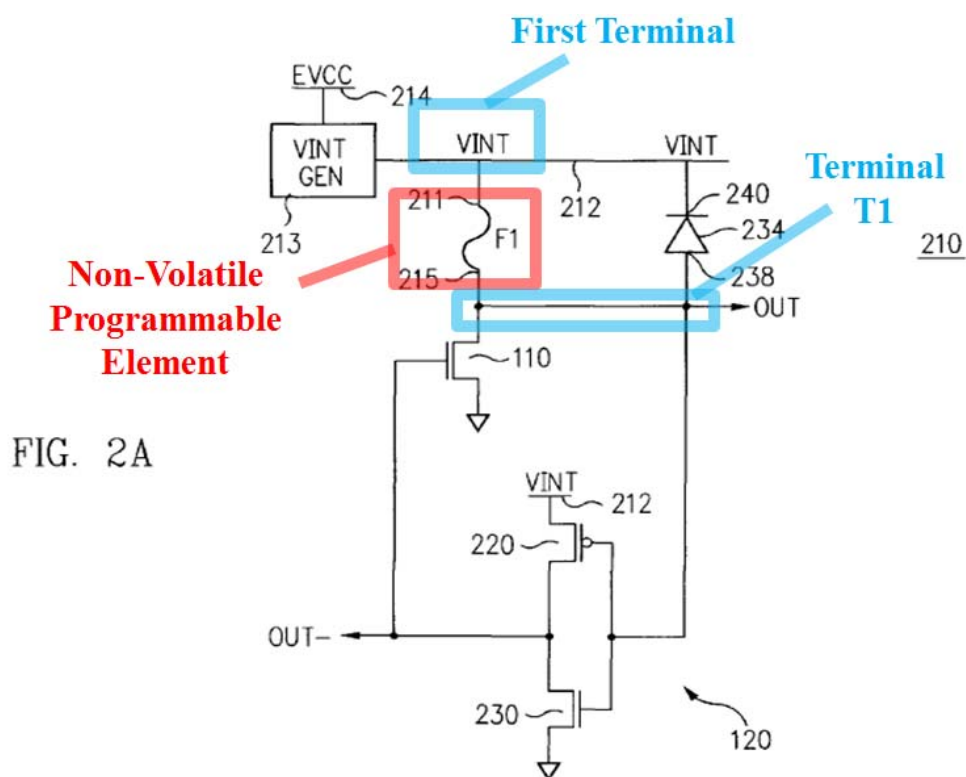
(Ex. 1006 at FIG. 1 (annotated).)

121. As shown in annotated figure 1 above, the fuse 10 (“non-volatile programmable element”) is coupled between Vcc (“first terminal”) and node 14 (“terminal T1”) and therefore constitutes “a non-volatile programmable element connected to the terminal T1 and the first terminal.”

122. If the fuse 10 is intact such that the conductor within the fuse is not broken or cut by, for example, a laser, the fuse allows current to flow between its two terminals (i.e., it is “conductive”). Therefore, when the fuse is intact and “conductive,” it provides an electrical connection between Vcc (“first terminal”) and node 14 (“terminal T1”). (*Id.* at 2:8-11; *see also* my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.B.1(a).) Therefore, in my opinion, McAdams discloses “the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive.”

123. If the fuse 10 is blown such that the conductor within the fuse is severed and there is an open circuit between the two terminals of the fuse, the fuse is non-conductive and does not allow current to flow between the terminals. Therefore, when the fuse is blown and “non-conductive,” the fuse does not provide an electrical connection between Vcc (“first terminal”) and node 14 (“terminal T1”). (*Id.* at 2:21-24 (explaining that even though Vcc is powered up, node 14 remains at Vss); *see also* my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.B.1(a).) As shown in figure 1 of McAdams, if the fuse is broken, there is no electrical path between Vcc and node 14, and therefore node 14 (“terminal T1”) is “isolated” from Vcc (“the first

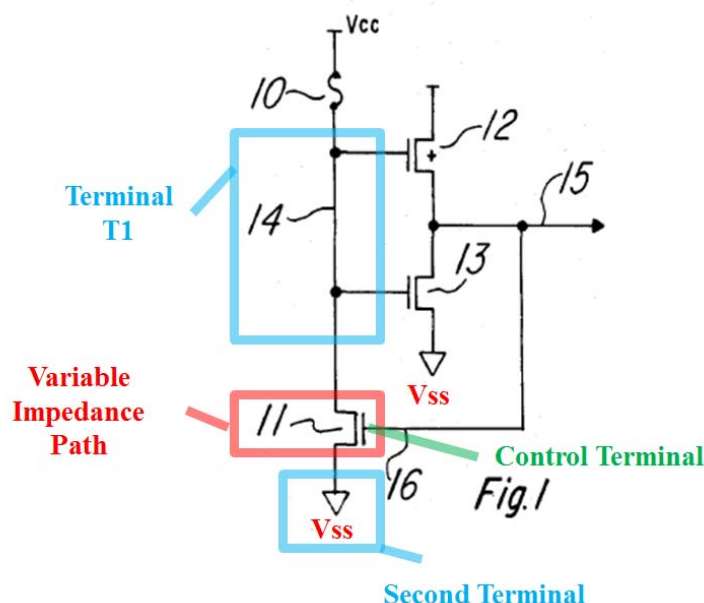
terminal”). Thus, “terminal T1” is isolated from the “first terminal.” Therefore, McAdams discloses “the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive.”



(Ex. 1001 at FIG. 2A (annotated).)

- f) “a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and”

125. In my opinion, McAdams discloses this feature. For example, a person of ordinary skill in the art would have understood that the N-channel (NMOS) transistor 11 highlighted below in annotated figure 1 is a “variable-impedance electrical path” as that term is used in the ’492 patent. Indeed, such an understanding is consistent with the disclosure of the ’492 patent, which shows an NMOS transistor as the “variable-impedance electrical path” in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 7:57-66.) I also understand that claim 19, which depends from claim 14, recites “wherein the variable-impedance electrical path is an NMOS transistor.” As such, a person of ordinary skill in the art would have understood that an NMOS transistor is a “variable-impedance electrical path” in the context of claim 14 and the ’492 patent. (*Id.* at 10:38-39.)



(Ex. 1006 at FIG. 1 (annotated).)

126. As shown in annotated figure 1 above, the NMOS transistor 11 (“variable-impedance electrical path”) is coupled between node 14 (“terminal T1”) and Vss (“second terminal”) and therefore constitutes a “variable-impedance electrical path connected between the terminal T1 and the second terminal.”

127. The gate terminal of the NMOS transistor N_1 determines whether the NMOS transistor is on or off. (See Section V.B above.) A person of ordinary skill in the art would have understood that the impedance of the transistor N_1 , where the impedance of the transistor includes its opposition to current flow, is less when the transistor is on than when the transistor is off. Therefore, the NMOS transistor 11 (“variable impedance path”) has a gate terminal (“having a control terminal”) that

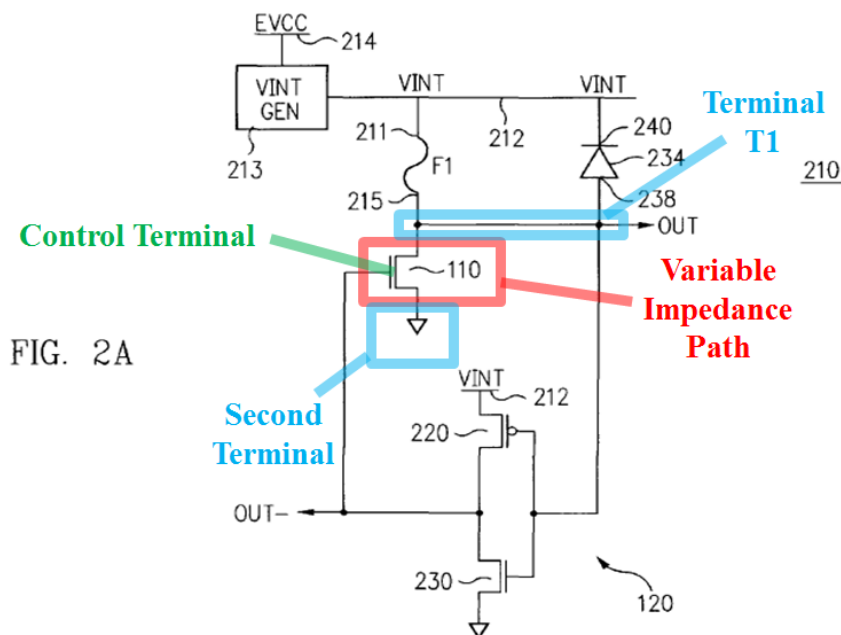
determines whether the NMOS transistor is on or off (“for controlling the impedance of the variable-impedance path”). McAdams discloses:

As soon as Vcc and node 14 reach the N-channel threshold voltage, Vtn, the transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to the Vcc transition, and so the transistor 11 is held off. Thus the only current flowing through the fuse 10 from the Vcc supply is leakage current, on the order of nanoamps....

If the fuse 10 has been blown, as Vcc is powered up, node 14 is at Vss and the P-channel transistor 12 turns on as soon as its threshold Vtp is reached, causing the output node 15 to follow Vcc. **Once the node 15 reaches the threshold Vtn, the transistor 11 turns on, keeping the node 14 at Vss.**

(*Id.* at 2:12-26 (emphasis added).)

128. As shown in annotated figure 2A of the '492 patent below, the “variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path” highlighted in figure 1 of McAdams above is consistent with the “variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path” disclosed by the '492 patent. (See Ex. 1001 at 3:31-32, 3:46-51.)

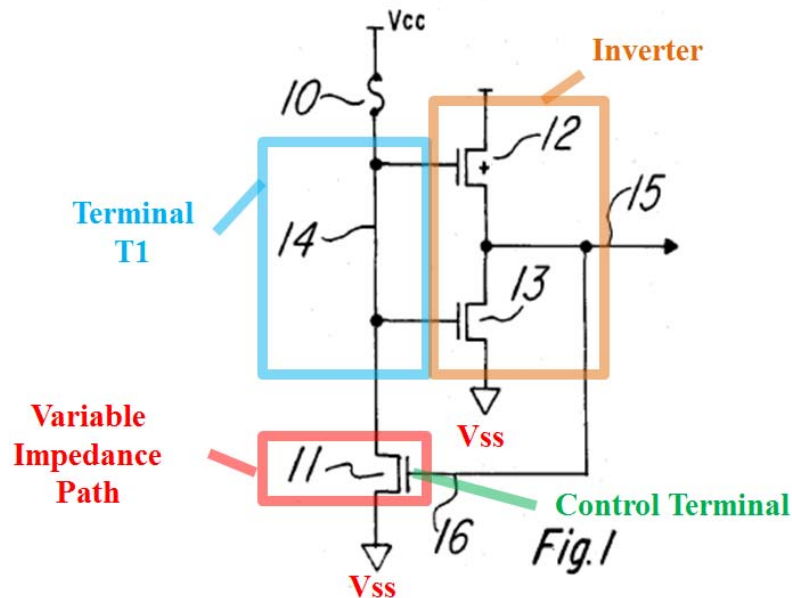


(Ex. 1001 at FIG. 2A (annotated).)

- g) “an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.”

129. In my opinion, McAdams discloses this feature. For example, as shown in annotated figure 1 of McAdams below, transistors 12 and 13 together form an inverter. (Ex. 1006 at FIG. 1, 2:3-6, “A CMOS inverter including a P-channel transistor 12 and an N-channel transistor 13 has the node 14 as an input and produces an output 15.”) The gates of transistors 12 and 13 (“the input of the inverter”) are connected to the node 14 (“terminal T1”). (*Id.* at FIG. 1, 2:3-6.) The

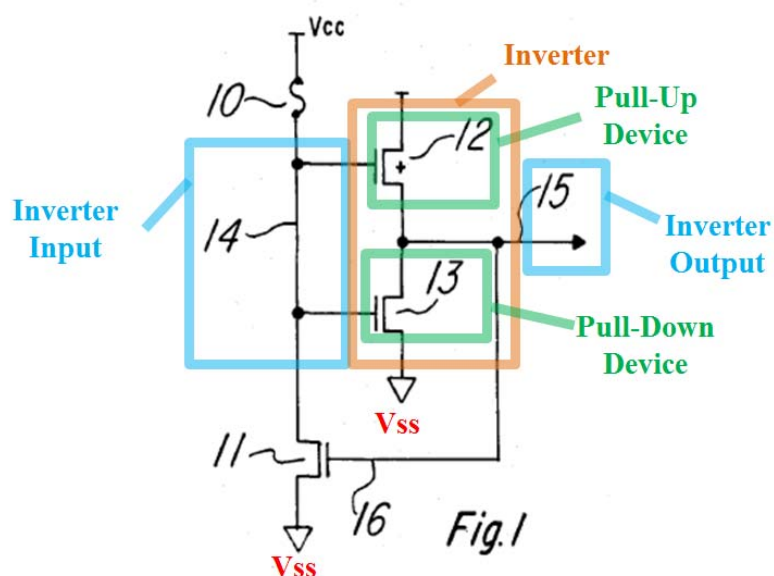
output 15 of the inverter is connected to the gate of the transistor 11 (“an output connected to the control terminal of the variable-impedance path”). (*Id.* at 2:6-7.)



(*Id.* at FIG. 1 (annotated).)

130. As I discussed above in section V.B, a person of ordinary skill in the art at the time of the invention would have understood that an inverter includes a pull-up device and a pull-down device. (See Section V.B above.) The inverter of McAdams includes a P-channel transistor 12 (“pull-up device”) coupled between the output 15 and Vcc, where, when the P-Channel transistor 12 is on, it pulls the voltage on output node 15 up to 5V and therefore would have been understood to operate as a “pull-up” transistor in the inverter. Similarly, the inverter includes N-channel transistor 13 (“pull-down device”) coupled between the output 15 and Vss,

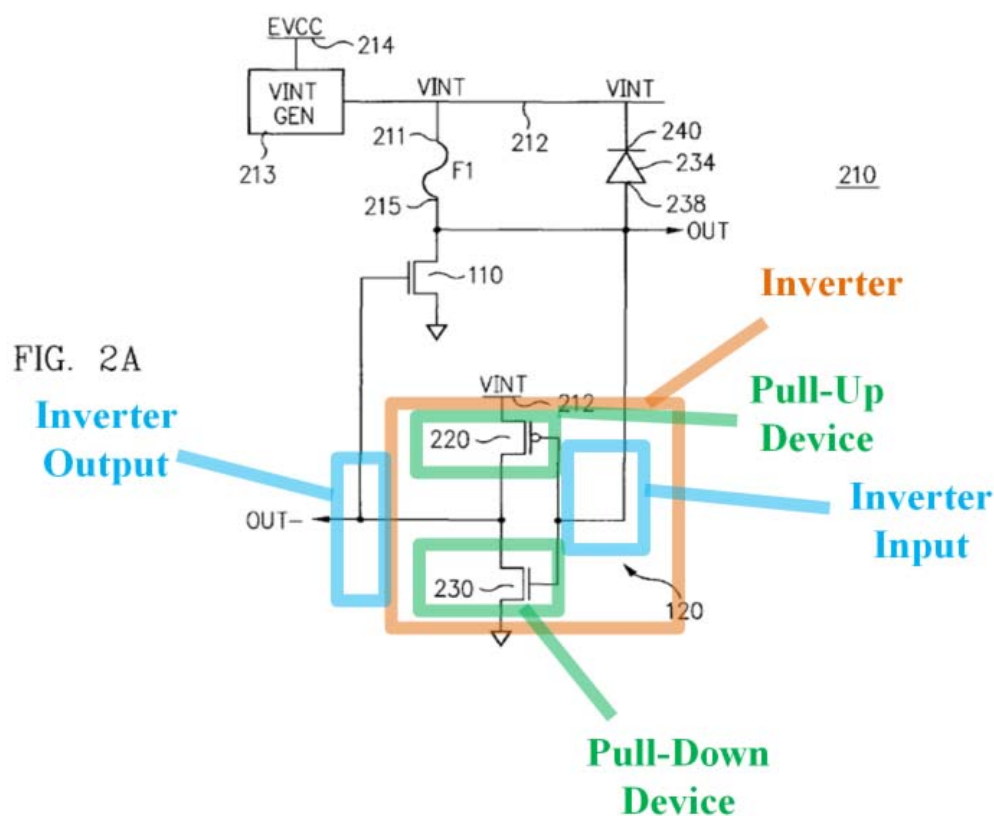
where, when the N-Channel transistor 13 is on, it pulls the voltage on output node 15 down to V_{ss} and therefore would have been understood to operate as a “pull-down” transistor in the inverter. (Ex. 1006 at FIG. 1, 2:3-6; see also my discussion above in Section V.B.)



(Ex. 1006 at FIG. 1 (annotated).)

131. As shown in annotated figure 1 above, both the P-channel transistor 12 (“pull-up device”) and the N-channel transistor 13 (“pull-down device”) are coupled to the inverter input at node 14 and the inverter output 15 (“at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output”). (Ex. 1006 at FIG. 1, 2:3-6.)

132. The disclosure of transistors 12 and 13 of McAdams being “pull-up” and “pull-down” devices, respectively, is consistent with the disclosure of the '492 patent, which shows the inverter including a PMOS transistor 220 (“pull-up device”) and an NMOS transistor (“pull-down device”) in figure 2A. (Ex. 1001 at 3:24-32, FIG. 2A.)

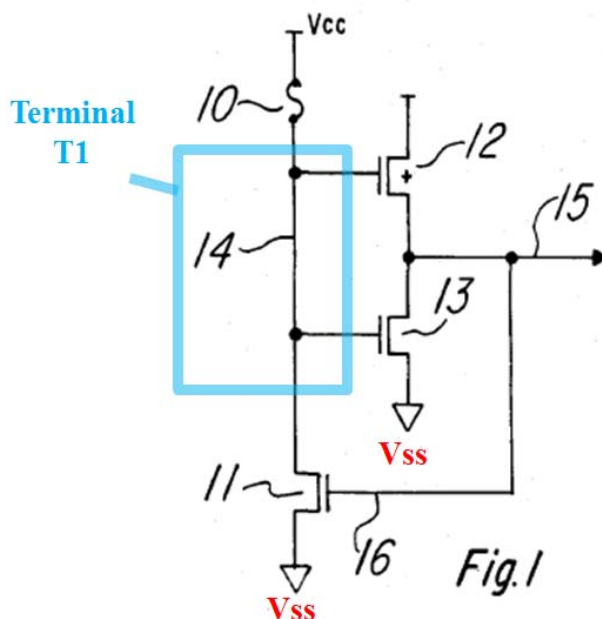


(*Id.* at FIG. 2A (annotated).)

2. Claim 15

a) “The programmable latch of claim 14 wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.”

133. In my opinion, McAdams discloses this feature. As shown in annotated figure 1 of McAdams below, the fuse circuit (“programmable latch”) of McAdams does not receive any inputs from outside of the circuit illustrated. (Ex. 1006 at FIG. 1.) As discussed above with respect to claim feature 14[a], when power is applied, the voltage at node 14 (“terminal T1”) is only influenced by the power supply voltage Vcc and Vss terminals (“first and second terminals”) and the state of the fuse 10 (“programmable element”). (*Id.* at 1:67-2:33; *see also* my discussion above in Section IX.B.1(a).)



(Ex. 1006 at FIG. 1 (annotated).)

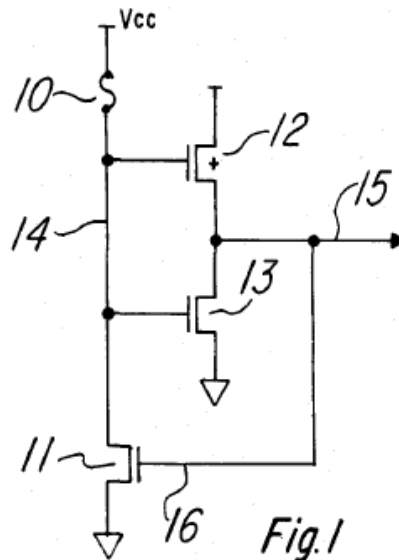
134. Therefore, McAdams discloses “wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.”

3. Claim 16

a) “The programmable latch of claim 14 wherein the latch does not receive any latch initialization signal from outside the latch.”

135. In my opinion, McAdams discloses this feature. As shown in figure 1 of McAdams below, the fuse circuit (“programmable latch”) of McAdams does not receive any inputs from outside of the circuit illustrated and the state of the latch is

completely determined by the state of the fuse 10 and the voltages on the Vcc and Vss terminals. (See my discussion above in Section IX.B.2; Ex. 1006 at FIG. 1.)



(*Id.* at FIG. 1.)

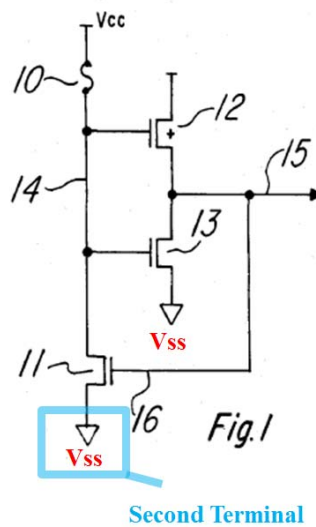
136. Therefore, McAdams discloses “wherein the latch does not receive any latch initialization signal from outside the latch.”

4. Claim 17

a) “The programmable latch of claim 14 wherein the second terminal is to receive a ground voltage throughout operation of the latch.”

137. In my opinion, McAdams discloses this feature. As discussed above with respect to claim element 14[c], when power is applied to the fuse circuit (“programmable latch”), the second terminal is connected to Vss throughout operation of the latch. (See my discussion above at Section IX.B.1(c).) McAdams

confirms that Vss is a ground voltage because it states that when node 15 is pulled low to Vss, the voltage thereon is zero volts. (Ex. 1006 at 2:14-17, “[T]he transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to Vcc transition.”) The claims of McAdams further confirm that Vss corresponds to ground (0V). (*Id.* at 3:24-26, “one of the first and second terminals of said power supply is a positive voltage and said other is ground”; *see also id.* at 4:20-22, “a power supply having a first terminal at a positive voltage and a second terminal at a ground potential” (emphasis added), 2:2-3 (explaining that Vss and Vcc are the two terminals of the supply voltage).)



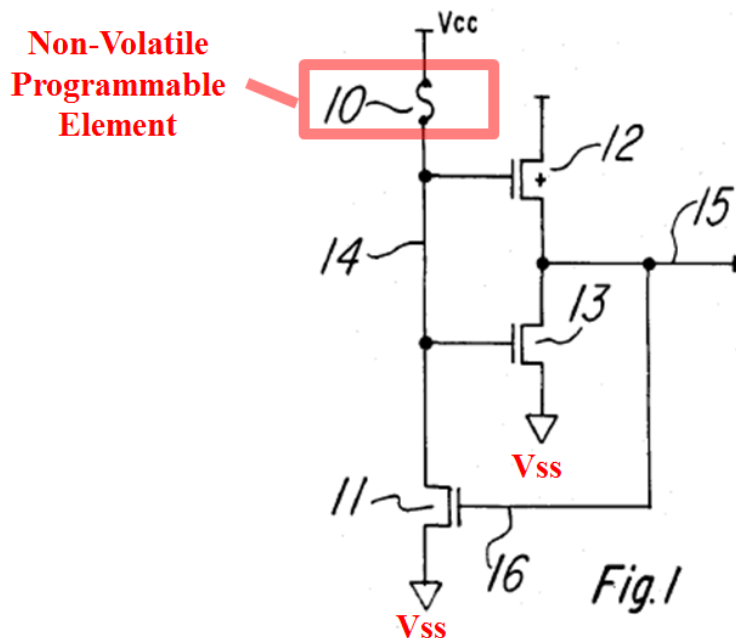
(*Id.* at FIG. 1 (annotated).)

138. Therefore, McAdams discloses that “the second terminal is to receive a ground voltage throughout operation of the latch” as recited in claim 17.

5. Claim 18

a) “The programmable latch of claim 14 wherein the programmable element is a fuse.”

139. In my opinion, McAdams discloses this feature. As demonstrated above with respect to claim feature 14[e], the fuse 10 shown in annotated figure 1 below is a “non-volatile programmable element.” (See my discussion above in Section IX.B.1(e).) Therefore, McAdams discloses “wherein the programmable element is a fuse.”

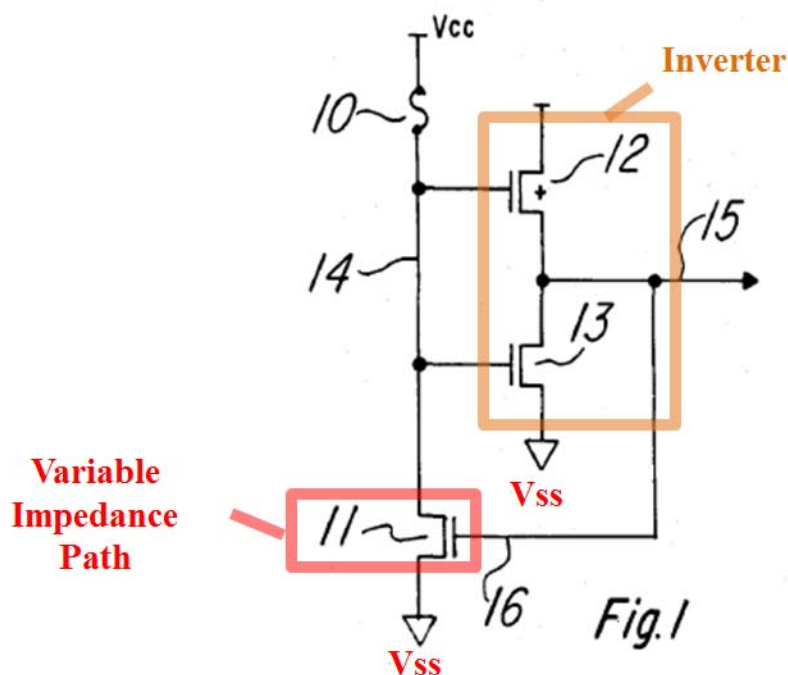


(Ex. 1006 at FIG. 1 (annotated).)

6. Claim 19

a) “The programmable latch of claim 14 wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.”

140. In my opinion, McAdams discloses this feature. As demonstrated above with respect to claim features 14[f] and 14[g], the N-channel (NMOS) transistor 11 in annotated figure 1 below corresponds to the claimed “variable impedance electrical path” and the CMOS inverter that includes PMOS transistor 12 and NMOS transistor 13 corresponds to the claimed “inverter.” (See my discussion above in Sections IX.B.1(f)-(g).) Therefore, McAdams discloses “wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.”



(Ex. 1006 at FIG. 1 (annotated).)

C. Fu in Combination with Sugibayashi Discloses or Suggests the Features of Claims 14-19

141. In my opinion, Fu in view of Sugibayashi discloses or suggests all of the features of claims 14-19 of the '492 patent.

1. Claim 14

142. As I discussed above in Section IX.A, it is my opinion that Fu discloses all of the features of claim 14. (See my analysis above in Section V.A.) For example, as I discussed above, the circuit of figure 4 of Fu includes a “first terminal” to which a constant non-ground voltage (Vcc) is applied when the circuit of figure 4 operates. (See my analysis above in Section IX.A.1(b).)

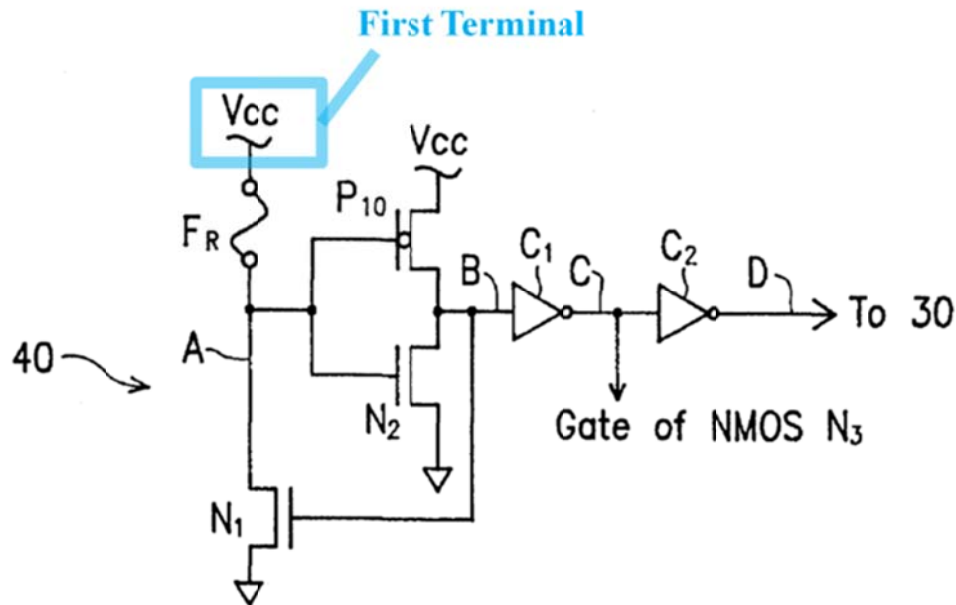


FIG. 4

(Ex. 1005 at FIG. 4 (annotated).)

143. I have been asked to consider a scenario in which Patent Owner contends that the voltage on the Vcc terminal in Fu is not “a *constant* non-ground voltage throughout operation of the latch,” as recited in claim element 14(b). I disagree with that assertion for reasons I discussed above in Section IX.A.1(b).

144. But even if Patent Owner's contention was assumed to be correct for the sake of argument, it is my opinion that a person of ordinary skill would nevertheless have been motivated in view of Sugibayashi to provide the supply voltage V_{cc} in a manner that ensures it is constant throughout the operation of the

memory in which the latch is included. As I discuss below, in view of Sugibayashi, a person of ordinary skill in the art would have been motivated to include an internal voltage supply generating circuit in the semiconductor memory as disclosed in Fu to ensure that the voltage on the terminal Vcc is constant throughout the operation of the latch.

145. In my opinion, a person of ordinary skill in the art would have known that in memory devices such as the one disclosed in Fu, the power supply (e.g., Vcc) provided to circuits in the memory device fluctuated, which was a problem because such fluctuations caused malfunction of the circuit components. As I explain below, Sugibayashi provided a known solution to this known problem by disclosing an internal voltage supply generator that generated a constant voltage for the circuit components of the memory chip.

146. In my opinion, a person of ordinary skill would have known that fluctuations in the power supply voltage used within a memory device can negatively impact the functionality of a memory device. For example, Sugibayashi discloses:

[I]f the external power voltage Vcc is undesirably decayed under the target level Vreg due to, for example, turbulence in the external power supply system, the undesirable voltage drop

decreases the differential voltage between the source and drain of the p-channel enhancement type variable load transistor Q1.

(Ex. 1011 at 2:33-38.)

[A] problem is encountered in the prior art dynamic random access memory device in that malfunction takes place in internal component circuits (not shown) powered with the internal power voltage V_{int} . The storage capacitor of the memory cell is one of the internal component circuits affectable by the voltage fluctuation of the internal power voltage V_{int} . In detail, when the external power voltage V_{cc} is decayed below the target level V_{reg} , the detection circuit I allows the p-channel enhancement type variable load transistor Q2 to supplement current to the power voltage line PW2. The detection circuit produces the gate control signal SEN when the external power voltage level V_{cc} is decayed under a critical level V_{sen} , and the critical level V_{sen} is slightly higher than the target level V_{reg} as shown in FIG. 4. Such a voltage margin between the critical level V_{sen} and the target level V_{reg} retards rapid voltage drop on the power supply line PW2. However, after the p-channel enhancement type variable load transistor Q2 turns on, the power supply line PW2 is dominated by the external power voltage level V_{cc} , and the power supply line PW2 is rapidly elevated to the voltage level equal to the critical level V_{sen} . If the external power voltage V_{cc} is continuously decreased from the critical level V_{sen} , the internal power

voltage V_{int} follows the external power voltage V_{cc} , and the internal power voltage traces V_{int} of FIG. 4. As a result, an overshoot OS takes place while the external power voltage v_{cc} passes through the range between the critical level V_{sen} and the target level V_{reg} . The overshoot OS decreases voltage margin for the internal component circuits (not shown) powered with the internal power voltage V_{int} , and malfunction is liable to take place due to the loss of the voltage margin.

(*Id.* at 2:58-3:24.)

As will be better seen from the foregoing description, the decrement of the step-down power voltage V_{int} cancels an overshoot due to the current through the p-channel enhancement type variable load transistor 12f, and the internal power supply system 12 keeps the step-down power voltage V_{int} constant in so far as the external power voltage V_{cc} is higher than the reference level REF. For this reason, the step-down power voltage V_{int} does not decrease the voltage margin for the component circuits, and any malfunction never take place.

(*Id.* at 7:5-15.)

147. Therefore, it is my opinion that a person of ordinary skill would have known that it was desirable to provide a stable (i.e., constant) supply voltage to the circuitry on the memory device to ensure proper operation. Such a skilled person

also knew that, from the perspective of the semiconductor memory device itself (e.g. a memory chip), the external voltage supplied to the memory device is not under control of the memory device. Therefore, in my opinion, it was routine for memory chip designers to include an internal voltage supply generator in the memory chip, where the internal voltage supply generator receives an external voltage supply and generates an internal supply for the circuits on the memory chip. For example, Sugibayashi explains:

A typical example of the dynamic random access memory device is disclosed by Nakagome et al. in "Low-voltage Circuit Technology for 64 Mb DRAMs", IEICE Technical Report, ICD90-200, pages 7 to 13. FIG. 1 illustrates an internal power circuit incorporated in the dynamic random access memory device disclosed in the paper.

(Ex. 1011 at 1:16-22.)

148. Similarly, Jung explains that “by installing on-chip an internal power-supply voltage supplier, regardless of the external power-supply voltage a constant voltage is applied to the interior of the memory device.” (Ex. 1012 at 1:19-23.)

149. As I explain below, Sugibayashi provides an example of a well-known internal power-supply generator that was capable of providing a constant internal power supply to the circuits of the memory chip.

150. Sugibayashi discloses “a dynamic random access memory device embodying the present invention is fabricated on a single semiconductor chip 11, and largely comprises an internal power supply system 12 for producing a step-down power voltage V_{int} ” (Ex. 1011 at 4:40-45.) Sugibayashi further discloses that the disclosed “internal power supply system [] does not produce any overshoot upon fluctuation of an external power supply” (*id.* at 3:28-31), where the internal power supply “keep[s] the step-down power voltage constant” (*id.* at 3:55; *see also id.* at 3:39-68).

151. According to Sugibayashi, while internal voltage supply generators for memory devices such as DRAMs were known, such prior art voltage supply generators could result in malfunctions in the internal component circuits of the memories as a result of the loss of voltage margin caused by an overshoot (OS) condition. (*Id.* at 2:58-3:24.) The overshoot condition in Sugibayashi is shown in figure 4, where the overshoot (OS) corresponds to when the internal voltage supply generated (V_{int}) exceeds the target voltage level (V_{reg}). (*Id.*; *id.* at FIG. 4 (annotated below).)

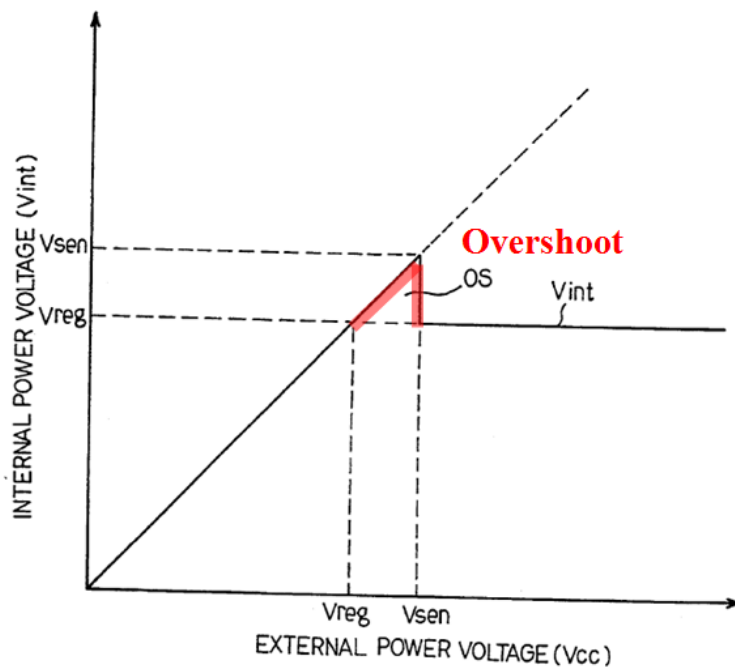


Fig. 4
PRIOR ART

(Ex. 1011 at FIG. 4 (annotated).)

152. In order to avoid the malfunctions that could result from the overshoot on the internal voltage (V_{int}), Sugibayashi discloses an internal power supply system 12 depicted in annotated figure 5 below. (Ex. 1011 at 4:40-52.)

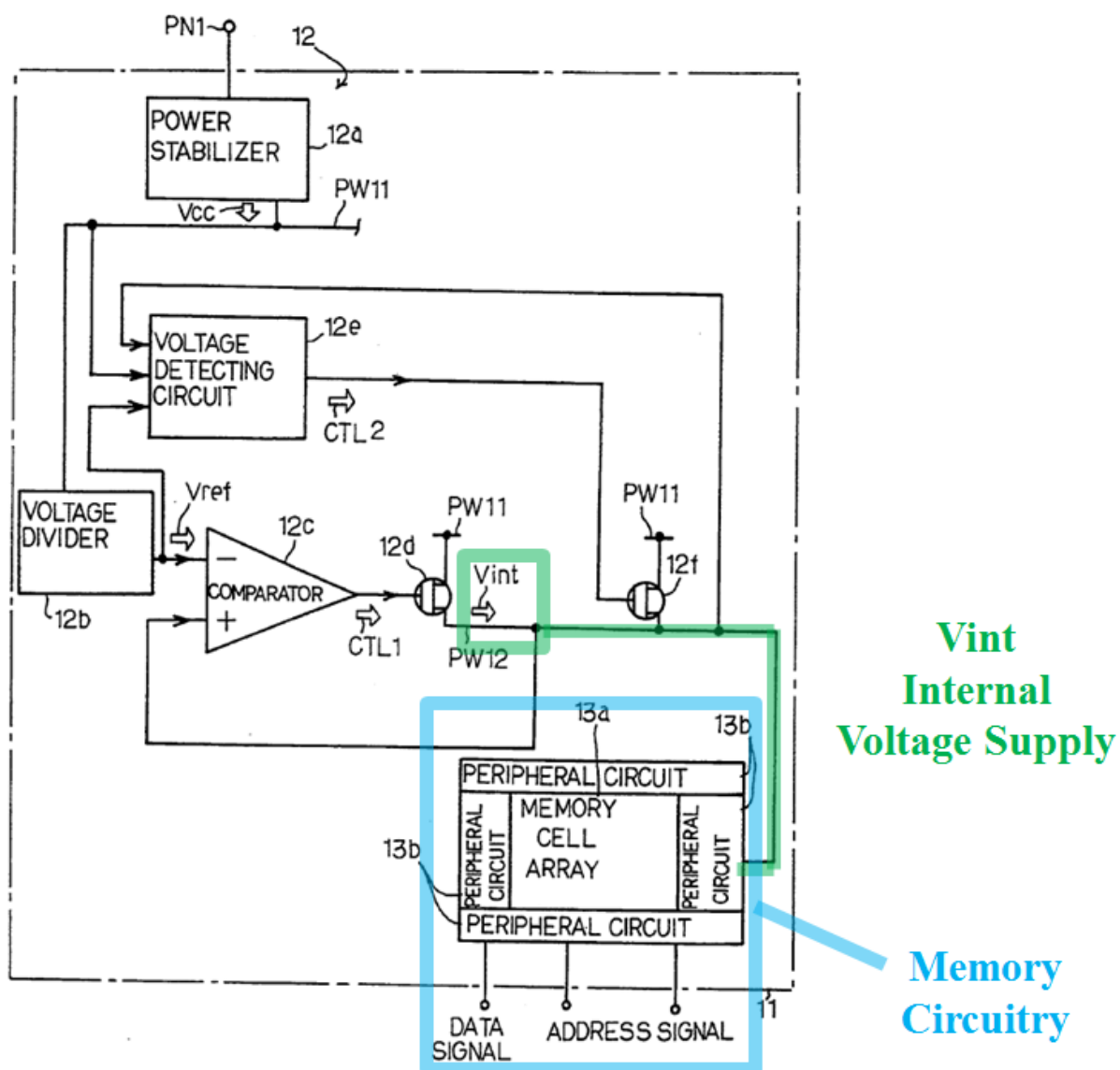


Fig. 5

(Ex. 1011 at FIG. 5 (annotated); *see also id.* at 4:40-52 (below).)

Referring to FIG. 5 of the drawings, a dynamic random access memory device embodying the present invention is fabricated on a single semiconductor chip 11, and largely comprises an internal power supply system 12 for producing a step-down

power voltage V_{int} and a dynamic random access memory cell array 13a accompanied with peripheral circuits 13b such as address decoders, a precharging circuit, sense amplifier circuits, a column selector and a data buffer circuit. The dynamic random access memory cell array 13a and the peripheral circuits 13b serve as a main circuit. However, they are well known to those skilled in the art, and no further description is incorporated hereinbelow.

(*Id.* at 4:40-52.)

153. As shown in annotated figure 5 above, a comparator 12c compares the internal voltage V_{int} with a reference voltage V_{ref} , and, based on whether the internal voltage V_{int} is greater or less than V_{ref} , comparator 12c controls the transistor 12d to keep V_{int} at the desired reference voltage level V_{ref} . (*Id.* at 5:7-31, FIG. 5.) The internal power supply system 12 shown above also includes voltage detecting circuit 12e, which, in combination with variable load transistor 12f, ensures that variations in the external power voltage V_{cc} do not result in similar variations on the internal voltage supply V_{int} . (*Id.* at 6:48-68 (describing that when there is “turbulence in an external supply system” the “step-down power voltage V_{int} is *kept constant* as shown in FIG. 8”) (emphasis added).)

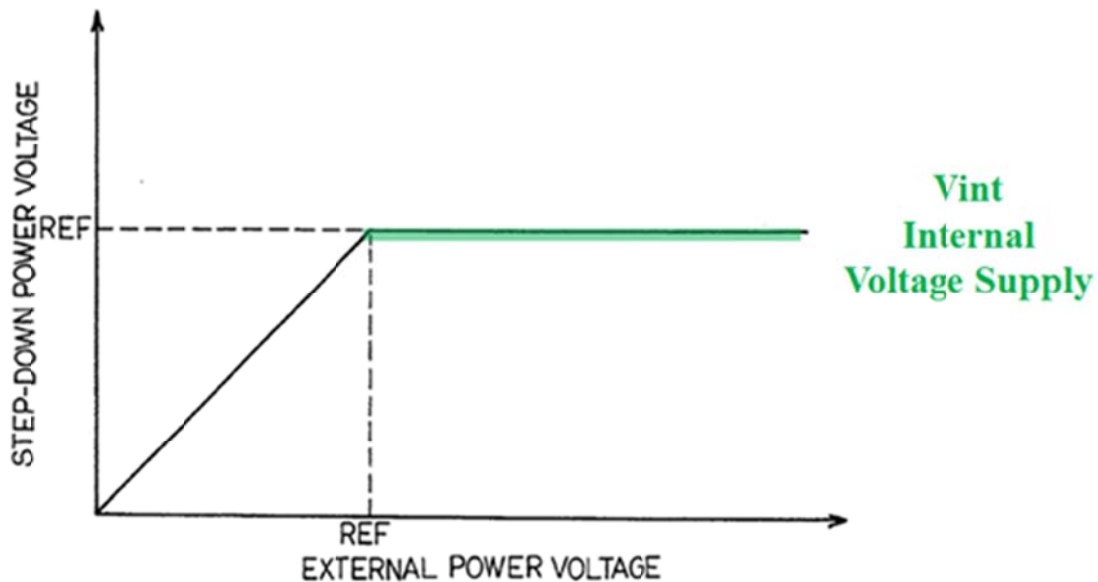


Fig.8

(Id. at FIG. 8 (annotated).)

154. In my opinion, based on the teachings of Sugibayashi, a person of ordinary skill in the art would have been motivated to modify the circuit of figure 4 in Fu such that the Vcc supply voltage in Fu is provided by an internal voltage supply generator similar to the one disclosed in Sugibayashi *in order to ensure a constant internal supply voltage and avoid malfunctions in internal component circuits of the memory*. Such skilled person would have looked to Sugibayashi because, for example, Sugibayashi, like Fu, is related to integrated circuit memory devices.

Reference is now made to FIG. 2 in which the schematic diagram of a memory redundancy circuitry in accordance with the present invention is shown. The memory redundancy circuitry 2 of the present invention is suitable for being utilized by a main memory cell array 50 of a semiconductor memory device, as shown in FIG. 3, namely a memory integrated circuit device, for backing up the main memory cell array 50 by providing redundant memory cells 60 and their activation circuitry 40.

(Ex. 1005 at 3:27-35.)

This invention relates to an integrated circuit device and, more particularly, to an ultra large scale integration such as, for example, a dynamic random access memory device equipped with an internal step-down circuit.

(Ex. 1011 at 1:9-13; *see also id.* at 4:40-48.)

155. In my opinion, having looked to Sugibayashi, a person of ordinary skill would have been motivated to combine the teachings of Sugibayashi with Fu to implement an internal voltage supply generator (like in Sugibayashi) to generate the voltage supply V_{cc} that is provided to the internal component circuits of Fu's memory, including the latch circuit shown in figure 4 of Fu, for at least the following reasons.

156. First, such a modification of Fu would have been within the capabilities of a person of ordinary skill because Sugibayashi discloses how such an internal supply voltage generator is included in a semiconductor memory device and explains how the internal supply voltage generator operates to ensure a *constant* internal voltage in spite of variations in the external voltage supply. In my opinion, a person having ordinary skill in the art would have had the capability to implement the above modification of Fu's memory device in such a way to ensure the combination would work for its intended purpose of providing a constant Vcc voltage to Fu's figure 4 circuit.

157. Second, as I discussed above, a person of ordinary skill would have recognized a benefit to making such a modification because it would have resulted in a memory device that is less likely to suffer malfunctions due to variations in the external power supply voltage.

158. In my opinion, a person of ordinary skill in the art would have recognized that applying Sugibayashi's technique (e.g., generating a constant internal voltage from an external power supply voltage) to Fu's memory device would have improved Fu's device in the same way Sugibayashi's technique improves Sugibayashi's memory device (e.g., prevents malfunctioning of the

circuits within the memory device); and such application was within the level of ordinary skill.

159. Including the internal supply voltage generator as disclosed by Sugibayashi with the circuit of figure 4 of Fu would not have negatively impacted the disclosed circuit in Fu and would have solved a known problem of circuit malfunction in memory devices like Fu.

160. Therefore, in my opinion the combined Fu-Sugibayashi circuit discloses or suggests “a constant non-ground voltage throughout operation of the latch” because in the combination, Vcc (“non-ground voltage”) is produced by an internal voltage generator that produces a constant voltage.

161. It is my opinion that Fu in combination with Sugibayashi discloses or suggests the remaining limitations of claim 14 for the reasons I discussed above for claim 14 in Section IX.A.1, with the only modification to my analysis for claim 14 being the one I discussed above. (See my analysis above in Sections IX.A.1(a)-(g).)

2. Claims 15-19

162. Fu in combination with Sugibayashi discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.A.2-6. The same analysis presented above for these claims in Section IX.A is

applicable for the Fu-Sugibayashi combination discussed above in Section IX.C.1. That is, the combination of Sugibayashi with Fu for claim 14 does not affect the analysis for claims 15-19 in Section IX.A except that the ground for these claims is modified to include Sugibayashi.

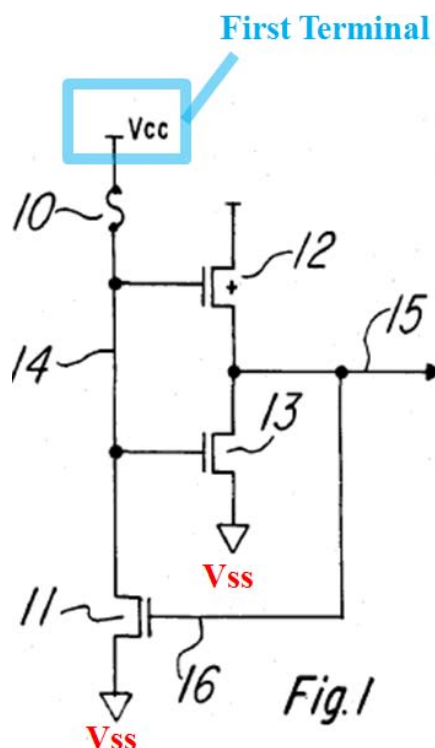
D. McAdams in Combination with Sugibayashi Discloses or Suggests the Features of Claims 14-19

163. In my opinion, McAdams in view of Sugibayashi discloses or suggests all of the features of claims 14-19 of the '492 patent.

1. Claim 14

164. As I discussed above in Section IX.B.1, it is my opinion that McAdams discloses all of the features of claim 14. For example, as I discussed above, McAdams includes a “first terminal” Vcc, where Vcc is a “supply voltage” that is applied when power is applied to the circuit of figure 1. (See my analysis above in Section IX.B.1(b); Ex. 1006 at 2:2-3 (“[T]his series circuit is connected between a supply voltage Vcc and Vss.”), 2:8-9 (“During power-up of the supply voltage Vcc, as Vcc goes from zero to +5 v...”), 3:24-26 (“said one of the first and second terminals of said power supply is a positive voltage and said other is ground”), 4:20-22 (“a power supply having a first terminal at a positive voltage and a second terminal at a ground potential”).) As I additionally discussed above, Vcc is at +5 v after power up of the latch and therefore is “a constant non-ground

voltage throughout operation of the latch.” (See my citations and analysis above in Section IX.B.1(b).) Therefore, in my opinion the terminal highlighted in blue below constitutes a “first terminal for receiving a constant non-ground voltage throughout operation of the latch.”



(Ex. 1006 at FIG. 1 (annotated).)

165. I have been asked to consider a scenario in which Patent Owner contends that the voltage on the Vcc terminal in McAdams is not “a *constant* non-ground voltage throughout operation of the latch,” as recited in claim element 14(b) (see above in Section IX.B.1(b).) I disagree with that assertion for reasons I discussed above in Section IX.B.1(b).

166. But even if Patent Owner's contention was assumed to be correct for the sake of argument, it is my opinion that a person of ordinary skill would have been motivated in view of Sugibayashi to provide the supply voltage V_{cc} in a manner that ensures it is constant throughout the operation of the memory in which the latch is included. As I discuss below, in view of Sugibayashi, a person of ordinary skill would have been motivated to include an internal voltage supply generating circuit in the semiconductor memory as disclosed in McAdams to ensure that the voltage on the terminal V_{cc} is constant throughout the operation of the latch.

167. As I explained above in Section IX.C.1, at the time of the alleged invention there existed a known problem in memory devices (such as McAdams) that the power supply (e.g., V_{cc}) provided to circuits in the memory device fluctuated, thereby causing malfunction of the circuit components. (See my analysis above in Section IX.C.1.) As I also explained above in Section IX.C.1, Sugibayashi provided a known solution to this known problem by disclosing an internal voltage supply generator that generated a constant voltage for the circuit components of the memory chip. (*Id.*)

168. In my opinion, based on the teachings of Sugibayashi, a person of ordinary skill in the art would have been motivated to modify the circuit of figure 1

in McAdams such that the Vcc supply voltage in McAdams is provided by an internal voltage supply generator similar to the one disclosed in Sugibayashi *in order to ensure a constant internal supply voltage and avoid malfunctions in internal component circuits of the memory*. Such a skilled person would have looked to Sugibayashi because, for example, Sugibayashi, like McAdams, relates to integrated circuit memory devices.

This invention relates to semiconductor integrated circuit devices, and more particularly to fuse circuits of the type used in VLSI CMOS semiconductor memory devices or the like.

In self-repairing semiconductor memory devices, fuses are used to store the addresses of faulty locations, so redundant cells can be substituted.

(Ex. 1006 at 1:5-12 (from Background section of McAdams).)

This invention relates to an integrated circuit device and, more particularly, to an ultra large scale integration such as, for example, a dynamic random access memory device equipped with an internal step-down circuit.

(Ex. 1011 at 1:9-13.)

Referring to FIG. 5 of the drawings, a dynamic random access memory device embodying the present invention is fabricated on a single semiconductor chip 11, and largely comprises an

internal power supply system 12 for producing a step-down power voltage V_{int} and a dynamic random access memory cell array 13a accompanied with peripheral circuits 13b such as address decoders, a precharging circuit, sense amplifier circuits, a column selector and a data buffer circuit.

(*Id.* at 4:40-48.)

169. In my opinion, having considered the teachings of Sugibayashi, a person of ordinary skill would have been motivated to combine the teachings of Sugibayashi with McAdams to implement an internal voltage supply generator (like in Sugibayashi) to generate the voltage supply V_{cc} that is provided to the internal component circuits of McAdams's memory, including the latch circuit shown in figure 1 of McAdams, e.g., for the following reasons.

170. First, in my opinion, such a modification of McAdams's memory device would have been within the capabilities of a person of ordinary skill because Sugibayashi discloses how such an internal supply voltage generator is included in a semiconductor memory device and explains how the internal supply voltage generator operates to ensure a *constant* internal voltage in spite of variations in the external voltage supply. In my opinion, a person having ordinary skill in the art would have had the capability to implement the above modification of McAdams's memory device in such a way to ensure the combination would

work for its intended purpose of providing a constant V_{cc} voltage to McAdams's figure 1 circuit.

171. Second, as I explained above, a person of ordinary skill would have recognized a benefit to making such a modification because it would have resulted in a memory device that is less likely to suffer malfunctions due to variations in the external power supply voltage.

172. In my opinion, a person of ordinary skill would have recognized that applying Sugibayashi's technique (e.g., generating a constant internal voltage from an external power supply voltage) to McAdams's memory device would have improved McAdams's device in the same way Sugibayashi's technique improves Sugibayashi's memory device (e.g., prevents malfunctioning of the circuits within the memory device), and such application was within the level of ordinary skill.

173. Including the internal supply voltage generator as disclosed by Sugibayashi with the circuit of figure 1 of McAdams would not have negatively impacted the disclosed circuit in McAdams and would have solved a known problem of circuit malfunction in memory devices like McAdams. Therefore, in my opinion the combined McAdams-Sugibayashi circuit discloses or suggests "a constant non-ground voltage throughout operation of the latch" because in the

combination, Vcc (“non-ground voltage”) is produced by an internal voltage generator that produces a constant voltage.

174. In my opinion, McAdams in combination with Sugibayashi discloses or suggests the remaining limitations of claim 14 for the reasons I discussed above for claim 14 in Section IX.B.1, with the only modification to my analysis for claim 14 being the one I discussed above. (See my analysis above in Sections IX.B.1(a)-(g).)

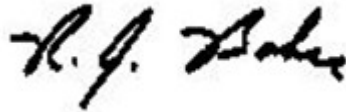
2. Claims 15-19

175. McAdams in combination with Sugibayashi discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.B.2-6. The same analysis presented above for these claims in Section IX.B is applicable for the McAdams-Sugibayashi combination discussed above in Section IX.B.1. That is, the combination of Sugibayashi with McAdams for claim 14 does not affect the analysis for claims 15-19 in Section IX.B except that the ground for these claims is modified to include Sugibayashi.

X. CONCLUSION

176. In summary, it is my opinion that all of the features recited in claims 14-19 of the '492 patent are disclosed or suggested by the prior art.

177. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: March 5, 2019

By: _____
R. Jacob Baker, Ph.D., P.E.