

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

Case IPR2019-00779
Patent No. 6,163,492

REBUTTAL DECLARATION OF R. JACOB BAKER, PH.D., P.E.

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. As I testified in my declaration signed March 5, 2019, which I understand has been labeled as Exhibit 1002 in this proceeding, I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I previously provided testimony in this proceeding in my March 5, 2019 declaration. (*See* Ex. 1002.) As with my previous work relating to this proceeding, no part of my compensation is contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding. Relevant aspects of my educational background, career history, and other qualifications were provided in my March 5, 2019 declaration. (*See id.* at ¶¶ 5-15.)

2. I have been asked to provide my opinions regarding certain positions that I understand have been asserted by Mr. de la Iglesia. My rebuttal opinions are set forth below.¹ My opinions in this rebuttal declaration are based on the documents

¹ Although I respond to selected opinions offered by Mr. de la Iglesia, doing so does not mean that I agree with any of Mr. de la Iglesia’s testimony that I do not respond to in this rebuttal declaration.

I reviewed and my knowledge and professional judgment. In forming my opinions in this rebuttal declaration, I considered the Declarations of Mr. de la Iglesia (Exs. 2001, 2003) and any other materials that I refer to in this declaration in support of my opinions. In forming these opinions, I have also drawn on my knowledge and experience in designing, developing, and researching semiconductor technology, and rely on my opinions and discussions set forth in my March 5, 2019 declaration, including my opinions regarding the level of skill of one of ordinary skill in the art. In providing my rebuttal to the positions of Mr. de la Iglesia, I do not change my opinions that I provided in my March 5, 2019 declaration.

II. CLAIM CONSTRUCTION

A. “A Terminal T1 For Providing a Signal Indicating a State of the Programmable Latch”

3. It is my understanding that ProMOS has proposed that “a terminal T1 for providing a signal indicating a state of the programmable latch” should be construed as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” (Ex. 2003 at ¶ 23.) In my opinion, a person of ordinary skill in the art would have readily appreciated the meaning of this claim term from the words themselves – the “terminal T1” limitation simply requires a terminal capable of providing a signal that indicates the state of the programmable latch. Such a person of ordinary skill in the

art would have recognized that this is the ordinary and customary meaning of this claim term.

4. In my opinion, the proposed construction adds a further limitation to the claim that is not recited in the claim. A terminal is a very simple circuit element, and nothing in the claim suggests that the voltage on the terminal T1 must be dissipated after programming. I understand that Mr. de la Iglesia asserts that the proposed construction is supported because “the embodiment without a diode must be operated such that power is turned off after programming” in order to avoid a false state on the terminal T1 due to excess voltage that may be on terminal T1. (Ex. 2003 at ¶¶ 24-25.) I disagree with Mr. de la Iglesia’s position for at least the following reasons.

5. As an initial matter, claim 1 includes the “terminal T1” limitation and also recites a diode that “keep[s] a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” (Ex. 1001 at 8:55-57.) Thus, claim 1 explicitly defines what happens to the voltage at terminal T1—it is kept within a predetermined range of values. The claimed diode, which corresponds to the diode 234 in figure 2A, also “prevent[s] the latch from assuming an incorrect state when power is supplied to the latch” (*id.* at 8:55-58), and therefore conflicts with Mr. de la Iglesia’s assertion that voltage at terminal T1 must be dissipated after programming in order to ensure proper operation of the programmable latch.

6. In fact, the '492 patent also discloses other techniques that can be used to ensure that the programmable latch will provide the correct state of the latch – even when the voltage on “terminal T1” is a “high voltage” and not at ground before power-up of the latch. Claims 20 and 21, which depend from independent claim 14 and therefore also include “a terminal T1 for providing a signal indicating a state of the programmable latch,” are directed to two additional techniques that the '492 patent indicates can help ensure the output of the latch represents the state of the fuse. Claim 20 adds features concerning selecting the trip voltage of the inverter, and claim 21 adds features concerning selecting the threshold voltage of the variable impedance path NMOS transistor 110. The '492 patent discloses that such features are associated with embodiments where the voltage on terminal OUT (terminal T1 in claim 14) is a **high value** (i.e. the voltage on the terminal has not been dissipated) immediately before power is applied to the latch:

Further, in some embodiments, **even if the voltage on the terminal OUT is at a high value** immediately before the power is turned on, the latch operates properly due to the selection of the **trip voltage of the inverter and/or the threshold voltage of transistor 110.**

(Ex. 1001 at 2:51-55, emphasis added.)

7. Claims 20 and 21 do not recite a diode, and therefore these embodiments demonstrate that Mr. de la Iglesia's assertion that in the embodiments

without the diode, the terminal T1 has to be at ground before power is applied is incorrect. Instead, by setting the inverter trip point and/or threshold voltage of transistor 110 to the appropriate values, proper operation of the latch can be ensured **even if the voltage on terminal T1 is a high value** when power is applied to the latch. (*Id.* at 6:9-17 (describing how the trip voltage of the inverter can be set to a high value (e.g. 1.6 volts) “to ensure that the trip voltage will be higher than any voltage on terminal OUT”), 6:18-28 (describing how the threshold voltage of transistor 110 is made low “so that even if the terminal OUT is slightly above the inverter trip voltage when the fuse is blown” the OUT node will still be pulled low by transistor 110).) Like the diode recited in claim 1, the embodiments described in the ’492 patent (*id.* at 2:51-55, 6:8-32) and recited in claims 20 and 21 (which do not include a diode and do not require the terminal T1 to be at ground at power-up) confirm that the ordinary meaning of the “terminal T1” would not require dissipating voltage from the terminal T1 after programming.

8. Notably, Mr. de la Iglesia asserts that “[t]he purpose of the ’492 patent is to avoid false states at the output, a condition that may occur if **excess voltage is allowed to accumulate at the output node during programming** (either due to buildup during fuse cutting, for example laser application, or from capacitive coupling at the output node).” (Ex. 2003 at ¶24 (citing Ex. 1001 at 1:46-48, 1:38-47) (emphasis added).) However, the passages to which he refers in the background

of the '492 patent do not indicate that excess voltage resulting **from programming** is the problem, and instead indicate the problem is that the “terminal OUT is floating”—a problem not solved by simply turning off the power after programming.

9. According to Mr. de la Iglesia, the terminal OUT may indicate the wrong state before power is supplied to the latch because of two situations that are mentioned in the background section of the '492 patent: (1) terminal OUT is floating and “may tend to have its potential raised to a logic level ‘1’”; and (2) the terminal OUT potential may become unstable due to capacitive coupling. (Ex. 2003 at ¶ 15.) Notably, the diode recited in claim 1, which corresponds to diode 234 in figure 2A, serves the purpose of dissipating voltage and preventing the latch from having a false state when power is applied to the latch after fuse programming. However, unlike the inclusion of a physical structure like the diode, merely turning off the power to the latch does not prevent the terminal OUT from floating or from suffering from capacitive coupling. To prevent terminal OUT from floating and suffering from capacitive coupling, a physical structure, like, for example, the diode recited in claim 1 is required.

10. A diode can ensure that the node is no longer “floating” by providing a current path through which any accumulated charge can be dissipated. Similarly, if capacitive coupling results in charge being deposited on the node, the diode provides a path for that charge to be dissipated. Turning of the power doesn't provide such a

path. Furthermore, if, for example, turning on the power to the device results in charge building on the floating node due to capacitive coupling, having previously turned off the power will not resolve any problems created by that charge that is induced on the floating node when the power is turned on. Therefore, in my opinion, turning off the power after fuse programming and prior to latch operation does not “solve” the problems mentioned in the background of the ’492 patent.

B. “A First Terminal for Receiving a Constant Non-Ground Voltage Throughout Operation of the Latch”

11. Claim 14 recites, among other things, “a first terminal for receiving a constant non-ground voltage throughout operation of the latch.” I understand that ProMOS has proposed that “throughout operation of the latch” should be construed as “at all times during circuit operation without being disabled.” (Ex. 2003 at ¶ 27.) In my opinion, the meaning of this claim term would have been apparent a person of ordinary skill in the art based on its plain language. In my opinion, the words “throughout operation of the programmable latch” have an ordinary meaning, which is “at all times when the programmable latch operates.

12. The proposed construction proffered by ProMOS introduces extraneous limitations that are ambiguous and are not apparent based on the actual claim language. For example, the proposed construction includes a “circuit,” but claim 14 does not recite a “circuit,” and it is unclear whether the “circuit” in ProMOS’s claim

construction is the same as the “latch” recited in the claim term “throughout operation of the latch.” The construction is also unclear because it requires that the non-ground voltage is provided “at all times during circuit operation *without being disabled*” (emphasis added). But a person of ordinary skill in the art would recognize that if a non-ground voltage is provided to a circuit, that voltage is necessarily enabled. If the voltage were disabled, then no voltage would be provided to the circuit and it would not be operational. As such, the “without being disabled” language is redundant in my opinion.

13. I understand that Mr. de la Iglesia refers to a particular synchronous dynamic random access memory (SDRAM) embodiment described in the following passage of the '492 patent as allegedly providing context for “throughout operation of the latch.” (Ex. 2003 at ¶ 28, citing Ex. 1001 at 4:66-5:7.)

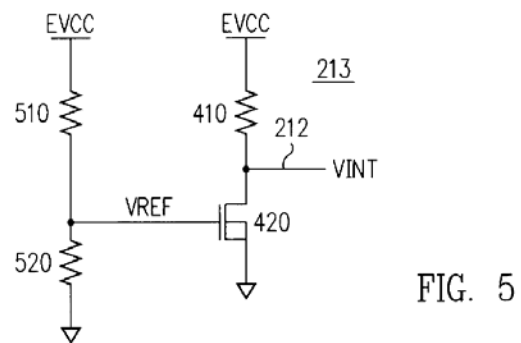
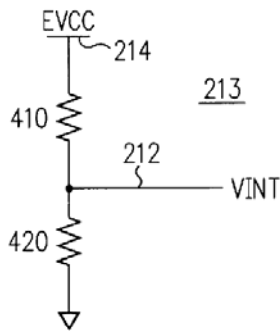
In some embodiments, the synchronous DRAM includes several generators 213. Each generator is enabled by its own signal EN. Thus, selective generators 213 can be disabled to reduce power consumption (in stand-by mode, for example). However, at least one generator 213 is enabled throughout the circuit operation in order to power circuits that are never disabled, for example, the buffer 386. Hence, the VINT voltage is a constant value **throughout the operation of the integrated circuit.**

(Ex. 1001 at 4:66-5:7 (emphasis added).)

14. I disagree with Mr. de la Iglesia's assertions that the "term 'throughout operation of the latch' appears once in the specification" and that that phrase is used in the passage cited above. (Ex. 2003 at ¶ 28.) "Throughout operation of the latch" does not appear in the passage above or anywhere else in the '492 patent outside of the claims. Instead, the passage above refers to "throughout operation of the integrated circuit." As I noted above, ProMOS's construction is ambiguous as it includes "circuit" instead of "latch," and a person of ordinary skill in the art would not equate "latch" and "integrated circuit."

15. In my opinion, ProMOS's construction is also inconsistent with the specification because it appears to require that the "non-ground voltage" recited in claim 14 must have an enable/disable feature. In other words, the construction seems to require that an enable signal can be provided that can cause the non-ground voltage to be enabled (turned on) or disabled (turned off). Indeed, one of the arguments that Mr. de la Iglesia makes regarding Fu states that "Fu does not describe circuitry where power is selectively enabled," thereby suggesting that he believes that the non-ground voltage recited in claim 14 must be a voltage that can be enabled or disabled. (Ex. 2003 at ¶35.) In my opinion, the "constant non-ground voltage" recited in claim 14 would not be required to include enable/disable functionality for a number of reasons.

16. While the SDRAM embodiment described in the cited passage above does describe enable/disable functionality associated with a VINT internal voltage, there are other embodiments of the '492 patent that do not. In particular, the figure 4 and 5 embodiments disclose VINT generators that can be used with the programmable latch circuit of figure 2A, and the figure 4 and 5 VINT generators do not include an enable/disable signal. (Ex. 1001 at 5:17-32, FIGs. 4, 5.)



(*Id.* at FIGs. 4, 5.)

17. Notably, the VINT generators in figures 4 and 5 each provide “a constant non-ground voltage throughout operation of the latch” according to ProMOS’s construction as they each provide a constant non-ground voltage “at all times during circuit operation without being disabled.” For example, figure 4 is a simple voltage divider that take the external voltage supply EVCC 214 and, using resistors 410 and 420, generates VINT 212 as a voltage that is some fraction of EVCC. But neither of the circuits shown in figures 4 and 5 contemplates enabling/disabling VINT. The external power supply voltage (EVCC) in the '492

patent is supplied by a pin (*id.* at 3:13-16), and a person of ordinary skill in the art would understand that the the EVCC voltage is supplied at all times while the integrated circuit is powered on and the latch is operational. Consistent with the embodiments shown in figures 4 and 5, if EVCC is a constant non-ground voltage, VINT will also be a constant non-ground voltage.

18. Notably, the phrase “throughout operation of the latch” is also used in claims 17 and 21, which depend from claim 14. Specifically, both claims 14 and 17 recite “the second terminal is to receive a ground voltage throughout operation of the latch.” (*Id.* at 10:35-37, 10:50-51.) Nothing in the ’492 patent suggests enable/disable functionality associated with the ground terminals included in the disclosed embodiments. As such, a person of ordinary skill in the art would not associate the phrase “throughout operation of the latch” with enable/disable functionality.

19. I have been asked to assume that ProMOS may argue that its construction of “throughout operation of the latch” also requires the latch to receive a non-ground voltage at all times when the integrated circuit (which includes the latch) is powered. In other words, that ProMOS’s construction requires the programmable latch to be always enabled (i.e., receives power) as long as the integrated circuit receives power. In my opinion, such a requirement is not supported by the passage (Ex. 1001 at 4:66-5:7) that ProMOS relies upon. While the ’492

patent states that the clock buffer 386 (shown in figure 3) in the SDRAM embodiment is one example of a circuit that is never disabled during operation of the integrated circuit, it does not suggest that the programmable latch 210 in figure 2A is never disabled. (Ex. 1001 at 5:3-5.) As described by the '492 patent, the synchronous DRAM can include several generators 213, and some of those generators can be disabled to reduce power consumption. (*Id.* at 4:66-5:2.) The only example of a circuit that is not disabled is the clock buffer 386 that receives the clock signal CKE and produces the internal clock signal ICKE. (*Id.* at 5:3-5, FIG. 3.) In the described synchronous DRAM that includes multiple internal voltage generators 213 producing multiple internal voltages VINT 212, the '492 patent does not suggest that the non-disabled VINT signal of figure 3 that is provided to the clock buffer is the same VINT signal that is provided to the programmable latch.

III. THE PRIOR ART DISCLOSES OR SUGGESTS ALL OF THE FEATURES OF CLAIMS 14-19

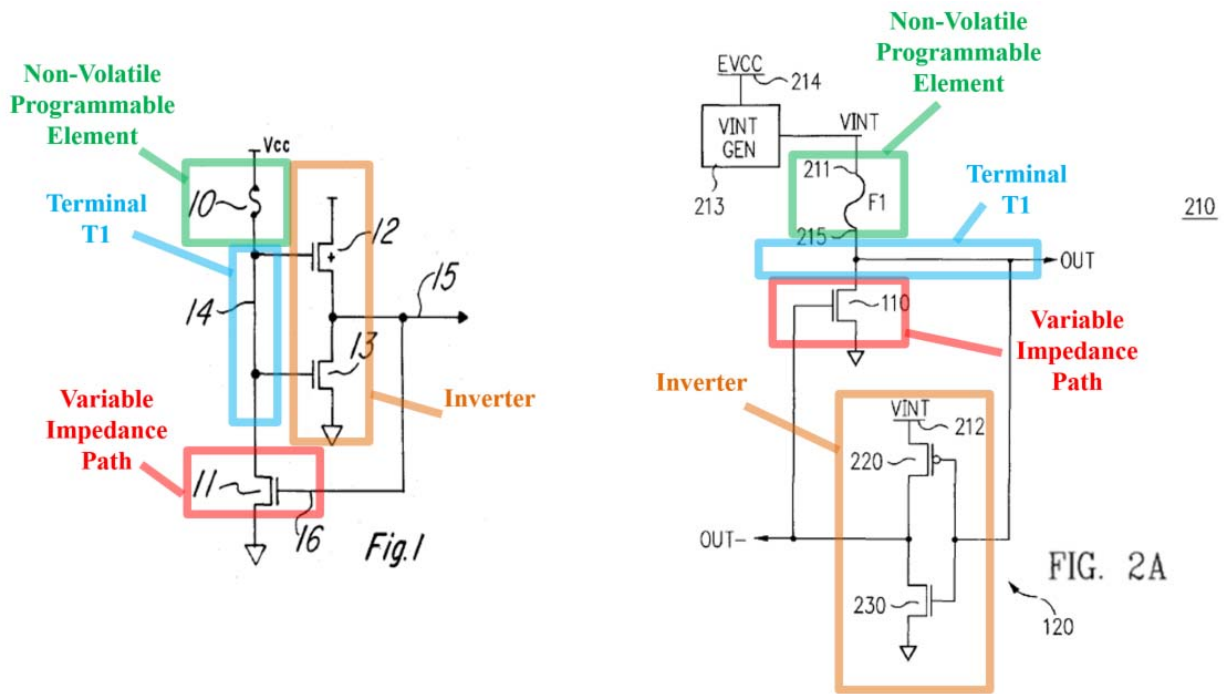
A. McAdams Discloses the Claimed “Terminal T1”

20. As I opined in my March 5, 2019 declaration, when the ordinary meaning of the term is applied, McAdams discloses “a terminal T1 for providing a signal indicating a state of the programmable latch.” (Ex. 1002 at ¶¶ 118-119.) It is also my opinion that McAdams discloses this claim feature even when ProMOS’s proposed construction is applied.

21. Mr. de la Iglesia asserts that McAdams does not disclose the operation of the latch disclosed and that “McAdams has no specific mechanism for dissipating all voltage at nodes 14 and 15.” (Ex. 2003 at ¶ 39.) Based on this, he asserts that McAdams does not teach the “terminal T1” limitation. (*Id.*) I disagree with Mr. de la Iglesia for at least the following reasons.

22. McAdams discloses a scenario in which, after fuse 10 has been blown (i.e., programmed), “Vcc is powered up.” (Ex. 1006 at 2:22-24.) A person of ordinary skill in the art would understand the “powering up” of Vcc to mean that Vcc starts at ground (0 volts), and then a voltage is applied to Vcc until it reaches the expected steady state value (e.g. 3.3 volts, 5 volts, etc.). In McAdams, as Vcc increases, the voltage at node 14 could increase due to “capacitive coupling” between node 14 and the Vcc terminal. (*Id.* at 2:26-29.) But McAdams discloses that any resulting voltage increase at node 14 due to capacitive coupling “is quickly discharged” via the drain of transistor 11 and node 14 “discharges to Vss” as a result. (*Id.* at 2:26-33.) The discharging of the voltage level at node 14 can occur, for example, as a result of leakage via the drain of transistor 11 connected with node 14. Indeed, this is the same mechanism by which terminal OUT discharges to ground voltage after fuse programming in the embodiment of the ’492 patent that does not include a diode.

23. As is apparent from the demonstrative I created below, a comparison of figure 2A of the '492 patent (modified to remove the diode) and figure 1 of McAdams shows that there is no structural difference between terminal OUT in the '492 patent and node 14 in McAdams. As can be seen in the figures below, each of McAdams and the '492 patent show a terminal T1 (node 14, terminal OUT) that is connected to one end of a fuse (fuse 10, fuse F1), the gates of two transistors that form an inverter (transistors 12 and 13, transistors 212 and 230), and the drain of an NMOS transistor that constitutes the “variable impedance path” (transistor 11, transistor 110). (Ex. 1006 at FIG. 1; Ex. 1001 at FIG. 2A.) A person of ordinary skill in the art would have understood that because these circuits have the same structure, any charge that accumulates at the terminal OUT or node 14 could be dissipated in the same way with the same “mechanism.” For at least these reasons, it is my opinion that McAdams discloses that voltage dissipates from node 14 after fuse programming as is required by ProMOS’s proposed construction of the “terminal T1” limitation.



(Ex. 1006 at FIG. 1 (left) (annotated); Ex. 1001 at FIG. 2A (right) (annotated).)

24. A person of ordinary skill in the art would have understood that there is no structural difference between the latch recited in claim 14 and the latch disclosed in McAdams. All of the circuit elements recited in claim 14 are present in McAdams. For example, McAdams discloses node 14, which is a “terminal T1” as recited in claim 14, where node 14 is connected to a “a non-volatile programmable element” (fuse 10), a “variable impedance path” (NMOS transistor 11) and an inverter formed by PMOS transistor 12 and NMOS transistor 13. Tuning power off to the latch does not constrain the structure of McAdams’ programmable latch. There is nothing special about the disclosed terminal T1 in the ’492 patent, and there is no “mechanism for dissipating voltage” attached to the terminal T1 in the relevant

embodiment of the '492 patent that is not also present in McAdams. Just like the '492 patent, charge would leak/dissipate from node 14 via the drain of the NMOS transistor connected to node 14 of McAdams.

25. I understand that ProMOS argues that McAdams does not disclose turning power off to the latch after programming the fuse. I disagree. McAdams explicitly discloses that Vcc is powered from zero to +5V both “if the fuse has not been blown” and “[if] the fuse 10 has been blown.” (Ex. 1006 at 2:8-11, 2:21-24.) In the latter scenario, McAdams discloses that the power to the latch is provided *after* the fuse 10 has been blown, thereby confirming that there is a period of time after programming of the fuse and before power is applied to the latch. (*Id.* at 2:21-24 (“If the fuse 10 has been blown, as Vcc is powered up . . .”).)

26. A person of ordinary skill in the art would have understood that this makes sense because programming of the latch by blowing fuse 10 typically occurs during testing of memory device. After testing has been completed, the device is shipped to customers for use. During shipping there is no power applied to the latch. Thus, between testing and the ultimate use of the memory device by a customer, the power to the latch is necessarily turned off in McAdams. Later, power is resupplied to the latch when the memory device is used by the customer. This understanding is supported by the '492 patent, which states that fuses are typically programmed

during testing and shipped to the customer with the power off. (Ex. 1001 at 5:57-62.)

27. I also understand that Mr. de la Iglesia asserts that McAdams suffers from the same problem that is described the '492 patent. (Ex. 2003 at ¶ 39.) Specifically, I understand that Mr. de la Iglesia contends that McAdams does not allow the voltage at nodes 14 and 15 to dissipate to ground after programming. (*Id.*) I disagree. McAdams is just like the '492 patent in that node 14 is at ground at power-up in the scenario where fuse 10 has been blown. (Ex. 1006 at 2:21-24.)

B. Fu Discloses the Claimed “Terminal T1”

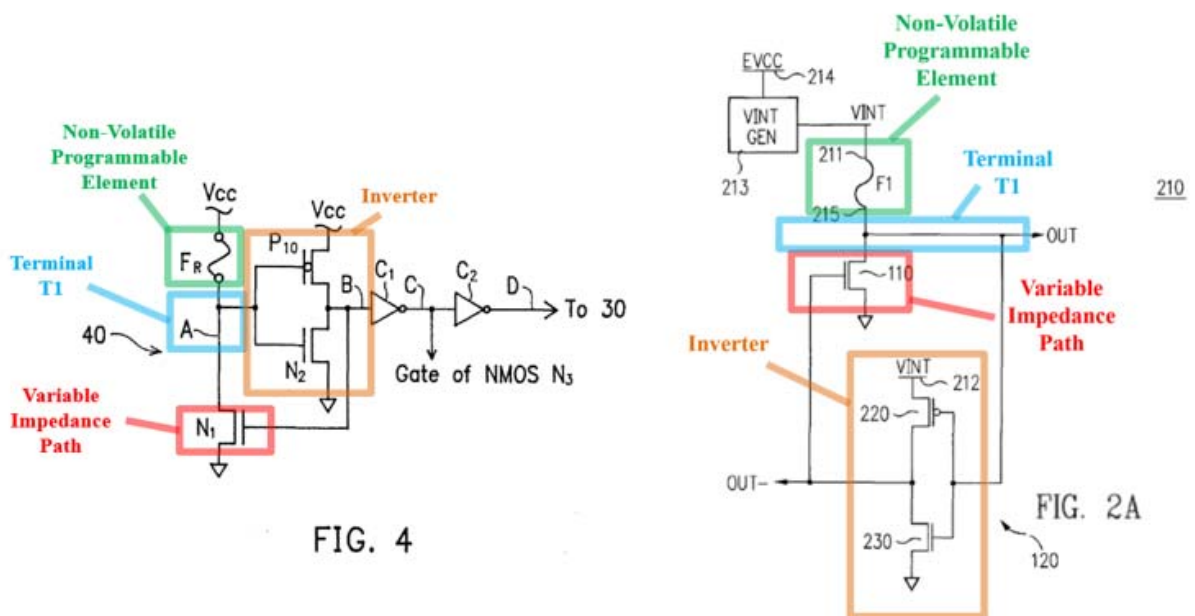
28. As I opined in my March 5, 2019 declaration, when the ordinary meaning of the term is applied, Fu discloses “a terminal T1 for providing a signal indicating a state of the programmable latch.” (Ex. 1002 at ¶¶ 79-80.) It is also my opinion that Fu discloses this claim feature even when ProMOS’s proposed construction is applied.

29. Mr. de la Iglesia asserts that Fu does not disclose the operation of the “programmable device” disclosed and that “Fu has no specific mechanism for dissipating voltage from the nodes in the latch.” (Ex. 2003 at ¶ 33.) Based on this, he asserts that Fu does not teach the “terminal T1” limitation. (*Id.*) I disagree with Mr. de la Iglesia for at least the following reasons.

30. Fu discloses that once the fuse F_R is blown (i.e., “after programming”), node A in figure 4 of Fu is at a “low electric potential.” (Ex. 1005 at 5:19-26.) A person of ordinary skill in the art would have understood that this means that any charge or voltage buildup on node A (for example, as a result of blowing the fuse) would have been dissipated for node A to be at ground after the fuse is programmed (i.e., the fuse is blown). Moreover, any accumulated charge on node A will leak away via the drain of transistor N1 in the exact same manner as the ’492 patent. In fact, after the fuse is blown in Fu during testing, power to the latch (which is part of the memory device) would be turned off just like in McAdams (*see* my discussion above in Section III.A) and the ’492 patent, and any accumulated charge or voltage would dissipate from node A.

31. As is apparent from the demonstrative I created below, a comparison of figure 2A of the ’492 patent (modified to remove the diode) and figure 4 of Fu shows that there is no structural difference between terminal OUT in the ’492 patent and node A in Fu. As can be seen in the figures below, each of Fu and the ’492 patent show a terminal T1 (node A, terminal OUT) that is connected to one end of a fuse (fuse F_R , fuse F1), the gates of two transistors that form an inverter (transistors P₁₀ and N₂, transistors 212 and 230), and the drain of an NMOS transistor that constitutes the “variable impedance path” (transistor N₁, transistor 110). (Ex. 1005 at FIG. 4; Ex. 1001 at FIG. 2A.) A person of ordinary skill in the art would have understood

that because these circuits have the same structure, any charge that accumulates at the terminal OUT or node A could be dissipated in the same way with the same “mechanism.” For at least these reasons, it is my opinion that Fu discloses that voltage dissipates from node A after fuse programming as is required by ProMOS’s proposed construction of the “terminal T1” limitation.



(Ex. 1005 at FIG. 4 (left) (annotated); Ex. 1001 at FIG. 2A (right) (annotated).)

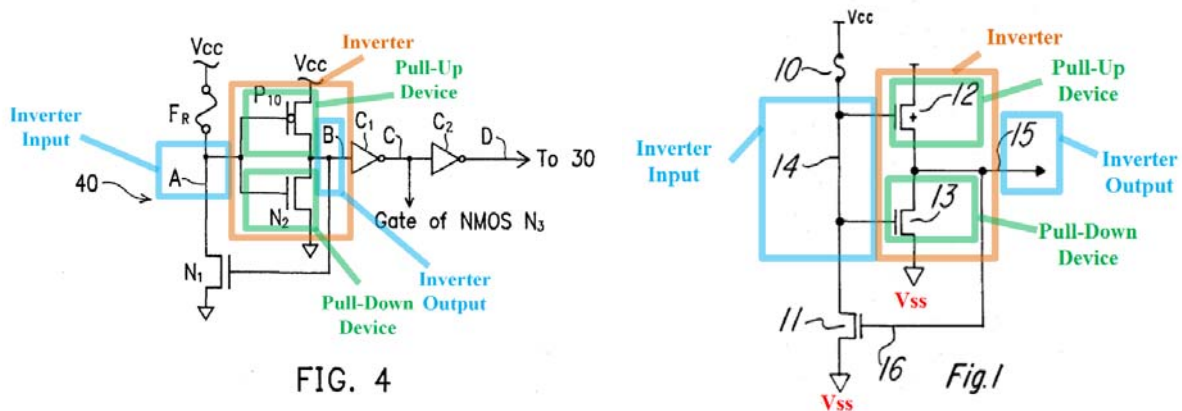
32. A person of ordinary skill in the art would have understood that there is no structural difference between the latch recited in claim 14 and the latch disclosed in Fu. All of the circuit elements recited in claim 14 are present in Fu. For example, Fu discloses node A, which is a “terminal T1” as recited in claim 14, where node A is connected to a “a non-volatile programmable element” (fuse F_R), a

“variable impedance path” (NMOS transistor N₁) and an inverter formed by PMOS transistor P₁₀ and NMOS transistor N₂. Tuning power off to the latch does not constrain the structure of Fu’s programmable latch, and there is nothing special about the disclosed terminal T1 in the ’492 patent. Moreover, there is no “mechanism for dissipating voltage” attached to the terminal T1 in the relevant embodiment of the ’492 patent that is not also present in Fu. Just like the ’492 patent, charge would leak/dissipate from node A in Fu via the drain of the NMOS transistor connected to node A of Fu.

C. McAdams and Fu Disclose the Claimed “First Terminal”

33. I understand that ProMOS asserts that each of Fu and McAdams (Fu/McAdams) does not describe **when** the voltage Vcc is provided to the latch, and therefore does not teach that Vcc is provided in Fu/McAdams “without being disabled.” Similarly, I understand that Mr. de la Iglesia contends Fu/McAdams “does not describe specific circuitry whose power is selectively enable” and “does not discuss operating in different power modes, control of the power to circuitry or describe any circuitry as being advantageously power-gated.” (Ex. 2003 at ¶¶ 35, 41.) Based on Mr. de la Iglesia’s statement that “the term ‘throughout operation of the latch’ is related to the operation of circuitry whose power is not disabled during operation,” it appears that ProMOS’s position is that McAdams and Fu do not disclose “a first terminal for receiving a constant non-ground voltage throughout

operation of the latch” because both McAdams and Fu have latches that are directly coupled to Vcc. I disagree. A person of ordinary skill in the art would understand that Vcc, which Mr. de la Iglesia refers to as the “(positive voltage) rail” (*id.*), is a constant non-ground voltage when the latch is operational. Indeed, Mr. de la Iglesia’s confirmation that Vcc is the power supply voltage on the positive power supply rail supports the understanding that a person of ordinary skill in the art would have known that a voltage is necessarily applied to Vcc for the device to be operational. Therefore, the circuits in each of Fu and McAdams are only operational when power (Vcc) is supplied to those circuits. For example, each of Fu and McAdams disclose an inverter having its input connected to the terminal T1.



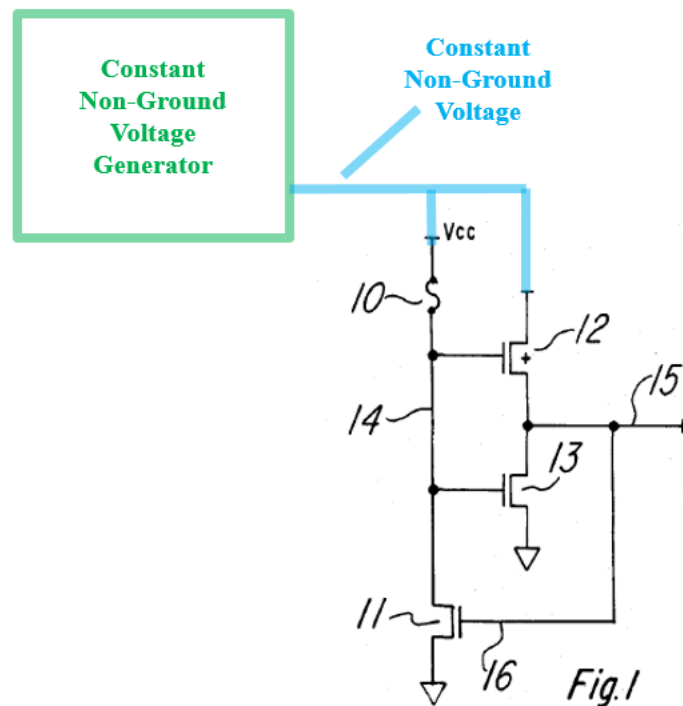
(Ex. 1005 at FIG. 4 (left) (annotated); Ex. 1006 at FIG. 1 (right) (annotated).)

34. If power is not enabled on Vcc, the inverters included in the programmable latch circuits in figure 4 of Fu and figure 1 of McAdams cannot function to produce an output that is “high,” and the latches/circuits would not be

operational. As such, for the latch circuits of Fu and McAdams to be operational, a non-zero voltage is necessarily applied (enabled) on Vcc. If Vcc is disabled, the latch circuits are not operational and the respective outputs will not reflect the state of the respective fuses in the latch circuits. Indeed, in McAdams, the latch operates (i.e., outputs a high or low voltage at output node 15) after “Vcc goes from zero to +5 v.” (Ex. 1006, 2:8-34.) For example in Fu, when the fuse is not blown, node A is at Vcc (high level) and when the fuse is blown, transistor P10 turns on, which is only possible if Vcc is at a high level. Thus, in both instances (fuse blown or intact), Fu’s circuit needs Vcc to be provided to operate. Therefore, in both of Fu and McAdams, V_{CC} is a non-zero voltage throughout operation of the latch, i.e., at all times during latch operation. Therefore, a person of ordinary skill in the art would have understood that Vcc is a non-zero voltage throughout operation of the latch in both of Fu and McAdams.

35. I have been asked to consider whether the Vcc terminal in each of Fu and McAdams is **capable of** “receiving a constant non-ground voltage at all times during circuit operation without being disabled.” A person of ordinary skill in the art would have readily understood that Vcc in each of McAdams and Fu is clearly “capable of” receiving a constant non-ground voltage throughout operation of the latch. Vcc is simply a node in the circuit and can easily be connected to, for example, a constant non-ground voltage. The Vcc terminal is just a node that can be connected

to any appropriate circuit, and a constant non-ground V_{cc} voltage can be provided to that node for as long as desired. Setting aside that the V_{cc} power supply would be understood by a person of ordinary skill in the art to be exactly such a voltage that is constant, non-ground, and supplied throughout the operation of the latch, nothing would preclude the V_{cc} nodes in each of Fu and McAdams from receiving a constant non-ground voltage. I have created the demonstratives below to demonstrate the simplicity of V_{cc} receiving such a constant non-ground voltage in each of Fu and McAdams.



(Ex. 1006 at FIG. 1 (annotated).)


119.

(Ex. 1005 at FIG. 4 (annotated).)

IV. CONCLUSION

36. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 6, 2020


R. Jacob Baker, Ph.D., P.E.