

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2019-00781
Patent 6,163,492

**PATENT OWNER PROMOS TECHNOLOGIES, INC.'S PRELIMINARY
RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

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I. INTRODUCTION

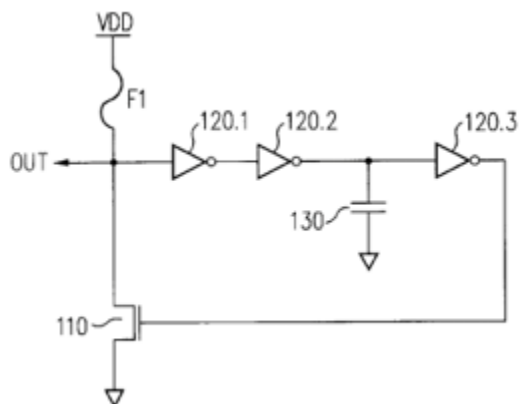
Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Patent Owner ProMOS Technologies, Inc. hereby preliminarily responds to Samsung's Petition for *Inter Partes* Review seeking cancellation of claims 1, 2, and 4-13 of U.S. Patent No. 6,163,492 (Ex. 1001, hereinafter the "'492 patent").

Samsung raises three proposed grounds for review. All of these proposed combinations rely on Joo (Ex. 1010) as the primary reference. Claim 1 of the '492 patent includes a limitation that requires "when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal." When properly construed, this term means "the programmable element is the only circuit element that controls the conductivity of the path between the terminal T1 to the first terminal." Joo's structure does not contain such a programmable path. In addition to a fuse, the path identified by Samsung in its petition includes a transistor MP1 in series with its fuse that isolates the fuse from the remainder of the circuit. Thus, Joo does not disclose the properly construed claim element, and none of the secondary references cures this fundamental deficiency. Accordingly, Samsung has not met its burden to institute *inter partes* review of the challenged claims.

II. OVERVIEW OF '492 PATENT.

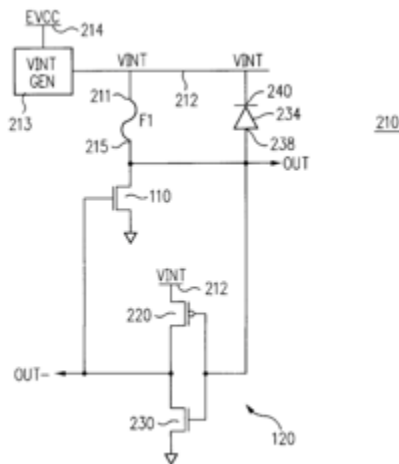
The '492 patent, titled "Programmable latches that include non-volatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



Ex. 1001 at Fig. 1.

One aspect of the invention, shown for example in figure 2A below, is that the fuse connects the power source VINT to the output node OUT, whose value is read to indicate the state of the latch.



Ex. 1001 at Fig. 2A.

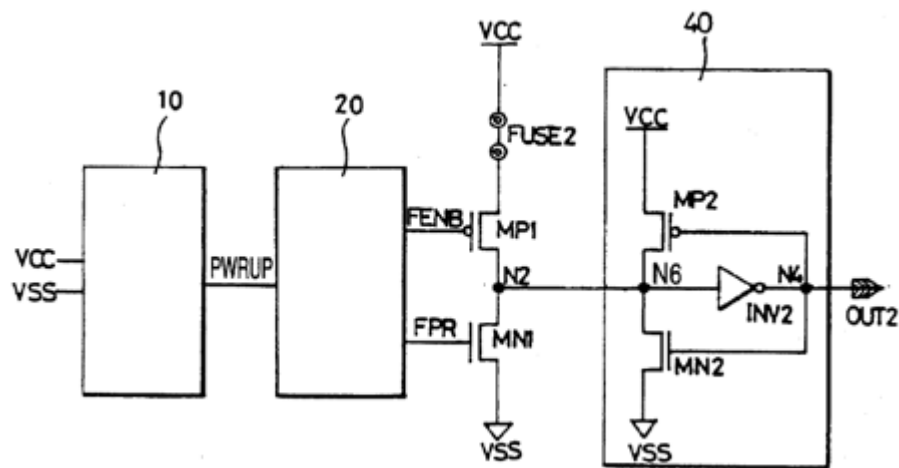
The fuse is claimed as a “non-volatile programmable element,” and each of claims 1 and 14 require that, when conductive, it connects the claimed “first terminal” (power) to the claimed “terminal T1” (terminal indicating the state of the latch). Ex. 1001 at claims 1, 14. Because of this structure, the fuse is directly indicative of the state of the latch and is the only device which affects the output. This concept was taken from the prior art embodiment in figure 1, which “has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals. This advantage is

preserved by some embodiments of the present invention.” Ex. 1001 at col. 2:22-27, 3:66-4:3.

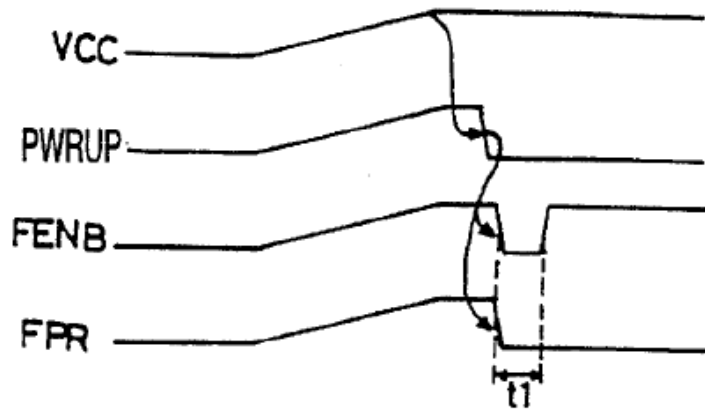
III. OVERVIEW OF PRIOR ART.

A. Joo

Joo teaches a circuit with isolation transistors MP1 and MN1 which isolate the latch from the power source during power up and when the latch is being read. The PMOS transistor MP1 is between fuse 2 and node N2 (what Samsung identifies as the terminal T1, Pet. at 17). MP1 is controlled by FENB, a latch initialization signal that is driven identically as FEN to a second series NMOS transistor MN1 during power up and initialization. Ex. 1010 at Figs. 2-3. Joo figure 2 shows these transistors schematically and figure 3 shows the associated timing.



Ex. 1010 at Fig. 2.



Ex. 1010 at Fig. 3.

Because FNEB and FEN begin at a low state, MP1 is off and the state of the fuse does not impact the circuit. By the time they have reached the full voltage level, MN1 is turned on and N2 is pulled low to VSS. This causes OUT2 to go high, resulting in a feedback loop (with MN2 and INV2) that maintains a high voltage on the output. Once both FNEB and FEN go low, at t1, MP1 is turned on and MN1 is turned off. Then, the state of the fuse impacts OUT2, and if FUSE2 is unblown then OUT2 goes low, and visa-versa. After this programming phase (after t1) FENB goes high and the fuse is electrically isolated from the latch circuit again. The state on OUT2 is maintained and read out. Ex. 1010 at col. 3:21-40.

IV. ARGUMENT.

- A. **“when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal” means “the programmable element is the only circuit element that controls the conductivity of the path between the terminal T1 to the first terminal”**

The term “when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal” should be construed to mean “the programmable element is the only circuit element that controls the conductivity of the path between the terminal T1 to the first terminal.” This means that the fuse must be the only device that either connects or disconnects the power from a node that indicates the state of the latch. Samsung has not proposed any construction for this term, instead arguing that all claim terms are to be given their ordinary and customary meaning. Pet. at 7-8.

Claim construction in this proceeding is to be under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); see 83 Fed. Reg. 51340-58 (Oct. 11, 2018).

The claim language in this limitation is clear – it requires that a programmable path exists, and that the state of the connection be controlled by the programmable element. The claim simply states that when the fuse is conductive the path is conductive, and when the fuse is not conductive the path is not

conductive. Put simply, the fuse must control conductivity of the path. Ex. 2001 at ¶¶29, 31-33.

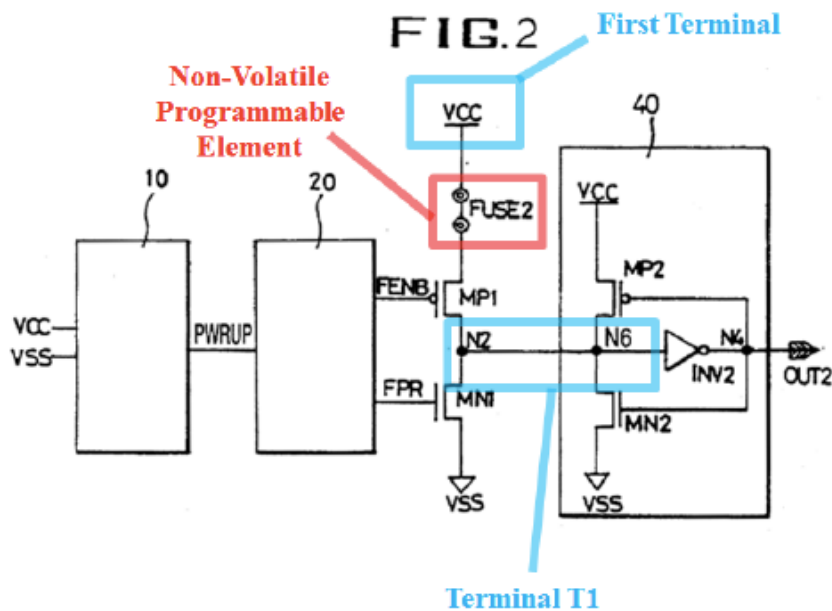
This construction is also required by the '492 specification. For example, Figure 2A shows that the programmable element is the fuse illustrated as element F1 in figure 2A, which connects the power source at one side to a node at the other that indicates the state of the latch output. Ex. 1001 at Fig. 2A. In the background of the invention, the inventors explained that prior art figure 1A “has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals. This advantage is preserved by some embodiments of the present invention. This advantageously distinguishes such embodiments of the invention from the latch described in U.S. Pat. No. 5,566,107 issued Oct. 15, 1996 to Gilliam in describing a circuit that needs an external ‘activate’ signal for initialization.” Ex. 1001 at col. 2:22-32 (emphasis added). The applicants have expressly stated that a separate latch initialization signal is undesirable, and adopted the prior art concept that the fuse is the only circuit element that controls the conductivity of the claimed path.

For at least these reasons, the '492 patent emphasized that its circuit benefited from the advantages of not having an initialization signal, and the

simplicity of indicating the latch output with only the fuse. Ex. 1001 at col. 2:22-27; Ex. 2001 at ¶33.

- B. Joo does not teach “a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal” (claims 1, 2, and 4-13)**

Samsung identifies the following as the terminal T1 and “first terminal in Joo’s circuit:



Pet. at 17.

As can be seen in this figure, Joo’s circuit has an electrical path that includes not only a fuse (FUSE2), but also includes a transistor MP1 in series with the fuse.

Ex. 1010 at Fig. 2. This structure does not meet the claim limitation because MP1

is not conductive at all times that the latch circuit is used. Ex. 1010 at col. 3:63-4:4, Fig. 3; Ex. 2001 at ¶¶36-39. The purpose of MP1 is to isolate the fuse, and thus it does not “connect[] the terminal T1 to the first terminal” “when the programmable element is conductive” as required by the proper construction of this claim term. Ex. 2001 at ¶¶34, 40.

Figure 3 of Joo shows that MP1 is conductive at the start of the waveform and during the short period during t1. Ex. 1010 at col. 3:63-4:4, Fig. 3; Ex. 2001 at ¶36. It is not conductive at the other times, when FENB is high. Ex. 1010 at Fig. 3; Ex. 2001 at ¶36. Because it isolates FUSE2, there are times that the fuse is conductive but because FENB is high terminal T1 is not connected to the “first terminal.” Ex. 2001 at ¶39. Therefore Joo does not satisfy this claim limitation or otherwise suggest that this limitation is met.

Petitioners claim that the '492 patent at 7:62-66 supports their conclusion that the '492 patent teaches providing other elements between the fuse and the node while still practicing the invention. Pet. at 17-18. But this is incorrect. First, this portion of the '492 patent (“[i]n some embodiments, other circuit elements (such as resistors, perhaps variable-impedance resistors) are included between the terminal OUT and the ground or VINT terminals.”) is talking about replacing and supplementing the transistor 110 of figure 2A, not the fuse. Ex. 1001 at col. 7:62-66. It simply means that the single transistor can be replaced by a group of series

or parallel transistors that act similar to a single transistor. Secondly, the passage describes additions between the terminals “OUT and the ground or VINT,” not rewriting the claim language which requires the fuse to connect the first terminal to terminal T1. And third, at best it can be interpreted to mean that passive circuit elements (not additional active elements like transistors) could be added.

None of the secondary references cited by Samsung – Weste, Keeth or Tomishima, cure this fundamental deficiency in Joo. Pet. at pp. 15-18, 61-69. Accordingly, Samsung has failed to meet its burden to show that claims 1, 2 and 4-13 are unpatentable, and no *inter partes* review should be instituted.

ProMOS explicitly reserves its right to argue that the cited references do not anticipate or render obvious the identified claims if the IPR is instituted.

Dated: June 14, 2019

Respectfully submitted,

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APPENDIX OF EXHIBITS

Exhibit No.	Description
2001	Declaration of Erik de la Iglesia in Support of Patent Owner ProMOS Technologies, Inc.'s Preliminary Response

CERTIFICATE OF SERVICE

I hereby certify that on June 14, 2019, a true and correct copy of the foregoing *Patent Owner Promos Technologies, Inc.'s Preliminary Response to Petition for Inter Partes Review of United States Patent No. 6,163,492* and all supporting exhibits were served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

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**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION REQUIREMENTS**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned attorney of record, hereby
certifies that:

This brief complies with the type-volume limitation of 37 C.F.R. § 42.24(b).
The brief contains 1,757 words, excluding the parts of the brief exempted by 37
C.F.R. § 42.24.

Date: June 14, 2019

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