

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES INC.
Patent Owner

Case: IPR2019-00779
U.S. Patent No. 6,163,492

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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LIST OF EXHIBITS

Exhibit No.	Description	Previously Submitted
1001	U.S. Patent No. 6,163,492	X
1002	Declaration of R. Jacob Baker, Ph.D., P.E.	X
1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.	X
1004	Prosecution History of U.S. Patent No. 6,163,492	X
1005	U.S. Patent No. 5,457,656 (“Fu”)	X
1006	U.S. Patent No. 4,621,346 (“McAdams”)	X
1007	RESERVED	
1008	RESERVED	
1009	RESERVED	
1010	RESERVED	
1011	U.S. Patent 5,373,477 (“Sugibayashi”)	X
1012	U.S. Patent No. 5,592,121 (“Jung”)	X
1013	RESERVED	
1014	RESERVED	
1015	Taur <i>et al.</i> , <u>Fundamentals of Modern VLSI Devices</u> , 2009 (“Taur”)	X
1016	RESERVED	
1017	Transcript of Deposition of Mr. Erik de la Inglesia	
1018	Rebuttal Declaration of R. Jacob Baker, Ph.D., P.E.	
1019	RESERVED	
1020	RESERVED	
1021	<i>Samsung Electronics, Co., Ltd. v. ProMOS Technologies, Inc.</i> , IPR2019-00781, Paper No. 6 (June 14, 2019)	

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) submits this Reply concerning claims 14-19 of U.S. Patent No. 6,163,492 (“the ’492 Patent”) (Ex. 1001). ProMOS Technologies, Inc.’s (“ProMOS”) arguments should be rejected and the claims found unpatentable for at least the reasons set forth in the Petition and accompanying exhibits, the Board’s decision to institute *inter partes* review (“Decision”), cross-examination testimony, and the additional reasons below. The record supports the instituted grounds, and the Board should find each of the challenged claims unpatentable and cancel them.¹

II. CLAIM CONSTRUCTION

A. “A Terminal T1 For Providing a Signal Indicating a State of the Programmable Latch”

In the Institution Decision, the Board rejected ProMOS’s attempt to limit the “terminal T1” limitation recited in claim 14 to “a terminal T1 from which voltage is

¹ ProMOS offers certain background for the ’492 patent on pages 1-7 of the Preliminary Response and pages 3-6 of the Response. Petitioner does not acquiesce to any statements in those pages. In any event, Petitioner addresses them in the appropriate sections in this paper to the extent the statements are relevant to the issues here.

dissipated after programming in order to provide a signal indicating a state of the programmable latch.” (Decision, 8-10.) While ProMOS reargues its failed construction, the Board should affirm its preliminary finding.

1. The Claims Do Not Support ProMOS’s Construction

The starting point for any claim construction analysis is the language of the claims. *See Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1375 (Fed. Cir. 2017); *Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1350 (Fed. Cir. 2019) (“We begin with the language of the claims.”). ProMOS’s analysis, however, simply ignores the language of the claims. The claim term simply requires a terminal capable of providing a signal that indicates the state of the programmable latch, which is also the ordinary and customary meaning of this claim term. (Ex. 1018, ¶¶3-4.) ProMOS’s construction thus conflicts with the claim language as it attempts to add an unclaimed limitation (“from which voltage is dissipated after programming”) to the “terminal T1” limitation.² Here, no further

² ProMOS’s proposed construction is odd given that it seeks to constrain a simple structural element of the apparatus claim—a “terminal T1”—by its manner of operation. For instance, ProMOS does not seek a construction that limits the *structure* of “terminal T1”; instead, ProMOS seeks to define the terminal by how it

construction beyond the ordinary meaning is necessary because when the “ordinary meaning of [a] claim [is] readily apparent,” like here, “claim construction will involve little more than the application of the widely accepted meaning of commonly understood words.” *Homeland Housewares, LLC*, 865 F.3d at 1375 (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-14 (Fed. Cir. 2005) (en banc)).

Moreover, other claims of the ’492 counsel against ProMOS’s construction. Claim 1 includes the same “terminal T1” limitation as in claim 14. But claim 1 additionally recites a diode that “keep[s] a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” (Ex. 1001, 8:55-57.) Thus, claim 1 explicitly defines what happens to the voltage at terminal T1—it is kept within a predetermined range of values. (Ex. 1018, ¶5.) If patentee wished to further define the voltage at terminal T1 in claim 14, which ProMOS’s construction proposes to do, the patentee would have done so like it did in claim 1. Instead, patentee recited the claimed “terminal T1” in broad terms and the patentee’s choice of words should be given its full effect. Moreover, the claimed diode, which “prevent[s] the latch from assuming an incorrect state when power is supplied to the

operates or functions (a terminal “from which voltage is dissipated after programming”).

latch” (Ex. 1001, 8:55-58) undercuts ProMOS’s argument that its construction is required to ensure that terminal T1 does not indicate an incorrect state at power-up. (Response, 9-10.)

As discussed above, the claims themselves demonstrate the fallacy in ProMOS’s construction. The “terminal T1” limitation should thus be given its ordinary and customary meaning unless ProMOS can demonstrate that patentee narrowed the claim through definition or disclaimer. *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) (citing *Phillips*, 415 F.3d at 1316); *InterDigital Commc’ns, LLC v. Int’l Trade Comm’n*, 690 F.3d 1318, 1324 (Fed. Cir. 2012). But, as explained below, ProMOS can point to no such definition or disavowal in the specification or the prosecution history that can compel its construction.

2. The Specification Does Not Support ProMOS’s Construction

ProMOS does not contend that the specification defines or disavows the full scope of the “terminal T1” limitation. (Response, 7-11.) By itself, that renders irrelevant all of ProMOS’s arguments regarding what the specification allegedly shows. *Thorner*, 669 F.3d at 1365. In any event and as explained below, ProMOS’s arguments are without merit.

ProMOS first urges that its construction is supported by the ’492 patent because in an exemplary embodiment (specifically, the one without the diode),

terminal OUT is “at ground before power-up” and, per ProMOS, such grounding of the terminal OUT before power-up is necessary to achieve a correct state of the programmable latch. (Response, 9-11.) According to ProMOS, in this embodiment, the power is turned off after programming of the fuse and “any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated.” (*Id.*, citing Ex. 1001, 5:51-6:8.) None of this, however, is sufficient to limit the claim beyond its ordinary meaning.

As the Board correctly recognized, ProMOS is asking “to import into the claim a requirement that terminal T1 be at ground voltage where one does not currently exist” and while an embodiment may have the terminal OUT at ground at power-up, “it is important not to import into a claim limitations that are not part of the claim.” (Decision, 10.) Here, the statements to which ProMOS points merely reflect the operation of an exemplary embodiment and in no way serve to define the claimed “terminal” as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” In fact, the ’492 patent recognizes that terminal OUT need not be at ground at power-up for the latch to indicate the correct state at power-up. (Ex. 1001, 2:51-55; Ex. 1018, ¶¶6-7.) Indeed, the ’492 patent explains and also *claims* techniques (e.g., increasing the trip point of the inverter connected to terminal OUT and/or decreasing the threshold voltage of the variable-impedance path connected to

terminal OUT) that ensure proper latch operation without the need for ensuring that terminal OUT is at ground before power-up. (Ex. 1018, ¶¶6-7 (citing Ex. 1001, 6:8-32, claims 20 and 21).)

ProMOS's appeal to the purpose of the invention also fails. (Response, 9-10.) As explained above, the '492 patent itself recognizes that dissipation of voltage from terminal T1 is not necessary for proper latch operation because it states that the latch can indicate the correct state even if the terminal T1 is not at ground at power-up. ProMOS's argument is thus meritless for this and other reasons discussed below.

First, it is black-letter law that a claim will not be limited beyond its ordinary meaning in order to ensure that it serves "a perceived 'purpose' of the invention." *Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1345 (Fed. Cir. 2008).

Second, if the purpose of the invention, as ProMOS says, is to prevent the latch from assuming an incorrect state at power-up, claim 1 of the '492 patent demonstrates that patentee knew how to recite features that accomplish such a purpose. For instance, claim 1 explicitly recites a diode that "prevent[s] the latch from assuming an incorrect state when power is supplied to the latch." (Ex. 1001, 8:55-58.) As acknowledged by ProMOS's declarant, the claimed diode refers to diode 234 in figure 2A of the '492 patent and diode 234 serves the purpose of dissipating voltage and preventing the latch from having a false state when power is

applied to the latch after fuse programming. (Ex. 1017, 47:11-48:12; Ex. 1018, ¶9; Ex. 1001, FIG. 2A, 3:33-49; *see also* Response, 5-6 (explaining that the diode solves the problems identified in the background of the '492 patent).) But patentee included no such features in claim 14, thereby leaving it broad.

Third, ProMOS's proposed construction should be rejected because, even though claim 1 is an *apparatus* claim, ProMOS omits from its construction any *structural* aspects that presumably solve the problems ProMOS alleges are addressed by the '492 patent. Per ProMOS, by simply turning off the power to the latch after blowing the fuse, the '492 patent solves the false state problem. (Response, 9-10.) But turning power off after programming is not included in ProMOS's construction. Nor does ProMOS explain how turning off the latch's power places any structural limitation on the claimed "terminal T1." In contrast to the diode limitation, which further defines the latch's structure, turning power off to the latch is a manner of operating the latch that adds no further structural limitation to the claimed "terminal T1."

Fourth, ProMOS's argument that turning off the power to the latch after fuse programming would solve the problems identified in the background of the '492 patent is technically incorrect. (Ex. 1018, ¶¶8-10.) ProMOS explains that the false state problem occurs in the prior art because terminal OUT is "floating" when power is off or become unstable due to capacitive coupling during power up. (Response,

5-6, 9.) Per ProMOS, turning power off to the latch after programming resolves these issues. (*Id.*) But merely turning off the power to the latch does not prevent the terminal OUT from floating or from suffering from capacitive coupling. (Ex. 1018, ¶¶8-10.) To prevent terminal OUT from floating and suffering from capacitive coupling, a physical structure (e.g., a diode) is required. (*Id.*, ¶¶9-10.) Simply put, contrary to ProMOS’s assertions, turning off the power after fuse programming and prior to latch operation does not “solve” the problems posited in the background of the ’492 patent.³

ProMOS’s argument that the specification compels its construction thus fails for the above reasons.

3. ProMOS’s Assertion That Claim 1 Includes Two Solutions Is Unsupported

In rejecting ProMOS’s construction, the Board noted that claim 1, like claim 14, recites “a terminal T1 for providing a signal indicating a state of the

³ ProMOS’s allegations regarding the background of the ’492 patent, Response, 9 (citing Ex. 1001, 1:46-48, 1:38-47), are incorrect because the background does not indicate that excess voltage resulting **from programming** is the problem, and instead indicates the problem is that the “terminal OUT is floating”—a problem not solved by simply turning off the power after programming. (Ex. 1018, ¶8.)

programmable latch.” (Decision, 8-9.) ProMOS criticizes the Board for assuming “that ProMOS was arguing for [] different constructions for the relevant term in the two different claims.” (Response, 8.) But ProMOS did not argue for the same construction for claim 1 in its preliminary response in IPR2019-00780 and IPR2019-00781, thereby suggesting to the Board that construction of the term was not appropriate for claim 1 and the ordinary meaning of the term should apply.⁴

In response, ProMOS states that it is not asking for different constructions and alleges that “[c]laim 1 addresses the stated ‘false state’ problem with two solutions – a diode and ‘a terminal T1 from which voltage is dissipated after programming’” (Response, 8.) ProMOS’s argument fails for at least two reasons. First, ProMOS provides no explanation why claim 1 recites two solutions when both solutions standing alone resolve the “false state” problem. Second, if ProMOS’s argument were true that claim 1 recites “two” distinct solutions to the “false state” problem, then claim 1 would be invalid for lack of written description support. This is because there is no embodiment in the ’492 specification having both solutions. Specifically, the only support for the first solution (turning off power to the latch) is an

⁴ Notably, ProMOS attempts to remedy its inconsistency and construes the “terminal T1” term in its responses in IPR2019-000780 and IPR2019-000781.

embodiment in which the diode is omitted. (Decision, 8 (“Patent Owner’s proposed construction, however, is limited to a described embodiment of the programmable latch that does not have a diode . . .”).) ProMOS’s arguments thus fail for this additional reason.

B. “A First Terminal for Receiving a Constant Non-Ground Voltage Throughout Operation of the Latch”

Claim 14 recites, *inter alia*, “a first terminal for receiving a constant non-ground voltage throughout operation of the latch.” ProMOS contends that “throughout operation of the latch” should be construed as “at all times during circuit operation without being disabled.” (Response, 11-12.) This construction should be rejected because it is untethered to the plain language of the claim, has no basis in the intrinsic record, and introduces ambiguous extraneous limitations that ProMOS’s own declarant is unable to explain.

1. The Claim Does Not Support ProMOS’s construction

The “first terminal” limitation is clear and unambiguous in that it simply requires a first terminal that is capable of receiving a constant non-ground voltage throughout operation of the programmable latch. The words “throughout operation of the programmable latch” have an ordinary meaning, which is “at all times when the programmable latch operates.” (Ex. 1018, ¶11.) This is not a limitation for which further construction is required because the ordinary meaning is readily apparent. *Homeland Housewares, LLC*, 865 F.3d at 1375 (citing *Phillips v. AWH*

Corp., 415 F.3d 1303, 1312-14 (Fed. Cir. 2005) (en banc)). Recognizing that the prior art clearly discloses the “first terminal” limitation under the plain meaning, ProMOS proposes a construction that introduces extraneous limitations, which are ambiguous and inconsistent with the claim language. For instance, the proposed construction introduces a new term “circuit” without clarifying whether circuit refers to the claimed “latch” or something else. Indeed, ProMOS’s declarant was unable to give a clear answer to the simple question as to whether the term “circuit” in the proposed construction is the same as the “latch” recited in the claim. (Ex. 1017, 153:6-154:21.)

Furthermore, ProMOS’s construction introduces redundant language by requiring that the non-ground voltage is provided “at all times during circuit operation *without being disabled*” (emphasis added). As a POSITA would recognize, if a non-ground voltage is provided to a circuit, the voltage is necessarily enabled because if the voltage is disabled, no voltage would be provided to the circuit. (Ex. 1018, ¶12.)

2. ProMOS’s Declarant Cannot Explain the Meaning of ProMOS’s Proposed Construction

Under cross-examination, ProMOS’s declarant Mr. de la Iglesia was unable to provide any cogent explanation of the meaning of “throughout operation of the latch” as recited in claim 14 under ProMOS’s construction. Instead, he repeatedly referred to a portion of the ’492 specification as allegedly providing the only

explanation of what that claim language means under ProMOS’s construction. (Ex. 1017, 61:16-62:8, 64:18-67:10, 75:4-13, 88:1-10, 132:5-133:20.) Even when pressed to explain the requirements of the construction, he could not articulate whether the construction requires multiple voltage generators (*id.*, 64:18-67:10) or whether enable/disable functionality is required (*id.*, 157:18-159:12). The ambiguity in ProMOS’s proposed construction is evident from Mr. de la Iglesia’s inability to map claim 14 to figure 2A of the ’492 patent (*Id.*, 69:2-23, 70:8-15, 132:14-20)⁵ or even indicate whether or not the VINT node in figure 2A is *capable* of receiving a “constant non-ground voltage throughout operation of the latch.” (*Id.*, 126:11-127:15, 129:6-20, 130:11-131:8.) Indeed, when asked to identify a figure in

⁵ In its Preliminary Response in IPR2019-00781, when it wanted to narrow the scope of the claims based on specific embodiments disclosed in the specification, ProMOS readily relied upon a mapping of the claims to figure 2A of the ’492 patent. (Ex. 1021, 7. In contrast, Mr. de la Iglesia repeatedly stated that he thought mapping claim 14 to any of the figures in the ’492 patent amounted to providing an “infringement opinion,” and that such a mapping would require an understanding of the structure of the entire device that included the latch shown in figure 2A. (Ex. 1017, 67:12-70:15, 71:3-14, 73:15-75:13, 78:19-24, 85:2-12.)

the '492 patent that discloses “a first terminal for receiving a constant non-ground voltage throughout operation of the latch,” Mr. de la Iglesia was unable to do so. (*Id.*, 70:21-71:14, 72:2-73:13.) According to Mr. de la Iglesia, even the external power supply EVCC provided in the '492 patent cannot be described as a “constant non-ground voltage during operation of the integrated circuit” because the '492 patent does not provide enough description of EVCC to make that determination. (*Id.*, 108:1-20.)

3. The Specification Does Not Support ProMOS's Construction

The specification also does not support ProMOS's construction. ProMOS does not allege that the specification compels the proposed construction by virtue of a definition or disclaimer. (Response, 11-12.) ProMOS's arguments are thus irrelevant. *Thorner*, 669 F.3d. at 1365 (holding that deviating from the ordinary and customary meaning requires definition or disclaimer). In any event, ProMOS's assertions are unsupported.

ProMOS alleges that “throughout operation of the latch” is only used once in the specification. (Response, 11 (citing Ex. 1001, 4:66-5:7).) But the cited portion refers to a VINT voltage that is constant “throughout operation of the **integrated circuit**,” not “throughout operation of the **latch**.” “Throughout operation of the latch” is never used in the specification outside of the claims.

ProMOS's construction is further inconsistent with the specification because

it appears to allege that the “non-ground voltage” must be provided by a circuit have an *enable/disable* feature.⁶ (Ex. 1018, ¶¶12-19.) To support its construction, ProMOS asserts that the specification “explains that the VINT voltage is supplied without being disabled, for use by circuits that are always operational.” (Response, 11.) While at least one embodiment has an enable/disable functionality associated with the VINT voltage, other embodiments of the ’92 patent do not. (Ex. 1018, ¶16; Ex. 1001, 5:17-32, FIGs. 4, 5.)

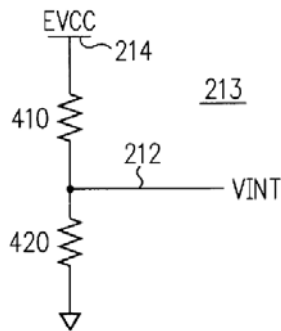


FIG. 4

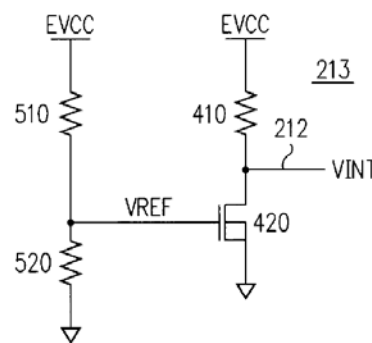


FIG. 5

(Ex. 1001, FIGs. 4, 5.) Notably, the generators in figures 4 and 5 each provide “a constant non-ground voltage throughout operation of the latch” as required by the claim. (Ex. 1018, ¶17.) But neither circuit contemplates enabling/disabling VINT. Thus, ProMOS’s construction must be rejected because it would exclude other

⁶ While not confirmed by ProMOS’s declarant during cross-examination (Ex. 1017, 157:18-159:6), ProMOS’s prior art arguments suggest this. (*See also* Ex. 2003, ¶35 (“Fu does not describe circuitry where power is selectively enabled.”).)

disclosed embodiments. *See Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1320 (Fed. Cir. 2005).

While unclear from ProMOS's construction, ProMOS may argue that its construction also requires the programmable latch to receive non-ground voltage at all times when the integrated circuit (which includes the latch) is powered. Again, such a requirement is unsupported by the '492 patent specification. (Ex. 1018, ¶19.) While the '492 patent states that the buffer 386 is one example of a circuit that is never disabled during operation of the integrated circuit, it does not suggest that the programmable latch 210 is never disabled. (Ex. 1001, 5:3-5.)

III. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF CLAIMS 14-19

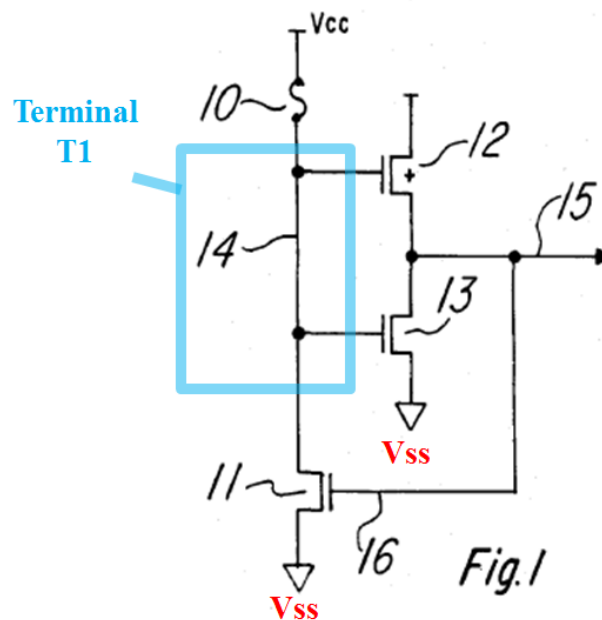
A. McAdams and Fu Disclose 'A Terminal T1 For Providing A Signal Indicating A State Of The Programmable Latch'

Applying the ordinary meaning, McAdams and Fu anticipate claim 14. But even if ProMOS's faulty constructions were adopted, McAdams and Fu disclose the disputed claim features as explained in detail below.

1. McAdams and Fu Disclose the Claimed "Terminal T1" Under the Term's Ordinary and Customary Meaning

Claim 14 recites, *inter alia*, "a terminal T1 for providing a signal indicating a state of the programmable latch." Figure 1 of McAdams discloses a programmable latch and node 14 in that latch corresponds to the claimed "terminal T1." (Petition, 54-56; Ex. 1002, ¶¶118-119.) If the fuse is intact, node 14 is at Vcc (high), but if

the fuse is blown, node 14 is at Vss (low). (Ex. 1006, 2:8-24.) Therefore, the voltage at node 14 provides a signal indicating a “state of the programmable latch” because the voltage at node 14 indicates whether the fuse is blown or not. (Petition, 54-55; Ex. 1002, ¶118.) Thus, McAdams discloses the limitation under its ordinary and customary meaning.



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶118.)

Similarly, figure 4 of Fu discloses a programmable latch and node A in that circuit corresponds to the claimed “terminal T1.” (Petition, 26-28; Ex. 1002, ¶¶79-80.) During operation of the latch, if the fuse is intact, node A is at Vcc (high), but if the fuse is blown, node A is at GND (low). (Ex. 1005, 4:67-5:29.) Therefore, the voltage at node A provides a signal indicating a “state of the programmable latch” because the voltage at node A indicates whether the fuse is blown or not. (Petition,

26-27; Ex. 1002, ¶79.) Thus, Fu discloses the limitation under its ordinary and customary meaning.

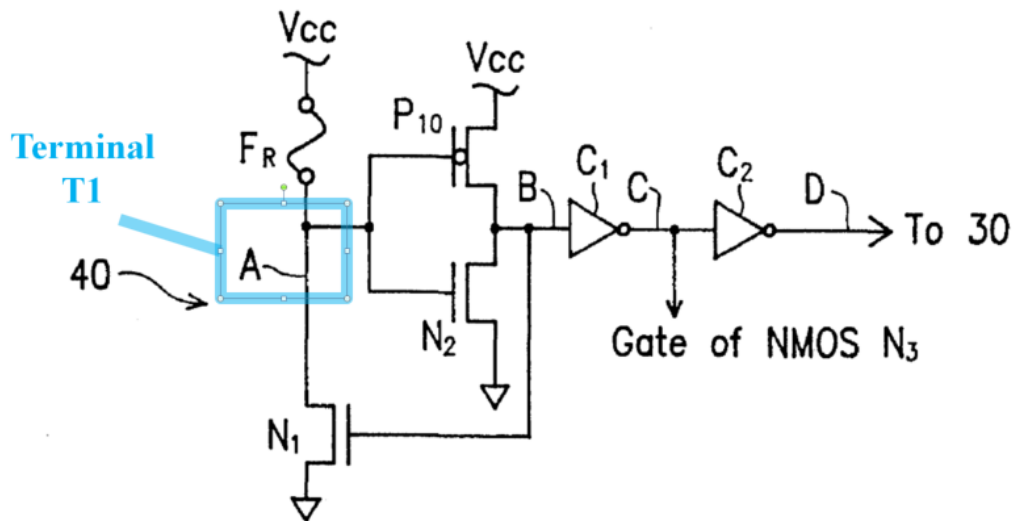


FIG. 4

(Ex. 1005, FIG. 4 (annotated); Ex. 1002, ¶79.)

Moreover, as discussed below, both McAdams and Fu disclose the claimed “terminal T1” even under ProMOS’s construction.

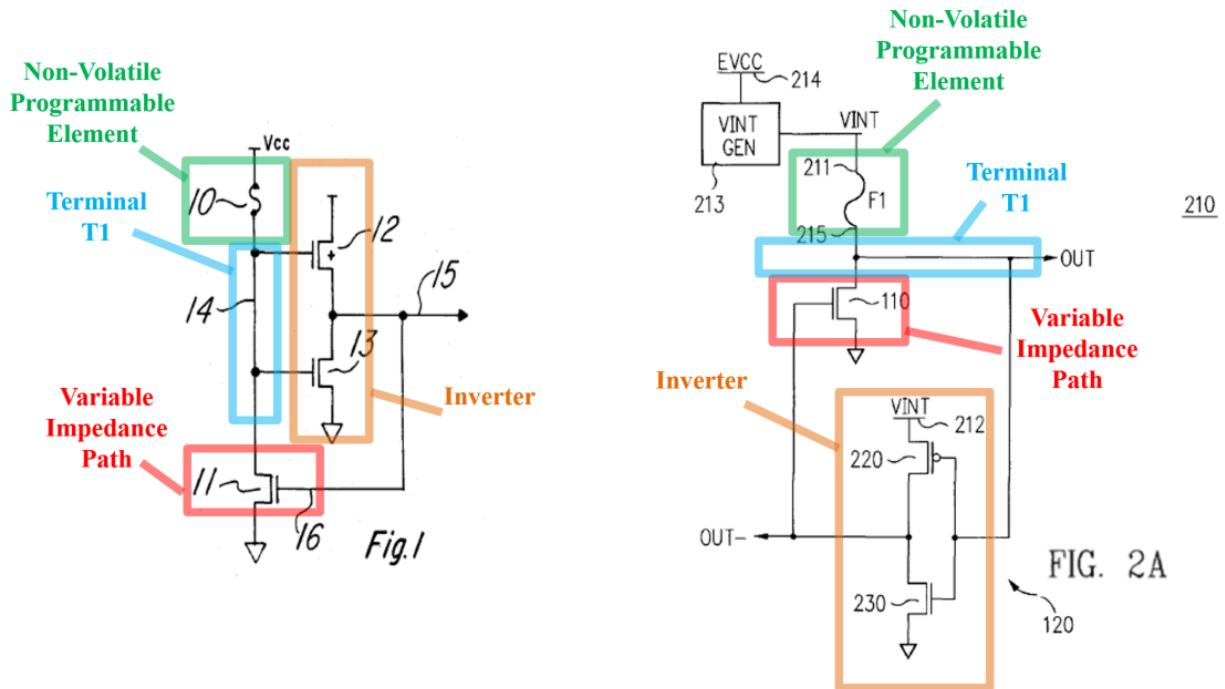
2. McAdams Discloses the Claimed “Terminal T1” Under ProMOS’s Construction

ProMOS’s construction requires “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” As discussed above, node 14 in figure 1 of McAdams corresponds to the claimed “terminal T1.” ProMOS does not contest that node 14 provides a signal indicating a state of the programmable latch. (Response, 18-19.)

Instead, ProMOS contends that “voltage [is not] dissipated after programming” from node 14, as required by ProMOS’s construction. (*Id.*, 18 (“McAdams does not state that voltage that accumulates on nodes 14 and 15 is dissipated after programming.”).) Contrary to ProMOS’s argument, McAdams explicitly discloses voltage dissipation from node 14 after fuse programming. (Ex. 1018, ¶¶20-27.)

In particular, McAdams discloses a scenario in which, after fuse 10 has been blown (i.e., programmed), “Vcc is powered up.” (Ex. 1006, 2:22-24; Ex. 1018, ¶22.) As Vcc increases, the voltage at node 14 could increase due to “capacitive coupling” between node 14 and the Vcc terminal. (Ex. 1006, 2:26-29; Ex. 1018, ¶22.) But McAdams discloses that any resulting voltage increase at node 14 due to capacitive coupling “is quickly discharged” via the drain of transistor 11 and node 14 “discharges to Vss” as a result. (Ex. 1006, 2:26-33; Ex. 1018, ¶22.) As explained by Dr. Baker, leakage via the drain of transistor 11 connected with node 14 is the same mechanism by which terminal OUT discharges to ground voltage after fuse programming in the embodiment of the ’492 patent that does not include a diode. (Ex. 1018, ¶22.) Indeed, as apparent from the demonstrative below, a comparison of figure 2A of the ’492 patent (modified to remove the diode) and figure 1 of McAdams shows that there is no structural difference between terminal OUT in the ’492 patent and node 14 in McAdams. (Ex. 1018, ¶¶23-24.) Thus, McAdams discloses that voltage dissipates from node 14 after fuse programming, as required

by ProMOS's construction.



(Ex. 1006, FIG. 1 (left) (annotated); Ex. 1001, FIG. 2A (right) (annotated); Ex. 1018, ¶23.)

ProMOS's other arguments, for example, that McAdams is "silent about" *turning power off after programming* (Response, 19) are simply irrelevant because they are not tied to the plain language of ProMOS's proposed construction, which merely requires voltage dissipation from terminal T1 after fuse programming. In any event, these arguments lack merit.

First, ProMOS's assertion that McAdams fails to disclose turning power off to the latch after programming the fuse is demonstrably false. McAdams explicitly discloses that Vcc is powered from zero to +5V under both conditions: "if the fuse has not been blown" and "[if] the fuse 10 has been blown." (Ex. 1006, 2:8-11, 2:21-

24; Ex. 1018, ¶25.) With respect to the second scenario, McAdams discloses that the power to the latch is provided *after* the fuse 10 has been blown, thereby confirming that there is a period of time after programming of the fuse and before power is applied to the latch. (Ex. 1006, 2:21-24 (“If the fuse 10 has been blown, as Vcc is powered up”); Ex. 1018, ¶25.) This makes sense because programming of the latch by blowing fuse 10 typically occurs during testing of memory device following which the device is shipped to customers for use. (Ex. 1018, ¶26.) Of course, during shipping no power is applied to the latch. (*Id.*) Thus, between the testing and ultimate use of the memory device by the customer, the power to the latch is necessarily turned off in McAdams and power is resupplied to the latch when the memory device is used by the customer. (*Id.*; *see also* Ex. 1001, 5:57-62.)

Second, ProMOS’s assertion that McAdams suffers from the same problem that the ’492 patent addresses is again false. (Ex. 2003, ¶39.) ProMOS contends that the ’492 patent solves the “false state” problem by ensuring that terminal OUT is at ground before power-up. (Response, 9-10; *see also* Decision, 10 (recognizing that ProMOS relies on the embodiment in which terminal OUT is at ground at power-up).) But McAdams is just like the ’492 patent in that node 14 is at ground at power-up in the scenario where fuse 10 has been blown. (Ex. 1006, 2:21-24; Ex. 1018, ¶27.)

Third, and most importantly, each of ProMOS’s arguments fails because

ProMOS cannot show that there is any *structural* difference between the elements recited in claim 14 and those shown in figure 1 of McAdams. It is well-settled that an apparatus claim, like claim 14, can only be distinguished over the prior art based on its structure. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990) (“Apparatus claims cover what a device is, not what a device does.”); *ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018). None of ProMOS’s arguments attempt to distinguish claim 14 from figure 1 of McAdams based on any claimed structural features.

For instance, ProMOS’s argument that the power is not turned off to the latch after programming or that voltage is not dissipated from node 14 after programming relate to the *manner of operating the latch*; they do not constrain the structure of the latch. (Ex. 1018, ¶24.) Indeed, McAdams discloses all structural aspects of the disputed claim limitation — “terminal T1” (e.g., node 14 is a terminal and it is connected to “a non-volatile programmable element,” a “variable impedance path,” and an inverter). (Ex. 1017, 135:14-20, 136:9-137:5.) There is nothing special about the disclosed terminal T1 in the ’492 patent, and there is no “mechanism for dissipating voltage” attached to the terminal T1 in the relevant embodiment of the ’492 patent that is not also present in McAdams. (Ex. 1017, 96:16-97:3; Ex. 1018, ¶24.) As discussed above, just like the ’492 patent, charge would leak/dissipate from node 14 via the drain of the NMOS transistor connected to node 14.

For all of the above reasons, McAdams discloses the claimed “terminal T1” even under ProMOS’s erroneous construction.

3. Fu Discloses the Claimed “Terminal T1” Under ProMOS’s Construction

As discussed above, node A in figure 4 of Fu corresponds to the claimed “terminal T1.”

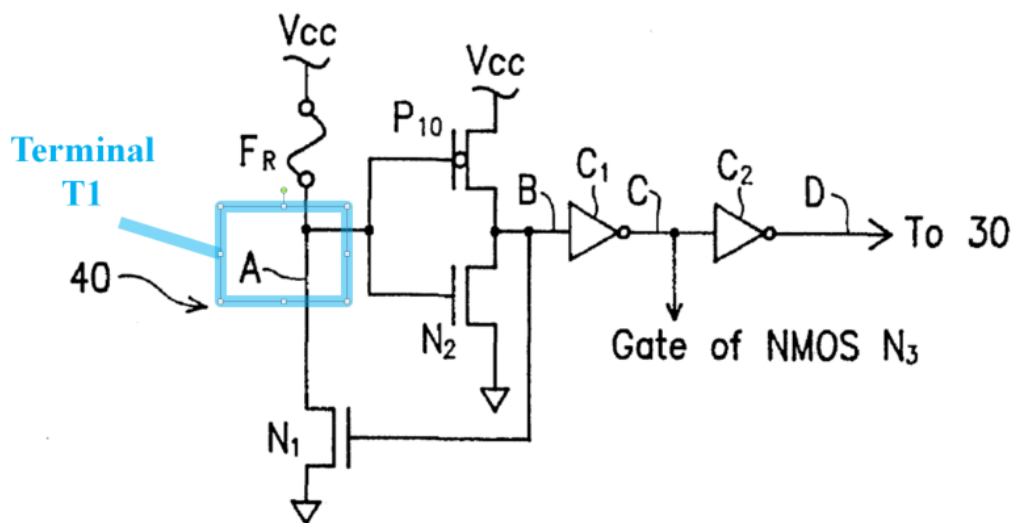


FIG. 4

(Ex. 1005, FIG. 4 (annotated); Ex. 1002, ¶¶79.)

As was the case with McAdams, contends that Fu does not disclose dissipation of voltage from node A after fuse programming. (Response, 17.) ProMOS’s argument lacks merit for several reasons. (Ex. 1018, ¶¶28-32.)

First, Fu discloses that once the fuse F_R is blown (i.e., “after programming”), node A in figure 4 of Fu is at a “low electric potential” and any charge or voltage

buildup on node A would have been dissipated (Ex. 1005, 5:19-26; Ex. 1018, ¶30.) Charge on node A will leak away via the drain of transistor N1 in the exact same manner as the '492 patent. (Ex. 1018, ¶30.) Like McAdams, power to the latch would be turned off after programming, and any accumulated charge or voltage would dissipate from node A. (*Id.*)

Second, ProMOS cannot show that there is any *structural* difference between “terminal T1” in claim 14 and those shown in figure 4 of Fu. ProMOS’s argument that voltage is not dissipated from node A in Fu after programming relates to the *manner of operating the latch*; it does not constrain the structure of the latch. (Ex. 1018, ¶32.) Indeed, Fu discloses all structural aspects of the disputed claim limitation. (Ex. 1018, ¶32; Ex. 1017, 188:6-20.)

B. McAdams and Fu Disclose the Claimed “First Terminal”

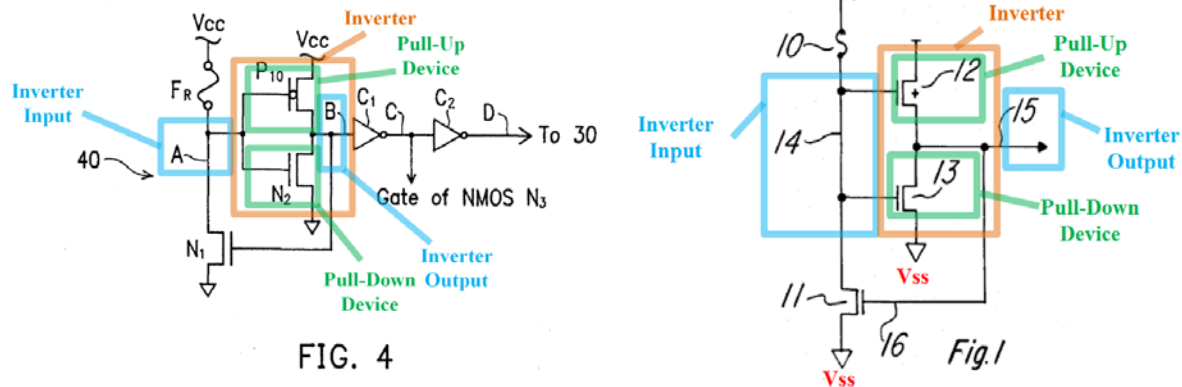
There is no dispute that the VCC terminals in figure 4 of Fu and figure 1 of McAdams constitute a “first terminal for receiving a constant non-ground voltage.” (Petition, 22-24, 49-52; Response, 18-19.) The dispute centers around ProMOS’s assertion that the Vcc terminals in McAdams and Fu do not receive Vcc “throughout operation of the latch” under ProMOS’s construction. (Response, 18-19.) Specifically, ProMOS contends the references do not disclose “when Vcc is provided to the latch” and that “Vcc is provided without being disabled,” as required by ProMOS’s construction. (Response, 18-19.) ProMOS is wrong.

Because “for receiving a constant non-ground voltage throughout operation of the latch” is a functional limitation, it cannot distinguish claim 14 from the prior art as the claimed structure (i.e., the “first terminal”) is capable of performing such a function. *Hewlett-Packard Co.*, 909 F.2d at 1468; *ParkerVision, Inc.*, 903 F.3d at 1361. As explained by Dr. Baker, the Vcc terminal a node that can be connected to any appropriate circuit, and a constant non-ground Vcc voltage can be provided to that node for as long as desired; thus, the Vcc terminal in each of Fu and McAdams is capable of “receiving a constant non-ground voltage at all times during circuit operation without being disabled” according to ProMOS’s proposed construction. (Ex. 1018, ¶¶33-35.)⁷

Furthermore, both Fu and McAdams disclose that Vcc is provided to the Vcc terminal at all times during the latch’s operation. The circuits in each of Fu and McAdams are only operational when power (Vcc) is supplied to those circuits. (Ex. 1018, ¶¶33-34; Ex. 1017, 59:2-14, 137:6-14, 137:24-138:4.) For example, as shown below, each of Fu and McAdams include an inverter connected to the terminal T1.

⁷ In contrast, Mr. de la Iglesia stated that he was unable to determine whether the Vcc terminal in figure 4 of Fu was capable of receiving a constant non-ground voltage without seeing the “entirety of the device.” (Ex. 1017, 190:19-191:9.)

(Petition at 34-38, 62-65; Ex. 1002, ¶¶90-95, 129-132.)



(Ex. 1005, FIG. 4 (left) (annotated); Ex. 1006, FIG. 1 (right) (annotated); Ex. 1002, ¶¶93, 130.)

If power is not enabled on Vcc for the inverters included in the programmable latch circuits in figure 4 of Fu and figure 1 of McAdams, those inverters cannot function to produce an output that is “high.” (Ex. 1018, ¶34.) As such, for the latch circuits of Fu and McAdams to be operational, Vcc must be providing a non-zero voltage. (*Id.*) If Vcc is disabled, the latch circuits are not operational and the respective outputs would not reflect the state of the respective fuses in the circuits. (*Id.*) Indeed, in McAdams, the latch operates (i.e., outputs a high or low voltage at output node 15) after “Vcc goes from zero to +5 v.” (Ex. 1006, 2:8-34.) In Fu, when the fuse is not blown, node A is at Vcc (high level) and when the fuse is blown,

transistor P10 turns on, which is only possible if Vcc is at a high level. (Ex. 1018, ¶34.) Thus, in both instances (fuse blown or intact), Fu’s circuit needs Vcc to be provided to operate. Therefore, in both of Fu and McAdams, Vcc is a non-zero voltage throughout operation of the latch, i.e., at all times during latch operation.

ProMOS’s other arguments fail because they are premised on its erroneous construction. Mr. de la Iglesia contends that each of Fu and McAdams “does not describe specific circuitry whose power is selectively enabled” and “does not discuss operating in different power modes, control of the power to circuitry or describe any circuitry as being advantageously power-gated.” (Ex. 2003, ¶¶35, 41.) But no such “power modes” or “selective enabl[ing]” of power are recited in claim 14, and it is unclear why “power-gat[ing]” of circuitry would be required by claim 14. (*See* Section II.A.) Indeed, Mr. de la Iglesia states that “[t]he exemplary diagrams of [Fu/McAdams] also show circuitry receiving power directly from the Vcc (positive voltage) rail” (*id.*), thereby confirming that when the circuit is operational, Vcc is supplying a non-ground (positive) voltage. (Ex. 1018, ¶33.) ProMOS’s argument seems to suggest that power on the Vcc rail would be disabled during operation, which makes little sense as the circuitry cannot operate without power being applied. (Ex. 1018, ¶¶33-34; Ex. 1017, 59:2-14, 137:6-14, 137:24-138:4.)

IV. CONCLUSION

The Board should find claims 14-19 of the ’492 patent unpatentable and

cancel them.

Respectfully submitted,

Dated: March 6, 2020

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)

Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petitioner's Reply to ProMOS's Response contains, as measured by the word-processing system used to prepare this paper, 5,477 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: March 6, 2020

By: /Naveen Modi/
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Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioner a true and correct copy of the foregoing Petitioner's Reply to ProMOS's Response and supporting exhibits by electronic means at the following address of record:

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