

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner

Case IPR2019-00779
Patent 6,163,492

**DECLARATION OF ERIK DE LA IGLESIA IN SUPPORT OF PATENT
OWNER PROMOS TECHNOLOGIES, INC.'S PRELIMINARY
RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

I, Erik de la Iglesia, hereby declare as follows

I. INTRODUCTION

1. I have been retained as an expert on behalf of ProMOS Technologies, Inc. (“ProMOS”) for the above-captioned Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 6,163,492 (the “’492 patent”).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$650 per hour. My compensation is not dependent on the outcome of this proceeding, the results of my analysis, or on the substance of my opinions and testimony.

3. I have been asked to provide my opinion on certain issues identified by counsel for ProMOS, set forth below.

4. In preparing this Declaration, I have reviewed the ’492 patent, the file history of the ’492 patent, and certain prior art references. I have also reviewed the petition for *inter partes* review from Petitioners Samsung Electronics Co. Ltd. (“Petitioner” or “Samsung”), including the material contained therein.

5. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and I have considered the viewpoint of a person having ordinary skill in the relevant art at the time of the invention.

II. BACKGROUND AND QUALIFICATIONS

6. I hold a BS in Electrical Engineering from the University of Florida and an MS in Electrical Engineering from Stanford where I was an NSF Research Fellow. My graduate focus included VLSI CMOS architecture and high-speed circuit design. I have worked in several computer and electrical engineering related fields for over 20 years resulting in 68 issued US patents which have been cited over 1650 times in USPTO patent applications. Since 2003 I have served in a number of chief architect and founder roles of companies that have been acquired or gone public.

7. Between December 1997 and November 1999, the time period of the invention, I was a circuit design engineer at Intel Corporation within the Mobile and Handheld Products Group. My responsibilities included working on several aspects of mobile processors and chipsets including clock and power distribution, dynamic clock frequency selection and the circuit design, device simulation and validation of such features. Capabilities such as dynamic clock frequency selection included fuse-enabled functionality that allowed manufacturing engineers to enable or disable the functionality for different product variants. My role included design, simulation and validation of the fuse structure and the fuse-enabled feature for release in the 1999 mobile Pentium III. Until March of 2000, I

worked on similar functionality within the Microprocessor Products Group for the Itanium 3 and 4 products.

8. Between March 2000 and September 2003 I worked as a logic designer and architect for WebStacks and later, through acquisition, Extreme Networks. WebStacks built a fully hardware-based TCP stack for network processing functions including load balancing, proxy processing and content rewrite. Upon acquisition by Extreme Networks, I worked as a logic design manager.

9. Between August 2003 and August 2007 I worked as Founder, Chief Architect and Director of Engineering for Reconnex, later acquired by McAfee. Reconnex built a gigabit line-rate network security analyzer capable of classification, heuristic analysis and policy enforcement on arbitrary protocols and content types.

10. Between August 2007 and September 2008 I founded Strangways, a company focused on addressing messaging security for webmail and internet messaging protocols. Products and technology developed by Strangways were sold to SendMail Inc, Iron Port (Cisco) and other companies.

11. Between September 2008 and April 2014 I worked as Chief Architect for Gridiron Systems and through acquisition Sr. Director of Technology for Violin Memory before and after the IPO. My responsibilities included architecture

and design of flash media controllers, adaptive caching design and machine learning for application behavior analytics.

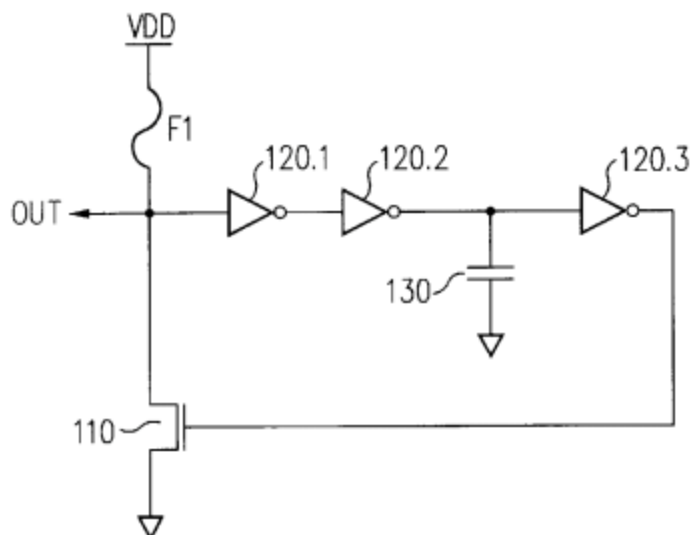
12. Additional information regarding my employment history is attached as Exhibit A.

III. BACKGROUND OF THE '492 PATENT

A. Brief Overview of the '492 Patent

13. The '492 patent, titled "Programmable latches that include non-volatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

14. Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



Ex. 1001 at Fig. 1.

15. Before power is applied to the latch at VDD, the terminal OUT may indicate the wrong state. Ex. 1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent: “when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal ‘may tend to have its potential raised to a logic level ‘1’.’ In addition, the terminal OUT potential may become ‘unstable due to the capacitive coupling’ in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown.” *Id.* at col. 1:38-47. Attempting to address these situations through the use of capacitor 130 causes operation to be delay-dependent and potentially faulty during slow powerup. *Id.* at col. 1:61-65.

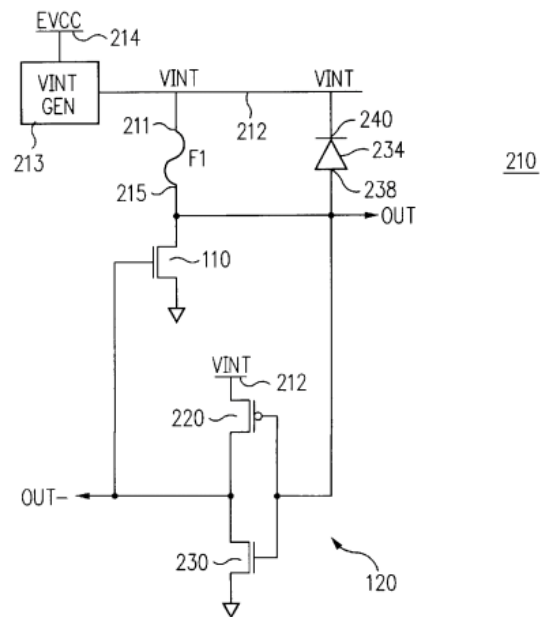
16. The solution presented in the '492 patent accomplishes the twin goals of preventing the output node (terminal OUT) from floating above ground when

power is off and from destabilizing through capacitive coupling during power-up.

In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node.

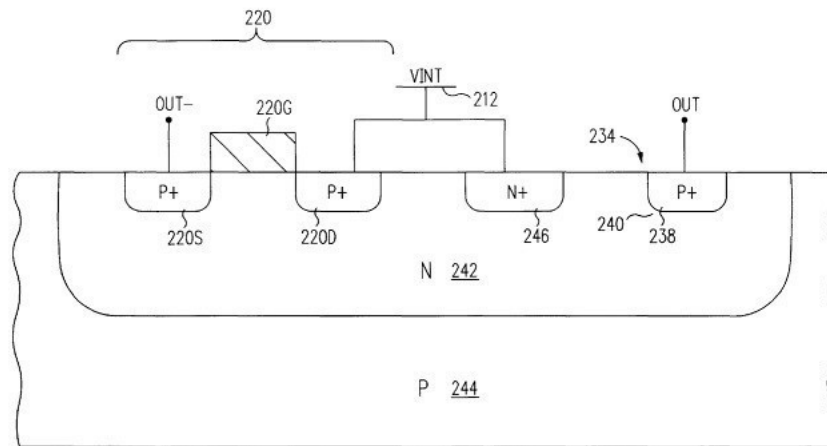
17. One prior attempt to address this problem described in the background of the '492 patent (at Fig. 1) is to place a capacitor 130 such that “[d]uring power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown. Then the ground voltage on terminal OUT propagates through the three inverters to keep transistor 110 on.” Ex. 1001 at col. 1:50-55. This design creates “delays provided by capacitor 130,” in particular when VDD rises slowly as the capacitor takes time to reach the correct voltage. *Id.* at col. 1:61-67.

18. The '492 patent solved these problems at power up through a first embodiment with a new circuit having a “diode that keeps a voltage on a latch output terminal within a predetermined range of values before power supplied is supplied to the latch.” Ex. 1001 at col. 2:1-4, claim 1. This first embodiment of the invention, including a diode, is shown in Fig. 2A:



Ex. 1001 at Fig. 2A.

19. The diode 234 in one preferred embodiment of the '492 patent is a CMOS diode constructed using a P-type anode and an N-type cathode. The conventional circuit diagram including the diode is shown in FIG. 2A wherein diode 234 has anode 238 (terminal at the flat-edge of the triangle) and cathode 240 (terminal at the pointed end of the triangle). Ex. 1001 at col. 3:34-36. In FIG. 2B, the anode is the P+ diffusion region 238 within an N-well 242 serving as cathode. *Id.* at col. 3:62-65.



Ex. 1001 at Fig. 2B.

20. Claim 1 is an example of an embodiment that utilizes a diode to discharge any voltage buildup on the terminal OUT:

1.pre) A programmable latch comprising:

1.a) a first terminal for receiving a first voltage;

1.b) a second terminal for receiving a second voltage;

1.c) a terminal T1 for providing a signal indicating a state of the programmable latch;

1.d) a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;

1.e) a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and

1.f) a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Ex. 1001 at Claim 1.

21. There are other embodiments that address the same problem – maintaining OUT at ground and preventing destabilization through capacitive coupling – without using a diode. In these embodiments, described below, any charge buildup at the output node must be allowed to dissipate from the circuit – with power off – before the output of the latch is used. The specification describes this embodiment, without a diode:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a

customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8.

22. In allowing excess voltage at the output node to dissipate before reading the latch, the risk of capacitive coupling at the terminal OUT is mitigated.

23. Claim 14 describes this embodiment which addresses the problem without using a diode:

14.pre) A programmable latch comprising:

14.a) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

14.b) a second terminal for receiving a voltage;

14.c) a terminal T1 for providing a signal indicating a state of the programmable latch;

14.d) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

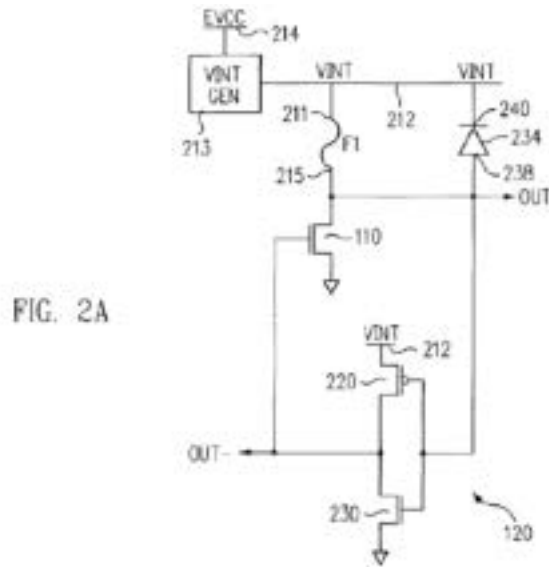
14.e) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and

14.f) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

Ex. 1001 at Claim 14.

24. By connecting a diode 234 to the OUT node (claim 1) or ensuring that the fuse is not programmed at run-time (claim 14), the '492 patent eliminates the possibility that increasing voltage or capacitive coupling at the OUT terminal causes that node to rise to a level that will turn on inverter 120 and cause a false state at the OUT terminal, in particular during power up.

25. Another aspect of the invention, shown for example in figure 2A below, is that the fuse connects the power source VINT to the output node OUT, whose value is read to indicate the state of the latch.



Ex. 1001 at Fig. 2A.

26. The fuse is claimed as a “non-volatile programmable element,” and each of claims 1 and 14 require that, when conductive, it connects the claimed “first terminal” (power) to the claimed “terminal T1” (terminal indicating the state of the latch). Ex. 1001 at claims 1, 14. Because of this structure, the fuse is directly indicative of the state of the latch and is the only device which affects the output. This concept was taken from the prior art embodiment in figure 1, stating “consistent with one advantage of prior art latch Figure 1, which the specification describes: “Prior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch

is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals. This advantage is preserved by some embodiments of the present invention.” Ex. 1001 at col. 2:22-27, 3:66-4:3.

IV. PERSON OF ORDINARY SKILL IN THE ART

27. I have adopted and applied Samsung’s level or ordinary skill in the art for purposes of this opinion.

V. CLAIM CONSTRUCTION

28. Other than the specific claim term discussed below, I have been asked to assume that the remaining claim terms have their ordinary customary meaning and that there are no specific constructions that I am to apply.

1. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch”

29. I understand that ProMOS has proposed a construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch” that is “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” I believe that this construction is consistent with the ’492 invention, including the specification and file history. There are several reasons I believe this to be the correct understanding:

30. First, the purpose of the '492 patent is to avoid false states at the output, a condition that may occur if excess voltage is allowed to accumulate at the output node during programming (either due to buildup during fuse cutting, for example laser application, or from capacitive coupling at the output node). Ex. 1001 at col. 1:46-48, 1:38-47. After programming, in order to avoid false states, the embodiment claimed in claim 14 must allow that excess voltage to dissipate before reading out the latch – otherwise the latch may indicate a false state and the terminal T1 will not indicate the state of the programmable latch, as claimed.

31. The specification also describes this conclusion, stating that the embodiment without a diode must be operated such that power is turned off after programming to avoid this problem:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse

was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

32. Thus, this embodiment without a diode requires the claim term “providing a signal indicating a state of the programmable latch” to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”

VI. INVALIDITY ANALYSIS

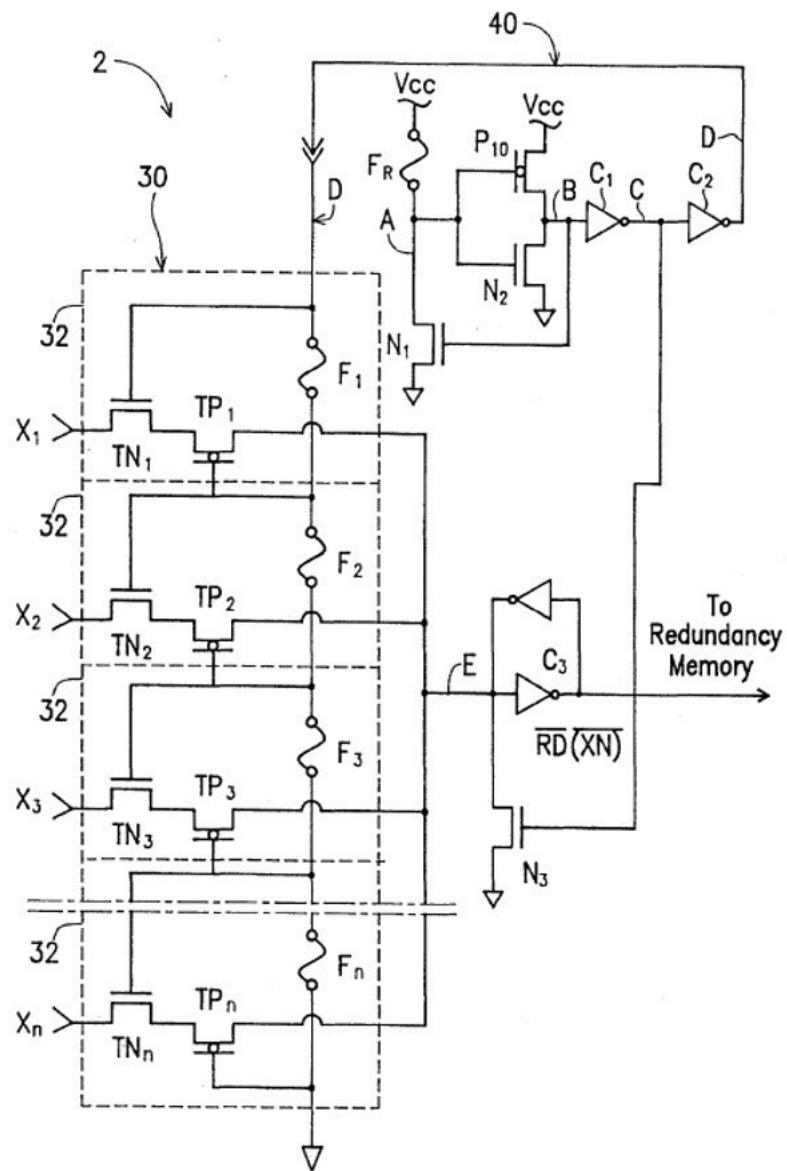
1. Fu and Fu/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

33. It is my opinion that the Fu reference (and therefore Fu/Sugibayashi) does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

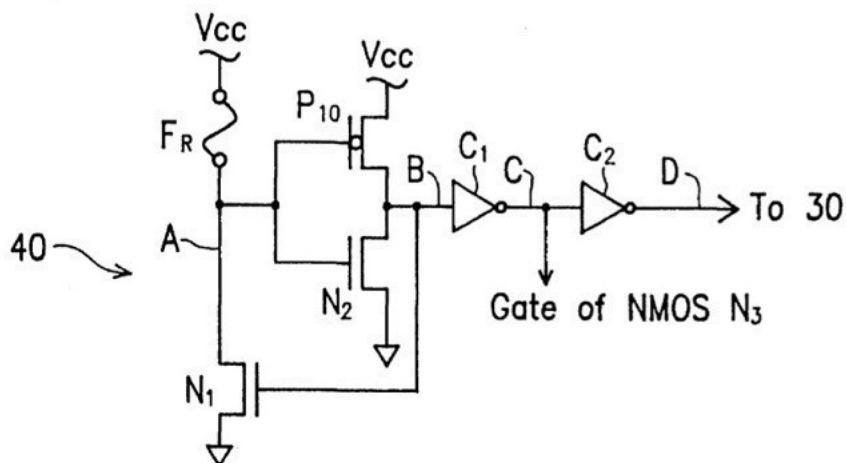
34. US5457656 to Fu (Fu) titled “Zero static power memory device redundancy circuitry” was filed as application number 08/292,331 on August 17, 1994 and has an earliest priority date of August 17, 1994. The invention relates generally to reducing the static power consumed by redundancy circuits for memory cells in memory devices. Ex. 1005 at col. 1:7-13, 2:60-62.

35. The Sugibayashi reference (US5373477) is only relied on by Samsung for its teaching of a generic internal voltage supply generating circuit, but does not include any teaching relevant to ProMOS’s claim construction.

36. Fu discloses an embodiment of a “redundancy activation circuit” (a latch controlled by a fuse) as Fig. 4 from the larger redundancy circuit of Fig. 2. The latch includes an inverter constructed using P_{10} and N_2 as well as inverters C_1 and C_2 . All three inverters are elements of the latch as the latch output is taken from nodes C and D, but not B. Ex. 1005 at col. 4:64-5:14.



Ex. 1005 at Fig. 2.



Ex. 1005 at Fig. 4.

37. Although Fu makes reference to the entire memory array operating between the same electrical potentials (Ex. 1005 at col. 3:44:51), Fu does not disclose “a terminal T1 for providing a signal indicating a state of the programmable latch.” The Fu circuit has no mechanism for dissipating voltage from the nodes in the latch. Fu describes the programming of the fuses (Ex. 1005 at col. 1:57-62) but does not disclose the operation of the programmable device. Specifically, as discussed earlier, claim 14 requires restricting operation of the latch to such times that any residual programming charge above a threshold value has dissipated. Ex. 1001 at col. 5:62-65. For this reason, Fu and the Fu/Sugibayashi combination do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

38. Sugibayashi describes an internal power supply system to remove overshoot within a step-down converter. Ex. 1011 at Abstract. As Sugibayashi

does not discuss latches, it cannot cure the above deficiency of Fu with regards to a “a terminal T1 for providing a signal indicating a state of the programmable latch.”

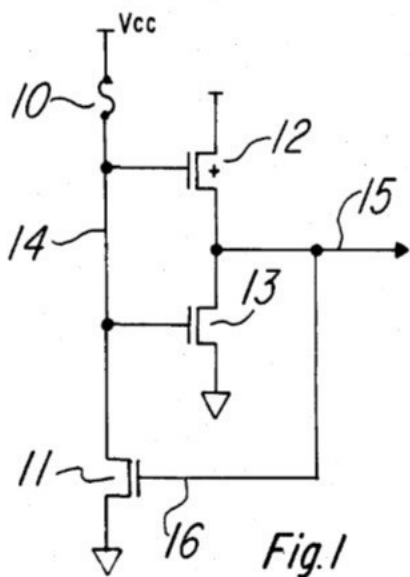
39. For the above reasons, I believe that Fu and Fu/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

2. McAdams and McAdams/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

40. It is my opinion that the McAdams reference (and therefore McAdams/Sugibayashi) do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

41. US4621346 to McAdams (McAdams) titled “Low power CMOS fuse circuit” was filed as application number 06/652,378 on September 20, 1984 and has an earliest priority date of September 20, 1984. The invention relates generally to a CMOS fuse designed for use in self-repairing memory devices. Ex. 1006 at Abstract.

42. The McAdams circuit is shown as Fig. 1 with fuse element 10 connected to the inverter formed by transistors 12 and 13. Ex. 1006 at col. 1:67-2:7.



Ex. 1005 at Fig. 1.

43. As with Fu, McAdams describes the programming of the fuse (Ex. 1006 at col. 1:12-14) but does not disclose operation of the latch. Specifically, as discussed earlier, claim 14 requires restricting operation of the latch to such times that any residual programming charge above a threshold value has dissipated. Ex. 1001 at col. 5:62-65. And the McAdams has no specific mechanism for dissipating all voltage at nodes 14 and 15, falling prey to the same problem described in the '492 patent. For this reason, McAdams and the McAdams/Sugibayashi combination do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

44. As Sugibayashi does not discuss latches at all, it cannot cure the above deficiency of McAdams with regards to “a terminal T1 for providing a signal indicating a state of the programmable latch.”

45. For the above reasons, I believe that McAdams and McAdams/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

46. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Dated: June 14, 2019

Respectfully submitted,

By: 
Erik de la Iglesia

Exhibit A

Erik de la Iglesia

Curriculum Vitae

Expert witness and IP strategist with entrepreneurial background as chief architect for both hardware and software-based companies in the information technology sector having generated acquisition values over \$100M and public offerings.

Legal and Litigation Experience

4/19 – Current TechKnowledge Law Group LLP (IPR, Patent Infringement, Validity)
Samsung Electronics v. Promos Technologies, Inc. Supporting Promos Technologies, Inc.

4/19 – Current Davis Firm PC (Patent Infringement)
Implicit, LLC v. Netscout Systems, Inc 2:18-cv-53-JRG Supporting Implicit

2/19 – Current Davis Firm PC (Patent Infringement)
RPost Holdings v. Adobe Systems 2:11-CV-325-JRG
RPost Holdings v. Amazon.com Inc., et al. 2:10-CV-258-JRG
RPost Holdings v. Right Signature, LLC (Citrix) 2:10-CV-258-JRG
RPost Holdings v. Selligent, Inc 2:12-cv-00515-JRG
Supporting RPost Holdings

11/18 – Current Russ August & Kabat (IPR / Patent Infringement)
Claims of Linksmart Wireless Technology IPR2019-00043 supporting Linksmart

5/18 – Current Stubbs Alderton & Markiles (Patent Infringement)
Claims of PersonalWeb Technologies, LLC supporting PersonalWeb Technologies, LLC.
PersonalWeb Technologies v. Amazon 5:18-cv-00767-BLF
PersonalWeb Technologies v. Twitch Interactive 5:18-cv-05619-BLF

3/18 – 4/18 Carlson Caspers (Technical Consulting)
Topics: Cellular Telephony

2/18 – 12/18 Latham Watkins (IPR, Patent Infringement)
FotoNation and DigitalOptics Corp v. Samsung 2:17-CV-669-RWS supporting FotoNation and DigitalOptics Corp

12/17 – Current Carlson Caspers (Patent Infringement)
CommScope Technologies v. Dali Wireless 3:16-cv-00477-M supporting CommScope

11/17 – 6/18 Demarais (Technical Consulting)
Topics: SAN / NAS Storage Technology

6/17 – 9/17 Cozen O'Connor (Patent Infringement, Validity, Domestic Industry)
LG v. BLU ITC 337-TA-1051 Supporting BLU

6/17 – 12/17 Fish & Richardson (Patent Infringement, Validity, Domestic Industry)
Broadcom v. MediaTek Inc. et al., 8:17-cv-00405-JVS-JCG
Broadcom v. MStar Semiconductor Inc., 8:17-cv-00406-JVS-JCG
Broadcom v. Mediatek / MStar ITC 337-TA-1047
Supporting Mediatek / MStar

3/17 – 5/17 Orrick, Herrington & Sutcliffe LLP (Technical Consulting)
Case: Mentor Graphics v. Synopsys supporting Synopsys
USC of Appeals for the Federal Circuit 2015-1470, 2015-1554, 2015-1556
Reviews of 3:10-cv-00954-MO, 3:12-cv-01500-MO, 3:13-cv-00579-MO

2/17 – 6/17 Cozen O'Connor (Patent Infringement)
BlackBerry vs. BLU 16-23535-CIV Supporting BLU

12/16 – 5/19 Weil, Gotshal & Manges (Technical Consulting)
Topics: Cloud Computing, Security

5/16 – 10/16 Gibson, Dunn & Crutcher (Patent Infringement, Validity)
EMC Corporation v. Pure Storage, Inc. 1:16-CV-00176-RGA Supporting EMC
Deposition

3/16 – 7/18 Schmeiser, Olsen & Watts (Technical Consulting)
Topics: Cellular Telephony, Power Generation Turbines

10/15 – 3/16 McKool Smith (Patent Infringement, Validity)
TCL Communication v. Telefonaktiebolaget LM Ericsson 8:14-CV-00341 Supporting Ericsson

4/15 – 9/15 McKool Smith (Patent Infringement)
AT&T Intellectual Property v. Cox Communications 14-1106-GMS Supporting AT&T

3/15 – 3/15 Keker & Van Nest (Patent Infringement)
Round Rock Research, LLC v. Sandisk 1:12-cv-12569-SLR Supporting Sandisk

11/14 – 3/15 Orrick, Herrington & Sutcliffe LLP (Patent Infringement)
Nvidia v. Qualcomm / Samsung ITC 337-TA-932 Supporting Nvidia
Deposition and Direct Testimony

7/14 – 10/15 Keker & Van Nest (Trade Secrets)
Sandisk v. Hynix 1:14-cv-262078 Supporting Sandisk

4/14 – 9/15 Latham & Watkins (Patent Infringement, Validity)
Market Track LLC v. ECRM, LLC 1:14-cv-4957 Supporting Market Track LLC.

4/14 – 12/14 McDermitt Will & Emory (Contract Dispute)
OneNeck v. Patrick 3:13-cv-00894 Supporting Patrick

Deposition

4/14 – 6/14 Latham & Watkins (Patent Infringement)
InterDigital v. Samsung 1:13-cv-00008-RGA Supporting InterDigital

4/13 – 5/14 Latham & Watkins (Patent Infringement)
InterDigital v. Samsung ITC 337-TA-868 Supporting InterDigital
Deposition and Direct Testimony

3/13 – 11/13 McKool Smith (Patent Infringement)
Ericsson v. Samsung ITC 337-TA-862 Supporting Ericsson

Technical Advisor Experience

9/14 – 12/16 Kodiak Data, Inc
Technology and Strategic advisor (Cloud Container Technology)

4/16 – 5/19 ShieldX
Technology and Strategic advisor (Cloud Security Technology)

Areas of Consulting and Expertise

ASIC, FPGA and Full-Custom Design, Computer Architecture, Computer Bus, Datapath, Pipelines, Cache, Memory and IO Systems, Network Protocols and Appliances, Wireless Networks and Transmission Systems, Network Application and Content Security, Email Processing, Security and Content Management, Storage Protocols and Appliances, Clustering Protocols, Storage Systems, Media and Technology, Flash Device, Controller and System Technology, Flash Wear Management and Issues, Hardware Description Languages and Design, Software Programming Languages and Environments, Storage Compression, Encoding, Deduplication and Error Correction, Performance Monitoring and Analysis, Application and Infrastructure Performance Optimization, Public and Private Cloud Infrastructure, Data Center Architecture and Performance, Computer Graphics

Issued US Patents (68)

6,490,703 6,553,545 6,732,288 7,152,124 7,298,746 7,321,926 7,434,058 7,447,777
7,584,262 7,657,104 7,689,614 7,730,011 7,774,604 7,814,327 7,818,326 7,899,828
7,907,608 7,930,540 7,958,227 7,962,591 7,984,175 8,005,863 8,010,689 8,160,070
8,166,307 8,176,049 8,200,026 8,214,599 8,214,608 8,271,794 8,285,961 8,301,635
8,307,007 8,307,206 8,402,198 8,402,246 8,417,871 8,417,895 8,442,059 8,443,150
8,463,800 8,504,537 8,548,170 8,554,774 8,560,693 8,635,416 8,650,362 8,656,039
8,667,366 8,683,035 8,713,252 8,730,955 8,762,386 8,775,741 8,788,758 8,830,836
8,832,384 8,838,850 8,959,288 8,972,689 9,069,676 9,092,471 9,094,338 9,195,407
9,244,861 9,344,525 9,374,225 9,424,180

Patents have been cited over 1650 times in USPTO issued patent.

Education

BS Electrical Engineering, University of Florida

MS Electrical Engineering, Stanford

Employment History

5/14 – Current

Technical and Legal Consulting

1/13 – 4/14 Violin Memory

Sr. Director of Technology

Responsible for integration of Gridiron technology with Violin Memory storage environments, patent strategy and portfolio acquisitions, technical review of development, systems architecture and flash media technology.

9/08 – 12/12 Gridiron Systems (acquired by Violin Memory)

Office of the CTO, Chief Architect

Gridiron Systems developed an in-line caching appliance for storage area networks using NAND Flash as a caching media. By deploying transparently within a fibre channel network, the appliance allows an existing storage system to operate at solid-state speeds without the need to reconfigure applications, servers or storage and with no data migration or changes to the storage configuration. Responsible for flash technology, adaptive caching, analytics and behavioral modeling, machine learning using Bayesian networks and clustering analytics.

8/07 – 9/08 Strangways

President, CEO

Lead team that designed and sold data leakage protection technology and design consulting to customers including SendMail Inc, IronPort (CSCO), Reconnex (MFE) and Autonomic Networks. Specialized in adaptive lexical parsing to handle webmail reconstruction and parsing for content scanning and policy enforcement.

8/07 - 9/08 Intellectual Property Consultant

Patent analysis consulting service for expert witnesses and patent portfolio evaluations. Infringement analysis and read citations from existing product literature, technical documents and corporate presentations.

8/03 – 8/07 Reconnex (Acquired by McAfee Corp)

Founder, Chief Architect, Director of Engineering

Lead technical development of Reconnex Data Leakage Protection security product with industry first gigabit-speed capture, document and content registration capability, real-time image analysis and classification, heuristic and policy-driven enforcement and data usage analytics. Reconnex technology allows enterprise IT staff to monitor their networks for illicit use of intellectual property or proprietary information and provides the enforcement capability and pattern analysis to aid in policy development.

3/01 – 7/03 Extreme Networks
Logic Design Manager

Lead hardware team supporting hardware and firmware elements of the acquired WebStacks product line. Switch design manager for stackables.

3/00 – 3/01 WebStacks (Acquired by Extreme Networks)
Architect

Developed TCP and HTTP proxy appliances using multiple FPGA-based protocol and semantic processing engines, TCAM search engines and embedded processing elements. Standards-based protocol analysis and handling in silicon for all layers of OSI stack.

12/97 – 3/00 Intel Corporation
Design Engineer

Power and Leakage modeling for future processors and processes. Analysis and development of bulk decoupling strategies and in-die process parameter skew. Developed first circuit to accurately determine the specific process parameter responsible for a yield deficiency.

Publications

Article for ComputerWorld
<http://www.computerworld.com.au/author/1205198773/erik-de-la-iglesia/articles>
Data leakage prevention: Port dependence dangers

Creative Storage Conference
[http://www.creativestorage.org/2011/book/erik de la iglesia.pdf](http://www.creativestorage.org/2011/book/erik%20de%20la%20iglesia.pdf)
Revolutionizing Streaming and Post-Production with Solid State Appliances

Flash Memory Summit 2011 (speaker)
[http://www.flashmemorysummit.com/English/Collaterals/Proceedings/2011/20110810_T1B_del aIglesia.pdf](http://www.flashmemorysummit.com/English/Collaterals/Proceedings/2011/20110810_T1B_del%20aIglesia.pdf)
MLC Flash for Enterprise Storage Performance

Flash Memory Summit 2012 (speaker)

http://www.flashmemorysummit.com/English/Collaterals/Proceedings/2012/20120822_TG21_Iglesia.pdf

Driving Down Healthcare Costs with Flash

Flash Memory Summit 2012 (speaker)

http://www.flashmemorysummit.com/English/Collaterals/Proceedings/2012/20120823_S301C_Iglesia.pdf

Abstracting the Flash Translation Layer for Enterprise-ready MLC

Storage Network Industry Association

https://www.snia.org/sites/default/education/tutorials/2012/spring/solid/Erik-delalglesia_Comparing_Three_Homes_SSD.pdf

Comparing the Three Homes for SSD in the Infrastructure

VMWare User Group Meetings (Melbourne and Sydney Australia Feb 2014)

Mission-Critical Enterprise Applications

Speaker at Vendor, Industry and User Group Events

- Oct 2011 – SF SQL Server User Group – How to Accelerate Your SQL Server Data Warehouse Workloads
- Feb 2012 - Northern California Oracle User Group – Increase Performance of Existing Oracle RAC
- October 2012 – New York Oracle User Group – Increase Performance of Existing Oracle RAC
- 2012 - Rocky Mountain Oracle User Group
- April 2012 Collaborate 12: Independent Oracle User Group – Get Exadata-class performance out of your existing Oracle RAC
- Assorted Vendor Conferences such as VM World, EMC World and Intel Developer's Forum conference