

FIG. 1
PRIOR ART

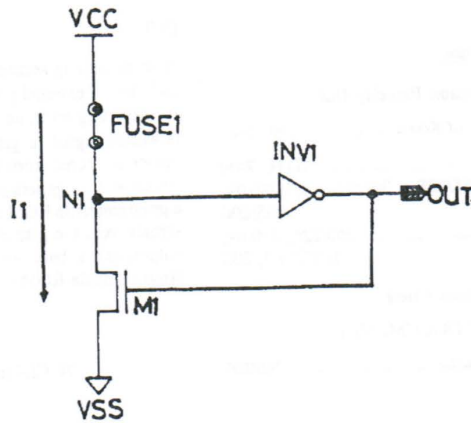
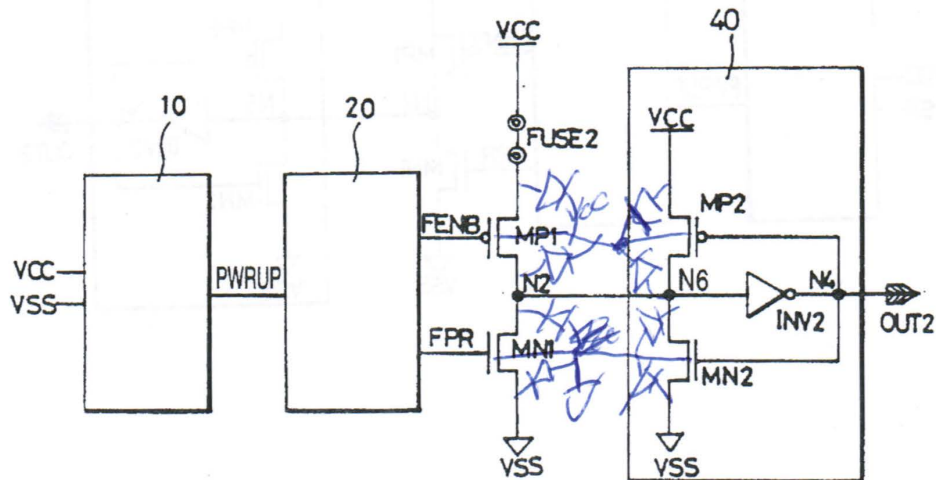


FIG. 2



N-well
P-sub





US005619469A

United States Patent [19]**Joo**[11] **Patent Number:** **5,619,469**[45] **Date of Patent:** **Apr. 8, 1997**[54] **FUSE REDUNDANCY CIRCUITRY FOR A SEMICONDUCTOR MEMORY DEVICE**

5,300,840 4/1994 Drouot 327/51

[75] Inventor: **Yang-Sung Joo**, Seoul, Rep. of Korea

Primary Examiner—Viet Q. Nguyen

[73] Assignee: **LG Semicon Co., Ltd.**,
Chungcheongbuk-do, Rep. of Korea

Assistant Examiner—Andrew Q. Tran

Attorney, Agent, or Firm—Morgan, Lewis and Bockius LLP

[21] Appl. No.: **569,795**[57] **ABSTRACT**[22] Filed: **Dec. 6, 1995**[30] **Foreign Application Priority Data**

May 26, 1995 [KR] Rep. of Korea 95-13405

[51] Int. Cl.⁶ **G11C 7/00**[52] U.S. Cl. **365/225.7; 365/226; 365/230.08;**
365/200[58] Field of Search 365/226, 230.08,
365/225.7, 200

A programming section of a semiconductor memory device includes an external power source detecting circuit adapted for detecting an initial power supply and for generating a power-up signal, a gate control section for receiving the power-up signal from the external power source detecting circuit and for generating a first signal and a second signal, a programmable ROM cell for receiving the first and second signals from the gate control section and for generating an output, and a latch section for latching the output of the programmable ROM cell.

[56] **References Cited****U.S. PATENT DOCUMENTS**

4,571,707 2/1986 Watanabe 365/200

20 Claims, 2 Drawing Sheets