

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner

Case IPR2019-00779
Patent 6,163,492

**DECLARATION OF ERIK DE LA IGLESIA IN SUPPORT OF PATENT
OWNER PROMOS TECHNOLOGIES, INC.'S RESPONSE TO PETITION
FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

I, Erik de la Iglesia, hereby declare as follows

I. INTRODUCTION

1. I have been retained as an expert on behalf of ProMOS Technologies, Inc. (“ProMOS”) for the above-captioned Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 6,163,492 (the “’492 patent”).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$650 per hour. My compensation is not dependent on the outcome of this proceeding, the results of my analysis, or on the substance of my opinions and testimony.

3. I have been asked to provide my opinion on certain issues identified by counsel for ProMOS, set forth below.

4. In preparing this Declaration, I have reviewed the ’492 patent, the file history of the ’492 patent, and certain prior art references. I have also reviewed the petition for *inter partes* review from Petitioners Samsung Electronics Co. Ltd. (“Petitioner” or “Samsung”), including the material contained therein.

5. In particular, I reviewed all claims at issue in the ’492 patent, including dependent claims, and Dr. Baker’s treatment of those claims. Dr. Baker’s opinions do not affect the outcome of my conclusions below.

6. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and I have considered the viewpoint of a person having ordinary skill in the relevant art at the time of the invention.

II. BACKGROUND AND QUALIFICATIONS

7. I hold a BS in Electrical Engineering from the University of Florida and an MS in Electrical Engineering from Stanford where I was an NSF Research Fellow. My graduate focus included VLSI CMOS architecture and high-speed circuit design. I have worked in several computer and electrical engineering related fields for over 20 years resulting in 68 issued US patents which have been cited over 1650 times in USPTO patent applications. Since 2003 I have served in a number of chief architect and founder roles of companies that have been acquired or gone public.

8. Between December 1997 and November 1999, the time period of the invention, I was a circuit design engineer at Intel Corporation within the Mobile and Handheld Products Group. My responsibilities included working on several aspects of mobile processors and chipsets including clock and power distribution, dynamic clock frequency selection and the circuit design, device simulation and validation of such features. Capabilities such as dynamic clock frequency selection included fuse-enabled functionality that allowed manufacturing engineers

to enable or disable the functionality for different product variants. My role included design, simulation and validation of the fuse structure and the fuse-enabled feature for release in the 1999 mobile Pentium III. Until March of 2000, I worked on similar functionality within the Microprocessor Products Group for the Itanium 3 and 4 products.

9. Between March 2000 and May 2003 I worked as a logic designer and architect for WebStacks and later, through acquisition, Extreme Networks. WebStacks built a fully hardware-based TCP stack for network processing functions including load balancing, proxy processing and content rewrite. Upon acquisition by Extreme Networks, I worked as a logic design manager.

10. Between August 2003 and August 2007 I worked as Founder, Chief Architect and Director of Engineering for Reconnex, later acquired by McAfee. Reconnex built a gigabit line-rate network security analyzer capable of classification, heuristic analysis and policy enforcement on arbitrary protocols and content types.

11. Between August 2007 and September 2008 I founded Strangways, a company focused on addressing messaging security for webmail and internet messaging protocols. Products and technology developed by Strangways were sold to SendMail Inc, Iron Port (Cisco) and other companies.

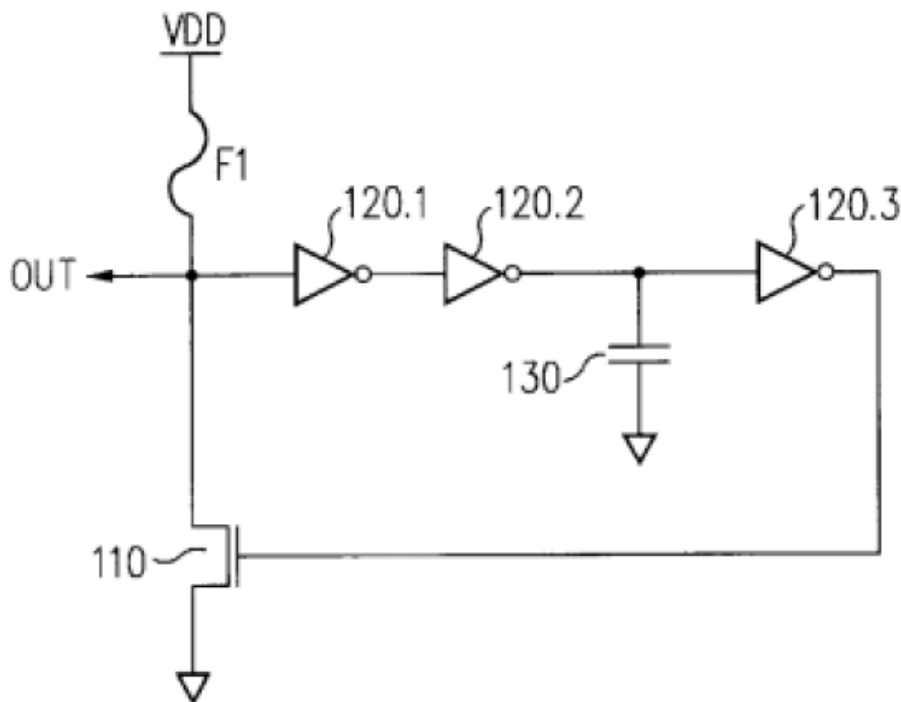
12. Between September 2008 and April 2014 I worked as Chief Architect for Gridiron Systems and through acquisition Sr. Director of Technology for Violin Memory before and after the IPO. My responsibilities included architecture and design of flash media controllers, adaptive caching design and machine learning for application behavior analytics.

III. BACKGROUND OF THE '492 PATENT

A. Brief Overview of the '492 Patent

13. The '492 patent, titled "Programmable latches that include nonvolatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

14. Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



Ex. 1001 at Fig. 1.

15. Before power is applied to the latch at VDD, the terminal OUT may indicate the wrong state. Ex. 1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent: "when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal 'may tend to have its potential raised to a logic level '1'.' In addition, the terminal OUT potential may become 'unstable due to the capacitive coupling' in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown." *Id.* at col. 1:38-47. Attempting to address these situations through the use of capacitor 130 causes operation to be delay dependent and potentially faulty during slow powerup. *Id.* at col. 1:61-65.

16. The solution presented in the '492 patent accomplishes the twin goals of preventing the output node (terminal OUT) from floating above ground when power is off and from destabilizing through capacitive coupling during power-up. In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node.

17. One prior attempt to address this problem described in the background of the '492 patent (at Fig. 1) is to place a capacitor 130 such that “[d]uring power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown. Then the ground voltage on terminal OUT propagates through the three inverters to keep transistor 110 on.” Ex. 1001 at col. 1:50-55. This design creates “delays provided by capacitor 130,” in particular when VDD rises slowly as the capacitor takes time to reach the correct voltage. *Id.* at col. 1:61-67.

18. Some embodiments address this problem – maintaining OUT at ground and preventing destabilization through capacitive coupling – by ensuring that any charge buildup at the output node is allowed to dissipate from the circuit – with power off – before the output of the latch is used. The specification describes this embodiment:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This

is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8.

19. In allowing excess voltage at the output node to dissipate before reading the latch, the risk of capacitive coupling at the terminal OUT is mitigated.

Claim 14 describes this embodiment which addresses the problem:

14.pre) A programmable latch comprising:

- 14.a) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;
- 14.b) a second terminal for receiving a voltage;
- 14.c) a terminal T1 for providing a signal indicating a state of the programmable latch;
- 14.d) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;
- 14.e) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable impedance path; and
- 14.f) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

Ex. 1001 at Claim 14.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. I have adopted and applied Samsung's level or ordinary skill in the art for purposes of this opinion.

V. CLAIM CONSTRUCTIONS

21. Other than the specific claim terms discussed below, I have been asked to assume that the remaining claim terms have their ordinary customary meaning and that there are no specific constructions that I am to apply.

22. For the claim constructions discussed below, my opinion is based on what a person of ordinary skill in the art would understand the claim terms to mean at the time the '492 patent application was filed.

A. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch”

23. I understand that ProMOS has proposed a construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch” that is “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” I believe that this construction is consistent with the '492 invention.

24. The purpose of the '492 patent is to avoid false states at the output, a condition that may occur if excess voltage is allowed to accumulate at the output node during programming (either due to buildup during fuse cutting, for example laser application, or from capacitive coupling at the output node). Ex. 1001 at col. 1:46-48, 1:38-47. After programming, in order to avoid false states, the

embodiment claimed in claim 14 must allow that excess voltage to dissipate before reading out the latch – otherwise the latch may indicate a false state and the terminal T1 will not indicate the state of the programmable latch, as claimed.

25. The specification also describes this conclusion, stating that the embodiment without a diode must be operated such that power is turned off after programming to avoid this problem:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its

final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

26. Thus, this embodiment without a diode requires the claim term “providing a signal indicating a state of the programable latch” to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”

B. “throughout operation of the latch” means “at all times during circuit operation without being disabled”

27. I understand that ProMOS has proposed a construction of the term “throughout operation of the latch” that is “at all times during circuit operation without being disabled.” I believe that this construction is consistent with the ’492 invention.

28. The term “throughout operation of the latch” appears once in the specification and is used to describe an embodiment in which a plurality of generators is used to power a synchronous DRAM. (’492 @ 4:66-5:7) In this embodiment, selective generators can be disabled to save power (id @ 5:1-2) to enable standby modes while at least one generator is enabled to power selected

circuitry. Under such design, the voltage VINT is described as “a constant value through the operation of the integrated circuit”. (id @ 5:5-7)

29. Such configuration is advantageous for a number of reasons. Leaving selected circuitry in standby while other circuitry is unpowered is a common technique to allow faster return from low-power or standby operation. Additionally, utilizing multiple enable signals allows higher granularity in the selection of which circuitry to power enabling a higher number of operating modes. In some cases, multiple power enable signals can also be used to enable the use of a device within multiple power envelopes (such as desktop, mobile, embedded, etc).

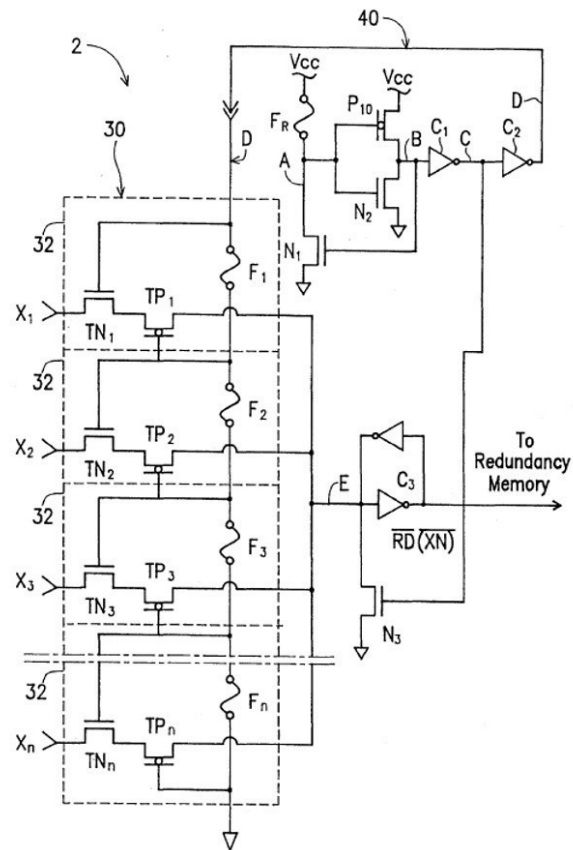
VI. INVALIDITY ANALYSIS

A. Fu does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch”

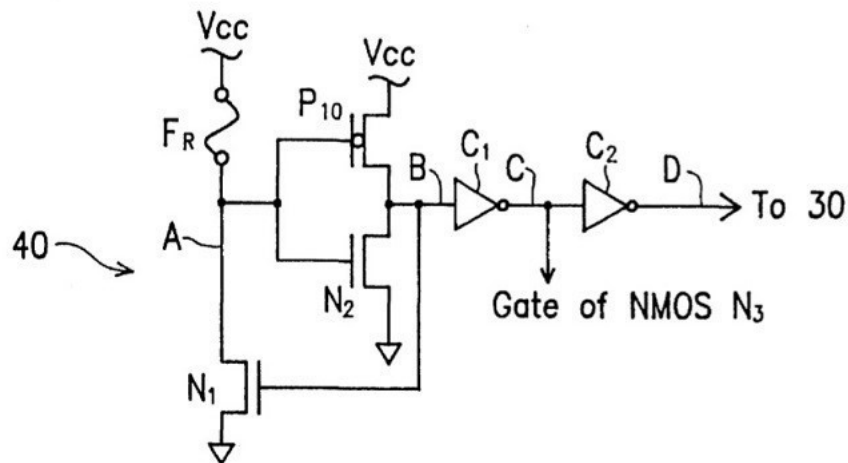
30. It is my opinion that the Fu reference does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

31. US5457656 to Fu (Fu) titled “Zero static power memory device redundancy circuitry” was filed as application number 08/292,331 on August 17, 1994 and has an earliest priority date of August 17, 1994. The invention relates generally to reducing the static power consumed by redundancy circuits for memory cells in memory devices. Ex. 1005 at col. 1:7-13, 2:60-62.

32. Fu discloses an embodiment of a “redundancy activation circuit” (a latch controlled by a fuse) as Fig. 4 from the larger redundancy circuit of Fig. 2. The latch includes an inverter constructed using P_{10} and N_2 as well as inverters C_1 and C_2 . All three inverters are elements of the latch as the latch output is taken from nodes C and D, but not B. Ex. 1005 at col. 4:64-5:14.



Ex. 1005 at Fig. 2.



Ex. 1005 at Fig. 4.

33. Although Fu makes reference to the entire memory array operating between the same electrical potentials (Ex. 1005 at col. 3:44:51), Fu does not disclose “a terminal T1 for providing a signal indicating a state of the programmable latch.” The Fu circuit has no mechanism for dissipating voltage from the nodes in the latch. Fu describes the programming of the fuses (Ex. 1005 at col. 1:57-62) but does not disclose the operation of the programmable device. Specifically, as discussed earlier, claim 14 requires restricting operation of the latch to such times that any residual programming charge above a threshold value has dissipated. Ex. 1001 at col. 5:62-65. For this reason, Fu does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

B. Fu does not teach “throughout operation of the latch”

34. It is my opinion that the Fu reference does not teach “throughout operation of the latch.”

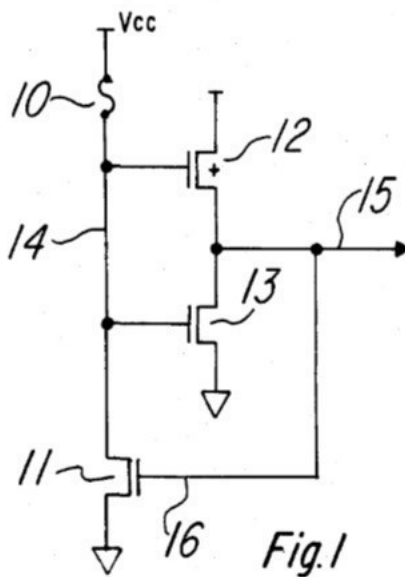
35. As described above, the term “throughout the operation of the latch” is related to the operation of circuitry whose power is not disabled during operation. Fu does not describe specific circuitry whose power is selectively enabled. In fact, Fu does not discuss operating in different power modes, control of the power to circuitry or describe any circuitry as being advantageously power-gated. The exemplary diagrams of Fu also show circuitry receiving power directly from the Vcc (positive voltage) rail.

C. McAdams does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch”

36. It is my opinion that the McAdams reference does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

37. US4621346 to McAdams (McAdams) titled “Low power CMOS fuse circuit” was filed as application number 06/652,378 on September 20, 1984 and has an earliest priority date of September 20, 1984. The invention relates generally to a CMOS fuse designed for use in self-repairing memory devices. Ex. 1006 at Abstract.

38. The McAdams circuit is shown as Fig. 1 with fuse element 10 connected to the inverter formed by transistors 12 and 13. Ex. 1006 at col. 1:67-2:7.



Ex. 1005 at Fig. 1.

39. As with Fu, McAdams describes the programming of the fuse (Ex. 1006 at col. 1:12-14) but does not disclose operation of the latch. Specifically, as discussed earlier, claim 14 requires restricting operation of the latch to such times that any residual programming charge above a threshold value has dissipated. Ex. 1001 at col. 5:62-65. And the McAdams has no specific mechanism for dissipating all voltage at nodes 14 and 15, falling prey to the same problem described in the '492 patent. For this reason, McAdams does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

D. McAdams does not teach “throughout operation of the latch”

40. It is my opinion that the McAdams reference does not teach “throughout operation of the latch.”

41. As described above, the term “throughout the operation of the latch” is related to the operation of circuitry whose power is not disabled during operation. McAdams does not describe specific circuitry whose power is selectively enabled. In fact, McAdams does not discuss operating in different power modes, control of the power to circuitry or describe any circuitry as being advantageously power-gated. The exemplary diagrams of McAdams also show circuitry receiving power directly from the Vcc (positive voltage) rail.

E. Sugibayashi does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch”

42. It is my opinion that the Sugibayashi reference does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

43. The Sugibayashi reference (US5373477) is only relied on by Samsung for its teaching of a generic internal voltage supply generating circuit, but does not include any teaching relevant to ProMOS’s claim construction.

44. Sugibayashi describes an internal power supply system to remove overshoot within a step-down converter. Ex. 1011 at Abstract. As Sugibayashi

does not discuss latches, it cannot cure the above deficiency of Fu with regards to a “a terminal T1 for providing a signal indicating a state of the programmable latch.”

F. Sugibayashi does not teach “throughout operation of the latch”

45. It is my opinion that the Sugibayashi reference does not teach “throughout operation of the latch.” As described above, the term “throughout the operation of the latch” is related to the operation of circuitry whose power is not disabled during operation. Sugibayashi does not describe the enablement or disablement of power to circuitry nor any concept of selectively powering circuitry. The Sugibayashi invention deals with managing the overshoot of a voltage during powerup of a step-down power converter.

46. As a general matter, step-down power converters are generally not designed as multiple separately-enabled generators for complexity and stability reasons. It is also difficult to implement such design where circuitry must enter multiple power states (selective enablement) as the comparators (such as elements 12j, 12m, 12n and 12p of Sugibayashi FIG. 6) take time to bias and consume considerable static current. And voltage generators are often used with enable/disable circuitry, logic enabling, or other clocking in order to conserve power where not needed. This would make the Sugibayashi design a poor choice for the power enable concept of the ‘492 patent.

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I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Dated: December 5, 2019

Respectfully submitted,

By:



Erik de la Iglesia