

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2019-00779
Patent 6,163,492

**PATENT OWNER PROMOS TECHNOLOGIES, INC.'S PRELIMINARY
RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
PO Box 1450
Alexandria, Virginia 22313-1450

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. OVERVIEW OF '492 PATENT	1
III. OVERVIEW OF PRIOR ART	8
A. Fu	8
B. McAdams	9
IV. ARGUMENT	10
A. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch”	10
B. Fu and Fu/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch” (claims 14-19)	13
C. McAdams and McAdams/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch” (claims 14-19)	13

TABLE OF AUTHORITIES

Page(s)

Cases

MasterMine Software, Inc. v. Microsoft Corp.,
874 F.3d 1307 (Fed. Cir. 2017)10

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) (en banc)10

Statutes

35 U.S.C. § 3131

Other Authorities

37 C.F.R. § 42.1071

83 Fed. Reg. 51340-58 (Oct. 11, 2018)10

I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Patent Owner ProMOS Technologies, Inc. hereby preliminarily responds to Samsung's Petition for *Inter Partes* Review seeking cancellation of claims 14-19 of U.S. Patent No. 6,163,492 (Ex. 1001, hereinafter the "'492 patent").

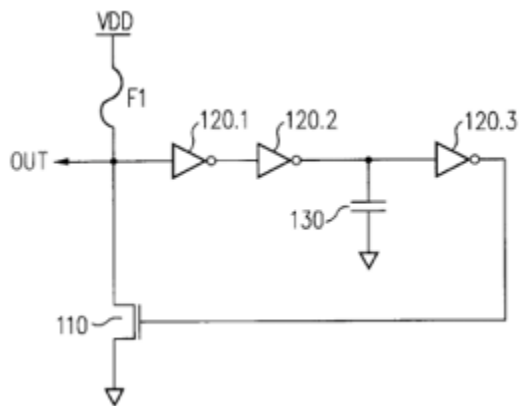
Samsung's petition relies on a flawed understanding of the claim term "a terminal T1 for providing a signal indicating a state of the programmable latch." In order for the terminal T1 to "provid[e] a signal indicating a state of the programmable latch" and not a false state instead, any voltage accumulated on the output during programming must be dissipated before the latch is used. Thus, the term should be construed as "a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch." With this proper construction, both Fu and McAdams – the two references submitted as meeting this claim element – fail to teach it. Accordingly, Samsung has not met its burden to institute *inter partes* review of the challenged claims.

II. OVERVIEW OF '492 PATENT

The '492 patent, titled "Programmable latches that include non-volatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention

relates generally to improving the reliability of programmable latches during power up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



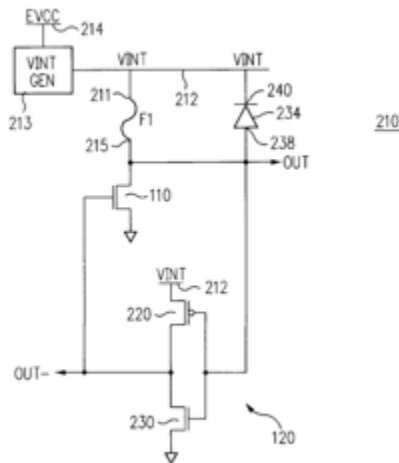
Ex. 1001 at Fig. 1.

Before power is applied to the latch at VDD, the terminal OUT may indicate the wrong state. Ex. 1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent: "when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal 'may tend to have its potential raised to a logic level '1'." In addition, the

terminal OUT potential may become ‘unstable due to the capacitive coupling’ in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown.” *Id.* at col. 1:38-47. Attempting to address these situations through the use of capacitor 130 causes operation to be delay-dependent and potentially faulty during slow power up. *Id.* at col. 1:61-65.

The solution presented in the ’492 patent accomplishes the twin goals of preventing the output node (terminal OUT) from floating above ground when power is off and from destabilizing through capacitive coupling during power up. In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node.

The ’492 patent solved these problems at power up through a first embodiment with a new circuit having a “diode that keeps a voltage on a latch output terminal within a predetermined range of values before power is supplied to the latch.” Ex. 1001 at col. 2:1-4, claim 1. This first embodiment of the invention, including a diode, is shown in Fig. 2A:



Ex. 1001 at Fig. 2A.

Claim 1 is an example of an embodiment that utilizes a diode to discharge any voltage buildup on the terminal OUT:

- 1.pre) A programmable latch comprising:
 - 1.a) a first terminal for receiving a first voltage;
 - 1.b) a second terminal for receiving a second voltage;
 - 1.c) a terminal T1 for providing a signal indicating a state of the programmable latch;
 - 1.d) a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;

1.e) a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and

1.f) a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Ex. 1001 at Claim 1.

There are other embodiments that address the same problem – maintaining OUT at ground and preventing destabilization through capacitive coupling – without using a diode. In these embodiments, described below, any charge buildup at the output node must be allowed to dissipate from the circuit – with power off – before the output of the latch is used. The specification describes this embodiment, without a diode:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a

customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

In allowing excess voltage at the output node to dissipate before reading the latch, the risk of a floating voltage or capacitive coupling at the terminal OUT is mitigated.

Claim 14 describes this embodiment which addresses the problem without using a diode:

14.pre) A programmable latch comprising:

14.a) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

14.b) a second terminal for receiving a voltage;

14.c) a terminal T1 for providing a signal indicating a state of the programmable latch;

14.d) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

14.e) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and

14.f) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

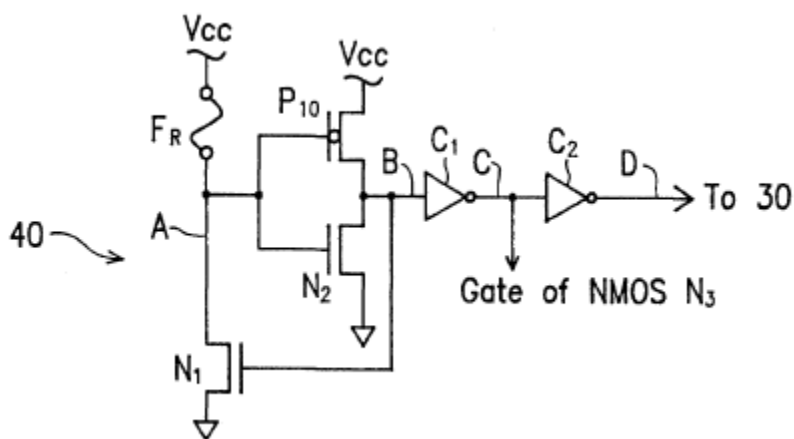
Ex. 1001 at Claim 14.

By connecting a diode 234 to the OUT node (claim 1) or ensuring that the fuse is not programmed at run-time (claim 14), the '492 patent eliminates the possibility that increasing voltage or capacitive coupling at the OUT terminal causes that node to rise to a level that will turn on inverter 120 and cause a false state at the OUT terminal.

III. OVERVIEW OF PRIOR ART

A. Fu

Fu describes a memory redundancy apparatus used for replacing defective memory cells, like the '492. However, Fu is not directed at reducing false-state transitions and is not directed at problems associated with capacitive coupling or floating voltage increases at the output. Rather, Fu is a circuit aimed at power savings when not in use. Ex. 1005 at col. 1:11-13. Fu Fig. 4 is repeated below:

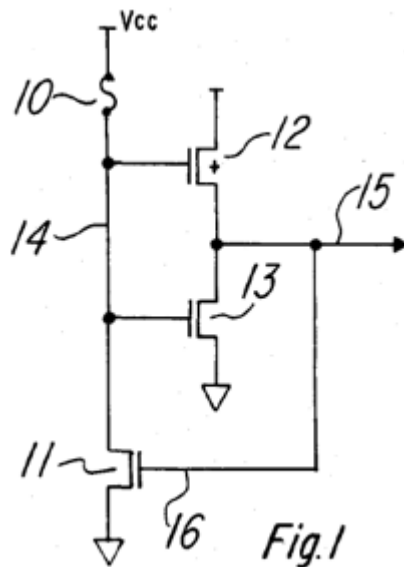


Ex. 1005 at Fig. 4.

In the above figure, the W/L ratio of N1 is much larger than N2, and therefore a low voltage at node A and a high voltage at node B is maintained, without any electric power consumption. Ex. 1005 at col. 4:35-44. Fu talks about programming the fuse (*Id.* at col 1:57-62), but does not talk about operation of the latch, and specifically does not disclose when programming is done with respect to run-time of the latch.

B. McAdams

McAdams teaches a fuse circuit for selecting a new memory cell where one is defective, and according to McAdams less power is consumed using the circuit of figure 1 because of feedback transistor 11, connected to the output of inverter 12/13.



Ex. 1006 at Fig. 1.

The McAdams circuit above does not inherently ensure that undesired voltage at nodes 14 and 15 dissipates, and further the patent does not discuss operation of the latch at all. More specifically, McAdams does not specify when the latch is operated with respect to programming and whether power is turned off in order to allow voltage to dissipate after programming.

IV. ARGUMENT

- A. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch”**

Claim 14 claims “a terminal T1 for providing a signal indicating a state of the programmable latch.” This term means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” Samsung has not proposed any construction for this term, instead arguing that all claim terms are to be given their ordinary and customary meaning. Pet. at 15-16.

Claim construction in this proceeding is to be under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); *see* 83 Fed. Reg. 51340-58 (Oct. 11, 2018).

Importantly, this term requires that power to the latch is off between programming and use, because otherwise the terminal will not “indicate[] a state of the programmable latch” as it suffers from the risk of false output that was discussed in the background of the patent. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2001 at ¶30; *see e.g., MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1315 (Fed. Cir. 2017) (interpreting an apparatus claim with “presents,” “receives,” and “generates” terms as requiring “capability of the structure” or the

“particular capabilities” of the structure) (citing *UltimatePointer, LLC v. Nintendo Co.*, 73 F. Supp. 3d 1305, 1308 (W.D. Wash. 2014)).

As stated in the background of the '492 patent, the entire purpose of the invention is to eliminate the problem of a false output because of excess voltage at T1 accumulated from programming or from capacitive coupling at the output. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2001 at ¶30. And if voltage is not dissipated after programming, then the terminal T1 will not necessarily indicate the state of the latch, as claimed, because it may indicate a false state due to this programming voltage. Ex. 2001 at ¶30. Therefore, in order for the terminal T1 to “indicate[] a state of the programmable latch” as claimed, power must be turned off to allow voltage to dissipate from the output node after programming.

The specification also specifically supports this construction. Ex. 2001 at ¶31. In distinguishing embodiments with a diode (claim 1) from those without (the immediate claim, claim 14), the specification states that power must be turned off after programming, as ProMOS's construction requires:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part

of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

Thus, in order to practice this embodiment (without a diode), and to perform the claimed operation of “providing a signal indicating a state of the programmable latch” the claim term “a terminal T1 for providing a signal indicating a state of the programmable latch” must be construed to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”

B. Fu and Fu/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch” (claims 14-19)

The Fu reference (Exhibit 1005) does not have “a terminal T1 for providing a signal indicating a state of the programmable latch” throughout operation of the latch. Fu does not teach any mechanism for dissipating voltage from its internal nodes, and further does not teach any operation of its latch. There is therefore no teaching that any voltage buildup at the internal nodes is dissipated before operation. Ex. 2001 at ¶¶36-37. This creates the potential that the Fu circuit falls failure to the same problem that the ’492 invention solved – the latch may indicate the wrong state during power up. *Id.* Therefore, Fu and Fu/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

C. McAdams and McAdams/Sugibayashi do not teach “a terminal T1 for providing a signal indicating a state of the programmable latch” (claims 14-19)

The McAdams reference (Exhibit 1006) similarly does not have “a terminal T1 for providing a signal indicating a state of the programmable latch,” when that phrase is properly construed. The McAdams circuit does not inherently dissipate voltage that accumulates on nodes 14 and 15, which is the point of the ’492 invention. Ex. 2001 at ¶43. The capacitive coupling downstream from this circuit in McAdams allows the floating node 15 to stray far from its initialization state,

and absent any teaching that the latch is programmed and left unpowered before being read, the McAdams circuit suffers from this capacitive coupling. *Id.*

McAdams therefore does not meet the proper construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Except as to the claim limitation acknowledged above, ProMOS explicitly reserves its right to argue that the cited references do not anticipate or render obvious the identified claims if the IPR is instituted.

Dated: June 14, 2019

Respectfully submitted,

By: /s/ Craig R. Kaufman
Registration No. 34,636
Lead Counsel for Patent Owner
TechKnowledge Law Group LLP
100 Marine Parkway, Suite 200
Redwood Shores, CA 94065
650-517-5200

APPENDIX OF EXHIBITS

Exhibit No.	Description
2001	Declaration of Erik de la Iglesia in Support of Patent Owner ProMOS Technologies, Inc.'s Preliminary Response

CERTIFICATE OF SERVICE

I hereby certify that on June 14, 2019, a true and correct copy of the foregoing *Patent Owner Promos Technologies, Inc.'s Preliminary Response to Petition for Inter Partes Review of United States Patent No. 6,163,492* and all supporting exhibits were served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

Naveen Modi (Reg. No. 46,224)
Paul Hastings LLP,
875 15th St. N.W.
Washington, DC, 20005
Telephone: 202.551.1990
Fax: 202.551.1705
Email: PH-Samsung-ProMOS3-
IPR@paulhastings.com

Joseph E. Palys (Reg. No. 46,508)
Paul Hastings LLP,
875 15th St. N.W.
Washington, DC, 20005
Telephone: 202.551.1996
Fax: 202.551.1705
Email: PH-Samsung-ProMOS3-
IPR@paulhastings.com

Chetan R. Bansal
(Limited Recognition No. L0667)
Paul Hastings LLP,
875 15th St. N.W.
Washington, DC, 20005
Telephone: 202.551.1948
Fax: 202.551.1705
Email: PH-Samsung-ProMOS3-
IPR@paulhastings.com

Paul M. Anderson
(Reg. No. 39,896)
Paul Hastings LLP,
600 Travis Street
Houston, TX 77002
Telephone: 713.860.7353
Fax: 713.353.3473
Email: PH-Samsung-ProMOS3-
IPR@paulhastings.com

By: /s/ Deborah L. Grover
Deborah L. Grover
TechKnowledge Law Group LLP
100 Marine Parkway, Suite 200
Redwood Shores, CA 94065
650-517-5200

**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION REQUIREMENTS**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned attorney of record, hereby
certifies that:

This brief complies with the type-volume limitation of 37 C.F.R. § 42.24(b).
The brief contains 2,685 words, excluding the parts of the brief exempted by 37
C.F.R. § 42.24.

Date: June 14, 2019

/s/ Craig R. Kaufman
Registration No. 34,636
Lead Counsel for Patent Owner