

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2019-00779
Patent 6,163,492

Before KEVIN F. TURNER, JO-ANNE M. KOKOSKI, and
JULIA HEANEY, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 14–19 of U.S. Patent No. 6,163,492 (“the ’492 patent,” Ex. 1001). Paper 1 (“Pet.”). ProMOS Technologies, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314; *see* 37 C.F.R. § 42.4. Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least 1 claim of the ’492 patent. Accordingly, we institute an *inter partes* review of claims 14–19 of the ’492 patent.

A. *Related Proceedings*

The parties indicate that the ’492 patent is being asserted in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:18-cv-00307-RGA (D.Del.), and is the subject of IPR2019-00780 and IPR2019-00781, also filed by Petitioner. Pet. 1; Paper 5, 1.

B. *The ’492 Patent*

The ’492 patent is titled “Programmable Latches That Include Non-Volatile Programmable Elements.” Ex. 1001, at [54]. According to the ’492 patent, “[p]rogrammable latches with fuses are used in integrated circuits to enable modification of the circuits without changing the masks used for circuit fabrication.” *Id.* at 1:19–21. An example of such a prior art latch is depicted in Figure 1 of the ’492 patent. *Id.* at 1:24–25. The ’492 patent

explains that during operation of the latch of Figure 1, the output terminal OUT will be pulled to VDD if fuse F1 is intact. *Id.* at 1:32. If fuse F1 is blown, then transistor 110 will be turned on and keep output terminal OUT at ground. *Id.* at 1:34–35. The '492 patent explains that when the power is off, output terminal OUT is floating and may provide an unstable or erroneous voltage. *Id.* at 1:38–47. In the prior art latch of Figure 1, bypass capacitor 130 is intended to avoid such malfunction and insure correct initialization of the latch on power-up. *Id.* at 1:36–55. “During power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown.” *Id.* at 1:49–52.

The '492 patent further describes how “[d]ependence on delays is undesirable because delay-dependent circuits may not operate properly if VDD rises slowly.” *Id.* at 1:63–65. Thus, according to the '492 patent, programmable latches such as those described in the specification are more reliable “because they do not depend on delays such as delays provided by capacitor 130.” *Id.* at 62–63. In particular, “[h]igh reliability is achieved in some embodiments by a diode that keeps a voltage on a latch output terminal within a predetermined range of values before power is supplied to the latch.” *Id.* at 2:1–4.

Figure 2A of the '492 patent is reproduced below.

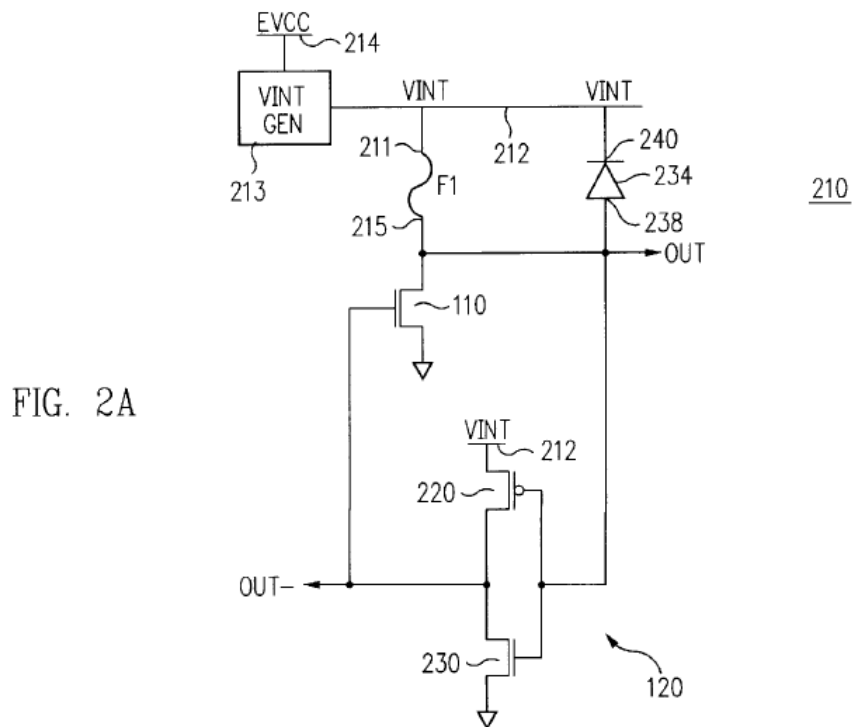


Figure 2A “is a circuit diagram of a programmable latch according to the present invention.” Ex. 1001, 2:64–65. Figure 2A shows a programmable latch 210 including a fuse F1, NMOS¹ transistor 110, CMOS inverter 120, VINT generator 213, and diode 234. As depicted in Figure 2A, CMOS inverter 120 is formed by PMOS pull-up transistor 220 and NMOS pull-down transistor 230. *Id.* at 3:24–26.

In the embodiment of Figure 2A, output terminal OUT is connected to terminal 215 of fuse F1, the drain of NMOS transistor 110, and anode terminal 238 of diode 234. *Id.* at 3:20–23. Thus, “[i]f fuse F1 is conductive, then terminal OUT is at VINT, and transistor 110 is turned off by inverter

¹ MOS stands for metal-oxide-semiconductor. Ex. 1015, 12.

120.” *Id.* at 3:50–51. When the power is off, VINT terminal 212 is at ground, and diode 234 limits the voltage on terminal OUT to the threshold voltage of diode 234. *Id.* at 3:35–40. The threshold voltage of diode 234 is “below the trip voltage of inverter 120 and even below the threshold voltage of NMOS transistor 230.” *Id.* at 3:42–43. “Therefore, if fuse F1 is blown, transistor 230 remains off when the power is turned on.” *Id.* at 3:45–46. When the power is turned on, PMOS pull-up transistor 220 charges the gate of transistor 110 to its threshold voltage, and transistor 110 connects the terminal OUT to ground. *Id.* at 3:46–49.

C. Challenged Claims

Petitioner challenges claims 14–19 (“the challenged claims”) of the ’492 patent. Claim 14 is the only independent claim, and is reproduced below.

14. A programmable latch comprising:
 - a first terminal for receiving a constant non-ground voltage throughout operation of the latch;
 - a second terminal for receiving a voltage;
 - a terminal T1 for providing a signal indicating a state of the programmable latch;
 - a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;
 - a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for

controlling the impedance of the variable-impedance path; and

an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter input.

Ex. 1001, 10:3–27.

D. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 14–19 of the '492 patent on the following grounds:

Reference(s)	Basis	Challenged Claims
Fu ²	§ 102	14–19
McAdams ³	§ 102	14–19
Fu and Sugibayashi ⁴	§ 103	14–19
McAdams and Sugibayashi	§ 103	14–19

Petitioner relies on the Declaration of R. Jacob Baker, Ph.D., P.E. (“Baker Declaration,” Ex. 1002) in support of its contentions. Patent Owner relies on the Declaration of Erik de la Iglesia (Ex. 2001) in support of its Preliminary Response.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person having ordinary skill in the art (“POSITA”) “would have had a bachelor’s degree in electrical engineering or a similar field, and at least two to three years of experience in integrated

² U.S. Patent No. 5,457,656, issued Oct. 10, 1995 (Ex. 1005).

³ U.S. Patent No. 4,621,346, issued Nov. 4, 1986 (Ex. 1006).

⁴ U.S. Patent No. 5,373,477, issued Dec. 13, 1994 (Ex. 1011).

circuit design,” and that “[m]ore education can supplement practical experience and vice versa.” Pet. 3–4. Patent Owner does not dispute Petitioner’s proposed definition at this stage of the proceeding. *See* Ex. 2001 ¶ 27 (Patent Owner’s declarant stating that he has “adopted and applied Samsung’s level [of] ordinary skill in the art for purposes of” his opinions). Accordingly, for purposes of this Decision, we adopt Petitioner’s assessment of the level of ordinary skill in the art, which is consistent with the level of ordinary skill in the art at the time of the invention as reflected in the prior art in this proceeding. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Claim Interpretation

For petitions such as this one, filed after November 13, 2018, we apply the same claim construction standard “used in the federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), which is articulated in” *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 83 Fed. Reg. 51,340, 51,343 (Oct. 11, 2018). Under the *Phillips* standard, the “words of a claim ‘are generally given their ordinary and customary meaning,’” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312–13. Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the

extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner contends that “no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.” Pet. 15–16. Patent Owner argues that the term “a terminal T1 for providing a signal indicating a state of the programmable latch” in claim 14 should be construed to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” Prelim. Resp. 10. Patent Owner argues that “this term requires that power to the latch is off between programming and use, because otherwise the terminal will not ‘indicate[] a state of the programmable latch’ as it suffers from the risk of false output that was discussed in the background of the patent.” *Id.* (citing Ex. 1001, 1:38–48; Ex. 2001 ¶ 30). Patent Owner further argues that the Specification supports this construction because, “[i]n distinguishing embodiments with a diode (claim 1) from those without (the immediate claim, claim 14), the specification states that power must be turned off after programming.” *Id.* at 11 (citing Ex. 1001, 5:51–6:8).

We are not persuaded at this stage of the proceeding that Patent Owner’s construction is warranted. As an initial matter, we note that claim 1 (the only other independent claim in the ’492 patent) also includes the claim limitation “a terminal T1 for providing a signal indicating a state of the programmable latch.” Ex. 1001, 8:41–42. Patent Owner’s proposed construction, however, is limited to a described embodiment of the programmable latch that does not have a diode, and claim 1 requires the presence of a diode. *See* Prelim. Resp. 12 (“Thus in order to practice the

embodiment (without a diode), and perform the claimed operation of ‘providing a signal indicating a state of the programmable latch’ the claim term ‘a terminal T1 for providing a signal indicating a state of the programmable latch’ must be construed to mean ‘a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”); *compare* Ex. 1001, 8:38–58 *with id.* at 10:3–27). Patent Owner does not address sufficiently why the claim term “a terminal T1 for providing a signal indicating a state of the programmable latch” should be construed differently in claims 1 and 14. *See Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003) (“[W]e presume, unless otherwise compelled, that the same claim term in the same or related patents carries the same construed meaning.”).

The section of the Specification on which Patent Owner relies discusses one of a number of described embodiments. *See, e.g.*, Ex. 1001, 4:39–7:39. With respect to that embodiment, the Specification teaches that “if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming.” *Id.* at 5:52–55. The Specification further teaches that

[a]s soon as the terminal OUT– is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards the final value), the terminal OUT is quickly returned to ground. If the power is turned off and on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.

Id. at 5:66–6:8. These disclosures indicate that, in some embodiments, the terminal OUT is at ground at power-up, and that this state can be achieved, for example, by the passage of time between programming and power up, or by turning the power off and on again. We are not inclined, on this record, to import into the claim a requirement that terminal T1 be at ground voltage where one does not currently exist. *See SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (“Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.”); *see also Phillips*, 415 F.3d at 1323 (“[A]lthough the specification often describes very specific embodiments of the invention, [the Federal Circuit has] repeatedly warned against confining the claims to those embodiments.”).

Accordingly, at this stage and on the present record, we are not persuaded by Patent Owner’s argument restricting the scope of “a terminal T1 or providing a signal indicating a state of the programmable latch” as it is used in claim 14 to “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch” as Patent Owner proposes. During trial, we invite the parties to present arguments and evidence, specifically addressing the Specification and prosecution history in detail, in support of, opposing, or modifying Patent Owner’s proposed construction of this term, although we do not adopt it for purposes of this Decision.

Figure 2 is a schematic drawing of a memory redundancy circuitry in accordance with the invention described in Fu. *Id.* at 3:10–11. Memory redundancy circuitry 2 comprises redundancy activation circuit 40 and programmable redundancy decoder logic 30, and “operates between two electric potentials, i.e., the high (V_{CC}) and low (GND) levels, together with its host main memory cell array of the entire memory device.” *Id.* at 3:46–51. Memory redundancy circuitry 2 accepts a plurality of address bit signals X_i ($i = 1, 2, \dots n$) generated by an input circuitry “as inputs for the plurality of decoder units 32 of the programmable redundancy decoder logic 30.” *Id.* at 3:51–56. Each decoder unit 32 “comprises a first switch element, which is an NMOS transistor TN_i , a second switch element, the PMOS transistor TP_i , and a fuse element F_i .” *Id.* at 3:64–66.

Figure 4 of Fu is reproduced below.

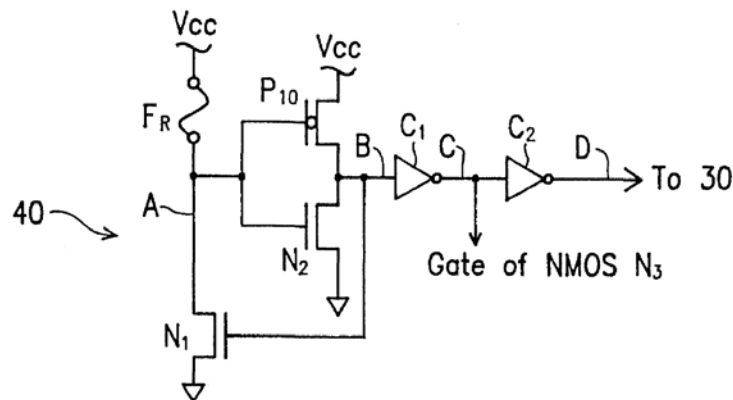


FIG. 4

Figure 4 is a schematic diagram of an embodiment of redundancy activation circuit 40 for memory redundancy circuitry 2. *Id.* at 4:14–17. Redundancy activation circuit 40 includes fuse element F_R , PMOS transistor P_{10} , two NMOS transistors N_1 and N_2 , and two inverters C_1 and C_2 . *Id.* at 4:17–19.

Fuse element F_R is connected in series with NMOS transistor N_1 , with the other end tied to V_{CC} and the transistor end tied to ground. *Id.* at 4:20–23.

Fu explains that when fuse element F_R is not blown, “the potential of node A is at its high level (V_{CC}) and the NMOS transistor N_2 is in a conduction mode to pull node B to the GND potential,” and “ N_1 is maintained to in non-conduction mode, helping to maintain the potential of node A at the high level.” *Id.* at 4:67–5:8. Fu further explains that when fuse element F_R is blown open, each of fuse elements F_i in decoder units 32 in programmable redundancy decoder logic 30 “that correspond to a defective memory cell in the main memory cell array are also blown.” *Id.* at 5:19–24. According to Fu, “[a]t this instant, node A is at a low electric potential, making the PMOS transistor P_{10} conduct,” which “brings node B to the high potential level” and “also make the NMOS transistor N_1 conducts, so that node A is ensured to be maintained at a low potential level.” *Id.* at 5:25–29.

2. *Analysis*

Petitioner asserts, with supporting testimony from Dr. Baker, that Fu discloses all of the elements of independent claim 14. Pet. 16–38. For example, Petitioner contends that Fu discloses “a first terminal for receiving a constant non-ground voltage throughout operation of the latch” (the terminal that receives V_{CC} , which is a constant non-ground voltage, when the circuit in Figure 4 of Fu operates), “a second terminal for receiving a voltage” (the terminal that receives GND, which corresponds to a low voltage, as shown in Figure 4 of Fu), and “a terminal T1 for providing a signal indicating a state of the programmable latch” (node A as shown in

Figure 4 of Fu that indicates the state of the fuse, which corresponds to the state of the programmable latch.). *Id.* at 22–27.

Patent Owner responds that “Fu does not teach any mechanism for dissipating voltage from its internal nodes, and further does not teach any operation of the latch,” and “[t]here is therefore no teaching that any voltage buildup at the internal nodes is dissipated before operation.” Prelim.

Resp. 13 (citing Ex. 2001 ¶¶ 36–37). For the reasons set forth in Section II.B, *supra*, we are not persuaded by Patent Owner’s argument that “a terminal T1 or providing a signal indicating a state of the programmable latch” as it is used in claim 14 means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” Patent Owner does not make any other arguments with respect to the limitations of the challenged claims.

We are persuaded, on this record, that Petitioner’s discussions of the particular structures in Fu, and the explanations in the Petition and Baker Declaration, are sufficient to establish a reasonable likelihood that independent claim 14 is unpatentable as anticipated by Fu. We have also considered the arguments and evidence with respect to claims 15–19 that directly depend from claim 14, and are likewise persuaded, on the current record, that Petitioner has demonstrated a reasonable likelihood that it would prevail as to those claims as well.

D. Anticipation by McAdams

Petitioner contends that claims 14–19 are unpatentable under 35 U.S.C. § 102(b) as anticipated by McAdams. Pet. 45–71. Petitioner relies on the Baker Declaration in support of its contentions. *Id.*

1. *Overview of McAdams*

McAdams “relates to semiconductor integrated circuit devices, and more particularly to fuse circuits of the type used in VLSI CMOS semiconductor memory devices or the like.” Ex. 1006, 1:5–8. According to McAdams, the principal object of the invention is “to provide improved fuse circuits exhibiting a low current drain for use in semiconductor integrated circuits such as memory for microcomputer devices, particularly CMOS devices with low standby power dissipation and minimum complexity.” *Id.* at 1:33–38.

Figure 1 of McAdams is reproduced below.

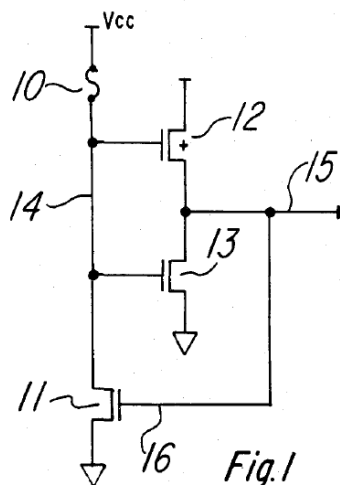


Figure 1 is an electrical circuit diagram of a CMOS fuse circuit according to one embodiment described in McAdams. *Id.* at 1:60–61. Fuse element 10 is connected in series with N-channel feedback transistor 11, and this series circuit is connected between supply voltage V_{cc} and V_{ss} . *Id.* at 1:67–2:3. A CMOS inverter including P-channel transistor 12 and N-channel transistor 13 has node 14 as an input and produces output 15. *Id.* at 2:3–6. “Feedback

is provided from the output node 15 to the gate of transistor 11 by a line 16.”
Id. at 2:6–7.

McAdams explains that, as V_{cc} goes from zero to +5 volts during power-up, if the fuse has not been blown “node 14 follows V_{cc} since the node 15 starts at V_{ss} potential and the transistor 11 is off.” *Id.* at 2:8–11. Because node 14 follows V_{cc} , P-channel transistor 12 stays off, and as soon as V_{cc} and node 14 reach the N-channel threshold voltage V_{tn} , transistor 13 turns on, holding node 15 at V_{ss} . *Id.* at 2:11–15. McAdams teaches that “[t]his quickly discharges to zero and capacitive coupling of voltage to the output node 15 at power-on due to the V_{cc} transition,” and, “[t]hus the only current flowing through the fuse 10 from the V_{cc} supply is leakage current, on the order of nanoamps.” *Id.* at 2:15–20. McAdams further explains that, when fuse 10 has been blown, node 14 is at V_{ss} and P-channel transistor 12 turns on as soon as its threshold V_{tp} is reached, causing output node 15 to follow V_{cc} . *Id.* at 2:21–24. “Once the node 15 reaches the threshold V_{tn} , the transistor 11 turns on, keeping the node 14 at V_{ss} ,” and “[a]ny capacitive coupling of voltage to node 14 from the V_{cc} transition is quickly discharged.” *Id.* at 2:24–28.

2. *Analysis*

Petitioner asserts, with supporting testimony from Dr. Baker, that McAdams discloses all of the elements of independent claim 14. Pet. 45–65. For example, Petitioner contends McAdams discloses “a first terminal for receiving a constant non-ground voltage throughout operation of the latch” (terminal V_{cc} , where V_{cc} is a supply voltage that is applied when power is applied to the circuit depicted in Figure 1 of McAdams), “a second terminal for receiving a voltage” (terminal for receiving V_{ss} as shown in Figure 1 of

McAdams), and “a terminal T1 for providing a signal indicating a state of the programmable latch” (node 14 in Figure 1 of McAdams that indicates the state of the fuse, which corresponds to the state of the programmable latch). *Id.* at 49–56.

Patent Owner argues that McAdams does not disclose “a terminal T1 for providing a signal indicating a state of the programmable latch” because the “McAdams circuit does not inherently dissipate voltage that accumulates on nodes 14 and 15.” Prelim. Resp. 13 (citing Ex. 2001 ¶ 13). According to Patent Owner, “absent any teaching from that the latch is programmed and left unpowered before being read,” “capacitive coupling downstream from” the circuit in McAdams “allows the floating node 15 to stray far from its initialization state.” *Id.* at 13–14. For the reasons set forth in Section II.B, *supra*, we are not persuaded by Patent Owner’s argument that “a terminal T1 or providing a signal indicating a state of the programmable latch” as it is used in claim 14 means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” Patent Owner does not make any other arguments with respect to the limitations of the challenged claims.

We are persuaded, on this record, that Petitioner’s discussions of the particular structures in McAdams, and the explanations in the Petition and Baker Declaration, are sufficient to establish a reasonable likelihood that independent claim 14 is unpatentable as anticipated by McAdams. We have also considered the arguments and evidence with respect to claims 15–19 that directly depend from claim 14, and are likewise persuaded, on the current record, that Petitioner has demonstrated a reasonable likelihood that it would prevail as to those claims as well.

E. Obviousness Grounds

Petitioner contends the combined teachings of Fu and Sugibayashi, and the combined teachings of McAdams and Sugibayashi, teach or suggest each limitation of claims 14–19. Pet. 71–87. Specifically, Petitioner contends that “to the extent that Patent Owner argues or the Board finds the voltage on the Vcc terminal” in Fu or McAdams is not “a constant non-ground voltage throughout the operation of the latch” as required by claim 14, “it would have been obvious in view of Sugibayashi to provide the supply voltage Vcc in a manner that ensures it is constant throughout the operation of the memory in which the latch is included.” *Id.* at 72 (citing Ex. 1002 ¶¶ 141–161), 83 (citing Ex. 1002 ¶¶ 163–174).

Having found that Petitioner has established a reasonable likelihood of prevailing with respect to its contentions that claims 14–19 of the ’492 patent are anticipated by Fu and McAdams, we also institute review with respect the obviousness grounds that include Sugibayashi as well. *See* United States Patent and Trademark Office, *Guidance on the Impact of SAS on AIA Trial Proceedings*, Patent Trial and Appeal Board (April 26, 2018).

III. CONCLUSION

Based on the arguments in the Petition and Preliminary Response, and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail on its challenge to at least one claim of the ’492 patent.

Although we exercise our discretion and institute review, we remind the parties that we have not yet made a final determination as to the patentability of any of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 14–19 of the '492 patent with respect to the grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this Decision.

IPR2019-00779
Patent 6,163,492

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