

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,163,492

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,163,492**

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 6,163,492 (“the ’492 patent”) (Ex. 1001).¹

2. I am being compensated at a rate of \$615/hour for my work in this proceeding.

3. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

4. I have been asked to consider whether certain references disclose or suggest the features recited in claims 1-13 of the ’492 patent. My opinions are set forth below.

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’492 patent.

II. BACKGROUND AND QUALIFICATIONS

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding circuit design and memory devices referenced in this declaration.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

8. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

9. As described in my CV, I am a licensed Professional Engineer in the state of Idaho and have more than 30 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of flash memory while at Micron. My efforts resulted in more than a dozen flash memory-related patents. Among other experiences, I led development of the delay-locked loop (DLL) in the late 90's so that Micron products could transition to the DDR memory standard. I have worked as a consultant at other companies designing memory chips, including Sun, Oracle, and Contour Semiconductor. I also worked on the design of CISs and memory as a consultant for OmniVision.

10. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, and fiber optics. As a professor, I have been the main advisor to over 85 Master's and Doctoral students.

11. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on 149 granted U.S. patents in integrated circuit designs including flash memory and DRAM.

12. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

13. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

14. I have received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award the four years I have been at UNLV.

15. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

16. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding circuits, including fuse-based circuits used in memory devices.

17. In forming my opinions expressed in this Declaration, I reviewed the '492 patent (Ex. 1001), the prosecution file history for the '492 patent (Ex. 1004); U.S. Patent No. 4,621,346 ("McAdams") (Ex. 1006); U.S. Patent No. 5,519,658 ("Uda") (Ex. 1007); U.S. Patent No. 5,552,739 ("Keeth") (Ex. 1008); Weste *et al.*, Principles of CMOS VLSI Design: A Systems Perspective, 2d. ed. 1993 ("Weste") (Ex. 1009); U.S. Patent No. 5,592,121 ("Jung") (Ex. 1012); U.S. Patent No. 5,604,710 ("Tomishima") (Ex. 1013); Taur *et al.*, Fundamentals of Modern VLSI Devices, 2009 ("Taur") (Ex. 1015); and any other materials I refer to in this Declaration in support of my opinions.

18. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions

have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '492 patent at the time of the alleged invention, which I have been asked to initially consider was the mid-to-late 1990s (including October 23, 1998, the filing date of U.S. Application No. 09/178,445 ("the '445 application")) that matured into the '492 patent). My opinions reflect how one of ordinary skill in the art would have understood the '492 patent, the prior art to the '492 patent, and the state of the art at the time of the alleged invention.

19. Based on my experience and expertise, it is my opinion that certain references disclose or suggest all the features recited in claims 1-13 ("challenged claims") of the '492 patent, as I discuss in detail below.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '492 patent as of what I understand is the filing date of October 23, 1998 for the '445 application. Specifically, based on my review of the '492 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in art

would have had would have had a B.S. degree in electrical engineering, or equivalent thereof, and at least two to three years of experience in integrated circuit design. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and become familiar with the prior and current solutions to those problems.

21. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe, i.e., mid-to-late 1990s, including the time preceding the '445 application filing date of October 23, 1998.

V. TECHNICAL BACKGROUND

22. In this section, I present a brief overview of basic circuit concepts that will assist in better understanding the '492 patent and the prior art that I discuss in this declaration. In particular, I cover below the operation of a metal-oxide semiconductor field-effect transistor (MOSFET or MOS transistor), which is the building block of the circuits described in the '492 patent and the prior art. I also briefly discuss the basic structure and operation of a diode.

A. MOSFET

23. A metal oxide semiconductor field effect transistor (MOSFET) was a well-known building block of circuits in various applications long before the alleged time of the invention. In fact, MOSFETs have been known since at least as early as 1960, *i.e.*, decades before the alleged invention of the '492 patent. As an example, a book by Taur entitled Fundamentals of Modern VLSI Devices ("Taur") explains some of the known characteristics of MOSFETs. (*See, e.g.*, Ex. 1015 at 2.)²

24. The MOSFET was known to be a four-terminal device with the terminals designated as gate, source, drain, and substrate (substrate is sometimes referred to as a body). The substrate was typically a silicon substrate. Although pure silicon is a poor conductor, the electrical conductivity of silicon was known to

² My understanding of such background MOSFET technologies is based on my experience and knowledge, and my reference to Taur is only for exemplary purposes. Taur was published in 2009, and based on my experience and knowledge, the disclosure of MOSFET technologies in Taur that I refer to in this declaration is consistent with what one of ordinary skill in the art would have understood regarding such technologies in the mid-to-late 1990s.

be increased by introducing impurity atoms, or dopants, into the silicon. Silicon material doped with p-type dopants is called p-type silicon, and silicon material doped with n-type dopants is called n-type silicon. Taur provides an example of the basic structure of a MOSFET in figure. 3.1, where the basic structure includes a p-type silicon substrate and n-type source and drain regions that are each heavily doped compared to the substrate.

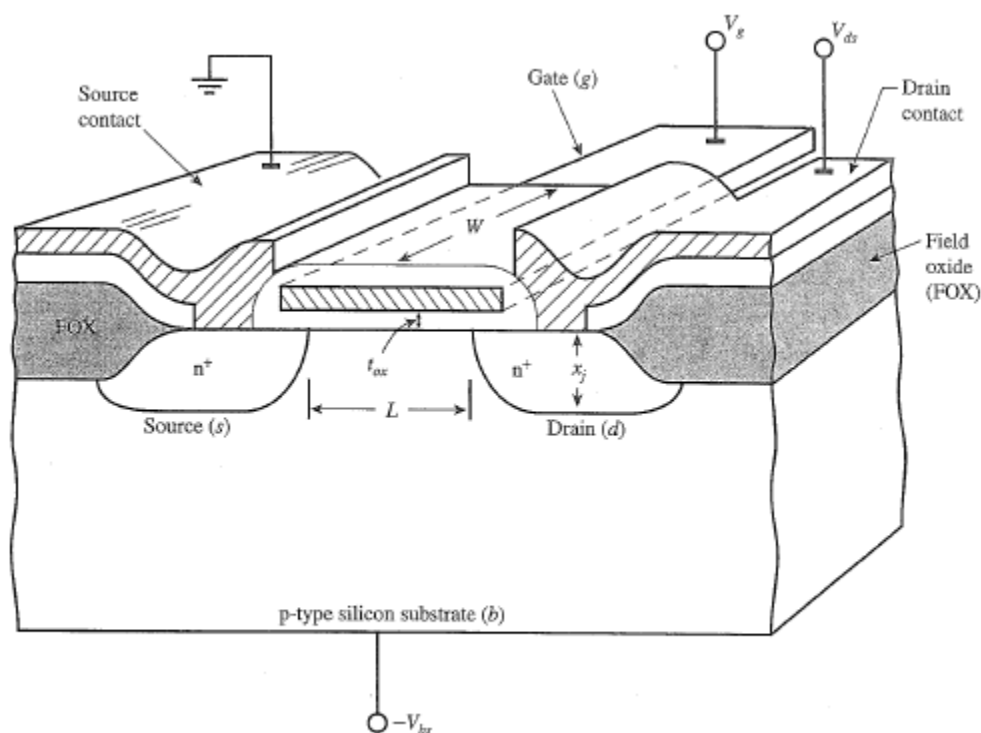


FIGURE 3.1. Three-dimensional view of basic MOSFET device structure. (After Arora, 1993.)

(*Id.* at 149, FIG. 3.1) The configuration shown in Figure 3.1 of Taur was consistent with the basic structure of such a configured MOSFET that one skilled

in the art would have understood during the 1990s. (*See, e.g.*, reference to Arora 1993 below the figure).

25. In configurations where the source and drain regions are heavily n-doped, similar to the configuration shown in figure 3.1 above, the MOSFET was typically known as an n-channel MOSFET (or NMOSFET, NMOS transistor, or simply NMOS). Another type of MOSFET was known as a p-channel MOSFET (or PMOSFET, PMOS transistor, or simply PMOS), in which the dopant types are reversed compared to those of an n-channel MOSFET as I described above (and exemplary shown in figure 3.1.) (*See also id.* at 148.)

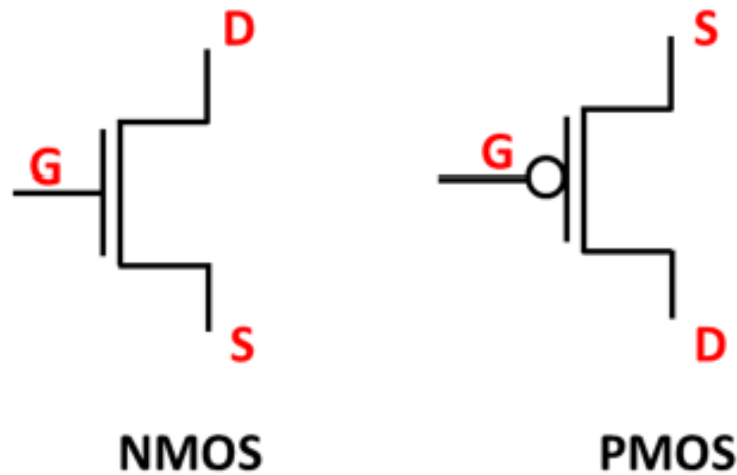
B. MOSFET as a Switch

26. In a simplified configuration of a MOSFET in the mid-to-late 1990s (and still today), there was no current flow between the source and drain unless the voltage difference between gate and source terminals exceeds a threshold voltage. When a sufficiently large voltage (typically called the threshold voltage of the transistor or V_T) is applied between the gate and the source, the silicon surface between the source and drain is inverted to n-type, which forms a conductive n-channel between the source and drain. (*Id.*) Where a voltage difference existed between the source and drain, current would then flow between those terminals. In such circumstances, it was known that the MOSFET would operate like a switch

and would conduct current depending on the $|V_{GS}|$ (magnitude of voltage between gate and source terminals).³ (*Id.*) For a PMOS, the current flows from source to drain when the gate voltage is below the source voltage by the threshold voltage. On the contrary, for an NMOS, the current flows from drain to source when the gate voltage is greater than the source voltage by the threshold voltage.

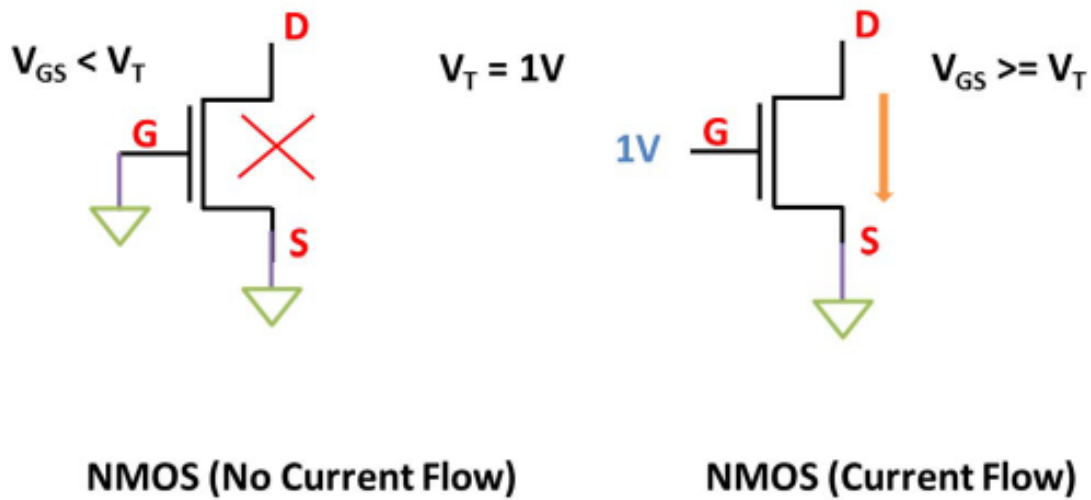
27. The following demonstratives illustrate the above basic concepts that were known to those skilled in the art in the 1998 timeframe. Demonstrative A illustrates the symbols that were commonly attributed to an NMOS and a PMOS in circuit designs at that time. The gate, drain, and source are respectively labeled G, D, and S in these demonstratives.

³ The MOSFET was also known to operate in what was known as the “subthreshold” region, where a very small amount of current is conducted by the MOSFET because the gate-source voltage is lower than the threshold voltage. As a result, where the applied voltages result in the gate-source voltage being higher than the threshold voltage, the “sub-threshold” mode is not implicated in the operation of the MOSFET at that state.



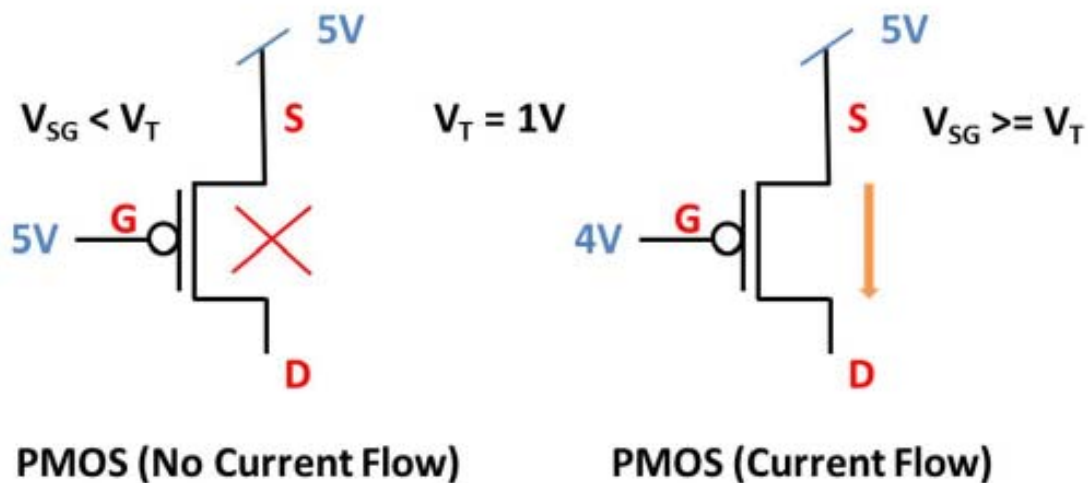
DEMONSTRATIVE A

28. Demonstrative B illustrates an NMOS with a threshold voltage of 1V and describes that when the gate to source voltage (V_{GS}) is less than 1V (*e.g.*, both gate and source are at ground (shown by the green triangles), no current flows through the NMOS (represented by the red “X”), but when the gate to source voltage is greater than or equal to the threshold voltage, current flows from drain to source (shown by the orange arrow).



DEMONSTRATIVE B

29. Demonstrative C similarly illustrates the operation of a PMOS with the difference being that for the PMOS, the gate voltage has to be lower than the source voltage for the PMOS to conduct current. That is, instead of V_{GS} being greater than or equal to V_T , the V_{SG} must be greater than or equal to V_T .



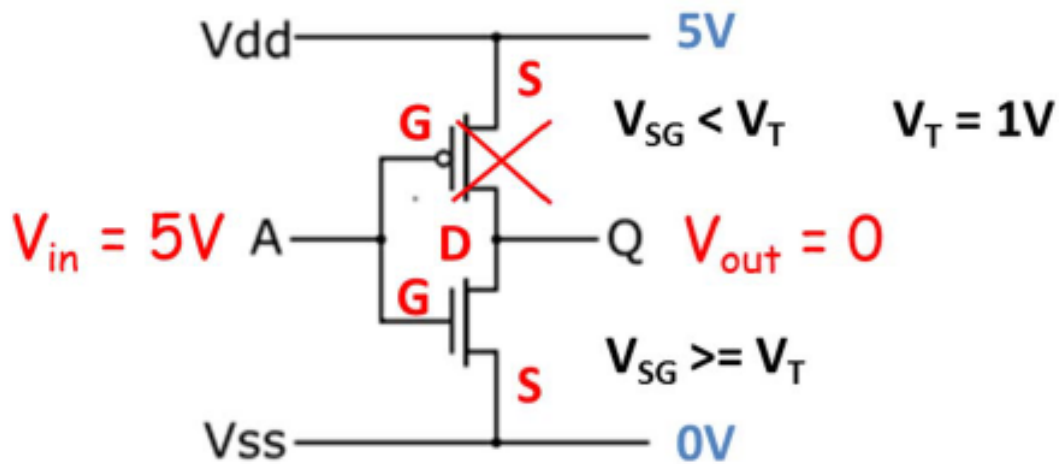
DEMONSTRATIVE C

30. A simple circuit example of an inverter brings together the above basic MOSFET concepts in a scenario using digital logic. It was well known long before the time of the alleged invention to use digital logic in various data processing contexts. For example, it was well known to represent data using two logic values—a logic HIGH (commonly designated ‘1’), and a logic LOW (commonly designated ‘0’). The two logic values HIGH (‘1’) and LOW (‘0’) were called logical complements of each other. A horizontal bar over a digital signal’s name was a common way to designate a logical complement, e.g., \bar{X} would have been the logical complement of X. In the context of circuits, it was known to interpret a relatively low voltage (e.g., 0V) as a logic LOW, and to interpret a relatively high voltage (e.g., 5V) as a logic HIGH.

31. Various circuit devices were known for manipulating digital logic signals. For example, it was well known to use complementary metal oxide semiconductor (CMOS) technology for implementing logic gates that would manipulate such digital logic signals. The simplest example was an inverter, which performed the logic operation of inverting a logic value from LOW to HIGH (i.e., generate a ‘1’ at the output of the inverter when the input to the inverter is ‘0’) and from HIGH to LOW (i.e., generate a ‘0’ at the output of the inverter when

the input to the inverter is '1'). In other words, the output of the inverter had a logic value that was the logical complement of the input of the inverter.

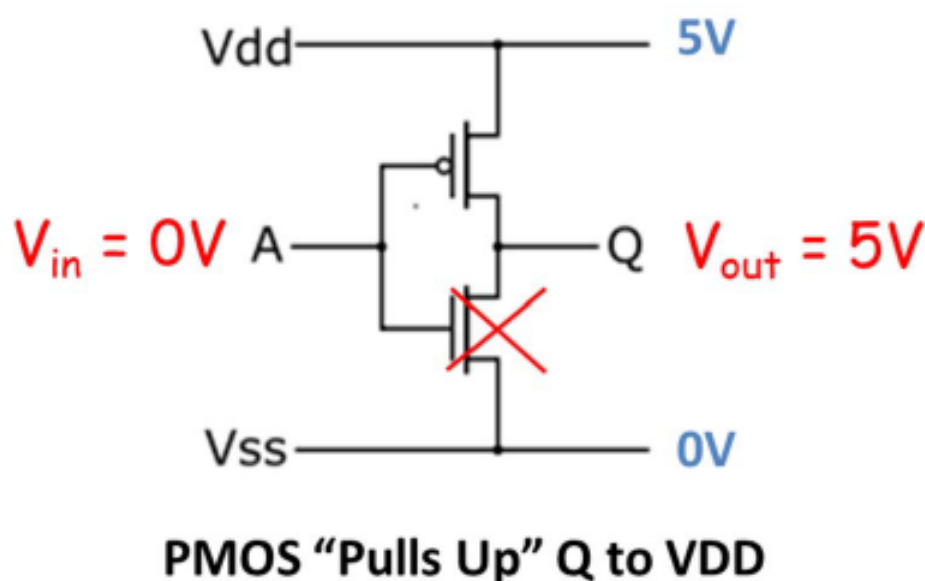
32. As shown below in demonstrative D, an inverter consists of a PMOS and NMOS in series with shared drain terminals. This configuration is consistent with what was known to one of ordinary skill in the art at the time of the alleged invention for the '492 patent. The source of the PMOS is at 5V (High) in this example and the source of the NMOS is at 0V (Low). It is assumed that the threshold voltage for both transistors is 1V. When an input voltage (V_{IN}) of 5V is provided to the gates of both the PMOS and the NMOS, the V_{SG} of the PMOS is 0V (less than V_T) and the V_{GS} of the NMOS is 5V (greater than V_T). Accordingly, the PMOS is turned OFF and the NMOS is turned ON. Because there is no current flowing through the PMOS, the NMOS will "pull down" the voltage at its drain terminal causing an output voltage (V_{OUT}) of 0V, and the NMOS in this configuration was referred to as a "pull-down transistor."



NMOS “Pulls Down” Q to VSS

DEMONSTRATIVE D

33. If, however, in the same example the input voltage is at 0V, the PMOS will turn ON, the NMOS will shut off, and, as a result, the PMOS will “pull up” the voltage at its drain to 5V causing an output voltage of the inverter circuit of 5V. The PMOS in this configuration was referred to as a “pull-up transistor.”



DEMONSTRATIVE E

34. I refer to these basic concepts of “pull up” and “pull down” when I explain the prior art below (*see* below at Sections VIII, IX).

35. The current-conducting capability of the MOSFET was known at that time to depend on the dimensions of the transistor, *i.e.*, width (W) and length (L). (*See also* Ex. 1015 at FIG. 3.1). It was known that when the MOSFET operates in the above-threshold region (*i.e.*, $|V_{GS}|^4$ is greater than the threshold voltage), for a

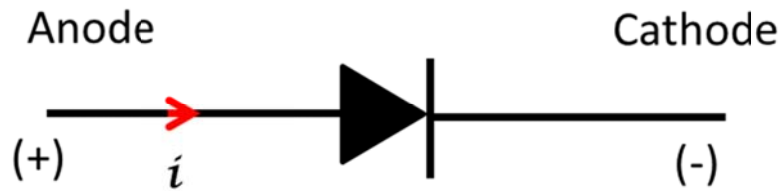
⁴ I use the absolute value sign with V_{GS} (*i.e.*, gate-to-source voltage) because for a PMOS, the V_{SG} (*i.e.*, source-to-gate voltage) has to be greater than threshold for the PMOS to conduct current.

given V_{DS} , the MOSFET current (i.e., the drain-source current or the source-drain current) is proportional to $|V_{GS}|$, i.e., a higher $|V_{GS}|$ results in a higher current through the MOSFET.

C. Basic Operating Principles of a Diode

36. Below, I explain some of the basic operating principles of a diode that were known to those skilled in the art in the 1998 timeframe.

37. A diode was a well-known two-terminal semiconductor device that, in normal operating conditions, conducts current in one direction, but not the other. As an example, Taur explains some of the known characteristics of diodes. (*See, e.g., id.* at 38-39 (Section 2.2.1.1, reference to Shockley of 1950).) A diode can be created by forming a junction between metal and a semiconductor or between two different types (e.g., p-type and n-type) of semiconductor materials. For example, a p-n junction diode can be created by forming a junction between a region of a semiconductor substrate that is doped with n-type dopants (excess negative charge carriers) and another region that is doped with p-type dopants (excess positive charge carriers). (*See, e.g., id.* at 35 (Section 2.2 (discussions on p-n junctions).) Demonstrative F illustrates the schematic symbol that was commonly attributed to a diode in the circuit designs at the relevant time.



DEMONSTRATIVE F

38. The terminals of a diode are called the anode (p-type side) and the cathode (n-type side). The red arrow points in the direction where current flow occurs when the diode is forward biased. The diode is forward biased when the voltage applied to the anode is greater than the voltage applied to the cathode by at least the threshold voltage of the diode, which is typically around 0.65 volt for a p-n junction diode formed using silicon. On the other hand, when a diode is reversed biased, there is negligible current flow through the diode.⁵ As such, under normal operation conditions, a diode only allows a current to flow through it in a *single direction*, from the anode to the cathode, as indicated by the red arrow in the above demonstrative when it is forward biased. As shown in the figure below, current

⁵ If a high reverse-bias voltage is applied across the diode, a condition referred to “reverse breakdown” can occur where current flows from the cathode to the anode. However, such a breakdown voltage would have been understood to be outside the normal operating conditions for the diode.

starts to flow across the diode after the applied bias across the junction reaches about 0.65 volt.

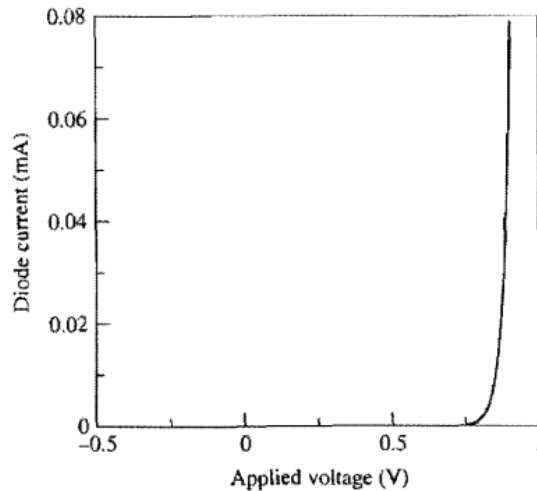


Figure 2.14. A schematic linear plot of the current of a typical silicon diode as a function of its applied voltage. On a linear plot, the reverse current is too low to be observable.

(*Id.* at 41, FIG. 2.14)

39. It was well known before the time of the alleged invention to use a diode as a voltage rectifier to manipulate digital logic signals. For example, it was well known to use a p-n diode (for its highly directional nature that allows a current to pass in only one direction) to convert a sinusoidal input signal (with both positive and negative components, i.e., current flowing in two directions) to an output voltage which is purely positive (i.e., current flowing only in one direction).

VI. OVERVIEW OF THE '492 PATENT

40. The '492 patent is entitled "Programmable Latches that Include Non-volatile Programmable Elements." (Ex. 1001 at Cover.) Consistent with the title,

the '492 patent relates to “programmable latches that include non-volatile programmable elements” where “[e]xamples of non-volatile programmable elements are fuses.” (*Id.* at 1:15-17.)

41. As disclosed by the '492 patent, such programmable latches “are used in integrated circuits to enable modification of the circuits without changing the masks used for circuit fabrication.” (*Id.* at 1:18-20.) For example, the '492 patent discloses that such programmable latches can be used for replacing defective memory cells with spare memory cells in semiconductor memories. (*Id.* at 1:20-22.) The '492 patent acknowledges that programmable latches using non-volatile programmable elements such as fuses were known in the art before the alleged invention disclosed in the '492 patent. (*Id.* at 1:24-54.)

42. Figure 1 of the '492 patent, replicated below, illustrates one prior art programmable latch that includes a “[f]use F1 connected between the power supply VDD and the latch output terminal OUT.” (*Id.* at 1:24-27.)

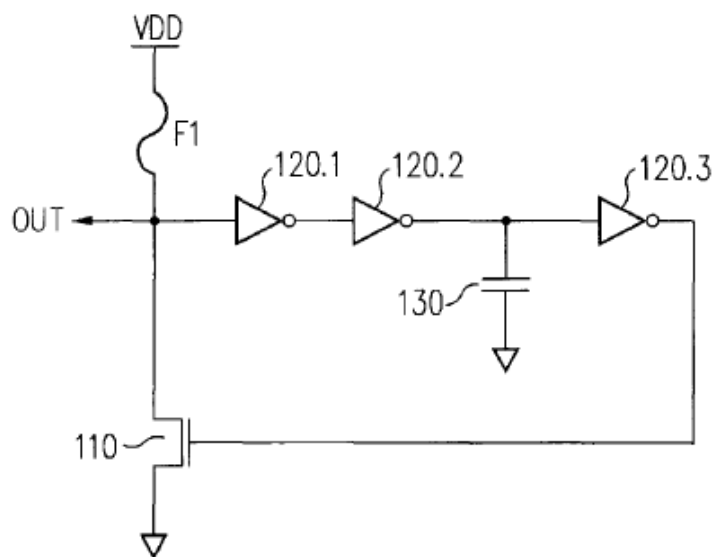


FIG. 1
(PRIOR ART)

(*Id.* at FIG. 1.)

43. The '492 patent describes the operation of the prior art latch circuit of figure 1 as follows:

If fuse F1 is intact, the terminal OUT is pulled to VDD. The inverters 120 keep transistor 110 off. If fuse F1 is blown, the terminal OUT is at the ground voltage. The inverters turn transistor 110 on to keep the terminal OUT at ground.

(*Id.* at 1:32-35.)

44. The '492 patent discloses that the capacitor 130 is included in the circuit of figure 1 above to ensure proper initialization when power is supplied to the circuit. (*Id.* at 1:36-54 (reproduced below).) Specifically, the '492 patent, referring to the disclosure in U.S. Patent No. 4,546,455, indicates that a

malfunction can occur on power up when the fuse is blown. Specifically, when power is off, transistor 110 is off and the node OUT is floating. (*Id.* at 1:38-40.) A person of ordinary skill in the art would have understood that a “floating” node is a node that is not being pulled to any particular voltage such as ground and that an indeterminate voltage can exist on that node. Because the node OUT is floating, there is a concern that OUT can inadvertently be raised to a logic “1” (High) by capacitive coupling or otherwise. (*Id.* at 1:40-44.) The ’492 patent discloses:

Bypass capacitor 130 is connected between the input of inverter 120.3 and the ground terminal to insure correct initialization of the latch on power-up. More particularly, when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating. According to U.S. Pat. No. 4,546,455, the terminal OUT may "tend to have its potential raised to a logic level '1'". In addition, the terminal OUT potential may become "unstable due to the capacitive coupling" in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown. As a result, the terminal OUT would provide an erroneous voltage.

Capacitor 130 is intended to avoid such malfunction. During power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown.

Then the ground voltage on terminal OUT propagates through the three inverters to keep transistor 110 on.

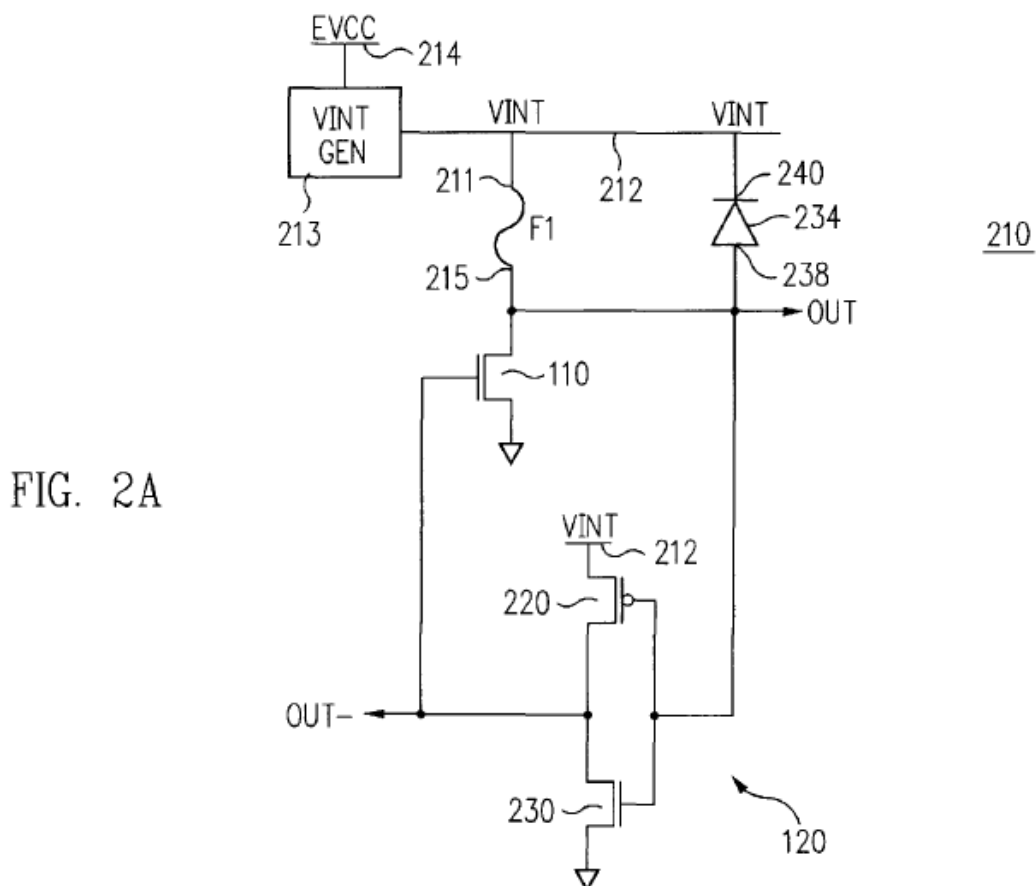
(*Id.* at 1:36-54.)

45. If the fuse F1 is blown, when power is applied to the latch, if the OUT node, which has been floating while the power is off, is at a logic “1” due to charge accumulated on that node, the charge on OUT corresponding to the logic “1” (high) can keep the transistor 110 off. If transistor 110 is kept off, it prevents the charge on OUT from being drained away. (*Id.* at 1:44-46.) Therefore, even if the fuse has been blown, the output of the programmable latch, which should be logic “0” (low), may remain high. (*Id.* at 1:46-47.) According to the ’992 patent, “[c]apacitor 130 is intended to avoid such malfunction” and “keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown” such that OUT properly reflects the state of the fuse F1. (*Id.* at 1:48-54.) According to the ’992 patent:

Prior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals.

(*Id.* at 2:22-26.)

46. The '492 patent proposes an alternative programmable latch shown in figure 2A below. (*Id.* at 3:10-11.)



(*Id.* at FIG. 2A.)

47. The programmable latch shown in figure 2A above includes a fuse 211, an inverter 120 that includes transistors 220 and 230, and a transistor 110. (*Id.* at 3:10-33, FIG. 2A.) The programmable latch of figure 2A also includes a diode 234. (*Id.* at 3:33-35, “Diode 234 has its anode terminal 238 connected to terminal OUT and its cathode terminal 240 connected to the VINT terminal 212.”)

As disclosed by the '492 patent, the diode 234 holds the OUT node at a voltage not higher than a threshold voltage of the diode 234 when the VINT terminal is ground. (*Id.* at 3:35-41, “When the power is off, the VINT terminal is at ground. . . . Therefore, the voltage on the terminal OUT is not higher than one threshold voltage of the diode 234.”)

48. The '492 patent indicates that by maintaining the voltage on OUT low using the diode 234, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on and “connects the terminal OUT to ground,” resulting in a correct output. (*Id.* at 3:41-49.) This happens because terminal OUT is held “no higher than one threshold voltage of diode 234,” and at such a voltage, transistor 230 does not turn on because its threshold voltage (e.g., 1.2V) is greater than the threshold voltage of diode 234. (*Id.*) Per the '492 patent, the latch can operate correctly even if the diode is omitted. (*Id.* at 5:51-6:7.)

49. The above features were well known as I discussed below at Sections VIII and IX.

VII. CLAIM CONSTRUCTION

50. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is mid-to-late

1990s (including October 23, 1998, the filing date of the U.S. Application maturing into the '492 patent). In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

VIII. OVERVIEW OF THE PRIOR ART

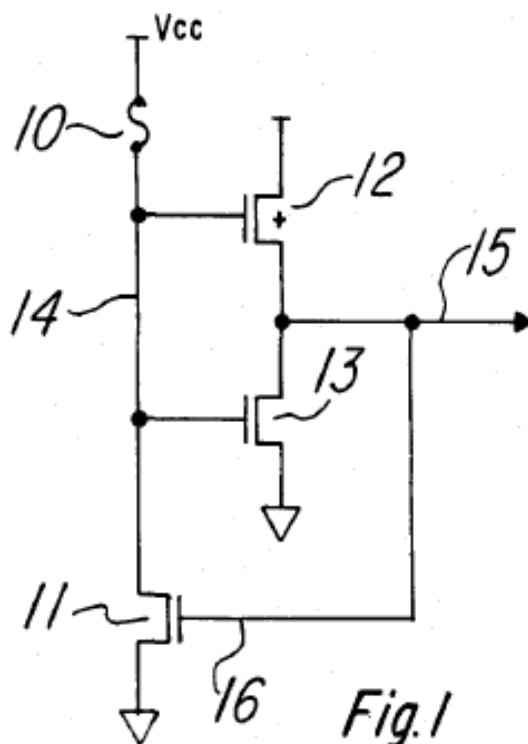
A. McAdams

51. McAdams relates to a “fuse circuit as used in self-repairing memory devices.” (Ex. 1006 at Abstract.) McAdams describes the operation of the fuse circuit as follows:

In self-repairing semiconductor memory device, fuses are used to store the addresses of faulty locations, so redundant cells can be substituted. Or, the fuse may be used to generate an enabling signal. These fuses are usually polysilicon conductor strips that are selectively blown by an indexed laser beam.

(*Id.* at 1:9-14.)

52. McAdams discloses operation of a particular fuse circuit in connection with figure 1. (*Id.* at FIG. 1.)



(*Id.* at FIG. 1.)

53. The fuse circuit shown in figure 1 of McAdams includes “[a] fuse element 10,” “an N-channel feedback transistor 11,” and “[a] CMOS inverter [that] include[s] a P-channel transistor 12 and an N-channel transistor 13.” (*Id.* at 1:67-2:6.) The fuse circuit of figure 1 “produces an output 15” and “[f]eedback is provided from the output node 15 to the gate of the transistor 11.” (*Id.* at 2:3-7.)

54. McAdams discloses how the fuse circuit operates when power-up occurs and Vcc goes from zero to +5v. (*Id.* at 2:8-26.) For example, when power is applied, “if the fuse has not been blown, the node 14 follows Vcc” (*id.* at 2:8-10), which, as a person of ordinary skill in the art would have understood, results

in the output node 15 of the inverter being pulled low to Vss. If the fuse has been blown, node 14 is at Vss when power is applied, and transistor 12 turns on, causing the output node 15 to follow Vcc and be pulled high. (*Id.* at 2:21-24; *see* my analysis above in Section V.B.) As the output node 15 goes high, transistor 11 turns on, thereby keeping the node 14 at Vss. (*Id.* at 2:24-26.)

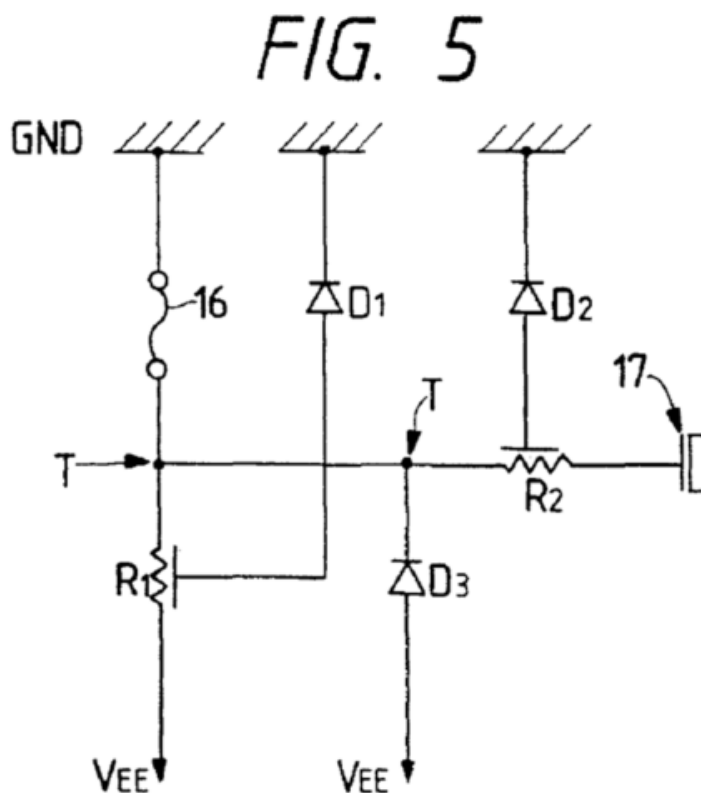
B. Uda

55. Uda also relates to semiconductor integrated circuit devices, including redundancy circuits for memory devices that use fuses to enable such redundancy circuits. (Ex. 1007 at 1:10-17, 3:15-19, 3:32-37, FIG. 5.) Uda discloses:

It is another object of the invention to provide a technology that prevents any degradation in the reliability of semiconductor integrated circuit devices, the degradation being otherwise caused by the melting of fuses constituting part of a redundancy circuit arrangement in the devices.

(*Id.* at 3:15-19.)

56. Uda discloses a fuse circuit that includes diodes to prevent damage to a transistor, where figure 5 depicts how the fuse arrangement is connected in one embodiment.



(*Id.* at FIG. 5.)

57. Uda discloses that the fuses are used to switch between faulty and backup elements on the chip, where the “[t]he fuses are melted, illustratively, by use of a laser means or electrical means.” (*Id.* at 1:38-42.)

58. According to Uda, “[t]he purpose of furnishing diodes D1 through D3 and the resistor R2 is to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the NMOS gate.” (*Id.* at 9:44-47.) For example, the diodes D1 and D2 allow the excess charge to pass to the

ground line GND, which protects the gate electrode of the NMOS 17 from being damaged. (*Id.* at FIG. 5.) Specifically, Uda discloses:

The purpose of furnishing the diodes D_1 through D_3 and the resistor R_2 is to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the MOS gate. These components work as follows: If a positive charge develops, the charge is led to the ground line GND via the diodes D_1 and D_2 ; if a negative charge occurs, the charge is led to the power line V_{EE} via the diode D_3 . Any residual charge loses its energy when entering the resistor R_2 , whereby the MOS gate is protected from destruction.

(*Id.* at 9:44-53.)

C. Keeth

59. Keeth relates to a memory circuit that “includes a power supply for generating an internal operating voltage.” (Ex. 1008 at Abstract; *see also id.*, 1:11-60.) Keeth discloses that an integrated circuit (e.g., a DRAM) “conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts.” (Ex. 1008 at 1:17-19.) This externally applied voltage (V_{CCX}) is converted by a power supply circuit to “an internal voltage V_{CCR} ,” which is used as the power supply for the memory circuits. (*Id.* at 1:31-34; *see also id.*, Abstract (“internal operating

voltage, designated V_{CCR} ”), 6:19 (“Signal V_{CCR} . . . powers circuit 30,” where circuit 30 includes DRAM, SRAM, etc.) For example, Keeth discloses:

Circuit 30 is a circuit for performing an electrical function of IC 10. In various embodiments circuit 30 is an analog circuit, a digital circuit, or a combination of analog and digital circuitry. Although the present invention is effectively applied where circuit 30 includes dynamic memory (DRAM), a static memory (SRAM), or a video memory (VRAM) having a serial port, the present invention can be beneficially and equivalently applied by a person of ordinary skill to integrated circuits in general, whether or not the integrated circuit is powered from a single power supply potential.

(*Id.* at 4:12-22.)

60. According to Keeth, conventional power supply circuits for converting an external power supply voltage to an internal power supply voltage suffered from several problems. (*Id.* at 1:31-60.) To overcome these deficiencies, Keeth discloses a circuit (voltage reference 100) in FIG. 3 that receives power signal V_{CCX} and provides the internal power supply voltage V_{CCR} . (*See, e.g., id.* at 5:58-62, FIG. 3.)

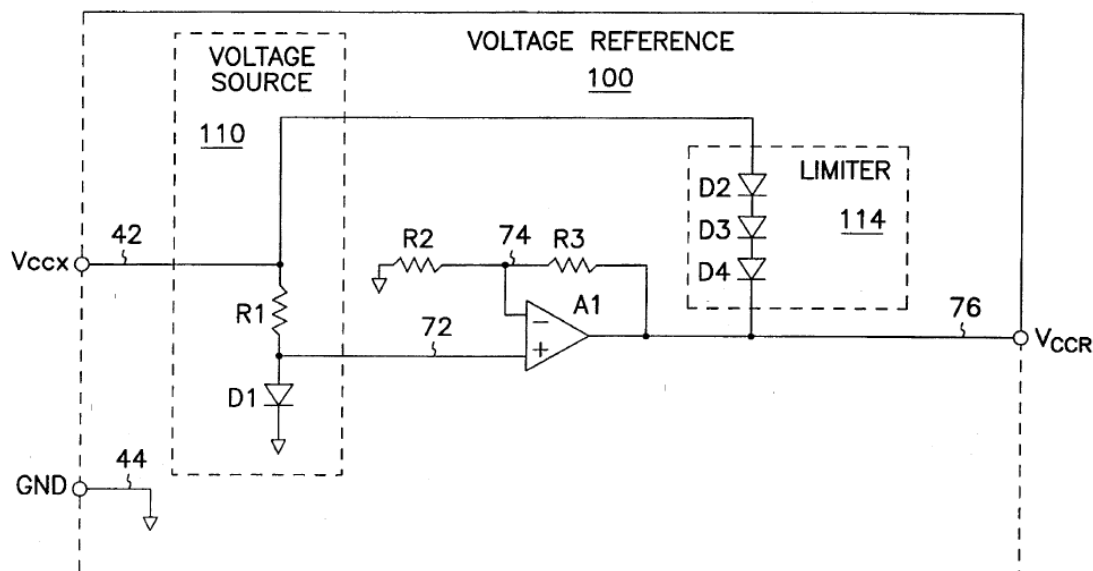


FIG. 3

(*Id.* at FIG. 3.)

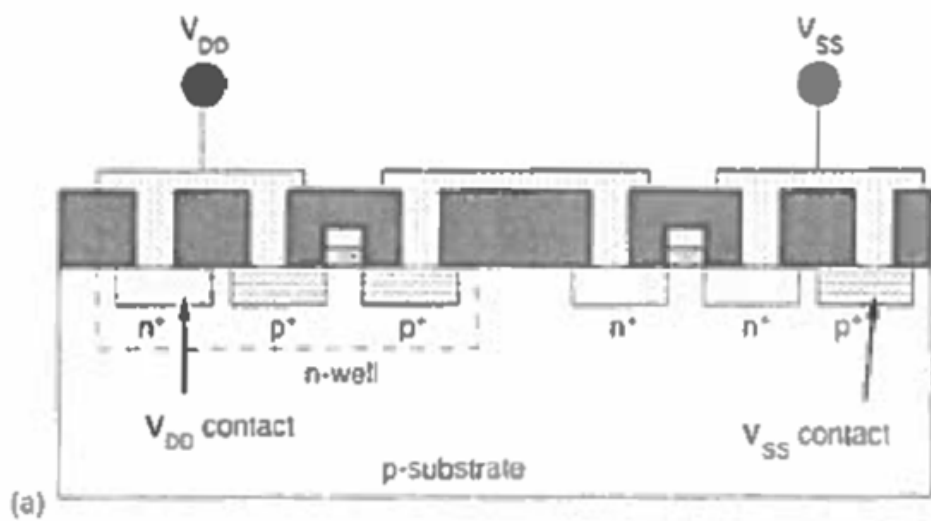
61. Keeth discloses that the voltage reference 100 shown in figure 3 above achieves a “piecewise linear relationship between V_{CCX} and V_{CCR} ” that alleviates shortcomings of similar prior art circuits. (*Id.* at 4:37-5:62.) For example, the voltage reference 100 operates over three ranges of input values for V_{CCX} . According to Keeth, “operation in the first segment provides data retention at low power consumption,” “[o]peration in the second segment supports speed grading individual devices with a margin for properly stating memory performance specifications,” and “[o]peration in the third segment supports screening at

elevated temperatures for identifying weak and defective memory devices.” (*Id.* at Abstract; *see also id.*, 4:37-5:62.)

D. Weste

62. Weste is a treatise in the field of semiconductor integrated circuit devices, specifically CMOS technology. (Ex. 1009 at 1, 379, 625.) Weste describes the operation and construction of semiconductor circuit elements that are used in McAdams, such as NMOS and PMOS transistors, diodes, latches, and fusible links. (*Id.* at 19-21, 41-51, 91-93, 117-130, 318-322, 395-400.) For example, Weste discloses how both NMOS and PMOS transistors are constructed on a semiconductor substrate.

63. For example, Weste discloses a conventional n-well CMOS process in which the NMOS transistors are built in the native p-substrate but a separate n-well is created inside the p-substrate to mimic the function of an n-substrate for the PMOS transistors. (*Id.* at 122-23.) Weste further discloses (*see id.*) that in such an n-well CMOS process, an inverter (which includes an NMOS transistor and a PMOS transistor sharing their drain terminals) would be constructed as shown below:

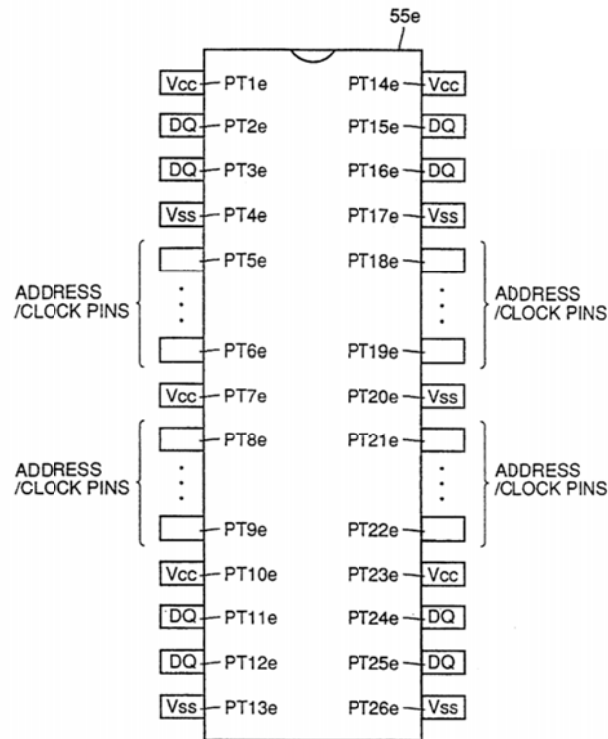


(*Id.* at 124 (FIG. 3.9).)

E. Tomishima

64. Tomishima relates to a memory circuit that has “an arrangement of power supply pads and data input/output pads in a semiconductor memory device.” (Ex. 1013 at 1:13-15; *see also id.*, Abstract.). Tomishima discloses that the power supply pin terminals receive V_{cc} and V_{ss} from a pin external to the memory device. For example, with respect to figure 23, Tomishima discloses that “power supply pin terminals and ground pin terminals are arranged on each respective side of package 55e.” (*Id.* at 24:32-40.)

FIG.23



(*Id.* at FIG. 23.)

IX. THE PRIOR ART DISCLOSES OR SUGGESTS ALL OF THE FEATURES OF CLAIMS 1-13 OF THE '492 PATENT

65. I have reviewed McAdams, Uda, Keeth, Weste, and Tomishima. As I describe below in Sections IX.A-E, in my opinion, these references, in various combinations, disclose or suggest all of the features of claims 1-13 of the '492 patent.

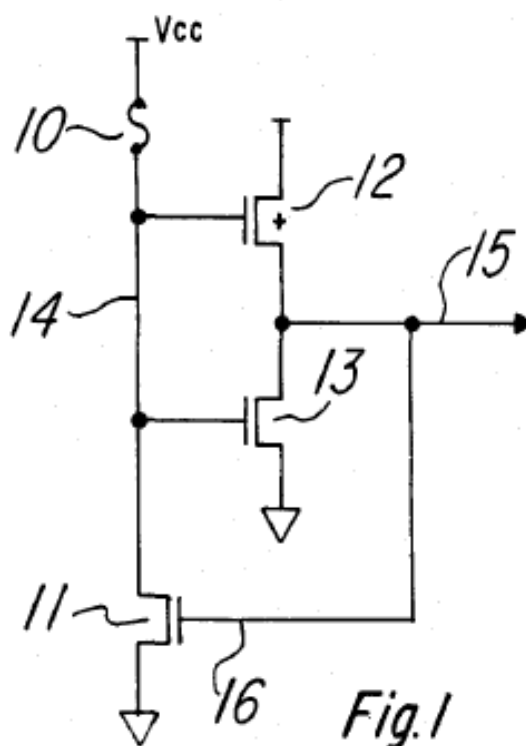
A. McAdams in Combination with Uda Discloses or Suggests Claims 1-5, 8-10, and 13

66. In my opinion, McAdams in Combination with Uda discloses all of the features of claims 1-5, 8-10, and 13 of the '492 patent.

1. Claim 1

a) “A programmable latch comprising:”

67. I understand that “[a] programmable latch comprising” is the preamble of claim 1. I have been asked to assume that the preamble is limiting. In my opinion, McAdams discloses this feature. For example, McAdams discloses a fuse circuit depicted in figure 1.



(Ex. 1006 at FIG. 1.)

68. McAdams describes the operation of the fuse circuit of figure 1 as follows:

Referring to FIG. 1, a fuse circuit constructed according to the invention is illustrated. **A fuse element 10** is connected in series with **an N-channel feedback transistor 11**, and this series circuit is connected between a supply voltage V_{cc} and V_{ss} . **A CMOS inverter including a P-channel transistor 12 and an N-channel transistor 13** has the node 14 as an input and produces an output 15. **Feedback is provided from the output node 15 to the gate of the transistor 11 by a line 16.**

(*Id.* at 1:67-2:7 (emphases added).)

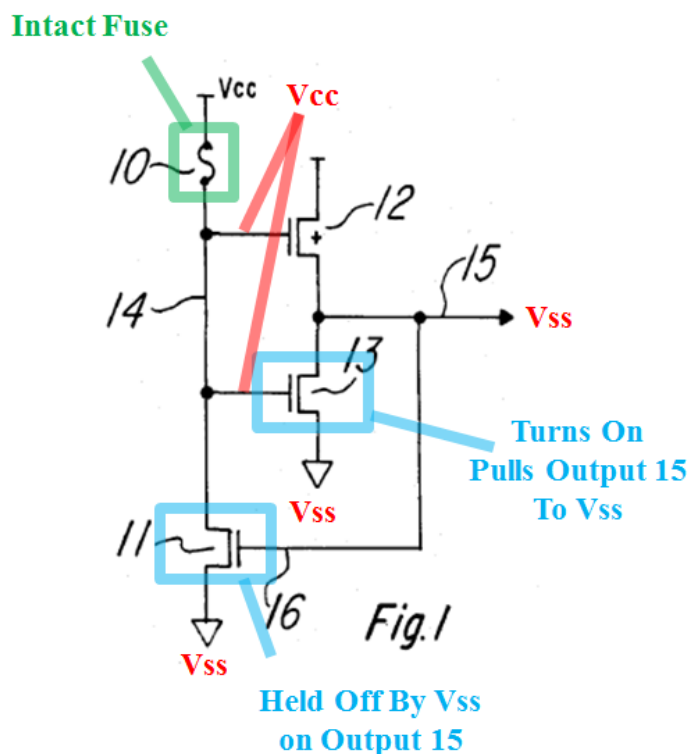
69. I have annotated figure 1 of McAdams below to show how the circuit of figure 1 operates when the fuse has not been blown. As shown, when the fuse 10 is intact and has not been blown when power is applied to the circuit, the node 14 follows the power supply V_{cc} , which turns on transistor 13. McAdams describes the operation of the circuit of figure 1 as follows:

During power-up of the supply voltage V_{cc} , as V_{cc} goes from zero to +5 v, if the fuse has not been blown, the node 14 follows V_{cc} since the node 15 starts at V_{ss} potential and the transistor 11 is off. Since the node 14 follows V_{cc} , the P-channel transistor 12 stays off. As soon as V_{cc} and node 14 reach the N-channel threshold voltage, V_{tn} , the transistor 13 turns on, holding the output node 15 at V_{ss} . This quickly discharges to zero any capacitive coupling of voltage to the

output node 15 at power-on due to the V_{cc} transition, and so the transistor 11 is held off.

(*Id.* at 2:8-18.)

70. When transistor 13 turns on, any charge on the output node 15 is discharged, pulling the output 15 to V_{ss} . (*Id.*; see also my discussion above in Section V.B.) The V_{ss} voltage on the output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state. (Ex. 1006 at 2:8-18.)

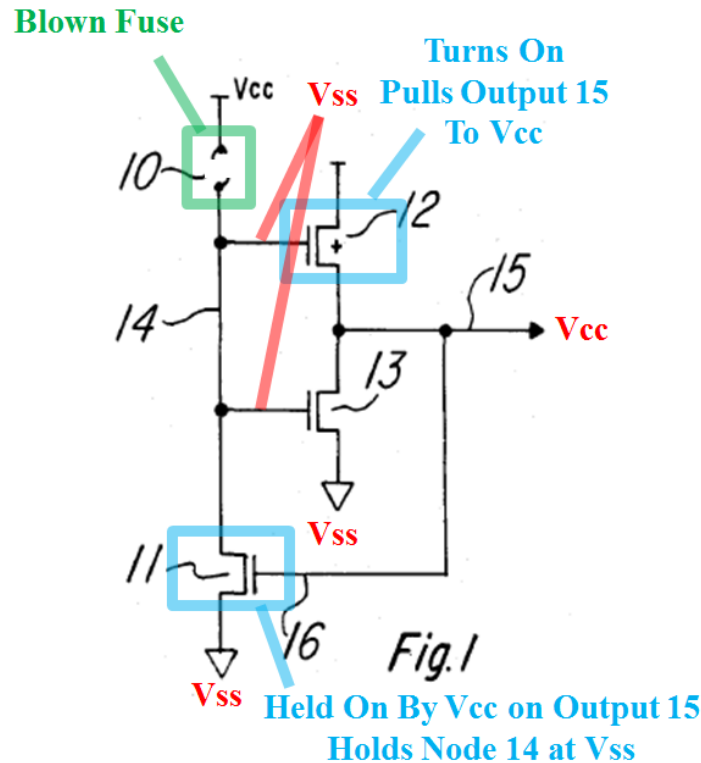


(*Id.* at FIG. 1 (annotated).)

71. I have also created a demonstrative in order to show how the circuit shown in figure 1 of McAdams operates when the fuse has been blown. As shown in the demonstrative below, the blown fuse includes a break (open circuit) in the conductor included inside the fuse 10. According to McAdams, when the fuse is blown, the node 14 is at Vss when power is applied. (*Id.* at 2:21-22.) Because the gate of P-channel transistor 12 is at Vss, transistor 12 turns on and the output node 15 is pulled to Vcc. (*Id.* at 2:22-24.) The Vcc voltage on the output is fed back to the gate of transistor 11, which turns transistor 11 on and holds the node 14 at Vss. (*Id.* at 2:24-26; *see also* my discussion above in Section V.B.) Holding node 14 at Vss ensures that the P-channel transistor 12 remains on and the output 15 is held is Vcc. McAdams discloses:

If the fuse 10 has been blown, as Vcc is powered up, node 14 is at Vss and the P-channel transistor 12 turns on as soon as its threshold Vtp is reached, causing the output node 15 to follow Vcc. Once the node 15 reaches the threshold Vtn, the transistor 11 turns on, keeping the node 14 at Vss.

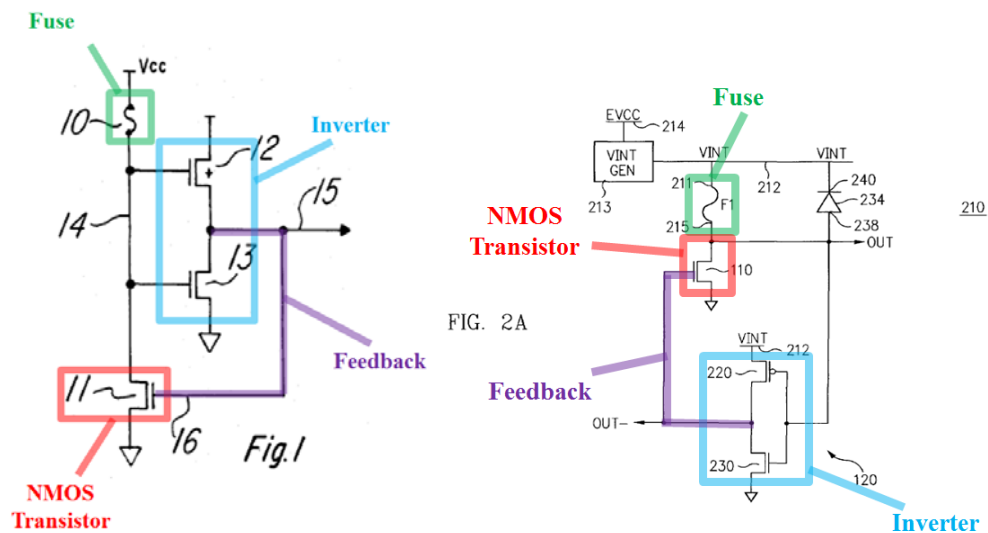
(Ex. 1006 at 2:21-26.)



(*Id.* at FIG. 1 (annotated and modified to show open circuit in fuse 10).)

72. Therefore, a person of ordinary skill in the art would have understood that based on whether the fuse 10 has been blown or is intact, the output 15 of the fuse circuit shown in figure 1 will be held at either Vcc or Vss. (*Id.* at 2:8-26.) The feedback of the output of the inverter to the transistor 11 holds that output at Vcc or Vss. (*Id.*) Therefore, the output is latched at either Vcc or Vss based on whether or not the fuse is blown. (*Id.*) A person of ordinary skill in the art would have recognized that the fuse circuit constitutes a “programmable latch” where the programming corresponds to the state of the fuse, which determines the latched value at the output.

73. Indeed, a person of ordinary skill in the art would have recognized that the fuse circuit of McAdams corresponds to a “programmable latch” in the same manner as that disclosed in the figure 2A of the ’492 patent. As shown in the annotated figures below, the programmable latch shown in figure 2A of the ’492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the fuse circuit in figure 1 of McAdams. (Ex. 1001 at FIG. 2A; Ex. 1006 at FIG. 1.)

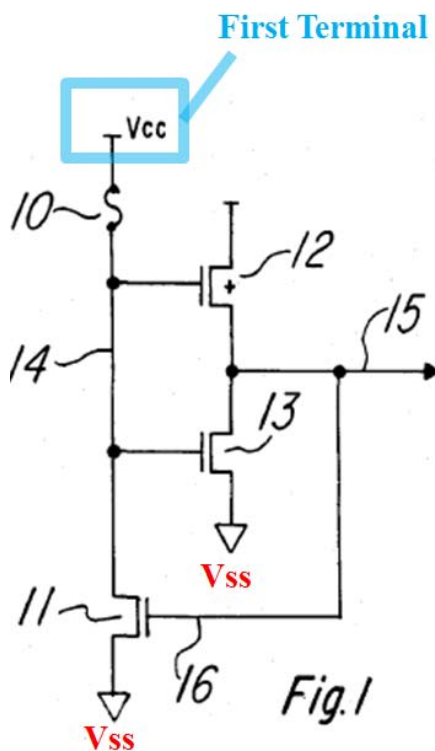


(Ex. 1006 at FIG. 1 (annotated); Ex. 1001 at FIG. 2A (annotated).)

b) “a first terminal for receiving a first voltage;”

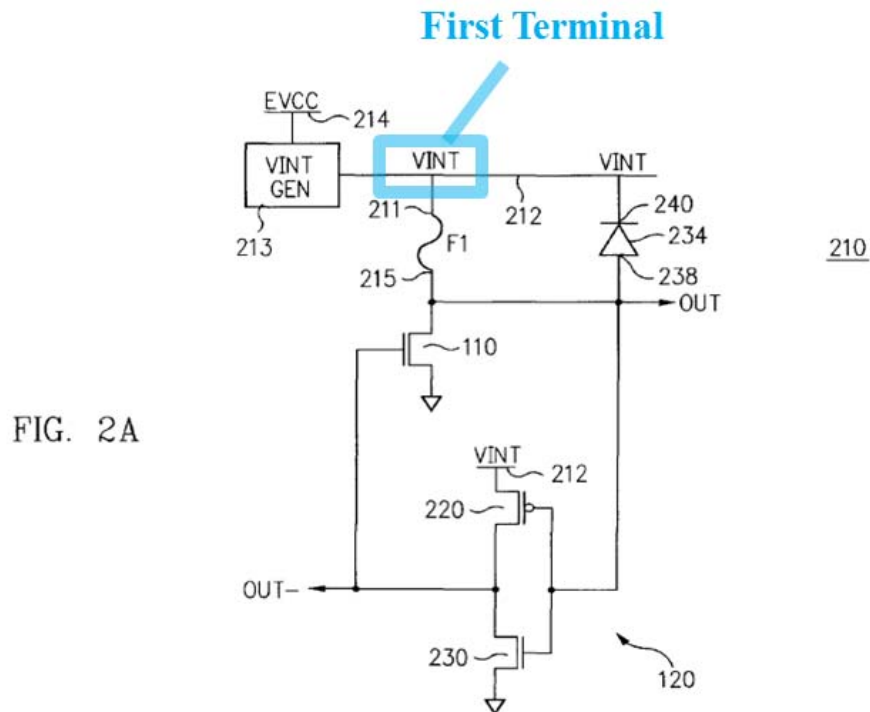
74. In my opinion, McAdams discloses this feature. As shown in annotated figure 1 below, the “programmable latch” of McAdams includes a “terminal” Vcc, where Vcc is a “supply voltage” that is applied when power is applied to the circuit of figure 1. (Ex. 1006 at 2:2-3, “series circuit is connected

between a supply voltage V_{cc} and V_{ss} ”, 2:8-9, “During power-up of the supply voltage V_{cc} as V_{cc} goes from zero to +5 v”, 3:24-26, “wherein said one of the first and second terminals of said power supply is a positive voltage and said other is ground”, 4:20-22, “a power supply having a first terminal at a positive voltage and a second terminal at a ground potential”). In the example embodiment of McAdams, V_{cc} is at +5 v after power up of the latch and therefore constitutes “a first voltage.” Therefore, the terminal highlighted in blue below constitutes a “first terminal for receiving a first voltage.”



(*Id.* at FIG. 1 (annotated).)

75. As shown in annotated figure 2A of the '492 patent below, a person of ordinary skill in the art would have understood that the “first terminal” highlighted in figure 1 of McAdams above is consistent with the “first terminal” disclosed by the '492 patent.

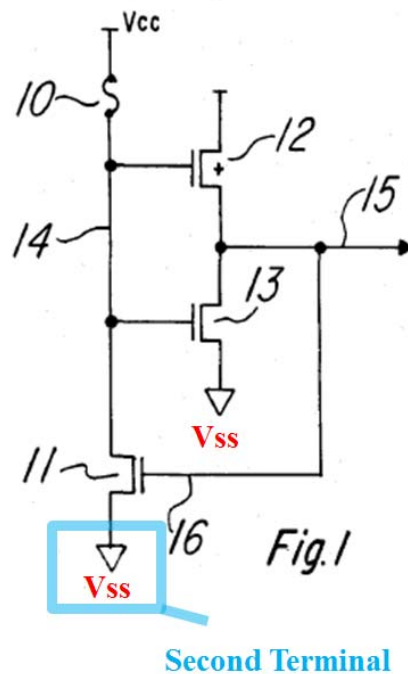


(Ex. 1001 at FIG. 2A (annotated).)

c) “a second terminal for receiving a second voltage”

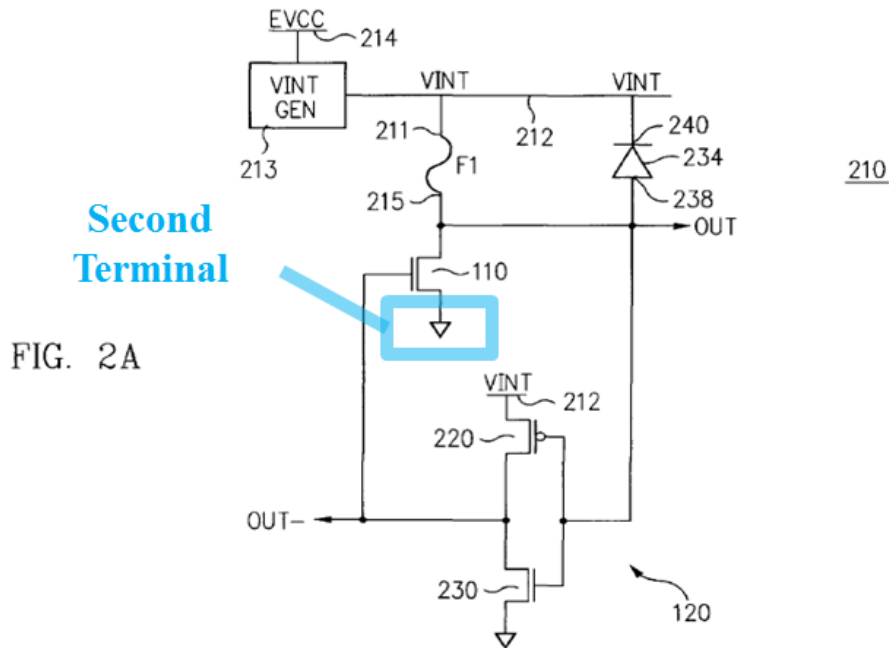
76. In my opinion, McAdams discloses this feature. For example, the programmable latch circuit in figure 1 of McAdams includes a terminal (“second terminal”) for receiving V_{ss} (“a second voltage”). (Ex. 1006 at 2:2-3, “series circuit is connected between a supply voltage V_{cc} and V_{ss} ”, 2:8-9, “During power-

up of the supply voltage V_{cc} , as V_{cc} goes from zero to +5 v”, 2:14-17, “[T]he transistor 13 turns on, holding the output node 15 at V_{ss} . This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to V_{cc} transition.”) Therefore, McAdams discloses “a second terminal for receiving a second voltage.”



(*Id.* at FIG. 1 (annotated).)

77. As shown in annotated figure 2A of the '492 patent below, a person of ordinary skill in the art would have understood that the “second terminal” highlighted in figure 1 of McAdams above is consistent with the “second terminal” disclosed by the '492 patent.

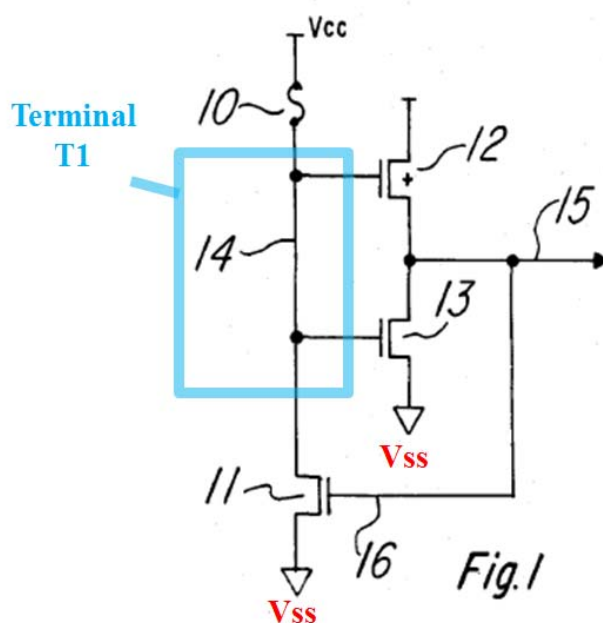


(Ex. 1001 at FIG. 2A (annotated).)

d) “a terminal T1 for providing a signal indicating a state of the programmable latch;”

78. In my opinion, McAdams discloses this feature. For example, as shown in annotated figure 1 below, the node 14 indicates the state of the fuse, which corresponds to the state of the programmable latch (“a terminal T1 for providing a signal indicating a state of the programmable latch”). As I discussed above with respect to claim element 1(a), when power is applied to the latch, if the fuse is intact, node 14 is at Vcc (high), but if the fuse is blown, node 14 is at Vss (low). (See also my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.A.1(a).) Therefore, the voltage at node 14

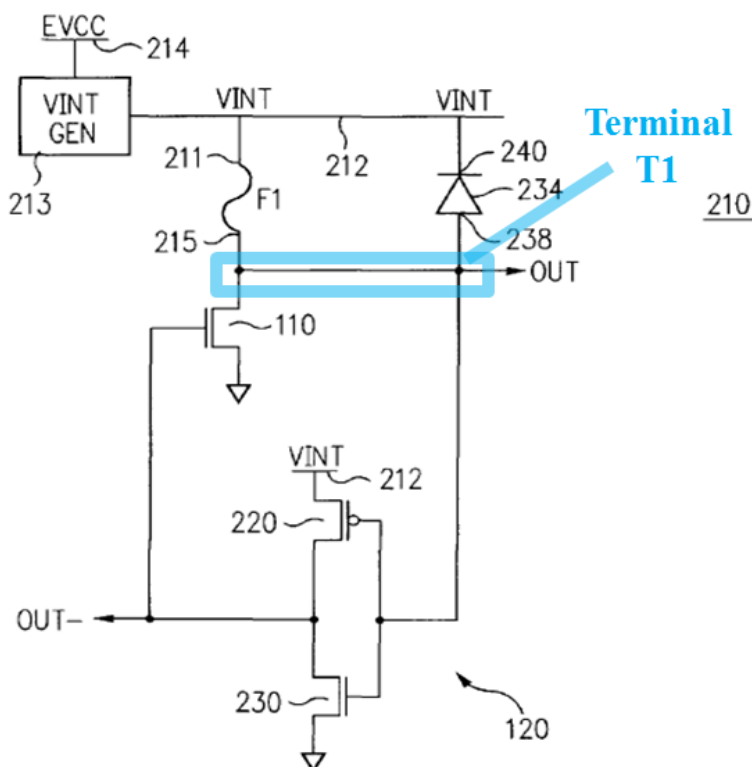
indicates a “state of the programmable latch” because it indicates whether the fuse is blown or not.



(Ex. 1006 at FIG. 1 (annotated).)

79. As shown in annotated figure 2A of the '492 patent below, a person of ordinary skill in the art would have understood that the “terminal T1” highlighted in figure 1 of McAdams above is consistent with the “terminal T1” disclosed by the '492 patent.

FIG. 2A

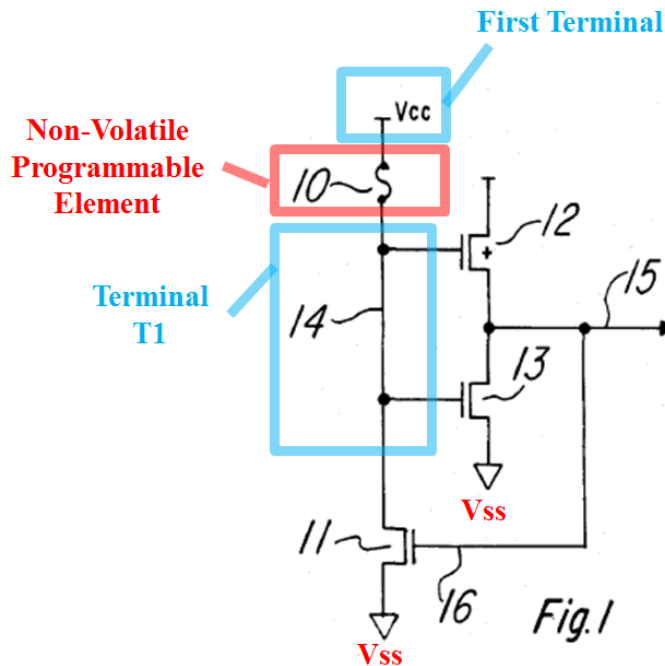


(Ex. 1001 at FIG. 2A (annotated).)

e) “a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;”

80. In my opinion, McAdams discloses this feature. For example, the fuse 10 that I have highlighted in red in annotated figure 1 below is a “non-volatile programmable element.” Such an understanding is consistent with the disclosure of the ’492 patent, which shows a fuse as the “non-volatile programmable element” in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 3:10-23, 7:24-36.)

Moreover, claim 10, which depends from claim 1, recites “wherein the programmable element is a fuse,” thereby demonstrating that a fuse is a “non-volatile programmable element” in the context of claim 1 and the ’992 patent. (*Id.* at 9:25-27.)



(Ex. 1006 at FIG. 1 (annotated).)

81. As shown in annotated figure 1 above, the fuse 10 (“non-volatile programmable element”) is coupled between Vcc (“first terminal”) and node 14 (“terminal T1”), thereby forming an “electrical path” between Vcc (“first terminal”) and node 14 (“terminal T1”). When the fuse 10 is intact, such that the conductor within the fuse is not broken or cut by, for example, a laser, the fuse

allows current to flow between its two terminals (i.e. it is “conductive”). Therefore, when the fuse is intact and “conductive,” it provides an electrical connection between Vcc (“first terminal”) and node 14 (“terminal T1”). (*Id.* at 2:8-11; *see also* my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.A.1(a).) Therefore, in my opinion, McAdams discloses “when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal.”

82. If the fuse 10 is blown such that the conductor within the fuse is severed and there is an open circuit between the two terminals of the fuse, the fuse is non-conductive and does not allow current to flow between the terminals. Therefore, when the fuse is blown and “non-conductive,” the fuse does not provide an electrical connection between Vcc (“first terminal”) and node 14 (“terminal T1”). (*Id.* at 2:21-24 (explaining that even though Vcc is powered up, node 14 remains at Vss); *see also* my discussion above regarding the operation of the circuit in figure 1 of McAdams in Section IX.A.1(a).) As shown in figure 1 of McAdams, if the fuse is broken, there is no electrical path between Vcc (“the first terminal”) and node 14 (“terminal T1”). Therefore, McAdams discloses “when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal.”

83. In my opinion, because the state of the fuse may be modified or programmed to determine whether or not the electrical path connects Vcc (“first terminal”) to node 14 (“terminal T1”), a person of ordinary skill in the art would have understood that McAdams discloses a “programmable electrical path” having the features recited in claim element 1(e).

f) “a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and”

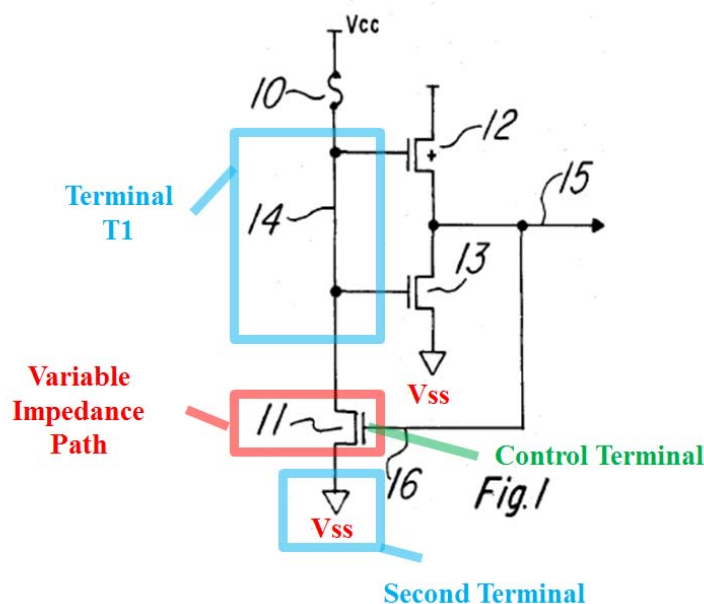
84. In my opinion, McAdams discloses this feature. For example, a person of ordinary skill in the art would have understood that the N-channel (NMOS) transistor 11 highlighted below in annotated figure 1 is a “variable-impedance electrical path” as that term is used in the ’492 patent. Indeed, such an understanding is consistent with the disclosure of the ’492 patent, which shows an NMOS transistor as the “variable-impedance electrical path” in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A.) As the ’492 patent explains:

In some embodiments, transistor 110 is replaced by a *variable-impedance electrical path which includes a number of transistors* connected in series or in parallel between the terminal OUT and the ground terminal. One or more of the transistors have their gates connected to the output of inverter 120 or 120.3. In some embodiments, other circuit elements (such as resistors, perhaps variable-impedance resistors) are

included between the terminal OUT and the ground or VINT terminals.

(*Id.* at 7:58-66, emphasis added.)

85. I also understand that claim 10, which depends from claim 1, recites “the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal.” (*Id.* at 9:28-30.) As such, a person of ordinary skill in the art would have understood that an NMOS transistor is a “variable-impedance electrical path” in the context of claim 1 and the ‘492 patent.



(Ex. 1006 at FIG. 1 (annotated).)

86. As shown in annotated figure 1 above, a person of ordinary skill in the art would have understood that the NMOS transistor 11 (“variable-impedance

electrical path”) is coupled between node 14 (“terminal T1”) and Vss (“second terminal”) and therefore constitutes “variable-impedance electrical path connected between the terminal T1 and the second terminal.”

87. In my opinion, McAdams also discloses that “the impedance of the electrical path is controlled by a signal on the terminal T1,” as recited in claim element 1(f). For instance, as shown in annotated figure 1 above, the signal on node 14 (“terminal T1”) is inverted by the CMOS inverter collectively formed by transistors 12 and 13, and the output of the inverter at node 15 is coupled to the gate of the NMOS transistor 11. (*Id.* at FIG. 1.) A person of ordinary skill in the art would have understood that the voltage on the gate terminal of the NMOS transistor 11 controls whether the transistor 11 is on or off.

88. If the NMOS transistor 11 is on, it has a lower impedance than when the NMOS transistor 11 is off. (*See* my discussion above in Section V.B.) A person of ordinary skill in the art would have understood that the signal at node 14 (“terminal T1”) determines the signal at node 15, which in turn determines whether the NMOS transistor 11 is on or off, i.e., has a low or high impedance (“the impedance of the electrical path is controlled by a signal on the terminal T1”). McAdams discloses:

As soon as Vcc and node 14 reach the N-channel threshold voltage, Vtn, the transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to the Vcc transition, and so the transistor 11 is held off. Thus the only current flowing through the fuse 10 from the Vcc supply is leakage current, on the order of nanoamps.

If the fuse 10 has been blown, as Vcc is powered up, node 14 is at Vss and the P-channel transistor 12 turns on as soon as its threshold Vtp is reached, causing the output node 15 to follow Vcc. **Once the node 15 reaches the threshold Vtn, the transistor 11 turns on, keeping the node 14 at Vss.**

(*Id.* at 2:12-26 (emphasis added).)

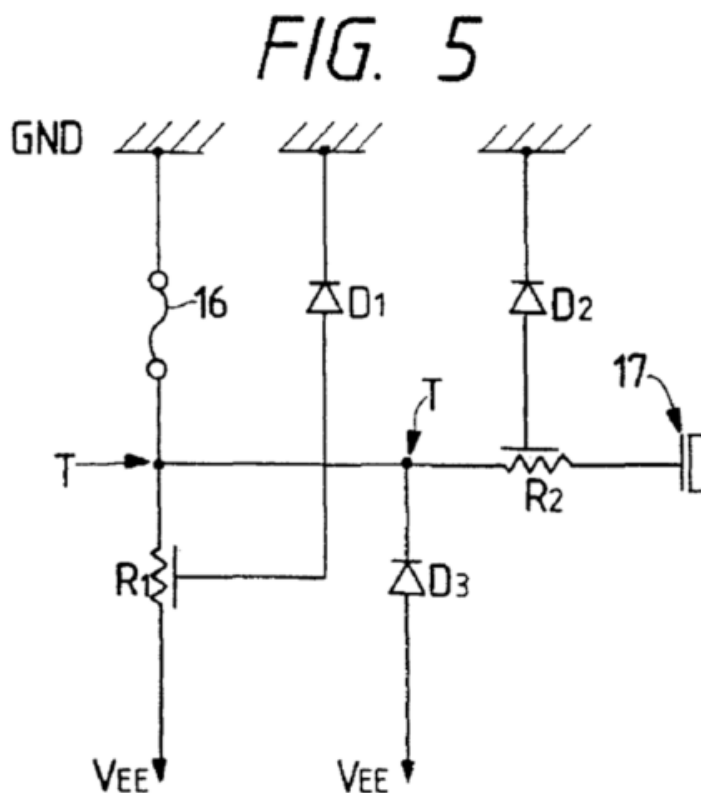
g) “a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.”

89. In my opinion, McAdams in view of Uda discloses or suggests this feature. McAdams does not explicitly disclose “a diode” for keeping the voltage on the terminal T1 within a predetermined range of values as recited in claim element 1(g). But in my opinion, Uda discloses such a feature, and in view of Uda, a person of ordinary skill in the art would have been motivated to include a diode

in McAdams. As I explain below, in the resulting combination, the voltage on node 14 (“terminal T1”) is kept within a predetermined range of values.

90. Uda, like McAdams, is in the field of semiconductor integrated circuit devices, including redundancy circuits for memory devices that use fuses to enable such redundancy circuits. (Ex. 1006 at 1:5-12, 1:41-51, FIG. 1; Ex. 1007 at 1:10-17, 3:15-19, 3:32-37, FIG. 5.) Therefore, a person of ordinary skill in the art implementing the circuit of McAdams would have had reason to look to Uda.

91. Uda discloses “[a] fuse arrangement that acts to replace a defective cell with the corresponding backup cell,” where figure 5 depicts “how the fuse arrangement is connected” in one embodiment. (Ex. 1007 at 9:21-29.)



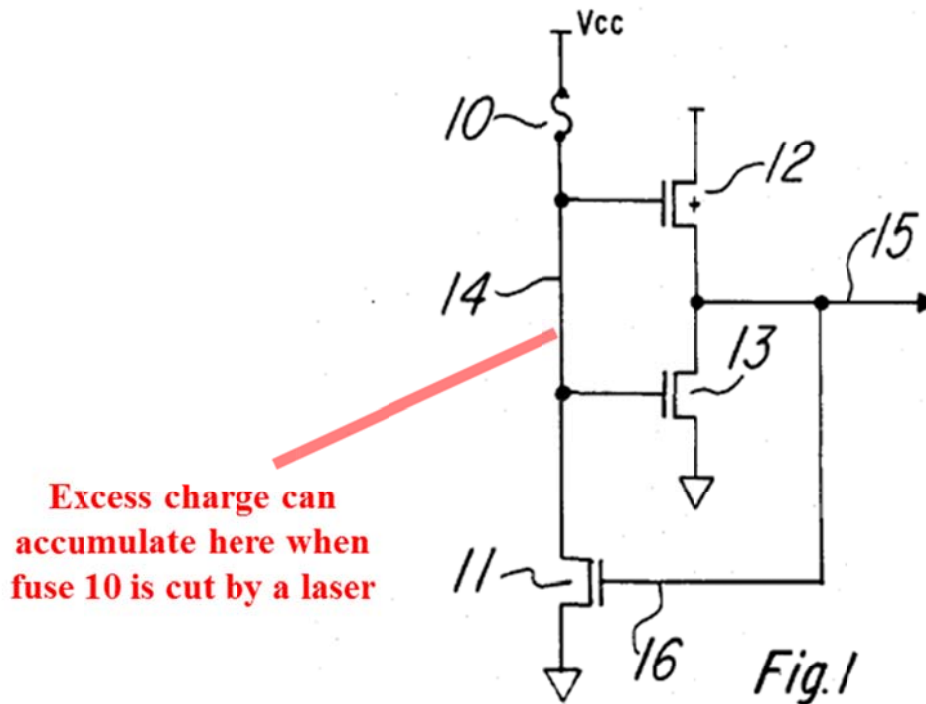
(*Id.* at FIG. 5.)

92. Uda discloses that “[t]he switching between faulty parts and their backup elements in the semiconductor chip is accomplished by the melting of fuses constituting part of the redundancy circuit therein” where “[t]he fuses are melted, illustratively, by use of a laser means or electrical means.” (*Id.* at 1:38-42.) Uda further discloses that “[t]he purpose of furnishing diodes D1 through D3 and the resistor R2 is to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the NMOS gate.” (*Id.* at 9:44-47.)

Specifically, Uda discloses that “[i]f a positive charge develops, the charge is led to the ground line GND via the diodes D1 and D2,” which contributes to protecting the NMOS gate 17 from destruction. (*Id.* at 9:47-53.)

93. McAdams, like Uda, discloses that a laser can be used to program the fuse 10 shown in figure 1 of McAdams. (Ex. 1006 at 1:12-14 (“These fuses are usually polysilicon conductor strips that are selectively blown by an indexed laser beam.”).) Based on the teachings of Uda, a person of ordinary skill in the art would have been motivated to modify the circuit of figure 1 in McAdams to implement a diode like that disclosed in Uda in order to provide protection for the transistors 12 and 13, the gates of which are connected to node 14.

94. A person of ordinary skill would have recognized that when a laser is used to blow a fuse (i.e., program the fuse), charge from the laser can accumulate at various points in the circuit. (Ex. 1007 at 9:44-47.) As shown below, just like in Uda, one place in the McAdams’s circuit where excess charge can accumulate is node 14, which is connected to the gates of transistors 12 and 13.

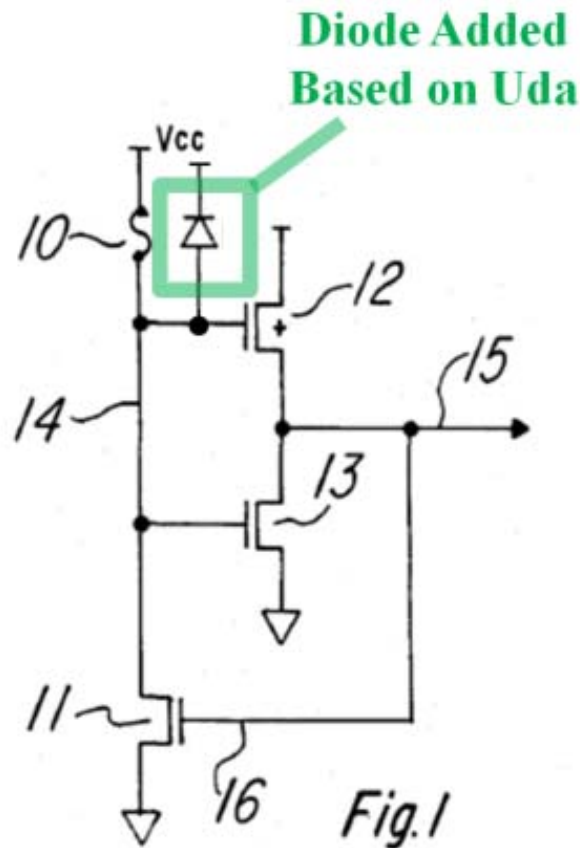


(Ex. 1006 at FIG. 1 (annotated).)

95. For example, in view of Uda, a person of ordinary skill in the art would have been motivated to implement, among other things, a diode connected between the node 14 and the power supply voltage V_{CC} such that when the fuse 10 is programmed using a laser, any excess charge on node 14 stemming from the laser cutting of the fuse would be led to the power supply node V_{CC} . As a non-limiting example, a demonstrative is provided below, showing certain aspects of the combined McAdams-Uda circuit that a person of ordinary skill in the art would

have found to be consistent with the modification of the circuit of FIG. 1 of McAdams based on Uda.⁶

⁶ The demonstrative is a non-limiting and exemplary demonstrative that I have created to help explain the McAdams-Uda combination. Indeed, all of the demonstratives in this declaration, where I have modified a figure from a prior art or created a drawing to explain basic circuit concepts, are exemplary and should not be viewed as limiting.



(*Id.* at FIG. 1 (annotated).)

96. Specifically, a person of ordinary skill in the art would have recognized that a diode positioned between node 14 and the Vcc node as shown above would have allowed any excess charge that might develop on node 14 during laser cutting to be dissipated to ground *such that the excess charge would not damage the gate of transistors 12 and 13.* (See Ex. 1007 at 9:44-53.) A person of ordinary skill in the art would have understood that when the fuse is cut using a laser, power would not be applied to the memory device that includes the latch

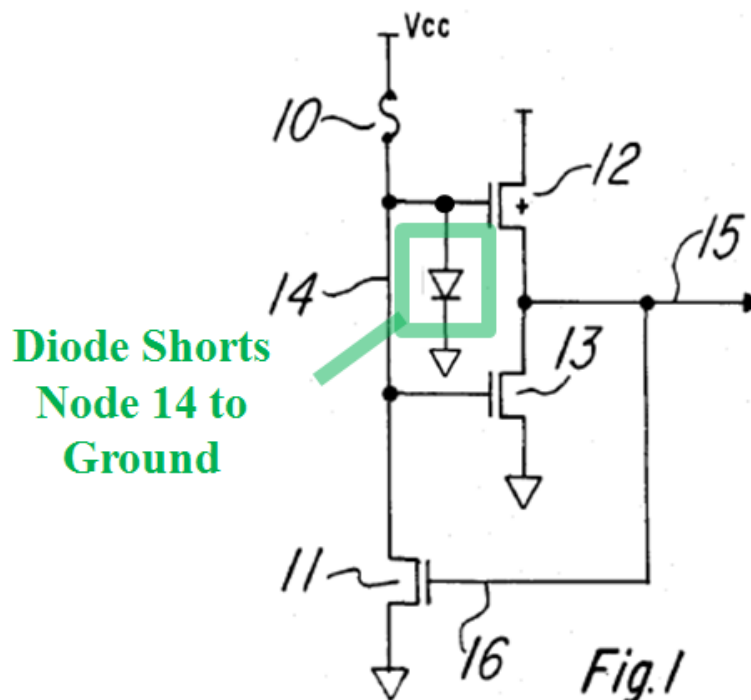
circuit of McAdams. As such, the Vcc node shown in figure 1 of McAdams would be at 0v (ground) when the laser cutting of the fuse occurs. (Ex. 1006 at 2:8-9.)

97. As disclosed by Uda, such laser cutting can induce unwanted charge on the node 14, which is coupled to the fuse 10. (Ex. 1007 at 9:44-47.) For example, positive charge resulting from laser cutting that builds up on node 14 could result in a gate-to-source voltage for one or both of the transistors 12 and 13 that is sufficiently high to cause damage to the transistors. As disclosed by Uda, “[i]f a positive charge develops, the charge is led to the ground line GND via the diodes D1 and D2,” which contributes to protecting the NMOS gate 17 from destruction. (Ex. 1007 at 9:47-53.)

98. A person of ordinary skill in the art modifying McAdams based on Uda would have recognized that the placement of the diode as shown in the demonstrative above would have allowed for the charge on node 14 to be dissipated while not interfering with the operation of the latch circuit in McAdams. For example, while the Vcc node in McAdams is at ground when power is not applied the device, which allows the diode to dissipate any positive charge on node 14 at that time, when power is supplied to the device, Vcc is at a voltage that is as high or higher than the voltage on the node 14. Therefore, during operation of the programmable latch in McAdams, because Vcc is high, the diode cannot be

forward biased because the voltage at the anode will not exceed the voltage at the cathode (+5 v). (See my discussion regarding diodes in Section V.C above.) Therefore, while the diode can protect the transistors during laser cutting, it will not interfere with the operation of the circuit when power is applied.

99. A person of ordinary skill in the art would have recognized that, in contrast to the diode positioning shown in the demonstrative above, a diode connected between node 14 and the ground terminal (instead of the Vcc terminal) would interfere with the normal operation of the latch circuit. The demonstrative below shows such a diode connected between node 14 and ground.



(Id. at FIG. 1 (annotated).)

100. While the diode shown in the demonstrative immediately above would provide protection to the transistors 12 and 13 during laser cutting by dissipating charge from node 14 in the same manner as the diode connected between node 14 and Vcc discussed above, a person of ordinary skill in the art would have understood that the diode connected between node 14 and ground would not allow the circuit of figure 1 of McAdams to function properly. For example, when power is applied to the device, the diode would effectively short the node 14 to ground. If the fuse 10 is intact, node 14 will be pulled towards Vcc (+5 v) and the diode will become forward biased as soon as the node 14 exceeds the threshold voltage of the diode. As a result, current will continuously flow through the fuse and diode between Vcc and ground, which a person of ordinary skill in the art would have understood is undesirable and in conflict with the “low power” objectives of McAdams. (Ex. 1006 at 1:18-38.)

101. Moreover, depending on the resistance through the fuse and the diode, the inclusion of a diode between node 14 and ground (Vss) may not allow the node 14 to be pulled up to a voltage sufficiently high to turn on the NMOS transistor 13 included in the inverter of McAdams’ latch circuit. Additionally, the inclusion of the diode in the above configuration may cause the fuse to blow because of excessively high current through the fuse. As a result, assuming that node 14

remains low, the PMOS transistor 12 turns on and pulls output node 15 high. If output node 15 is pulled high, then NMOS transistor 11 turns on, thereby creating another path between Vcc and ground and resulting in not only an incorrect output at node 15, but also in additional power consumption through another direct path between Vcc and ground. For at least these reasons, a person of ordinary skill in the art would have understood that the diode in the McAdams-Uda combination should be placed between the node 14 and the Vcc power supply node such that it would achieve the desired objective of protecting the transistors 12 and 13 without interfering with the proper operation of the latch circuit. Moreover, it is my opinion that any modifications necessary to ensure that the diode as in Uda would work in the McAdams fuse circuit would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

102. A person of ordinary skill in the art would also have recognized that while the circuit shown in Uda includes additional components that may also facilitate Uda's objective of protecting the gate of the transistor 17 from unwanted charge that can accumulate on the node coupled to the gate of that transistor, not all of those components would be required in order to realize the benefit of protecting the transistors 12 and 13 in the McAdams-Uda combination. Instead, a person of ordinary skill in the art would have understood that the inclusion of the

diode between node 14 and VDD discussed above would *by itself* provide tangible benefit in dissipating positive charge on node 14 regardless as to whether any of the other circuit components shown in Uda are also included. (Ex. 1007 at 9:44-49.) Similarly, while Uda describes a particular physical construct for the diodes shown in figure 5 of Uda (*id.* at 10:36-41), a person of ordinary skill in the art would have understood that the functionality of the diode as described in Uda (dissipating charge on the node to avoid damage to the transistor) is not dependent on the specific materials or methods used to form the diode.

103. Moreover, even if a person of ordinary skill in the art were to include additional aspects of the circuit shown in figure 5 of Uda, such a person of ordinary skill in the art would have understood how to include such circuitry in a manner that would not adversely affect the functionality of the McAdams' fuse circuit. For example, a person of ordinary skill in the art would have understood the diode D3 coupled between V_{EE} and the node T in Uda would have allowed negative charge that might build up on the node T to be dissipated to the supply V_{EE} (the diode would be forward biased if the voltage on node T becomes more negative than V_{EE} by more than a threshold voltage of the diode D3). (*Id.* at 9:49-51.) Similarly, Uda indicates that the resistor R2 causes any residual charge (which a person of ordinary skill in the art would have understood would be

minimal after the discharging by the diodes) to lose its energy. A person of ordinary skill in the art would have understood that if the laser-cutting of the fuse could result in significant negative charge or the residual charge could be problematic, then such additional components could be added to the fuse circuit of McAdams in a manner that does not alter the overall functionality of the circuit.

104. A person of ordinary skill in the art would have been motivated to combine the teachings of McAdams and Uda as described above to implement a fuse-based redundancy circuit that is more robust in that damage to transistors included in the circuit is avoided when the fuse in the circuit is blown using a laser. Such a modification of McAdams' disclosed circuit would have been straightforward for a person of ordinary skill in the art to implement because Uda discloses how such a diode is included in a fuse-based circuit and explains how the diode allows excess charge on a node coupled to one end of the fuse to be led to a supply voltage (e.g. ground). For example, the McAdams circuit is similar to Uda's circuit because, just like Uda includes a fuse between the gate of transistor 17 and a power supply terminal,⁷ McAdams, like Uda, includes a fuse connected

⁷ In Uda, the power supply terminal is GND. (Ex. 1007 at FIG. 5.) But Uda's power supply terminal (GND) is analogous to Vcc in McAdams because both

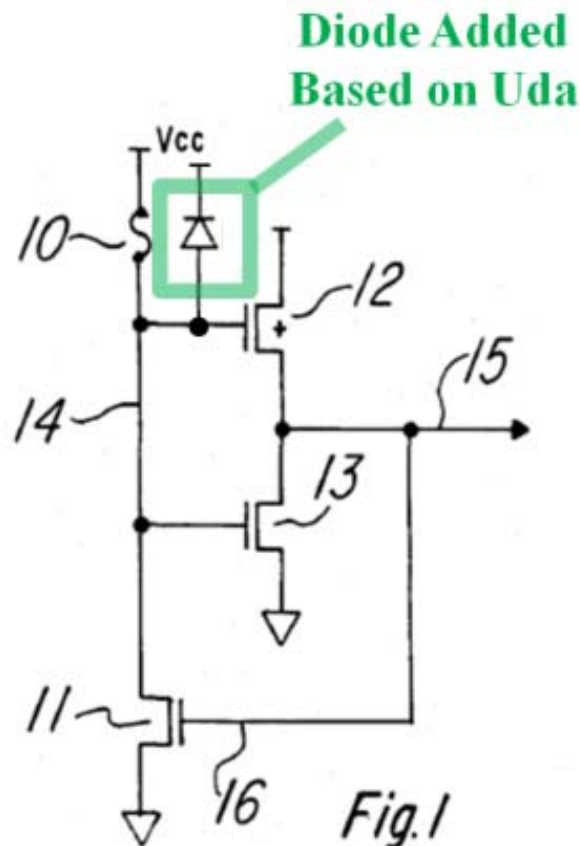
between node 14 and a power supply terminal (V_{CC}), where the node 14, also like Uda, is used to provide a signal to the gate of a transistor. A person of ordinary skill in the art would have thus had reason and the capability to modify McAdams based on Uda as noted above. For instance, as I discussed above, a person of ordinary skill in the art would have recognized that adding the diode in the McAdams circuit would have provided protection for the transistors 12 and 13 in the event that any excess charge is deposited on node 14 during laser cutting of the fuse 10. (*Id.*) Adding the diode in the McAdams circuit would have made the McAdams circuit more robust, and therefore, a person of ordinary skill in the art would have been motivated to, and would have been capable of, making the above noted modification of the McAdams circuit based on Uda.

105. As also discussed above, including the diode like that disclosed by Uda in the circuit of figure 1 of McAdams would not have negatively impacted the circuit. Rather, it would have been a predictable combination of known

terminals receive the highest voltage in the circuit. Specifically, in Uda, the GND terminal receives 0V whereas the VEE terminal receives -4V. (Ex. 1007 at 9:28-36.) In McAdams, the Vcc node goes from 0V to 5V and Vss is at ground (i.e., 0V). (Ex. 1006 at FIG. 1, 2:8-11, claim 4.)

components according to known methods (e.g., replication of Uda's transistor-protecting diode in the fuse-based redundancy circuit disclosed by McAdams), and would have been consistent with the expected result that it would be less likely that transistors 12 and 13 would be damaged when the laser is used to blow fuse 10.

106. The circuit illustrated in the demonstrative below for the McAdams-Uda combination discloses or suggests claim element 1(g), as I explain below.



(*Id.* at FIG. 1 (annotated).)

107. McAdams discloses that before power is supplied to the latch shown in figure 1, the supply voltage V_{CC} is at 0V (ground). (*Id.* at 2:8-9 (“During power-up of the supply voltage V_{CC} , as V_{CC} goes from zero to +5 v”).) A person of ordinary skill in the art would have understood that when V_{CC} is at 0V (i.e., “before power is supplied to the latch”), the diode in the combined McAdams-Uda circuit would not allow the voltage at node 14 to exceed 0 volts by more than a threshold voltage of the diode. Such an understanding is consistent with the disclosure of Uda as discussed above and also consistent with the disclosure of the ’492 patent:

High reliability is achieved in some embodiments by a diode that keeps a voltage on a latch output terminal within a predetermined range of values before power is supplied to the latch. In some embodiments, the diode’s anode is connected to terminal OUT, and the cathode is connected to an external power supply pin EVCC or to a reference voltage terminal. When power is off, the EVCC pin or the reference voltage terminal is at ground, and therefore the voltage on the terminal OUT is not higher than one diode threshold voltage relative to ground (0.65V in some embodiments.) The maximum voltage of 0.65 V on terminal OUT allows the latch to be powered up correctly even if fuse F1 is blown.

(Ex. 1001 at 2:1-12.)

108. Therefore, the combined McAdams-Uda circuit discloses “a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” That is, the diode keeps the voltage on terminal T1 below the threshold voltage of the diode (“predetermined range of values”) before power is supplied to the latch. The “predetermined range” within which the McAdams-Uda circuit keeps the voltage at node 14 (“terminal T1”) is consistent with a “predetermined range” as understood by the ’492 patent as claim 13, which depends from claim 1, recites “said predetermined range consists of all voltages below a predetermined value.” (*Id.* at 9:50-52.) As I discussed above, in the McAdams-Uda combination, the diode keeps the voltage on terminal T1 below the diode threshold and therefore “within a predetermined range of values,” consistent with the disclosure of the ’492 patent.

109. A person of ordinary skill in the art would also have understood that the addition of the diode would not only keep the voltage on node 14 (“terminal T1”) “within a predetermined range of values before power is supplied to the latch,” but the diode would also “**prevent the latch from assuming an incorrect state when power is supplied to the latch**” (emphasis added). Specifically, a person of ordinary skill in the art would have understood that in the correct state of the latch, the voltage on node 14 is V_{cc} (+5V) if the fuse 10 is not blown and V_{ss}

(0V) if the fuse 10 is blown. The diode in the McAdams-Uda combination would ensure the latch circuit operates correctly when power is supplied thereto (e.g. V_{CC} goes from 0 v to +5 v).

110. For instance, consider the situation in which the fuse 10 is blown. If the latch assumes a correct state when power is supplied to the latch, the voltage on node 14 should be 0V. Based on the discussion in the background of the '492 patent, in the absence of the diode, node 14 would be floating when power is applied. (*Id.* at 1:36-47.) As also discussed in the '492 patent, there is some concern that in such a situation there may be excess charge on node 14. (*Id.*) If such a situation exists, as the '492 patent suggests, and power was supplied to the latch of McAdams, the voltage on node 14 could be high enough that transistor 13 would turn ON, pulling down the gate of transistor 11. This would result in transistor 11 remaining OFF. As a result, node 14 would continue to remain at a high voltage as the excess charge on node 14 would not be drained to V_{SS} by transistor 11 even though fuse 10 is blown. That is, the latch would have assumed an "incorrect state when power is supplied to the latch."

111. But the diode included in the McAdams-Uda combination to protect the transistors 12 and 13 from damage during laser-programming also ensures that any excess charge on node 14 bleeds away such that if the fuse 10 has been blown,

PMOS transistor 12 (and not NMOS transistor 13) will turn ON as soon as V_{CC} becomes high enough so that the threshold voltage for transistor 12 is reached. For example, McAdams discloses:

If the fuse 10 has been blown, as V_{CC} is powered up, node 14 is at V_{SS} and the P-channel transistor 12 turns on as soon as its threshold V_{tp} is reached, causing the output node 15 to follow V_{CC} .

(Ex. 1006 at 2:21-24.)

112. Specifically, before power is supplied to the latch, the V_{CC} node in the McAdams-Uda combination is at 0V. (Ex. 1006 at 2:8-9 (“During power-up of the supply voltage V_{CC} , as V_{CC} goes from zero to +5 v ...”).) Therefore, the voltage on the node 14 will be held at or below the threshold voltage of the diode included in the McAdams-Uda circuit before power is supplied to the latch. (See Ex. 1001 at 2:33-50 (explaining that if the cathode of the diode is at ground, the anode can go no higher than a threshold of the diode (e.g., +0.65V).))

113. Because the voltage on the node 14 is held at or below the threshold voltage of the diode included in the McAdams-Uda circuit before power is supplied to the circuit, the gate-to-source voltage for the PMOS transistor 12 will quickly surpass the threshold voltage as V_{CC} goes from 0 v to +5 v. As disclosed by McAdams, when transistor 12 turns on, it pulls the output node 15 high, thereby

turning on NMOS transistor 11, which keeps the node 14 at V_{SS} and ensures that the output of the latch correctly reflects the state of the fuse 10. (*Id.* at 2:21-26.) Therefore, the diode in the McAdams-Uda combination “**prevents the latch from assuming an incorrect state when power is supplied to the latch**” because it ensures that if the fuse is blown and power is then supplied, the voltage on node 14 is quickly pulled down to V_{SS} , which is the correct state of the latch if the fuse is blown. Indeed, the diode in the McAdams-Uda circuit works just like diode 234 in the '492 patent. (Ex. 1001 at FIG. 2A, 2:33-50.)

114. Notably, if the fuse 10 is not blown when power is applied, the node 14 will rise with V_{CC} as it goes from 0 v to +5 v, and the diode will remain off as the same voltage (V_{CC}) is at the anode and the cathode of the diode. The high voltage on the node 14 turns on transistor 13 pulling node 15 low and maintaining transistor 11 in the off state. Thus, as discussed above, the diode does not interfere with the operation of the circuit when the fuse is not blown.

115. Therefore, in my opinion, the combined McAdams-Uda circuit discloses or suggests “a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied, to the latch to prevent the latch from assuming an incorrect state when power is supplied to the latch.”

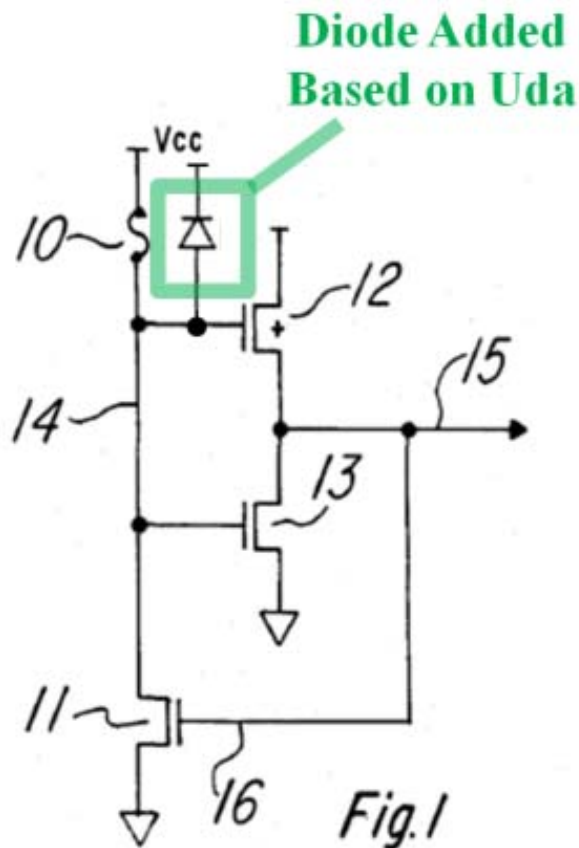
2. Claim 2

a) “The programmable latch of claim 1 wherein during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltages.”

116. In my opinion, McAdams in view of Uda discloses or suggests this feature. As I discussed above with respect to claim element 1(a), when power is applied, the voltage at node 14 (“terminal T1”) is only influenced by the power supply voltage V_{cc} and V_{ss} (“first and second voltages”) and the state of the fuse 10 (“programmable element”). (See my discussion above in Section IX.A.1(a); Ex. 1006 at 1:67-2:33.) If the fuse 10 is not blown, node 14 is pulled to V_{cc} when power is supplied (i.e., during operation of the latch). (See my discussion above in Section IX.A.1(a); Ex. 1006 at 1:67-2:34.) If the fuse is blown, node 14 is pulled to V_{ss} when power is supplied (i.e., during operation of the latch). (See my discussion above in Section IX.A.1(a); Ex. 1006 at 1:67-2:34.) No outside signals are provided to the fuse circuit in McAdams and therefore, “during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltages.”

117. As shown in the demonstrative below, the inclusion of the diode in the circuit of McAdams based on Uda does not cause the circuit in the McAdams-Uda combination to receive any inputs from outside of the circuit illustrated. As further

discussed above with respect to claim element 1(g), the inclusion of the diode ensures the same operation discussed above when power is supplied to the latch (i.e., node 14 is at VCC if fuse 10 is not blown, whereas node 14 is at VSS if fuse 10 is blown).



(*Id.* at FIG. 1 (annotated).)

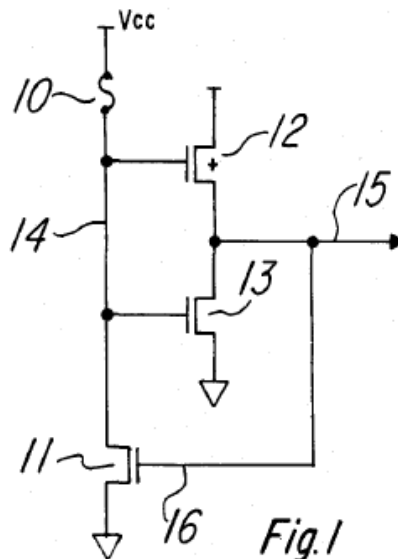
118. Therefore, the McAdams-Uda combination discloses or suggests “wherein during operation the voltage on the terminal T1 is completely determined

by the state of the programmable element and the voltages on the first and second terminals.”

3. Claim 3

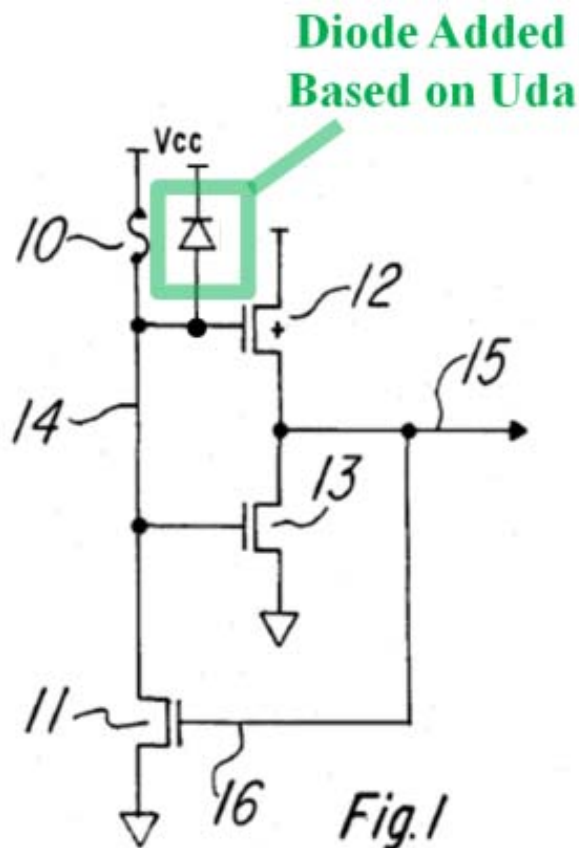
a) “The programmable latch of claim 1 wherein the latch does not receive any latch initialization signal from outside the latch.”

119. In my opinion, McAdams in view of Uda discloses or suggests this feature. As shown in figure 1 of McAdams below, the fuse circuit (“programmable latch”) of McAdams does not receive any inputs from outside of the circuit illustrated and the state of the latch is completely determined by the state of the fuse 10 and the voltages on the Vcc and Vss terminals. (See my discussion above in Section IX.A.2; Ex. 1006 at FIG. 1.)



(Ex. 1006 at FIG. 1.)

120. Therefore, McAdams discloses “wherein the latch does not receive any latch initialization signal from outside the latch.” Further, as shown in the demonstrative below, the inclusion of the diode in the circuit of McAdams based on Uda does not cause the circuit in the McAdams-Uda combination to receive any inputs from outside of the circuit illustrated. Therefore, the McAdams-Uda combination discloses or suggests “wherein the latch does not receive any latch initialization signal from outside the latch” for the same reasons discussed above with respect to claim 2. (See my discussion above in Section IX.A.2.)



(Ex. 1006 at FIG. 1 (annotated).)

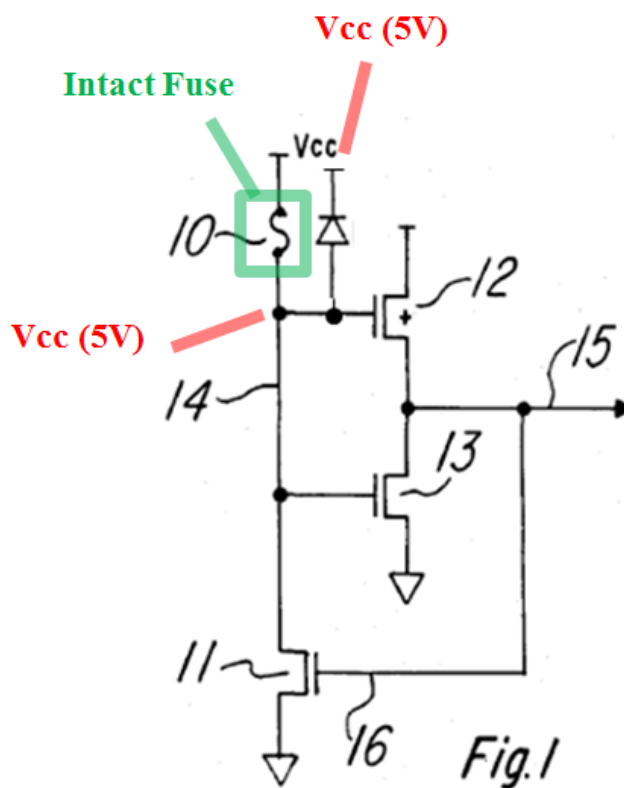
4. Claim 4

a) “The programmable latch of claim 1 wherein no current flows through the diode during normal operation of the latch, but when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values.”

121. In my opinion, McAdams in view of Uda discloses or suggests this feature. In order for current to flow through the diode included in the McAdams-Uda combination, the diode must be in the “forward bias” state, i.e., the voltage on the anode of the diode must be greater than the voltage on the cathode of the diode by at least the threshold voltage of the diode.

122. When power is applied to the fuse circuit (“programmable latch”) during normal operation of the latch in the McAdams-Uda combination, the first terminal is connected to Vcc, which corresponds to 5V. (Ex. 1006 at 2:2-3, 2:8-9, “During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v”.) In this scenario, the diode is not in a “forward bias” state and thus no current flows through the diode. In particular, as shown in the demonstrative below, when the fuse 10 is intact, the fuse provides an electrical path from the “first terminal” (Vcc) to the node 14 and therefore the voltage at node 14 is at Vcc (5V). As such, the voltage at both the anode (node 14) and the cathode (first terminal) of the diode is

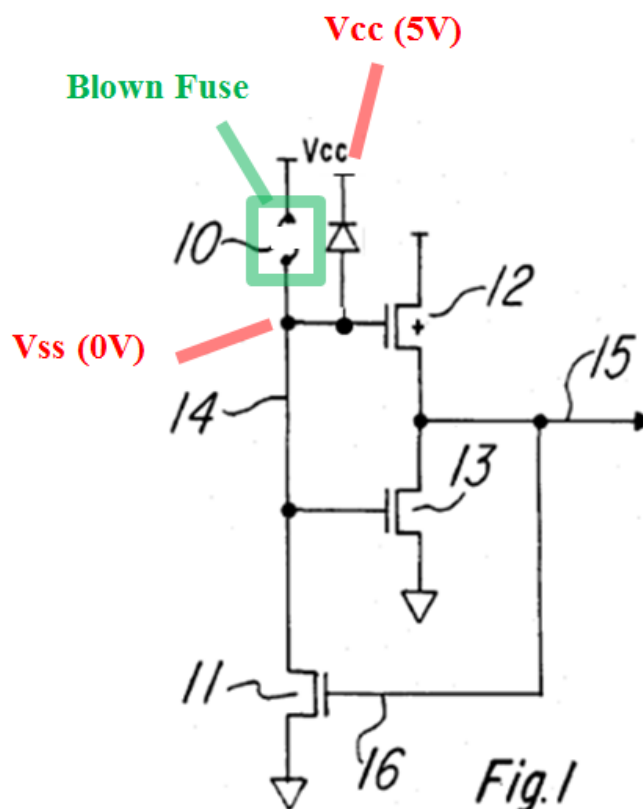
Vcc or 5V. Therefore, a person of ordinary skill in the art would have understood that the voltage at the anode of the diode (5V) does not exceed the voltage at the cathode of the diode (also 5V) by at least a threshold voltage of the diode and no current flows through the diode.



(Ex. 1006 at FIG. 1 (annotated).)

123. Similarly, during operation of the latch when the fuse has been blown, node 14 is pulled low to ground (Vss) by the transistor 11. (See my discussion above in Section IX.A.1(a).) As such, the voltage on the anode of the diode (node 14) is Vss (0V) and the voltage on the cathode of the diode (first terminal) is Vcc

(5V). Therefore, the voltage at the anode of the diode (0V) does not exceed the voltage at the cathode of the diode (5V) by at least a threshold voltage of the diode and no current flows through the diode.



(Ex. 1006 at FIG. 1 (annotated).)

124. As demonstrated above, when power is applied to the programmable latch of the McAdams-Uda combination (i.e., during normal operation), no current flows through the diode regardless as to whether or not the fuse has been blown. Therefore, the McAdams-Uda combination discloses “wherein no current flows through the diode during normal operation of the latch.”

125. As disclosed by McAdams, when the power is off, the power supply voltage V_{cc} is at 0V (ground). (Ex. 1006 at 2:8-9 (“During power-up of the supply voltage V_{cc} as V_{cc} goes from zero to +5 v”).)) As I discussed above with respect to claim element 1(g), when the power is off, the diode in the combined McAdams-Uda circuit will not allow the voltage at node 14 to exceed 0V by more than a threshold voltage of the diode. (See my discussion above at Section IX.A.1(g). This is because if the voltage on the anode of the diode (node 14) were more than a threshold voltage above the voltage at the cathode of the diode (0V), the threshold voltage of the diode would be exceeded and the diode would turn on, thereby causing current to flow through the diode from node 14 to ground. Such current flow would continue until the voltage across the diode becomes less than the threshold voltage and the diode turns off. (See my discussion above in Section V.C.)

126. Therefore, the combined McAdams-Uda circuit discloses or suggests that when the power is off, V_{cc} is at 0V, and current flows through the diode if the voltage on node 14 (“terminal T1”) exceeds the threshold voltage of the diode (“when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values”). (See my discussion

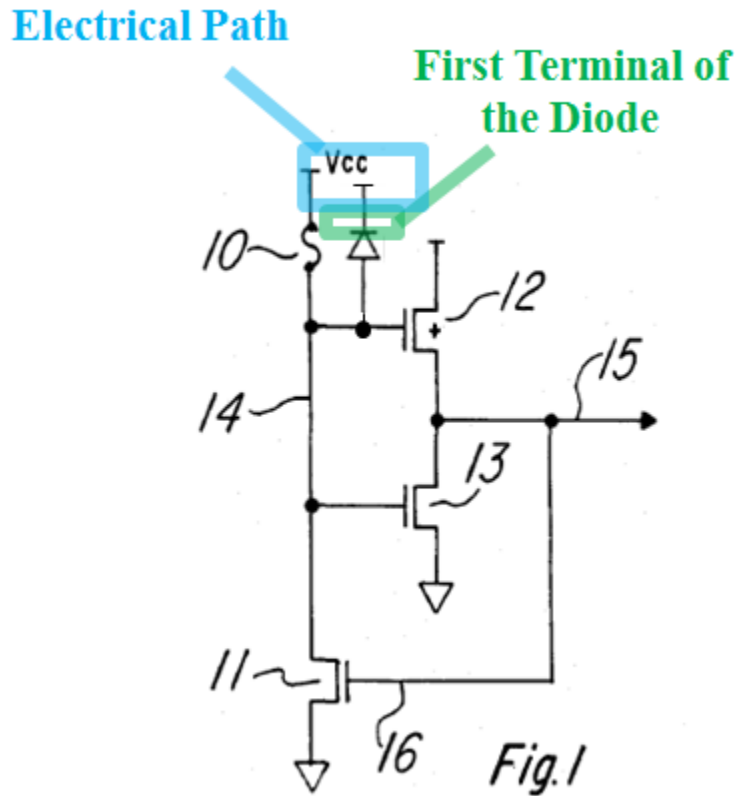
above in Section IX.A.1(g) describing that the “predetermined range of values” is the range of voltages less than the diode threshold voltage.)

5. Claim 5

a) “The programmable latch of claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.”

127. In my opinion, McAdams in view of Uda discloses or suggests this feature. As shown in the demonstrative below, the diode of the McAdams-Uda combination has a first terminal corresponding to the cathode of the diode, which is coupled to the supply node Vcc. As disclosed by McAdams, when power is not applied to the fuse circuit, the power supply node Vcc is at 0V. (Ex. 1006 at 2:8-9 (“During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v”.)) Therefore, a person of ordinary skill in the art would have understood that McAdams necessarily discloses an electrical path from the terminal marked as Vcc to a ground terminal because the voltage at the terminal marked Vcc is at 0V when power is not supplied to the fuse circuit. Accordingly, a person of ordinary skill in the art would have understood that when power is not supplied to the fuse circuit, there is an electrical path from the cathode of the diode (“first terminal of the

diode”) to a “ground terminal” because the voltage on the cathode of the diode is 0V.



(*Id.* at FIG. 1 (annotated).)

128. Further, as shown in the demonstrative above, the first terminal of the diode is coupled to Vcc, and therefore, there is necessarily “a first electrical path interconnecting a first terminal of the diode and a ground terminal” as McAdams discloses that the terminal Vcc is at ground when power is not supplied to the fuse circuit.

129. In my opinion, the McAdams-Uda combination also discloses or suggests “wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode.” As disclosed by McAdams, during normal operation (e.g. when power is supplied to the fuse circuit), Vcc is at 5V. (Ex. 1006 at 2:8-9, “During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v”.) As I discussed above with respect to claim 4, when the voltage at the cathode of the diode is at +5V during normal operation, the diode is off as the anode of the diode is either at 0V or +5V depending on the state of the fuse. (See my discussion above in Section IX.A.4.) As such, a person of ordinary skill in the art would have understood that the McAdams-Uda combination discloses that during normal operation the cathode of the diode (“first terminal of the diode”) is charged to +5V (“is charged to a voltage that turns off the diode”).

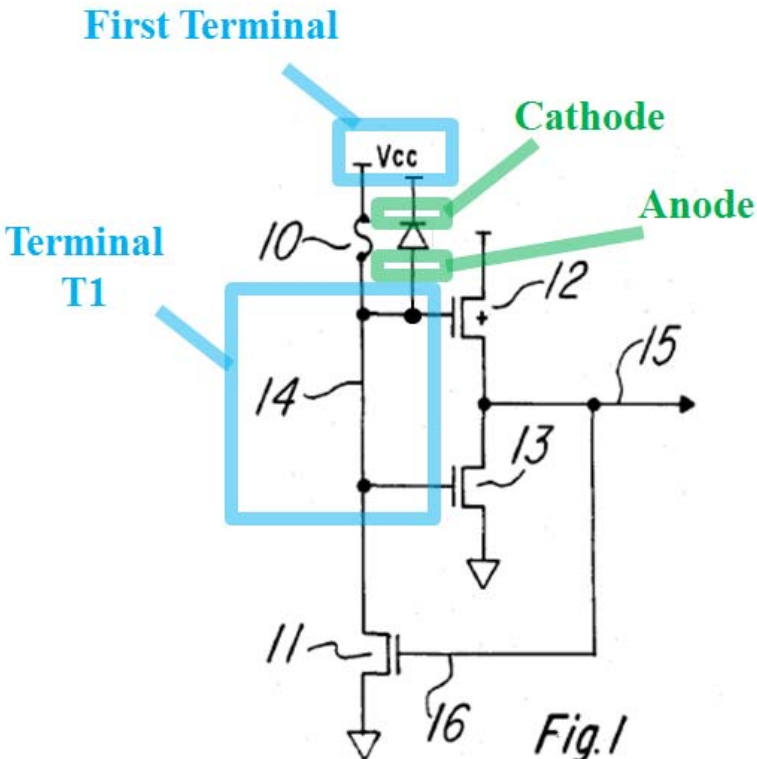
130. Additionally, as discussed above, when the power is off in the McAdams-Uda combination, the Vcc node is at 0V, and therefore there is necessarily a “first electrical path” that connects the Vcc node to a ground terminal. Because the Vcc node is grounded and the cathode of the diode is coupled to Vcc, the first terminal of the diode (i.e., the cathode of the diode) will be discharged to ground through the electrical path (i.e., the path that connects the cathode to ground through the Vcc node) when the power is off. Therefore, the

McAdams-Uda combination also discloses or suggests that “when the power is off the first terminal of the diode is discharged through said first electrical path” as recited in claim 5.

6. Claim 8

a) “The programmable latch of claim 1 wherein the diode has one terminal connected to the terminal T1, and the diode has another terminal connected to the first terminal.”

131. In my opinion, McAdams in view of Uda discloses or suggests this feature. As shown in the demonstrative below, the diode in the McAdams-Uda combination has one terminal (the anode) connected to node 14, which corresponds to “terminal T1.” (*See* my discussion above in Sections IX.A.1(d),(g).) The diode also has another terminal (the cathode) connected to Vcc, which corresponds to the “first terminal” recited in claim 1 above. (*See* my discussion above in Sections IX.A.1(b),(g).)



(Ex. 1006 at FIG. 1 (annotated).)

132. Therefore, in my opinion, the McAdams-Uda combination discloses or suggests a programmable latch “wherein the diode has one terminal connected to the terminal T1, and the diode has another terminal connected to the first terminal” as recited in claim 8.

7. Claim 9

- a) “The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,”

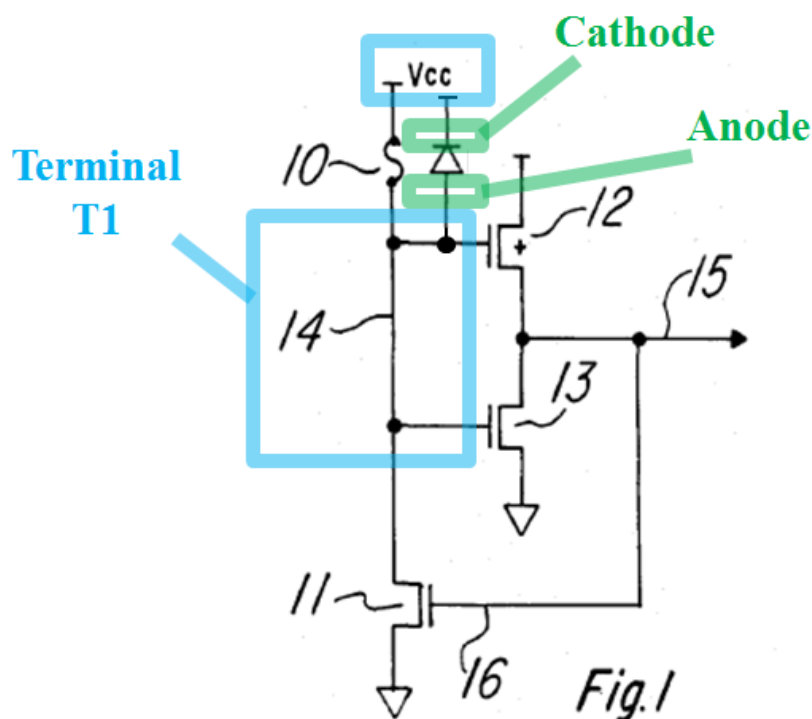
133. In my opinion, McAdams in view of Uda discloses or suggests this feature. For example, McAdams discloses that “the principal object of this invention [is] to provide improved fuse circuits exhibiting a low current drain for use in semiconductor integrated circuits such as memory or microcomputer devices, particularly CMOS devices with low standby power dissipation and minimum complexity.” (Ex. 1006 at 1:33-38.) McAdams further discloses that “[t]his invention relates to semiconductor integrated circuit devices, and more particularly to fuse circuits of the type used in VLSI CMOS semiconductor memory devices or the like.” (*Id.* at 1:5-8.)

134. Therefore, a person of ordinary skill in the art would have understood that McAdams discloses that the disclosed fuse circuit (“latch”) (*see* my discussion above in Section IX.A.1(a)) is used in an integrated circuit device such as a memory device (“the latch is an integrated circuit or part of an integrated circuit”).

- b) “wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.”

135. In my opinion, McAdams in view of Uda discloses or suggests this feature. For example, as shown in the demonstrative below, the anode (“one terminal”) of the diode in the McAdams-Uda combination is connected to node 14

(“terminal T1”) and the cathode (“another terminal”) of the diode is connected to Vcc.



(Ex. 1006 at FIG. 1 (annotated).)

136. As I discussed above with respect to claim element 1(b), Vcc is a “supply voltage” that is supplied when power is applied to the circuit of figure 1. (*Id.* at 2:2-3 (“series circuit is connected between a supply voltage Vcc and Vss”), 2:8-9 (“During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v”), 3:24-26 (“wherein said one of the first and second terminals of said power supply is a positive voltage and said other is ground”), 4:20-22 (“a power supply having a first terminal at a positive voltage and a second terminal at a ground

potential”).) In the example embodiment of McAdams, V_{cc} is at +5 V after power-up of the latch and therefore constitutes “non-ground power-supply voltage.” A person of ordinary skill in the art would have understood that a power supply voltage for an integrated circuit is commonly provided via an external pin and therefore would have understood that the V_{cc} power-supply voltage in McAdams would have been received “from an external pin of the integrated circuit” on which the fuse circuit is located.

137. To the extent that McAdams does not disclose that the V_{cc} terminal receives the non-ground supply voltage from an external pin, a person of ordinary skill in the art would have been motivated to provide the +5V supply voltage V_{cc} from an external pin. McAdams discloses that the power supply has a first terminal and a second terminal, where one of the first and second terminals is a positive voltage and the other is ground. (*Id.* at 3:3, 3:24-29.) A person of ordinary skill in the art would have understood that supply voltages for integrated circuits are commonly supplied via pins on the integrated circuit that permit connectivity to circuitry and voltage sources outside of the integrated circuit. (*See, e.g.,* Ex. 1007 at FIG. 1.)

138. Indeed, Keeth (Ex. 1008) discloses that “[a]s one example of an integrated circuit (IC) having a power supply circuit, consider a dynamic random

access memory (DRAM) formed as an integrated circuit.” (Ex. 1008 at 1:15-17.)⁸ Keeth explains that “[s]uch an IC conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts.” (*Id.* at 1:17-19.) Because Keeth discloses that “ V_{CCX} is applied with a voltage in a range including 5 volts measured relative to a ground contact,” the power signal V_{CCX} described by Keeth is a non-ground power supply voltage. (*Id.* at 1:19-21.) Keeth’s disclosure regarding receiving an externally applied non-ground power supply voltage at a contact of an IC was known even at the time of Keeth, as it is found in the Background section of Keeth. (*Id.* at 1:15-19.) Furthermore, Uda (Ex. 1007) discloses an integrated circuit housed in a chip carrier, where the chip is connected to external CCB bumps (external pins). (Ex. 1007 at 8:6-67, FIG. 1.) A person of ordinary skill in the art would have understood that these external pins are used to provide all signals to the integrated chip, including power.

139. As demonstrated above, Keeth supports my understanding that a person of ordinary skill in the art would have been motivated to provide the external non-ground power supply to a circuit such as that of the McAdams-Uda

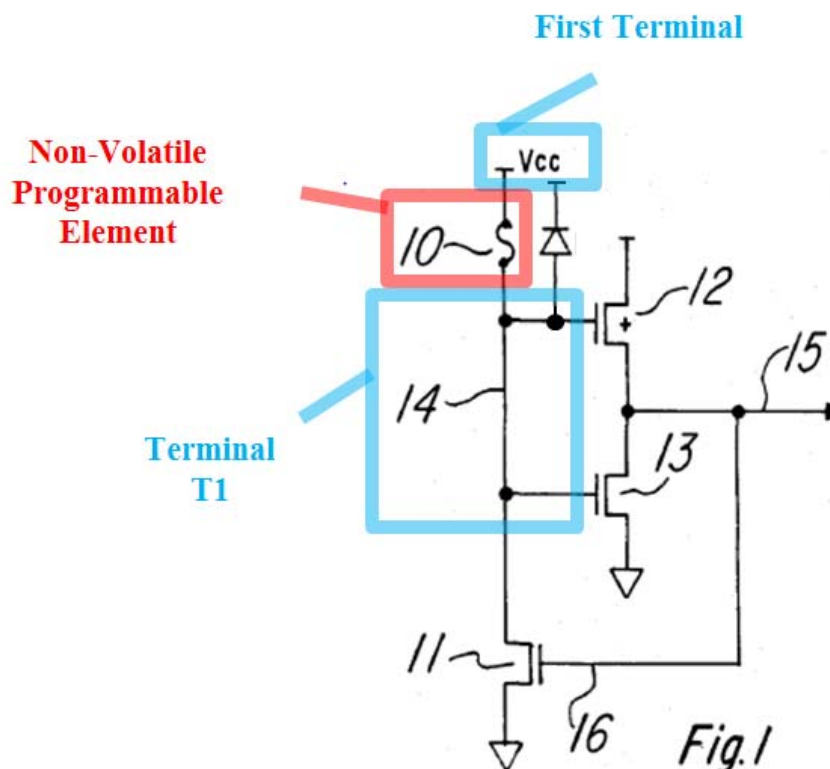
⁸ I am referring to Keeth (Ex. 1008) to show what a person of ordinary skill in the art would have known at the time of the alleged invention.

combination using an external pin of the integrated circuit device upon which the circuit is included. For at least these reasons, in my opinion, the McAdams-Uda combination discloses or suggests “the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.”

8. Claim 10

- a) “The programmable latch of claim 1 wherein: the programmable element is a fuse connected to and between the terminal T1 and the first terminal;”

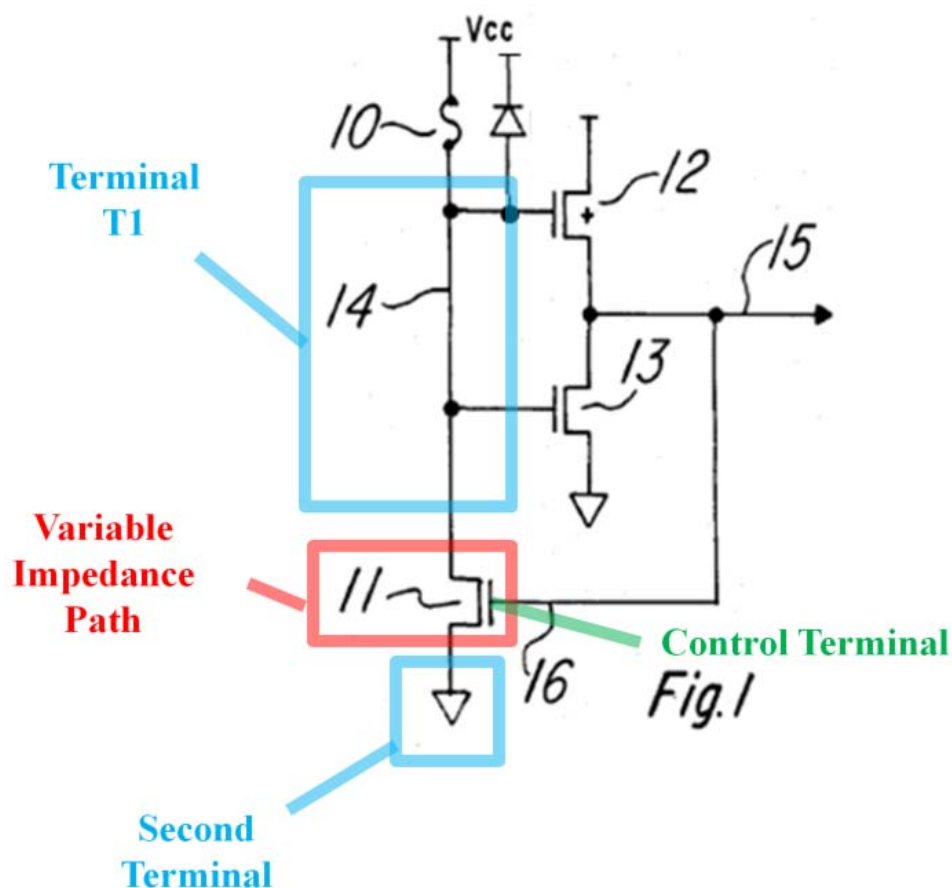
140. In my opinion, McAdams in view of Uda discloses or suggests this feature. As demonstrated above with respect to claim element 1(e), McAdams discloses a fuse 10 that constitutes a “programmable element,” where the fuse 10 is connected between node 14 (“terminal T1”) and Vcc (“the first terminal”).) (*See* my discussion above in Section IX.A.1(e).) Therefore, the McAdams-Uda combination discloses or suggests “the programmable element is a fuse connected to and between the terminal T1 and the first terminal.”



(Ex. 1006 at FIG. 1 (annotated).)

- b) “the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal;”

141. In my opinion, McAdams in view of Uda discloses or suggests this feature. As demonstrated with respect to claim element 1(f) above, the NMOS transistor 11 highlighted in the McAdams-Uda combination below is a “variable-impedance electrical path.” (See my discussion above in Section IX.A.1(f).)

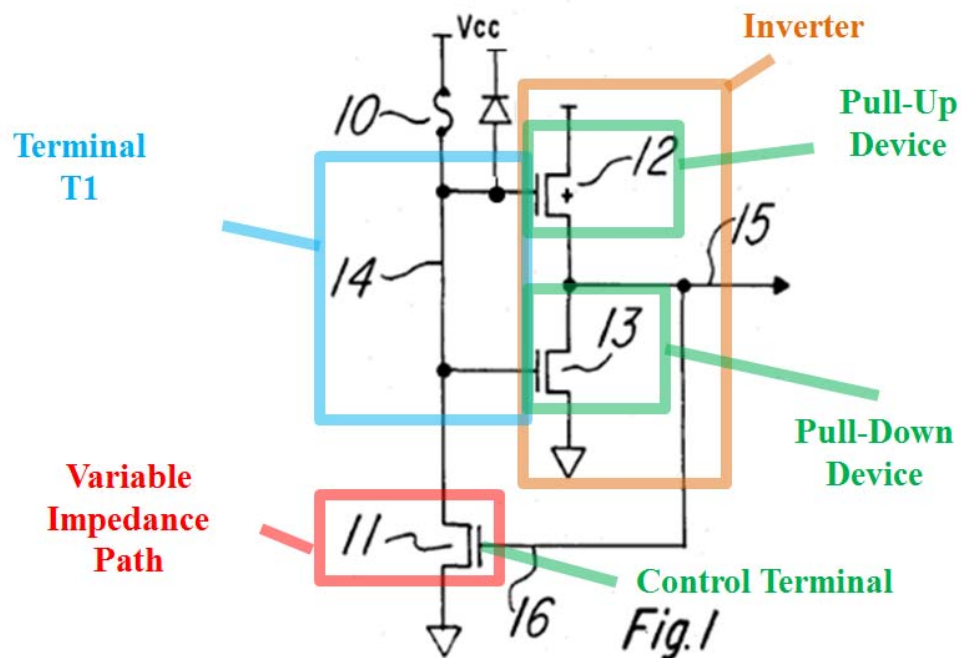


(Ex. 1006 at FIG. 1 (annotated).)

142. As shown in the demonstrative above, the NMOS transistor 11 (“variable-impedance electrical path”) is coupled between node 14 (“terminal T1”) and Vss (“second terminal”) and therefore is “connected to and between the terminal T1 and the second terminal.” Furthermore, a person of ordinary skill in the art would have understood that the gate of transistor 11 is used to control whether the transistor 11 is on or off, and therefore the gate of transistor 11 is a “control terminal.” (See my discussion above in Sections V.B, IX.A.1(f).)

- c) “the programmable latch further comprises an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.”

143. In my opinion, McAdams in view of Uda discloses or suggests this feature. For example, the McAdams-Uda combination discloses a programmable latch that includes an inverter, where the inverter is highlighted in orange in the demonstrative below.



(Ex. 1006 at FIG. 1 (annotated).)

144. As shown in the demonstrative above, the inverter includes P-channel (PMOS) transistor 12 (“pull-up device”) coupled between output 15 and V_{cc} , where, when the P-channel transistor 12 is on, it pulls the voltage at output node 15 up to 5V and therefore would be understood to operate as a “pull-up” transistor in the inverter. (See my discussion above regarding inverters in Section V.B.) Similarly, the inverter includes N-channel transistor 13 (“pull-down device”) coupled between output 15 and V_{ss} , where, when the N-channel transistor 13 is on, it pulls the voltage at output node 15 down to V_{ss} and therefore would be understood to operate as a “pull-down” transistor in the inverter. (*Id.*; Ex. 1006 at FIG. 1, 2:3-6.)

145. As also shown in the demonstrative above, both the P-channel transistor 12 (“pull-up device”) and the N-channel transistor 13 (“pull-down device”) are coupled to inverter input at node 14, which corresponds to “terminal T1” (“an inverter whose input is connected to the terminal T1”). (Ex. 1006 at FIG. 1, 2:3-6.) A person of ordinary skill in the art would have understood that the input of the inverter corresponds to the node that is coupled to the gates of both the PMOS and NMOS transistors in the inverter. (See Section V.B above.) Both the P-channel transistor 12 (“pull-up device”) and the N-channel transistor 13 (“pull-down device”) are also coupled to inverter output at node 15, which corresponds to

the input of the gate of transistor 11 (“an inverter ... whose output is connected to the control terminal of said transistor”). (Ex. 1006 at FIG. 1, 2:3-6.) A person of ordinary skill in the art would have understood that the output of the inverter is the node that is coupled to the drains of both the PMOS and NMOS transistors in the inverter. (See Section V.B above.) As is evident from the demonstrative above, both transistors 12 and 13 are connected to the inverter input at node 14 (“at least one of the pull-up and pull-down devices is connected to the inverter input”), and both transistors 12 and 13 are connected to the inverter output at node 15 (“both of the pull-up and pull-down devices are connected to the inverter output”).

146. Therefore, in my opinion, the McAdams-Uda combination discloses or suggests “an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.”

9. Claim 13

- a) “The programmable latch of claim 1 wherein: said predetermined range consists of all voltages below a predetermined value; and”

147. In my opinion, McAdams in view of Uda discloses or suggests this feature. As I discussed above with respect to claim element 1(g), the McAdams-Uda combination discloses “a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” (*See* my discussion above in Section IX.A.1(g).) Specifically, a person of ordinary skill in the art would have understood that when VCC is at 0V (i.e., “before power is supplied to the latch”), the diode in the combined McAdams-Uda circuit would not allow the voltage at node 14 to exceed 0 volts by more than a threshold voltage of the diode. (*Id.*) Therefore, a person of ordinary skill in the art would have understood that the McAdams-Uda combination discloses that the “predetermined range consists of all voltages below a predetermined value” where the predetermined value is the threshold voltage of the diode.

- b) “when the programmable element is conductive, the variable-impedance path is non-conductive.”

148. In my opinion, McAdams in view of Uda discloses or suggests this feature. As I discussed above in claim element 1(a), if the fuse in McAdams is not blown (“programmable element is conductive”) when power is applied to the circuit, the node 14 follows the power supply voltage Vcc, which turns on transistor 13. (Ex. 1006 at 2:8-15; *see* my discussion above in Section IX.A.1(a).) When transistor 13 turns on, any charge on the output node 15 is discharged,

pulling the output to V_{ss}. (Ex. 1006 at 2:8-15; *see* my discussion above in Section IX.A.1(a).) The V_{ss} voltage on the output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state (“the variable-impedance path is non-conductive”). (Ex. 1006 at 2:8-18.)

149. A person of ordinary skill in the art would have understood that the inclusion of the diode in the circuit of McAdams based on Uda does not alter this aspect of the operation of the fuse circuit in McAdams. Therefore, the McAdams-Uda combination discloses that the “when the programmable element is conductive, the variable-impedance path is non-conductive.”

B. Ground 2: McAdams in Combination with Uda and Keeth Discloses or Suggests Claims 5-7

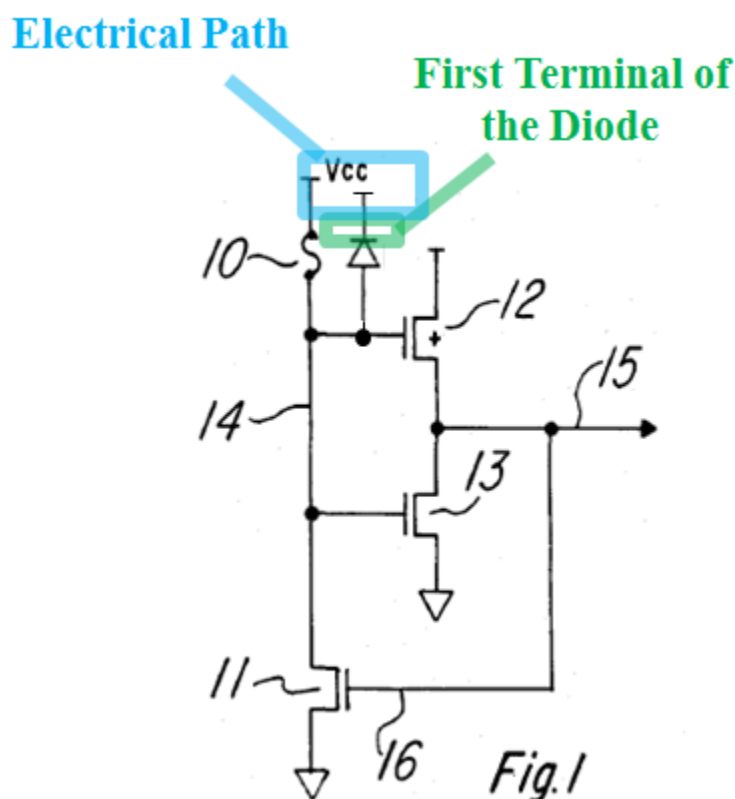
150. In my opinion, McAdams in combination with Uda and Keeth discloses or suggests all of the features of claims 5-7 of the '492 patent.

1. Claim 5

- a) “The programmable latch of claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.”

151. As I explained above with respect to claim 5 in Section IX.A.5, the McAdams-Uda combination discloses or suggests the features of claim 5.

Specifically, it is my opinion that the McAdams-Uda combination discloses an electrical path connecting the cathode of the diode (“first terminal of the diode”) with a ground terminal when power is not supplied to the fuse circuit because the terminal marked as Vcc in figure 1 of McAdams is 0V (i.e., ground voltage). (See my discussion above in Section IX.A.5.)



(Ex. 1006 at FIG. 1 (annotated).)

152. However, I have been asked to assume that the combination of McAdams and Uda does not explicitly or necessarily disclose or suggest “a first

electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.” Based on that assumption, it is my opinion that a person of ordinary skill in the art would have been motivated, based on Keeth, to include such a feature in the McAdams-Uda combination. Specifically, as I discussed below, a person of ordinary skill in the art would have been motivated to provide the Vcc voltage (as shown in the McAdams-Uda demonstrative above) from a power supply circuit, which would include a path from the Vcc terminal to a ground terminal.

153. At the time of the alleged invention of the '492 patent, it was well-known that memory devices could include an internal power supply generator that would generate an internal power supply from an external voltage supply. (Ex. 1008 at 1:17-35 (explaining that an integrated circuit memory (e.g., a DRAM) “conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts” that is then converted to an internal voltage V_{CCR}); Ex. 1012 at 1:19-23 (“by installing on-chip an internal power-supply voltage supplier, regardless of the external power-supply voltage a constant voltage is applied to the interior of the memory device.”).) When implementing the McAdams-Uda system, a skilled

person would have understood that McAdams and Uda do not expressly disclose details of the voltage supplies (e.g., V_{cc}) used therein. But because McAdams and Uda disclose semiconductor memory devices (Ex. 1006 at Abstract (“A fuse circuit as used in self-repairing **memory devices** or the like....”) (emphasis added); Ex. 1007 at 1:10-18 (“[T]he invention relates to a semiconductor integrated circuit device having a redundancy circuit arrangement such as a static RAM (random access **memory**)....”) (emphasis added), the skilled person would have understood that the voltages in their respective circuits (e.g., V_{cc} in figure 1 of McAdams and V_{EE} in figure 5 of Uda) could be provided from an internal power-supply generator. Therefore, a skilled person looking to implement the McAdams-Uda combination would have looked to references that disclose an internal power-supply generator. Accordingly, such a skilled person would have looked to Keeth because, as discussed below, Keeth discloses an internal power-supply generator for a memory device and also explains how its novel internal power-supply generator overcomes several problems of conventional designs for such circuits.

154. Keeth, like McAdams (Ex. 1006 at Abstract) and Uda (Ex. 1007 at 1:10-18), relates to memory circuits:

Circuit 30 is a circuit for performing an electrical function of IC 10. In various embodiments circuit 30 is an analog circuit, a digital circuit, or a combination of analog and digital circuitry.

Although the present invention is effectively applied where circuit 30 includes dynamic memory (DRAM), a static memory (SRAM), or a video memory (VRAM) having a serial port, the present invention can be beneficially and equivalently applied by a person of ordinary skill to integrated circuits in general, whether or not the integrated circuit is powered from a single power supply potential.

(Ex. 1008 at 4:12-22.)

155. Keeth discloses that an integrated circuit memory (e.g., a DRAM) “conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts.” (Ex. 1008 at 1:17-19.) This externally applied voltage (V_{CCX}) is converted by a power supply circuit to “an internal voltage V_{CCR} ,” which is used as the power supply for the memory circuits. (*Id.* at 1:31-34; *see also id.*, Abstract (“internal operating voltage, designated V_{CCR} ”), 6:19 (“Signal V_{CCR} . . . powers circuit 30,” where circuit 30 includes DRAM, SRAM, etc. (*id.* at 4:12-22).) But Keeth also discloses that the conventional power supply circuits for converting an external power supply voltage to an internal power supply voltage suffered from several problems:

The circuits that make up the conventional 3.3 volt DRAM include a power supply circuit that receives V_{CCX} and provides an optimal value for an internal voltage V_{CCR} . The value of V_{CCR} cannot be obtained by measurement after the

DRAM has been encapsulated. Process variation from lot to lot and from device to device in an extreme case can produce a percentage of DRAMs each having a power supply circuit wherein the transition points for the piecewise linear function of VCCR as a function of VCCX vary widely from design values. This variation limits the effectiveness of DRAM testing, especially burn-in screening for the removal of weak parts from inventory to be sold.

In addition to the lack of burn-in screening effectiveness, testing for purposes of guaranteeing operating specifications is also made difficult by conventional DRAM power supply circuitry. The conventional power supply circuit provides a regulated value for VCCR over a wide range of values of VCCX. Since many operating specifications are affected by VCCR, the fact that VCCR is not measurable in an encapsulated DRAM makes selection of a guaranteed specification a difficult empirical exercise. To avoid a large number of devices found to not conform to the guaranteed specification after delivery, manufacturers pad the specification to allow for process variation, testing tolerances, and temperature variation, to name a few significant variables. If on the other hand, the padded specification is too conservative, many superior devices will be sold as if they were lower grade devices and the premium price for superior devices cannot be collected.

(*Id.* at 1:31-60.)

156. To overcome these deficiencies, Keeth discloses a novel circuit (voltage reference 100) in FIG. 3 that receives an external power signal V_{CCX} and provides the internal power supply voltage V_{CCR} . (*See, e.g., id.* at 5:58-62, FIG. 3.)

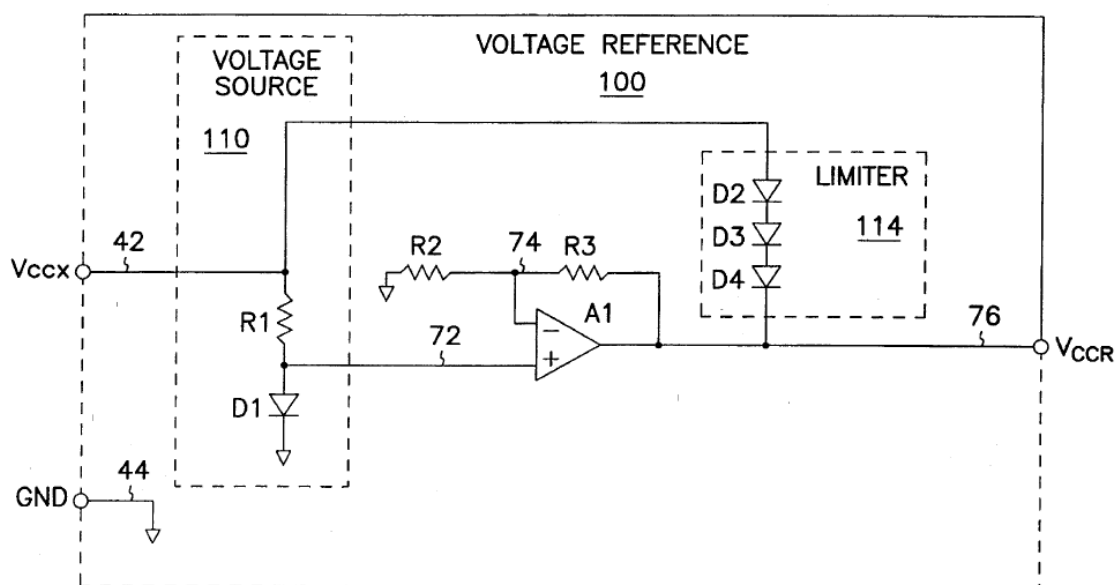


FIG. 3

(*Id.* at FIG. 3.)

157. As disclosed by Keeth, the voltage reference 100 achieves a “piecewise linear relationship between V_{CCX} and V_{CCR} ” that alleviates shortcomings of similar prior art circuits. (*Id.* at 4:37-5:62.) Specifically, the voltage reference 100 operates over three segments (i.e., three ranges of input values for V_{CCX}) and “[w]hen used in a dynamic random access memory integrated

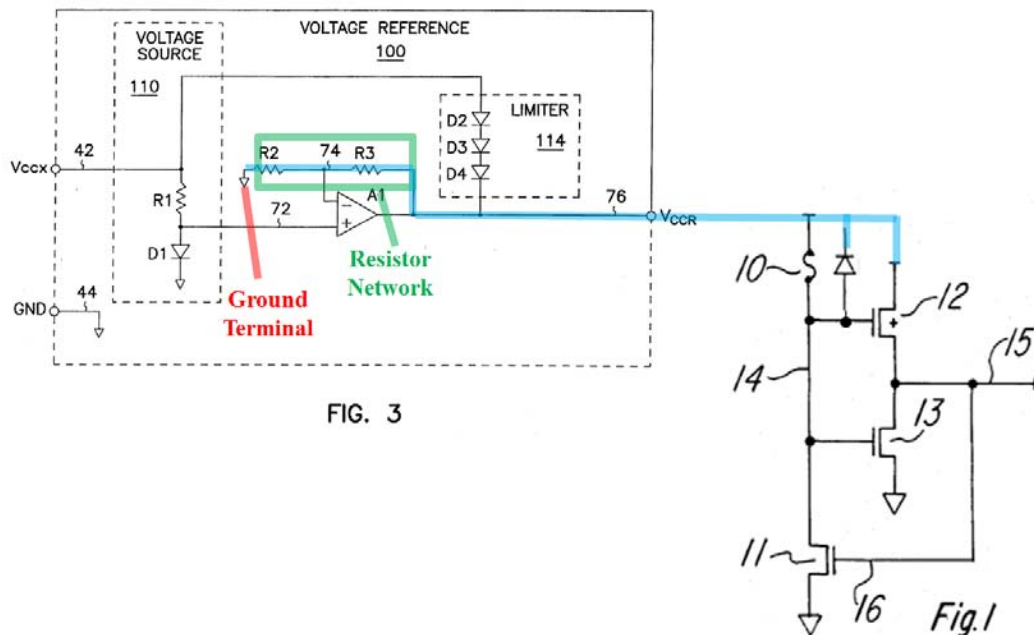
circuit, operation in the first segment provides data retention at low power consumption. Operation in the second segment supports speed grading individual devices with a margin for properly stating memory performance specifications. Operation in the third segment supports screening at elevated temperatures for identifying weak and defective memory devices.” (*Id.* at Abstract; *see also id.*, 4:37-5:62.) According to Keeth, the voltage reference 100 prevents the “useful life of the IC” from being shortened, increases “[s]ystem reliability,” and allows “improved integrated circuit testing and screening.” (*Id.* at 5:51-54, Abstract; *see also id.*, 4:37-5:62.)

158. A person of ordinary skill in the art would have recognized and appreciated the advantages of the internal power supply generator of Keeth. Indeed, given the above-noted advantages associated with the voltage reference 100, it is my opinion that a person of ordinary skill in the art would have been motivated to combine the teachings of McAdams, Uda, and Keeth such that the power supply V_{cc} in figure 1 of McAdams is provided by a circuit similar to voltage reference 100, which receives an external power supply (e.g., V_{CCX}) and converts it to an internal power supply voltage (e.g., V_{CCR}). When implementing the McAdams-Uda system, a person of ordinary skill in the art would have looked to teachings associated with internal power supply circuits, such as those disclosed

by Keeth, given that McAdams and Uda do not expressly disclose details of the voltage supplies used therein. Having looked to Keeth, the skilled person would have been motivated to combine its teachings with the McAdams-Uda combination because, for example, the voltage reference 100 prevents the “useful life of the IC” from being shortened, increases “[s]ystem reliability,” and allows “improved integrated circuit testing and screening.” (Ex. 1008 at 5:51-54, Abstract; *see also id.*, 4:37-5:62.) Indeed, the combination of Keeth’s voltage reference 100 and the McAdams-Uda circuit would have been nothing more than the combination of familiar elements (e.g. the voltage reference 100 of Keeth and the McAdams-Uda memory device) according to known methods (providing an electrical connection between the Vcc node in the McAdams-Uda circuit and the V_{CCR} node in the voltage reference 100) that would have yielded an expected result (the power supply in the McAdams-Uda circuit is provided by the voltage reference 100 of Keeth).

159. In my opinion, the combined McAdams-Uda-Keeth system set forth above discloses or suggests the features of claim 5. Specifically, as I discussed above, in the McAdams-Uda-Keeth system, the Vcc terminal in figure 1 of McAdams (as modified by Uda) would be connected to the V_{CCR} terminal in figure 3 of Keeth. It is my opinion that any modifications necessary to ensure that

Keeth's internal power supply circuit would work on an integrated circuit with the McAdams-Uda latch circuit would have been apparent to, and within the capabilities of, a person of ordinary skill in the art. I have created the demonstrative below to show that connection.



(Ex. 1006 at FIG. 1 and Ex. 1008 at FIG. 3 (annotated and modified to illustrate a non-limiting configuration of the McAdams-Uda-Keeth combination).)

160. As shown in the demonstrative above, the V_{CCR} terminal is connected to the ground terminal through a resistor network that includes resistors R2 and R3. (Ex. 1008 at FIG. 3.) As also shown in the demonstrative above, the anode of the diode is coupled to node 14, while the cathode of the diode is coupled to V_{cc} , which in turn is coupled to ground via the terminal V_{CCR} and the resistor network.

Accordingly, a person of ordinary skill in the art would have understood that the McAdams-Uda-Keeth combination discloses an electrical path connecting the cathode of the diode (“first terminal of the diode”) in the McAdams-Uda combination with a ground terminal through a resistor network (R2 and R3 like in Keeth).

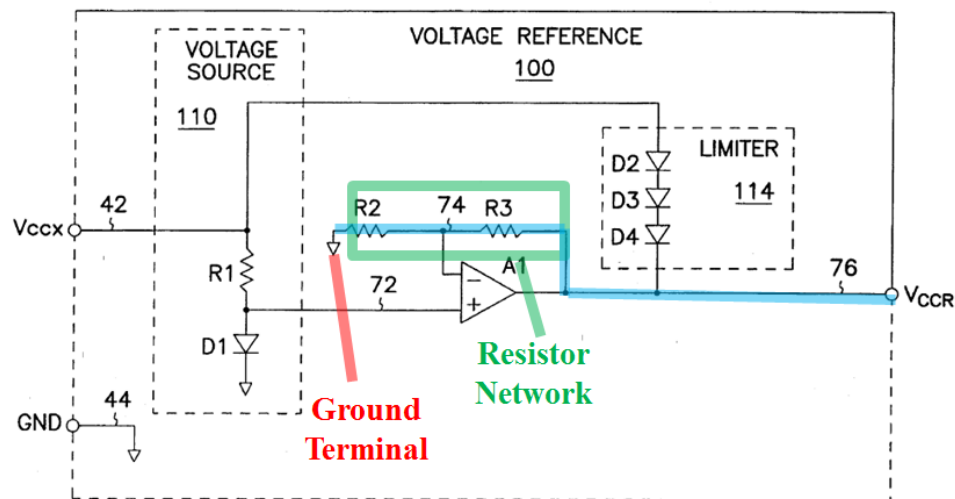


FIG. 3

(Ex. 1008 at FIG. 3 (annotated).)

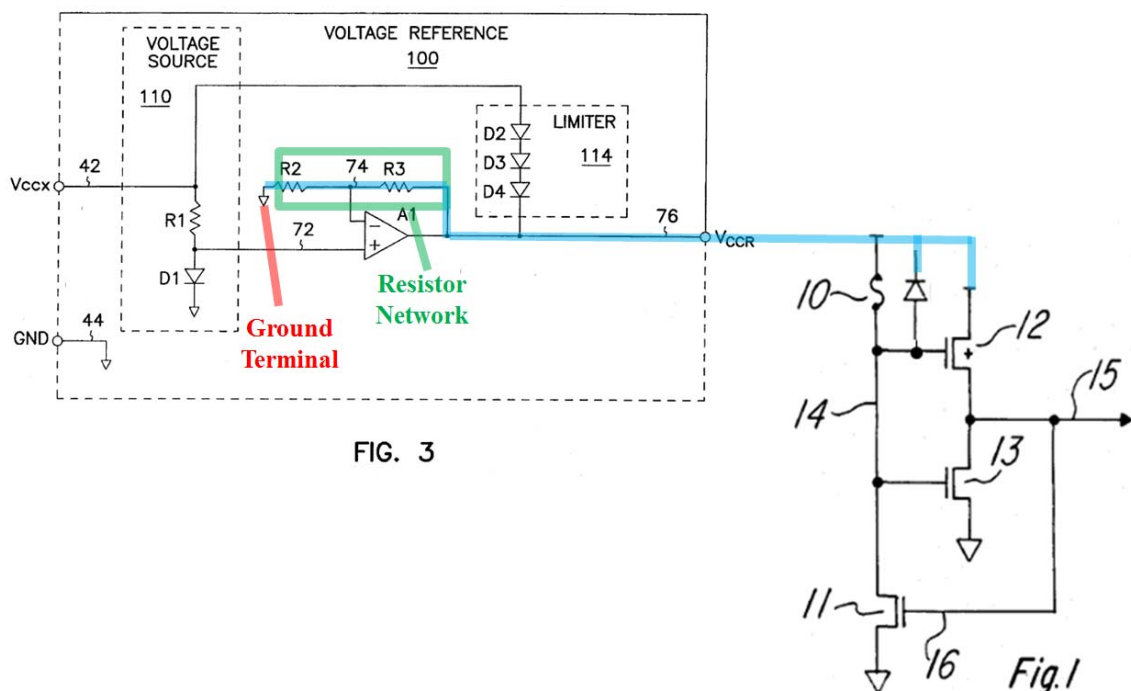
161. Additionally, as discussed above, when the power is off in the McAdams-Uda-Keeth combination, the Vcc node remains connected to ground via the “first electrical path” highlighted in blue in the demonstrative above. Because the Vcc node is grounded and the cathode of the diode is coupled to Vcc (and hence coupled to ground as well), the first terminal of the diode (i.e., the cathode of

the diode) will be discharged to ground through the electrical path (highlighted in blue above) when the power is off.

2. Claim 6

- a) “The combination of claim 5 wherein the first electrical path is a resistor or a resistor network.”

162. In my opinion, the combined McAdams-Uda-Keeth system discloses or suggests this limitation. As I discussed above for claim 5 with respect to the McAdams-Uda-Keeth combination, in the modified system the disclosed “first electrical path” includes resistors R2 and R3, and thus includes “a resistor or a resistor network.” (See my discussion above in Section IX.B.1.)



(Ex. 1006 at FIG. 1 and Ex. 1008 at FIG. 3 (annotated and modified to illustrate a non-limiting configuration of the McAdams-Uda-Keeth combination).)

3. Claim 7

- a) “The combination of claim 5 wherein the first electrical path is part of a reference voltage generator whose output is connected to the diode's first terminal.”

163. In my opinion, the combined McAdams-Uda-Keeth system discloses or suggests this limitation. As I discussed above for claim 5 with respect to the McAdams-Uda-Keeth combination, the modified system discloses that the output V_{CCR} of voltage reference 100 (“reference voltage generator”) is connected to the cathode of the diode (“the diode’s first terminal”) in the McAdams-Uda

combination. (See my discussion above in Section IX.B.1.) Therefore, the “first electrical path” (annotated in blue below) is part of a reference voltage generator (voltage reference 100).

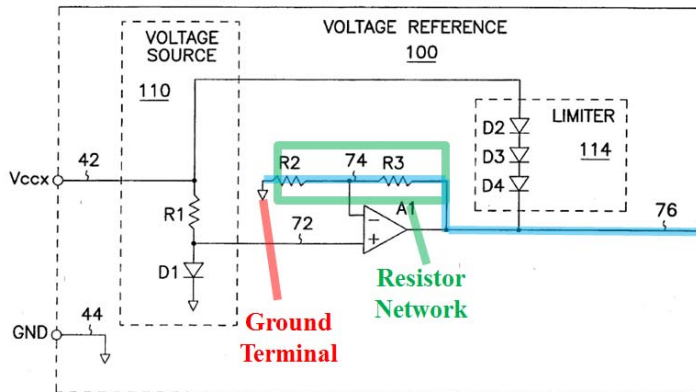
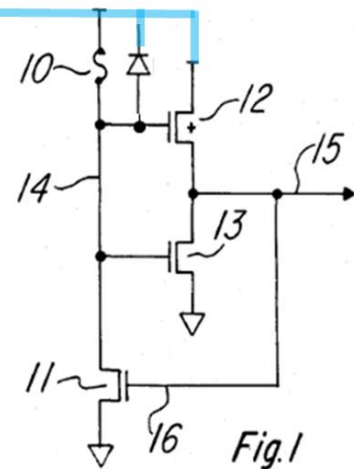


FIG. 3



(Ex. 1006 at FIG. 1 and Ex. 1008 at FIG. 3 (annotated and modified to illustrate a non-limiting configuration of the McAdams-Uda-Keeth combination).)

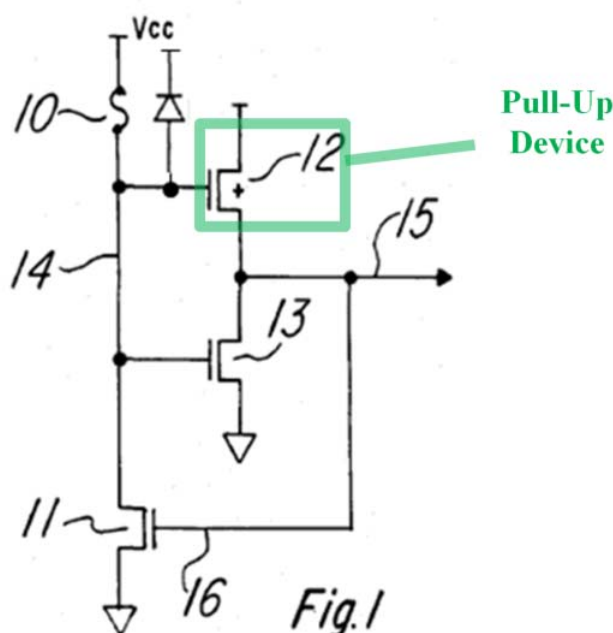
C. Ground 3: McAdams in Combination with Uda and Weste Discloses or Suggests Claims 11 and 12

164. In my opinion, McAdams in combination with Uda and Weste discloses or suggests all of the features of claims 11 and 12 of the '492 patent.

1. Claim 11

- a) “The programmable latch of claim 10 wherein one of the pull-up and pull-down devices is a MOS transistor formed in a first semiconductor region of a first conductivity type, and the diode comprises a second semiconductor region of a second conductivity type forming a junction with the first semiconductor region, the second region being connected to the terminal T1.”

165. In my opinion, McAdams in view of Uda and Weste discloses or suggests this feature. As I explained above, the inverter shown in figure 1 of McAdams includes both a PMOS pull-up transistor and an NMOS pull-down transistor. (*See* my analysis above in Section IX.A.8.) As shown in the demonstrative below, the “pull-up device” in the inverter of the McAdams-Uda combination is a P-channel (PMOS) transistor. (Ex. 1006 at 1:67-2:7.) Therefore, the McAdams-Uda combination discloses that “one of the pull-up and pull-down devices is a MOS transistor.”

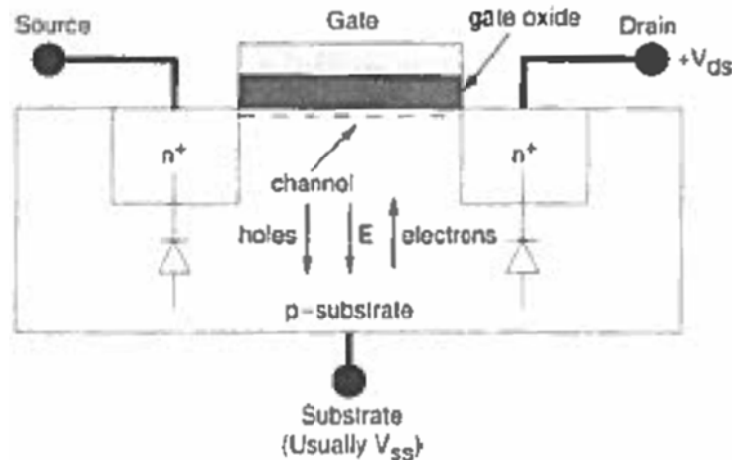


(Ex. 1006 at FIG. 1 (annotated to illustrate a non-limiting implementation of the McAdams-Uda combination).)

166. While neither McAdams nor Uda discloses how the P-channel transistor 12 is formed, a person of ordinary skill in the art would have known that P-channel transistors are formed such that the source and drain are p-type doped regions in an n-type substrate or n-well. Weste, which is a treatise in the field of semiconductor integrated circuit devices, provides specific disclosure as to how such transistors are formed. (Ex. 1009 at 1, 379, 625.) Weste describes the technology and construction of semiconductor circuit elements used in McAdams

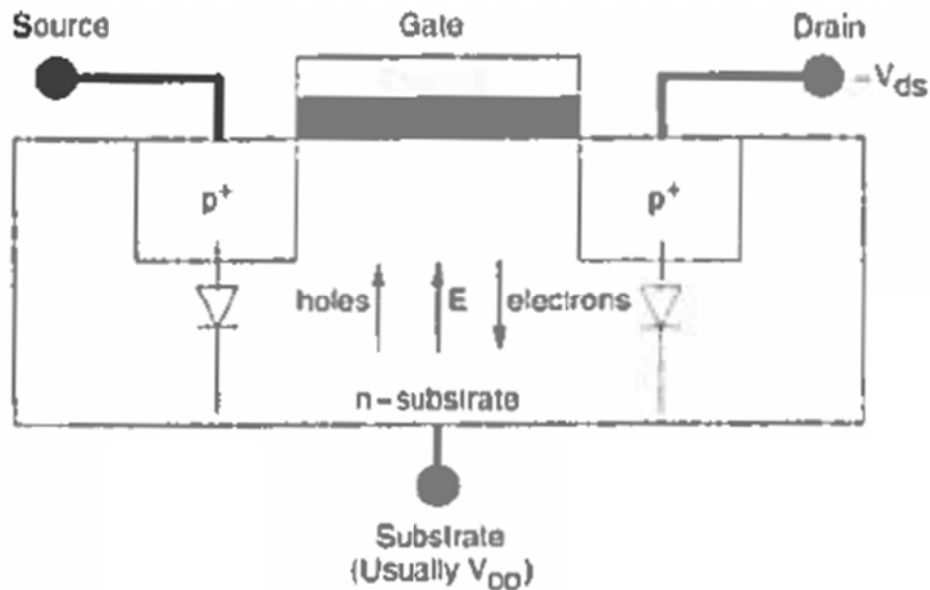
and Uda, such as NMOS and PMOS transistors, diodes, latches, and fusible links. (See, e.g., *id.* at 19-21, 41-51, 91-93, 117-130, 318-322, 395-400.)

167. For example, Weste discloses how both NMOS and PMOS transistors are constructed on a semiconductor substrate, as shown below. Weste explains that an NMOS transistor is formed by diffusing two n^+ doped regions (corresponding to the source and drain) in a moderately doped p-type region (e.g., a p-substrate). (*Id.* at 43, FIG. 2.3.)



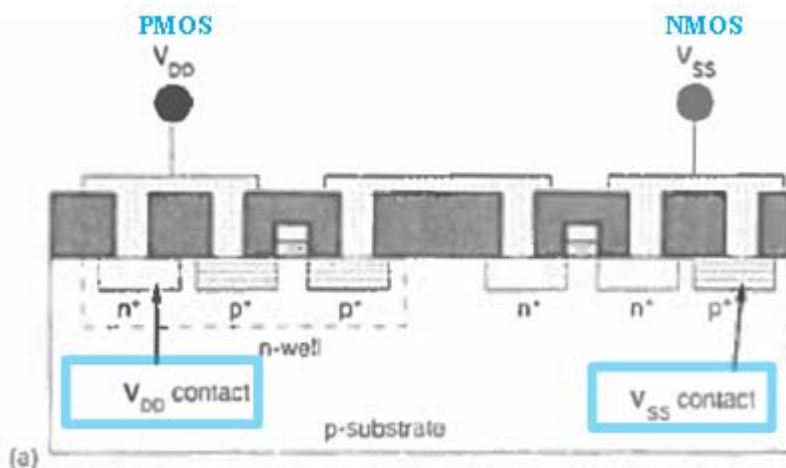
(*Id.* at 43 (FIG. 2.3, showing an NMOS transistor).)

168. Similarly a PMOS transistor is formed by diffusing two p^+ regions (corresponding to the source and drain) into a moderately doped n-type region (e.g., an n-substrate). (See *id.* at 47, FIG. 2.6.)



(*Id.* at 47 (FIG. 2.6, showing a PMOS device).)

169. A person of ordinary skill in the art would have understood that when building circuits that include both PMOS and NMOS transistors, CMOS technology is used as it is “the leading VLSI systems technology.” (*Id.* at 117.) A person of ordinary skill in the art would also have known at the time of the alleged invention as well as today that the most commonly used CMOS process is the n-well CMOS process. In an n-well process, the NMOS transistors are built in the native p-substrate, whereas a separate n-well is created inside the p-substrate to mimic the function of an n-substrate for the PMOS transistors. (*Id.*) In such an n-well CMOS process, an inverter (which includes an NMOS transistor and a PMOS transistor sharing their drain terminals) would be constructed as shown below:



(*Id.* at 124 (FIG. 3.9, annotated); *see id.* at 122-23.)

170. As seen from figure 3.9 of Weste, the NMOS transistor is formed by two n+ regions formed inside a p-substrate while the PMOS transistor is formed by two p+ regions formed inside an n-well. The figure above also illustrates ohmic contacts (highlighted in blue) that are used to properly bias the n-well itself and the p-substrate. As shown in the figure, the n-well is tied to V_{DD} (logic “high”) whereas the p-substrate is tied to V_{SS} (logic “low”).

171. Taur (Exhibit 1015) is another well-known treatise⁹ that shows the identical layout for a CMOS inverter where the PMOS transistor is formed inside an n-well next to an NMOS transistor in the p-substrate:

⁹ I am referring to *Taur* (Ex. 1015) to show what a person of ordinary skill in the art would have known at the time of the alleged invention.

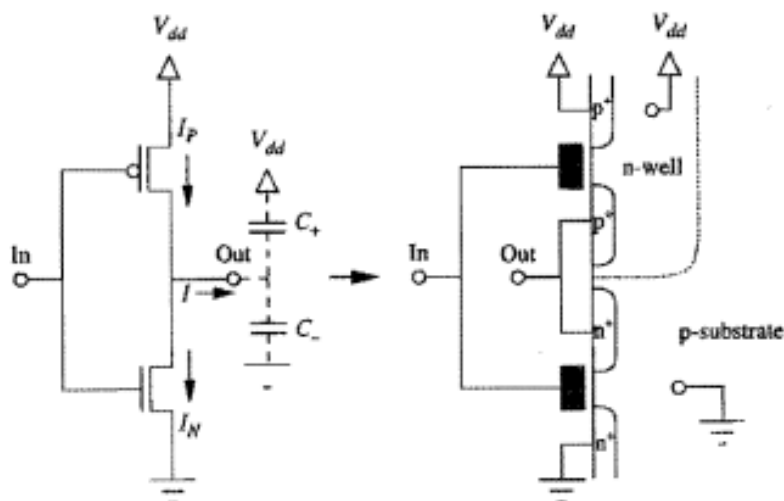
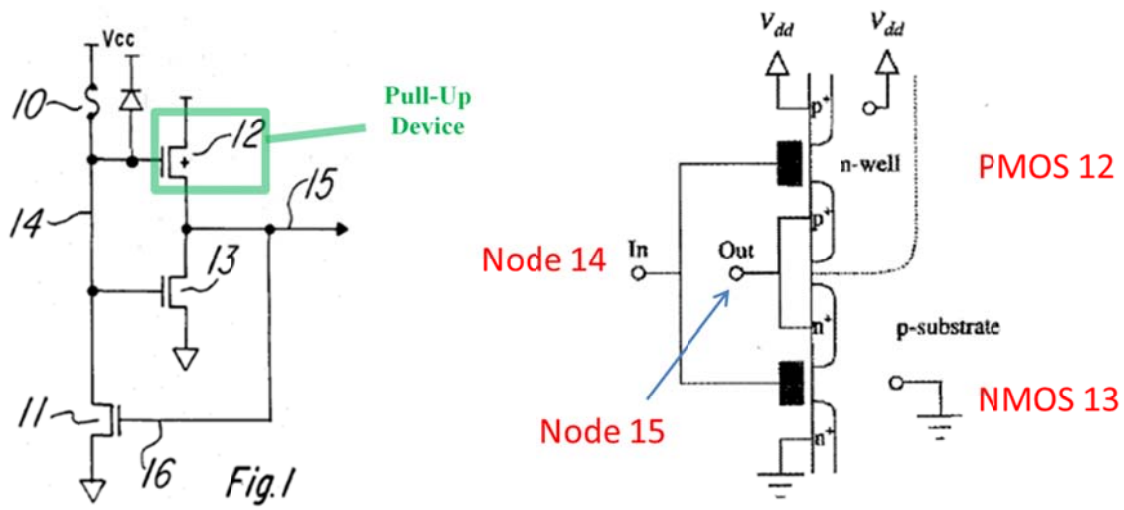


Figure 5.2. Circuit diagram and schematic cross section of a CMOS inverter.

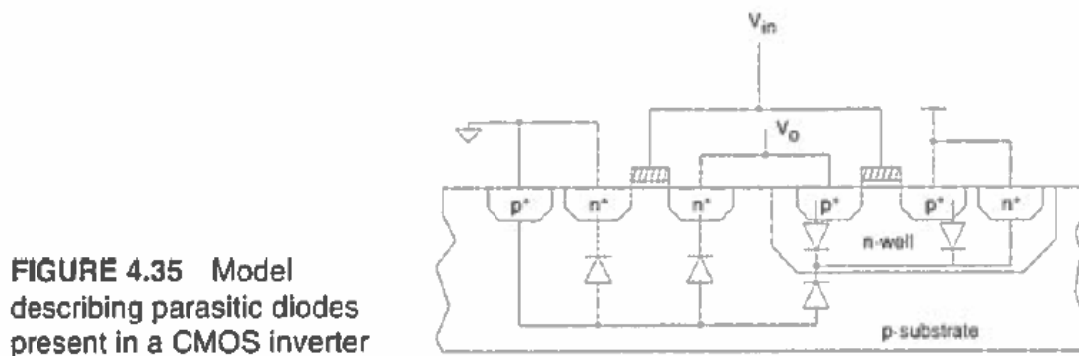
(Ex. 1015 at 257.)

172. In view of the above, a person of ordinary skill in the art would have understood that the inverter in the McAdams-Uda combination, i.e., the combination of PMOS transistor 12 and NMOS transistor 13 in figure 1 of McAdams, would be formed using the following layout (which is the same layout as discussed in both Weste and Taur):



(Ex. 1006 at FIG. 1 (annotated) (left); Ex. 1015 at FIG. 5.2 (annotated) (right).)

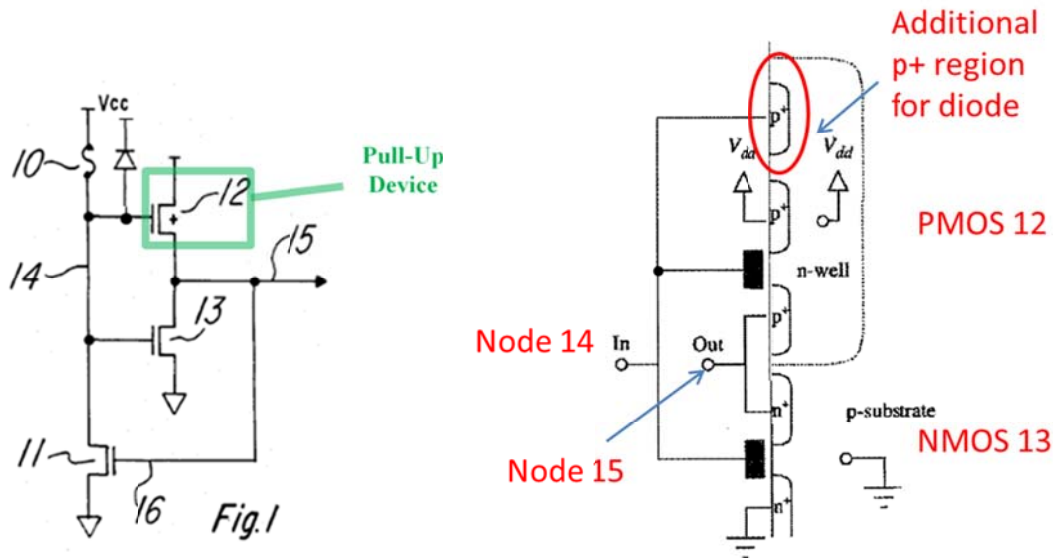
173. The above layout (the right side of the demonstrative above) includes intrinsic diodes formed between the p+ regions and n-region. This is illustrated by West (as shown below):



(Ex. 1009 at 232.)

174. Because the McAdams-Uda combination also includes a diode, an additional p+ region would have been included in the n-well region so that a p-n

diode would be formed by the p⁺ region and the n-well because as seen from figure 4.35 of Weste, a p⁺ region forms an p-n diode with the n-well region. The additional p⁺ region is illustrated below in the demonstrative on the right:



(Ex. 1006 at FIG. 1 (annotated); Ex. 1015 at 257 (FIG. 5.2, annotated and modified to show an additional p⁺ region).¹⁰)

¹⁰ My use of figure 5.2 of Taur to show the features of claim 11 does not alter the fact that I rely on the combination of McAdams, Uda, and Weste. As I indicated above, figure 5.2 of Taur is the same as figure 4.35 of Weste, i.e., both Taur and Weste show the same layout for a CMOS inverter. I use Taur's figure to show the claimed features merely for convenience and ease of representation.

175. A person of ordinary skill in the art would have understood that the diode would be formed using a p-n junction. (See my discussion above in Section V.C.) A person of ordinary skill in the art also would have recognized that the diode shares common connections with the PMOS transistor 12, and therefore the diode and transistor 12 would be placed in close proximity on the chip in order to reduce interconnect. Moreover, since the n-well in which the PMOS transistor is formed is tied to Vdd, which corresponds to Vcc in the McAdams-Uda circuit, the n-portion of the p-n junction for the diode is already present in the layout of the inverter that includes transistors 12 and 13. A person of ordinary skill in the art would have recognized that creating the diode would simply involve the addition of the p+ region as shown in the demonstrative above, where the anode connection for the diode, which corresponds to node 14, is readily available as node 14 is also coupled to the gate of the PMOS transistor as shown in the demonstrative. Indeed, such layout of semiconductor structures is fundamental to integrated circuit design and would have been well within the ability of a person of ordinary skill in the art at the time of the alleged invention. Moreover it is my opinion that any modifications necessary to ensure that the layout shown above that includes the diode and the PMOS transistor in the n-well would function properly would be within the capabilities of a person of ordinary skill in the art.

176. Notably, a person of ordinary skill in the art would have understood that more than one n-well can be included in the p-substrate, but such a person would have recognized that the PMOS transistor 12 and the diode would logically be formed in the same n-well as, as illustrated in the demonstrative above. As noted above, they are located in close proximity in the circuit and share points of connectivity. Moreover, a person of ordinary skill in the art would have understood that having multiple n-wells for multiple circuit elements rather than sharing the n-well between multiple circuit elements would require additional chip area as design rules only allow certain structures to be placed within a certain distance of an n-well, and including multiple n-wells would force the circuitry to be spread across a larger chip area.

177. The above layout illustrated in the demonstrative discloses the features of claim 12. For instance, the PMOS transistor 12 is formed in the n-well (“first semiconductor region of a first conductivity type”) as shown in the demonstrative above. Further, the diode is formed by a p⁺ region (“the diode comprises a second semiconductor region of a second conductivity type”) forming a junction with the n-well (“forming a junction with the first semiconductor region”). The p⁺ region of the diode would be connected to node 14 in the

combination (“the second region being connected to the terminal T1”) as shown in the demonstrative above.

178. A person of ordinary skill in the art would have been motivated to look to a treatise like Weste when implementing the McAdams-Uda combination and would have chosen the CMOS process for implementing the combination because the CMOS process “is the leading VLSI systems technology” (Ex. 1009 at 117) and McAdams states that the inverter that includes transistors 12 and 13 is a “CMOS” inverter. (Ex. 1006 at 2:3-7.) The skilled person would have had reason to combine the teachings of the McAdams-Uda combination with Weste because while the McAdams-Uda combination discloses a circuit diagram (i.e., a schematic like figure 1 of McAdams), the combination does not disclose how to actually implement the components of the circuit in silicon. Weste discloses well-known CMOS fabrication techniques that have been used to form transistors such as those in the McAdams-Uda combination for several decades. Therefore, the person of ordinary skill would have implemented the McAdams-Uda combination using the CMOS fabrication techniques disclosed in Weste.

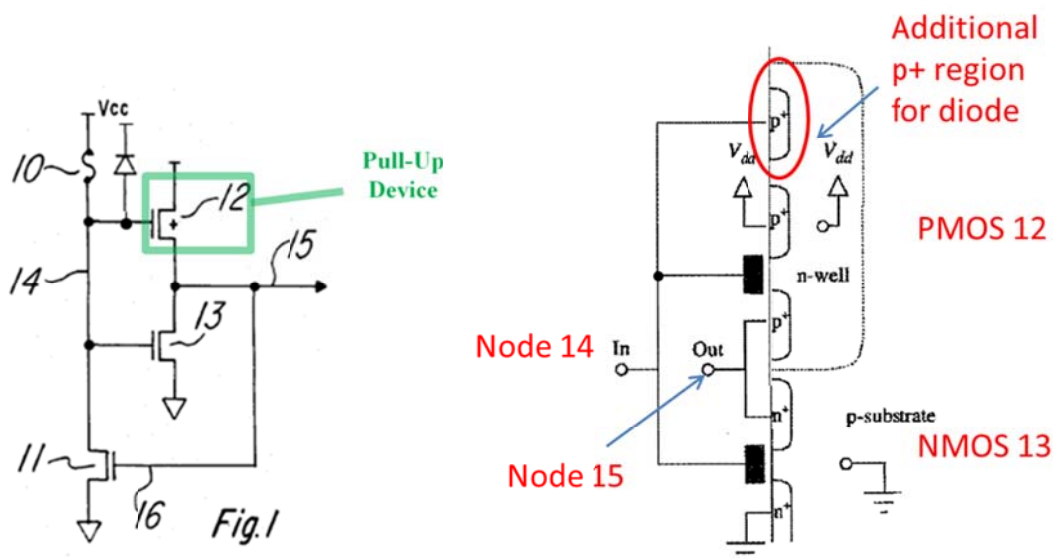
179. Having chosen the CMOS fabrication process, a person of ordinary skill in the art would have naturally arrived at the layout set forth in the demonstrative above because, as described above, that is most the logical way of

implementing the relevant portions (inverter and diode) of the McAdams-Uda circuit.

2. Claim 12

- a) “The programmable latch of claim 11 wherein the MOS transistor is a PMOS transistor, the first conductivity type is type N, the second conductivity type is type P, and the first semiconductor region is to receive a positive voltage.”

180. In my opinion, McAdams in view of Uda discloses or suggests this feature. As I discussed above with respect to claim 11 (*see* above in Section IX.C.1), a person of ordinary skill in the art would have been motivated to implement the inverter and diode in the McAdams-Uda circuit using the following layout:



(Ex. 1006 at FIG. 1 (annotated); Ex. 1015 at 257 (FIG. 5.2, annotated and modified).¹¹)

181. As seen from the above layout, the MOS transistor formed in the n-well is a PMOS transistor (*see* my discussion above in Section IX.C.1), the n-well (“first semiconductor region”) is of conductivity type n (“the first conductivity type is type N”), and the p⁺ region (“second semiconductor region”) is of a conductivity type p (“the second conductivity type is type P”). Moreover, as is evident from the demonstrative above, the n-well is tied to V_{dd}, which is a positive voltage (+5V) in the McAdams-Uda circuit (“the first semiconductor region is to receive a positive voltage”). A person of ordinary skill in the art would have understood that the n-well is tied to the highest voltage in the circuit (e.g. V_{dd}) to ensure proper operation of the circuit. As stated by Weste:

¹¹ My use of figure 5.2 of Taur to show the features of claim 12 does not alter the fact that I rely on the combination of McAdams, Uda, and Weste. As I indicated above, figure 5.2 of Taur is the same as figure 4.35 of Weste, i.e., both Taur and Weste show the same layout for a CMOS inverter. I use Taur’s figure to show the claimed features merely for convenience and ease of representation.

In an n-well process, the p-type substrate is normally connected to the negative supply (V_{SS}) through what are termed V_{SS} substrate contacts, while the well has to be connected to the positive supply (VDD) through VDD substrate (or well or tub) contacts. .

(Ex. 1009 at 122-23.)

182. The reason for such a connection is to ensure that the source/drain regions of the transistor do not become forward-biased with respect to the substrate or well they are made in. For example, for a PMOS, by tying the n-well to the highest voltage in the circuit, i.e., VDD, the p+ regions forming the source/drain would not receive a voltage greater than the n-well. Therefore, the p-n junction formed between the p+ region forming the source/drain and the n-well would not become forward-biased.

183. For at least these reasons, it is my opinion that the McAdams-Uda-Weste combination discloses or suggests “the MOS transistor is a PMOS transistor, the first conductivity type is type N, the second conductivity type is type P, and the first semiconductor region is to receive a positive voltage” as recited in claim 12.

D. Ground 4: McAdams in Combination with Uda and Tomishima Discloses or Suggests Claim 9

184. In my opinion, McAdams in combination with Uda and Tomishima discloses or suggests all of the features of claim 9 of the '492 patent.

1. Claim 9

- a) “The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,”

185. As I explained above in Section IX.A.7(a), the McAdams-Uda combination discloses or suggests this feature. (*See* my discussion above in Section IX.A.7(a).)

- b) “wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.”

186. As I explained above in Section IX.A.7(b), the McAdams-Uda combination discloses or suggests this feature. (*See* my discussion above in Section IX.A.7(b).)

187. However, I have been asked to assume that the combination of McAdams and Uda does not explicitly or necessarily disclose or suggest that the Vcc terminal of the combined McAdams-Uda fuse circuit is received “from an external pin of the integrated circuit” as recited in claim element 9(b). Based on that assumption, it is my opinion that a person of ordinary skill in the art would have been motivated, based on Tomishima (Ex. 1013), to configure the combined

McAdams-Uda fuse circuit to receive the power supply Vcc from an external pin of the integrated circuit.

188. As I discussed above in Section IX.D.1(a), the McAdams-Uda circuit is implemented in an integrated circuit. As I discussed above in Section IX.A.7(b), it was common practice for the integrated circuit device to receive power on an external pin of the integrated circuit and for the circuits inside the integrated circuit to use the received power either directly from the pin or through an intermediate circuit (e.g., an internal power supply generator). (*See* above in Sections IX.A.7(b), IX.B.1.) Indeed, in my opinion, providing power to integrated circuits using external pins was so routine and well-known at the time of the alleged invention that disclosures such as McAdams and Uda would not have provided specifics as to the origin of the power supply inside the chip (e.g., Vcc in figure 1 of McAdams). As demonstrated below, Tomishima supports my opinions and confirms that providing the power supply to an integrated circuit device was commonly accomplished using an external pin of the integrated circuit.

189. Tomishima, like McAdams (Ex. 1006 at Abstract) and Uda (Ex. 1007 at 1:10-18), relates to memory circuits:

The present invention generally related to semiconductor memory device, and in particular, to an arrangement of power supply pads and data input/output pads in a semiconductor

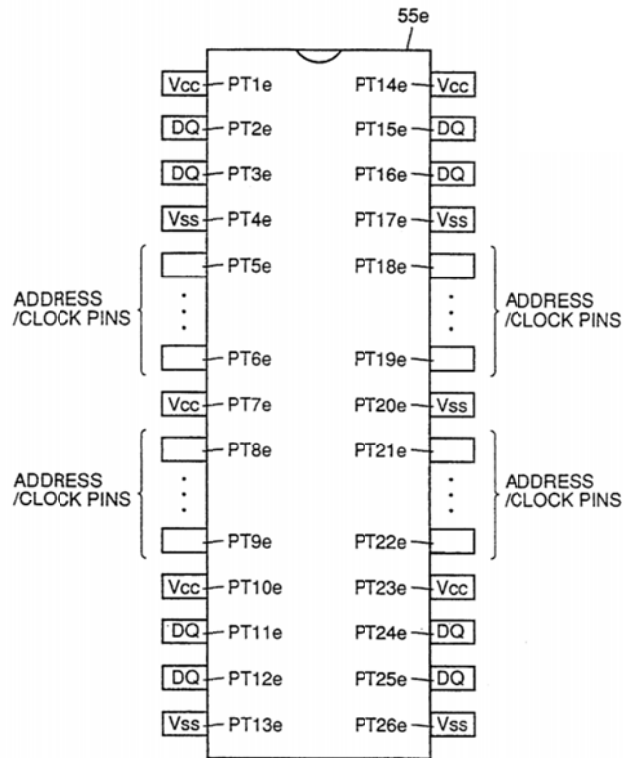
memory device. More particularly, the present invention relates to a layout of power supply pads, and data input/output buffers and peripheral circuits, and a multibit test circuit in a general-purpose DRAM (Dynamic Random Access Memory.)

(Ex. 1013 at 1:12-19.)

190. Tomishima discloses that in an integrated circuit memory (e.g., a DRAM), a center region is conventionally designed to have “pads for receiving external power supply voltage and ground voltage and for input/output of signals.” (Ex. 1013 at 1:31-35.) Tomishima discloses that such a configuration, however, does not allow all structures in the memory device to operate stably at high speed. (*Id.* at 2:40-41.) To overcome these deficiencies, Tomishima discloses a specific arrangement of power supply pads that receive power from a source external to the integrated circuit. (*Id.* at 4:6-14.)

191. Figure 23 of Tomishima discloses an “external pin arrangement of a semiconductor memory device,” where the pin arrangement corresponds to a “memory package housing.” (*Id.* at 6:18-19, 24:32-34, FIG. 23.)

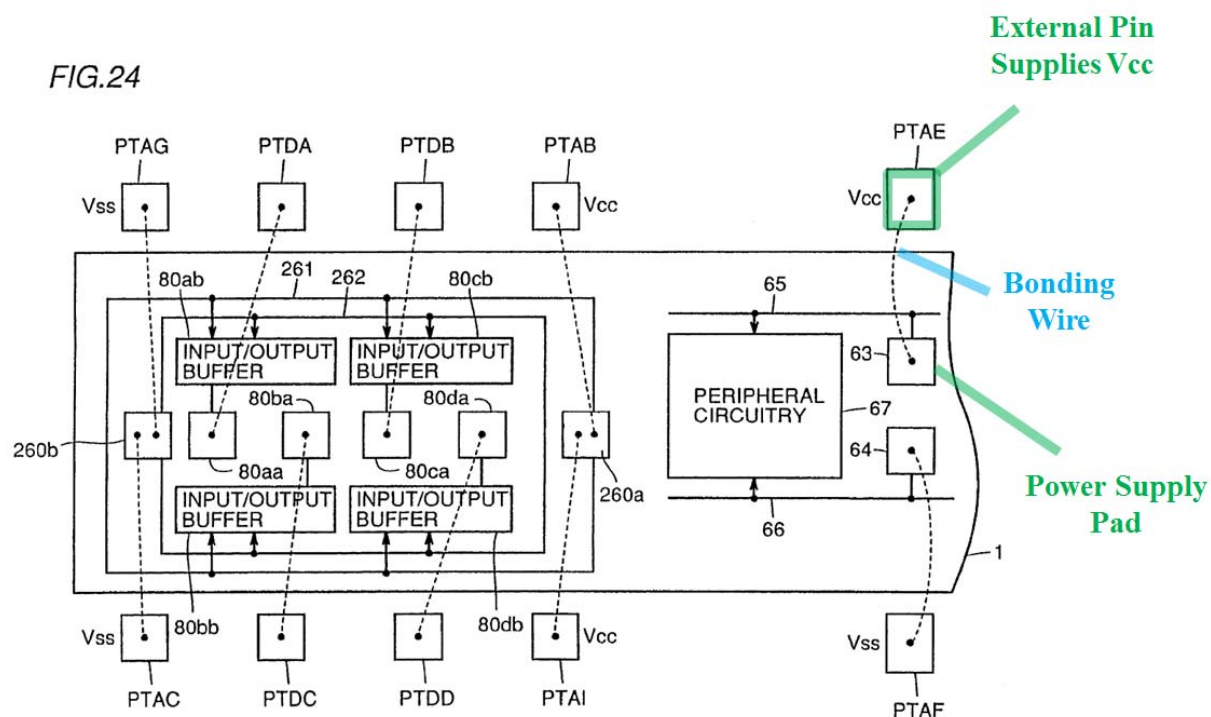
FIG.23



(*Id.* at FIG. 23.)

192. Tomishima explains that “power supply pin terminals and ground pin terminals are arranged on each respective side of package 55e.” (*Id.* at 24:32-40.) “The voltages Vcc and Vss supplied to pin terminals PT7e and PT20e are used by peripheral circuitry operating on the signals received through address/clock pin terminals” (*Id.* at 24:56-59.) Figure 24 of Tomishima, annotated below, shows an inner pad layout of the semiconductor memory device in the package of figure 23. (*Id.* at 6:21-22, 24:60-61.)

FIG. 24



(*Id.* at FIG. 24 (annotated).)

193. I have annotated figure 24 above to help identify the bonding wires (broken lines) that are used to connect the power supply pins to power supply pads (e.g. 260a) on the integrated circuit memory device. (*Id.* at 24:65-25:1.) A person of ordinary skill in the art would have understood that using bonding wires to connect the external pins to the bonding pads on the integrated circuit device was a common connection technique that had been used in the industry for many years before the alleged invention of the '492 patent.

194. In my opinion, a person of ordinary skill in the art would have been motivated to combine the teachings of McAdams, Uda, and Tomishima such that

the power supply V_{cc} in the McAdams-Uda combination is provided by an external pin of the integrated circuit. Neither McAdams nor Uda provides specific disclosure as to how the power supply (e.g., V_{cc} as shown in figure 1 of McAdams) is configured for the integrated circuits disclosed therein or from where the power supply is received. Therefore, a person of ordinary skill in the art would have looked to teachings associated with external power supply connections, such as those disclosed by Tomishima, so that V_{cc} in the McAdams-Uda combination could be provided with the necessary voltage. (Ex. 1006 at 2:8-9 (“During power-up of the supply voltage V_{CC} , as V_{CC} goes from zero to +5 v ...”).)

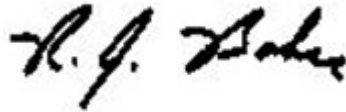
195. A person of ordinary skill in the art would have understood that a connection to an external power supply is necessary for the memory devices like those disclosed in McAdams and Uda to function. Accordingly, a person of ordinary skill would have combined the teachings of the McAdams-Uda combination and Tomishima because Tomishima explains how a power supply can be received by an external pin of an integrated circuit (e.g., the memory device including the McAdams-Uda) and such a power supply can be used to power circuits inside an integrated circuit. (Ex 1013 at 24:56-59.) It is my opinion that any modifications necessary to ensure that the power supply received by an external pin as disclosed in Tomishima would work on in integrated circuit that

includes the latch circuit of McAdams-Uda would have been apparent to, and within the capabilities of, a person of ordinary skill in the art. Moreover, such a person of ordinary skill in the art would have recognized that using an external power supply received on an external pin of the integrated circuit in the McAdams-Uda combination, based on Tomishima, would have been nothing more than the combination of familiar elements (receiving a power supply voltage V_{cc} in the McAdams-Uda combination) according to known methods (using an external pin as in Tomishima to receive a power supply (e.g., V_{cc})) that yields an expected result (a functional memory device that receives a power supply needed for operation).

X. CONCLUSION

196. In summary, it is my opinion that all of the features recited in claims 1-13 of the '492 patent are disclosed or suggested by the prior art.

197. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: March 5, 2019

By: _____
R. Jacob Baker, Ph.D., P.E.