

PATENT NUMBER

6163492



6163492

U.S. UTILITY PATENT APPLICATION

O.I.P.E. SCANNED <u>A.G. ③</u> Q.A. <u>me</u>	PATENT DATE DEC 19 2000
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SECTOR	CLASS 365 327	SUBCLASS 225.7 525	ART UNIT 2818	EXAMINER V. NGUYEN
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PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL			CROSS REFERENCE(S)							
CLASS		SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
365		225.7	365	230.08	189.05	185.14				
INTERNATIONAL CLASSIFICATION										
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11/2/00 / Formal Drawings (5 shts) set / 3/28/2000

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 95	Figs. Drwg. 9	Print Fig. 2A	Total Claims 21	Print Claim for O.G. 1 (AT Final)
☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	VIET Q. NGUYEN Viet Q. Nguyen Primary Examiner _____ (Primary Examiner) 2/19/00 (Date)			2-29-00 ISSUE FEE 28	
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☐ c) The terminal _____ months of this patent have been disclaimed.	[Signature] 3/1/00 (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER I 861	

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Formal Drawings (____ sheets) (____ EL AREA)

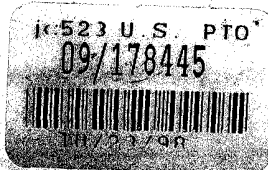
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PATENT APPLICATION



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INITIALS 4

CONTENTS

Date received
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1. Application 9 papers.

2. FDS

12-7-98

3. RESTRICT (20 days)

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6. Suppl. PTO-37(-)

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7. AMENDMENT B

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9. FDS

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10. suppl. PTO-37(-)

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POSITION	INITIALS	ID NO.	DATE
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O.I.P.E. CLASSIFIER	<i>W</i>		<i>11-3</i>
FORMALITY REVIEW		<i>60574</i>	<i>11-6-94</i>

INDEX OF CLAIMS

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SEARCH NOTES

(INCLUDING SEARCH STRATEGY)

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PATENT APPLICATION SERIAL NO.

09/178,445

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
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SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNI	ATTORNEY DOCKET NO.		
09/178,445	10/23/98	257	2811	M-5598-US		
APPLICANT	NIKOLAS SREDANOVIC, MOUNTAIN VIEW, CA; HELENA CALENDAR, MOUNTAIN VIEW, CA.					
	CONTINUING DOMESTIC DATA*** VERIFIED <u>None</u>					
	371 (NAT'L STAGE) DATA*** VERIFIED <u>None</u>					
	FOREIGN APPLICATIONS*** VERIFIED <u>None</u>					
	FOREIGN FILING LICENSE GRANTED 11/05/98					
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	PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE PROGRAMMABLE ELEMENTS					
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October 23, 1998

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Washington, D. C. 20231

Enclosed herewith for filing is a patent application, as follows:

Inventors: Sredanovic, Nikolas; Calendar, Helena
Title: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE
PROGRAMMABLE ELEMENTS

- 9 Sheet(s) of drawings
19 page(s) Specification (Including Addendum A (2 pages))
10 page(s) Claims
1 page Abstract
3 page(s) Declaration/Power of Attorney
1 page(s) Recordation Cover Sheet (in duplicate)
2 page(s) Assignment
X Transmittal Letter (in duplicate)
page(s) PTO Form 1449
☐ Copy(ies) of Cited References
☐ Other: _____

CLAIMS AS FILED (fees computed under §1.9(f))

For	Number Filed		Number Extra		Rate		Basic Fee
						\$	790.00
Total Claims	31	-20 =	11	x	\$22 =	\$	242.00
Independent Claims	5	-3 =	2	x	\$82 =	\$	164.00
☐ Application contains one or more multiple dependent claims (\$270 total fee)						\$	0.00

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Respectfully submitted,

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Attorney for Applicants
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PROGRAMMABLE LATCHES THAT INCLUDE
NON-VOLATILE PROGRAMMABLE ELEMENTS

Nikolas Sredanovic

Helena Calendar

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CROSS-REFERENCE TO RELATED APPLICATIONS

Not applicable.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

10 Not applicable.

BACKGROUND OF THE INVENTION

356201 "4482F60
The present invention relates to programmable
latches that include non-volatile programmable
15 elements. Examples of non-volatile programmable
elements are fuses.

20 Programmable latches with fuses are used in
integrated circuits to enable modification of the
circuits without changing the masks used for circuit
fabrication. For example, fuse programmable latches
are used to replace defective memory cells with spare
cells in semiconductor memories.

25 Fig. 1 shows one such latch described in U.S.
Patent 4,546,455 issued October 8, 1985 to Iwahashi et
al. Fuse F1 is connected between the power supply
terminal VDD and the latch output terminal OUT. An
NMOS transistor 110 is connected between the terminal
OUT and the ground terminal. Three serially connected

inverters 120.1, 120.2, 120.3 are provided between the output terminal OUT and the gate of transistor 110.

If fuse F1 is intact, the terminal OUT is pulled to VDD. The inverters 120 keep transistor 110 off. If
5 fuse F1 is blown, the terminal OUT is at the ground voltage. The inverters turn transistor 110 on to keep the terminal OUT at ground.

Bypass capacitor 130 is connected between the input of inverter 120.3 and the ground terminal to
10 insure correct initialization of the latch on power-up. More particularly, when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating. According to U.S. Patent 4,546,455, the terminal OUT may "tend to have its potential raised to
15 a logic level '1' ". In addition, the terminal OUT potential may become "unstable due to the capacitive coupling" in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown. As a result, the terminal OUT
20 would provide an erroneous voltage.

Capacitor 130 is intended to avoid such malfunction. During power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge
25 the terminal OUT to ground if the fuse is blown. Then the ground voltage on terminal OUT propagates through the three inverters to keep transistor 110 on.

It is desirable to provide alternative programmable latches.

30

SUMMARY

Some embodiments of the present invention provide simple and reliable programmable latches. Some programmable latches are reliable because they do not depend on delays such as delays provided by capacitor 130. Dependence on delays is undesirable because delay-dependent circuits may not operate properly if VDD rises slowly. Some latches are simple because they omit capacitor 130 and include only one CMOS inverter.

High reliability is achieved in some embodiments by a diode that keeps a voltage on a latch output terminal within a predetermined range of values before power is supplied to the latch. In some embodiments, the diode's anode is connected to terminal OUT, and the cathode is connected to an external power supply pin EVCC or to a reference voltage terminal. When power is off, the EVCC pin or the reference voltage terminal is at ground, and therefore the voltage on the terminal OUT is not higher than one diode threshold voltage relative to ground (0.65V in some embodiments.) The maximum voltage of 0.65V on terminal OUT allows the latch to be powered up correctly even if fuse F1 is blown.

In some embodiments, the diode's cathode is connected to a reference voltage which is used also in other parts of the integrated circuit. The reference voltage is generated by a reference voltage generator which includes one or more pull-down resistors connected to the reference voltage terminal and to the

ground terminal. When the power is off, these resistors discharge the reference voltage terminal to ground. Hence, the OUT voltage is not higher than one diode threshold relative to ground when the power is
5 off.

Prior art latch of Fig. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the
10 state of fuse F1 and the voltages on the VDD and ground terminals. This advantage is preserved in some embodiments of the present invention. This advantageously distinguishes such embodiments of the invention from the latch described in U.S. Patent
15 5,566,107 issued October 15, 1996 to Gilliam in describing a circuit that needs an external "activate" signal for initialization.

Some embodiments do not include a capacitor to generate a delay.

20 In some embodiments, only one inverter having a pull-up device and one pull-down device is provided between the output terminal OUT and the gate of transistor 110.

Some embodiments with only one CMOS inverter and
25 no capacitor operate successfully even without a diode because in such embodiments the voltage on the terminal OUT is at the ground level before the power is turned on. The voltage could drift away from the ground level during fuse programming if, for example, the fuse is
30 programmed electrically. (Of note, some embodiments

use laser programmable fuses rather than electrically programmable fuses.) However, even if the voltage on terminal OUT becomes high when the fuse is being programmed, the power is turned off after programming, and the voltage on the terminal OUT is allowed to return to ground before the power is turned on again.

Further, in some embodiments, even if the voltage on the terminal OUT is at a high value immediately before the power is turned on, the latch operates properly due to the selection of the trip voltage of the inverter and/or the threshold voltage of transistor 110.

Other features and advantages of the invention are described below. The invention is defined by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a prior art programmable latch.

Fig. 2A is a circuit diagram of a programmable latch according to the present invention.

Fig. 2B illustrates a semiconductor cross section of the latch of Fig. 2A.

Fig. 3 is a circuit diagram illustrating a reference voltage generator that powers the latch of Fig. 2A.

Figs. 4 and 5 are circuit diagrams of alternative reference voltage generators for the latch of Fig. 2A.

Figs. 6-8 are circuit diagrams of programmable latches according to the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 2A illustrates a programmable latch 210 according to the present invention. Terminal 211 of fuse F1 is connected to a terminal 212 providing a constant non-ground voltage VINT. Voltage VINT is an internal power supply voltage generated by VINT generator 213 from an external power supply voltage EVCC received on an external pin 214 of the integrated circuit containing the latch 210. Voltage VINT also powers other parts of the integrated circuit. Voltage VINT is a positive voltage.

Terminal 215 of fuse F1 is connected to terminal OUT.

The terminal OUT is connected to the drain of NMOS transistor 110 whose source is connected to a ground terminal.

Terminal OUT is connected to the input of CMOS inverter 120 formed by PMOS pull-up transistor 220 and NMOS pull-down transistor 230. The inverter input is connected to the gates of transistors 220, 230. The source of transistor 220 is connected to VINT terminal 212. The source of transistor 230 is connected to the ground terminal. The drains of the two transistors are connected to complimentary output terminal OUT- of latch 210. Terminal OUT- is connected to the gate of transistor 110.

Diode 234 has its anode terminal 238 connected to terminal OUT and its cathode terminal 240 connected to

the VINT terminal 212. When the power is off, the VINT terminal is at ground. (VINT terminal is connected to ground by a resistor network in generator 213, as described below in connection with Fig. 3.) Therefore, the voltage on the terminal OUT is not higher than one threshold voltage of diode 234. If diode 234 is a silicon PN junction diode, the voltage on terminal OUT is not higher than 0.65V. This value is below the trip voltage of inverter 120 and even below the threshold voltage of NMOS transistor 230 (the threshold voltage of transistor 230 is 1.2V in some embodiments). Therefore, if fuse F1 is blown, transistor 230 remains off when the power is turned on. As soon as transistor 220 charges the gate of transistor 110 to the threshold voltage of transistor 110, transistor 110 connects the terminal OUT to ground.

If fuse F1 is conductive, then terminal OUT is at VINT, and transistor 110 is turned off by inverter 120.

During operation of latch 210 the diode is off and thus no current flows through diode 234.

Fig. 2B illustrates a cross section of a portion of the integrated circuit incorporating the latch 210 in some embodiments. The source 220S and the drain 220D of transistor 220 are P+ semiconductor regions in N well 242 in P substrate 244. Gate 220G of transistor 220 is separated from N well 242 by silicon dioxide (not shown). The N well is connected to the VINT terminal via an ohmic contact in the N+ region 246 formed in the N well. The diode cathode 238 is a P+ region formed in the N well. The diode is formed by

the PN junction between the region 238 and the surrounding region 240 of N well 242.

No external signal is used to initialize the latch. The state of the latch (the voltage on the terminal OUT) during the latch operation is completely determined by the state of fuse F1 and by the voltages on the terminal 212 and the ground terminal.

Fig. 3 shows one embodiment of VINT generator 213. The output terminal 212 of the VINT generator is connected to ground by a resistor network which includes: (1) resistors R1, R2, R3 connected in parallel between terminal 212 and a node FD; and (2) resistor R4 interconnecting the node FD and the ground terminal.

The pull-up path between the terminal 212 and the external voltage supply EVCC is through PMOS transistor 310. The gate of transistor 310 is connected to the output of a differential amplifier formed by PMOS transistors 314, 318 and NMOS transistors 322, 326, 330 and 334. The sources of transistors 314, 318 are connected to the EVCC pin. The gates are connected to each other and to the drain of transistor 314. The drain of transistor 318 is the amplifier output connected to the gate of transistor 310. The drain of transistor 318 is also connected to the drain of transistor 326. The drain of transistor 314 is connected to the drain of transistor 322. The gate of transistor 322 is connected to the node FD. The gate of transistor 326 receives a reference voltage VREF generated by some reference voltage generator (not



shown) as known in the art. The sources of transistors 322, 326 are connected to the drain of transistor 330. The source of transistor 330 is connected to the drain of transistor 334. The source of transistor 334 is
5 connected to ground.

The gate of transistor 334 receives a reference voltage VCMN generated by a reference voltage generator (not shown). The gate of transistor 334 is also connected to ground through MOS capacitor 340. (A MOS
10 capacitor is a capacitor formed by a MOS transistor whose source and drain are shorted together.) The gate of transistor 330 receives an enable signal EN. The signal EN is also delivered to the gate of PMOS transistor 344 whose drain is connected to the gate of
15 transistor 310 and whose source is connected EVCC. When EN is low (ground), the VINT terminal 212 is at ground. When EN is at EVCC, the terminal 212 provides a voltage between ground and EVCC.

Terminal 212 is connected to node FD by MOS
20 capacitor 350.

Node FD is connected to the drain of NMOS transistor 354. The source node 358 of transistor 354 is connected to the drain of transistor 362 whose source is connected to ground. Node 358 is connected
25 to terminal 212 through MOS capacitor 366.

The gate of transistor 362 is connected to the output of NAND gate 370. The output of gate 370 is also connected to the input of inverter 374 whose output is connected to the gate of transistor 354. One
30 input of two-input gate 370 receives the enable signal

EN. The enable signal EN is delivered to the other output of gate 370 through three serially connected inverters 374, 378, 382.

In some embodiments, voltage VINT on terminal 212 is an internal power supply voltage that powers also other parts of the integrated circuit containing the latch 210. In some embodiments, the integrated circuit is a synchronous dynamic random access memory (SDRAM). The voltage VINT powers the memory address decoders, command decoding circuitry, burst counting circuitry, and input buffers such as clock enable buffer 386. Buffer 386 receives a clock enable signal CKE from an external pin and generates an internal clock enable ICKE at ground and VINT voltage levels.

In some embodiments, the synchronous DRAM includes several generators 213. Each generator is enabled by its own signal EN. Thus, selective generators 213 can be disabled to reduce power consumption (in stand-by mode, for example). However, at least one generator 213 is enabled throughout the circuit operation in order to power circuits that are never disabled, for example, the buffer 386. Hence, the VINT voltage is a constant value throughout the operation of the integrated circuit.

In some embodiments, the outputs 212 of some or all of the generators 213 are shorted together. However, some generators 213 are sometimes disabled (in stand-by mode for example) when the current drawn from the common terminal 212 of generators 213 is reduced.

In some embodiments, VINT = 2.5V and EVCC = 3.3V.

Addendum A provides transistor sizes and resistor values and some other particulars for one embodiment of a VINT generator 213.

5 Figs. 4 and 5 show other embodiments of a VINT generator 213. In Fig. 4, VINT generator 213 is a voltage divider formed by resistors 410, 420 connected in series between EVCC pin 214 and the ground pin of the integrated circuit.

10 In Fig. 5, resistor 420 is replaced by an NMOS transistor (a long channel transistor in some embodiments) whose body region is connected to the ground terminal. The gate of transistor 420 receives a reference voltage VREF. This voltage is generated by a voltage divider consisting of resistors 510, 520
15 connected in series between EVCC and ground. When the power is off, the VREF terminal is at ground, and transistor 420 is off. However, the drain/body diode of transistor 420 does not allow the voltage on terminal 212 to rise above one diode threshold relative
20 to ground.

Other resistors are replaced by transistors in some embodiments. Still other embodiments use other VINT generators, known in the art or to be discovered.

25 Latch 210 of Fig. 6 is identical to the latch of Fig. 2A except that in Fig. 6 the diode cathode 240 is connected to EVCC pin 214.

Some embodiments include two diodes, with one diode connected as in FIG. 6 and the other diode connected as in FIG. 2A. Some embodiments include

diodes connected in series or in parallel between the terminal OUT and the terminal 212 or 214.

In some embodiments, the terminals 211 and 240 are both connected to the EVCC terminal 214. Inverter 120
5 is powered by EVCC. When the power is off, the EVCC terminal is at ground because the integrated circuit includes a voltage divider, such as the voltage divider 213 of Fig. 4, to generate an intermediate voltage.

In some embodiments, diode 234 is omitted.
10 Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed
15 (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory
20 is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at
25 ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on
30 terminal OUT increased slightly at the beginning of the

power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, 5 the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.

In some embodiments, the inverter 120 trip voltage, measured when EVCC has reached its final value, is made high to ensure that the trip voltage 10 will be higher than any voltage on terminal OUT. For example, in some embodiments, the inverter trip voltage is 1.6 V when EVCC = 3.3 V. The trip voltage can be made large by making transistor 220 large relative to transistor 230, or by increasing the threshold voltage 15 of transistor 230, or by other methods known or to be discovered.

In some embodiments, the threshold voltage of transistor 110 is made low (lower than the threshold voltages of other NMOS transistors, including 20 transistor 230, in the same integrated circuit), so that even if the terminal OUT is slightly above the inverter trip voltage when the fuse is blown, the inverter will charge the complementary terminal OUT- to a sufficiently high voltage to pull the terminal OUT 25 down. As the terminal OUT is being pulled down, the voltage on terminal OUT- increases, the current through transistor 110 also increases, and eventually the terminal OUT is pulled to ground by the transistor 110.

In some embodiments with or without the diode 234, 30 EVCC = 3.3V, the threshold voltage of transistor 230 is

1.2V, the threshold voltage of transistor 220 is -0.8V, and the threshold voltage of transistor 110 is 0.5V. The trip voltage of inverter 120 is 1.6V at the final EVCC value of 3.3V.

5 Fig. 7 illustrates another embodiment of latch 210. Fuse F1 and diode 234 are connected to terminals VINT and OUT, and NMOS transistor 110 is connected to the terminal OUT and to the ground terminal, as in Fig. 2A. However, three inverters 120.1, 120.2, 120.3 are
 10 provided between the terminal OUT and the gate of transistor 110. In inverter 120.1, the gates of PMOS transistor 220.1 and NMOS transistor 230.1 are connected to the terminal OUT. The source of transistor 220.1 is connected to VINT. The source of
 15 transistor 230.1 is connected to ground. The drains of transistors 220.1, 230.1 are connected to the gates of PMOS transistor 220.2 and NMOS transistor 230.2 of inverter 120.2. The drains of transistor 220.2, 230.2 are connected to the gates of PMOS transistor 220.3 and
 20 NMOS transistor 230.3 of inverter 120.3. The sources of transistors 220.2, 220.3 are connected to the VINT terminal 212. The sources of transistors 230.2, 230.3 are connected to ground. The drains of transistors 220.3, 230.3 are connected to the gate of transistor
 25 110.

The voltage VINT is generated by some voltage generator such as the generator 213 of Fig. 3.

In some embodiments, diode 234 is omitted, or its cathode is connected to EVCC pin 214.

30 No capacitor is used in the latch of Fig. 7.

The output of inverter 120.1 (the terminal connected to the drains of transistors 220.1, 230.1) is the complimentary output OUT- of latch 210.

If the fuse F1 is conductive, then terminal OUT is
5 at VINT, and the three inverters keep transistor 110 off. If the fuse is blown, then terminal OUT is at ground, or is at most one diode threshold above ground, for essentially the same reasons as those explained above in connection with Fig. 2A. Therefore, when the
10 power is supplied, transistor 110 is turned on.

In some embodiments, the trip voltage of inverter 120.1 is made high to ensure that when the fuse is blown, the trip voltage will be higher than any possible voltage on the terminal OUT.

15 In some embodiment, the threshold voltage of transistor 110 is made low (lower than threshold voltages of other NMOS transistors in the same integrated circuit) to facilitate discharge of terminal OUT, similarly to the Fig. 2A embodiment.

20 Some embodiments include five inverters, or some other number of inverters, connected in series between the terminal OUT and the gate of transistor 110.

Latch 210 of Fig. 8 is similar to the latch of Fig. 2A, but the supply voltage EVCC and the voltage
25 VINT are negative. Transistors 110 and 230 are PMOS transistors. Transistor 220 is an NMOS transistor. Diode 234 has its anode connected to VINT terminal 212 and its cathode connected to terminal OUT.

Some embodiments of the latch of Fig. 7 or of latches with five or more inverters also use negative supply voltages.

Some embodiments use a non-ground reference
5 voltage instead of the ground.

In some embodiments of Figs. 2A, 7, 8, fuse F1 is a laser programmable fuse made of polysilicon, metal (for example, aluminum), or some other conductive material. In other embodiments, the fuse F1 is an
10 electrically programmable fuse, for example, a polysilicon fuse which can be blown by current supplied through another transistor (not shown). In still other embodiments, fuse F1 is replaced by some other programmable element, for example, an antifuse, an
15 EPROM, EEPROM, or UPROM cell (see B. Prince, "Semiconductor Memories" (1991), pages 762-764 incorporate herein by reference), or some other non-volatile programmable element known or to be discovered.

20 In some embodiments, the inverters 120 of Figs. 2A, 7, 8 are non-CMOS inverters. For example, in some embodiments the pull-up transistors 220 are replaced by suitable resistors or depletion mode transistors.

Programmable latches 210 are suitable for use in a
25 wide variety of memory and non-memory circuits. Some latch embodiments are used in dynamic random access memories. Some latch embodiments are used in spare row and column decoders to select spare rows or columns. Such use of programmable latches is described in U.S.
30 Patent 4,546,455 issued October 8, 1985 to Iwahashi et

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al. and incorporated herein by reference. In some embodiments, programmable latches 210 are used to adjust delay times or select a clock signal, as described in U.S. Patent 5,440,246 issued August 8, 1995 to Murray et al. and incorporated herein by reference. In some embodiments, the latches 210 are used to salvage defective memories as described in U.S. Patent Application 08/840,337 filed April 28, 1997 by Li-Chun Li et al. ^{now U.S. Patent No. 5,689,414 issued on March 30, 1999} and incorporated herein by reference.

10 The invention is not limited by the embodiments described above. In some embodiments, transistor 110 is replaced by a variable-impedance electrical path which includes a number of transistors connected in series or in parallel between the terminal OUT and the ground terminal. One or more of the transistors have their gates connected to the output of inverter 120 or 120.3. In some embodiments, other circuit elements (such as resistors, perhaps variable-impedance resistors) are included between the terminal OUT and 20 the ground or VINT terminals. In some embodiments, diode 234 is a Schottky diode. Other embodiments and variations are within the scope of the invention, as defined by the appended claims.

ADDENDUM A

The table below specifies transistor channel width/length dimensions (in micrometers) and resistor values for one embodiment of a VINT generator 213 of Fig. 3. The NAND gate 370 and all the inverters are CMOS circuits.

Device	Specification
Resistor R1	5.6 K Ω
Resistor R2	90 K Ω
Resistor R3	90 K Ω
Resistor R4	6 K Ω
Transistor 310	1000/1
Transistor 314	50/0.6
Transistor 318	100/0.6
Transistor 322	50/0.6
Transistor 326	100/0.6
Transistors 330	100/1
Transistor 334	100/1
Transistor 340	2/15
Transistor 344	2/2
Transistor 350	2/100
Transistor 354	20/1
Transistor 362	4/1
Transistor 366	2/70
NAND gate 370	10/1 for each transistor
Inverter 374	P = 6/1 (PMOS transistor width length), N = 6/1 (NMOS transistor

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Device	Specification
	width/length)
Inverters 374, 378, 382	P = 5/1, N = 2/2

Each resistor R1, R2, R3, R4 is an N-type diffusion region in a P-type monocrystalline silicon substrate region biased at ground.

CLAIMS

- 1 A programmable latch comprising:
a first terminal for receiving a first
voltage;
5 a second terminal for receiving a second
voltage;
a terminal T1 for providing a signal
indicating a state of the programmable latch;
a programmable electrical path including a
10 non-volatile programmable element such that when
the programmable element is conductive, the
programmable path connects the terminal T1 to the
first terminal, and when the programmable element
is non-conductive, the programmable path does not
15 connect the terminal T1 to the first terminal;
a variable-impedance electrical path between
the terminal T1 and the second terminal, wherein
the impedance of the electrical path is controlled
by a signal on the terminal T1; and
20 a diode for keeping a voltage on the terminal
T1 within a predetermined range of values before
power is supplied to the latch, to prevent the
latch from assuming an incorrect state when power
is supplied to the latch.
25
2. The programmable latch of Claim 1 wherein
during operation of the latch the signal on the
terminal T1 is completely determined by the state of
the programmable element and the first and second
30 voltages.

3. The programmable latch of Claim 1 wherein the latch does not receive any latch initialization signal from outside the latch.

5

4. The programmable latch of Claim 1 wherein no current flows through the diode during normal operation of the latch, but when the power is off then current flows through the diode if the voltage on the terminal
10 T1 is outside the predetermined range of values.

5. The programmable latch of Claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a
15 ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.

20

6. The combination of Claim 5 wherein the first electrical path is a resistor or a resistor network.

7. The combination of Claim 5 wherein the first
25 electrical path is part of a reference voltage generator whose output is connected to the diode's first terminal.

8. The programmable latch of Claim 1 wherein the
30 diode has one terminal connected to the terminal T1,

and the diode has another terminal connected to the first terminal.

9. The programmable latch of Claim 1 wherein the
5 latch is an integrated circuit or a part of an integrated circuit, wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.

10

10. The programmable latch of Claim 1 wherein:
the programmable element is a fuse connected to and between the terminal T1 and the first terminal;

15

the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal;

20

the programmable latch further comprises an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the
25 pull-up and pull-down devices are connected to the inverter output.

25

11. The programmable latch of Claim 10 wherein one of the pull-up and pull-down devices is a MOS
30 transistor formed in a first semiconductor region of a

first conductivity type, and the diode comprises a second semiconductor region of a second conductivity type forming a junction with the first semiconductor region, the second region being connected to the
5 terminal T1.

12. The programmable latch of Claim 11 wherein the MOS transistor is a PMOS transistor, the first conductivity type is type N, the second conductivity
10 type is type P, and the first semiconductor region is to receive a positive voltage.

13. The programmable latch of Claim 1 wherein:
said predetermined range consists of all voltages
15 below a predetermined value; and
when the programmable element is conductive, the variable-impedance path is non-conductive.

20 14. A method for generating a signal indicating a state of a non-volatile programmable element connected to a first terminal and a terminal T1, the method comprising:

25 providing an electrical path between the first terminal and the terminal T1 before supplying power to the first terminal, to keep a voltage on the terminal T1 within a predetermined range of values; then

30 supplying power to the first terminal and turning off said electrical path, and supplying a ground voltage to a ground terminal, wherein an

impedance between the ground terminal and the terminal T1 is controlled by the voltage on the terminal T1, and wherein during operation of the latch the voltage on the terminal T1 is completely determined by the state of the programmable element and by a voltage on the first terminal.

15. The method of Claim 14 wherein the electrical path comprises a diode connected between the first terminal and the terminal T1.

14 16. A programmable latch comprising:

a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

a second terminal for receiving a voltage;
a terminal T1 for providing a signal indicating a state of the programmable latch;

a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a

control terminal for controlling the impedance of the variable-impedance path; and

an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

~~15~~ 17. The programmable latch of Claim ~~16~~ wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.

~~16~~ 18. The programmable latch of Claim ~~16~~ wherein the latch does not receive any latch initialization signal from outside the latch.

~~17~~ 19. The programmable latch of Claim ~~16~~ wherein the second terminal is to receive a ground voltage throughout operation of the latch.

~~18~~ 20. The programmable latch of Claim ~~16~~ wherein the programmable element is a fuse.

¹⁹
~~21~~. The programmable latch of Claim ¹⁴~~16~~ wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.

5 ²⁰
~~22~~. The programmable latch of Claim ¹⁴~~16~~ wherein the first voltage is about 2.5 V, and the trip voltage of the inverter at a final value of a voltage that powers the inverter is about 1.6 V.

10 ²¹
~~23~~. The programmable latch of Claim ¹⁴~~16~~ wherein the variable-impedance path is an NMOS transistor having a threshold voltage of about 1.2 V, the constant non-ground voltage is about 2.5 V, and the second terminal is to receive a ground voltage throughout
15 operation of the latch.

20 24. A programmable latch comprising:
a first terminal for receiving a first voltage which is a non-ground voltage;
a second terminal for receiving a second voltage;
a terminal T1 for providing a signal indicating a state of the programmable latch;
a non-volatile programmable element connected
25 to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1

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from the first terminal when the programmable element is non-conductive;

a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable impedance path; and

one or more serially connected inverters $IV_1, \dots, IV_n$ ($n \geq 1$), wherein the terminal T1 is connected to an input of inverter IV_1 , and the control terminal is connected to an output of inverter IV_n ;

wherein during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltage; and

wherein no capacitor is provided between an input of any inverter IV_i ($i=1, \dots, n$) and the second terminal.

25. The programmable latch of Claim 24 wherein the second voltage is ground.

26. The programmable latch of Claim 24 wherein the variable-impedance path comprises a transistor connected to and between the second terminal and the terminal T1.

27. The programmable latch of Claim 24 wherein the first voltage is about 2.5 V, and the trip voltage

of the inverter IV_1 at a final value of a voltage that powers the inverter is about 1.6 V.

28. The programmable latch of Claim 24 wherein
5 the programmable latch is part of an integrated circuit, and the programmable latch is to control another circuit which is part of the same integrated circuit.

10 29. The programmable latch of Claim 24 wherein the programmable element is a laser programmable fuse.

30. A method for providing a signal indicating a state of a non-volatile programmable element
15 interconnecting a first terminal and a terminal T1, the method comprising:

supplying power to the first terminal to develop a non-ground voltage on the first terminal;

20 controlling an impedance of a variable-impedance electrical path interconnecting the terminal T1 and a second terminal, wherein the controlling operation uses an inverter whose input is connected to the terminal T1 and whose output
25 is connected to a control terminal of the electrical path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and

pull-down devices are connected to the inverter output, such that:

if the programmable element is non-conductive, the inverter causes the variable-impedance path to be conductive;

if the programmable element conducts and causes the voltage on the terminal T1 to move away from the ground voltage, the variable-impedance path is non-conductive,

wherein the signal on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.

31. The method of Claim 29 wherein when power is supplied to the first terminal, the second terminal is at a ground voltage.

PROGRAMMABLE LATCHES THAT INCLUDE
NON-VOLATILE PROGRAMMABLE ELEMENTS

Nikolas Sredanovic

Helena Calendar

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09/178445

ABSTRACT OF THE DISCLOSURE

A non-volatile programmable latch (210) has a fuse
(F1) connected between a non-ground voltage terminal
10 (212) and an output terminal (OUT). A NMOS transistor
(110) is connected between the output terminal and
ground. An inverter (120) has an input connected to
the output terminal and an output connected to the gate
of the NMOS transistor. A diode connects the output
15 terminal to the non-ground voltage terminal (212) to
prevent a charge build up on the output terminal when
the power is off.

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled Programmable Latches that Include Non-Volatile Programmable Elements

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on ____ (if applicable).

I hereby state that ~~I have reviewed~~ and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal

atty. Docket No.: M-5598 US

Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Alan H. MacPherson (24,423); Thomas S. MacDonald (17,774); Kenneth E. Leeds (30,566); Brian D. Ogonowsky (31,988); David W. Heid (25,875); Norman R. Klivans (33,003); Edward C. Kwok (33,938); David E. Steuber (25,557); Michael Shenker (34,250); Stephen A. Terrile (32,946); Peter H. Kang (40,350); T. Lester Wallace (34,748); Ronald J. Meetin (29,089); Ken John Koestner (33,004); Omkar K. Suryadevara (36,320); David T. Millers (37,396); Kent B. Chambers (38,839); Serge J. Hodgson (40,017); Michael P. Adams (34,763); Bernard Berman (37,279); Michael J. Halbert (40,633); Gary J. Edwards (41,008); William B. Tiffany (41,347); James E. Parsons (34,691); Daniel P. Stewart (41,332); Philip W. Woo (39,880); John T. Winburn (26,822); Tom Chen (42,406); Fabio E. Marino (43,339); William W. Holloway (26,182); Elaine H. Lo (41,158); and Don C. Lawrence (31,975).

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I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

ttty. Docket No.: M-5598 US

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Inventor's Signature: *Helena Calendar* Date: 9/21/98
Residence: Mountain View, California
Post Office Address: 1960 California Street #5, Citizenship: Swedish
Mountain View, CA 94041

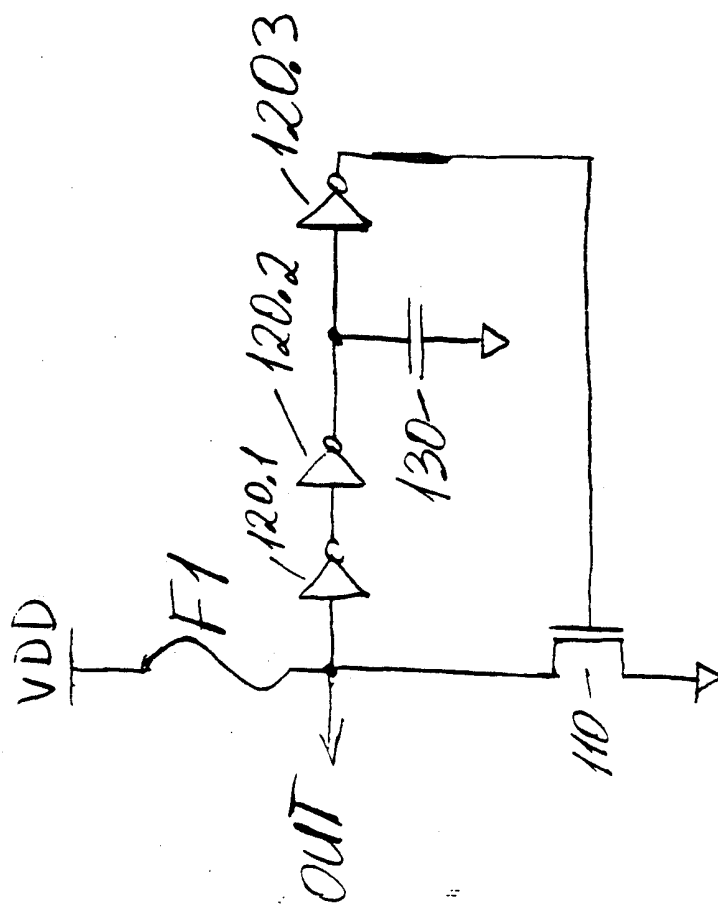


FIG. 1 PRIOR ART

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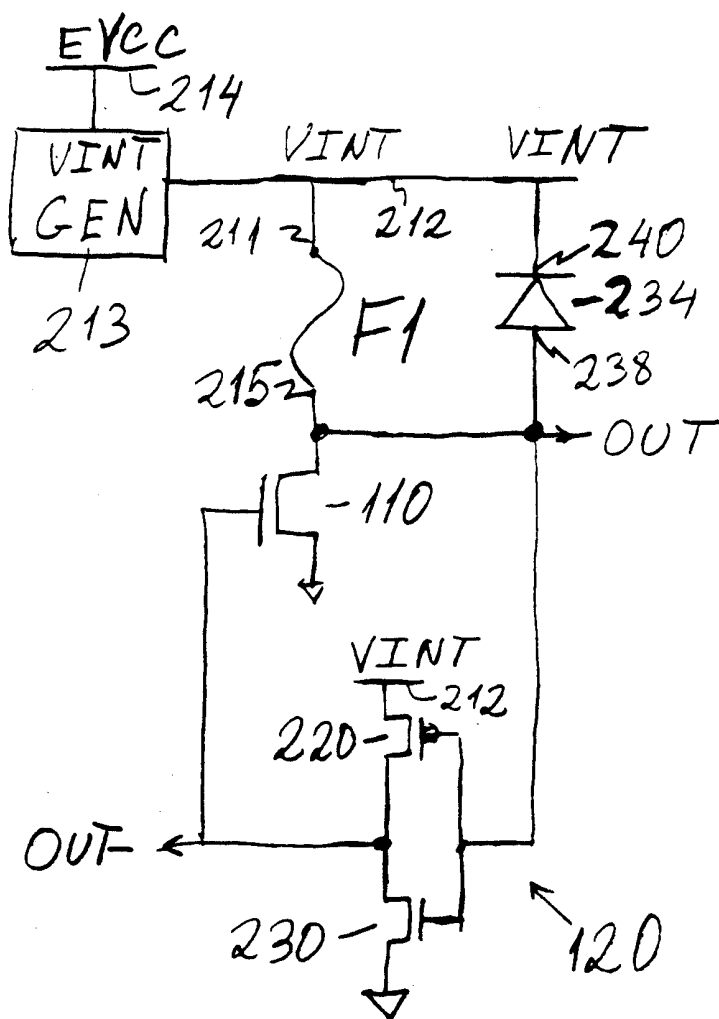


FIG. 2A

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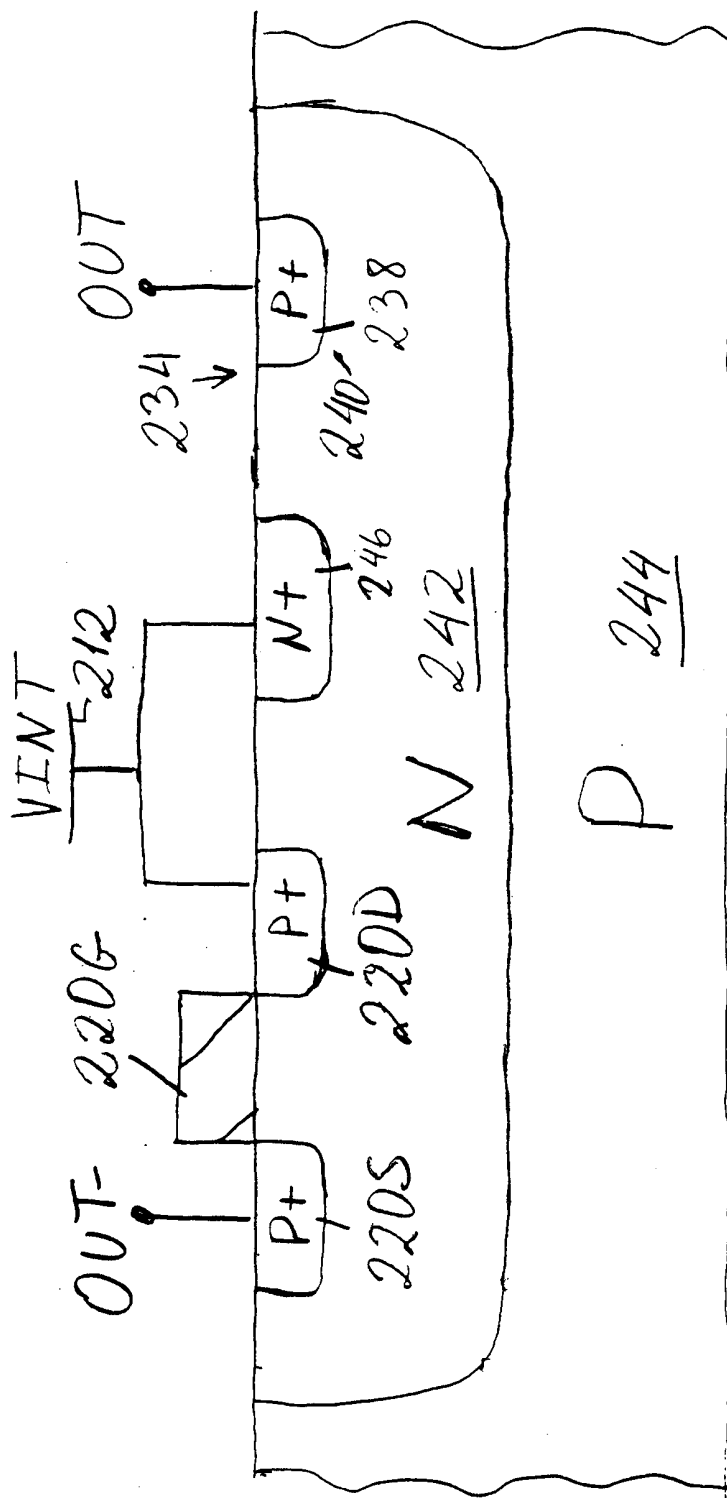


FIG. 2B

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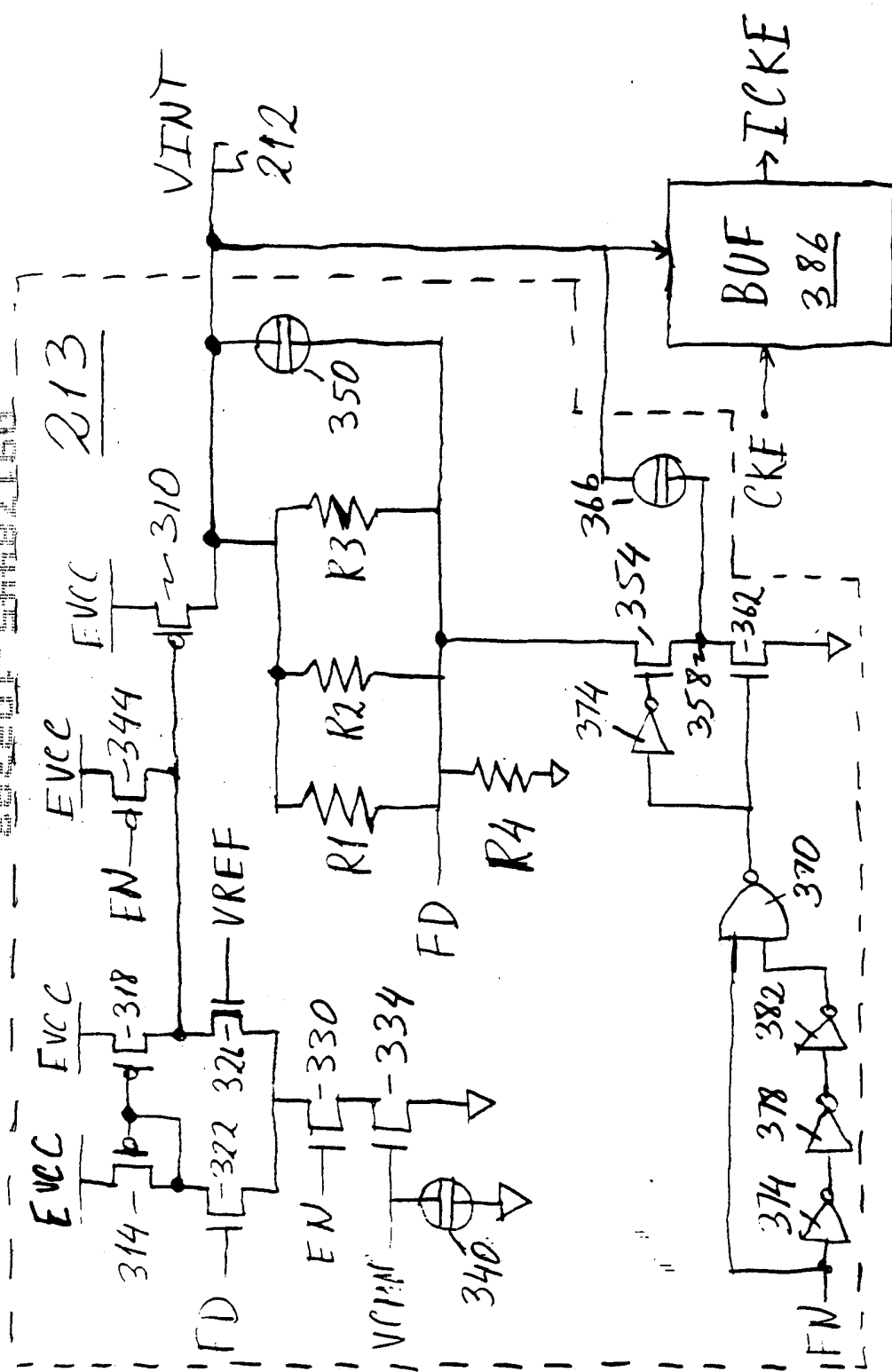


FIG. 3

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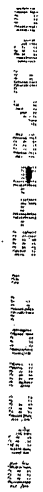


FIG. 4

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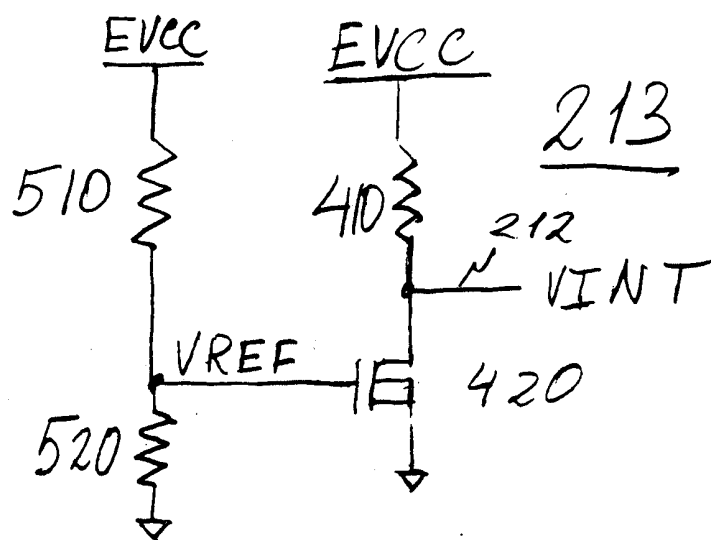


FIG. 5

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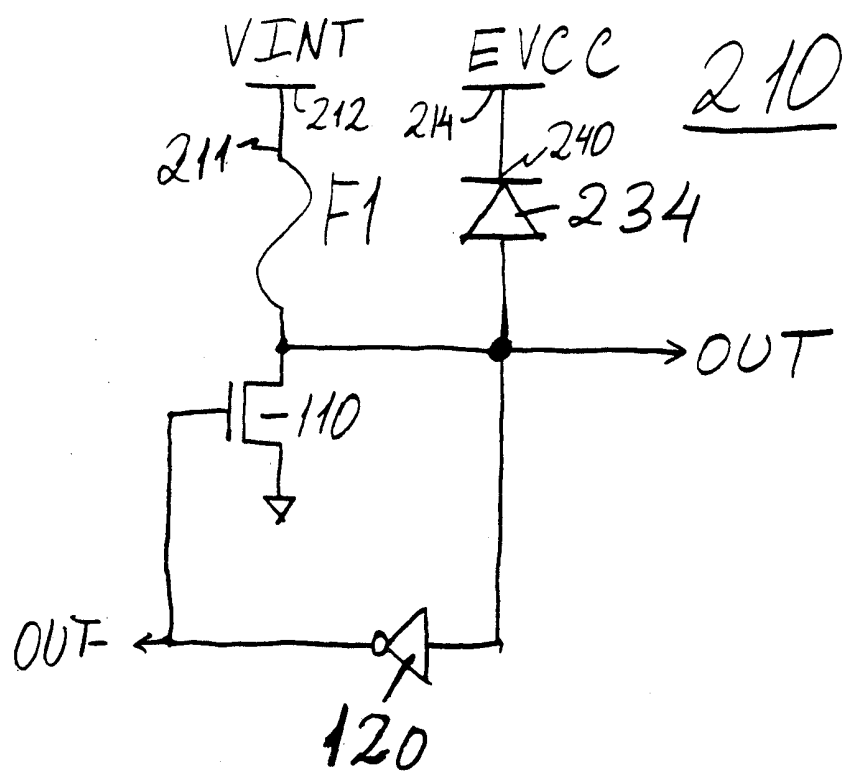
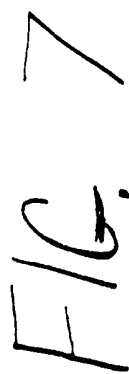
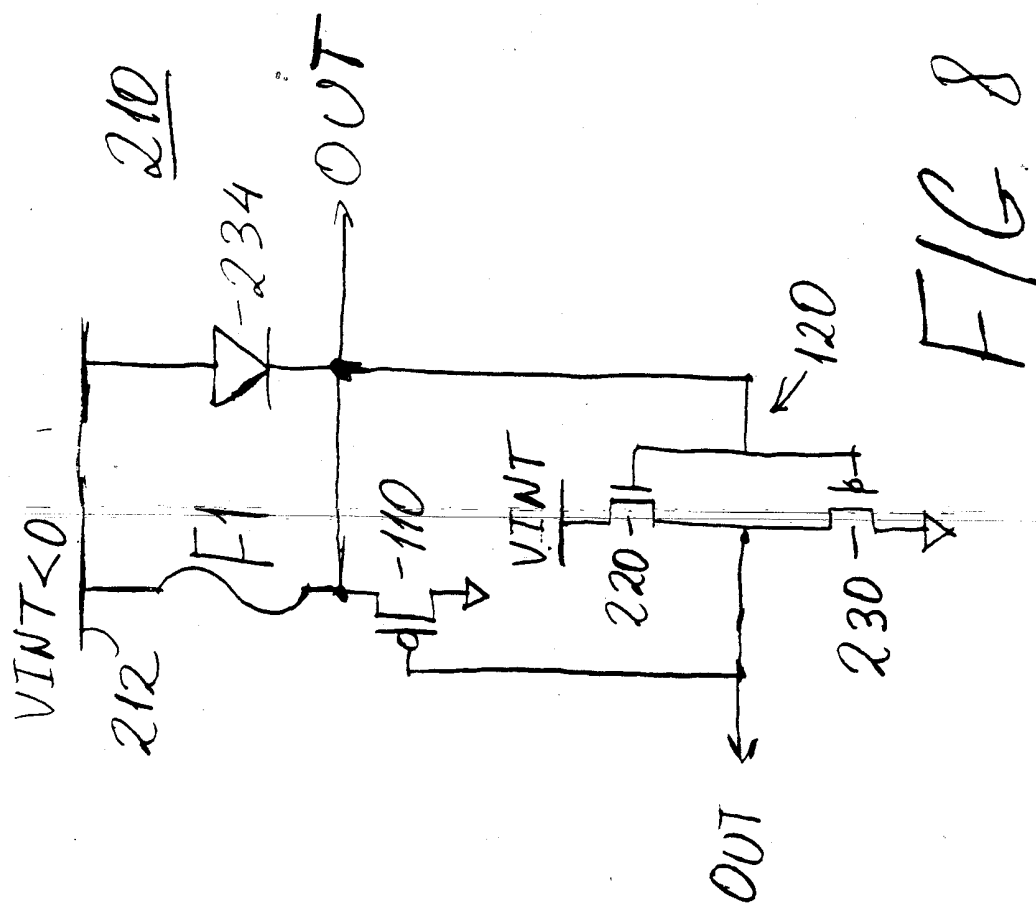


FIG. 6





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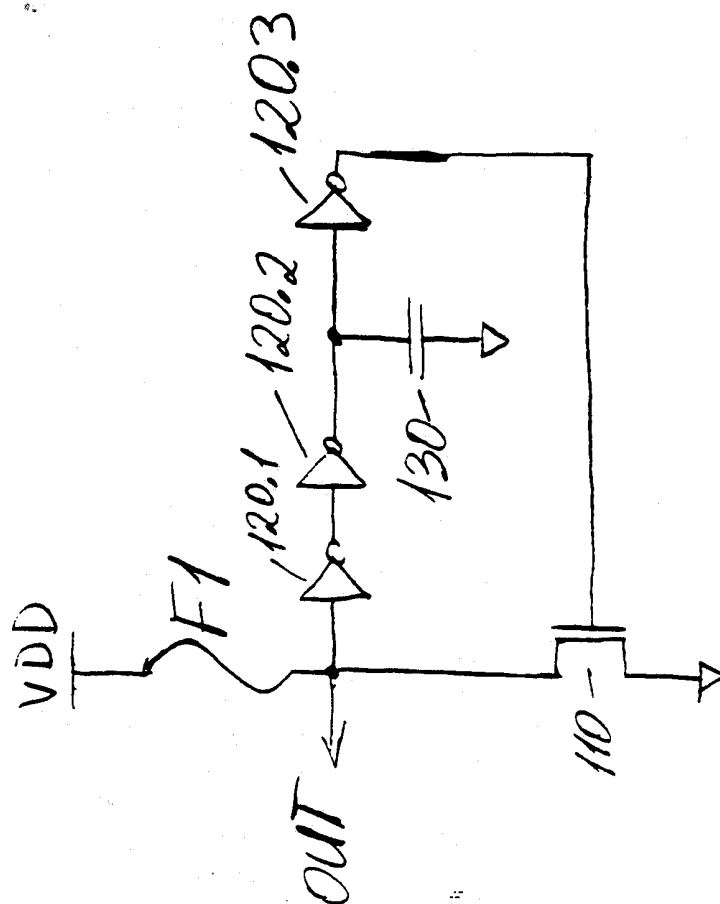


FIG. 1 PRIOR ART

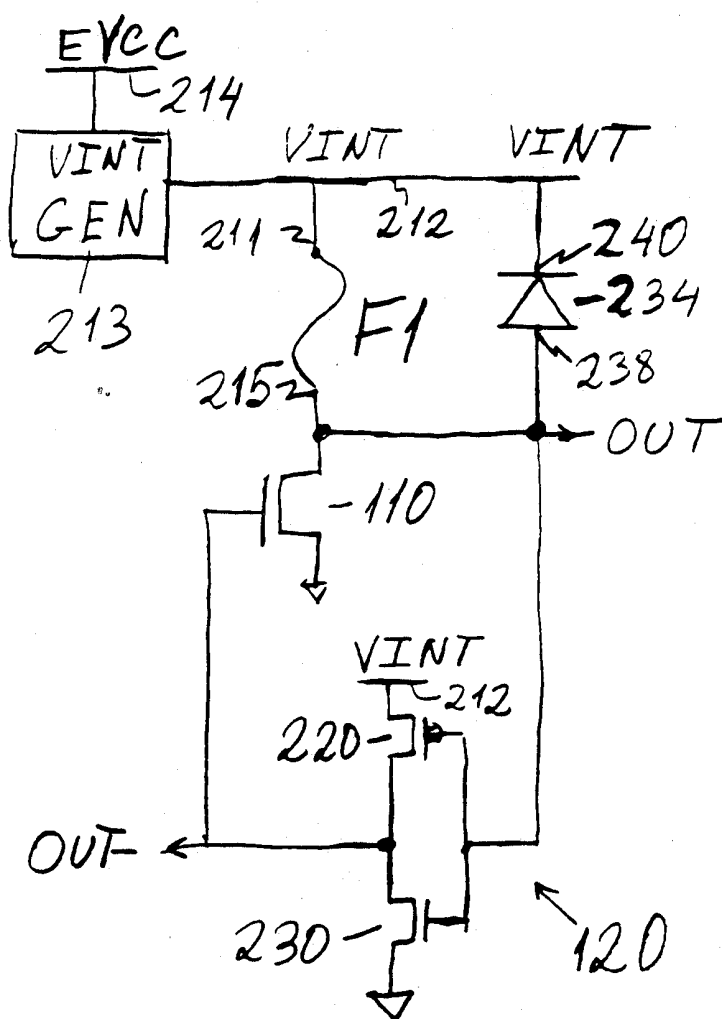


FIG. 2A

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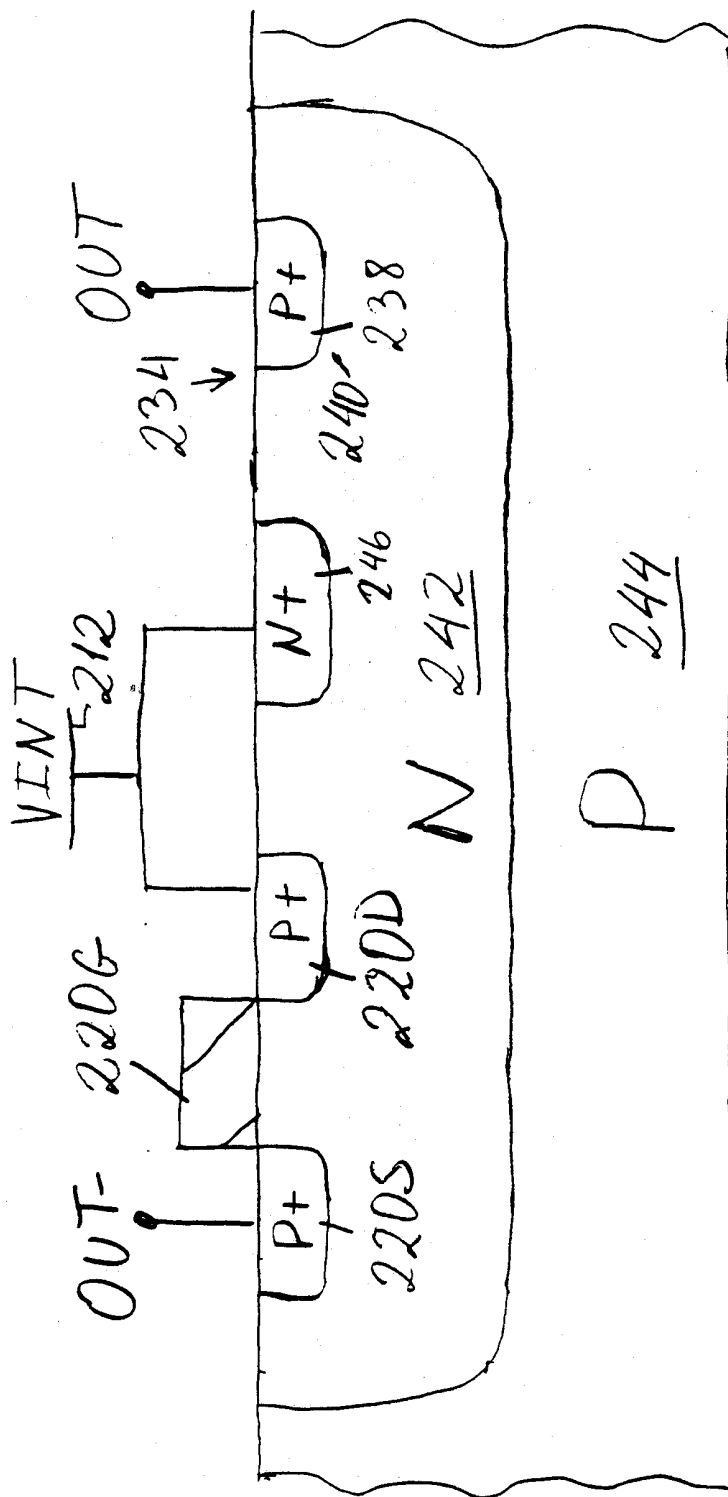


FIG. 2B

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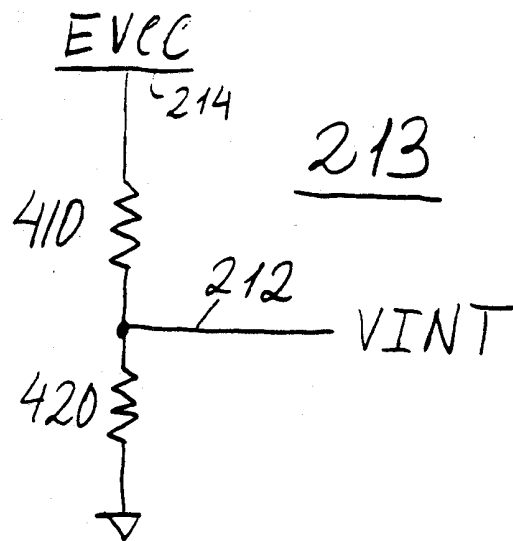


FIG. 4

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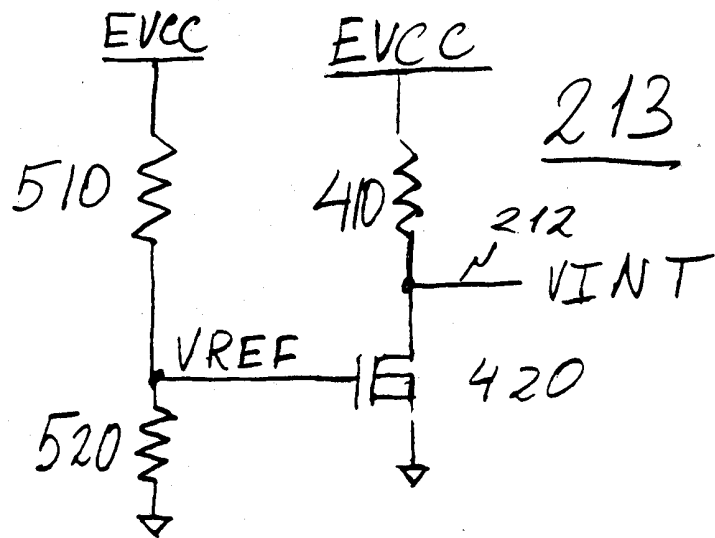


FIG. 5

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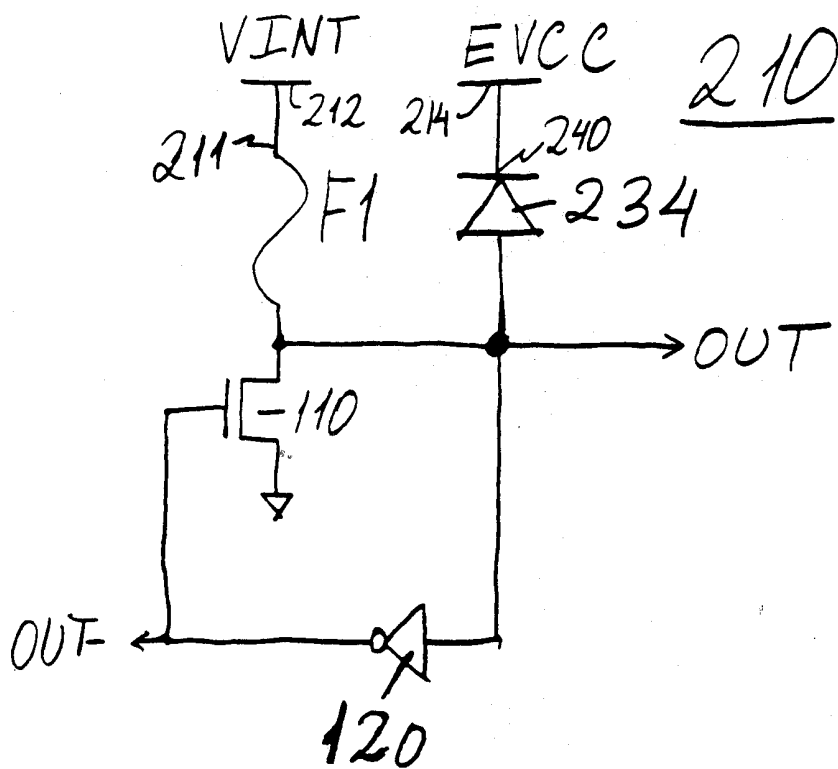


FIG. 6

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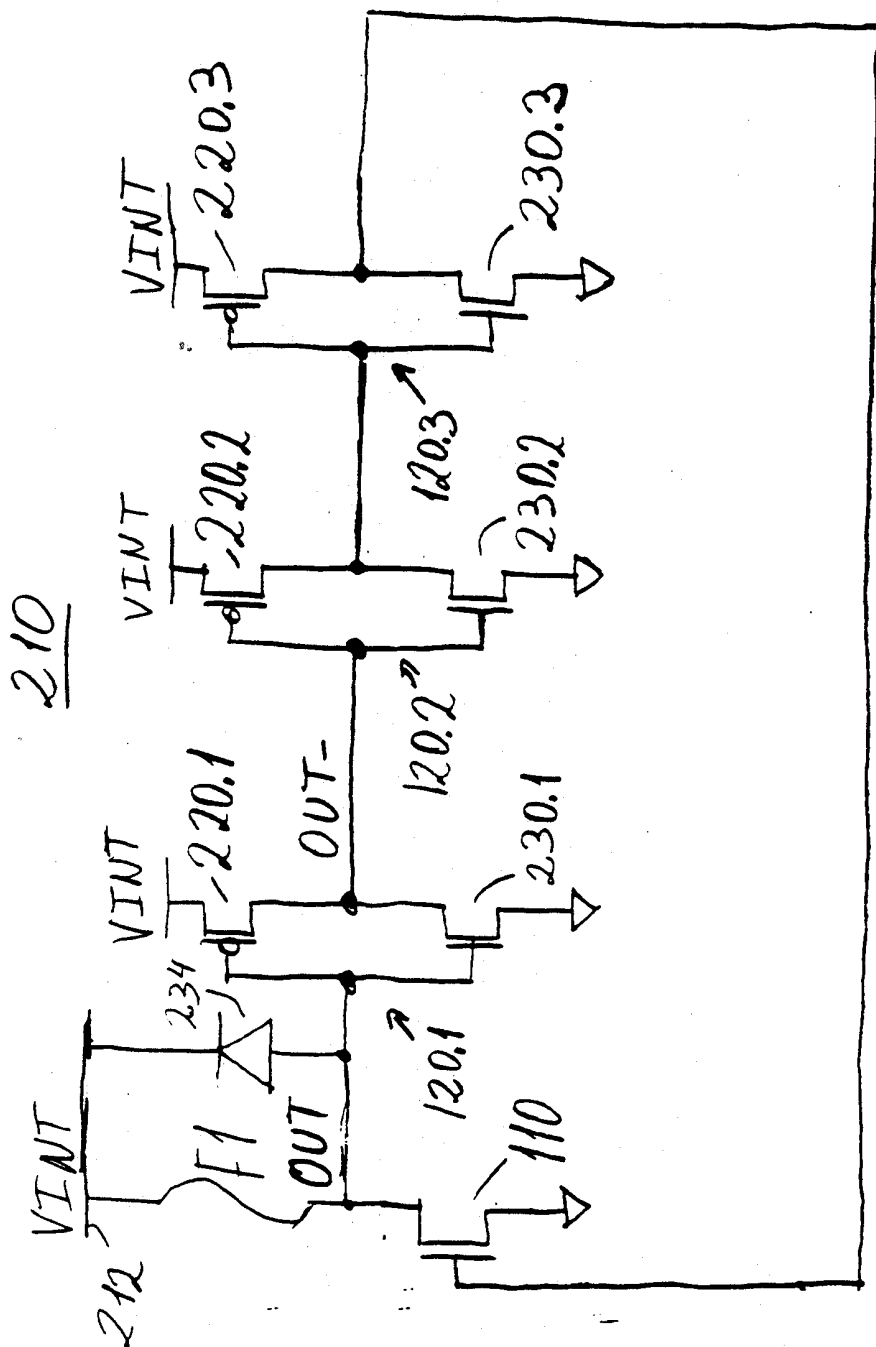
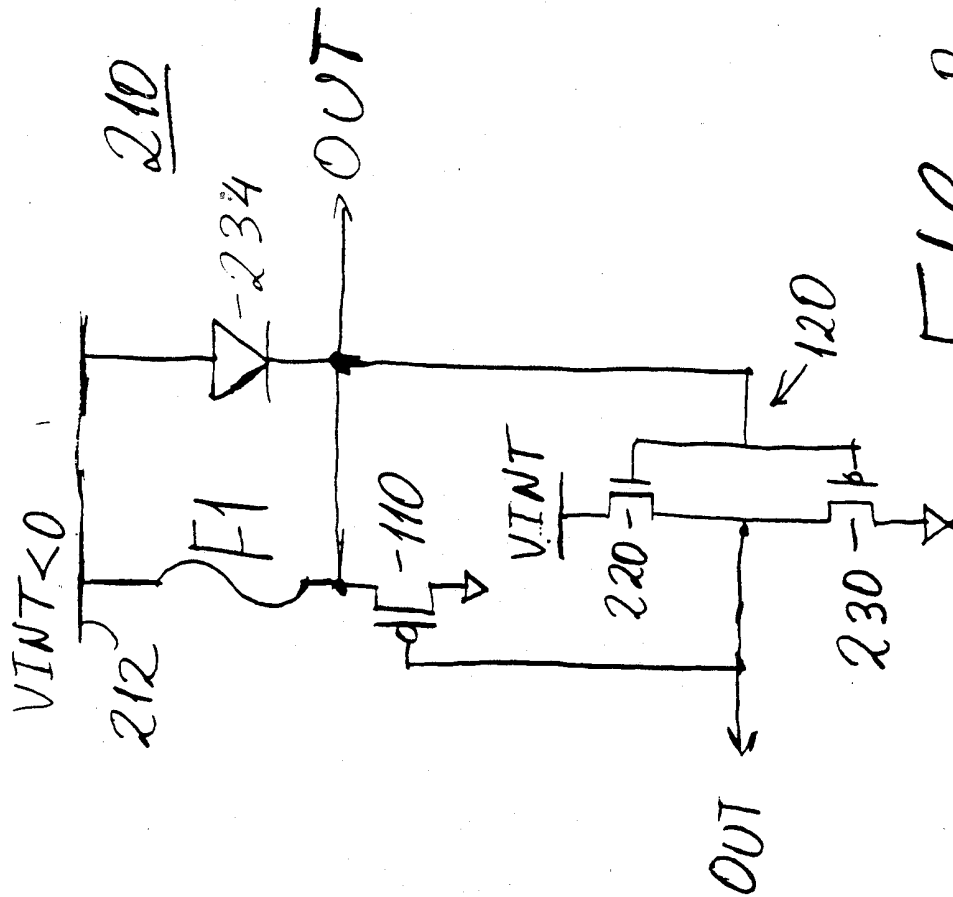


FIG. 7

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Sheet 1 of 1



F/G 8

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Sheet 2 of 2

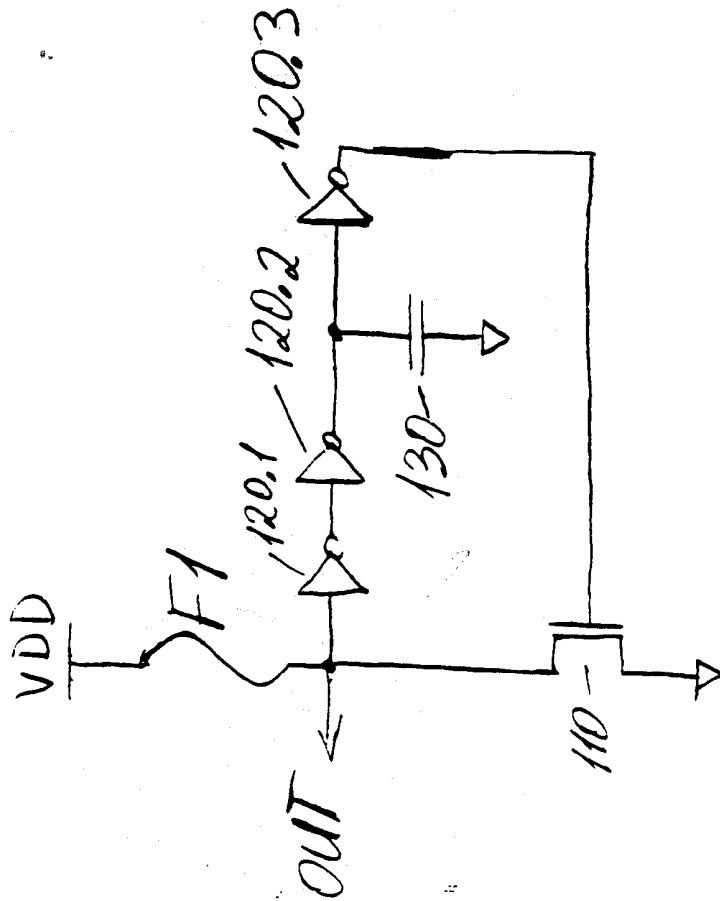


FIG. 1 PRIOR ART

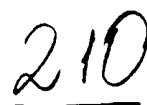


FIG. 2A

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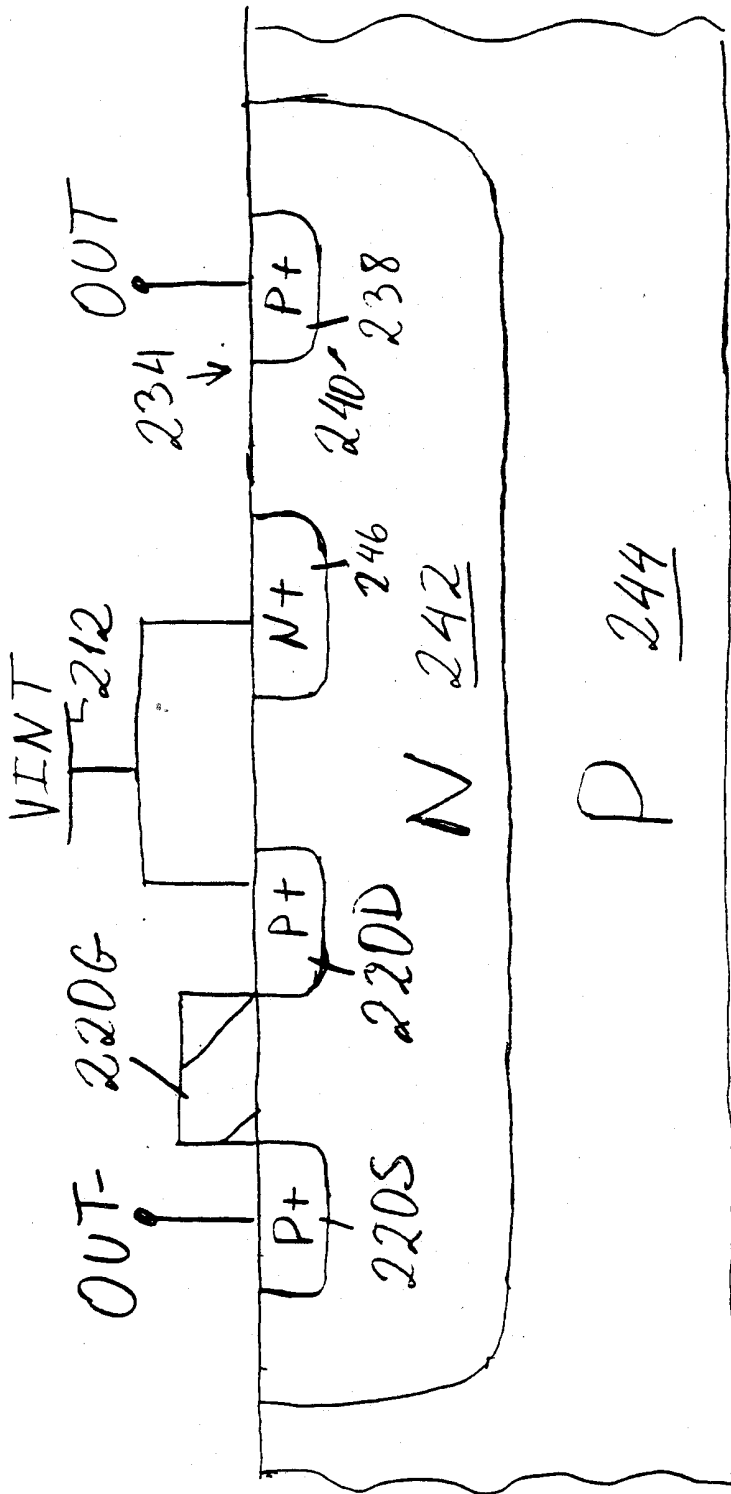


FIG. 2B

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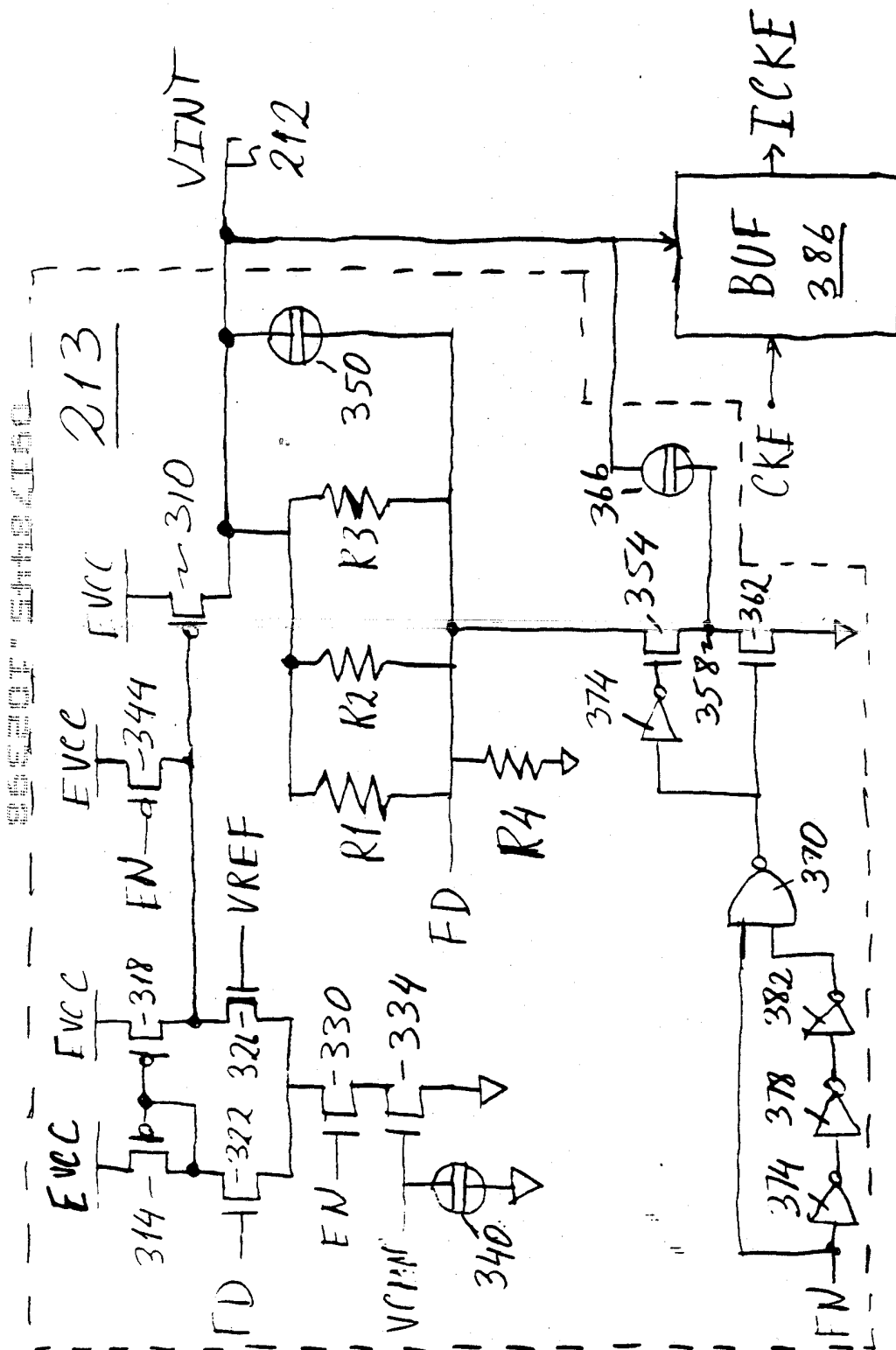


FIG. 3

FIG. 4

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Sheet 5 of 5

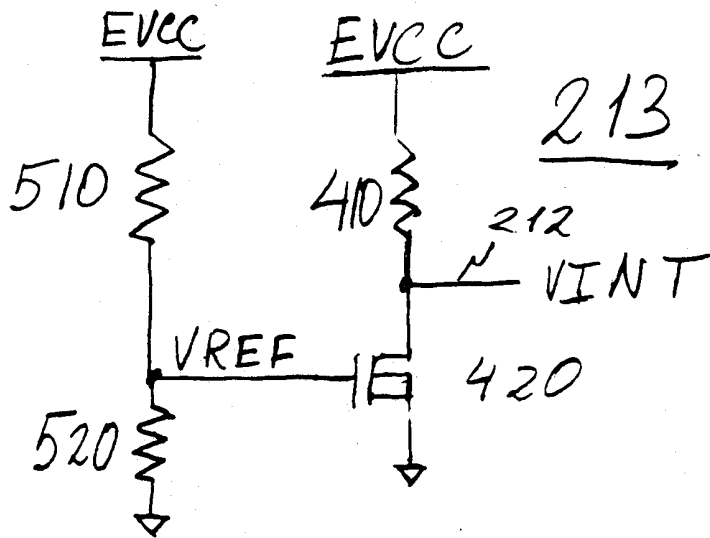


FIG. 5

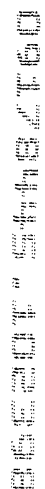


FIG. 6

Sheet 5 of 5

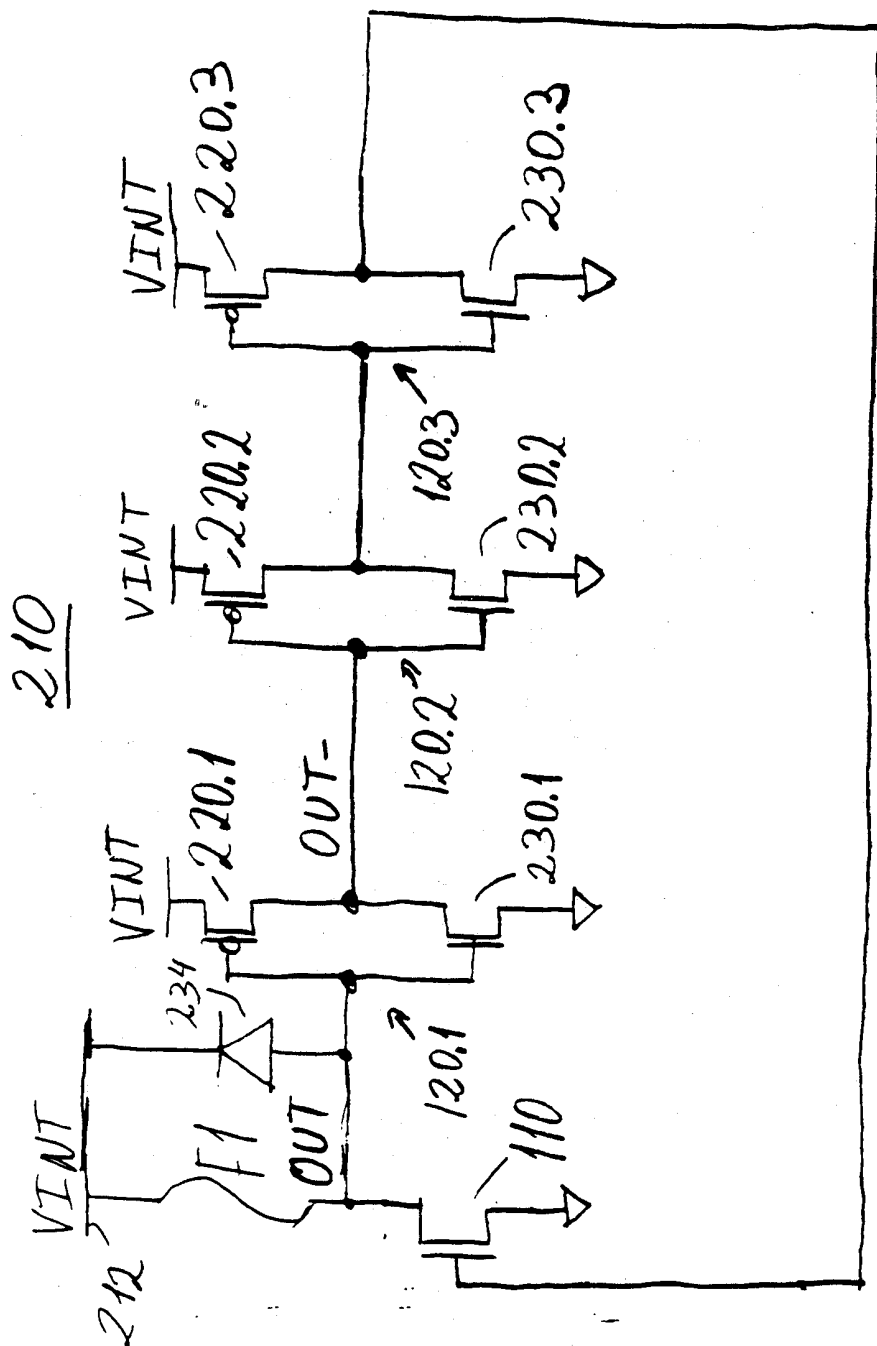
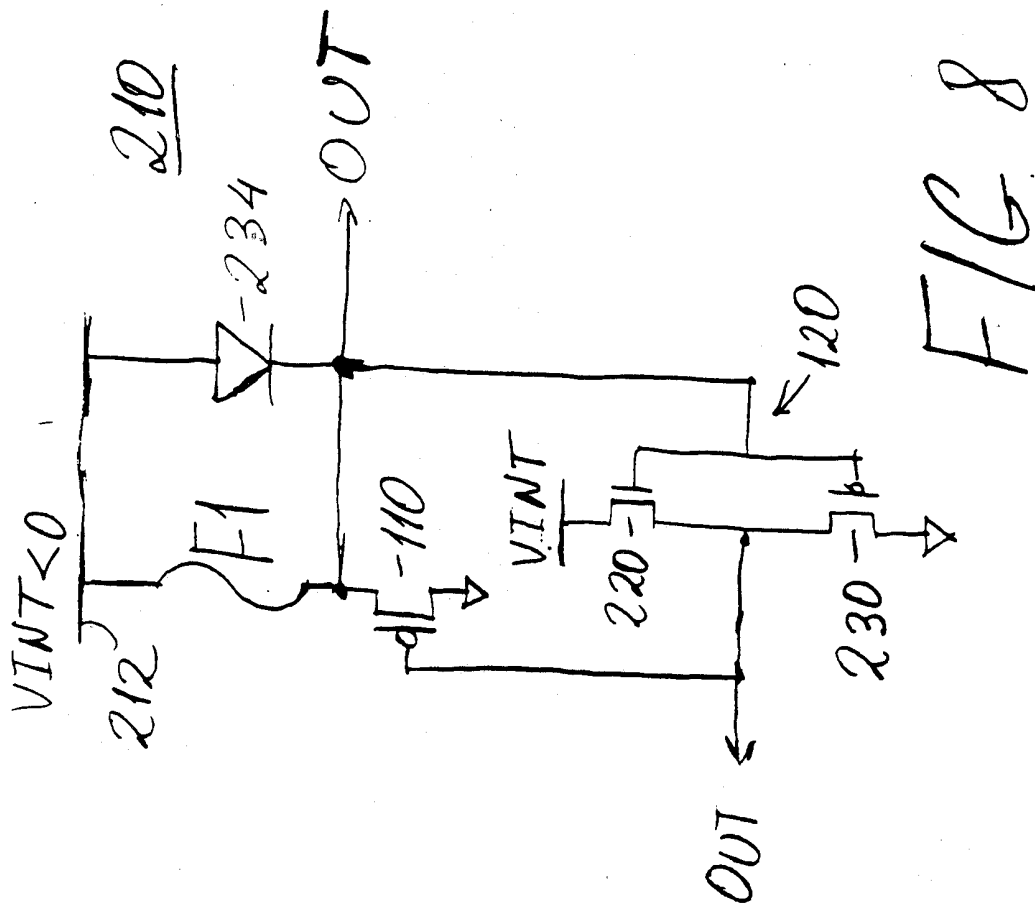


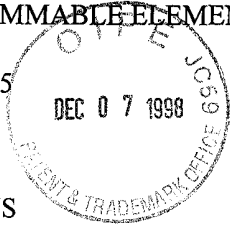
FIG. 7



GAU2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Sredanovic, Nikolas; Calendar, Helena
Assignee: Mosel Vitelic, Inc.
Title: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE PROGRAMMABLE ELEMENTS
Serial No.: 09/178,445
Examiner: Unknown
Docket No.: M-5598 US
Filed: October 23, 1998
Group Art Unit: Unknown



#2/IDS
5-1-99
JROC

San Jose, California
December 4, 1998

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants bring the documents listed in the enclosed form PTO-1449 to the Examiner's attention in the above-captioned application. Copies of the listed documents are enclosed.

Explanation of Relevance: The East German document DD 288689 discloses a CMOS redundancy decoder.

Citation of the listed documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231,

on Dec 4, 1998
Michael Shenker 12-4-98
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker
Michael Shenker
Attorney for Applicants
Reg. No. 34,250

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

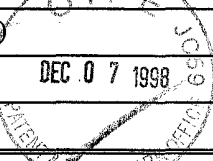
25 METRO DRIVE
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(408) 453-9200
FAX (408) 453-7979

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- 1 -

SER. NO. 09/178,445

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-5598 US		09/178,445	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Sredanovic, Nikolas; Calendar, Helena			
DEC 07 1998					Filing Date		Group	
					October 23, 1998		2818	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
VN	AA	4,387,503	6/14/83	Aswell et al.	29	575	8/13/81	
VN	AB	4,404,635	9/13/83	Flaker	364	481	3/27/81	
VN	AC	4,532,607	7/30/85	Uchida	365	96	7/16/82	
VN	AD	4,546,455	10/8/85	Iwahashi et al.	365	200	12/3/82	
VN	AE	4,614,881	9/30/86	Yoshida et al.	307	219	1/27/84	
VN	AF	4,617,651	10/14/86	Ip et al.	365	200	2/22/84	
VN	AG	4,725,979	2/16/88	Hoberman	365	96	12/5/96	
VN	AH	4,771,285	9/13/88	Agrawal et al.	340	825	11/5/85	
VN	AI	4,779,229	10/18/88	Agrawal	365	94	7/2/86	
VN	AJ	4,837,520	6/6/89	Golke et al.	324	550	11/12/87	
VN	AK	4,852,044	7/25/89	Turner et al.	364	900	8/22/88	
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
VN	AL	DD 288 689	10/27/83	East Germany				
	AM							
	AN	Vict Q. Nguyen Primary Examiner						
	AO	Vict Q. Nguyen Primary Examiner						
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
VN	AQ	B. Prince, "High Performance Memories" New Architecture DRAMs and SRAMs Evolution and Function, 1996 , pp. 135-227.						
VN	AR	B. Prince, "Semiconductor Memories" A Handbook of Design, Manufacture and Application, Second Edition, (1991), pp. 762-764						
VN	AS	"Synchronous Graphics RAM" Micron Technology, Inc. of Boise Idaho, 1998, pp. 1-45						
Examiner		V. NGUYEN		Date Considered		2/13/00		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-5598 US		09/178,445	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Sredanovic, Nikolas; Calendar, Helena			
					Filing Date		Group	
					October 23, 1998		Unknown	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
VN	AA	4,943,804	7/24/90	Lee et al.	340	825	9/26/89	
VN	AB	5,066,998	11/19/91	Fischer et al.	357	51	8/20/90	
VN	AC	5,086,331	2/4/92	Hartgring et al.	357	51	1/18/91	
VN	AD	5,134,585	7/28/92	Murakami et al.	365	200	3/29/90	
VN	AE	5,185,291	2/9/93	Fischer et al.	437	173	9/6/91	
VN	AF	5,285,953	2/11/93	Tsujimoto	365	200	6/25/92	
VN	AG	5,440,246	8/8/95	Murray et al.	326	38	3/22/94	
VN	AH	5,566,107	10/15/96	Gilliam	365	200	5/5/95	
VN	AI	5,506,638	4/16/96	Cowles et al.	326	38	5/26/95	
VN	AJ	5,459,684	10/17/95	Nakamura et al.	365	149	2/16/94	
VN	AK	4,532,402	7/30/85	Overbeck	219	121 LU	9/2/83	
AL								
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AR							
	AS							
	AT							
Examiner		V. NGUYEN		Date Considered		2/13/00		GROUP 2100
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

54

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/178,445	10/23/98	SREDANOVIC	N M-5598-US

MM42/0114

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

EXAMINER

NGUYEN, V

ART UNIT	PAPER NUMBER
2818	3

DATE MAILED: 01/14/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No. 09/178,445 Applicant(s)Examiner V. NGUYENGroup Art Unit 2818

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 ~~TH~~ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☐ Responsive to communication(s) filed on _____.
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1-31 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☐ Claim(s) _____ is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☒ Claim(s) 1-31 are subject to restriction or election requirement.

Application Papers

- ☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
 - ☐ received in Application No. (Series Code/Serial Number) _____.
 - ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
- ☐ Interview Summary, PTO-413
- ☐ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Informal Patent Application, PTO-152
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Other _____

Office Action Summary

Art Unit: 2818

This application contains claims directed to the following patentably distinct species of the claimed invention: Group I, claims 1-13, 16-23 are drawn to a programmable latch having a programmable electrical path, a variable-impedance electrical path, and a diode for keeping a voltage on the terminal T, within a predetermined range of values before power is supplied to the latch to prevent the latch from assuming an incorrect date when power is supplied to the latch;

Group II, claims 14-15 are drawn to a method for generating a signal indicating a state of non-volatile programmable element;

Group III, claims 24-29 are drawn to a programmable latch having a non-volatile programmable element, a variable-impedance electrical path, and one or more connected inverters wherein no capacitor is provided between an input of any inverter and a second terminal, etc.,

Group IV, claims 30-31 are drawn to a method for providing a signal indicating a state of non-volatile element having steps of "controlling an impedance of the variable-impedance electrical path...", etc

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable

Art Unit: 2818

thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication should be directed to Viet Nguyen at telephone number (703) 308-4897.

VN
Nguyen/ds

01/10/00



Viet Q. Nguyen
Primary Examiner

178445

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 10/23/98 are:A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:

Black ink. Color.

☐ Color drawings are not acceptable until petition is granted.

Fig(s) _____

☐ Pencil and non black ink not permitted. Fig(s) _____

2. PHOTOGRAPHS. 37 CFR 1.84 (b)

☐ 1 full-tone set is required. Fig(s) _____☐ Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____☐ Poor quality (half-tone). Fig(s) _____

3. TYPE OF PAPER. 37 CFR 1.84(e)

☐ Paper not flexible, strong, white, and durable.

Fig(s) _____

☒ Erasures, alterations, overwritings, interlineations,folds, copy machine marks not accepted. Fig(s) 1-8☐ Mylar, vellum paper is not acceptable (too thin).

Fig(s) _____

4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:

☐ 21.0 cm by 29.7 cm (DIN size A4)☐ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)☐ All drawing sheets not the same size.

Sheet(s) _____

☐ Drawings sheets not an acceptable size. Fig(s) _____

5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm

SIZE: A4 Size

Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm

SIZE: 8 1/2 x 11

Margins not acceptable. Fig(s) 2b, 3, 6☒ Top (T) 2b, 3, 6 Left (L)☐ Right (R) _____ Bottom (B)

6. VIEWS. 37 CFR 1.84(h)

REMINDER: Specification may require revision to correspond to drawing changes.

Partial views. 37 CFR 1.84(h)(2)

☐ Brackets needed to show figure as one entity.

Fig(s) _____

☐ Views not labeled separately or properly.

Fig(s) _____

☐ Enlarged view not labeled separately or properly.

Fig(s) _____

7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)

☐ Hatching not indicated for sectional portions of an object.

Fig(s) _____

☐ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)

☐ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. SCALE. 37 CFR 1.84(k)

☐ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.

Fig(s) _____

10. CHARACTER OF LINES, NUMBERS, & LETTERS.

37 CFR 1.84(i)

☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).Fig(s) 1-8

11. SHADING. 37 CFR 1.84(m)

☐ Solid black areas pale. Fig(s) _____☐ Solid black shading not permitted. Fig(s) _____☐ Shade lines, pale, rough and blurred. Fig(s) _____

12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.

37 CFR 1.84(p)

☒ Numbers and reference characters not plain and legible.Fig(s) 1-8☒ Figure legends are poor. Fig(s) 1-8☐ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)

Fig(s) _____

☐ English alphabet not used. 37 CFR 1.84(p)(2)

Figs _____

☐ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)

Fig(s) _____

13. LEAD LINES. 37 CFR 1.84(q)

☐ Lead lines cross each other. Fig(s) _____☐ Lead lines missing. Fig(s) _____

14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)

☐ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____

15. NUMBERING OF VIEWS. 37 CFR 1.84(u)

☐ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____

16. CORRECTIONS. 37 CFR 1.84(w)

☐ Corrections not made from prior PTO-948 dated _____

17. DESIGN DRAWINGS. 37 CFR 1.152

☐ Surface shading shown not appropriate. Fig(s) _____☐ Solid black shading not used for color contrast.

Fig(s) _____

COMMENTS

REVIEWER [Signature]DATE 11/12/98TELEPHONE NO. 305-8406ATTACHMENT TO PAPER NO. [Signature]

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

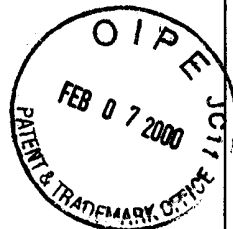
2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.



GP 2818
#4/Electr
5/18/00
Tia

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sredanovic, Nikolas; Calendar, Helena
Assignee: Mosel Vitelic, Inc.
Title: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE PROGRAMMABLE ELEMENTS
Serial No.: 09/178,445 Filed: 10/23/98
Examiner: V. Nguyen Group Art Unit: 2818
Docket No.: M-5598 US

RECEIVED San Jose, California

FEB 10 2000

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

TECHNOLOGY CENTER 2800

RESPONSE TO RESTRICTION REQUIREMENT

Dear Sir:

The Office Action dated January 14, 2000 requires Applicants to elect one of the following groups of claims.

Group I, Claims 1-13, 16-23;

Group II, Claims 14-15;

Group III, Claims 24-29;

Group IV, Claims 30-31.

In response, Applicants elect Group I, Claims 1-13, 16-23.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Feb. 2, 2000.

Michael Shenker 2-2-00
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicants
Reg. No. 34,250

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

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v11



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
--------------------	-------------	-----------------------	---------------------

09/178,445 10/23/98 SREDANOVIC N M-5598-US

MM42/0229

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

EXAMINER

NGUYEN, V

ART UNIT

PAPER NUMBER

2818

DATE MAILED:

02/29/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Election filed on 2/7/00

☒ The allowed claim(s) is/are 1-13, 16-23

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. 5

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

PTOL-37 (Rev. 8/97)

*U.S. GPO:1998/444-443

Viet Nguyen

Viet Q. Nguyen
Primary Examiner

5/A

Application/Control Number: 09/178,445

Page 2

Art Unit: 2818

DETAILED ACTION

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance:

The prior arts fail to teach or fairly suggest a programmable latch having first terminal, second terminal, a terminal for indicating a state of programmable latch, a programmable electrical path, a variable-impedance electrical path between the terminal and the second terminal, and a diode for keeping a voltage on the terminal within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Application/Control Number: 09/178,445

Page 3

Art Unit: 2818

Examiner's Amendment

Claims 14-15 and 24-31 are canceled as directed to a non-elected invention.

2. Any inquiry concerning this communication should be directed to Viet Nguyen at the number (703) 308-4897.

VN

V. Nguyen

2/13/00

Viet Nguyen

Viet Q. Nguyen
Primary Examiner

Notice of References Cited	Application No. 09/178,445	Applicant(s) Sredanovic, et al	
	Examiner V. Nguyen	Group Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS					
*		DOCUMENT NO.	DATE	NAME	CLASS SUBCLASS
A		5,696,455	12/9/97	Madurawe	326 41
B		5,892,712	4/6/99	Hrose et al	365 185.02
C		5,455,937	6/3/95	Berman et al	295 500
D		4,571,704	2/18/86	Bohac, Jr.	365 156
E					
F					
G					
H					
I					
J					
K					
L					
M					

FOREIGN PATENT DOCUMENTS						
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS SUBCLASS
N						
O						
P						
Q					Viet Q. Nguyen	
R					Primary Examiner	
S						
T						

NON-PATENT DOCUMENTS		
*	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V	Viet Q. Nguyen Primary Examiner	
W		
X		



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM42/0229

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE, CA 95110-1349

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/178,445	10/23/98	021	NGUYEN, V 2818	02/29/00
First Named Applicant	BREDANDVIC	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE PROGRAMMABLE ELEMENTS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 M-5528-US	365-225.700	186	UTILITY	NO	\$1210.00	05/30/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
 - If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
 - If the status is the same, pay the FEE DUE shown above.
 - Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
 - All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.
- If the SMALL ENTITY is shown as NO:

 - Pay FEE DUE shown above, or
 - File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

7560/7530
04/10/00 B

BEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Calendar, Helena; Sredanovic, Nikolas
Assignee: Mosel Vitelic, Inc.
Title: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE
PROGRAMMABLE ELEMENTS
Serial No.: 09/178,445 Filed: 10/23/98
Batch No.: I86 Date Allowed: February 29, 2000
Examiner: V. Nguyen Group Art Unit: 2818
Docket No.: M-5598 US



ISSUE FEE DUE MAY 30, 2000

San Jose, California
March 24, 2000

BOX ISSUE FEE
Attn: Official Draftsperson
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit five (5) sheets of formal drawings, consisting of Figures 1, 2A, 2B, 3, 4, 5, 6, 7 and 8, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at 408/453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Mar. 24, 2000.

Michael Shenker 3-24-00
Attorney for Applicants Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicants
Reg. No. 34,250

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LAW OFFICES OF
SKJERNEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

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(408) 453-9200
FAX (408) 453-7979

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- 1 -

SER. NO.

6163492

1/5

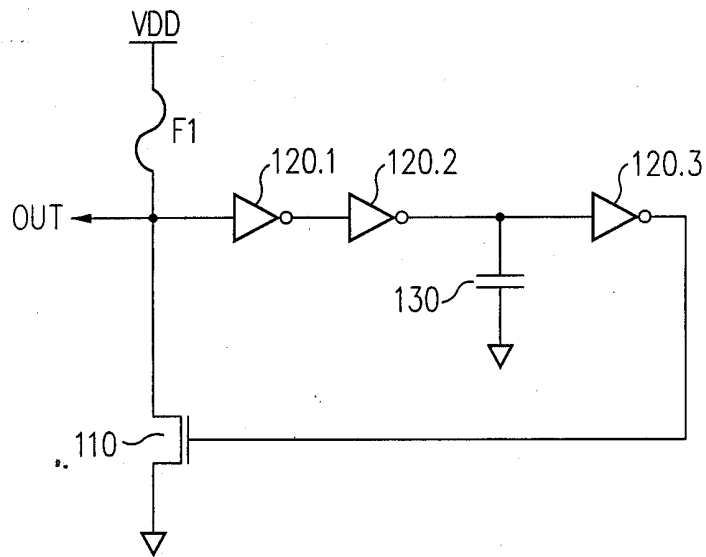


FIG. 1
(PRIOR ART)

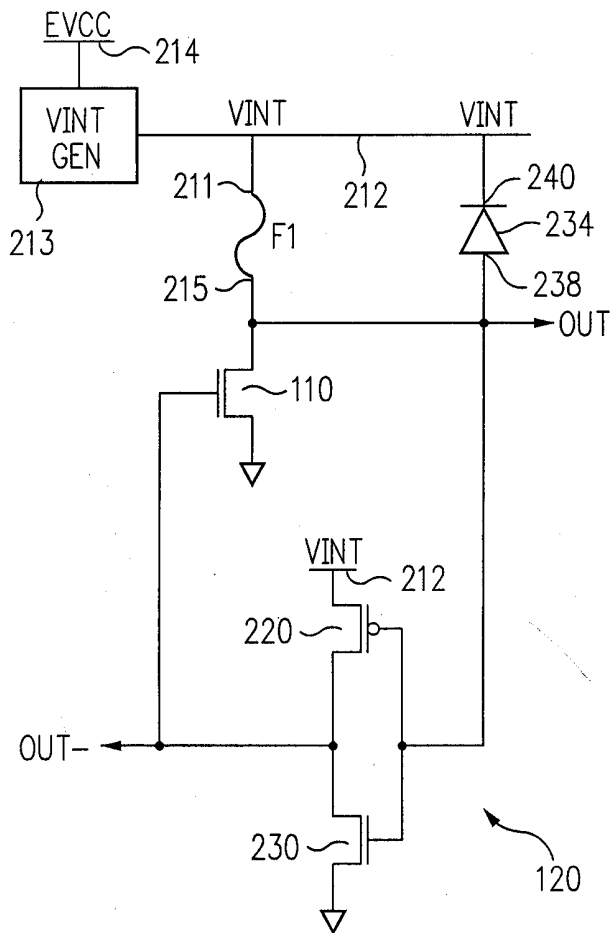


FIG. 2A

210

DRAFT

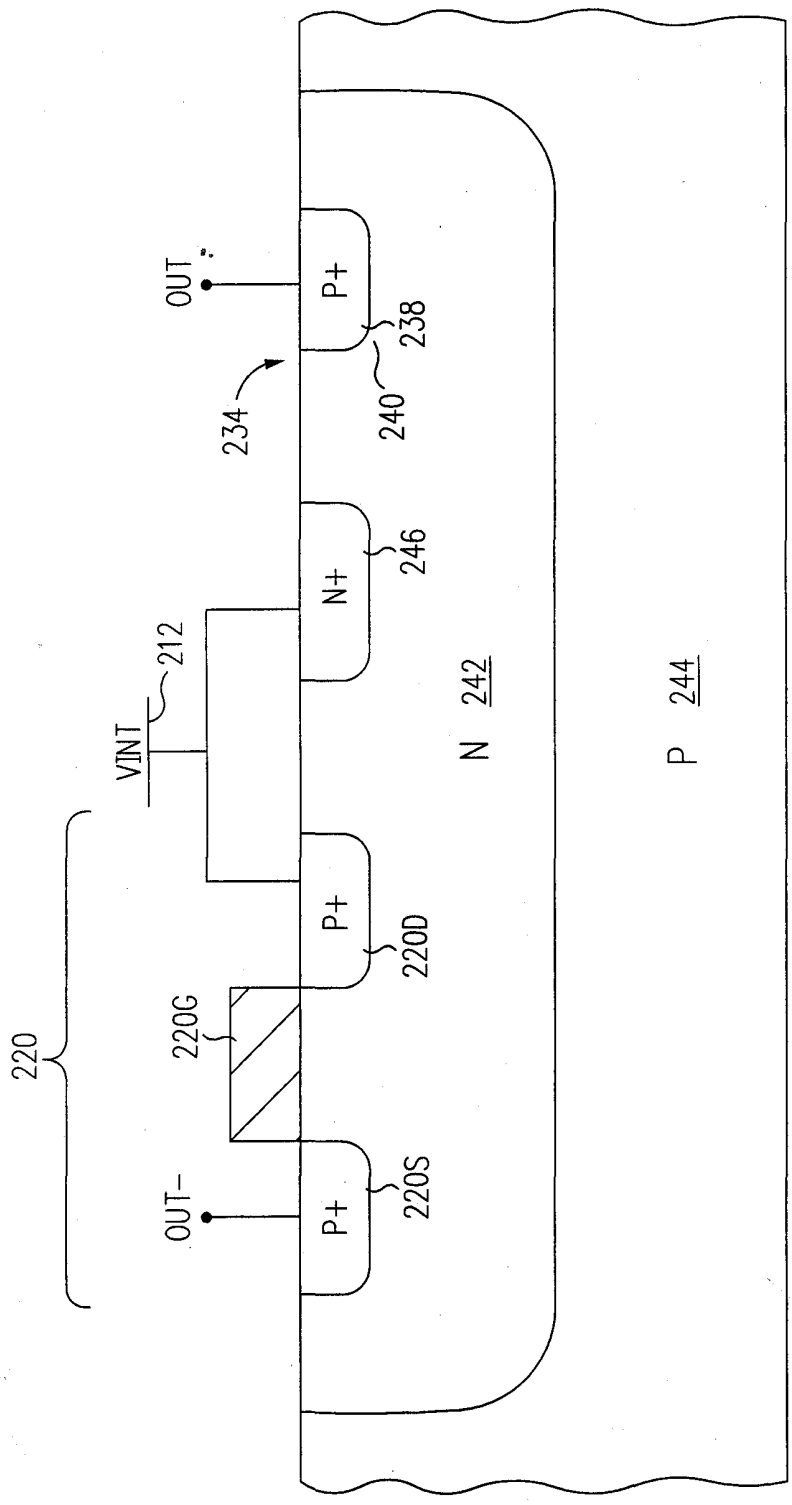


FIG. 2B

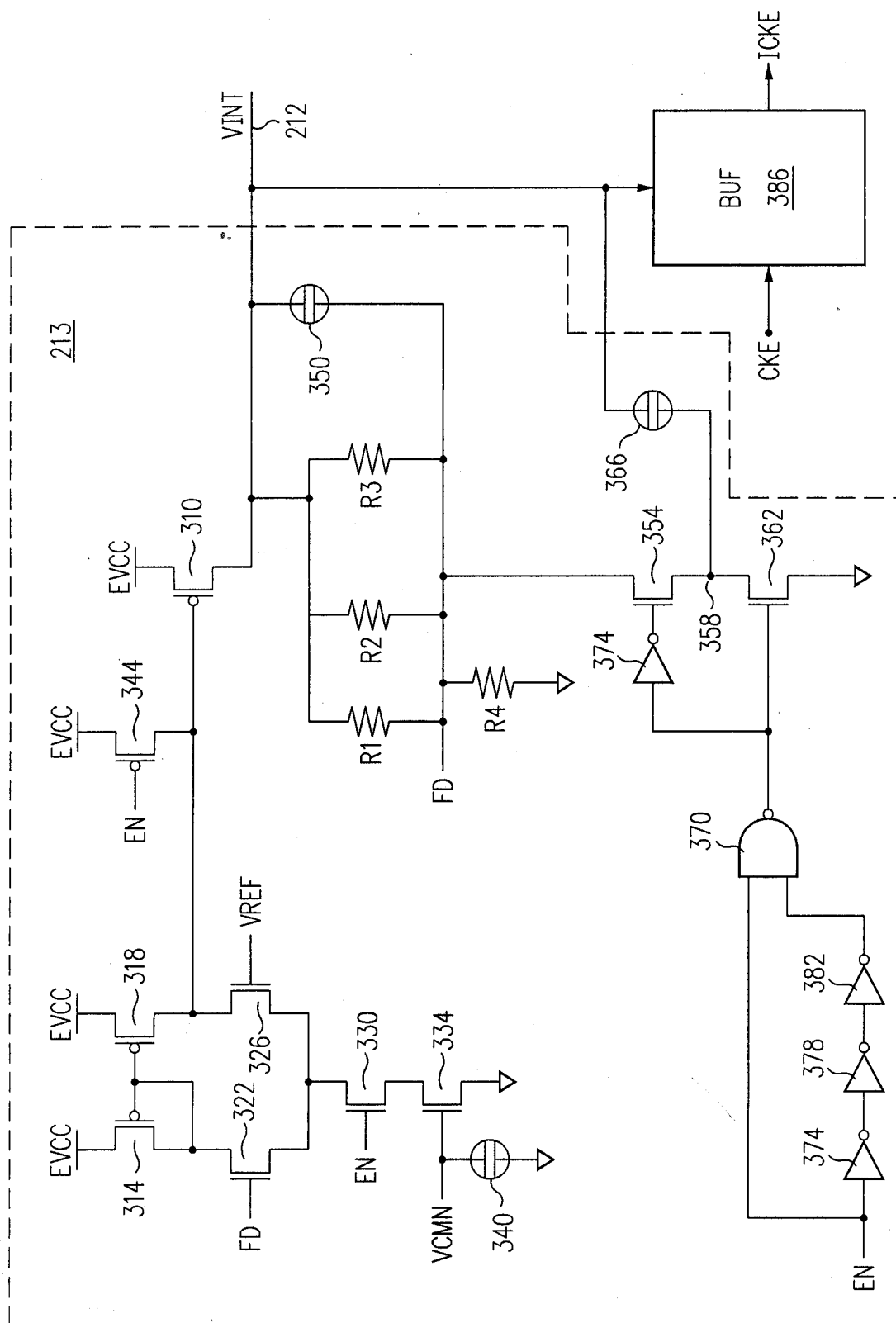


FIG. 3



4/5

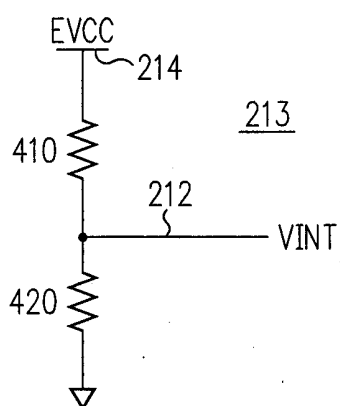


FIG. 4

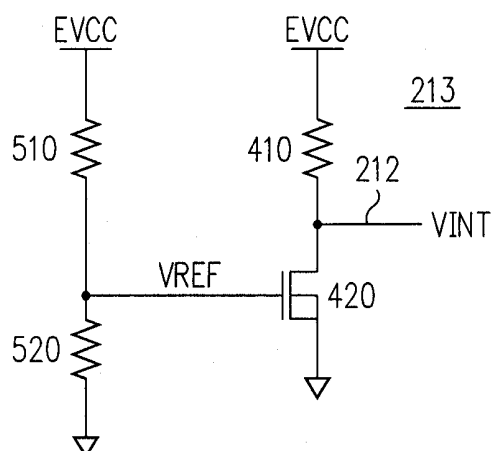


FIG. 5

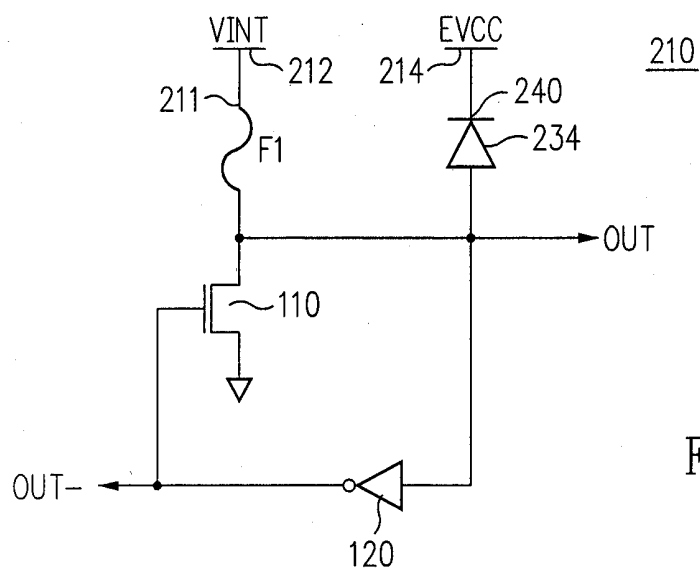


FIG. 6

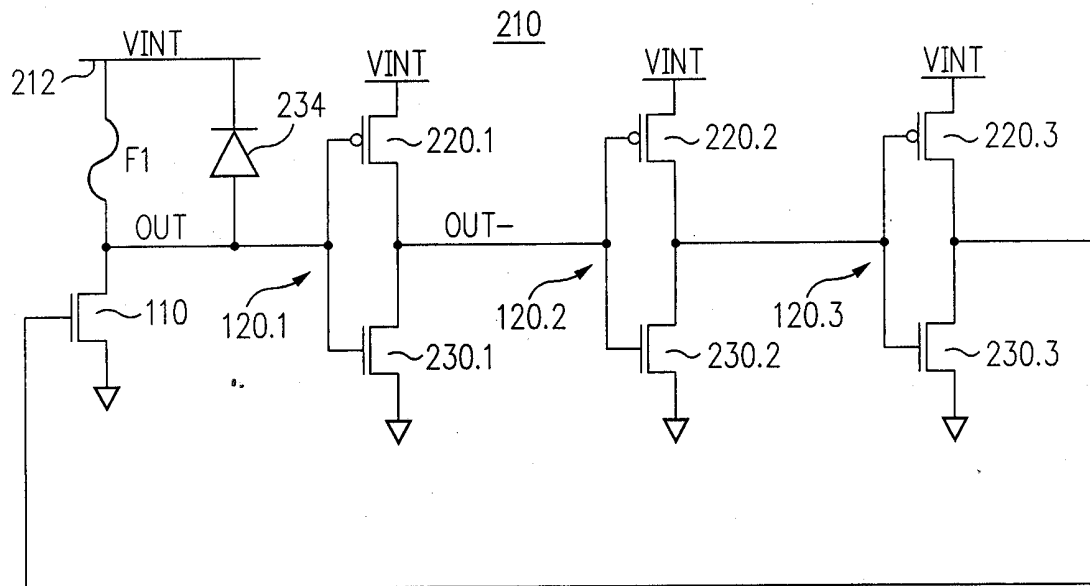


FIG. 7

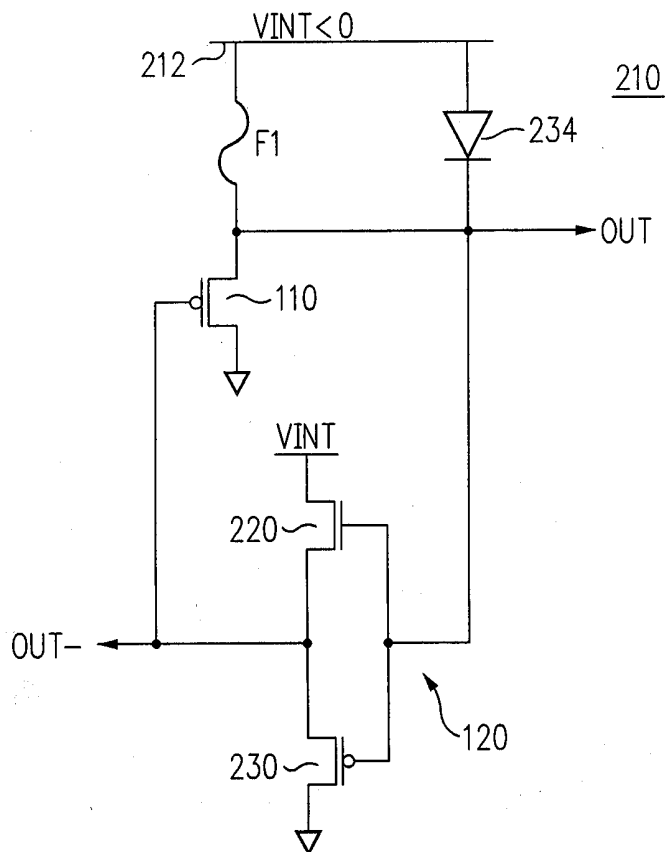


FIG. 8



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/178,445	10/23/98	SREDANOVIC	N M-5598-US

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

MM41/0823

EXAMINER
NGUYEN, V

ART UNIT PAPER NUMBER
2818 6

DATE MAILED: 08/23/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Election filed on 2/7/00.

☒ The allowed claim(s) is/are ~~1-13~~ 1-13, 16-23.

☒ The drawings filed on 3/28/00 are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Draftperson's Patent Drawing Review, PTO-948 (Approved)

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

Viet Q. Nguyen
Primary Examiner

09/178445

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 3/28/00 are:A. ☒ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color. _____
Color drawings are not acceptable until petition is granted.
Fig(s) _____
Pencil and non black ink not permitted. Fig(s) _____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
1 full-tone set is required. Fig(s) _____
Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s) _____
Poor quality (half-tone). Fig(s) _____
3. TYPE OF PAPER. 37 CFR 1.84(e)
Paper not flexible, strong, white, and durable. Fig(s) _____
Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____
Mylar, velum paper is not acceptable (too thin). Fig(s) _____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
21.0 cm by 29.7 cm (DIN size A4)
21.6 cm by 27.9 cm (8 1/2 x 11 inches)
All drawing sheets not the same size. Fig(s) _____
Sheet(s) _____
Drawings sheets not an acceptable size. Fig(s) _____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
SIZE: A4 Size
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: 8 1/2 x 11
Margins not acceptable. Fig(s) _____
Top (T) _____ Left (L) _____
Right (R) _____ Bottom (B) _____
6. VIEWS. 37 CFR 1.84(h)
REMINDER: Specification may require revision to correspond to drawing changes.
Partial views. 37 CFR 1.84(h)(2)
Brackets needed to show figure as one entity. Fig(s) _____
Views not labeled separately or properly. Fig(s) _____
Enlarged view not labeled separately or properly. Fig(s) _____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
Hatching not indicated for sectional portions of an object. Fig(s) _____
Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____
9. SCALE. 37 CFR 1.84(k)
Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) _____
11. SHADING. 37 CFR 1.84(m)
Solid black areas pale. Fig(s) _____
Solid black shading not permitted. Fig(s) _____
Shade lines, pale, rough and blurred. Fig(s) _____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
Numbers and reference characters not plain and legible. Fig(s) _____
Figure legends are poor. Fig(s) _____
Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____
English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____
Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____
13. LEAD LINES. 37 CFR 1.84(q)
Lead lines cross each other. Fig(s) _____
Lead lines missing. Fig(s) _____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
16. CORRECTIONS. 37 CFR 1.84(w)
Corrections not made from prior PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
Surface shading shown not appropriate. Fig(s) _____
Solid black shading not used for color contrast. Fig(s) _____

COMMENTS

REVIEWER _____

DATE

8/10/00

TELEPHONE NO.

308-0011

ATTACHMENT TO PAPER NO. _____

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

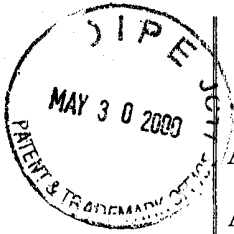
2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have **acceptable** corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Calendar, Helena; Sredanovic, Nikolas
Assignee: Mosel Vitelic, Inc.
Title: Programmable Latches That Include Non-Volatile Programmable Elements
Serial No.: 09/178,445 Filing Date: 10/23/98
Examiner: V. Nguyen Group Art Unit: 2818
Docket No.: M-5598 US Batch No. I86
Date Allowed: February 29, 2000

San Jose, California
May 25, 2000

BOX Issue Fee
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

AMENDMENT UNDER 37 CFR 1.312

Sir:

Please amend the above patent application as follows:

IN THE SPECIFICATION

Page 17, line 9: After "et al." delete "and" and insert --, now U.S. Patent No. 5,889,414 issued on March 30, 1999,--

REMARKS

The specification is amended to update the status of a patent application referenced in the specification.

Please telephone Applicants' attorney at 408-453-9200, ext. 1234, if there are any questions.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on May 25, 2000.

Michael Shenker 5-25-00
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicant(s)
Reg. No. 34,250

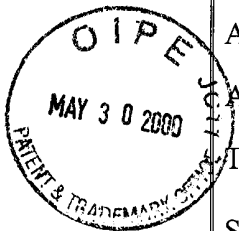
LAW OFFICES OF
SKJERVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

635233 vl

-1-

Serial No. 09/178,445



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Calendar, Helena; Sredanovic, Nikolas
Assignee: Mosel Vitelic, Inc.
Title: Programmable Latches That Include Non-Volatile Programmable Elements
Serial No.: 09/178,445 Filing Date: 10/23/98
Examiner: V. Nguyen Group Art Unit: 2818
Docket No.: M-5598 US Batch No. I86
Date Allowed: February 29, 2000

San Jose, California
May 25, 2000

BOX Issue Fee
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

REQUEST TO RETURN AN INITIALIZED FORM PTO-1449

Sir:

On February 3, 2000, Applicants mailed to the U.S. Patent and Trademark Office an Information Disclosure Statement including Form PTO-1449. A copy of the Form PTO-1449 is enclosed. Also enclosed is a copy of the Return Receipt Postcard showing that the Form PTO-1449 was received by the U.S. Patent and Trademark Office on February 8, 2000.

Applicants have not received a copy of the Form PTO-1449 initialed by the Examiner. Please return the initialized Form PTO-1449 to Applicants' attorney. Please telephone the undersigned at 408-453-9200, ext. 1234, if any problems arise.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on May 25, 2000.

Michael Shenker 5-25-00
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicants
Reg. No. 34,250

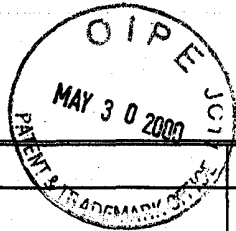
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MACPHERSON, FRANKLIN
& FRIEL LLP

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(408) 453-9200
FAX (408) 453-7979

635341 v1

-1-

Serial No. 09/178,445



Sheet 1 of 1

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-5598 US		09/178,445	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Sredanovic, Nikolas; Calendar, Helena			
					Filing Date		Group	
					October 23, 1998		2818	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,497,355	3/1996	Mills et al.	365	230.08		
	AB	5,526,320	6/1996	Zager et al.	365	233.5		
	AC	5,544,124	8/1996	Zager et al.	365	230.08		
	AD	5,640,364	6/1997	Merritt et al.	365	233.5		
	AE	5,710,741	6/1995	McLaury	365	226		
	AF	5,793,688	8/1998	McLaury	365	203		
	AG	5,812,489	9/1998	Matsui	365	233		
	AH	5,870,342	2/1999	Fukuda	365	201		
	AI	5,898,621	4/1999	Takahashi et al.	365	185.33		
	AJ							
	AK							
	AL							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AR							
	AS							
	AT							
Examiner			Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								



10

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Applicants: Sredanovic, Nikolas; Calendar, Helena
Assignee: Mosel Vitelic, Inc.
Title: Programmable Latches That Include Non-Volatile Programmable Elements
Serial No.: 09/178,445
Filed: October 23, 1998
Atty Docket No.: M-5598 US

ENCLOSED:

1. This Return Receipt Postcard
2. Information Disclosure Statement (1 p.)
3. Form PTO-1449 citing nine references (hp)
4. Copies of nine cited references

MS/van
February 3, 2000

SKIPPEN, M. J. & T. J. PHILSON
FRANKLIN & HILL

FEB 15 2000

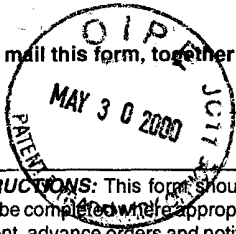
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BY DOCKET DEPT



PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fee, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231



KS

B \$ BO
AD

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

MM42/0229

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

MICHAEL SHENKER

(Depositor's name)

Michael Shenker

(Signature)

May 25, 2000

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/178,445	10/23/98	021	NGUYEN, V 2818	02/29/00
First Named Applicant	SREDANOVIC, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE PROGRAMMABLE ELEMENTS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 M-5598-US	365-225.700	I86	UTILITY	NO	\$1210.00	05/30/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Skjerven, Morrill, MacPherson, Franklin & Friel LLP

2 Michael Shenker

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type). PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE MOSEL VITELIC, INC.

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Hsin Chu, Taiwan

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

- ☐ Issue Fee
- ☐ Advance Order - # of Copies

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER 19-2386
(ENCLOSE AN EXTRA COPY OF THIS FORM)

- ☒ Issue Fee 11
- ☒ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Michael Shenker

(Date)

5-25-00

Michael Shenker, Reg. No. 34,250

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

05/31/2000 CV0222 00000059 192386 09178445
1210.00 CH
33.00 CH
01 FD:142
02 FD:561



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

09/178,445 APPLICATION NUMBER	10/23/98 FILING DATE	SREDANOVIC FIRST NAMED APPLICANT	N ATTORNEY DOCKET NO. 10098-118
----------------------------------	-------------------------	-------------------------------------	---------------------------------

7542/0915
MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

NGUYEN, NHA

ART UNIT 3 PAPER NUMBER

09/05/00

DATE MAILED:

Response to Rule 312
Communication

- ☐ The petition filed on _____ under 37 CFR 1.312(b) is granted. The paper has been forwarded to the examiner for consideration on the merits.

Director,
Patent Examining Group _____

- ☒ The amendment filed on 05/30/00 under 37 CFR 1.312 has been considered, and has been:
☒ entered.

- ☐ entered as directed to matters of form not affecting the scope of the invention (Order 3311).
☐ disapproved. See explanation below.
☐ entered in part. See explanation below.

Publishing Division

GP 2818

9/IDS

9-29-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sredanovic, Nikolas; Calendar, Helena

Assignee: Mosel Vitelic, Inc.

Title: PROGRAMMABLE LATCHES THAT INCLUDE NON-VOLATILE
PROGRAMMABLE ELEMENTS

Serial No.: 09/178,445 Filed: October 23, 1998

Examiner: V. Nguyen Group Art Unit: 2818

Docket No.: M-5598 US

San Jose, California
February 3, 2000

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RECEIVED
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TECHNOLOGY CENTER 2800

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on Feb. 3, 2000.

Michael Shenker 2-3-00
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicants
Reg. No. 34,250

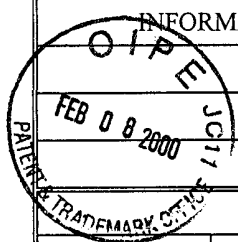
LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

- 1 -

SER. NO. 09/178,445

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-5598 US	09/178,445
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)
(Use several sheets if necessary)		Sredanovic, Nikolas; Calendar, Helena
Filing Date		Group
October 23, 1998		2818



U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
VN	AA	5,497,355	3/1996	Mills et al.	365	230.08	
VN	AB	5,526,320	6/1996	Zager et al.	365	233.5	
VN	AC	5,544,124	8/1996	Zager et al.	365	230.08	
VN	AD	5,640,364	6/1997	Merritt et al.	365	233.5	
VN	AE	5,710,741	6/1995	McLaury	365	226	
VN	AF	5,793,688	8/1998	McLaury	365	203	
VN	AG	5,812,489	9/1998	Matsui	365	233	
VN	AH	5,870,342	2/1999	Fukuda	365	201	
VN	AI	5,898,621	4/1999	Takahashi et al.	365	185.33	
	AJ	Viet Q. Nguyen Primary Examiner					
	AK						
	AL						

Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AM						
	AN						
	AO						
	AP						
	AQ						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
Viet Q. Nguyen Primary Examiner	
AS	
AT	Viet Q. Nguyen Primary Examiner

Examiner	V. NGUYEN	Date Considered	10/2/00
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.			



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
--------------------	-------------	-----------------------	---------------------

09/178,445 10/23/98 SREDANOVIC

N M-5598-US

MM41/1011

MICHAEL SHENKER
SKJERVEN MORRILL MACPHERSON
FRANKLIN & FRIEL
25 METRO DRIVE SUITE 700
SAN JOSE CA 95110-1349

EXAMINER

ART UNIT PAPER NUMBER

2818
DATE MAILED:

10/11/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

Supplemental
NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to IDS filed on 2/8/00

☒ The allowed claim(s) is/are 1-13, 16-23

☒ The drawings filed on 3/28/00 are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 9

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

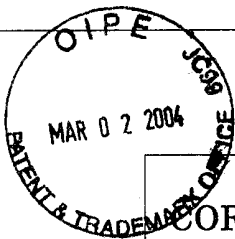
☐ Examiner's Statement of Reasons for Allowance

Viet Nguyen

Viet Q. Nguyen
Primary Examiner

This file wrapper was thoroughly reviewed by Our technical staff. Correspondence Address Change & Change in Power of Attorney dated 04/03/2003 is missing from the original USPTO file history.

This has been brought to your attention so that you will know it has not been overlooked.



DSD

CHANGE OF CORRESPONDENCE ADDRESS PATENT		
Address to: Commissioner for Patents P.O. Box 1450 Alexandra, VA 22313-1450	Patent Number	6,163,492
	Issue Date	19-Dec-00
	Application Number	09/178,445
	Filing Date	23-Oct-98
	First Named Inventor	Nikolas Sredanovic
	Attorney Docket Number	M-5598 US

Please change the Correspondence Address for the above-identified patent application to:

☐ Customer Number:
OR

☒ Firm or Individual Name **MacPherson Kwok Chen & Heid LLP**
Address **1762 Technology Drive**
Address **Suite 226** State **CA** Zip **95110**
City **San Jose**
Country **U.S.A.**
Telephone **(408) 392-9250** Fax **(408) 392-9262**

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This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTOSB/47).

I am the:

- ☐ Patentee.
☐ Assignee of record of the entire interest. See 37 CFR 3.71
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).
☒ Attorney or Agent of record. Registration Number 25,875

Typed or Printed	
Name	David W. Heid
Signature	<i>David W. Heid</i>
Date	2/25/04
Telephone	(408) 392-9250
NOTE: Signature of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*	

☒ *Total of <u>(1)</u> forms are submitted.

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	31 minus 20 = *	11
INDEPENDENT CLAIMS	5 minus 3 = *	2
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐

OR

OTHER THAN
SMALL ENTITY

RATE	FEE		RATE	FEE
	395.00	OR		790.00
x\$11=		OR	x\$22=	242.00
x41=		OR	x82=	164.00
+135=		OR	+270=	
TOTAL		OR	TOTAL	1,196.00

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
x\$11=		OR	x\$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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Terms	Documents
13 and (fuse\$ or antifuse\$ or anti-fuse\$)	14

Database: US Patents Full-Text Database ▼

Refine Search: 13 and (fuse\$ or antifuse\$ or anti-fuse\$) ▲ ▼

Search History

DB Name	Query	Hit Count	Set Name
USPT	13 and (fuse\$ or antifuse\$ or anti-fuse\$)	14	<u>L4</u>
USPT	12 and voltage and diode\$	54	<u>L3</u>
USPT	11 and power	203	<u>L2</u>
USPT	program\$ adj1 latch\$	264	<u>L1</u>

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Edit S Numbers

1. Document ID: US 6009284 A
Entry 1 of 14
US-PAT-NO: 6009284
DOCUMENT-IDENTIFIER: US 6009284 A

Dec 28, 1999

TITLE: System and method for controlling image processing devices from a remote location
DATE-ISSUED: December 28, 1999

NAME	CITY	STATE	ZIP CODE	COUNTRY
Weinberger, Joseph	East Brunswick	NJ	N/A	N/A
Bricault, Gary	Rochester	NY	N/A	N/A
Laird, James	Rochester	NY	N/A	N/A

US-CL-CURRENT: 399/8; 345/354, 399/77, 710/67

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	FOI/C	Image
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2. Document ID: US 5892712 A
Entry 2 of 14
US-PAT-NO: 5892712
DOCUMENT-IDENTIFIER: US 5892712 A

Apr 6, 1999

TITLE: Semiconductor non-volatile latch device including embedded non-volatile elements
DATE-ISSUED: April 6, 1999

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hirose; Ryan T.	Colorado Springs	CO	N/A	N/A
Lancaster; Loren T.	Colorado Springs	CO	N/A	N/A

US-CL-CURRENT: 365/185.07; 365/154, 365/189.05

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	WORD	Image
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☐ 3. Document ID: US 5752047 A
Entry 3 of 14

May 12, 1998

US-PAT-NO: 5752047
DOCUMENT-IDENTIFIER: US 5752047 A

TITLE: Modular solid state power controller with microcontroller
DATE-ISSUED: May 12, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Darty; Mark Anthony	Madison	AL	N/A	N/A
Prickett; Guy Brent	Grant	AL	N/A	N/A
Schwarz; Charles Raymond	Huntsville	AL	N/A	N/A

US-CL-CURRENT: 713/300; 361/2, 713/310

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMNC	Image
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☐ 4. Document ID: US 5696455 A

Entry 4 of 14

File: USPT

Dec 9, 1997

US-PAT-NO: 5696455

DOCUMENT-IDENTIFIER: US 5696455 A

TITLE: Reconfigurable programmable logic device
DATE-ISSUED: December 9, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 326/41; 326/44, 365/189.08

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMNC	Image
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☐ 5. Document ID: US 5603060 A

Entry 5 of 14

File: USPT

Feb 11, 1997

US-PAT-NO: 5603060

DOCUMENT-IDENTIFIER: US 5603060 A

TITLE: Method of controlling copy machines from a remote location
DATE-ISSUED: February 11, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Weinberger; Joseph	East Brunswick	NJ	N/A	N/A
Bricault; Gary	Rochester	NY	N/A	N/A
Laird; James	Rochester	NY	N/A	N/A

US-CL-CURRENT: 399/8; 345/354, 399/77, 399/81, 709/223, 710/67

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMNC	Image
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☐ 6. Document ID: US 5548552 A

Entry 6 of 14

File: USPT

Aug 20, 1996

US-PAT-NO: 5548552
DOCUMENT-IDENTIFIER: US 5548552 A
TITLE: Reconfigurable programmable logic device
DATE-ISSUED: August 20, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.33; 326/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Image
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☐ 7. Document ID: US 5548228 A

Entry 7 of 14

File: USPT

Aug 20, 1996

US-PAT-NO: 5548228
DOCUMENT-IDENTIFIER: US 5548228 A

TITLE: Reconfigurable programmable logic device having static and non-volatile memory
DATE-ISSUED: August 20, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 326/41; 326/39, 365/189.08

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Image
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☐ 8. Document ID: US 5455937 A

Entry 8 of 14

File: USPT

Oct 3, 1995

US-PAT-NO: 5455937
DOCUMENT-IDENTIFIER: US 5455937 A

TITLE: Microcontroller with fuse-emulating latches
DATE-ISSUED: October 3, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Berman; Eric	Hicksville	NY	N/A	N/A
Italiano; Greg	Hicksville	NY	N/A	N/A
Padgaonkar; Ajay	Sugarland	TX	N/A	N/A
Allen; Ray	Mesa	AZ	N/A	N/A

US-CL-CURRENT: 395/500.44; 714/1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Image
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☐ 9. Document ID: US 5398206 A

Entry 9 of 14

File: USPT

Mar 14, 1995

DOCUMENT-IDENTIFIER: US 5398206 A

INVENTOR- INFORMATION:

US-CL-CURRENT: 365/200; 365/230.01, 365/230.03, 365/230.06, 365/230.08

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	ROUND	Image
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Jul 26, 1994

DOCUMENT-IDENTIFIER: US 5333286 A

INVENTOR- INFORMATION:

US-CL-CURRENT: $\frac{714}{47}$; $\frac{364}{921.8}$, $\frac{364}{927.92}$, $\frac{364}{927.95}$, $\frac{364}{927.99}$, $\frac{364}{928}$,
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 $\frac{364}{940.1}$, $\frac{364}{943.9}$, $\frac{364}{944.7}$, $\frac{364}{\text{DIG2}}$, $\frac{395}{500.45}$, $\frac{395}{500.46}$, $\frac{399}{8}$

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Image
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Terms	Documents
13 and (fuse\$ or antifuse\$ or anti-fuse\$)	14

11

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Search Results - Record(s) 11 through 14 of 14 returned.

☐ 11. Document ID: US 5214772 A

Entry 11 of 14File: USPTMay 25, 1993

US-PAT-NO: 5214772

DOCUMENT-IDENTIFIER: US 5214772 A

TITLE: System for automatically monitoring copiers from a remote location

DATE-ISSUED: May 25, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Weinberger; Joseph	East Brunswick	NJ	N/A	N/A
Bricault; Gary	Rochester	NY	N/A	N/A
Laird; James	Rochester	NY	N/A	N/A

US-CL-CURRENT: 714/47; 364/921.8, 364/927.2, 364/927.5, 364/927.92, 364/927.95, 364/927.99, 364/928, 364/928.2, 364/928.6, 364/932.8, 364/933.62, 364/933.8, 364/939, 364/939.3, 364/939.5, 364/940, 364/940.1, 364/940.61, 364/940.62, 364/941, 364/942, 364/943.9, 364/944.7, 364/948.4, 364/959.1, 364/965, 364/965.76, 364/DIG2, 395/500.44, 399/8

Full Title Citation Front Review Classification Date Reference Claims KWD Image

☐ 12. Document ID: US 4571704 A

Entry 12 of 14File: USPTFeb 18, 1986

US-PAT-NO: 4571704

DOCUMENT-IDENTIFIER: US 4571704 A

TITLE: Nonvolatile latch

DATE-ISSUED: February 18, 1986

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bohac, Jr.; Frank J.	Laguna Hills	CA	N/A	N/A

US-CL-CURRENT: 365/185.07; 257/316, 257/904

Full Title Citation Front Review Classification Date Reference Claims KWD Image

☐ 13. Document ID: US 4459582 A

Entry 13 of 14File: USPTJul 10, 1984

US-PAT-NO: 4459582
DOCUMENT-IDENTIFIER: US 4459582 A

TITLE: Local control apparatus for central station alarm system
DATE-ISSUED: July 10, 1984

INVENTOR-INFORMATION:
NAME CITY STATE ZIP CODE COUNTRY
Sheahan; Robert F. Staten Island NY N/A N/A
Terrett; David S. Lincroft NJ N/A N/A

US-CL-CURRENT: 340/539, 340/333, 340/506, 340/508, 340/510, 340/517, 340/518, 340/527, 340/528, 340/825.06, 340/825.1, 340/825.31, 379/43

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	EMC	Image
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☐ 14. Document ID: US 4427974 A
Entry 14 of 14 File: USPT Jan 24, 1984
US-PAT-NO: 4427974
DOCUMENT-IDENTIFIER: US 4427974 A
TITLE: Local control apparatus for central station alarm system
DATE-ISSUED: January 24, 1984

INVENTOR-INFORMATION:
NAME CITY STATE ZIP CODE COUNTRY
Sheahan; Robert F. Staten Island NY N/A N/A

US-CL-CURRENT: 340/539, 340/333, 340/506, 340/508, 340/510, 340/517, 340/518, 340/527, 340/528, 340/825.06, 340/825.1, 340/825.31, 379/43, 379/49

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	EMC	Image
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Display 10 Documents including document number 14

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