

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS, CO. LTD.,)
)
Plaintiff,)
)
vs.) No. IPR2019-00779
) IPR2019-00780
PROMOS TECHNOLOGIES, INC.,) IPR2019-00781
)
Patent Owner.)
_____)

** REVISED **

DEPOSITION OF ERIK DE LA IGLESIA
Redwood City, CA
Wednesday, January 29, 2020

STENOGRAPHICALLY REPORTED BY:
SUSAN F. MAGEE, RPR, CCRR, CLR, CSR No. 11661
Job No. 174893

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January 29, 2020
9:18 a.m.

Deposition of ERIK DE LA IGLESIA, held at the
offices of TechKnowledge Law Group LLP, 100 Marine
Parkway, Suite 200, Redwood City, CA 94065, pursuant to
Notice before SUSAN F. MAGEE, RPR, CCRR, CLR, CSR
No. 11661.

1 APPEARANCES:

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17 BY: KEVIN JONES, ESQ.

21 -- 000 --

----- I N D E X -----

WITNESS: ERIK DE LA IGLESIA

EXAMINATION BY

PAGE

BY MR. ANDERSON

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----- E X H I B I T S -----

NO.	DESCRIPTION	PAGE
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(No exhibits marked.)

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1 PREVIOUSLY MARKED EXHIBITS REFERENCED

2 EXHIBIT PAGE

3 Exhibit 1006 134

4 Exhibit 1010 174

5 Exhibit 1005 187

6 --000--

1 REDWOOD CITY, CA

2 Wednesday, January 29, 2020, 9:18 a.m.

3
4 ERIK DE LA IGLESIA,

5 called as a witness, having been duly sworn by a
6 Certified Shorthand Reporter, was examined and testified
7 as follows:

8
9 EXAMINATION BY MR. ANDERSON

10
11 Q. Good morning.

12 A. Good morning.

13 Q. Can you please state and spell your full name
14 for the record.

15 A. It's Erik de la Iglesia. That's E-r-i-k, last
16 name is d-e l-a I-g-l-e-s-i-a.

17 Q. Is it your understanding that this deposition
18 concerns three IPR proceedings corresponding to U.S.
19 Patent 6,163,492?

20 A. I don't have the first -- the prefix numbers,
21 but it is -- I understand it to be the '492 patent, and
22 there are three IPRs concerned, yes.

23 Q. And I see you have some documents in front of
24 you.

25 What are those documents?

1 A. These are the declarations that I submitted as
2 part of this case.

3 Q. Okay. So those are the declarations you
4 submitted in each of the three IPR proceedings?

5 A. That would be correct. Two preliminary
6 responses and three supplemental.

7 Q. Okay. And looking at those declarations, can
8 you confirm that the full patent number is 6,163,492? I
9 think it's right on the cover.

10 A. Yes. 6,163,492.

11 Q. And the three IPR proceedings are numbered IPR
12 2019-00779, -00780 and -00781; correct?

13 A. That's correct.

14 Q. And during this deposition, if it's okay with
15 you I'd like to refer to the -- the patent as the '492
16 patent.

17 A. That's how I refer to it.

18 Q. Perfect. And with respect to the different
19 declarations that you have, if I'm asking a question
20 specific to one of those declarations, I'll refer to,
21 for example, the -779 declaration or the -779
22 declaration in support of the preliminary response if I
23 talk about that one.

24 Is that understandable to you?

25 A. I understand that all questions stand on their

1 own. To the extent that I believe it applies to
2 multiple, I may ask you to clarify.

3 Q. Sure. I guess what I'm saying is, if I ask you
4 to look at paragraph 33 of the -779 declaration, what
5 I'm intending to say is look at that paragraph and the
6 declaration that you submitted with respect to the
7 Promos' response in the -779 proceeding. And if I'm
8 referring to something -- it's just a shorthand way.
9 But if you don't understand it, please ask.

10 A. I think that's a fair assumption.

11 Q. Okay. So before we begin, I just want to go
12 over some basic ground rules. So I'm going to ask
13 questions during this deposition, and your counsel may
14 object, but you need to answer the question unless he
15 instructs you not to answer.

16 Do you understand that?

17 A. I understand.

18 Q. And if a question that I ask is unclear, please
19 let me know so that I can rephrase it. Otherwise I'll
20 assume that you understood my question, okay?

21 A. Understood.

22 Q. And obviously our discussion will be
23 transcribed so gestures don't transcribe well. So
24 please maintain your answers in the verbal context and
25 not in a nod or a shake of the head, please.

1 Do you have any questions before we begin?

2 A. No.

3 Q. Okay. Is there any reason that would prevent
4 you from testifying truthfully and accurately today?

5 A. No.

6 Q. How did you prepare for this deposition?

7 A. Met with counsel.

8 Q. And when you say "counsel," are you referring
9 to Mr. Jones?

10 A. Yes.

11 Q. Anyone else?

12 A. No.

13 Q. How long did you spend with Mr. Jones?

14 A. About four hours.

15 Q. And when did you begin preparing?

16 MR. JONES: Objection. Vague.

17 THE WITNESS: So maybe you can clarify as to
18 whether we're talking about preparing for the deposition
19 in general or preparing with Mr. Jones.

20 BY MR. ANDERSON:

21 Q. Sure. When did you begin preparing for the
22 deposition in general?

23 A. Maybe two or three days ago.

24 Q. Okay. And did you meet with Mr. Jones
25 recently?

1 A. Yes.

2 Q. Yesterday?

3 A. Yesterday; that's correct.

4 Q. And will you represent to me that those are
5 clean copies of the declarations without any markings on
6 them?

7 MR. JONES: I'll handle that because I printed
8 them.

9 MR. ANDERSON: Okay.

10 MR. JONES: So I'll represent that they're
11 clean copies of the complete five declarations --

12 MR. ANDERSON: Okay.

13 MR. JONES: -- with no markings.

14 MR. ANDERSON: Okay. Thank you.

15 BY MR. ANDERSON:

16 Q. When were you first retained by Promos to
17 assist with the '492 patent?

18 A. I don't have the exact date, but I believe it
19 was in May of 2019.

20 Q. Okay. And was it Mr. Jones that retained you?

21 A. Yes.

22 Q. Okay. Have you been exposed to any
23 confidential Samsung information as a result of your
24 involvement with the '492 patent?

25 A. No.

1 Q. Okay. So looking at your CV, you have a
2 bachelor's degree from the University of Florida in
3 electrical engineering; is that correct?

4 A. That's correct.

5 Q. And what year did you graduate?

6 A. 1996.

7 Q. Okay. And from there you went to Stanford; is
8 that correct?

9 A. Yes. I have a master's at Stanford.

10 Q. And what year did you finish at Stanford?

11 A. 1997.

12 Q. And your degree from Stanford is electrical
13 engineering as well?

14 A. Yes. It's a master's of science in electrical
15 engineering.

16 Q. Did you have a particular area of
17 specialization when you did your work for your master's?

18 A. I did in terms of the electives that I took and
19 sort of the core specialization. I would say VLSI
20 design, semiconductor design, leaning more towards
21 custom and semicustom design.

22 Q. Digital, analog, both?

23 A. Absolutely both.

24 Q. Who was your graduate advisor at Stanford?

25 A. Mark Horowitz.

1 Q. I was going to ask if you knew Mark Horowitz.
2 I'm very familiar with Mike Horowitz.

3 So I understand you worked for Intel from
4 December '97 through at least November of '99, I guess
5 end of March of 2000.

6 Does that sound correct?

7 A. It was through March of 2000, yes.

8 Q. And did you go to work for Intel straight out
9 of school then or --

10 A. Yes. Straight out of school.

11 Q. All right. And I guess what did you do at
12 Intel during that time?

13 A. So I worked on a number of different aspects,
14 but the job that I held was as a design engineer in
15 mobile and handheld products. So my focus for the first
16 two years was working on specific power features and
17 regulations within the mobile P2 and mobile P3. These
18 dealt with the technology that allow laptops to assume
19 different operating frequencies when they are plugged
20 versus unplugged. That technology was basically
21 invented at Intel.

22 I also worked on power and performance modeling
23 of the various mobile Pentium products as well as some
24 of the server lines, the Itanium products later. But a
25 majority of my work was focused in the mobile and

1 handheld group dealing with the configuration, operation
2 and validation and design of these -- these power and
3 clocking features and all of the ancillary circuits that
4 involve them.

5 Q. So I'm curious. So Intel was manufacturing the
6 processors and the chipsets; right? They weren't
7 actually doing the end products; is that correct? So
8 end products being the mobile device itself.

9 Did Intel actually make the mobile device, or
10 did they make chips that went into the mobile device?
11 That would be my question, I guess.

12 A. So that depends on the business unit and the
13 product. Intel will generally make proof of concept
14 development vehicles and full products without the
15 intention to bring them to market. Sometimes those
16 products are taken as a whole and product ties by
17 external vendors, essentially using Intel as an OEM.

18 Other times those are used as references by
19 vendors to create their own products, and yet other
20 times vendors create their own chipsets and their own
21 features and simply use the Intel processor.

22 Q. When you say "chipsets," what do you mean by
23 chipsets?

24 A. So in the processor world, a processor is --
25 includes the operative cores, so the operating cores

1 that actually execute the instruction set, usually
2 memory controllers as well and several layers of cache.
3 A chipset is the supporting chips that allow that
4 processor to operate within a -- within a certain
5 product. So for instance, the chipset that allows your
6 Intel processor to work in your ThinkPad is different
7 than the chipset that allows an Intel processor to work
8 within a server, and it was the mobile and handheld
9 products group role to develop the features for those
10 chipsets, including all of the enabled features that
11 would be used in the processors. Processors in general
12 will share the same core design. In that time, the
13 mobile processor was just a lower-voltage,
14 lower-frequency version of the desktop processor. But
15 even at that time we were evolving to create special
16 variance of processors with additional features, so
17 different mask sets for the mobile product line.

18 Q. Did any of those processors include fuses?

19 A. All of those processors and the chipsets
20 included fuses.

21 Q. And what were the fuses used for in those
22 processors and chipsets at Intel?

23 A. Well, they were used to enable many features
24 and also to map around defective units of the cache. In
25 large processors we -- at that time frame we had just

1 started putting large amounts of L2 on die. Previous to
2 about '96, '95 or '96, most of the L2 cache was
3 external. You may remember buying Pentiums in a
4 cartridge format that had a processor with additional
5 cache dies external to them.

6 The first product that I worked on was the
7 integrated cache, which meant that the actual L2 cache
8 was on die, so a single die held a processor in the
9 cache. And so we had to, of course, remap all of the
10 bad areas of the cache.

11 Fuses were also used for all of the features.
12 They were not just for what features enable a mobile
13 processor versus a desktop processor but also things
14 that would be considered highly proprietary to Intel.
15 Among them would be, say, locking a bus fraction. You
16 may recall that during the time there was a lot of
17 scandals involving people buying processors that worked
18 at a certain frequency and trying to upsell them at a
19 higher frequency. Those frequencies were locked by fuse
20 settings that were programmed at manufacturing time, and
21 so designing and testing the fuses in such a way that
22 their values could not be detected or altered after
23 shipping was a high security concern. In my specific
24 unit because of our -- our need to change the clock
25 frequency, we also had to fuse that particular

1 capability at multiple levels. First as a feature
2 because we were going to charge more for processors that
3 had this docking feature set, so we had to provide --
4 the whole feature set had to be fuse enabled; and
5 second, what bus -- what frequencies you were allowed to
6 change to had to be locked in. So for instance, if I'm
7 selling a certain power envelope, then I can only allow
8 transitions to certain frequencies. Those would all be
9 fused set as well, burnt in.

10 It was -- those are, of course, not the only
11 reason that fuses --

12 Q. Sure.

13 A. Fuse blocks were enormous and controlled all
14 sorts of different features, including sometimes we used
15 fuses to correct clock skew on certain bins of products.
16 If we had a particular bad run and we could essentially
17 use fuses to correct some of the clock alignment on the
18 serpentines in the processor, we could do that even
19 though it wasn't, say, within the normal manufacturing
20 tolerance.

21 Q. Sure. So I guess my takeaway from that is some
22 of these fuses were used to configure certain features.
23 Some of them were used to enable redundant systems to
24 come into play if something tested badly.

25 Is that correct?

1 A. Right. And those fuses would also be used in
2 the case of when the laptop is switching from one
3 frequency to another. We actually put the processor
4 into deep sleep and come back out, in which case we have
5 to essentially reread portions of the fuse setting.
6 It's essentially as if we're resetting the processor but
7 doing it in a very fast way.

8 And so the fuse blocks had to be adjusted from
9 a design standpoint because when you go into deep sleep,
10 many sections of the chip are unpowered. Many further
11 sections are unclocked, and so there can be all sorts of
12 issues that arise from bringing a processor back up but
13 without actually resetting everything from a power
14 perspective.

15 Q. Okay. Okay. I'm going to hand you a copy of
16 the '492 patent.

17 And do you recognize U.S. Patent 6,163,492?

18 A. I do.

19 Q. Have you read it thoroughly?

20 A. I read it as thoroughly as I can.

21 Q. Understood. Is there any aspect of the '492
22 patent that is unclear to you or doesn't make sense from
23 a technical perspective?

24 MR. JONES: Objection. Vague.

25 THE WITNESS: No. If there are specific

1 portions of this that you believe are vague, I'd be
2 happy to address them. I don't know of any that are
3 vague.

4 BY MR. ANDERSON:

5 Q. Okay. And the title of the '492 patent is
6 "Programmable Latches That Include Nonvolatile
7 Programmable Elements"; correct?

8 A. That is the title.

9 Q. What are nonvolatile programmable elements in
10 the context of the '492 patent?

11 A. So a nonvolatile programming element is an
12 element that can be programmed or have its state set in
13 such a way that that state is not lost when power is
14 removed.

15 Q. And are there examples provided in the '492
16 patent?

17 A. Yes, there are examples discussed.

18 Q. And which specific examples does the '492
19 patent talk about?

20 A. Well, the -- if we start with Figure 2, so
21 Figure 2A, we see an example there of a fuse. This is,
22 of course, just a figure. I understand that the patent
23 discusses both fuses and antifuses.

24 Q. What's the difference between a fuse and an
25 antifuse?

1 A. If you have a fuse, you program it. It's
2 basically a conductor until you program it to be open
3 and an antifuse is the reverse.

4 Q. So when the '492 patent talks about programming
5 a fuse, it means blowing the fuse to create an open
6 circuit?

7 A. I would say more generally it involves changing
8 the state from the default state. If -- in the case of
9 an antifuse you wouldn't necessarily use the term "blow"
10 in antifuse.

11 Q. Sure. So in the case of a fuse being a
12 conductor that when blown becomes nonconductive, in that
13 sense if the fuse is programmed, that means you're
14 blowing the fuse to create an open circuit; correct?

15 A. I would be a little more specific that if I
16 have a block of fuses and I program the block of fuses,
17 that would entail that some of them could be blown. If,
18 let's say, for instance, that the programming was such
19 that none of the fuses would actually be blown, there
20 would be no need. The 1s and 0s of whatever was being
21 programmed were such that no fuses would actually be
22 blown. That would be a conceivable scenario.

23 Q. So are you saying that when the '492 patent
24 talks about programming the fuse F1 in Figure 2A, it
25 simply means it's determining whether or not the fuse is

1 blown?

2 A. No. I'm saying that in the '492 patent when
3 they discuss programming the fuse, they are -- they are
4 generally talking about it in terms of blowing the fuse.
5 But your question related to programming in general. I
6 just wanted to be clear that fuse blocks when programmed
7 will be blown or not blown, depending on the programming
8 content.

9 Q. Okay. Let me try to ask the question a little
10 bit more specifically then.

11 So in the context of Figure 2A, if the '492
12 patent is talking about programming the fuse F1, it's
13 talking about blowing the fuse F1; correct?

14 A. I think that's a fair statement. It's making
15 fuse F1 nonconductive.

16 Q. Thank you. And if you go to column 7 of the
17 '492 patent around line 30 -- and the line numbers are
18 always a little off in these patents, so bear with me.
19 I'm giving you approximate locations, but around line 30
20 it describes some other programmable elements; correct?

21 A. Yes.

22 Q. And the list there includes EPROMs, EEPROMs and
23 UPROMs.

24 What is a UPROM?

25 A. I don't recall right now the distinction on the

1 UPR0M.

2 Q. Okay.

3 A. The EPROMs and the EEPROMs, though, I'm
4 familiar with.

5 Q. Okay. So how does an EEPROM work?

6 A. Well, perhaps maybe we start with an EPROM and
7 then deal with an EEPROM just so that the distinction
8 makes sense. And I'll also distinguish these from sort
9 of the current version of this technology which would be
10 Flash. So an EPROM generally has -- you can think of it
11 as a transistor that has an extra oxide layer within the
12 gate, so there is a control gate, but there's also a
13 buried gate. In order to program the cell, you would
14 apply a higher than normal voltage to the gate and
15 essentially tunnel charge carriers into the intermediate
16 gate. The timing of those pulses and the voltage that's
17 applied needs to be set very carefully. In general
18 we're trying to effect something called Fowler-Nordheim
19 tunneling so that the charges will basically enter that
20 intermediate layer and stay there.

21 If sufficient charge is built up on the
22 intermediate gate, then applying a charge to the control
23 gate functions just like an NMOS transistor so the gate
24 is -- if the gate is high, the device is conductive. If
25 there is insufficient or no charge on the intermediate

1 gate, then no amount of the actual control gate at the
2 top is too far from the channel in order to invert it
3 and thereby make it conductive.

4 There are some nuances in terms of what kind of
5 charge, how they're trapped and how they are -- how
6 they're controlled. What also distinguishes EPROMs and
7 EEPROMs is that generally in the way that they're
8 constructed in arrays. It's a two-cell combination, so
9 it's an EEPROM and it's a bit select whereas, say, in --
10 a Flash cell also uses an intermediate gate, but they
11 are conducted in strings, and so there's only one cell
12 per bit.

13 Q. So --

14 A. I hope that explains the EPROM nature.

15 Q. Actually, and that might be enough for my
16 follow-on question which is, so if an integrated circuit
17 includes an EPROM, do you need power to be applied to
18 the integrated circuit for the EPROM to be conductive
19 between its drain and its source?

20 A. Taking the EPROM in isolation, the value of an
21 EPROM cell requires power to be read. You -- in the
22 event that the EPROM is used as a programmable control,
23 it would be considered programmed regardless of whether
24 power is applied or not.

25 Q. But you wouldn't know if it was programmed

1 without applying power to the EPROM; is that correct?

2 A. No. You would know that it is programmed based
3 on whether or not you programmed it.

4 Q. Sure. I guess if you -- if you weren't the
5 person that programmed it, say you're the end user and
6 the EPROM was programmed during manufacturing, is there
7 a way to detect the state of that EPROM without applying
8 power to the integrated circuit that includes it?

9 A. I would say, just as with the fuse case, if I
10 want to find out what a programmed value is, I'm going
11 to have to read it or use it in some way that is
12 determinative of that value.

13 Q. Okay. Can you please look at column 1, lines
14 20 to 22 of the '492 patent. Maybe I should have had
15 them stapled, but I kind of like them -- I like them
16 loose.

17 A. Let me read 20 to 22.

18 Q. Sure.

19 A. Okay.

20 Q. So there it says, "For example, fuse
21 programmable latches are used to replace defective
22 memory cells with spare cells in semiconductor
23 memories"; correct?

24 A. I see where you're reading that, yes.

25 Q. Sure. Can you explain how at the time of the

1 filing of the '492 patent latches were used to replace
2 defective memory cells?

3 A. Sure. So memory cells are -- and again, in the
4 context of this discussion we're talking about large
5 memory arrays, not individual memory cells just randomly
6 present within a -- within a circuit.

7 So an array of memory cells is -- takes up a
8 significant amount of area and is also one of the denser
9 elements in terms of design and as a consequence tends
10 to have manufacturing yield issues. These --

11 Q. What do you mean by manufacturing yield issues?

12 A. The larger the area of a functional unit, the
13 higher the probability that a random defect affects that
14 functional unit. So in my case, the L2 cache on a
15 mobile P2 processor was well over 40 percent of the die
16 area. So if you just statistically play -- is there a
17 defect, it's a very high probability that it would,
18 without redundant circuitry, render the whole unit --
19 the whole cache inoperative.

20 So to your question, the memories work by
21 exposing an array of storage elements to decoders which
22 take an address and figure out, say, which row or column
23 of a memory to enable. And subsequently a selector --
24 or it can be combined with a sense amp but then takes
25 the value that's stored in those memory arrays and

1 provides it to whoever the reading element is. And as
2 you can imagine, when these arrays are large, these
3 decoders and these selectors are very wide. They would
4 generally be addressed such as, for instance, if I have
5 an end bit address, then I have two to the end different
6 possibilities of rows that I can select.

7 The idea of the redundancy is to place a soft
8 mapping between that decoding layer and the actual
9 application of the physical row of the memory such that
10 we can have redundant rows, essentially additional rows.
11 And when one of those rows is found to be defective
12 during testing, we then remap how the decoder would
13 address that row to something else. It would -- the
14 actual methods of doing so in general involve some form
15 of nonprogrammable element -- sorry. But programmable
16 nonvolatile element.

17 But the method in which the encoders and
18 decoders work is implementation specific. But the idea
19 is that I have two to the N possible selections of rows
20 of memory. I have two to the N plus a little bit. In
21 the case of cache, it can be between 3 and 5 percent,
22 depending on the unit. As much as you are allowed to
23 make. And of course, if you have extra space in the
24 reticle that your unit is being built in, it's always
25 good to put extra in there just for manufacturing yield.

1 And then during testing we will use the --
2 usually a scan mapping. So instead of actually using
3 the address pins from the device, we'll scan in an
4 address so that we can access each and every row,
5 including the surplus rows, the replacement rows.

6 Q. Okay.

7 A. Test them, identify which ones work, identify
8 which ones don't work, and then we use the fuse settings
9 in order to make sure that those that don't work are not
10 used and that there is an alternate row used for that
11 decoder.

12 Q. So you test all of the memory, including the
13 redundant cells that you've included to replace the
14 regular cells if something's wrong; correct?

15 MR. JONES: Objection to form.

16 THE WITNESS: Well, you -- as a general matter
17 you would not replace something that is found to be
18 defective by something that has not been found to be
19 working.

20 BY MR. ANDERSON:

21 Q. Okay. So assuming that there is some defective
22 portion of the array, the fuse is blown as a part of the
23 testing such that the substitution of the redundant
24 memory cells for the defective memory cells occurs while
25 you're still in the testing process?

1 MR. JONES: Objection to form.

2 THE WITNESS: The sequence of the events is
3 going to be specific to the manufacturer. I can only
4 speak to that in general the idea is to identify things
5 that are defective, and "map around" is the term we use
6 in the industry. The exact sequence of when that
7 happens during which part of operation, that's going to
8 be up to the manufacturing floor.

9 BY MR. ANDERSON:

10 Q. Is there a final stage of testing for memory
11 devices that ensures that the fuses that have been blown
12 have done what they were intended to do in terms of
13 ensuring that the entirety of the memory array is
14 functional?

15 MR. JONES: Objection to form.

16 THE WITNESS: I would say that there is in most
17 semiconductors a final quality test that applies to the
18 entire product. And by necessity if you have a memory
19 array, that would require testing that the entire memory
20 array works as intended. That may imply that a lot of
21 other things have happened as intended. But again, I
22 can't speak to the sequence or the specific operation.

23 BY MR. ANDERSON:

24 Q. Okay. But before they would take that memory
25 device and ship it off to a customer there's going to be

1 some testing that ensures that it's fully functional;
2 correct?

3 MR. JONES: Objection to form.

4 THE WITNESS: Again, we would have to look at
5 the specific customer because certainly in the case of
6 Intel, OEMs are customers. Distributors are customers.
7 In the Flash world it is actually customary to let
8 different OEMs and different, say, hard drive member
9 designers develop their own quality metrics. There are
10 several cases in which, say, your key chain Flash would
11 have a different quality level than, say, the Flash
12 that's being used in an enterprise hard drive, which
13 might have a different quality level than the Flash used
14 in an enterprise -- some kind of enterprise cache for,
15 say, a storage controller.

16 BY MR. ANDERSON:

17 Q. Sure.

18 A. It would not be out of question for the users
19 or the ultimate company that assembles the product to do
20 their own testing and to have NDAed appropriately so
21 that they can decide.

22 Q. What's good enough to ship?

23 A. What the remediating conditions would be.

24 Q. Okay. I understand. So when you're doing this
25 testing and you're blowing fuses when necessary, is the

1 power on or is the power off when you actually blow the
2 fuse?

3 MR. JONES: Objection to form.

4 THE WITNESS: I'm going to need you to clarify
5 which power you are talking about in this case.

6 BY MR. ANDERSON:

7 Q. So if -- I guess if the fuse is the type of
8 fuse that you blow by cutting it with a laser, right, is
9 that something that would be done while, like, VDD and
10 ground is being applied to the device and active testing
11 is ongoing, or is that something where you take it out
12 of that tester and would blow the fuse and then put it
13 back in the tester?

14 MR. JONES: Objection to form.

15 THE WITNESS: That would very much depend on
16 the technology. As a General Electric engineering
17 process I would not want to apply a laser to anything
18 that's not grounded.

19 BY MR. ANDERSON:

20 Q. Okay. Do you need to have VDD applied to blow
21 a fuse that's being cut with a laser?

22 A. I think if we speak generally about I can aim a
23 laser at any semiconductor and do whatever I want
24 whenever I want. Whether that's the appropriate method
25 for some specific manufacturer, I wouldn't want to speak

1 to that.

2 Q. Okay. So once the configuration of the fuses
3 has been finalized, is that when the memory device is
4 done with testing?

5 MR. JONES: Objection to form.

6 THE WITNESS: In answering that question, let
7 me make two important caveats here. You're asking about
8 fuses, and we do in the patent refer to nonvolatile
9 programming elements, so my answers are going to be
10 specific to fuses, not necessarily --

11 BY MR. ANDERSON:

12 Q. Yes, that's fair.

13 A. -- the operation for other forms of nonvolatile
14 elements.

15 When something is, quote/unquote, finished is
16 an operational procedure and they will defer within
17 every manufacturer, including even potentially outside
18 of the manufacturer through customer acceptance
19 criteria.

20 Q. I believe you already have a copy of your -779
21 declaration; correct? And when I say "-779
22 declaration," I'm referring to the declaration that you
23 submitted in support of Promos' response to the
24 petition, not the preliminary response, okay?

25 A. So I'm going to understand that you're

1 referring to the -779 submitted in December at some
2 point?

3 Q. Yes.

4 A. Yes, I have that declaration in front of me.

5 Q. Okay. And can we turn back to Figure 1 of the
6 '492 patent.

7 And Figure 1 shows a prior art programmable
8 latch; correct?

9 A. It does.

10 Q. And do you see the fuse F1 in Figure 1?

11 A. I do.

12 Q. And the fuse F1 is connected between VDD and
13 the terminal OUT; correct?

14 A. That's correct.

15 Q. And is it -- the '492 patent refers to the
16 terminal out.

17 Is there a difference between a terminal and a
18 node in your view of how circuits are described?

19 A. I would say outside the scope of a patent, I
20 think they could be used interchangeably. With respect
21 to a specific patent or -- I would look for those terms
22 perhaps, you know, being used in the claim language or
23 described in the specification.

24 Q. Looking at Figure 1, if I refer to the terminal
25 OUT as a node, would that seem out of the ordinary to

1 you?

2 A. We can agree that they're the same thing for
3 the purposes of this discussion.

4 Q. Okay. Because I default to node typically. So
5 if the fuse F1 is blown, is VDD going to be provided to
6 the out node?

7 A. Well, with Fuse 1 blown, the connection to VDD
8 is nonexistent or open.

9 Q. Okay.

10 A. I'm not sure what you mean by "provided," but I
11 think maybe perhaps we can rephrase that and say that
12 out is not connected to VDD or it's not shorted to VDD.

13 Q. Okay. So when -- in a specific memory device
14 that includes this programmable latch shown in Figure 1,
15 if this were using to replace defective memory cells, is
16 it your understanding that the fuse F1 would be blown
17 while VDD is on?

18 A. So replacing an -- a damaged memory cell is
19 something that occurs during operation of the circuit.
20 I don't quite understand how you are linking that with
21 the act of blowing the fuse.

22 Q. So when -- I guess what are the different ways
23 that fuses like fuse F1 can be programmed?

24 There are a few mentioned in the '492 patent;
25 correct?

1 A. So there are ways to program a fuse, and there
2 are ways to program nonvolatile elements at which --
3 maybe you can clarify exactly which portion of that
4 you're asking.

5 Q. Sure. Assume fuse F1 is a fuse and a memory
6 device and not an EPROM or an EEPROM.

7 What are the different ways to program that
8 fuse F1?

9 A. So there are two principal methods, and they
10 depend on the construction of the fuse. If the fuse is
11 metallic, then generally you would need a laser in order
12 to or some form of heat to impart enough local energy to
13 sublimate the metallic material. Now, that's different
14 and takes different methodologies based on whether
15 you're dealing with tungsten or something else or
16 aluminum just as a wiring layer, but you would need to
17 impart enough energy to sublimate the metal.

18 There are also resistive fuses made using
19 polysilicon. I'm unclear why someone would use a laser
20 perhaps on that, but I think it's certainly possible
21 physically to do so.

22 Q. Sure.

23 A. The preferred method there is to supply an
24 impulsive current sufficient to cause the resistor to
25 break.

1 Q. So the resistance in the fuse is such that,
2 when enough current is sent through it, it breaks the
3 connectivity of the resistor and makes an open circuit?

4 A. It would operate similarly as a fuse, say,
5 within your house where at a certain -- except the fuse
6 in the house is not destructive in terms of its ability
7 to open. But when the current -- at a certain current
8 level, all resistors will eventually fail, and it's
9 simply a question of designing the polysilicon element
10 in such a way that; one, it can be imparted with a
11 sufficient voltage to break and is preferentially thin
12 enough to where it doesn't take an enormous quantity of
13 current to do so.

14 Q. Okay. So earlier you indicated that if you
15 were going to cut a fuse with a laser, you would
16 definitely ground the integrated circuited that includes
17 the fuse; correct?

18 A. I said that outside the copy of this patent,
19 whenever dealing with a semiconductor and especially
20 something which is going to be imparting some form of
21 energy on to the semiconductor such as taking it in my
22 hand and moving it, I would prefer that that
23 semiconductor be grounded or that I had a ground strap
24 available so that I can be sure to be grounded.

25 Q. So --

1 A. That's just a general operating principle in
2 the semiconductor field.

3 Q. And if fuse F1 in Figure 1 was blown using
4 laser cutting, would a person of ordinary skill in the
5 art provide power in the VDD node that's shown in Figure
6 1 during that laser cutting?

7 MR. JONES: Objection to form.

8 THE WITNESS: We would have to look at the
9 specific processes and procedures that they have in
10 place.

11 BY MR. ANDERSON:

12 Q. Can you think of any advantages to providing
13 power on the VDD node while laser cutting is used to
14 program the fuse F1 in Figure 1?

15 A. Well, depending on how complex the fuse is --
16 and just for background, again, we're talking about a
17 nonprogrammable -- a nonvolatile programmable element.
18 So if there were a way to -- if there were a way to,
19 say, sense exactly when sufficient current had been
20 applied in order to not, say, overdo it, not apply too
21 much laser energy, in some situations that could be
22 advantageous. But again, we would have to look at the
23 specific manufacturing process and what procedures that
24 manufacturer had in mind.

25 Q. Could you please turn to paragraph 15 of the

1 -779 declaration.

2 A. Paragraph 15, yes.

3 Q. And just above paragraph 15 is a copy of Figure
4 1 of the '492 patent; correct?

5 A. That's correct.

6 Q. And in paragraph 15 you talk about how the
7 terminal OUT in Figure 1 is floating; correct?

8 A. Yeah. In specific certain circumstances,
9 terminal OUT may have a tendency to float, yes.

10 Q. And what does the '492 patent mean when it says
11 the terminal OUT is floating?

12 A. Well, floating is a term that is -- of art that
13 essentially means not strongly driven. In logic design
14 we have the concept of nodes especially within a latch.
15 A latch is essentially a feedback loop, a positive
16 feedback loop. And so the state of the latch will not
17 change unless there is significant effort made by other
18 circuitry to change that latch.

19 A node which is floating is not actively driven
20 by an element, and so therefore it is subject to
21 accumulating charge from other sources.

22 Q. So is the terminal OUT in Figure 1 of the '492
23 patent floating if the fuse F1 is intact?

24 MR. JONES: Objection to form.

25 THE WITNESS: If the fuse F1 is intact, then

1 the terminal OUT is shorted to VDD. Whether out is
2 floating then simply is a matter of whether VDD is
3 floating at that time.

4 BY MR. ANDERSON:

5 Q. Is that also true of Figure 2A of the '492
6 patent?

7 MR. JONES: Objection to form.

8 THE WITNESS: Maybe you can re-ask the question
9 with respect to 2A so I can look at it.

10 BY MR. ANDERSON:

11 Q. Sure. In Figure 2A if the fuse F1 is intact,
12 is the terminal OUT floating?

13 MR. JONES: Objection to form.

14 THE WITNESS: Again, the terminal OUT is on its
15 own neither floating nor nonfloating. It is shorted in
16 the case of Figure 2A when the fuse is intact to
17 terminal V and would take on whatever properties V has.

18 BY MR. ANDERSON:

19 Q. So assuming that VINT in Figure 2A is either
20 tied to ground or tied to some nonground voltage, if the
21 fuse F1 in Figure 2A is intact, would the terminal OUT
22 be considered to be a floating node?

23 MR. JONES: Objection to form.

24 THE WITNESS: You're using the term would it be
25 considered a floating node. A node is neither a

1 floating node nor nonfloating node. It can have a
2 tendency to float depending on conditions.

3 BY MR. ANDERSON:

4 Q. So in the context of the '492 patent in the
5 background when it talks about the terminal OUT being
6 floating, is the terminal OUT floating if the fuse is
7 intact?

8 MR. JONES: Objection to form.

9 THE WITNESS: If the fuse is intact, then
10 terminal OUT is effectively driven by V.

11 BY MR. ANDERSON:

12 Q. What is capacitive coupling?

13 A. Capacitive coupling occurs when a transition, a
14 voltage transition happens on a specific node and/or
15 wire or line or interconnect and there is a capacitance
16 between that node and a second node.

17 Because the capacitor is essentially a short at
18 high frequency, a sufficiently fast transition can cause
19 coupling, which means that a charge will be accumulated
20 on the second node as a result of the transition. The
21 transition is sometimes called an attack, but that
22 depends a little bit more on what kind of circuit you're
23 designing.

24 Q. So looking at Figure 1 of the '492 patent, if
25 the fuse in Figure 1 has been blown and power is ramped

1 up on VDD, will capacitive coupling cause the voltage on
2 the terminal OUT to rise?

3 A. So it would be possible to have capacitive
4 coupling on to VDD itself. That's not -- that's not
5 precluded by any specific design. You're asking if the
6 node can have capacitive coupling, and like I said, any
7 node could have capacitive coupling.

8 Q. Sure. I'm trying to give a specific example.
9 So looking at the circuit in Figure 1 and assuming that
10 the fuse F1 has been blown such that it's an open
11 circuit, okay?

12 A. Okay. You're -- I'll just note that your
13 previous question F1 was closed -- was closed on
14 program.

15 Q. Oh. If it was, I apologize. So let's -- let's
16 start over then.

17 So looking at Figure 1 --

18 A. Yes.

19 Q. -- fuse F1 has been blown.

20 A. Understood.

21 Q. And it's an open circuit, okay? And you apply
22 VDD -- you apply a voltage to VDD, so you start ramping
23 up VDD and voltage.

24 Will that cause the voltage at the terminal OUT
25 to rise?

1 A. The change in voltage at the terminal OUT is
2 going to be determined by the point at which the
3 inverters 120.1.2.3 have their power ramped to them and
4 correctly assume their final values.

5 If we take Figure 1 in isolation, so basically
6 everything below VDD and we do not talk about what's
7 happening to those inverters and the fuse is blown, then
8 what happens on VDD is isolated to what happens on VDD.
9 The terminal OUT is not going to -- is going to be
10 impacted by the ramp up power to the inverters 120. Not
11 to the VDD on top of the fuse.

12 Q. So when the '492 patent talks about capacitive
13 coupling in the background, you think it's talking about
14 capacitive coupling between the power being supplied to
15 the inverters and the terminal OUT; is that correct?

16 A. That's not correct.

17 Q. Okay. I misunderstood your last answer then.

18 Can you explain what the capacitive coupling
19 issue is with respect to the terminal OUT as -- let me
20 rephrase.

21 So in column 1 at line 42 of the '492 patent it
22 says, "In addition, the terminal OUT potential may
23 become 'unstable due to capacitive coupling' in the
24 integrated circuit."

25 A. That's correct.

1 Q. Is it your understanding that that capacitive
2 coupling is going to be problematic whether or not the
3 fuse F1 has been blown?

4 A. The capacitive coupling is problematic whenever
5 the node is not driven. It's when the node is floating.

6 The patent and the specific -- and even the
7 specific portion of it that you're reciting does not
8 describe the source of the capacitive coupling if -- and
9 again, your questions were a little bit back and forth,
10 so let me address both situations. If Fuse 1 is not
11 blown so it is conductive, then the terminal OUT is
12 shorted to VDD, and whatever properties the terminal VDD
13 has the terminal OUT has as well because they're
14 shorted.

15 In the event that the fuse is blown they are
16 disconnected, and at that point the terminal OUT will
17 have different properties than VDD.

18 All nodes, regardless of what they are called
19 or what they do, may be subject to capacitive coupling,
20 and the patent is not -- describes the effect of
21 capacitive coupling on the out node, but it is not
22 describing the source of that coupling.

23 Q. Okay. I -- so if I understand what you're
24 saying correctly, if the fuse F1 is not blown, then the
25 terminal OUT is going to move with VDD.

1 A. Well, we're assuming that an unblown fuse is a
2 short.

3 Q. Yes.

4 A. So for that purpose, the terminal out will have
5 whatever potential VDD has.

6 Q. So would capacitive coupling influence the
7 terminal OUT if the fuse is not blown and VDD is held at
8 ground?

9 A. Whatever happens in that scenario, the VDD will
10 happen to out.

11 Q. And so assume that VDD is held at ground and
12 the fuse is not blown, would capacitive coupling
13 influence the state of the terminal OUT?

14 A. Again, you're using the term "held at ground."

15 Q. Yes.

16 A. And if we could -- if we could rephrase that to
17 strongly driven to the point of resisting capacitive
18 coupling, then VDD would not be in that situation
19 impacted by capacitive coupling by definition because it
20 is strongly driven to such an extent that it is not
21 impacted by it. And by virtue of Fuse 1 being
22 unprogrammed and conductive, node out would similarly
23 not be impacted because it inherits all the properties
24 from VDD.

25 Q. Okay. Looking at Figure 1, where are the

1 sources of voltage that could influence terminal OUT due
2 to capacitive coupling?

3 A. They are not necessarily shown in Figure 1.
4 The sources of capacitive coupling are myriad. It could
5 be any interconnect, any signal, any node which has some
6 capacitance to the output nodes. It could be an
7 interconnect traveling over it in parallel to wiring
8 that is tied on the output node. It could be things
9 that are coupled to transistors or logic which uses the
10 out node further on down the logic.

11 Q. So limiting the discussion to what is shown in
12 Figure 1, is VDD the only voltage source shown in Figure
13 1?

14 A. Well, Figure 1 -- if we discuss voltage sources
15 as positive voltage sources relative to ground, then VDD
16 is the only shown voltage source in Figure 1. The
17 voltage source for the inverters is not shown.

18 Q. Does the '492 patent indicate what voltage
19 source is supplied to those inverters?

20 A. We'd have to look through the discussion of
21 Figure 1. But certainly as a prior art element, it
22 could be VDD. It could be another supply.

23 Q. So if the power is off to the circuit in Figure
24 1 and VDD is held strongly at ground, would capacitive
25 coupling be an issue with respect to the terminal OUT?

1 MR. JONES: Objection to form.

2 THE WITNESS: You're making a contradictory
3 statement here. You're saying that power is off, but
4 yet it is strongly driven. So perhaps you can --

5 BY MR. ANDERSON:

6 Q. Oh.

7 A. Maybe you can clarify that.

8 Q. Assume that VDD is held strongly at ground and
9 the ground terminal is held strongly at ground. Are
10 there any capacitive coupling issues with respect to the
11 terminal OUT in Figure 1?

12 MR. JONES: Objection to form.

13 THE WITNESS: So I would -- let's start with
14 the term "issues." If we assume that an issue is a
15 potential incorrect use of a signal, then if the power
16 is off nothing is using that signal. So there may -- if
17 there are other elements that are on that provide some
18 capacitive coupling, maybe that wouldn't cause an issue
19 simply because nobody is using the circuit. It's off.

20 BY MR. ANDERSON:

21 Q. If the fuse in figure F1 is not blown, is
22 capacitive coupling going to potentially cause an
23 erroneous state to be read from the latch in Figure 1?

24 A. Again --

25 MR. JONES: Objection to form.

1 THE WITNESS: If the fuse in Figure 1 is not
2 blown, so it's conductive --

3 BY MR. ANDERSON:

4 Q. Yes.

5 A. -- then the conditions that apply to the
6 terminal out are determined by the conditions that
7 apply to VDD, and you can't make an assumption about out
8 without understanding what the conditions are on VDD.

9 Q. So it's your opinion that the capacitive
10 coupling issues are not limited to the case where the
11 fuse F1 has been blown in Figure 1; is that correct?

12 A. I'm sorry. Capacitive coupling is an issue for
13 all designs. I'm not sure what you mean by whether
14 it -- how it could really apply in certain
15 circumstances.

16 Q. Sure. So when the '492 patent says that the
17 "OUT potential may become 'unstable due to the
18 capacitive coupling' in the integrated circuit," is that
19 situation going to be true if the fuse F1 is not blown?

20 MR. JONES: Objection to form.

21 THE WITNESS: If the fuse F1 is not blown, then
22 the susceptibility of the terminal OUT to any condition
23 is determined by the susceptibility of VDD to the same
24 condition because they are shorted.

25 ///

1 BY MR. ANDERSON:

2 Q. Does the '492 patent provide a technique for
3 resolving capacitive coupling issues with respect to the
4 VDD voltage being unstable?

5 A. I'm not sure that the '492 patent describes
6 capacitive coupling on to the VDD node. The '492 patent
7 is dealing with a capacitive coupling on the out node.

8 Q. Can you please turn to paragraph 16 of your
9 declaration.

10 A. So I'm at paragraph 16 of -779.

11 Q. Thank you. So in paragraph 16 you indicate
12 that "The solution presented in the '492 patent
13 accomplishes the twin goals of preventing the output
14 node (terminal OUT) from floating above ground when
15 power is off and from destabilizing through capacitive
16 coupling during power-up."

17 A. That's correct.

18 Q. What is the solution that is presented in the
19 '492 patent that you were referring to in paragraph 16?

20 A. Well, the '492 patent presents two solutions.
21 It presents a diode which is provided as in Figure 2
22 between out and the first terminal of the programmable
23 element which acts to dissipate accumulated charge. And
24 this -- this diode is capable, among other things, of
25 dissipating charge that after power is just starting so

1 when power is ramping, that that could be induced by
2 capacitive coupling. The '492 patent also -- for
3 instance, that's claim 1 of the '492 patent.

4 Q. So can we look at claim 1 really quickly.

5 A. Sure.

6 Q. So I'm looking at column 8 of the '492 patent,
7 and at line 55 it recites a diode; correct?

8 A. That's correct.

9 Q. And is it your understanding that that diode
10 recited in claim 1 would correspond to the diode 234
11 that's depicted in Figure 2A of the '492 patent?

12 A. Yes. That is diode 234 of Figure 2A.

13 Q. And -- okay. And can you tell looking at
14 Figure 2A whether or not that diode 234 is a p-n
15 junction diode?

16 A. Figure 2A doesn't speak to that necessarily. I
17 think specification has mentioned that it could be a p-n
18 junction, but it could also be a Schottky diode.

19 Q. So how does the diode 234 dissipate the charge
20 on the terminal OUT in Figure 2A?

21 A. Let's -- let's take the assumption that V is at
22 ground and the fuse F1 is open, programmed basically
23 nonconductive. We can assume for the sake of argument
24 that before the power ramp has started or even during
25 the power ramp for that matter, there is some capacitive

1 coupling that causes charge to accumulate on the node
2 out. This would use the voltage on the out node to
3 start rising because transistor 110 is not on, and so
4 there is no place for that charge to go.

5 At the point where that accumulated charge
6 results in a voltage above the diode threshold voltage,
7 diode 234 starts conducting. Essentially it forms a
8 clamp from the node out on to the VINT of Figure 2,
9 thereby dissipating that charge. As long as VINT is at
10 ground, it won't matter whether that is just after
11 programming or whether that is just before power-up or
12 enduring the power-up before the threshold voltages have
13 been met for the inverter. As soon as the out node
14 reaches at least one diode threshold above ground, then
15 that accumulated charge will leak through diode 234,
16 basically clamping the voltage of out and limiting its
17 ability to rise beyond one diode threshold.

18 Q. Is there any difference between dissipating
19 voltage at the node out and dissipating charge at the
20 node out?

21 A. From an electrical engineering perspective,
22 yes. So voltage, if you look at the I-V curve of a
23 diode, the p-n junction will not sustain above a diode
24 threshold because the diode essentially becomes super
25 conductive if the voltage tries to exceed the diode

1 threshold voltage even by a little bit. That's the
2 famous hockey stick curve which I know Dr. Baker
3 mentioned.

4 Charge is basically a function of density of
5 charge carriers, so electrons holes or other matter, and
6 the voltage generated by that charge is dependent on the
7 resistance of the path to which it is dissipated.

8 So we can say that the voltage is clamped but
9 the amount of charge that that would entail is
10 implementation-specific because we have to look at the
11 specific device to understand how much charge is
12 required to achieve a specific voltage.

13 Q. Okay. Could you please turn to paragraph 23 of
14 your -779 declaration. And do you see the proposed
15 construction of the term "a terminal T1 for providing a
16 signal indicating a state of the programmable latch" is,
17 quote, a terminal T1 from which voltage is dissipated
18 after programming in order to provide a signal
19 indicating a state of the programmable latch, closed
20 quote, in that construction is dissipating voltage the
21 same as dissipating the charge at the terminal OUT?

22 A. Both will have to happen at the same time.
23 It's the same physical mechanism of charge carriers
24 moving across the p-n junction. The reason why voltage
25 is appropriate there is because it's the voltage that

1 causes the wrong value. It's not possible to say that a
2 certain amount of charge directly causes a wrong value.
3 It could in a certain implementation, but we know that
4 if a node assumes the wrong voltage that it assumes the
5 wrong value, and therefore it corrupts the signal that
6 that value is meant to impart.

7 Q. So in Figure 2A if the voltage at the terminal
8 OUT is greater than the threshold voltage of the diode
9 234 and the fuse is blown and VINT is at ground, then
10 the diode 234 will dissipate the voltage on the terminal
11 OUT; is that correct?

12 A. It will hold that voltage to below a -- the
13 threshold voltage of the diode. All of the current --
14 sorry. All of the charge will eventually dissipate, but
15 it dissipates much more quickly when you are close to
16 the threshold voltage. As an example, if you consider
17 the I-V curve of the diode, if the voltage is even a
18 little bit trying to tend above the threshold voltage,
19 then there's an almost infinite current capacity. So
20 the discharging of charge occurs very quickly.

21 As that voltage drops, you start getting into
22 the flat section of the I-V curve, and at that point
23 it's simply a slower process to discharge the node.

24 Q. So if the diode 234 in Figure 2A is conductive
25 and it is dissipating charge from the node out, is it

1 your understanding that that is how the voltage at the
2 node out is dissipated according to the construction in
3 paragraph 23 of your declaration?

4 A. Yes. It's any voltage -- any amount of charge
5 that can cause the voltage to exceed the voltage
6 threshold will be dissipated. I think it would be more
7 correct to say that it confines the voltage on the out
8 to a certain threshold.

9 Q. And it does that by dissipating charge from the
10 node out by providing a path for that charge to flow to
11 ground; is that correct?

12 A. That's the way the diode works, yes.

13 Q. So if -- so in the context of Figure 2A of the
14 '492 patent, does the terminal OUT satisfy the
15 construction for the terminal T1 claim term that you've
16 included in paragraph 23 of the -779 declaration?

17 A. I'm sorry. Maybe I misunderstood the question.
18 Could you repeat that maybe in a different way?

19 Q. Sure. So claim 1 recites a terminal T1 for
20 providing a signal indicating a state of the
21 programmable latch; correct?

22 A. Yes. I see that limitation of claim 1.

23 Q. Okay. And in paragraph 23 of your -779
24 declaration, you indicate that you understand that
25 Promos has proposed a construction of that term that is,

1 quote, a terminal T1 from which voltage is dissipated
2 after programming in order to provide a signal
3 indicating a state of the programmable latch.

4 Do you see that?

5 A. Yes. That's my opinion.

6 Q. So in Figure 2A of the '492 patent, does the
7 terminal OUT satisfy that claim limitation? Does the
8 terminal OUT provide a terminal T1 from which voltage is
9 dissipated after programming in order to provide a
10 signal indicating a state of the programmable latch?

11 A. So let me answer that this two parts. The
12 patent describes two ways in which the voltage can be
13 dissipated after programming. One of those is the
14 diode, and that is reflected in Figure 2A as the
15 terminal T1 being out, the diode being element 234 and
16 the voltage dissipate after programming being charge
17 that has accumulated on out at some point after
18 programming. This limitation also appears in claim 14
19 which does not involve a diode, and Figure 2A does not
20 speak directly to the condition in claim 14. Claim 14
21 requires that the -- that the charge be allowed to
22 dissipate after programming.

23 Q. So is it your opinion that claim 14 would not
24 cover the embodiment shown in Figure 2A of the '492
25 patent because it includes a diode?

1 A. That's not my opinion.

2 Q. So just to be clear, as shown in Figure 2A, is
3 terminal out a terminal from which voltage is dissipated
4 after programming in order to provide a signal
5 indicating a state of the programmable latch?

6 A. Yes.

7 Q. We've been going quite a while. I just
8 realized that. Sorry. Would you like to take a break?

9 A. I'm -- your call.

10 MR. JONES: Yeah. Let's take a short break. I
11 could use one.

12 (Recess taken from 10:37 a.m. to 10:47 a.m.)

13 BY MR. ANDERSON:

14 Q. Okay. Could you please turn to column 5, line
15 51 of the '492 patent. Do you see at line 51 it says,
16 "In some embodiments, diode 234 is omitted"?

17 A. I see that.

18 Q. Is there a figure in the '492 patent that shows
19 an embodiment where the diode is omitted?

20 A. I think to the extent that the figures are
21 illustrative of embodiments, if you have a discussion
22 about Figure 2A and you describe that there's an
23 embodiment that is similar to that but the diode is
24 omitted, then Figure 2A is serviceable for that
25 discussion.

1 Q. So if the diode 234 in Figure 2A were omitted
2 from Figure 2A, would you agree that the resulting
3 circuit corresponds to the embodiment that's being
4 described at column 5, line 51?

5 A. The column -- the column 5 embodiment is
6 describing a specific embodiment. It doesn't describe
7 what other features of that embodiment has. For the
8 purposes of claim construction I looked at the claims,
9 not arbitrary portions of embodiment.

10 Q. So the embodiment that's in column 5 at line
11 51, do you understand that embodiment to still retain
12 the rest of the structural features shown in Figure 2A
13 aside from the diode?

14 A. I understand those embodiments to have the
15 diode omitted, and that is the extent to which we can
16 understand a specific feature of that embodiment.

17 Q. Okay. So if we look at column 5, line 52 it
18 says, "Nevertheless, if the fuse F1 is nonconductive,
19 the terminal OUT is at ground before power-up."

20 So if the '492 patent is discussing fuse F1 and
21 the terminal OUT at line 52 and 53, what fuse F1 and
22 what terminal OUT is the '492 patent talking about
23 there?

24 A. Well, it's talking about an embodiment that
25 they are discussing. I'm going to point out that fuse

1 F1 and the terminal OUT exists in multiple figures and
2 could exist in other embodiments.

3 Q. So does the embodiment that starts at column 5,
4 line 51 include an inverter?

5 MR. JONES: Objection to form.

6 THE WITNESS: Again, the text at line -- at
7 column 5, line 51 and onward are describing an
8 embodiment where the diode is omitted. I don't see any
9 mention of inverters. We would have to look at
10 embodiments in the claims to understand whether the
11 claims themselves require inverters.

12 BY MR. ANDERSON:

13 Q. Okay. Let's look at claim 14.

14 Is there a figure in the '492 patent that you
15 think is representative of the elements that are
16 included in claim 14?

17 MR. JONES: Objection to form.

18 THE WITNESS: Again, I analyze the claim as a
19 claim. I'm not trying to tie it to a specific figure.

20 BY MR. ANDERSON:

21 Q. Does Figure 2A disclose a circuit that includes
22 all the elements that are recited in claim 14?

23 A. That sounds like you're asking an infringement
24 opinion, and I'd have to look at the specific circuiting
25 question in order to understand whether it practices

1 claim 14.

2 Q. Okay. You have the circuits in Figure 2A, so
3 let's step through claim 14 and see if we can find the
4 respective elements in Figure 2A.

5 So do you understand Figure 2A to show a
6 programmable latch?

7 A. Yes. I see a programmable latch.

8 Q. And how do you know that that latch is a
9 programmable latch?

10 A. I would say because the description of Figure
11 2A in the patent specification describes it as a
12 programmable latch and the fuse element F1 is
13 programmable.

14 Q. And does the circuit in Figure 2A include a
15 first terminal for receiving a constant nonground
16 voltage throughout operation of the latch?

17 A. That is unclear from Figure 2A.

18 Q. And what is unclear about that?

19 A. Well, as you'll note, the construction we're
20 using for throughout operation of the latch means at all
21 times during circuit operation without being disabled.

22 Q. Okay.

23 A. And that information is not salient from Figure
24 2A.

25 Q. And when you say "that information," what

1 information are you referring to in the construction?

2 A. Whether it is receiving a constant nonground
3 voltage at all times during circuit operation without
4 being disabled.

5 Q. Is the EVCC signal provided in Figure 2A
6 throughout operation of the circuit shown in Figure 2A?

7 A. That's not made clear by Figure 2A.

8 Q. What do you understand the EVCC signal to be in
9 the context of Figure 2A?

10 A. We can look at the exact description of Figure
11 2A and the description of Figure 2A which I'm going to
12 note again is not claim -- is not directly being
13 analyzed for here. I'm looking at claim 14 whether I'm
14 looking at claim 14, not Figure 2A.

15 Q. My -- so I'll just repeat the question. What
16 is the EVCC signal 214 in Figure 2A?

17 A. It is described as the external power supply
18 voltage, the EVCC.

19 Q. Is the external power supply voltage EVCC 214 a
20 voltage that will be a constant nonground voltage supply
21 throughout operation of the integrated circuit that
22 includes the circuit shown in Figure 2A?

23 A. Again, using the proper construction it is not
24 clear that it is available at all times during circuit
25 operation without being disabled as that term is

1 described in the specification.

2 Q. Is the circuit of Figure 2A able to operate
3 without any power supply being provided to it?

4 A. I think we -- as a general matter of
5 semiconductors outside of the scope of this patent,
6 semiconductors are said to operate when power is
7 applied.

8 Q. Right. So is the circuit of Figure 2A capable
9 of operation without any power being supplied on the
10 EVCC terminal?

11 A. Again, as a generic matter, outside of the
12 analysis of claim 14, I'm going -- I think it's safe to
13 assume that any semiconductor is -- cannot operate
14 without being powered.

15 Q. So throughout operation of the circuit shown in
16 Figure 2A, EVCC is necessarily a positive nonground
17 voltage, is it not?

18 A. That is not clear from the specifications
19 description of what throughout operation of the latch
20 means.

21 Q. I'm sorry. I don't think I said throughout
22 operation of the latch.

23 Speaking of the circuit that's shown in Figure
24 2A and 23 that circuit is operating, isn't it necessary
25 for EVCC to be a nonground voltage?

1 A. Again, without confining ourselves to claims or
2 any specific figure, if there is a semiconductor and you
3 represent to me that it's operating, I think I can
4 safely assume it's powered.

5 Q. So if the circuit of Figure 2A is operating,
6 then EVCC is going to be a positive nonground voltage;
7 correct?

8 A. I think there are embodiments wherein, for
9 instance, Figure A where VINT is less than ground.

10 Q. I'm sorry. I'm specific to Figure 2A here. So
11 if the circuit of Figure 2A is operating, then EVCC is
12 going to be a positive nonground voltage; correct?

13 MR. JONES: Objection to form.

14 THE WITNESS: If the circuit is operating, then
15 the value of EVCC is whatever voltage is required to
16 make the circuit operate.

17 BY MR. ANDERSON:

18 Q. Can it be ground?

19 A. I would say that the circuit still could be
20 made to work if you apply the negative voltage to where
21 the ground terminals were in Figure 2A. And again,
22 speaking strictly about the circuit in Figure 2A, any
23 semiconductor vice requires a potential difference in
24 order to operate, and it is not necessarily aware of the
25 absolute value of those potential differences.

1 Q. So going back to claim 14, assuming that EVCC
2 is a positive nonground voltage and VINT is also a
3 positive nonground voltage, does the terminal 212 where
4 VINT is constitute a first terminal for receiving a
5 constant nonground voltage throughout operation of the
6 latch?

7 A. That's not clear.

8 Q. What aspect of it is not clear?

9 A. Throughout operation of the latch aspect is
10 unclear.

11 Q. Is that because the VINT signal can be enabled
12 or disabled?

13 A. That is because the patent describes the
14 conditions which constitute a throughout operation of
15 the latch.

16 Q. What are the conditions that constitute
17 throughout operation of the latch?

18 A. So I'm going to refer you to column 4, line 66
19 through column 5, line 7. It notes that at the
20 conclusion at the end of this paragraph is that VINT
21 voltage is under this condition a constant value
22 throughout the operation of the integrated circuit, and
23 those conditions are described in the paragraph above
24 which is that there are selective generators, some of
25 which can be disabled but the particular generator that

1 supplies VINT is not disabled. So the condition is the
2 not being disabled in the presence of circuitry which
3 can be disabled.

4 Q. I want to make sure I understand this. So
5 you're saying that VINT can be enabled or disabled
6 according to this portion of the '492 patent, namely
7 column 4, line 66 through column 5, line 7?

8 A. No.

9 Q. Okay. Does the description in the '492 at
10 column 4, line 66 through column 5, line 7, refer to
11 Figure 2A?

12 A. It refers to some embodiments. It -- that's
13 the extent to which it refers to anything else.

14 Q. Is it referring to embodiments that are
15 synchronous DRAM embodiments?

16 A. It is discussing the synchronous DRAM
17 embodiments, but certainly the situation of the VINT
18 voltage being a constant value throughout the operation
19 of the integrated circuit could exist in other devices.

20 Q. Does the paragraph that starts at column 4,
21 line 66 and ends in column 5, line 7 use the term
22 "throughout operation of the latch"?

23 A. I believe it does. When they're saying
24 throughout the operation of the integrated circuit,
25 that's -- that's synonymous.

1 Q. Does that go both ways? So in the construction
2 that says "throughout the operation of the circuit,"
3 does that mean throughout operation of the latch?

4 A. Well, we're talking about the term "VINT" here,
5 so it would be throughout the operation of circuitry
6 which is powered by the VINT voltage.

7 Q. In synchronous DRAM embodiments that include
8 several generators 213, is each of those generators going
9 to generate a different VINT signal?

10 MR. JONES: Objection to form.

11 THE WITNESS: There is no specification in
12 the -- in column 4:66 through 5:7 regarding the voltages
13 provided by the other generators.

14 BY MR. ANDERSON:

15 Q. Let's go back to claim 14. If VINT is
16 generated as is discussed at the bottom of column 4 and
17 the top of column 5, the paragraph that we just
18 referenced, column 4, lines 66 through column 5, line 7,
19 if VINT is generated according to that paragraph in
20 Figure 2, does the VINT terminal constitute a first
21 terminal for receiving a constant nonground voltage
22 throughout operation of the latch in the context of
23 claim 14?

24 A. Again, to ascertain whether a particular device
25 practices claim 14, I need to see the device. Your

1 question seemed to ask whether if the terminal
2 corresponded to -- I'm sorry. If the voltage generator
3 corresponded to the language in column 4:66 through 5:7
4 and satisfied the condition, the VINT voltage is a
5 constant value throughout the operation of the
6 integrated circuit. Then by definition it is a constant
7 value throughout the operation of the circuit, and so
8 the property follows from the definition.

9 Q. Is it your opinion that based on Figure 2A you
10 cannot tell whether the terminal 212 is a terminal for
11 receiving a constant nonground voltage throughout
12 operation of the latch as that language is used in claim
13 14?

14 A. Again, speaking just to the description as
15 provided in Figure -- of Figure 2A, there is no
16 description of other generators that are disabled while
17 the VINT generator is -- remains enabled.

18 Q. Is it your understanding that in order to
19 satisfy the first terminal limitation in claim 14 you
20 have to have multiple voltage generators within the
21 integrated circuit?

22 A. Well, it's my understanding that the language
23 of the limitation must be met. The limitation language
24 throughout operation of the latch appears once and only
25 once in the specification, and it has a meaning which is

1 that that particular voltage is not disabled when others
2 are disableable. That is the direct language from
3 column 4:66 through 5:7. So again, conducting a -- if I
4 were to conduct an infringement analysis, that could
5 would be the correct way to ascertain whether the
6 limitation is met.

7 Q. So is it your understanding that, in order to
8 satisfy the first terminal limitation in claim 14, you
9 would have to have multiple voltage generators within
10 the integrated circuit?

11 A. I think in order to correspond to the language
12 in column 4, which I think we can read directly so
13 that -- make sure this is absolutely accurate --

14 Q. I think my question was about the limitation in
15 claim 14. So does the limitation in claim 14 require
16 that the integrated circuit that includes the
17 programmable latch necessarily has multiple internal
18 voltage generators?

19 A. I think it requires, as the language says, that
20 at least one generator is enabled throughout the circuit
21 operation. It's never disabled. And that at least one
22 generator being the VINT generator. And the fact that
23 it is not disabled at any point affords it the
24 description of providing a constant value throughout the
25 operation.

1 Q. Does the limitation in claim 14 require that
2 the integrated circuit that includes the programmable
3 latch necessarily has multiple internal voltage
4 generators?

5 MR. JONES: Objection. Asked and answered.

6 THE WITNESS: Again, the limitation of the
7 claim simply requires that it meet the language as -- of
8 the -- throughout the operation as it's described in the
9 specification which is to say that at least one
10 generator is enabled throughout circuit operation and
11 that by -- by meeting that requirement, the voltage
12 generated therein is a constant value throughout the
13 operation of the integrated circuit. That's the
14 requirement.

15 BY MR. ANDERSON:

16 Q. So only one voltage generator is required in
17 order to satisfy the provision of a constant nonground
18 voltage throughout operation of the latch in claim 14;
19 is that correct?

20 MR. JONES: Objection to form.

21 THE WITNESS: Again, claim 14 -- and I'm
22 reading the first limitation -- says "a first terminal
23 for receiving a constant nonground voltage throughout
24 operation of the latch." That's for receiving a
25 constant nonground voltage.

1 Reviewing the language of the specification to
2 understand throughout the operation of the latch, go to
3 column 4:66 through 5:7. It says that "at least one
4 generator 213 is enabled throughout the circuit
5 operation in order to power circuits that are never
6 disabled."

7 And this "at least one generator," the VINT
8 voltage in this case has a constant value throughout the
9 operation of the integrated circuit. That is the
10 requirement to meet the limitation.

11 BY MR. ANDERSON:

12 Q. Can you look at Figure 4 of the '492 patent.

13 A. Figure 4. Okay.

14 Q. Assume that an integrated circuit includes the
15 internal voltage generator shown in Figure 4, and EVCC
16 is the external power supply, and that is the only VINT
17 generator included in the integrated circuit.

18 Would the VINT signal shown in Figure 4 be a
19 constant nonground voltage that is provided throughout
20 operation of the latch, assuming that VINT connected to
21 the VINT terminal of Figure 2A?

22 A. Well, there was a lot of supposing there, but
23 my answer is that in order to ascertain whether there is
24 actual practice of the claim, that's an infringement
25 opinion, and I'm going to need to see the device, the

1 whole device.

2 Q. Well, the whole device is Figure 2A plus Figure
3 4. That's a programmable latch with an internal voltage
4 generator.

5 Is there anything else that's necessary to
6 practice claim 14?

7 A. Well, in order to provide an infringement
8 opinion on 14, I need to see the device.

9 Q. I'm not asking for an infringement opinion.
10 I'm asking if Figures 2A and 4 together support claim 14
11 of the '492 patent.

12 MR. JONES: Objection to form.

13 THE WITNESS: Again, if you're asking me if
14 something supports or conforms to claim 14, I'm sorry.
15 That's an infringement opinion, and I would need to see
16 the device in order to understand that.

17 BY MR. ANDERSON:

18 Q. So you cannot map claim 2A to claim 14?

19 MR. JONES: Objection to form.

20 THE WITNESS: As I've stated, Figure 2A is not
21 claim. It's a figure.

22 BY MR. ANDERSON:

23 Q. Yes. It's a figure that includes a number of
24 circuit elements; correct?

25 A. Figure 2 does have a number of circuit

1 elements.

2 Q. And you cannot tell from looking at Figure 2A
3 whether or not the VINT terminal corresponds to a first
4 terminal for receiving a constant nonground voltage
5 throughout operation of the latch shown in Figure 2A
6 when the internal voltage generator shown in Figure 4 is
7 used as the VINT generator 213 in Figure 2A? You're
8 unable to determine whether or not VINT satisfies that
9 claim element?

10 A. I am unable to provide an infringement opinion
11 on -- unless I see the entirety of the device.

12 Q. I didn't --

13 A. And have all the supporting materials for it.

14 Q. I didn't ask for an infringement opinion. I'm
15 asking whether or not what's shown in Figure 2A would
16 constitute a first terminal for receiving a constant
17 nonground voltage throughout operation of the latch in
18 the context of claim 14.

19 What else beyond what's in Figure 2A do you
20 need to know in order to make that determination?

21 A. If you're asking me anything in the context of
22 claim 14, you're asking me an infringement opinion. So
23 I think I've already answered the question.

24 Q. Okay. So it -- do you have an opinion as to
25 whether or not -- no. Strike that.

1 Does Figure 2A disclose a first terminal for
2 receiving a constant nonground voltage throughout
3 operation of the latch?

4 MR. JONES: Objection. Asked and answered.

5 THE WITNESS: I think I've already said that's
6 unclear.

7 BY MR. ANDERSON:

8 Q. So you do not know whether or not Figure 2A
9 discloses a first terminal for receiving a constant
10 nonground voltage throughout operation of the latch as
11 that term is used in claim 14?

12 MR. JONES: Objection. Asked and answered.

13 THE WITNESS: Yeah. Whether that limitation is
14 met is based on the entirety of the device matching the
15 properly construed language.

16 BY MR. ANDERSON:

17 Q. Does Figure 6 disclose a first terminal for
18 receiving a constant nonground voltage throughout
19 operation of the latch?

20 A. Again, that's also unclear.

21 Q. Can you point to any figure in the '492 patent
22 that discloses a first terminal for receiving a constant
23 nonground voltage throughout operation of the latch?

24 A. There's no need to point to a figure because
25 it's specified in the specification what that means.

1 And it is specified, as I said, column 4, line 66
2 through column 5, line 7.

3 Q. I didn't ask whether there was a need to point
4 to a figure. I asked can you point to any figure in the
5 '492 patent that discloses a first terminal for
6 receiving a constant nonground voltage throughout
7 operation of the latch.

8 A. Okay. The properly construed term throughout
9 operation of the latch means at all times during circuit
10 operation without being disabled. Figures are figures.
11 Devices are devices. And the devices will describe
12 under what conditions they are or are not disabled which
13 is why I repeat if you are asking an infringement
14 opinion, I need to see the device.

15 Q. If EVCC is a constant nonground voltage
16 throughout operation of the latch, can you point to any
17 figure in the '492 patent that discloses a first
18 terminal for receiving a constant nonground voltage
19 throughout operation of the latch?

20 MR. JONES: Objection to form.

21 THE WITNESS: Again, the support for that comes
22 from the specification which is describing some
23 embodiments. Those embodiments could be any of the
24 figures.

25 ///

1 BY MR. ANDERSON:

2 Q. So if EVCC is a constant nonground voltage
3 throughout operation of the latch, can you point to any
4 figure in the '492 patent that discloses a first
5 terminal for receiving a constant nonground voltage
6 throughout operation of the latch?

7 MR. JONES: Objection to form.

8 THE WITNESS: Again, any figure in the context
9 of the specification language, column 4, line 66 through
10 column 5, line 7 describes the aspect throughout the
11 operation of the latch.

12 BY MR. ANDERSON:

13 Q. So if EVCC is a constant nonground voltage
14 throughout operation of the latch, is the VINT signal in
15 Figure 4 a constant nonground voltage throughout
16 operation of the latch?

17 A. I don't see anything in the language that
18 describes throughout the operation of the latch, so
19 that's column 4, line 66 through column 5, line 7 that
20 describes EVCC.

21 Q. I provided a very specific limitation on EVCC.
22 EVCC -- assume EVCC is a constant nonground voltage
23 throughout operation of the latch.

24 With that assumption looking at Figure 4, will
25 VINT also necessarily be a constant nonground voltage

1 throughout operation of the latch?

2 A. I'm looking to the necessary specification for
3 the definition of throughout operation of the latch.
4 EVCC is not described, and so what -- there's no
5 specification support for understanding what it means
6 for EVCC.

7 Q. Okay. Do you understand, when I say assume
8 EVCC is a constant nonground voltage throughout
9 operation of the latch, what does that mean about EVCC
10 according to your understanding of claim 14?

11 MR. JONES: Objection to form.

12 THE WITNESS: It means to me that you're trying
13 to add to the specification.

14 BY MR. ANDERSON:

15 Q. Does the '492 patent describe any voltages that
16 are constant nonground voltages that are provided
17 throughout operation of the latch?

18 A. Yes. In column 4, line 66 through column 5,
19 line 7 describes VINT, and it only describes VINT as a
20 constant voltage throughout the operation.

21 Q. And how is VINT generated in the context of
22 what the '492 patent describes in column 4, line 66
23 through column 5, line 7?

24 A. The '492 patent in column 4, line 66 through
25 5:7 describes a -- at least one generator used to

1 generate VINT.

2 Q. Can that generator be the generator in Figure 4
3 of the '492 patent?

4 A. Again, for a specific design that, you know,
5 outside the scope of the -- of any claim analysis,
6 whether a specific internal voltage generator is
7 appropriate for a specific design, we'd have to look at
8 the design to understand that.

9 Q. Can the generator that's used to generate VINT
10 that is a constant value throughout operation of the
11 integrated circuit be realized with the circuit shown in
12 Figure 4?

13 A. That's unclear.

14 Q. What would you need to know to make it clear
15 beyond what's shown in Figure 4?

16 A. A design of the product.

17 Q. The entirety of the product?

18 A. Well, minimally the power aspects of the
19 product.

20 Q. And what aspects of the power aspects of the
21 product would you need to know in order to determine
22 whether or not the VINT signal in Figure 4 could be a
23 constant value throughout operation of the latch?

24 A. Your earlier question was whether it was an
25 appropriate design.

1 So are you changing the question, or are you
2 asking whether it is -- whether Figure 4 corresponds to
3 some language?

4 Q. Beyond what's shown in Figure 4 of the '492
5 patent, what would you need to know in order to
6 determine whether the VINT signal generated by Figure 4
7 could constitute a constant nonground voltage throughout
8 operation of the latch?

9 A. Regardless of Figure 4, the determination of
10 whether VINT corresponds a constant nonground voltage
11 throughout the operation of the latch is analyzed based
12 on checking its conformance to the language in column 4,
13 line 66 through column 5, line 7.

14 Q. And how would you go about doing that? How
15 would you determine whether or not it conforms to the
16 language in column 4, line 66 through column 5, line 7?

17 A. I would look at that language and determine
18 whether the device under scrutiny meets the descriptive
19 elements of the -- of VINT.

20 Q. And what are the descriptive elements that you
21 would be looking for?

22 A. That at least one generator 213 is enabled
23 throughout circuit operation to power circuits that are
24 never disabled. If that condition is met, then VINT is
25 a constant voltage throughout the operation.

1 Q. So if the EVCC signal in Figure 4 is provided
2 by a generator that is enabled throughout circuit
3 operation to power circuits that are never disabled, is
4 the VINT signal 212 in Figure 4 also a voltage that is
5 constant throughout operation of the latch?

6 MR. JONES: Objection to form.

7 THE WITNESS: Again, the '492 specification
8 only speaks to VINT and a property that it must meet in
9 order to be a constant value throughout the operation of
10 the integrated circuit. And I've stated what that
11 limitation is, that at least when generator 213 is
12 enabled throughout circuit operation there is no
13 discussion here about EVCC.

14 BY MR. ANDERSON:

15 Q. I -- that's why I provided the context for EVCC
16 in the question because there isn't specific context as
17 to what EVCC is in the '492 specification other than an
18 external power supply voltage; correct?

19 A. I'm sorry. Could you rephrase that question?

20 Q. Is there any context for the EVCC signal in the
21 '492 patent beyond the fact that it describes it as an
22 external power supply voltage?

23 A. Well, I could search the entire patent for --
24 to see if there's any other descriptions. I think we've
25 already established based on an earlier question that

1 the column 3 language defines the external power supply
2 voltage EVCC.

3 Q. Do you understand that to be a power supply
4 rail as you use that term in your declarations?

5 A. Maybe you can point to the exact location in my
6 declaration where I'm using the term "rail."

7 Q. We'll get there. Let's go back to claim 14.

8 Does Figure 2A disclose a second terminal for
9 receiving a voltage in the context of claim 14?

10 A. The description of Figure 2A outside of the
11 context of any claims describes the ground terminal as
12 the second terminal.

13 Q. Does Figure 2A show an inverter having an input
14 connected to the terminal T1 and an output connected to
15 the control terminal of the variable impedance path as
16 reciting in claim 14?

17 MR. JONES: Objection to form.

18 THE WITNESS: Again, outside of the scope of
19 the claims, Figure 2A is described as having the
20 inverter 120, and the inverter 120's input is connected
21 to out in Figure 2A, and the output is seen as the node
22 out bar.

23 BY MR. ANDERSON:

24 Q. I'm sorry. You said outside the scope of the
25 claims.

1 What is causing you to put that caveat on your
2 answer?

3 A. Because figures are not claims.

4 Q. But is it your understanding that claims recite
5 structural limitations that define the scope of the
6 invention?

7 A. I understand that the scope --

8 MR. JONES: Objection to form.

9 THE WITNESS: I understand that the scope of
10 the invention is written in the claims.

11 BY MR. ANDERSON:

12 Q. So when your previous answer regarding the
13 inverter 120 in Figure 2A, are you saying that Figure 2A
14 does not disclose the inverter claimed in claim 14?

15 A. I'm saying that Figure 2 is a figure, and if
16 there is a specific system that we want to analyze for
17 infringement or for practice of claim 14, then we have
18 to look at that system.

19 Q. Do you need to understand the entirety of a
20 system that includes the programmable latch of claim 14
21 in order to understand the scope of claim 14?

22 A. I think you need to understand the entire
23 system in order to determine whether a limitation of
24 claim 14 is met.

25 Q. So you can't determine whether Figure 2A

1 discloses the inverter claimed in claim 14 just looking
2 at Figure 2A?

3 A. Again, the inverter in claim 14 has elements
4 associated with it. The limitation is -- goes on for
5 several lines. It's inappropriate to describe a figure
6 as corresponding to a claim.

7 Q. Why is that inappropriate?

8 A. Because the specification contains additional
9 information.

10 Q. And would that information help support the
11 mapping of various elements in Figure 2A to structural
12 limitations in the claim?

13 A. Mapping elements to a claim would be done as
14 part of an infringement analysis.

15 Q. Do you understand that figure -- or that the
16 '492 patent needs to provide a description sufficient to
17 support the claims that are included in the '492 patent?

18 A. I understand that the description must support
19 the claims.

20 Q. Can you show me where the inverter that's
21 recited in claim 14 is described in the '492 patent?

22 A. I'm scanning the specification for the language
23 that includes the complete language of the last
24 limitation of claim 14 with the pull-up and pull-down
25 devices where at least one of them is connected. If

1 you've already identified that, I'd be happy to take
2 your point; otherwise I'm going to answer the question
3 by continuing to scan for that language.

4 Q. It's not a long patent. Please go ahead and
5 look for it.

6 A. I'm going to look from the back because I know
7 it's -- I'm just skimming over it. I'm looking for a
8 reference to inverter 120. Okay. Here we go. This is
9 column 3, line 24 through 32.

10 Q. And the passage you just referenced is
11 describing Figure 2A; correct?

12 A. Yes. It's describing Figure 2A.

13 Q. So based on the description in the '492 patent
14 at column 3, lines 24 to 26, does Figure 2A show an
15 inverter as recited in claim 14?

16 A. So the inverter of claim 14, if we take just
17 that limitation, an inverter having an output connected
18 to the terminal T1, et cetera, also requires that the
19 output control a variable impedance path, so we need to
20 find support language for the various -- for the
21 variable impedance path as well.

22 Q. Is there a variable impedance path shown in
23 Figure 2A of the '492 patent?

24 A. In Figure 2A there is a variable impedance
25 path, yes.

1 Q. And what is the variable impedance path that's
2 recited in claim 14 in Figure 2A of the '492 patent?

3 A. The variable impedance path of Figure 2A with
4 respect only to Figure 2A is the NMOS transistor 110.

5 Q. So in limiting it to only being in the context
6 of Figure 2A, are you saying that the transistor 110
7 does not constitute a variable impedance electrical path
8 as that is recited in claim 14 of the '492 patent?

9 A. I'm saying that determining whether the
10 limitation of claim 14 met is an infringement analysis
11 that involves looking at the device.

12 Q. Where is the support in the '492 patent for the
13 variable impedance electrical path that's recited in
14 claim 14 of the '492 patent?

15 A. I'm searching for the term variable impedance,
16 but I know it's used to refer to element 110.

17 Q. Element 110 in Figure 2A?

18 A. Element 110 in Figure 2A is referred to as a
19 variable impedance path.

20 Q. And in claim 14, the variable impedance
21 electrical path is connected between the terminal T1 and
22 a second terminal.

23 What do you understand the second terminal to
24 be in the context of claim 14?

25 A. Claim 14 simply describes the second terminal

1 receiving a voltage, presumably distinguishing it from
2 the first terminal.

3 Q. Where is the support in the '492 patent for a
4 second terminal that receives a voltage that's different
5 than the voltage that's received on the first terminal?

6 A. Let me preface my answer by saying I've said
7 that the first -- the second terminal was distinct from
8 the first terminal. I did not say the first voltage was
9 distinct from the second voltage. Maybe you'd like to
10 rephrase the question with that understanding.

11 Q. Is there support in Figure 2A of the '492
12 patent for the second terminal recited in claim 14?

13 A. I believe there is, and I'm going to ask you to
14 confirm that you would like me to search for it before I
15 start.

16 Q. Please tell me what you think in Figure 2A that
17 supports the recited second terminal for receiving a
18 voltage in claim 14.

19 A. Again, I can search for the description of
20 Figure 2 and find a description of the second terminal
21 if that's what you'd like me to do. That discussion
22 will be limited to Figure 2- -- 2A.

23 Q. Where is a second terminal for receiving a
24 voltage as recited in claim 14 disclosed in the '492
25 patent?

1 A. So the Figure 2A description actually describes
2 a ground terminal. I am searching for whether the
3 Figure 2A description uses the term "second terminal."
4 I don't believe it does.

5 Q. So does Figure 2A disclose the claim second
6 terminal recited in claim 14? I think that's a
7 yes-or-no question. Does Figure 2A disclose the second
8 terminal recited in claim 14?

9 A. Again, claim 14 stands on its own. The Figure
10 2A has a terminal VINT and a terminal ground, and they
11 are described in the specification with reference to
12 Figure 2A.

13 Q. So does Figure 2A disclose the second terminal
14 recited in claim 14 of the '492 patent? When I asked
15 you for support where the second terminal was, you
16 referred me to the ground terminal in Figure 2A. I
17 assume that by doing so, you meant to indicate that the
18 ground terminal in Figure 2A would correspond to the
19 second terminal even though it's not described as a
20 second terminal in the specification.

21 Does the ground terminal in Figure 2A
22 correspond to a second terminal for receiving a voltage
23 in claim 14 of the '492 patent?

24 A. Again, I think claim 14 stands on its own, and
25 figure -- Figure 2A is described in the specification.

1 So whether or not a specific entity has a first terminal
2 and a second terminal, that's up to the entity.

3 Q. Does Figure 2A have a second terminal for
4 receiving a voltage as recited in claim 14? You pointed
5 me to the ground terminal before. Is that a second
6 terminal for receiving a voltage as that term is used in
7 claim 14?

8 A. Again, claim 14 has many limitations. If we
9 limit ourselves only to the description from Figure 2, I
10 think it's -- it would be correct to say that the VINT
11 terminal could be considered a first terminal and that
12 the ground terminal can be considered a second terminal.

13 Q. So if we limit ourselves to the description of
14 Figure 2A, can we find all of the elements of claim 14
15 in Figure 2A?

16 MR. JONES: Objection to form. Asked and
17 answered.

18 THE WITNESS: I think we already covered that
19 the very first limitation of claim 14 requires more
20 information.

21 BY MR. ANDERSON:

22 Q. Is the only limitation that's in claim 14 that
23 requires looking outside of Figure 2A the limitation
24 that is a first terminal for receiving a constant
25 nonground voltage throughout operation of the latch?

1 Let me rephrase.

2 Can you determine that Figure 2A discloses all
3 of the limitations of claim 14 on its face with the
4 exception of the first terminal for receiving a
5 nonground voltage throughout operation of the latch?

6 A. Again, whether a specific element meets --
7 whether a specific design meets claim 14 is, I think, an
8 infringement opinion, and I think I've described at
9 least that the -- that the aspect throughout operation
10 of the latch which is present in claim 14 would be
11 something that requires an understanding of the
12 operation.

13 Q. So Figure 2A shows a second terminal for
14 receiving a voltage in the ground terminal; correct?

15 A. I think the --

16 MR. JONES: Objection. Asked and answered.

17 THE WITNESS: Again, I think the description of
18 Figure A describes a -- one voltage provided at VINT,
19 and it describes -- it describes the ground terminal
20 which I can search for if you desire.

21 BY MR. ANDERSON:

22 Q. And you indicated earlier that the terminal OUT
23 in Figure 2A corresponds to the terminal T1 as that term
24 is used in the claims of the '492 patent; correct?

25 A. I believe the description is clear on that

1 aspect that a -- the terminal T1 is in the claims
2 defined as an element that exists between the
3 programmable element and the variable impedance device.

4 Q. And that's consistent with the out terminal in
5 Figure 2A that's between the fuse F1 and the variable
6 impedance path 110; correct?

7 A. Yeah. In Figure 2A the out terminal is located
8 between the fuse F1 and the variable impedance device
9 110.

10 Q. Do you believe that mapping a claim to a figure
11 in the patent application that includes the claim is an
12 infringement analysis?

13 MR. JONES: Objection to form.

14 THE WITNESS: I believe that asking whether
15 something meets a particular claim is an infringement
16 analysis.

17 BY MR. ANDERSON:

18 Q. So asking you whether or not Figure 2A shows an
19 embodiment that includes all of the elements of
20 figure -- or of claim 14 is an infringement analysis in
21 your mind?

22 A. I'm sorry. Could you rephrase that?

23 Q. Asking you whether the circuit shown in Figure
24 2A includes all of the elements of claim 14 is an
25 infringement analysis in your mind.

1 Is that correct?

2 A. Asking for specification support of the
3 elements of claim 14 is not an infringement analysis.

4 Q. Okay. Is it your understanding that the
5 figures of the '492 patent are part of the
6 specification?

7 A. Yes. I would consider them part of the
8 specification.

9 Q. So when you look to Figure 2A, you're able to
10 rely on connections shown in Figure 2A to provide
11 support for those connections in the claims; correct?

12 A. I look to the specification's description of
13 the figure to understand what the figure means.

14 Q. So if the specification didn't say that the
15 input to the inverter 120 was connected to the terminal
16 OUT in Figure 2A, could the '492 patent support a claim
17 that recites that connection?

18 A. Again, I'm not a lawyer.

19 MR. JONES: Objection to form.

20 THE WITNESS: My understanding is that the
21 specification must provide support for the claims.

22 BY MR. ANDERSON:

23 Q. And the figures are part of the specification;
24 correct?

25 A. Figures are part of the specification.

1 Q. Is there any support for the first terminal for
2 receiving a constant nonground voltage throughout
3 operation of the latch in the '492 patent outside of
4 column 4, line 66 through column 5, line 7?

5 A. It's my belief that the only place where
6 throughout the operation is used and defined is in that
7 section of the specification. So specifically column 4,
8 line 66 through column 5, line 7. I am willing to
9 conduct a search if that's what you desire, but it's my
10 understanding that that's the only place it's mentioned.

11 MR. ANDERSON: We've been going quite a while.
12 It's about noon.

13 Do you want to take a break?

14 MR. JONES: Sure. Let's go off the record.

15 (Luncheon recess taken from 12:01 p.m. to
16 12:51 p.m.)

17 --000--
18
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A F T E R N O O N P R O C E E D I N G S :

BY MR. ANDERSON:

Q. So prior to the break, we were talking about Figure 2A a bit, and one of the things that we discussed was how the diode 234 allows the voltage on the node out to be dissipated if there's more voltage on node out than there is on VINT.

Do you recall that conversation?

A. It wasn't immediately prior to the break, but yes, we had that discussion.

Q. Okay. So the diode provides a mechanism for dissipating charge on node out in the embodiment shown in Figure 2A; correct?

A. So you switched to dissipating charge from dissipating voltage, so I'm going to ask you to clarify if that was intentional.

Q. It wasn't intentional. But would dissipating charge on the node out necessarily dissipate the voltage at node out as well?

A. So the way that a diode dissipates charge is that charge will leak through the diode as long as the diode is conductive. The voltage will correspond to the I-V curve for that diode given the current -- the current level.

1 Q. So in the embodiment of Figure 2A, does the
2 diode 234 dissipate charge from the node out?

3 A. Yes. It will dissipate accumulated charge if
4 that charge would cause the voltage to exceed the
5 threshold voltage of the diode.

6 Q. And when it dissipates that charge, does the
7 diode 234 also dissipate the voltage at the terminal
8 OUT?

9 A. I would say as it is dissipating that charge,
10 the voltage is being lowered in correspondence to the
11 I-V curve of the diode.

12 Q. And when you say the voltage is being lowered,
13 would you understand that to be dissipating the voltage?

14 A. Yes. I think that's a fair statement.

15 Q. Okay. So in the embodiment shown in Figure 2A,
16 if we assume that the diode 234 is not present, can you
17 assume that?

18 A. Yes.

19 Q. Okay. So if that's the case and there is
20 charge at the node out, how can that charge be
21 dissipated from the node out?

22 MR. JONES: Objection to form.

23 THE WITNESS: So it sounds like you're asking
24 on an arbitrary node that has charge on it how does that
25 charge leak if -- how does that charge dissipate if

1 there is no diode? Am I understanding that correctly?

2 BY MR. ANDERSON:

3 Q. Yes. With the understanding that I'm speaking
4 specifically about the node out. So if there's charge
5 on out and the diode isn't present, how is the charge at
6 terminal OUT dissipated?

7 A. Well, speaking in general, any semiconductor
8 that has a charge node, unless that node is
9 reenforced -- so it's driven is the term I think we used
10 previously -- the charge will tend to dissipate over
11 time if there's no activity in the circuit. The
12 mechanism by which it does that is a few different ways.
13 One would be -- for instance, there's going to be
14 channel leakage through Device 110. Even though that
15 device is off, there's going to be a finite but a quite
16 high resistance in that channel simply because it is
17 made of a semiconductor material.

18 Q. Can I interrupt you briefly? I just want to
19 make sure I understand.

20 When you say channel leakage, did you mean,
21 then, leakage from the drain of Transistor 110 to the --
22 or from the source of Transistor 110 to the drain of
23 Transistor 110? Is that what you mean by the channel
24 leakage?

25 A. Well, it's an NMOS device, so I'm going to

1 refer to source as the grounded node in this case. But
2 the NMOS device functions essentially as a switch in
3 which the channel is either at high resistance or low
4 resistance depending on whether the device is on or off.
5 So even the off device will have a high but noninfinite
6 resistance, and so charge would -- or current would flow
7 from out to ground in that manner. It might take a very
8 long time, and the manner in which it does so or that it
9 does so in a way that's suitable for a specific
10 assumption is indeterminate. We would have to look at a
11 specific implementation.

12 There is also -- there is some threshold
13 leakage, so we would look at -- you might be familiar
14 with leakage current that exists in MOS devices
15 especially at lower geometries where we have leakage not
16 from source to drain or drain to source but actually
17 through the gate material. It's essentially a tunneling
18 mechanism. So there is a very small hopefully current
19 which can be sustained, which would be able to be
20 sustained from the out node, say, through the gates of
21 Inverter 210 into the substrates.

22 The exact levels depend on what the level of
23 the voltage is and also on the quality of the oxides and
24 to what extent there are trapped charges, et cetera.
25 Then we would have to look at -- we would have to look

1 at the fuse itself because even if the fuse is
2 programmed that is cut, the patent anticipates a
3 programmable device, right? So in the event that we're
4 not talking a piece of metal which has been fully cut so
5 has infinite resistance, it's possible that, for
6 instance, an electrical -- electrically programmed
7 mechanism might have simply incredibly high resistance
8 in its equivalently programmed state.

9 Then we would look at what is hanging off the
10 out terminal, whether that has potential leakage. And
11 anything else basically that is connected electrically
12 to that node we would look at sort of paths to ground or
13 paths to a grounded node. If there's a voltage, if
14 there is a current, it's simply a question of how low
15 that current is. It could be so infinitesimally small
16 that it takes forever to dissipate, or for the purposes
17 of operation it never manages to dissipate.

18 Q. So one of the means for charge dissipation at
19 out that you mentioned was if the fuse F1 is something
20 other than metal fuse and would provide some path for
21 leakage; correct?

22 A. Let me rephrase that in a way that I think
23 would be more correct.

24 Q. Okay.

25 A. If we anticipate that programming a metal fuse

1 by sublimating the metal creates an absolute open, that
2 could be considered to have infinite resistance, so very
3 incredibly high and would not dissipate charge under any
4 circumstance.

5 Other implementations of the programmable
6 device would have other construction, and so we would
7 have to look at that construction to understand if there
8 would be similar parasitic paths as I explained for the
9 other devices.

10 Q. And one of the other devices that you mentioned
11 having parasitic paths is the Transistor 110; correct?

12 A. Maybe a parasitic path is not the right term,
13 but it has a -- it has a less than infinite resistance
14 in its off state. And so even if acting as a switch, it
15 is never fully on or fully off. It's always simply very
16 low resistance or very high resistance in the case of a
17 MOSFET operated in this manner.

18 Q. So the MOSFET 110, even when it's off it still
19 provides a path from out to ground. It's just a very
20 high resistance path?

21 A. For the purposes of this patent, it doesn't
22 provide a path that dissipates the charge during ramp up
23 to prevent the node from achieving an incorrect state.
24 It will have some leakage, and whether or not that
25 leakage is sufficient to dissipate a node, well, that's

1 a time question.

2 Q. I guess, assuming that the latch in Figure 2A
3 is used in a conventional memory device at the time of
4 the '492 patent, do you have any idea as to how long it
5 would take for charge at the out node to dissipate
6 through 110?

7 A. I would have to run a spice simulation to
8 determine that. I couldn't even give you an order of
9 magnitude.

10 Q. So looking at Figure 2A and again assuming that
11 diode 234 is not present and assume that fuse 1 is
12 blown, okay, can you assume that?

13 A. Yes. And I'm going to assume that it's blown
14 in a --

15 Q. Such that it's nonconductive?

16 A. Such that it is an open nonconductive state.

17 Q. That's a fair clarification. All right. So if
18 charge is accumulated at out under those conditions,
19 would that charge dissipate from the terminal OUT over
20 time?

21 A. Dissipate -- I'm sorry. Dissipate over?

22 Q. Time. Over some length of time. It would
23 eventually dissipate; correct?

24 A. In theory if the power is applied --
25 "disapplied," so removed and we walk away, eventually

1 there should be no charges on any nodes barring trapped
2 charge on, say, Flash or EPROM cells.

3 Q. And when the charge at out dissipates, the
4 voltage at out is also going to be reduced; correct?

5 A. Well, the voltage will eventually be reduced,
6 but I should specify that it is not -- it's not kept
7 below any specific threshold or it's not -- it's not
8 reduced in any kind of a controlled manner. It's simply
9 left to dissipate over a very high resistance.

10 So I wanted to distinguish that from, say, a
11 diode removing dissipating charge wherein the voltage is
12 clamped, and it is kept within a certain range versus
13 the general leakage of a device which is simply going to
14 dissipate current through its very high but not infinite
15 resistance.

16 Q. So in the situation that we were just
17 discussing where Fuse F1 is blown such that it's an open
18 circuit and the Diode 234 is not present, is there a
19 particular mechanism included in Figure 2A that allows
20 the voltage at node out to be dissipated when power is
21 not supplied?

22 MR. JONES: Objection to form.

23 THE WITNESS: Let me -- Figure 2A and the
24 specification support for Figure 2A do not describe any
25 of those mechanisms, and I don't think the patent in

1 general describes them. I think we've talked about them
2 in general sort of in the scope of just a generic
3 semiconductor.

4 BY MR. ANDERSON:

5 Q. Could you please turn to column 2 of the '492
6 patent starting around line 26.

7 A. Okay.

8 Q. In this part of the '492 patent, it's
9 explaining that some embodiments do not have a latch
10 initialization signal; correct?

11 A. Yes. With specific reference to Figure 1, the
12 entire paragraph describes the advantage of not having
13 latch initialization signals.

14 Q. And the '492 patent refers to another patent in
15 that paragraph; correct?

16 A. It does. That would be the '107 patent.

17 Q. Have you reviewed the '107 patent?

18 A. I believe I looked at it at one point, but it's
19 not something I remember off the top of my head.

20 Q. I'm going to hand you a copy of U.S. Patent
21 5,566,107 to Gilliam.

22 A. I'd like to take a moment to just peruse it
23 quickly.

24 Q. Yep.

25 A. I have not read through the entire patent, but

1 please continue.

2 Q. Do you recall looking at this patent previously
3 while reviewing the '492 patent?

4 A. I think I looked at it early on to understand
5 there was an enabled signal.

6 Q. Could you please turn to Figure 3 of the '107
7 patent. Is it okay if I call it Gilliam?

8 A. I'm holding the '107 patent to Gilliam, so
9 until you tell me to use another document, we'll assume
10 that's . . .

11 Q. Okay, perfect. So please turn to Figure 3 of
12 Gilliam.

13 A. So I'm at Figure 3.

14 Q. And do you see the activate signal on the upper
15 left portion of Figure 3?

16 A. I see the activate bar that's labeled as 28.

17 Q. What's the significance of the bar that's over
18 the activate?

19 MR. JONES: Objection. Outside the scope of
20 the expert's declarations.

21 THE WITNESS: I would say it's -- a bar in general is
22 used in semiconductors to denote something that's active
23 low. That's -- so outside the scope of all -- you know,
24 of just patents in general, that's a nomenclature that's
25 used in the art. Whether -- I probably would want to go

1 through the specification to make sure that that's how
2 it's used here, but that's the generally understood
3 method in which it's used.

4 BY MR. ANDERSON:

5 Q. Okay. Can we look back to column 2 of the '492
6 patent. And do you see at lines 30 to 31, the '492
7 patent indicates that Gilliam "needs an external
8 'activate' signal for initialization"? Do you see that?

9 A. I see where you're reading that.

10 Q. Looking at Figure 3 of Gilliam, is the activate
11 signal shown there a latch initialization signal in the
12 context of the '492 patent?

13 MR. JONES: Objection. Outside the scope of
14 the expert's declarations.

15 THE WITNESS: Yeah. That's not something that
16 I have -- that I analyzed as part of forming my opinion.
17 I would have to do a much closer reading of the patent
18 to understand that.

19 BY MR. ANDERSON:

20 Q. So the '492 patent says Gilliam is a circuit
21 that needs an external activate signal for
22 initialization.

23 Does that suggest to a person of ordinary skill
24 in the art that the activate signal would be an
25 initialization signal?

1 MR. JONES: Same objection.

2 THE WITNESS: I think it means exactly what it
3 says, which is that it needs the external activation
4 signal for initialization.

5 BY MR. ANDERSON:

6 Q. What is a latch initialization signal in the
7 context of the '492 patent?

8 A. It would be a signal that initializes a latch.

9 Q. Outside of Gilliam, does the '492 patent give
10 any examples of latch initialization signals?

11 A. It's my understanding that the '492 patent
12 describes the lack of requiring activation signals as an
13 advantage. Whether it mentions that repeatedly outside
14 of column 2:22 through -32, I can't be sure without
15 scanning the document.

16 Q. Is it your understanding that all of the
17 embodiments in the '492 patent exclude latch
18 initialization signals?

19 MR. JONES: Objection. Outside the scope of
20 the expert's declarations.

21 THE WITNESS: So if you would like to point me
22 to a particular claim, I can tell you whether or not an
23 activation signal is a requirement of that claim.

24 BY MR. ANDERSON:

25 Q. Turn back to Figure 3 of Gilliam.

1 A. I'm there.

2 Q. Do you see that the activate signal 28 is
3 provided to a Transistor 60?

4 A. Yes, I do.

5 Q. And I'll represent to you that Transistor 60 is
6 a PMOS transistor.

7 Are you okay with that?

8 MR. JONES: Objection to form.

9 THE WITNESS: I'm -- I would want to read
10 through Gilliam to make sure that that is correct.

11 BY MR. ANDERSON:

12 Q. Assume it's a PMOS transistor, okay?

13 A. Again, if I'm going to be asked to draw
14 conclusions based on that, then I would want to go
15 through Gilliam to confirm. Perhaps you can point me to
16 the section of Gilliam that describes Transistor 60.

17 Q. If you go to the bottom of column 3 at Gilliam,
18 at line 62 it says, "Circuit branch 58 includes a switch
19 60 which in one aspect of the invention is a P-channel
20 transistor having its source coupled to power supply
21 terminal 52, its gate coupled to control terminal 54,
22 and its drain coupled to a first input of a fuse circuit
23 62."

24 A. I see where you're reading that.

25 Q. Okay. So switch 60 is, in this example, a

1 P-channel transistor; correct?

2 MR. JONES: Objection. Outside of the scope of
3 the expert's declarations.

4 THE WITNESS: Again, if you're asking me to
5 confirm any element of Gilliam, I am going to want to
6 reread this reference especially in light of the
7 elements of '492 that you're linking it to. I
8 understand my review of this reference was strictly to
9 understand that it had an activate signal.

10 BY MR. ANDERSON:

11 Q. Okay. So you haven't formed an opinion as to
12 whether or not the activate signal in Figure 3 of
13 Gilliam would constitute a latch initialization signal
14 as that term is used in the '492 patent; correct?

15 A. I understand that the patent authors of the
16 '492 refer to Gilliam containing an external activate
17 signal.

18 Q. So you haven't formed an opinion as to whether
19 the activate signal in Figure 3 of Gilliam would
20 constitute a latch initialization signal as that term is
21 used in the '492 patent; correct?

22 A. The mention of Gilliam in the '492 patent says
23 that Gilliam describes a circuit that needs an external
24 activation signal for initialization. That's the extent
25 of the description of Gilliam, and it confirms my

1 understanding that Gilliam requires an external activate
2 signal for initialization.

3 Q. So I think my question is simpler. And I'm
4 just asking if you, yourself, have formed an opinion
5 based on what you've read in the '492 patent and what
6 you see in Figure 3 of Gilliam. Have you formed an
7 opinion as to whether the activate signal shown in
8 Figure 3 of Gilliam is a latch initialization signal as
9 that term is used in the '492 patent? It's a yes or no.

10 A. I have not reached any opinions in this
11 declaration regarding whether or not the signal in
12 Gilliam is a latch initialization signal.

13 Q. Have you formed any opinions that are not
14 reflected in your declaration in that respect?

15 A. I have not been asked to provide such opinions.

16 Q. I'm asking if you've formed such an opinion.

17 A. Not at this moment.

18 Q. Can you please turn to Figure 3 of the '492
19 patent.

20 A. Okay. I'm at Figure 3.

21 Q. And do you see the enable signal EN that is
22 provided to the transistor 330 on the left-hand side of
23 Figure 3?

24 A. It's provided to multiple elements, but it is
25 provided to transistor 330.

1 Q. Is it your understanding that the enable signal
2 EN has to be asserted high in order for the VINT signal
3 in Figure 3 to be a positive nonground voltage?

4 A. Well, in order for the comparator that is
5 formed by the differential pair 322 and 326, the enable
6 signal would have to turn on transistor 330. The exact
7 voltage necessary to do so I think is subject to
8 implementation.

9 Q. So if you look at column 4, line 37 of the '492
10 patent.

11 A. I'm sorry. Which line in column 4?

12 Q. Sure. It's column 4, line 37. And there it
13 says when EN is low (ground), the VINT terminal 22 is at
14 ground.

15 When EN is at EVCC, the terminal 212 provide
16 the voltage between ground and EVCC.

17 Do you see that?

18 A. I see where you're reading that, yes.

19 Q. Is the EN signal in Figure 3 a latch
20 initialization signal?

21 A. Could you point to the description of the latch
22 initialization signal in the patent?

23 Q. I think earlier you indicated it was a signal
24 that was used to initialize the circuit where you just
25 stated the latch. Is that not how you characterized it

1 before?

2 A. I think I said that it is a signal that
3 initializes a latch.

4 Q. Okay. So is the EN signal in Figure 3 a signal
5 that would initialize the latch?

6 MR. JONES: Objection to form.

7 THE WITNESS: I think that's indeterminate.

8 BY MR. ANDERSON:

9 Q. Why is it indeterminate?

10 A. Because Figure 3 is a voltage generator to
11 generate VINT. So as to whether a latch is initialized
12 or not, that could be a separate matter.

13 Q. If the VINT signal from Figure 3 is provided on
14 the terminal 212 in Figure 2A, is the EN signal a latch
15 initialization signal?

16 MR. JONES: Objection to form.

17 THE WITNESS: I'm not really sure how to
18 interpret that. I think the -- if the enable signal is
19 high, then VINT will be eventually driven to its
20 non-zero state. If VINT is at a non-zero state, the
21 circuit in Figure 2A is powered. I don't really know
22 what it means to impute initialization from that.

23 BY MR. ANDERSON:

24 Q. Does the state of the fuse F1 in Figure 2A
25 impact -- strike that.

1 Can the state of the fuse F1 in Figure 2A pull
2 the terminal OUT high if VINT is at ground?

3 MR. JONES: Objection to form.

4 THE WITNESS: The fuse F1, if it is not blown,
5 means that out is at the same potential at VINT.

6 BY MR. ANDERSON:

7 Q. So until the enable signal goes high, the
8 terminal OUT cannot be pulled high assuming the VINT
9 signal in Figure 2A is generated by the circuit in
10 Figure 3; correct?

11 A. Well, I think we've already discussed the
12 possibility of the out terminal having a voltage higher
13 than VINT.

14 Q. If the fuse is not blown, the output terminal
15 can have a voltage that's higher than VINT?

16 A. No. That was not my testimony. If the fuse is
17 not blown, then the output voltage equals whatever VINT
18 is.

19 Q. So if the voltage generator at Figure 3
20 provides VINT in Figure 2A and the fuse is not blown,
21 the terminal OUT can't be high unless EN is high;
22 correct?

23 A. That's not entirely true.

24 Q. Does EN in Figure 3 control whether or not VINT
25 in Figure 2A is high?

1 MR. JONES: Objection to form.

2 THE WITNESS: The enable signal is used to
3 charge the VINT node through the transistor 310. I can
4 at that point momentarily disable EN and VINT will still
5 have a value.

6 BY MR. ANDERSON:

7 Q. Doesn't that contradict what the '492 patent
8 says at column 4 where it says when EN is low, the VINT
9 terminal 212 is at ground?

10 A. And that's correct in a steady state
11 description. Your question related to is there any
12 situation in which the enable signal was low and there
13 was voltage on VINT, and I described the transient
14 situation where that could occur. It's equivalent to
15 your laptop has a battery and has a light. Even though
16 you're turning off the switch, there's still some
17 capacitance there, so it takes a while for the charge to
18 bleed off.

19 Q. Have you formed an opinion as to whether or not
20 the EN signal in Figure 3 is a latch initialization
21 signal?

22 A. Right now I have not formed such an opinion.

23 Q. Can you please turn to Figure 5 of the '492
24 patent?

25 A. Yes. Figure 5.

1 Q. EVCC in Figure 5 is an external power supply
2 voltage; correct?

3 A. That's the way it's described in the
4 specification, yes.

5 Q. And based on what's shown in Figure 5, you
6 cannot determine whether or not EVCC is a constant
7 nonground voltage during operation of the circuit shown
8 in Figure 5; can you?

9 A. I cannot determine whether the VINT voltage
10 meets the limitation of -- throughout operation of the
11 latch as properly construed, meaning at all times during
12 circuit operation without being disabled.

13 Q. My question was actually about EVCC. Based on
14 what's shown in Figure 5, can you tell me whether or not
15 EVCC is a constant nonground voltage during operation of
16 the integrated circuit that includes the circuitry shown
17 in Figure 5?

18 A. The patent does not describe the properties
19 attributed to EVCC under such conditions. It is silent
20 on the matter.

21 Q. And is it your understanding that the VINT
22 generator in Figure 5 can be used to generate the VINT
23 signal that's used in conjunction with the latch shown
24 in Figure 2A?

25 A. I think it's correct to say that one should not

1 assume that each particular embodiment of a VINT
2 generator could be applied to every circumstance of a
3 VINT using circuit. There may be circumstances or
4 conditions regarding the design that would favor some
5 designs or preclude others. There may be embodiments
6 where there are no restrictions, but I don't think a
7 blanket statement is fair.

8 Q. Figure 2, could you please look at Figure 2 of
9 the '492 patent.

10 A. Figure 2A.

11 Q. 2A. Thank you.

12 A. 2A, yes.

13 Q. I apologize. Do you see that it shows the VINT
14 generator 213?

15 A. Yes.

16 Q. Could you please turn to column 5 of the '492
17 patent at line 17.

18 Do you see there the '492 patent says that
19 "Figures 4 and 5 show other embodiments of a VINT
20 generator 213"?

21 A. I see where you read -- that's line 17 through
22 21 or -2?

23 Q. 17 to 18, I think --

24 A. Yes.

25 Q. -- says that.

1 A. Yes.

2 Q. So the '492 patent discloses that Figure 5
3 provides an embodiment of the VINT generator 213 where
4 the VINT generator 213 is shown in Figure 2A; correct?

5 A. I think it shows the -- one minute. I have
6 these out of order now. Let me assemble this.

7 I think Figures 4 and 5 show -- has stated
8 specification alternative VINT generators. And in some
9 embodiments they would be suitable for application in --
10 with 2A. Whether they are for a specific embodiment,
11 again, that's a generalization that I don't think is
12 appropriate.

13 Q. So Figure 3 is one example of a VINT generator
14 213; correct?

15 A. Yes, it is.

16 Q. And Figures 4 and 5 are alternative VINT
17 generators disclosed in the '492 patent; correct?

18 A. Yes, and so described in the passage that you
19 previously cited.

20 Q. So you would agree, then, that the '492 patent
21 discloses an embodiment where the VINT generators in
22 Figures 4 and 5 are used in conjunction with the
23 programmable latch shown in Figure 2A; correct?

24 A. Well, the programmable latch in 2A is itself an
25 embodiment. We have Figure 6. We have Figure 7, and we

1 have Figure 8. So there are embodiments in which each
2 of those latches are appropriate. And there are
3 embodies -- embodiments where each of those voltage VINT
4 generators are appropriate.

5 You seem to be asking whether a specific
6 internal voltage generator is usable with a specific
7 latch, and I would say, again, that's a generalization
8 that should not be made. You would have to look at the
9 design. There may be considerations for why you would
10 choose one embodiment over another.

11 Q. So would you agree that '492 patent discloses
12 that the VINT generators, the Figures 4 and 5 can be
13 used as the VINT generator 213 in Figure 2A?

14 A. I would agree that they -- that the '492 patent
15 discloses various forms of the VINT generator and which
16 particular form is used in one particular
17 implementation, physical implementation of a circuit
18 similar to Figure 2A would be a design choice.

19 Q. So when the '492 patent says that Figures 4 and
20 5 show other embodiments of a VINT generator 213, do you
21 think it's referring to a different VINT generator 213
22 than that depicted in Figure 2A?

23 A. That's not what I said. I think it's referring
24 to one and potentially more of the example 213 internals
25 described in Figures 3, 4, 5 -- 3 and 4 and 5.

1 Q. So I want to make sure I'm clear.

2 In Figure 2A there's a VINT generator 213;
3 correct?

4 A. Yes.

5 Q. And the '492 patent teaches that that VINT
6 generator 213 can be implemented using the circuits
7 shown in each of Figures 3, 4 and 5; correct?

8 A. I wouldn't say that it shows each of them.
9 It's -- I think that it shows that it could be
10 implemented by at least one of them for a specific
11 instance.

12 Q. Which one?

13 A. Well, that would be the design choice.

14 Q. Well, if you can choose, doesn't that mean you
15 can implement any of them?

16 A. A design choice that conforms to the
17 requirements of the design.

18 Q. Does the '492 patent provide any indications as
19 to why you would make design choices between Figures 3,
20 4 and 5?

21 A. I think this knowledge of one of ordinary skill
22 in the art leads one to understand why one would choose
23 between 3, 4 and 5 in terms of the VINT generators.

24 Q. And a person of ordinary skill in the art
25 reading the '492 patent would understand that when they

1 implemented the circuit shown in Figure 2A, they could
2 choose any of the VINT generators in Figures 3, 4 and 5;
3 isn't that correct?

4 A. As a designer, that to me is not correct. When
5 I look at Figure 2A, if I were to implement Figure 2A, I
6 understand that there is a VINT generator as necessary
7 component. So element 213. Whether my specific
8 implementation would be best served as the internals of
9 that VINT generator I think is an open design choice.

10 Q. So do you agree that the '492 patent discloses
11 that the VINT signal in Figure 2A can be provided by the
12 circuits in each of Figures 4 and 5?

13 A. I think for a specific implementation of Figure
14 2A, the '492 patent is suggesting three example internal
15 voltage generators in Figures 3, 4 and 5. And if I'm
16 not mistaken, it contains a reservation towards the end
17 that there might be other internal voltage generators in
18 the art or yet to be -- yet to be discovered.

19 So again, I do not believe that Figure 2A
20 teaches a specific one of implementations of VINT
21 generator. It's a figure, and we can tell by the number
22 that it's referring to the same concept, the VINT
23 generator.

24 Q. So yes or no? Do you agree that the '492
25 patent discloses that the VINT signal in Figure 2A can

1 be provided by the circuit of Figures -- Figure 4 or
2 Figure 5?

3 A. I think that's a complicated question, and the
4 answer is that Figure 2A does not suggest which
5 particular VINT generator implementation, be it
6 Figures 3, 4, 5 or other implementation, is appropriate
7 for any particular design.

8 Q. I understand that. But if you look at
9 Figure 4, it shows a VINT generator 213 that produces a
10 VINT signal 212; correct?

11 A. That is correct.

12 Q. Would a person of ordinary skill in the art
13 understand that they can take the VINT generator shown
14 in Figure 4 and put it into the circuit of Figure 2A
15 where the VINT generator 213 is shown?

16 A. Absolutely not without considering the
17 design -- the design requirements.

18 Q. Would they be capable of putting that circuit
19 in Figure 4 into the circuit of Figure 2A if they
20 decided that was a good idea?

21 A. If they had done the evaluation to determine
22 that it was the appropriate design, then there's nothing
23 that restricts Figure 4 from being the choice of VINT
24 generator of a particular design.

25 Q. Okay. So do you agree that the '492 patent

1 discloses that the VINT signal in Figure 2A can be
2 provided by the circuits shown in Figures 4 and 5? Yes
3 or no?

4 A. I'm going to ask you to repeat the question and
5 confirm that you said can be provided, not are provided.

6 Q. Do you agree that the '492 patent discloses
7 that the VINT signal in Figure 2A can be provided by the
8 circuits shown in Figures 4 and 5?

9 A. The '492 patent provides example VINT
10 generators, Figures 3, 4, and 5 and the yet to be
11 discovered versions. But whether the specific
12 implementation can be used in a specific implementation
13 of the circuit of Figure 2A is a design decision.

14 Q. So you can't answer "yes" or "no" whether or
15 not the '492 patent discloses that the VINT generator
16 213 in Figure 2A can be implemented using the circuits
17 shown in Figures 4 and 5?

18 A. The '492 patent does not describe an
19 implementation which under each and every circumstance
20 can take one particular VINT generator and apply to
21 every -- every single example of a latch. These are
22 examples of a VINT generator, and these are different
23 constructions of a latch.

24 And as I've said repeatedly now, the choice and
25 the determination of which VINT generator to use in a

1 design must take into consideration the design goals and
2 the design constraints. And it is not proper to say
3 that a specific design -- a specific VINT generator can
4 always be used with a specific latch.

5 Q. So it's not proper, then, that the '492 patent
6 labeled the circuit in Figure 4 213 and also labeled the
7 VINT generator in Figure 2A 213? Is that improper?

8 A. No. That is entirely proper because it is
9 separating the two and not attempting to create a link.
10 There is no diagram in the '492 patent that shows the
11 internals of the VINT generator and the internals of the
12 latch in one diagram together and suggesting that as a
13 particular embodiment.

14 Q. Okay. So let's assume that the VINT signal in
15 Figure 2A was provided by the circuit of Figure 4. Can
16 you make that assumption?

17 A. I think that's a viable assumption, yes.

18 Q. In such a case, would the VINT signal
19 constitute the claim first terminal in Claim 14?

20 MR. JONES: Objection to form.

21 THE WITNESS: So outside of the claims, if
22 we're looking at the first terminal as it corresponds
23 with the description in Figure 2, then VINT is described
24 as that first terminal.

25 ///

1 BY MR. ANDERSON:

2 Q. I actually was very specific to be in the
3 context of Claim 14 as you understand that claim should
4 be construed. If VINT is generated according to the
5 circuit of Figure 4, does VINT constitute the claim
6 first terminal in Figure 2A?

7 A. I'm sorry. Maybe --

8 MR. JONES: Objection to form.

9 THE WITNESS: Maybe you can clarify. It sounds
10 like, again, you're asking whether something is
11 practiced by Claim 14.

12 BY MR. ANDERSON:

13 Q. If VINT is generated by the circuits shown in
14 Figure 4, okay? And that's the VINT that's in
15 Figure 2A, okay?

16 A. Okay.

17 Q. In that case does VINT constitute the claim
18 first terminal in Claim 14 in the context of the claim?
19 Would it satisfy that claim limitation if it was
20 generated in that manner?

21 MR. JONES: Objection to form.

22 THE WITNESS: So if we were presupposing that
23 the limitation a first terminal is met, I don't see
24 anything in Claim 14 that describes the generation of
25 the constant nonground voltage outside the requirement

1 that it be throughout operation of the latch.

2 BY MR. ANDERSON:

3 Q. So if VINT was generated using the VINT
4 generator shown in Figure 4, would it satisfy that
5 limitation?

6 A. Well, whether something satisfies the
7 limitation of Claim 14 is -- as long as the first
8 terminal for receiving a constant nonground voltage
9 throughout operation of the latch is satisfied, I don't
10 see any further limitations in Claim 14 regarding the
11 generation of said constant nonground voltage applied to
12 the first terminal.

13 Q. Is node 212 in Figure 2A a terminal as that
14 term is used in Claim 14?

15 MR. JONES: Objection to form.

16 THE WITNESS: Well, we had earlier agreed to
17 use "terminal" and "node" interchangeably. Are -- do
18 you wish to redefine "terminal"?

19 BY MR. ANDERSON:

20 Q. I just want to confirm that in the context of
21 Claim 14, what's shown as VINT 212 in Figure 2A would
22 constitute a terminal.

23 MR. JONES: Objection to form and outside the
24 scope of the expert's declarations.

25 THE WITNESS: I'm not really -- I'm not really

1 sure I understand the question. Maybe I can -- can you
2 rephrase it another way?

3 BY MR. ANDERSON:

4 Q. Is there anything special about the word
5 "terminal" that suggests something other than what is
6 shown as VINT 212 in Figure 2A?

7 MR. JONES: Same objections.

8 THE WITNESS: So to the extent Claim 14
9 requires a first terminal, if we go to the specification
10 and look for support for that first terminal and we look
11 for the description of the VINT terminal, there is
12 correspondence there. I'm not sure how to answer the
13 rest of your question.

14 BY MR. ANDERSON:

15 Q. What I'm trying to do is clarify your use of
16 the word "terminal" and whether or not terminal has any
17 special meaning in the context of the claims.

18 Is a terminal something that's an end point
19 necessarily?

20 MR. JONES: Objection to form and outside the
21 scope of the expert's declarations.

22 THE WITNESS: So terminal is not a construed
23 term. When I look at first -- when I look at Claim 14,
24 I see that there are two terminals, a first terminal and
25 a second terminal and then followed by a third terminal

1 T1. The claim specifies the specialness or extra
2 material that are required of those terminals.

3 BY MR. ANDERSON:

4 Q. Okay. So you wouldn't disagree if VINT in
5 Figure 2A is characterized as a terminal?

6 MR. JONES: Same objections.

7 THE WITNESS: I think we've already sort of
8 agreed that a terminal and a node are interchangeable
9 for the purpose of general discussions of
10 semiconductors.

11 BY MR. ANDERSON:

12 Q. Is VINT one of those?

13 A. VINT is a connection point of devices. In a
14 circuit net list it would be called a node. If it is
15 named, it can be called a terminal. I think those are
16 fair descriptions of VINT.

17 Q. So VINT is a terminal based on your
18 understanding of the word "terminal" in the context of
19 the claims?

20 MR. JONES: Same objections. Asked and
21 answered.

22 THE WITNESS: Again, our initial discussion of
23 terminal and node was in the general parlance of
24 semiconductors. Terminal being a term that is used in
25 the patents, I think it's -- we've already gone through

1 that VINT can correspond to a terminal.

2 BY MR. ANDERSON:

3 Q. So your answer is yes?

4 MR. JONES: Same objections.

5 BY MR. ANDERSON:

6 Q. Yes, VINT is a terminal as it's shown in Figure
7 2A?

8 MR. JONES: Same objections.

9 THE WITNESS: Well, if I look at Figure 2A, I
10 can call VINT a terminal or a node, and I think those
11 are reasonable descriptions.

12 BY MR. ANDERSON:

13 Q. So if we look at column 5, line 22, in there
14 it's describing Figure 5; correct?

15 A. Yes.

16 Q. And the '492 patent states that the resistor
17 420 that was in Figure 4 has been replaced with an NMOS
18 transistor in Figure 5; correct?

19 A. That's -- let me just verify that. Yes, that's
20 correct.

21 Q. And the '492 patent indicates that the body
22 region of the transistor 420 is connected to ground;
23 correct?

24 A. Yes, I see where you're reading that.

25 Q. Why would the body region of the NMOS 420 be

1 connected to ground?

2 A. Well, that is a -- in most cases the body will
3 be at a ground bias through a substrate. The reason for
4 saying that the body is connected to ground is in the
5 usage of the transistor. There are two cases when you
6 do this. There may be others, but there's two examples
7 I can give.

8 The first is where you have a very long channel
9 and so you're using the transistor as a -- essentially a
10 voltage-controlled resistor. In order to make the
11 resistance more controllable by the gate voltage, it's
12 important to have the well contact, so the body contact
13 be very close to the source.

14 The other implementation where that's
15 particularly useful is in power diodes. Sorry. Power
16 transistors. So if you ever see motor drivers or
17 similar circuits, they will employ the same schematic
18 element and the same principle which is that you want to
19 have an absolute minimum chance of the channel
20 underneath the transistor drifting even a little bit
21 above ground. If it does, just because the control from
22 the gate is so specific and so critical, it will impede
23 the proper operation of the circuit.

24 Q. So are the body regions of NMOS transistors
25 typically connected to ground in CMOS circuits?

1 MR. JONES: Objection to form. Outside the
2 scope of the expert's declarations.

3 THE WITNESS: So in general CMOS architecture,
4 an NMOS transistor will be created by two NPLUS
5 diffusion regions over the generic p substrate. It
6 could be a p-minus. It depends on the technology. But
7 the substrate would be -- that would be grounded in such
8 a way that, when a positive voltage is applied to the
9 gate, carriers are formed in the channel, lowering
10 resistance of the device.

11 BY MR. ANDERSON:

12 Q. So at column 5, about line 29, the '492 patent
13 refers to the drain/body diode of the transistor 420 in
14 Figure 5.

15 Do you see that?

16 A. I do, yes.

17 Q. And what is a body diode?

18 A. A body diode is a parasitic device created by
19 the p-n junction of -- in this -- in the case of an NMOS
20 transistor, the P substrate to the NPLUS diffusion
21 region.

22 Q. So the '492 patent indicates that when the
23 power is off, transistor 420 is off; correct?

24 A. That is correct.

25 Q. And the '4- -- '492 patent also indicates that

1 when the power is off, the body diode of transistor 420
2 does not allow the voltage on the VINT terminal 212 to
3 rise above one diode threshold voltage relative to
4 ground.

5 Do you see that?

6 A. Let me reread the section real quick.

7 MR. JONES: Same objections.

8 THE WITNESS: Yeah, I see where you're reading
9 that.

10 BY MR. ANDERSON:

11 Q. How does the body diode keep the voltage on
12 terminal 212 from rising to a voltage that is more than
13 one diode threshold above ground?

14 MR. JONES: Same objections.

15 THE WITNESS: Well, that body diode is -- the
16 p-n directionality of it is from substrate into the
17 diffusion so the node that is equivalent to 212. So
18 looking at the language here, I think the way to
19 interpret what this is saying is that the drain/body
20 diode of transistor 420 does not allow the voltage on
21 Terminal 212 to be more than one diode threshold
22 relative to ground, and in this case it's going to be
23 negative relative to ground because that's the way the
24 diode is pointing.

25 ///

1 BY MR. ANDERSON:

2 Q. And how does it accomplish that limitation on
3 the voltage at node 212?

4 A. Well, if we turn off device 420, then we assume
5 that the gate of 420 is ground, the source is ground and
6 the body is ground. The body being ground means that
7 there is a 0 potential on the P side of the p-n
8 junction.

9 Q. Is that the anode of the diode?

10 MR. JONES: Same objections.

11 THE WITNESS: In terms of the parasitic diode,
12 the p section will be the -- NPLUS in this case would
13 be -- would form the cathode-like region.

14 So we have a diode whose anode is at ground
15 with its cathode at Terminal 212 which means that the
16 signal VINT could never go below one diode drop from
17 ground.

18 BY MR. ANDERSON:

19 Q. If it did go below one diode drop from ground,
20 what would happen?

21 MR. JONES: Same objections.

22 THE WITNESS: Charge carriers would move across
23 the diode and from the grounded body and restore the
24 voltage, essentially clamping it to minus one transition
25 voltage.

1 MR. ANDERSON: About an hour.

2 MR. JONES: Yeah. I was trying to find a good
3 junction. Is this a good stopping spot?

4 MR. ANDERSON: Yes.

5 (Recess taken from 1:58 p.m. to 2:09 p.m.)

6 BY MR. ANDERSON:

7 Q. So earlier in discussing Figure 2A, you
8 indicated that you can't tell from Figure 2A whether
9 VINT is a terminal T1 for providing -- oh, sorry. Let
10 me start over.

11 Earlier when we were discussing Figure 2A, you
12 indicated you can't tell from Figure 2A itself whether
13 VINT is a first terminal for receiving a constant
14 nonground voltage throughout operation of the latch as
15 that term appears in Claim 14; correct?

16 A. Yeah. I think we specifically said that the
17 aspect throughout operation of the latch could not be
18 determined.

19 Q. Is VINT capable of being a first terminal for
20 receiving a constant nonground voltage throughout
21 operation of the latch?

22 MR. JONES: Objection to form.

23 THE WITNESS: Well, in order for -- in order
24 for Claim 14 limitation 1 to be satisfied, the terminal
25 must meet all the limitations and all the words in the

1 limitation, and so if VINT meets the requirements as set
2 forth in column 4:66 through 5:7, then as defined
3 therein, VINT is a constant value throughout the
4 operation.

5 BY MR. ANDERSON:

6 Q. So is VINT in Figure 2A capable of receiving a
7 constant nonground voltage throughout operation of the
8 latch?

9 MR. JONES: Objection to form. Outside the
10 scope of the expert's declaration.

11 THE WITNESS: Again, I think I've said that
12 VINT is -- can satisfy the requirement of a constant
13 voltage throughout operation if it meets the
14 requirements of that condition as set forth in column
15 4:66 through column 5:7.

16 BY MR. ANDERSON:

17 Q. So if someone provides a constant nonground
18 voltage to VINT in Figure 2A throughout operation of the
19 latch, the latch will operate properly; correct?

20 MR. JONES: Objection to form.

21 THE WITNESS: Whether or not a latch operates
22 properly is quite a subjective term. I don't think I
23 can render an opinion generically on that.

24 To be very specific, there are multiple things
25 that can cause an element to behave properly or

1 improperly.

2 BY MR. ANDERSON:

3 Q. In column 3 of the '492 patent, in describing
4 Figure 2A, it states that voltage VINT is a positive
5 voltage at line -- lines 18 to 19.

6 Do you see that?

7 A. Yes. That's the description of the embodiment
8 in Figure 2A.

9 Q. So if VINT is a positive voltage throughout
10 operation of the latch, in Figure 2A does that disclose
11 the first terminal recited in Claim 14?

12 MR. JONES: Objection to form.

13 THE WITNESS: So looking at the first
14 limitation of Claim 14, you see a first terminal for
15 receiving a constant nonground voltage throughout
16 operation of the latch. So the requirements are there
17 has -- it has to be a first terminal, it has to receive
18 a constant nonground voltage, and it has to receive that
19 constant nonground voltage throughout operation of the
20 latch. If it meets those three conditions, then it
21 meets the -- this limitation of the claim.

22 BY MR. ANDERSON:

23 Q. And VINT in Figure 2A is capable of meeting
24 that limitation; correct?

25 MR. JONES: Objection to form. Outside the

1 scope of the expert's declarations.

2 THE WITNESS: So again, Figure 2 is just an
3 embodiment. Whether something is capable of meeting
4 that, that's an implementation question.

5 BY MR. ANDERSON:

6 Q. Is Figure 2A capable of receiving a constant
7 nonground voltage throughout operation of the latch on
8 VINT?

9 MR. JONES: Objection to form. Outside the
10 scope of the expert's declarations. Asked and answered.

11 THE WITNESS: So looking at Figure 2, the
12 question as to whether the VINT terminal can operate
13 throughout -- can receive the constant nonground voltage
14 throughout the operation of the latch is determined by
15 whether it meets the conditions as set out in the
16 specification for -- throughout operation of the latch
17 which properly construed at all times during circuit
18 operation without being disabled as supported in the
19 specification in the language at column 4:66 through
20 column 5/7.

21 BY MR. ANDERSON:

22 Q. So VINT and 2A is capable of receiving a
23 constant nonground voltage throughout operation of the
24 latch. It just is your opinion that that is not
25 disclosed specifically in Figure 2A; correct?

1 MR. JONES: Same objections.

2 THE WITNESS: Again, the embodiment in 2A is
3 described in some detail. The language of column 4:66
4 through 5:7 being the language that it necessitates or
5 describes the condition for the correct interpretation
6 throughout operation of the latch starts within some
7 embodiments. So certainly some embodiments can practice
8 the restriction imposed by -- throughout operation of
9 the latch.

10 BY MR. ANDERSON:

11 Q. Is Figure 2A one of those embodiments that can
12 receive a constant nonground voltage throughout
13 operation of the latch?

14 MR. JONES: Same objections.

15 THE WITNESS: Again, meeting those requirements
16 are specified in the specification. Whether or not
17 that -- this particular latch is capable, to understand
18 whether or not the particular implementation
19 corresponding to Figure 2 is capable, we would have to
20 see it and see what other circuitry is around it or what
21 design constraints it has.

22 BY MR. ANDERSON:

23 Q. So looking at Figure 2A, you're unable to tell
24 me whether or not VINT can receive -- is capable of
25 receiving a constant nonground voltage throughout

1 operation of the latch as recited in Claim 14?

2 MR. JONES: Same objections.

3 THE WITNESS: Sitting here today, I am capable
4 of telling you that in order to make that determination
5 for the latch in Figure 2A, you would have to look at
6 the -- all of the circuitry involved to determine
7 whether it meets the limitations as imposed by the text
8 between column 4:66 through 5:9.

9 BY MR. ANDERSON:

10 Q. And where is all of the circuitry involved to
11 determine whether it meets the limitations disclosed in
12 the '492 patent?

13 A. Well, we can -- we can read that section of the
14 specification where it describes. And then I'm reading
15 now from column 4:66. In some embodiments the
16 synchronous DRAM includes several generators. Each
17 generator is enabled by its own signal EN. Thus
18 selective generators 213 can be disabled to reduce power
19 consumption; instead by mode, for example.

20 The critical passage, however, at least one
21 generator 213 is enabled throughout circuit operation in
22 order to power circuits that are never disabled. For
23 example, the buffer 386. Hence the VINT voltage is a
24 constant voltage throughout the operation of the
25 integrated circuit.

1 So we would minimally need to understand at
2 least one generator 213 enabled throughout the circuit
3 operation in order to power circuits that are never
4 disabled. For example, buffer 386.

5 Q. So if VINT in Figure 2A was generated by the
6 circuit of Figure 3, would VINT receive a constant
7 nonground voltage throughout operation of the latch?

8 MR. JONES: Same objections.

9 THE WITNESS: Again, that's not a determination
10 that can be made without understanding what control --
11 all of the elements that controlled us in the adjoining
12 circuitry.

13 BY MR. ANDERSON:

14 Q. So if VINT and Figure 2A was generated by the
15 circuit of Figure 4, would VINT receive a constant
16 nonground voltage throughout operation of the latch as
17 that is recited in Claim 14?

18 MR. JONES: Same objections.

19 THE WITNESS: That is also indeterminate and it
20 is equally indeterminate for the same reasons.

21 BY MR. ANDERSON:

22 Q. If the VINT signal in Figure 2A is generated
23 using the circuit of Figure 5, is -- does the VINT
24 terminal receive a constant nonground VOLTAGE throughout
25 operation of the latch?

1 MR. JONES: Same objections.

2 THE WITNESS: Same answer as for Figure 3 and
3 Figure 4. That's indeterminate. Requires more
4 information.

5 BY MR. ANDERSON:

6 Q. So in looking at the '492 patent and looking at
7 Figure 2A, you cannot tell whether any of Figures 3, 4
8 or 5 are capable of providing a constant nonground
9 voltage to VINT throughout operation of the latch?

10 MR. JONES: Objection. Outside the scope of
11 the expert's declarations.

12 THE WITNESS: I think I've already answered
13 that the requirement for VINT to meet the cause constant
14 voltage throughout operation is spelled out in the
15 specification. If it meets that specification, then it
16 is -- can be said to have a cost of value throughout
17 operation. If it doesn't meet that specification, then
18 it doesn't. And I pointed now numerous times to the
19 section of the patent that spells out that
20 specification.

21 BY MR. ANDERSON:

22 Q. So do any of Figures 3, 4 or 5 provide a
23 constant nonground voltage throughout operation of the
24 latch?

25 MR. JONES: Same objections.

1 THE WITNESS: Again, that determination can't
2 be made looking strictly at Figures 3, 4, 5.

3 BY MR. ANDERSON:

4 Q. I'm going to hand you a copy of Exhibit 1006
5 which is U.S. Patent 4,621,346 to McAdams.

6 Do you recognize this patent?

7 A. I do.

8 Q. Could you please turn to the bottom of column 1
9 of McAdams. And starting at the bottom of column 1, do
10 you see that -- I mean all the way at the bottom of
11 column 1, McAdams is describing the operation of
12 Figure 1.

13 A. Okay. I see where you're getting that.

14 Q. Okay. And if you look at Figure 1 of McAdams,
15 would you agree that Figure 1 of McAdams includes all of
16 the circuit elements that are shown in Figure 2A of the
17 '492 patent?

18 A. I'm sorry. That Figure 1 of McAdams includes
19 all of the elements shown where?

20 Q. In Figure 2A of the '492 patent.

21 MR. JONES: Objection to form.

22 THE WITNESS: I see several items in Figure 2A
23 that are not present in Figure 1 of McAdams or that are
24 several elements in the '492 patent, Figure 2A, that are
25 not present in McAdams 346, Figure 1.

1 BY MR. ANDERSON:

2 Q. Which elements are we talking about?

3 A. So Figure 2A in the '492 patent includes diode
4 234 and also includes the VINT generator 213.

5 Q. Is there anything else in Figure 2A of the '492
6 patent that is not in Figure 1 of McAdams?

7 MR. JONES: Objection to form.

8 THE WITNESS: Let me preface by saying that it
9 may not be entirely proper to say that the same elements
10 are in one diagram versus another. I will say that
11 there are similar elements in the McAdams Figure 1 to a
12 subset of elements within '492 Figure 2A.

13 BY MR. ANDERSON:

14 Q. Would you agree that the fuse in Figure 1 of
15 McAdams is a nonvolatile programmable element?

16 A. If we assume that the fuse in McAdams is
17 metallic, then I think that's -- that is a safe
18 assumption. Want to caveat there that we can look for
19 exactly how McAdams describes the fuse, but I think it's
20 a safe assumption.

21 Q. Is there a fuse that would not be a nonvolatile
22 programmable element?

23 A. If somebody designed one, yes.

24 Q. Okay. So assuming the fuse in Figure 1 of
25 McAdams is programmed, will that result in excess charge

1 accumulating at Node 14?

2 MR. JONES: Objection to form.

3 THE WITNESS: There is no certainty, I would
4 say, if the fuse is programmed as to whether charge will
5 always or will never accumulate on node 14. It's a
6 circumstantial question. Charge could accumulate on
7 node 14.

8 BY MR. ANDERSON:

9 Q. Does the NMOS transistor 11 in Figure 1 of
10 McAdams constitute a variable impedance path?

11 MR. JONES: Objection to form.

12 THE WITNESS: I would say that in the context
13 of the '492 patent, the description of Transistor 110 as
14 a variable impedance path in Figure 2A is consistent
15 with the placement and function of transistor 11 in
16 McAdams Figure 1.

17 BY MR. ANDERSON:

18 Q. Transistors 12 and 13 in Figure 1 of McAdams
19 form an inverter; correct?

20 A. The inverter -- an inverter is traditionally
21 thought of as a PMOS device on top of an NMOS device.
22 It can have other constructions, but I would say that
23 that is an inverter construction.

24 Q. And the input of the inverter is connected to
25 node 14; correct?

1 A. Yes.

2 Q. And the output of the inverter is provided to
3 the gate of transistor 11; correct?

4 A. It is. And just for clarity of the record, we
5 are referring to Figure 1 of McAdams.

6 Q. And in order for the output 15 of the latch in
7 Figure 1 of McAdams to reflect the state of the fuse 10,
8 power has to be supplied to the VCC node; correct?

9 MR. JONES: Objection to form.

10 THE WITNESS: Well, if we assume that a fuse or
11 a fused latch, a fused controlled latch is a
12 semiconductor. In order to represent any state, the
13 semiconductor must be operational and an operational
14 semiconductor requires power.

15 BY MR. ANDERSON:

16 Q. So if power is not provided on VCC, then
17 transistor 12 in the inverter will be unable to pull the
18 output 15 high; correct?

19 MR. JONES: Objection to form.

20 THE WITNESS: Without power being applied to
21 VCC, the concept of high and low don't apply. High and
22 low are in reference to VCC versus ground.

23 BY MR. ANDERSON:

24 Q. So in other words, for the latch to be
25 operational, then power has to be applied to the latch;

1 correct?

2 MR. JONES: Same objection.

3 THE WITNESS: I think we've already agreed that
4 a semiconductor device requires power to be operational.
5 BY MR. ANDERSON:

6 Q. So looking at Figure 1 of McAdams, it includes
7 a nonvolatile programmable element in Fuse 10; correct?

8 A. Again, using the -- using the terminology as
9 per the '492 patent, the fuse there would be a
10 nonvolatile programmable element.

11 Q. And you indicated the transistor 11 is a
12 variable impedance path as that term is used in the '492
13 patent; correct?

14 A. In the construction in Figure 1 of McAdams, it
15 functions similarly.

16 Q. And am I correct that the Fuse 10, the variable
17 impedance path 11 and the inverter formed by transistors
18 12 and 13 are interconnected in the same manner as the
19 corresponding elements in Figure 2A of the '492 patent?

20 MR. JONES: Objection to form.

21 THE WITNESS: Well, the figure in 2A defines
22 out and out bar with the out signal being the node T1,
23 whereas McAdams has the output driven from node 15 which
24 would be the equivalent of the out bar signal from the
25 '492 patent.

1 BY MR. ANDERSON:

2 Q. But the elements that I just listed, those
3 elements are interconnected in the same manner in
4 Figure 1 of McAdams as they are in Figure 2A of the
5 '492; correct?

6 MR. JONES: Objection to form.

7 THE WITNESS: I don't know necessarily that I
8 would say they're connected in the same way. I'd say
9 the topology is similar.

10 BY MR. ANDERSON:

11 Q. So assume there's charge on node 14 in McAdams
12 and Fuse 10 has been blown, okay?

13 A. And I'm going to ask you to confirm again. So
14 Fuse 10 blown means that it is open, infinite
15 resistance; is that correct.

16 Q. An open circuit infinite resistance; correct.

17 A. Okay. Thank you.

18 Q. So with that assumption, where would the charge
19 on node 14 dissipate to?

20 A. Sorry. Under what circumstance?

21 Q. Assuming VCC is at 0 volts. Is the charge just
22 going to stay at node 14?

23 A. I'm sorry. What charge?

24 Q. Okay. The beginning of the hypothetical was
25 assume that there's some charge on node 14.

1 A. Okay. So okay. There is charge that has
2 magically appeared on node 14.

3 Q. Let's say that the charge magically appeared
4 when the fuse was blown.

5 A. Okay.

6 Q. And the fuse is blown. It's an open circuit.

7 A. Understood.

8 Q. Is the charge on node 14 going to stay there
9 indefinitely?

10 MR. JONES: Objection to form.

11 THE WITNESS: Again, I think we are accepting
12 the premise that a semiconductor device in your
13 hypothetical in which I understood VCC to be at 0 at
14 ground, that means that all power is off, and eventually
15 all charge must dissipate unless it is trapped within a
16 programmable structure.

17 BY MR. ANDERSON:

18 Q. And the charge that is on node 14 is not
19 trapped inside of a structure, is it?

20 A. You haven't told me where the hypothetical
21 charge came from, but if there's charge on a node as you
22 described, we can assume it's present minimally on the
23 interconnects between those nodes.

24 Q. Can the charge on node 14 leak through the
25 channel of transistor 11?

1 A. So in that circumstance, where all power is
2 removed from the device and ground is supplied so ground
3 is conductive, possible that charge on node 14 would,
4 over an indeterminate period of time and in a rather
5 unpredictable fashion, dissipate over the off resistance
6 of the channel of transistor 11.

7 Q. So earlier when we were talking about how
8 charge would be dissipated from the out node in Figure
9 2A of the '492 patent, I think you indicated there were
10 two ways that the Transistor 110 in Figure 2A could
11 facilitate the dissipation of that charge; is that
12 correct?

13 A. I think -- I think I described three ways in
14 which the charge could dissipate, one of which was
15 through the off resistance, the non-infinite off
16 resistance of the Transistor 110 in the '492 patent
17 Figure 2A.

18 Q. And I don't recall the specifics, but I think
19 you indicated that there was also another discharge path
20 associated with the Transistor 110. Am I remembering
21 that correctly?

22 A. The three examples I remember giving were the
23 discharge through the noninfinite resistance of the off
24 Transistor 110 -- and again, we're referring to '492
25 Figure 2A.

1 Q. Yes.

2 A. The gate leakage as -- that would be seen by
3 transistors 220 and 230, so that's tunnelling of charge
4 through the gate oxide into the substrate and any
5 associated leakage with material that is tied to that
6 out node, essentially logic or systems further on down
7 the line that utilize the out signal would be potential
8 sources of leakage.

9 Q. And in Figure 1 of McAdams, two of those three
10 sources of potential leakage exist for node 14; correct?

11 A. If we take Figure 1 in isolation, then two of
12 those three sources exist as there are no parent users
13 of the potential on node 14.

14 Q. So if the charge accumulates on node 14 due to,
15 say, laser programming of Fuse 10, is it your opinion
16 that that charge will eventually dissipate?

17 MR. JONES: Objection to form.

18 THE WITNESS: So again, I think all -- in the
19 absence of a driven node or a reenforcing active entity
20 in a circuit, a node that has charged on it -- charge on
21 it when all power is removed from the circuitry, that
22 charge will eventually dissipate.

23 BY MR. ANDERSON:

24 Q. And in Figure 1 of McAdams, if VCC is 0 volts,
25 that charge on node 14 can dissipate either through the

1 high resistance channel of transistor 11 or via a path
2 that involves the gates of transistors 12 and 13;
3 correct?

4 A. That's not quite accurate. What I said was
5 that if power was off to the entire semiconductor, it's
6 insufficient that the power is removed strictly from the
7 VCC of Figure 1.

8 Q. So with the condition that power is removed to
9 the -- from the entire semiconductor, if there's charge
10 on node 14, that charge will dissipate through the high
11 resistance channel of transistor 11 and through the
12 gates of transistors 12 and 13?

13 A. Or any other mechanism that may be associated
14 with node 14. McAdams doesn't describe this
15 construction. But again, the assumption is that if a
16 semiconductor is completely off and there is charge
17 somewhere in the semiconductor, it will eventually
18 dissipate, eventually being the indefinite but operative
19 word.

20 Q. So let's assume that Fuse 10 is an open
21 circuit, and there's charge on node 14 but the power is
22 on. What will happen in the circuit of Figure 1?

23 A. Well, that depends on many things, including to
24 what degree the power is on, whether the power is
25 transitioning, exactly what the level of the power is

1 and what the potential is of node 15 and the
2 construction of the transistors.

3 Q. So if the fuse is an open circuit, is there any
4 mechanism for pulling node 14 to VCC in the circuit of
5 Figure 1?

6 A. Yes. Coupling.

7 Q. Coupling between where and where?

8 A. Coupling between anywhere and node 14.

9 Q. And if node 14 is pulled high such that it
10 turns on transistor 13, that will pull node 15 low;
11 correct?

12 A. Well, let me be -- let's be specific. If node
13 14 is of a sufficiently high potential to turn on the
14 NMOS transistor 13 and relative to power is at a
15 sufficiently high potential as to turn off transistor
16 12, then node 15 will be discharged to ground through
17 transistor 13 or to the lowest potential.

18 Q. So if we assume that VCC is stable, meaning
19 it's not transitioning between different values and it's
20 fixed at a certain voltage level, will capacitive
21 coupling induce charge on node 14 from VCC?

22 MR. JONES: Objection to form.

23 THE WITNESS: Okay. There are several problems
24 with that question. Number one, it's not the stability
25 of VCC alone. It is the stability and the absolute

1 level of VCC with respect to the VGS turn on limitations
2 of the channels of 12 and 13 transistors.

3 And second, you repeatedly refer to coupling
4 from VCC to node 14, and I have repeatedly said that
5 it's coupling from anywhere on to node 14.

6 BY MR. ANDERSON:

7 Q. Okay. And by "anywhere," are you referring to
8 circuit elements in the integrated circuit that are not
9 shown on Figure 1?

10 A. I am referring to any device or any
11 interconnect, whether shown in Figure 1 or not, that
12 has -- that has capacitively coupled to some portion of
13 the interconnect 14.

14 Q. Is VCC in McAdams provided throughout operation
15 of the latch shown in Figure 1 of McAdams?

16 A. Using the term "throughout operation of the
17 latch" as described in the specification of the '492
18 patent, it is not determinable whether that condition is
19 met for VCC in Figure 1 of McAdams.

20 Q. If VCC is a constant voltage that is applied
21 throughout operation of the latch, does it meet the
22 limitation of Claim 14 with respect to the first
23 terminal?

24 A. If the latch meets the limitation of Claim 14,
25 then it meets the requirements of that limitation of

1 Claim 14.

2 Q. Is the VCC terminal in McAdams capable of
3 receiving a constant nonground voltage throughout
4 operation of the latch?

5 MR. JONES: Objection to form. Outside the
6 scope of the expert's declarations.

7 THE WITNESS: Yeah. That's not something that
8 can be determined by looking at Figure 1.

9 BY MR. ANDERSON:

10 Q. So you can't tell looking at Figure 1 of
11 McAdams whether or not that circuit is capable of
12 receiving on the VCC terminal a constant nonground
13 voltage throughout operation of the latch?

14 MR. JONES: Same objections.

15 THE WITNESS: I'm going to read the limitation
16 of Claim 14. "A first terminal for receiving a constant
17 nonground voltage throughout operation of the latch."

18 We understand that that imposes a limitation on
19 the constant nonground voltage as specified in the 492
20 specification at 4:66 through 5:9.

21 And McAdams does not specify. And any such
22 conditions for VCC, you're asking if whether it's
23 capable. We would have to look at the McAdams
24 implementation to understand whether it's capable.

25 ///

1 BY MR. ANDERSON:

2 Q. So can you please answer my question? The
3 question is so you can't tell looking at Figure 1 of
4 McAdams whether or not that circuit is capable of
5 receiving on the VCC terminal a constant nonground
6 voltage throughout operation of the latch?

7 MR. JONES: Objection. Form and outside the
8 scope of the expert's --

9 BY MR. ANDERSON:

10 Q. That's a yes-or-no question.

11 A. In order to make a determination about the
12 circuit, I would need more information about it.

13 Q. So you can't tell looking at Figure 1 of
14 McAdams whether or not that circuit is capable of
15 receiving on the VCC terminal a constant nonground
16 voltage throughout operation of the latch?

17 MR. JONES: Outside the scope --

18 BY MR. ANDERSON:

19 Q. Your answer is no?

20 MR. JONES: -- of the expert's declarations and
21 asked and answered several times now.

22 THE WITNESS: Again, if the VCC in McAdams
23 meets the requirements as specified in the '492 patent
24 as specified in column 4:66 through 5:9, then by
25 definition it practices throughout operation of the

1 latch. If it does not meet that requirement, then it
2 does not meet the condition.

3 BY MR. ANDERSON:

4 Q. So you can't tell looking at Figure 1 of
5 McAdams whether or not that circuit is capable of
6 receiving on the VCC terminal a constant nonground
7 voltage throughout operation of the latch? You can't
8 tell looking at Figure 1 whether or not it's capable of
9 receiving it?

10 MR. JONES: Outside the scope of the
11 declarations and asked and answered. It's getting a
12 little abusive here.

13 THE WITNESS: Now we're talking about a
14 semiconductor that implements this. And what those
15 capabilities are, I can't speak to those.

16 BY MR. ANDERSON:

17 Q. So is the VCC terminal capable of meeting the
18 conditions that you say need to be satisfied according
19 to the '492 patent?

20 MR. JONES: Objection to form. Outside the
21 scope of the declarations.

22 THE WITNESS: Again, if the VCC terminal meets
23 the conditions for -- throughout -- throughout operation
24 of the latch as defined in the '492 patent column 4:66
25 through 5:9, then it meets those conditions by

1 definition.

2 MR. ANDERSON: It's a good time for a break.

3 (Recess taken from 2:51 p.m. to 3:12 p.m.)

4 BY MR. ANDERSON:

5 Q. Could you please turn to paragraph 27 of the
6 -779 declaration.

7 A. Yes, I am there.

8 Q. And do you see at the heading B it's your
9 opinion that throughout operation of the latch means at
10 all times during circuit operation without being
11 disabled?

12 A. Yes, I see that.

13 Q. So I want to ask some questions to make sure I
14 understand what that actually entails. What do you mean
15 by at all times during circuit operation?

16 A. So I mean verbatim the description of this term
17 in the '492 specification which is to say that column 4,
18 line 66, through column 5, line 7, that the -- there is
19 "at least one generator 213 is enabled" throughout
20 circuit operation -- and we can read the whole
21 paragraph, maybe, to provide more context. But "In some
22 embodiments, the synchronous DRAM includes several
23 generators. Each generator is enabled by its own signal
24 EN. Thus, selective generators 213 can be disabled to
25 reduce power consumption (in standby mode, for example).

1 However, at least one generator 213 is enabled
2 throughout the circuit operation in order to power
3 circuits that are never disabled, for example, the
4 buffer 386. Hence, the VINT voltage is a constant value
5 throughout the operation of the integrated circuit."

6 BY MR. ANDERSON:

7 Q. So in that context, what do you mean by at all
8 times during circuit operation? Does it mean at all
9 times that power is applied to the circuit?

10 A. Well, I'm using circuit operation the way that
11 it's described in the patent. So if in this case there
12 are multiple generators that are presumably on and a
13 selective generator can be disabled, that indicates that
14 operation is -- was achieved at some point.

15 Q. Okay. So let's take a step back. I want to
16 make sure that all of this makes sense.

17 So Claim 14 says the first terminal for
18 receiving a constant nonground voltage throughout
19 operation of the latch?

20 A. Yes.

21 Q. And the construction says at all times during
22 circuit operation. Is the circuit in the construction
23 the same thing as the latch in Claim 14, or is it
24 something more?

25 A. So we would go to the circuit as it is being

1 used in the relevant citation. So at least one
2 generator 213 is enabled throughout the circuit
3 operation in order to power circuits that are never
4 disabled. So there is -- there is no specification in
5 this text as to what is not powered by a specific VINT.

6 Q. So I think my question is simpler. Is circuit
7 as used in your construction the same thing as the latch
8 that's recited in Claim 14? Because Claim 14 doesn't
9 recite a circuit, so I need to understand what you mean
10 by circuit in the construction. Is it the latch that's
11 recited in Claim 14?

12 A. So it is the latch that is recited in Claim 14.
13 The latch would be a part of the circuit.

14 Q. What circuit? There's no circuit in Claim 14.
15 Are you inserting a circuit that includes the latch?

16 A. No. I am describing the circuit which is used
17 in the specification to define the term throughout
18 operation of the latch.

19 Q. So in your construction, circuit can mean the
20 latch and something more; correct? The latch is a part
21 of the circuit, but it's not necessarily the entirety of
22 the circuit.

23 A. Outside of my construction, even in the
24 specification description, the -- throughout the
25 operation of the circuit describes the VINT voltage.

1 Now, we understand that the latch is using the VINT
2 voltage.

3 Q. So I want to make sure I understand the
4 construction of this claim term completely. And from
5 what you've just said, when you refer to at all times
6 during circuit operation, circuit there can be
7 integrated circuit that is mentioned in column 5, line 7
8 that includes the latch; correct?

9 MR. JONES: Objection to form.

10 THE WITNESS: The text at 4:66 through 5:7 says
11 that there is at least one generator 213 which is
12 enabled throughout the circuit operation in order to
13 power circuits that are never disabled. And the VINT,
14 if it meets these conditions, is then a constant value
15 throughout the operation of the integrated circuits.

16 BY MR. ANDERSON:

17 Q. So the problem I'm having is the integrated
18 circuit is not recited in Claim 14; right? Claim 14
19 recites a programmable latch. So if the latch is
20 operational and the integrated circuit that it's on is
21 not operational, isn't there a conflict?

22 A. No. It's only the VINT voltage that has to
23 have a constant value in the -- or the circuits that are
24 connected to VINT that are not disabled. It's
25 describing here that there is that one generator 213

1 which is enabled throughout the circuit operation in
2 order to power circuits that are never disabled. And so
3 VINT and only that VINT voltage, under that -- under
4 that description is the -- is a constant value
5 throughout the operation of the integrated circuit.

6 Q. So circling around all of that, I still want to
7 get back to the simple question of is the term "circuit"
8 as used in your construction the same or different as
9 the term "latch" recited the Claim 14?

10 A. Well, the latch is part of the circuit.

11 Q. So it's different because the circuit can be
12 more encompassing than simply the latch?

13 A. It's not different with respect to the power
14 VINT that supplies them.

15 Q. My question is very specific. I want to know
16 is the circuit the same as the latch recited in
17 Claim 14, and your answer suggests that circuit includes
18 more than simply the latch.

19 Is that your understanding?

20 A. With respect to the power delivery, they are
21 the same because they have the same conditions.

22 Q. In the context of Claim 14, are they the same,
23 or are they different?

24 A. In the context of Claim 14, the term throughout
25 operation of the latch leads to the explanation herein

1 in column 4 and column 5, and that states that the VINT
2 which is the internal voltage that is powering the latch
3 has this property. It's -- it comes from at least one
4 generator which is enabled throughout circuit operation
5 to power circuits that are never disabled, and a latch
6 is one of those circuits.

7 Q. So again, is the term "circuit" used in your
8 construction the same as the term "latch" used in
9 Claim 14? Is it the same entity? Is the circuit in
10 your construction the latch in Claim 14?

11 MR. JONES: Objection to form. Asked and
12 answered.

13 BY MR. ANDERSON:

14 Q. I think it's a yes-or-no question. Is circuit
15 equal to latch in Claim 14?

16 A. Well, circuit is not used independently. It's
17 used in the term "circuit operation." And so circuit
18 operation and latch operation under the terms of VINT,
19 if they're powered by the same source, have the same --
20 at least one generator enabling throughout the circuit
21 operation.

22 Q. Does Claim 14 state that the power supplied to
23 the latch is the same power that's supplied to the
24 circuit that's in your construction?

25 A. Well, that's exactly what this paragraph says.

1 Q. I'm confused. Can you please explain to me how
2 the paragraph indicates that the power that's supplied
3 to the circuit is the same as the power that's supplied
4 to the latch.

5 A. Again, you're asking a question with regards to
6 circuit alone. I'm using the term "circuit operation,"
7 which is the same as the -- during the time period of
8 latch operation.

9 The way it comes from the claim is that the
10 claim uses the term throughout operation of the latch.
11 "Throughout operation of the latch" is defined
12 specifically in column 4:66 through 5:7, and it is
13 described specifically as requiring "at least one
14 generator 213" that's "enabled throughout the circuit
15 operation to power circuits that are never disabled."
16 And because it's VINT, one of those circuits is the
17 latch.

18 Q. But the integrated circuit includes multiple
19 VINT generators; right?

20 A. The term operation of the integrated circuit is
21 defining time period here, but look at the language
22 of -- starting at line 3. At least one generator 213 is
23 enabled throughout the circuit operation. That circuit
24 operation comes from the specification directly which is
25 why we have circuit operation in the construction.

1 Q. But there's no circuit operation in the claim,
2 and that's why I'm trying to understand how circuit
3 operation relates to the other elements of the claim.
4 And the only thing that's close to a circuit in Claim 14
5 is the latch. So I need to understand, when you say at
6 all times during circuit operation, is that restricted
7 to at all times during latch operation?

8 A. Well, since the latch is part of that circuit,
9 they are by necessity the same. They are operate --
10 they are receiving their power from the same VINT.

11 Q. So the circuit that you're referring to in your
12 construction is not the integrated circuit that includes
13 the latch. It is a circuit within the integrated
14 circuit that includes the latch?

15 A. The term I'm using in the construction is
16 "circuit operation." It's not fair to break it -- to
17 dissect the term. "Circuit operation" comes directly
18 from the specification. I'm going to read again
19 starting at line 3.

20 "At least one generator 213 is enabled
21 throughout the circuit operation in order to power
22 circuits that are never disabled, for example, the
23 buffer 386."

24 And "the VINT voltage," if it satisfies that
25 condition, "is a constant value throughout the operation

1 of the integrated circuit," the integrated circuit being
2 the whole and the circuit connected to the generator
3 being that which is not disabled.

4 Q. Does Claim 14 require a voltage generator?

5 A. It requires a constant nonground voltage
6 throughout operation of the latch.

7 Q. Does that require a voltage generator?

8 A. If we look at the text starting at column 4,
9 line 66, going through column 5 and 7, we see that the
10 condition here is that at least one generator is enabled
11 through circuit operation.

12 Q. So at least one generator is required to
13 provide the VINT signal under your construction; is that
14 correct?

15 A. That is the -- that is the requirement. At
16 least one generator 213 is -- that is enabled throughout
17 circuit operation.

18 Q. Does that generator require the capability of
19 being enabled and disabled?

20 A. I think it has to -- it has to be enabled
21 throughout circuit operation. What other capabilities
22 it may have are not -- not within the scope.

23 Q. If something is on all the time, is it enabled
24 all the time?

25 MR. JONES: Objection to form.

1 THE WITNESS: Again, that sounds like a
2 question about a specific implementation.

3 BY MR. ANDERSON:

4 Q. Well, I'm trying to understand what "without
5 being disabled" means. So if the construction includes
6 without being disabled, that implies to me that it could
7 be disabled. Is it required to have the capability of
8 being disabled?

9 A. The requirement is exactly as is specified in
10 the specification language which is simply that at least
11 one generator that's enabled throughout circuit
12 operation.

13 Q. But that's not what the construction says. The
14 contribution doesn't say it's enabled throughout circuit
15 operation. It says it's during circuit operation
16 without being disabled, which suggests to me that it
17 could be disabled.

18 A. I'm sorry, but that's the same thing. Enabled
19 throughout the circuit operation is the same thing as
20 during circuit operation without being disabled.

21 Q. So is it your opinion that the voltage
22 generator necessarily can be enabled or disabled in the
23 context of Claim 14?

24 A. Well, in the context of this construction, I
25 think the specification clearly outlines the

1 requirements for throughout operation of the latch,
2 which is that at least one generator 213 is enabled
3 throughout the circuit operation. And when that
4 condition is met, then that generator is a constant
5 value throughout the operation of the integrated
6 circuit.

7 Q. Is an external power supply that's provided
8 constantly to an integrated circuit a power supply that
9 is provided at all times during circuit operation
10 without being disabled?

11 MR. JONES: Objection to form.

12 THE WITNESS: I'd have to see the power supply.

13 BY MR. ANDERSON:

14 Q. Is EVCC in Figure 2A of the '492 patent a
15 signal that's provided throughout operation of the latch
16 as that term is used in Claim 14?

17 MR. JONES: Objection to form.

18 THE WITNESS: Again, I would have to see the
19 implementation.

20 BY MR. ANDERSON:

21 Q. Implementation of what aspect?

22 A. Of what is generating the voltage EVCC and the
23 rest of the circuits.

24 Q. So if EVCC is connected to the power supply on
25 a computer that is turned on, is that -- it's directly

1 connected to the output of a power supply. Is that
2 going to be a voltage that is provided at all times
3 during circuit operation without being disabled?

4 MR. JONES: Objection to form.

5 THE WITNESS: I haven't formed any opinions on
6 power supplies, PC power supplies. And as I've stated,
7 in order to make that determination, I'm going to need
8 to see and investigate the actual product and its
9 configuration.

10 BY MR. ANDERSON:

11 Q. How do you know if a power supply is provided
12 at all times during circuit operation without being
13 disabled? How would you be able to detect that?

14 A. Well, if the power -- again, it depends on
15 meeting the limitation. And we're talking about the
16 generator here, not necessarily the power supply. If
17 the generator is enabled throughout circuit operation,
18 then it meets the requirement.

19 Q. Can you turn to column 5 of the '492 patent at
20 line 45?

21 A. Yes, 45.

22 Q. You see there it says, "In some embodiments,
23 the terminals 211 and 240 are both connected to the EVCC
24 terminal 214."

25 A. I see that.

1 Q. Do those embodiments include a power supply
2 that is provided at all times during circuit operation
3 without being disabled?

4 MR. JONES: Objection to form. Outside the
5 scope of the declarations.

6 THE WITNESS: Again, that can't be determined
7 without looking at them.

8 BY MR. ANDERSON:

9 Q. So if EVCC is simply an external voltage that's
10 supplied and there's no voltage generator involved in
11 producing it, can it be a voltage that is provided at
12 all times during circuit operation without being
13 disabled according to your construction?

14 MR. JONES: Same objections.

15 THE WITNESS: If the implementation can meet
16 the limitation, then it can meet the limitation. If the
17 implementation does meet the limitation, then it meets
18 the limitation. It's up to the implementation.

19 BY MR. ANDERSON:

20 Q. And the only example that you're able to
21 provide in the '492 patent of a voltage that is supplied
22 at all times during circuit operation without being
23 disabled is in the section between column 4, line 66,
24 and column 5, line 7; correct?

25 A. As far as I know, that is the only place that

1 it is discussed. If you're aware of other places where
2 it is discussed, I'd be happy to look at them.

3 Q. So again, I want to go back and make sure that
4 I understand the scope of this construction. And again,
5 I'm troubled by the language "without being disabled."

6 Does that require that the supply voltage has
7 the ability to be enabled or disabled? Or does it just
8 require that it is always present?

9 MR. JONES: Asked and answered.

10 THE WITNESS: The only requirement is that it
11 meets the limitation as it is set out in the
12 specification.

13 BY MR. ANDERSON:

14 Q. And I'm trying to understand what that is. And
15 I think the question is pretty straightforward. If it's
16 a supply voltage that's being provided to the circuit,
17 do you have to have an enable signal that turns it on
18 and off? Is that part of your construction?

19 MR. JONES: Same objection.

20 THE WITNESS: I don't see any mention of an
21 enable signal.

22 BY MR. ANDERSON:

23 Q. So you don't need an enable signal on a power
24 supply in order to meet this construction; is that
25 correct?

1 A. That's not clear.

2 MR. JONES: Same objection.

3 BY MR. ANDERSON:

4 Q. Is your proposed construction for throughout
5 operation of the latch applicable to the use of that
6 term throughout the claims of the '492 patent?

7 A. Well, I'm not aware of it being used outside of
8 14.

9 Q. Can you look at claim 17?

10 A. Oh, sorry. Oh, I'm sorry. I wasn't aware of
11 any independent claims that used it outside of 14.

12 Q. Yes. Could you look at claim 17 of the '492
13 patent?

14 A. Yes. 17 uses that same language, and the
15 construction there is also applicable.

16 Q. Does the '492 patent provide any disclosure of
17 enable/disable functionality associated with the grounds
18 provided in any of the embodiments shown?

19 MR. JONES: Outside the scope of the
20 declarations.

21 THE WITNESS: I think the '492 patent provides
22 ample specification which we've discussed at length for
23 the term "throughout operation of the latch."

24 BY MR. ANDERSON:

25 Q. Did you consider claim 17 when you opined on

1 the construction of throughout construction of the
2 latch?

3 MR. JONES: Objection to form.

4 THE WITNESS: Well, it's part of construction
5 under Philips (phonetic) is to consider the claim usage
6 of the term.

7 BY MR. ANDERSON:

8 Q. I'm asking, did you consider claim 17 when you
9 opined on the proposed construction of throughout
10 operation of the latch?

11 A. Yes.

12 Q. And when we were discussing throughout
13 operation of the latch in the context of the first
14 terminal, you indicated that a voltage generator was
15 part of providing the constant nonground voltage
16 throughout operation of the latch; correct?

17 MR. JONES: Misstates prior testimony.

18 THE WITNESS: I think the statement that I made
19 repeatedly was that the requirement to meet throughout
20 operation of the latch is to meet the specifications
21 description which is having at least one generator 213,
22 a generator being a path to provide power and ground to
23 circuits. That is enabled throughout the circuit
24 operation in order to power circuits that are never
25 disabled.

1 BY MR. ANDERSON:

2 Q. Where does the '492 patent disclose a generator
3 that provides ground voltage to any of the circuits
4 shown in the '492 patent?

5 A. I'm looking at column 5, line 3 through 7. A
6 generator that is enabled throughout circuit operation
7 in order to power circuits. Powering circuits means
8 providing power and ground.

9 Q. Does it ever say that the ground voltage is a
10 constant value throughout the operation of the
11 integrated circuit?

12 A. I think it does as it says that the generator
13 which powers the circuits is enabled throughout circuit
14 operation.

15 Q. So is it your opinion that a circuit could
16 have -- an integrated circuit could have multiple
17 voltage generators that provide different ground
18 potentials to different parts of the circuit?

19 MR. JONES: Objection to form and scope.

20 THE WITNESS: You're speaking about a
21 hypothetical circuit, but there's certainly circuits,
22 some of which I've worked on, that provide multiple
23 source voltages and multiple drain voltages.

24 BY MR. ANDERSON:

25 Q. Does the '492 provide that disclosure?

1 MR. JONES: Same objections.

2 THE WITNESS: I don't recall the exact portion
3 of the specification, but I know there's at least a
4 figure that describes using a negative ground voltage
5 and different -- different supply voltages.

6 BY MR. ANDERSON:

7 Q. I think you already have a copy of that. I'll
8 give one to Kevin.

9 This is a copy of the -780 declaration.

10 A. Okay. I'm going to leave the copy here and
11 close my -790 and take out my -780.

12 So I have the -780 declaration for '492 IPR
13 2019-00780.

14 Q. Can you please turn to paragraph 36 of the -780
15 declaration.

16 A. Yes.

17 Q. What is your understanding of the McAdams Uda
18 combination that Samsung is proposing?

19 A. Well, my understanding is that Samsung is
20 proposing that -- one of the buried layer resisted diode
21 combinations from the Uda reference would be
22 incorporated by somebody of ordinary skill in the art
23 looking at McAdams in order to modify that circuit. I
24 understand that to be Samsung's contention.

25 Q. So it's your understanding that Samsung is

1 proposing to take the specific diode as it's implemented
2 in Uda and insert that into the CMOS circuit of McAdams?

3 A. The element that Samsung has identified as a
4 diode, yes.

5 Q. Is it your understanding that the combination
6 requires taking a diode that's formed at the junction of
7 a resistive epitaxial P region and a buried N region and
8 putting that specific diode construction into the CMOS
9 circuit of McAdams?

10 A. Well, I understand that to be a combination
11 that could be made but as that is the diode that exists
12 within Uda, to claim that looking at a diode in Uda and
13 being inspired to move it would by necessity mean moving
14 that diode as it functions in Uda.

15 Q. Can you please turn to paragraph 38 of the same
16 -780 declaration?

17 A. Sure. Paragraph 38.

18 Q. Do you see that in paragraph 38 you say that
19 the diodes in Uda are to protect underlying circuitry
20 during fused programming?

21 A. Yes, to prepare against destructive damage
22 during fused programming, yes.

23 Q. And you also say in paragraph 38 that
24 protecting the underlying circuitry in Uda is solving a
25 different problem than that addressed by the '492

1 patent; correct?

2 A. That's correct.

3 Q. Is it your contention that a person of ordinary
4 skill in the art would not include a diode in McAdams to
5 protect the underlying circuitry in the same manner that
6 Uda uses a diode for in its implementation?

7 A. I would say that, first of all, McAdams doesn't
8 recognize the need to protect the node, but let's start
9 with, first, that protecting a node from actual damage
10 from laser which in Uda constitutes breaking the gate
11 oxide of an inset implemented by CMOS is a different
12 problem than protecting a node from erroneous value.
13 More specifically, an erroneous value is not something
14 which destroys the chip, renders it inoperable. It's
15 just something that gives you an incorrect logical
16 state.

17 Q. So it's your understanding that Uda doesn't
18 disclose that a diode is used to get rid of accumulated
19 charge on a node in order to prevent faulty values from
20 being read from a fuse; correct?

21 A. That's right. The Uda construction is a fuse
22 with a -- essentially an ECL-type construction. So it's
23 a fuse with a resistor of some medium value going to the
24 lower potential. So in essence there is no variable
25 impedance device. It is a constant impedance device,

1 and the fuse is either connecting to ground or not.

2 Q. And is it your understanding that Samsung's
3 combination of Uda and McAdams is that a person of
4 ordinary skill in the art would have been motivated to
5 include a diode like in Uda and McAdams in order to get
6 rid of accumulated charge to prevent false states? Is
7 that the motivation that was prevented by Samsung?

8 MR. JONES: Objection to form.

9 THE WITNESS: I can't speak to what the
10 motivation of Samsung was. I can speak -- I've reviewed
11 Dr. Baker's declaration, and he certainly seemed to
12 suggest that a McAdams-Uda combination would achieve the
13 same goals as the '492 patent. So whether it was
14 stated, it was certainly implied.

15 BY MR. ANDERSON:

16 Q. I -- do you understand there's a difference
17 between what a circuit is intended to do and what it
18 actually achieves?

19 A. Yes.

20 Q. So if the diode is present in McAdams as
21 presented in Samsung's combination, is it necessary for
22 that diode to be included for a particular purpose?

23 A. No. To -- to invalidate the claim, it has to
24 show that it practices all of the same limitations of
25 the claim, which is not the case.

1 Q. Do you say that the diode in the McAdams-Uda
2 combination does not maintain the voltage on the
3 Terminal T1 within a predetermined range of values
4 anywhere in your declaration?

5 A. That may not have been in this declaration, but
6 that's certainly the case.

7 Q. I'm going to hand you a copy of Dr. Baker's
8 declaration that was filed in the -780 proceedings, and
9 I'll just keep it open to page 75 because I want to
10 refer to the figure that's on that page.

11 A. Okay.

12 Q. So looking at the figure on page 75, assuming
13 that Fuse 10 has been blown, is it your opinion that the
14 diode shown in the green box will not maintain the
15 voltage on node 14 within a predetermined range before
16 power is supplied to the circuit in Figure 1?

17 MR. JONES: Objection. Outside the scope of
18 the declarations that this witness submitted in this
19 proceeding.

20 THE WITNESS: Maybe if we can bring up Uda, the
21 Uda reference, we can look at that Uda diode.

22 BY MR. ANDERSON:

23 Q. It's -- let's assume that's a diode that has an
24 anode and a cathode and operates as a diode operates
25 such that it has a threshold voltage. And when the

1 voltage on the anode is greater than the voltage on the
2 cathode by more than the threshold voltage, it will
3 conduct.

4 A. But that's not the diode in Uda.

5 Q. I'm representing to you to make the assumption
6 that the diode that's presented in Figure 1 is such a
7 diode. And I believe you indicated that if a diode was
8 present in the McAdams-Uda combination, it would not
9 maintain the voltage within a predetermined range of
10 values a few minutes ago in your testimony; is that not
11 correct?

12 MR. JONES: Objection to form.

13 THE WITNESS: Yeah. I think my testimony was
14 that the Uda diode placed within McAdams would not
15 satisfy keeping the voltage of terminal T1 within the
16 predetermined range.

17 BY MR. ANDERSON:

18 Q. So if the diode shown in Figure 1 on page 75
19 here was just a CMOS p-n junction diode, would it
20 accomplish what the claims of the '492 recite with
21 respect to the diode in terms of maintaining the voltage
22 on node 14 within a predetermined range of values?

23 MR. JONES: Objection to form and outside the
24 scope of declarations.

25 THE WITNESS: Again -- that, I think, is --

1 we'd have to look at that more cleanly in terms of
2 looking at a modification. I think we've already stated
3 that McAdams, with a diode as per the '492 patent, that
4 those diodes act the same.

5 My statement, and I want to be very clear on
6 this for the record, is that the Uda diode does not keep
7 the voltage on terminal 1 within the predetermined range
8 of values.

9 BY MR. ANDERSON:

10 Q. So you haven't opined, then, on if a regular
11 p-n junction diode that is compatible with the CMOS
12 process of McAdams were inserted as shown on page 75 of
13 Dr. Baker's report, how that would operate, have you?

14 A. Well, I think -- I think we can agree that if
15 Dr. Baker has created a diode drawing which mirrors the
16 '492 patent, then it mirrors the '492 patent. But the
17 question that you raised was the motivation to bring the
18 Uda diode into McAdams, and that's the context in which
19 I answered which is that the Uda diode brought into
20 McAdams does not keep the voltage at Terminal 1 within
21 the predetermined range of values.

22 Q. Does the '492 patent use a special diode in the
23 embodiments that include a diode?

24 A. I'm not sure what you mean by "special."

25 Q. I'm not sure I do either. Is there something

1 specific about the diode 234 in Figure 2 of the '492
2 patent that is dissimilar in operation from a standard
3 p-n junction diode?

4 MR. JONES: Objection to form.

5 THE WITNESS: The diode in Figure 2 is a
6 standard p-n diode unlike the Uda diode.

7 BY MR. ANDERSON:

8 Q. And does a person of ordinary skill in the art
9 know what you mean when you say a standard p-n junction
10 diode?

11 A. I would hope so.

12 Q. At the time of the invention of the '492
13 patent, would a person of ordinary skill in the art have
14 been able to include a standard p-n junction diode as
15 Dr. Baker has shown in the drawing on page 75?

16 MR. JONES: Objection to form and outside the
17 scope of the declarations.

18 THE WITNESS: Again, this is -- I have not
19 opined on what was possible at a specific time. I will
20 say that a diode that functions as a diode and as
21 described in the '492 patent is generally considered a
22 p-n junction and unlike the Uda diode which was brought
23 in by Dr. Baker. When he says in this declaration on
24 page 75 diode added based on Uda, I take that to mean a
25 diode added based on Uda, not a diode added based on the

1 general knowledge of p-n junctions.

2 BY MR. ANDERSON:

3 Q. I'm handing you a copy of Exhibit 1010 which is
4 U.S. Patent 5,619,469 to Joo, J-o-o.

5 A. I see that.

6 Q. Can you please turn to Figure 3 of Joo?
7 Actually, Figure 2 of Joo.

8 A. Okay. I'm on Figure 2 of Joo.

9 Q. So when MP1 in Figure 2 of Joo is conductive,
10 does the fuse, Fuse 2, connect terminal N2 and VCC?

11 MR. JONES: Objection to form.

12 THE WITNESS: Well, the Fuse 2 either does or
13 does not connect VC- -- VCC to N2. I'm not sure what --
14 why there was a condition based on MN1 implied in your
15 question.

16 BY MR. ANDERSON:

17 Q. So are FENB and FPR latch initialization
18 signals as that term is used in the '492 patent?

19 MR. JONES: Objection to form. Outside the
20 scope of the declarations.

21 THE WITNESS: Can you -- if you could point to
22 the exact place in the '492 patent where you're talking
23 about those latch initialization signals.

24 BY MR. ANDERSON:

25 Q. I believe the latch initialization signals are

1 discussed -- wait a second. I got to find my '492.

2 A. I have it. It's 2:22 through 32.

3 Q. Yes. Is it your opinion that the FENB and FPR
4 signals in Figure 2 of Joo are latch initialization
5 signals as that term is used in the '492 patent?

6 MR. JONES: Same objections.

7 THE WITNESS: They are certainly involved in
8 the power-up of the circuit in Figure 2. I think
9 whether they initialize the latch is something I would
10 have to consider.

11 BY MR. ANDERSON:

12 Q. Okay. I'm going to hand you your declaration
13 in support of the preliminary response in the -781
14 proceeding. And if you could turn to paragraph 38.

15 Well, actually, paragraph 37 you state that the
16 signal FENB, Fuse Enable Bar, and Fuse Predischage,
17 FPR, disable the fuse and discharge the node N2 during
18 power-up. This action disables the latching portion of
19 the circuit before power has stabilized.

20 So there you indicate that these signals
21 disabled the latch; is that correct?

22 A. They disabled the latching activity, which is
23 to say that they disable the latch from assuming -- and
24 the latch here being NP4 MN1 into Inverter 3, it
25 prevents them from assuming an incorrect latch state.

1 Q. Okay. And in paragraph 38 you state that the
2 '492 specification describes the absence of external
3 control signals for the latch as an advantage that is
4 preserved by some embodiments of the present invention.

5 Do you see that?

6 A. I do.

7 Q. And you cite to column 2, lines 22 to 27;
8 correct?

9 A. That's correct.

10 Q. And that is where the '492 patent discusses
11 latch initialization signals; correct?

12 A. That's correct.

13 Q. And you say that Joo teaches away from this
14 aspect.

15 What do you mean by "Joo teaches away from this
16 aspect"?

17 A. Well, the -- the '492 specification is saying
18 that a simpler latch, one that doesn't require external
19 control signals, is advantageous, which I think is a
20 statement that most POSITA would agree with.

21 And Joo is specifically creating two signals
22 that are used at power up in order to -- in order to
23 generate a state, an initial state of the latch and then
24 to sample the state of the fuse into that latch. And so
25 that is sort of directly contrary to what the '492

1 patent envisions as an advantage that it called out as
2 being a particular advantageous property of the prior
3 art that they maintain in their invention.

4 Q. And in column 2, it says that at line 21 or 22
5 prior art latch of Figure 1 has an advantage that a
6 latch initialization does not require a latch
7 initialization signal from outside the latch, and at
8 column 3, line 66 that you also cite to in paragraph 38,
9 it says no external signal is used to initialize the
10 latch.

11 So in paragraph 38, aren't you indicating that
12 Joo includes latch initialization signals which is
13 contrary to the teachings of the '492 patent?

14 A. Well, I would say that they have orthogonal
15 intents. And specifically when I use the term "teaching
16 away," I'm simply using that to mean that we have two
17 inventions which took completely orthogonal approaches
18 to a problem. One preserving the 0 initialization and 0
19 power-up signals for those advantages. And another one
20 that specifically created a power-up circuitry in order
21 to initialize the feedback of the latch inverter.

22 Q. Okay. So just to be clear, you haven't formed
23 an opinion with respect to whether or not FENB and FPR
24 in Figure 2 of Joo are latch initialization signals as
25 that term is used in the '492 patent; correct?

1 A. No. I think they are certainly used during
2 initialization to the extent that initialization is
3 defined as power-up. But the patent does not go into
4 great detail about what kind of additional properties
5 might be considered for latch initialization signals.

6 Q. All right. I'm confused by your answer. Have
7 you formed an opinion as to whether or not the FENB and
8 FPR signals in Figure 2 of Joo would constant latch
9 initialization signals as that term is used in the '492
10 patent?

11 MR. JONES: Objection to form.

12 THE WITNESS: Again, I think it's consistent in
13 the '492 patent's description of latch initialization
14 signals.

15 BY MR. ANDERSON:

16 Q. I'm handing you -- and I know you already have
17 a copy, but this is your declaration in support of the
18 response in the -781 proceeding.

19 A. Give me one minute to dispose of Joo.

20 Okay. I have that declaration.

21 Q. Okay. If you can please turn to paragraph 35.
22 And in paragraph 35 you refer to the body diode that
23 Samsung has pointed out in Joo.

24 Do you see that?

25 A. I do.

1 Q. And do you understand that the body diode in
2 Figure 2 of Joo that Samsung has identified is between
3 the node N2 and ground?

4 A. Yes, I understand that that's the body diode
5 that was identified.

6 Q. Do you agree that such a body diode exists if
7 the PMOS transistor MP1 is constructed according to
8 conventional CMOS fabrication techniques?

9 A. I think as long as we're dealing with a CMOS
10 process and not by CMOS, and I would say that a body
11 diode exists for the source and drain of a P MOSFET.

12 Q. So yes, the body diode that Samsung has
13 identified would exist if the PMOS transistor is
14 constructed according to a conventional CMOS fabrication
15 techniques?

16 MR. JONES: Objection. Outside the scope of
17 the declarations.

18 THE WITNESS: We may have to point to the exact
19 fabrication techniques, but in general a PMOS diode
20 designed in the technology of the day, pick your CMOS
21 version maybe what? 65 or 130 nanometer at the time,
22 that would include body diodes.

23 BY MR. ANDERSON:

24 Q. And do you understand that Samsung pointed to
25 an additional reference, the Westy (phonetic) reference,

1 to show conventional CMOS fabrication techniques?

2 A. Yes.

3 Q. So for the body diode that has its anode at
4 node N2 and its cathode at ground and you understand
5 that's the connectivity of the body diode that was
6 identified by Samsung; correct?

7 MR. JONES: Objection to form.

8 THE WITNESS: I think if you're referring to
9 the body diode, then the cathode should not be connected
10 to ground.

11 BY MR. ANDERSON:

12 Q. It would be connected to the terminal VCC?

13 A. So if -- if we are -- if we're looking at a
14 body diode -- let me make sure I got this correct --
15 then that is between the -- I'm sorry. I know the
16 diffusion regions are P plus, and so the anode is
17 connected to Node 2. And in order to dissipate voltage,
18 that diode would have to have its N which is its
19 cathode. It would have to point upward in order to
20 dissipate.

21 Q. So it would be connected to BDD? Or VCC?

22 A. VCC.

23 Q. And if the voltage on node N2 is more than a
24 diode threshold voltage greater than the voltage on the
25 terminal VCC, then that diode is forward-biased and

1 would conduct current; correct?

2 A. That assumes certain elements of construction.
3 There are situations where that might not happen. But
4 if the -- if the diode is constructed such that the P
5 plus region is the -- is the anode and the end is the
6 cathode, then that diode would clamp the voltage across
7 it to one diode drop. A higher forward voltage would
8 not be allowed.

9 Q. So if -- if the voltage at node N2 is more than
10 a diode threshold voltage greater than the voltage on
11 terminal VCC, then the diode is going to clamp and force
12 the voltage on node N2 to be no greater than the diode
13 threshold greater than the voltage at VCC; correct?

14 A. I would say in order for -- you may have to
15 short VCC to ground. If it were just at a 0 potential,
16 that might act a little bit differently. But if that
17 diode is going to limit the potential difference between
18 N2 and the cathode to one diode drop, and -- so the
19 cathode would -- that node N2 would by necessity not be
20 more than that diode drop above whatever the cathode is
21 connected to.

22 Q. So based on the presence on the body diode, if
23 power is not applied to -- the circuit of Figure 2 of
24 Joo, the voltage on node N2 cannot be more than a diode
25 threshold voltage greater than the voltage on VCC;

1 correct?

2 MR. JONES: Objection. Form. Outside the
3 scope of the declarations.

4 THE WITNESS: So in Joo, the parasitic diode
5 will impose that VT limit. What I objected to was the
6 statement that Joo specifically teaches that diode for a
7 diode, a discrete diode for that purpose of keeping the
8 voltage within a predetermined range.

9 BY MR. ANDERSON:

10 Q. So you don't disagree that the diode is there.
11 It's just the diode isn't there for the particular
12 purpose that the claim requires?

13 A. Well, the diode, the diode cannot serve that
14 purpose.

15 Q. I'm sorry. I don't understand the distinction.

16 A. Well, as I describe, Joo functions by
17 discharging N2 using the MN1 transistor. So the time --
18 what you're describing in terms of that node being above
19 VCC, even when VCC is grounded, is prevented in
20 operation by MN1.

21 Q. So it's your opinion that because MN1
22 discharges the voltage on node N2 after the fuse has
23 been programmed, the body diode can't dissipate the
24 charge on node N2?

25 A. I would say there's no opportunity for that

1 diode to dissipate that -- to dissipate charge because
2 there was no charge.

3 Q. Because N -- because MN1 has turned on, pulled
4 it all the way; is that correct?

5 A. It has -- it has minimally dissipated that
6 charge, assuming it's a functional MOS device. It has
7 dissipated that charge to VSS.

8 Q. So you don't dispute that the charge on node N2
9 is dissipated. It's just not done by the body diode
10 that Samsung has identified?

11 A. Well, specifically it would never be done by
12 that body diode because it's done by specialized Joo
13 circuitry.

14 Q. Okay. If we look at Claim 1 of the '492 patent
15 and this is at column 48 at line 55, it says a diode for
16 keeping a voltage on the terminal T1 within a
17 predetermined range of values before power is supplied
18 to the latch.

19 Can a transistor MN1 in Joo dissipate the
20 voltage on node N2 before power is supplied to the
21 latch?

22 A. Well, as power is stabilizing to the latch, if
23 we refer to Figure 3, I'd say that power has been
24 applied to the latch at the point before the T1 window.
25 At that point power has been applied to the latch.

1 Q. But before power is supplied to the latch, MN1
2 can't turn on, can it?

3 A. Before that point, the control line FPR is
4 rising, and it's rising with respect to ground.

5 Q. So you're drawing a distinction as to when
6 power is supplied to what portion of the latch? I
7 guess, what are you identifying as the latch in Figure 2
8 of Joo?

9 A. Well --

10 MR. JONES: Objection to form.

11 BY MR. ANDERSON:

12 Q. Is MN1 part of the latch?

13 A. Well, the entirety of the fuse and latch
14 combination is all of the circuitry here. A latch in
15 general is understood to be a pair of inverters or a
16 system which is in positive feedback. In other words,
17 the latch maintains its value.

18 Q. So that's what's shown in Figure 40; right? Or
19 in Box 40 of Figure 2 of Joo?

20 A. That is what's shown in Figure 40. But
21 depending on implementation, if a latch had, say,
22 certain enable signals or had certain additional
23 circuitry, it would not be improper to say that that
24 circuitry was part of the latch even though it's not the
25 inverter feedback.

1 Q. So as VCC ramps up, power is being supplied to
2 the latch circuitry in Box 40 as well as the chain of
3 elements that includes the Fuse 2; correct?

4 A. I'm sorry. Can you repeat that?

5 Q. Sure. Do you see in Figure 2 of Joo there's a
6 VCC rail at the top of Box 40 and above the fuse,
7 Fuse 2?

8 A. I do.

9 Q. So before power is supplied on VCC, will the
10 body diode that's between N2 and VCC keep the voltage on
11 node N2 within a predetermined range of values?

12 A. Well, the body diode is going to enforce a
13 one-threshold voltage limit in the difference between N2
14 and whatever potential the body of NP1 is at.

15 Q. And you would agree that the transistor MN1 in
16 Joo discharges the voltage on the node N2 after power
17 has been supplied to latch in Figure 2; correct?

18 A. I would say that it discharges it in the
19 process of power being applied to the latch.

20 Q. But it is necessary to have power supplied to
21 the latch in order for MN1 to be conducting, is it not?

22 A. It is not necessary for the final power value
23 of the ramp to have been achieved before MN1 is
24 conductive. In fact, MN1 will be conductive
25 significantly before the ramp is finished.

1 Q. Can you please turn to Claim 1 of the '492
2 patent? And do you see the term within the programmable
3 electrical patent that says -- and this is around line
4 47. I'll let you get there.

5 A. Okay.

6 Q. Claim 1 says when the programmable element --
7 one second. I'm one line too low.

8 So around line 45 it says when the programmable
9 element is conductive, the programmable path connects
10 the terminal T1 to the first terminal.

11 Do you see that?

12 A. I see where you're reading that.

13 Q. Is it your opinion that that term should be
14 understood to mean that the programmable path, the
15 programmable element is the only circuit element that
16 controls the conductivity of the path between the
17 terminal T1 and the first terminal?

18 A. Yes. In order to understand this limitation,
19 we have the requirement that the -- when the programmer
20 element is conductive, so in the case of the fuse, that
21 would be when it is whole, the programmable path must
22 connect T1 and the first terminal; the first terminal
23 being the power rail and the general implementation.
24 Connect meaning actually short those together. And when
25 the programmable element is nonconductive, equivalent

1 example being fuse blown, that the programmable path
2 does not connect terminal T1 to the first terminal.

3 Q. Okay.

4 A. And that connectivity is -- is understood by
5 one of ordinary skill in the art to not be subjective to
6 time or other limitations.

7 Q. And just to be concise, it's then your
8 understanding that that claim term means that the
9 programmable element is the only circuit element that
10 controls the conductivity of the path between the
11 terminal T1 and the first terminal; correct?

12 A. That's correct.

13 Q. And that's how a person of ordinary skill in
14 the art would understand the ordinary meaning of that
15 claim term?

16 A. Yes. That's how somebody looking at a
17 programmable element connecting two named nodes would
18 understand those two named nodes being connected as
19 being directly conductive or shorting or functionally
20 shorting.

21 MR. ANDERSON: Could we take a short break?

22 MR. JONES: Yeah, sure.

23 (Recess taken from 4:24 p.m. to 4:34 p.m.)

24 BY MR. ANDERSON:

25 Q. Okay. I'm going to hand you Exhibit 1005 which

1 is the Fu reference which I just have a few questions
2 with respect to Fu that I anticipate the answers will be
3 similar to what I got from McAdams.

4 Can you please turn to Figure 4 of Fu.

5 A. Okay. We are at Figure 4.

6 Q. And like we discussed earlier with respect to
7 Figure 1 of McAdams, does Figure 4 of Fu include an
8 inverter of programmable element in fuse FR and a
9 variable impedance path N1 as those features are shown
10 in Figure 2A of the '492 patent?

11 MR. JONES: Objection to form.

12 THE WITNESS: I would say that the Figure 4
13 in --

14 BY MR. ANDERSON:

15 Q. Fu.

16 A. Fu. Sorry. The elements and their
17 connectivity correspond -- those three elements and
18 their connectivity, the fuse, the variable impedance
19 path and the inverter could be said to correspond to
20 Figure 2A of the '492 patent.

21 Q. Okay. And if we assume that when fuse FR is
22 blown, some charge is deposited on node A, will the
23 charge on node A stay there indefinitely if power is not
24 supplied to the latch circuit shown in Figure 4?

25 A. So I'm going to give the same qualification as

1 with the McAdams case just that in order for -- to be
2 assured that power will eventually dissipate, the entire
3 semiconductor must be off.

4 Q. Thank you. Let me rephrase the question.

5 So if the power to the entire integrated
6 circuit device that includes the circuit shown in
7 Figure 4 of Fu is off and some charge is deposited on
8 node A when the fuse FR is blown, that charge will
9 eventually leak away; correct?

10 A. I'm going to assume that the intent of your
11 question was that the charge was deposited before power
12 went away. I don't know how charge would be deposited
13 after -- afterwards necessarily. That whole
14 semiconductor is off without the programming of the
15 fuse.

16 Q. Okay. That might be a fundamental
17 misunderstanding that I have, so let me ask one more
18 question about that.

19 So if power is off to a semiconductor device
20 and the laser is used to program the fuse FR, could the
21 cutting of that fuse result in charge being deposited on
22 the node A?

23 A. Yes.

24 Q. Okay. And the mechanism that the charge from
25 node A would be dissipated in Figure 4 of Fu is similar

1 to that shown in McAdams, namely the presence of the
2 variable impedance path N1 and the gates of P10 and N2
3 that are included in the inverter; is that correct?

4 MR. JONES: Objection to form.

5 THE WITNESS: So it's a -- assuming that all
6 power is off in the circuit -- we're in the entire
7 semiconductor -- and there exists through some mechanism
8 residual charge on node A, and the fuse FR is blown so
9 as to say completely open. The mechanisms by which that
10 charge would dissipate, again, over an indeterminate
11 time would be through the noninfinite resistance of the
12 transistor N1 from its -- from its drain to source.
13 Even when off, it has -- the channel has some
14 resistance. And through any potential leakage, gate to
15 body or gate to source or gate to drain over the
16 transistors P10 and N2 as shown in Figure 4 of the '696
17 patent.

18 BY MR. ANDERSON:

19 Q. Okay. In Figure 4 of Fu, is the VCC terminal
20 capable of receiving a constant nonground voltage at all
21 times during circuit operation without being disabled?

22 MR. JONES: Objection to form.

23 THE WITNESS: That can't be determined looking
24 at Figure 4.

25 ///

1 BY MR. ANDERSON:

2 Q. So you can't determine whether or not the VCC
3 terminal shown in Figure 4 is capable of receiving a
4 constant nonground voltage at all times during circuit
5 operation without being disabled; correct?

6 MR. JONES: Same objection.

7 THE WITNESS: As I said, you would need to see
8 the circuit and the entirety of the device in order to
9 make that determination.

10 MR. ANDERSON: No further questions.

11 MR. JONES: I have no questions either.

12
13 (Time noted: 4:40 p.m.)

14 --000--

15
16
17
18 _____
19 ERIK DE LA IGLESIA

20
21 Subscribed and sworn to before me
22 this _____ day of _____ 2020.

23
24 _____
25 NOTARY PUBLIC

C E R T I F I C A T E

State of California)
) ss:
County of Alameda)

I, Susan F. Magee, RPR, CCRR, CLR, Certified
Shorthand Reporter No. 11661 within and for the State of
California, do hereby certify:

That ERIK DE LA IGLESIA, the witness whose
deposition is hereinbefore set forth; was duly sworn by
me and that such deposition is a true record of the
testimony given by such witness.

I further certify that I am not related to any
of the parties to this action by blood or marriage; and
that I am in no way interested in the outcome of this
matter.

IN WITNESS WHEREOF, I have hereunto set my hand
this 10th day of February 2020.

Susan Magee

Susan F. Magee, RPR, CCRR, CLR
CSR No. 11661

ERRATA SHEET

Case Name:

Deposition Date:

Deponent:

Pg.	No.	Now Reads	Should Read	Reason
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Signature of Deponent

SUBSCRIBED AND SWORN BEFORE ME

THIS _____ DAY OF _____, 2020.

(Notary Public) MY COMMISSION EXPIRES:_____