

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

Case IPR2019-00780
Patent No. 6,163,492

REBUTTAL DECLARATION OF R. JACOB BAKER, PH.D., P.E.

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. As I testified in my declaration signed March 5, 2019, which I understand has been labeled as Exhibit 1002 in this proceeding, I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I previously provided testimony in this proceeding in my March 5, 2019 declaration. (*See* Ex. 1002.) As with my previous work relating to this proceeding, no part of my compensation is contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding. Relevant aspects of my educational background, career history, and other qualifications were provided in my March 5, 2019 declaration. (*See id.* at ¶¶ 5-15.)

2. I have been asked to provide my opinions regarding certain positions that I understand have been asserted by Mr. de la Iglesia. My rebuttal opinions are set forth below.¹ My opinions in this rebuttal declaration are based on the documents

¹ Although I respond to selected opinions offered by Mr. de la Iglesia, doing so does not mean that I agree with any of Mr. de la Iglesia’s testimony that I do not respond to in this rebuttal declaration.

I reviewed and my knowledge and professional judgment. In forming my opinions in this rebuttal declaration, I considered the Declaration of Mr. de la Iglesia (Ex. 2003) and any other materials that I refer to in this declaration in support of my opinions. In forming these opinions, I have also drawn on my knowledge and experience in designing, developing, and researching semiconductor technology, and rely on my opinions and discussions set forth in my March 5, 2019 declaration, including my opinions regarding the level of skill of one of ordinary skill in the art. In providing my rebuttal to the positions of Mr. de la Iglesia, I do not change my opinions that I provided in my March 5, 2019 declaration.

II. CLAIM CONSTRUCTION

3. It is my understanding that ProMOS has proposed that “a terminal T1 for providing a signal indicating a state of the programmable latch” should be construed as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” (Ex. 2003 at ¶ 28.) In my opinion, a person of ordinary skill in the art would have readily appreciated the meaning of this claim term from the words themselves – the “terminal T1” limitation simply requires a terminal capable of providing a signal that indicates the state of the programmable latch. Such a person of ordinary skill in the art would have recognized that this is the ordinary and customary meaning of this claim term.

4. In my opinion, the proposed construction adds a further limitation to the claim that is not recited in the claim. A terminal is a very simple circuit element, and nothing in the claim suggests that the voltage on the terminal T1 must be dissipated after programming. I understand that Mr. de la Iglesia asserts that the proposed construction is supported because “the embodiment without a diode must be operated such that power is turned off after programming” in order to avoid a false state on the terminal T1 due to excess voltage that may be on terminal T1. (Ex. 2003 at ¶¶ 29-30.) I disagree with Mr. de la Iglesia’s position for at least the following reasons.

5. As an initial matter, claim 1 includes the “terminal T1” limitation and also recites a diode that “keep[s] a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” (Ex. 1001 at 8:55-57.) Thus, claim 1 explicitly defines what happens to the voltage at terminal T1—it is kept within a predetermined range of values. The claimed diode, which corresponds to the diode 234 in figure 2A, also “prevent[s] the latch from assuming an incorrect state when power is supplied to the latch” (*id.* at 8:55-58), and therefore conflicts with Mr. de la Iglesia’s assertion that voltage at terminal T1 must be dissipated after programming in order to ensure proper operation of the programmable latch.

6. In fact, the ’492 patent also discloses other techniques that can be used to ensure that the programmable latch will provide the correct state of the latch –

even when the voltage on “terminal T1” is a “high voltage” and not at ground before power-up of the latch. Claims 20 and 21, which depend from independent claim 14 and therefore also include “a terminal T1 for providing a signal indicating a state of the programmable latch,” are directed to two additional techniques that the ’492 patent indicates can help ensure the output of the latch represents the state of the fuse. Claim 20 adds features concerning selecting the trip voltage of the inverter, and claim 21 adds features concerning selecting the threshold voltage of the variable impedance path NMOS transistor 110. The ’492 patent discloses that such features are associated with embodiments where the voltage on terminal OUT (terminal T1 in claim 14) is a **high value** (i.e. the voltage on the terminal has not been dissipated) immediately before power is applied to the latch:

Further, in some embodiments, **even if the voltage on the terminal OUT is at a high value** immediately before the power is turned on, the latch operates properly due to the selection of the **trip voltage of the inverter and/or the threshold voltage of transistor 110.**

(Ex. 1001 at 2:51-55, emphasis added.)

7. Claims 20 and 21 do not recite a diode, and therefore these embodiments demonstrate that Mr. de la Iglesia’s assertion that in the embodiments without the diode, the terminal T1 has to be at ground before power is applied is incorrect. Instead, by setting the inverter trip point and/or threshold voltage of

transistor 110 to the appropriate values, proper operation of the latch can be ensured **even if the voltage on terminal T1 is a high value** when power is applied to the latch. (Ex. 1001 at 6:9-17 (describing how the trip voltage of the inverter can be set to a high value (e.g. 1.6 volts) “to ensure that the trip voltage will be higher than any voltage on terminal OUT”), 6:18-28 (describing how the threshold voltage of transistor 110 is made low “so that even if the terminal OUT is slightly above the inverter trip voltage when the fuse is blown” the OUT node will still be pulled low by transistor 110).) Like the diode recited in claim 1, the embodiments described in the ’492 patent (*id.* at 2:51-55, 6:8-32) and recited in claims 20 and 21 (which do not include a diode and do not require the terminal T1 to be at ground at power-up) confirm that the ordinary meaning of the “terminal T1” would not require dissipating voltage from the terminal T1 after programming.

8. Notably, Mr. de la Iglesia asserts that “[t]he purpose of the ’492 patent is to avoid false states at the output, a condition that may occur if **excess voltage is allowed to accumulate at the output node during programming** (either due to buildup during fuse cutting, for example laser application, or from capacitive coupling at the output node).” (Ex. 2003 at ¶29 (citing Ex. 1001 at 1:46-48, 1:38-47) (emphasis added).) However, the passages to which he refers in the background of the ’492 patent do not indicate that excess voltage resulting **from programming**

is the problem, and instead indicate the problem is that the “terminal OUT is floating”—a problem not solved by simply turning off the power after programming.

9. According to Mr. de la Iglesia, the terminal OUT may indicate the wrong state before power is supplied to the latch because of two situations that are mentioned in the background section of the '492 patent: (1) terminal OUT is floating and “may tend to have its potential raised to a logic level ‘1’”; and (2) the terminal OUT potential may become unstable due to capacitive coupling. (Ex. 2003 at ¶ 15.) Mr. de la Iglesia contends that one solution to these problems in the '492 patent is the embodiment with a diode as recited in claim 1 (*id.* at ¶¶18-20), while another solution is to allow any charge buildup at the output node to dissipate from the circuit by turning the power off before the output of the latch is used. (*Id.* at ¶ 21.) I agree that the diode recited in claim 1, which corresponds to diode 234 in figure 2A, serves the purpose of dissipating voltage and preventing the latch from having a false state when power is applied to the latch after fuse programming. However, unlike the inclusion of a physical structure like the diode, merely turning off the power to the latch does not prevent the terminal OUT from floating or from suffering from capacitive coupling. To prevent terminal OUT from floating and suffering from capacitive coupling, a physical structure, like, for example, the diode recited in claim 1 is required.

10. A diode can ensure that the node is no longer “floating” by providing a current path through which any accumulated charge can be dissipated. Similarly, if capacitive coupling results in charge being deposited on the node, the diode provides a path for that charge to be dissipated. Turning of the power doesn’t provide such a path. Furthermore, if, for example, turning on the power to the device results in charge building on the floating node due to capacitive coupling, having previously turned off the power will not resolve any problems created by that charge that is induced on the floating node when the power is turned on. Therefore, in my opinion, turning off the power after fuse programming and prior to latch operation does not “solve” the problems mentioned in the background of the ’492 patent.

III. McADAMS DISCLOSES A “TERMINAL T1” AS RECITED IN THE CLAIMS

11. As I opined in my March 5, 2019 declaration, when the ordinary meaning of the term is applied, McAdams discloses “a terminal T1 for providing a signal indicating a state of the programmable latch.” (Ex. 1002 at ¶¶ 78-79.) It is also my opinion that McAdams discloses this claim feature even when ProMOS’s proposed construction is applied.

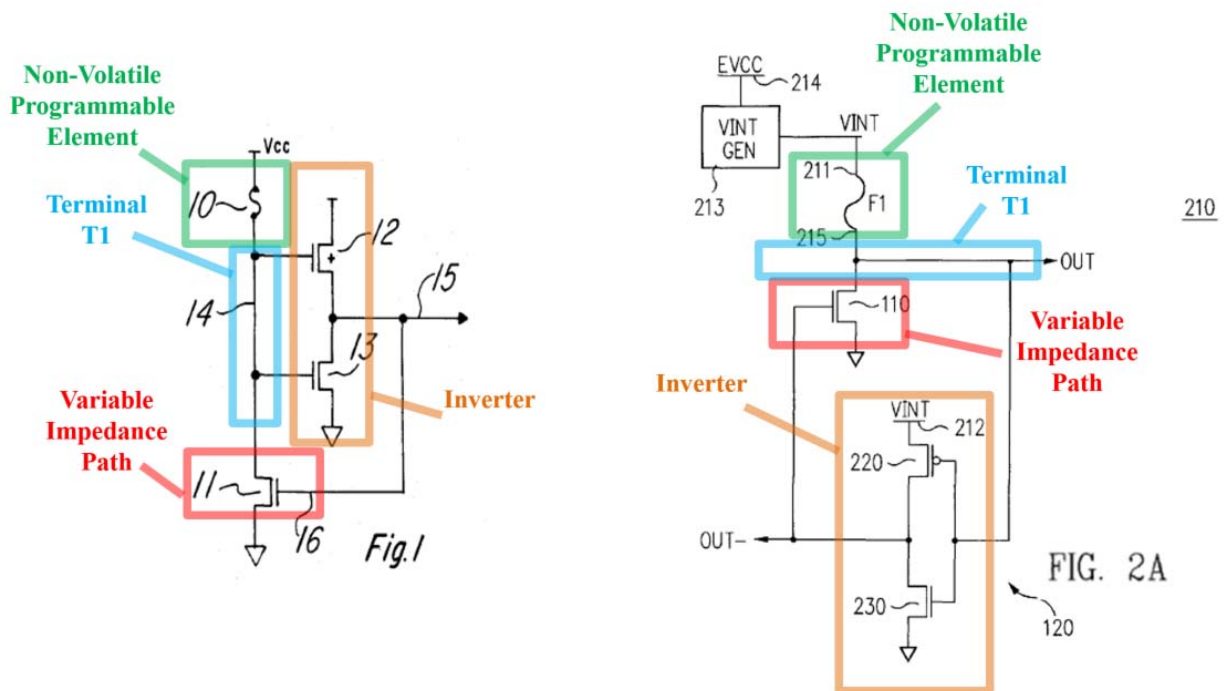
12. Mr. de la Iglesia asserts that McAdams does not disclose the operation of the latch disclosed and that “McAdams has no specific mechanism for dissipating all voltage at nodes 14 and 15.” (Ex. 2003 at ¶ 35.) Based on this, he asserts that

McAdams does not teach the “terminal T1” limitation. (*Id.*) I disagree with his analysis for at least the following reasons.

13. McAdams discloses a scenario in which, after fuse 10 has been blown (i.e., programmed), “Vcc is powered up.” (Ex. 1006 at 2:22-24.) A person of ordinary skill in the art would understand the “powering up” of Vcc to mean that Vcc starts at ground (0 volts), and then a voltage is applied to Vcc until it reaches the expected steady state value (e.g. 3.3 volts, 5 volts, etc.). In McAdams, as Vcc increases, the voltage at node 14 could increase due to “capacitive coupling” between node 14 and the Vcc terminal. (*Id.* at 2:26-29.) But McAdams discloses that any resulting voltage increase at node 14 due to capacitive coupling “is quickly discharged” via the drain of transistor 11 and node 14 “discharges to Vss” as a result. (*Id.* at 2:26-33.) The discharging of the voltage level at node 14 can occur, for example, as a result of leakage via the drain of transistor 11 connected with node 14. Indeed, this is the same mechanism by which terminal OUT discharges to ground voltage after fuse programming in the embodiment of the ’492 patent that does not include a diode.

14. As is apparent from the demonstrative I created below, a comparison of figure 2A of the ’492 patent (modified to remove the diode) and figure 1 of McAdams shows that there is no structural difference between terminal OUT in the ’492 patent and node 14 in McAdams. As can be seen in the figures below, each of

McAdams and the '492 patent show a terminal T1 (node 14, terminal OUT) that is connected to one end of a fuse (fuse 10, fuse F1), the gates of two transistors that form an inverter (transistors 12 and 13, transistors 212 and 230), and the drain of an NMOS transistor that constitutes the “variable impedance path” (transistor 11, transistor 110). (Ex. 1006 at FIG. 1; Ex. 1001 at FIG. 2A.) A person of ordinary skill in the art would have understood that because these circuits have the same structure, any charge that accumulates at the terminal OUT or node 14 could be dissipated in the same way with the same “mechanism.” For at least these reasons, it is my opinion that McAdams discloses that voltage dissipates from node 14 after fuse programming as is required by ProMOS’s proposed construction of the “terminal T1” limitation.



(Ex. 1006 at FIG. 1 (left) (annotated); Ex. 1001 at FIG. 2A (right) (annotated).)

15. A person of ordinary skill in the art would have understood that there is no structural difference between the latch recited in claim 14 and the latch disclosed in McAdams. All of the circuit elements recited in claim 14 are present in McAdams. For example, McAdams discloses node 14, which is a “terminal T1” as recited in claim 14, where node 14 is connected to a “a non-volatile programmable element” (fuse 10), a “variable impedance path” (NMOS transistor 11) and an inverter formed by PMOS transistor 12 and NMOS transistor 13. Turning power off to the latch does not constrain the structure of McAdams’ programmable latch. There is nothing special about the disclosed terminal T1 in the ’492 patent, and there is no “mechanism for dissipating voltage” attached to the terminal T1 in the relevant embodiment of the ’492 patent that is not also present in McAdams. Just like the ’492 patent, charge would leak/dissipate from node 14 via the drain of the NMOS transistor connected to node 14 of McAdams.

16. I understand that ProMOS argues that McAdams fails to disclose turning power off to the latch after programming the fuse. I disagree. McAdams explicitly discloses that Vcc is powered from zero to +5V both “if the fuse has not been blown” and “[if] the fuse 10 has been blown.” (Ex. 1006 at 2:8-11, 2:21-24.) In the latter scenario, McAdams discloses that the power to the latch is provided *after* the fuse 10 has been blown, thereby confirming that there is a period of time

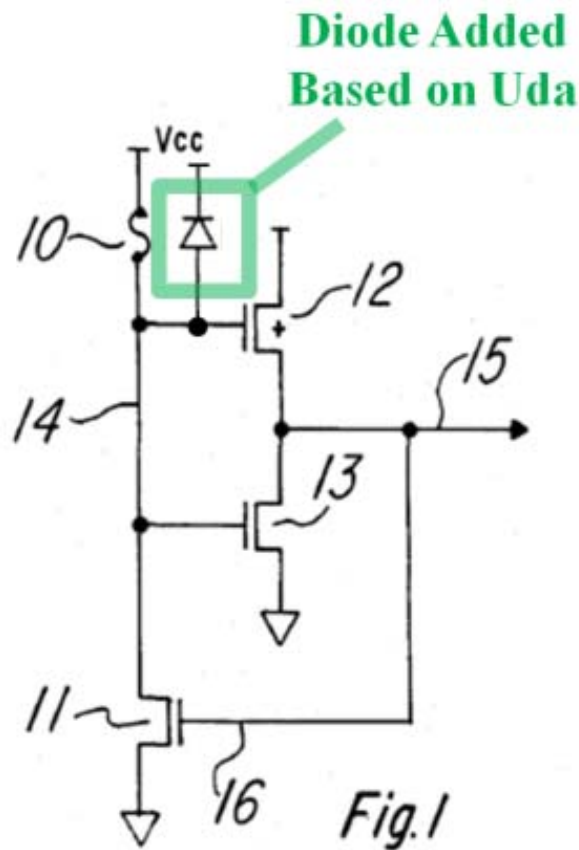
after programming of the fuse and before power is applied to the latch. (*Id.* at 2:21-24 (“If the fuse 10 has been blown, as Vcc is powered up”).)

17. A person of ordinary skill in the art would have understood that this makes sense because programming of the latch by blowing fuse 10 typically occurs during testing of memory device. After testing has been completed, the device is shipped to customers for use. During shipping there is no power applied to the latch. Thus, between testing and the ultimate use of the memory device by a customer, the power to the latch is necessarily turned off in McAdams. Later, power is resupplied to the latch when the memory device is used by the customer. This understanding is supported by the '492 patent, which states that fuses are typically programmed during testing and shipped to the customer with the power off. (Ex. 1001 at 5:57-62.)

18. I also understand that ProMOS and Mr. de la Iglesia assert that McAdams suffers from the same problem that is described the '492 patent. (Ex. 2003 at ¶ 35.) Specifically, I understand that ProMOS and Mr. de la Iglesia contend that McAdams does not allow the voltage at nodes 14 and 15 to dissipate to ground after programming, and therefore can suffer from a “false state” condition because there can be charge on nodes 14 and 15 at power up. (*Id.*) I disagree. McAdams is just like the '492 patent in that node 14 is at ground at power-up in the scenario where fuse 10 has been blown. (Ex. 1006 at 2:21-24.)

IV. A PERSON OF ORDINARY SKILL IN THE ART WOULD HAVE BEEN MOTIVATED TO COMBINE McADAMS AND UDA

19. As I demonstrated in my March 5, 2019 declaration, based on the disclosure of Uda, a person of ordinary skill in the art would have been motivated to include a diode in the programmable latch of McAdams (as shown below) in order to avoid damaging the gates of transistors 12 and 13. (Ex. 1002 at ¶¶ 89-115.)



(Ex. 1006 at FIG. 1 (annotated).)

20. Mr. de la Iglesia contends that a person of ordinary skill in the art would not combine the teachings of McAdams and Uda because “McAdams and Uda are

designed using different technologies.” (Ex. 2003 at ¶37.) Specifically, Mr. de la Iglesia states that the circuit of McAdams is implemented in CMOS, whereas Uda is implemented using a combination of ECL and CMOS. (*Id.*) Based on this, he concludes that the specific parasitic diodes formed in Uda “cannot be integrated into the CMOS process of McAdams.” (*Id.*) However, as Uda demonstrates, CMOS and ECL devices can coexist on an integrated circuit. Indeed, CMOS and ECL devices are often implemented together in order to provide the desired circuit characteristics (speed, drive strength, etc.) that are needed for a particular application.

21. For example, Uda explains that the same device (e.g., a memory like SRAM) can include devices made using both ECL and CMOS devices. (Ex. 1007 at 22:65-23:1 (“These switch circuits each include the combination of an ECL (emitter coupled logic) circuit with a CMOS . . . circuit forming part of the static RAM”).) For example, figure 4 of Uda shows a plan view of a semiconductor chip that includes SRAM (static random access memory) circuits that are made using BiCMOS (bipolar-complementary metal oxide semiconductor) technology, which combines bipolar transistors (such as those used in ECL) and CMOS transistors. (*Id.* at 9:1-7.) The semiconductor chip 7 shown in figure 4 includes memory circuit blocks with “memory cells made of MOS-FET’s” and backup memory cells that are redundant cells used to replace faulty cells. (*Id.* at 9:16-20.)

22. Figure 5 of Uda shows the fuse arrangement that is used to replace a defective cell with a corresponding backup memory cell. (*Id.* at 9:21-29.) The diodes D1, D2, and D3, which Mr. de la Iglesia describes as parasitic diodes constructed using a combination of ECL and CMOS, are connected to the gate of an NMOS transistor 17, which is a CMOS device:

Terminals T between the fuse 16 and the resistor R₁ are connected to a resistor R₂ and a diode D₃. In turn, the resistors R₁ and R₂ are connected to the ground line GND via diodes D₁ and D₂. The terminals T connected to the fuse 16 and resistor R₁ are further connected to the gate electrode of, for example, **an n-channel MOSFET (called nMOS) 17** via the resistor R₂.

The purpose of furnishing the diodes D₁ through D₃ and the resistor R₂ is to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the MOS gate. These components work as follows: If a positive charge develops, the charge is led to the ground line GND via the diodes D₁ and D₂; if a negative charge occurs, the charge is led to the power line V_{EE} via the diode D₃. Any residual charge loses its energy when entering the resistor R₂, **whereby the MOS gate is protected from destruction.**

(*Id.* at 9:37-53 (emphasis added).)

23. Uda further describes how the NMOS transistor 17, which is protected by the diodes, is used in the memory to replace faulty memory with its backup memory cell when the fuse 16 is cut. (*Id.* at 9:54-10:3.) As such, Uda supports the understanding that a person of ordinary skill in the art would have known that even if the diodes disclosed in figure 5 of Uda are implemented as ECL diodes, they could still be used on an integrated circuit that include CMOS devices as well.

24. Moreover, it is apparent that Mr. de la Iglesia misunderstands my position with respect to how a person of ordinary skill in the art would combine McAdams and Uda. I did not state in my March 5, 2019 declaration that a person of ordinary skill in the art would move the diode implemented in the particular manner disclosed in Uda into the circuit of McAdams. Instead, it is my opinion that a person of ordinary skill in the art would have recognized the functionality of a diode as disclosed in Uda in terms of the diode's role in protecting the gate of a CMOS device from damage due to charge buildup due to laser programming. In my opinion, a person of ordinary skill in the art would have applied that teaching to the circuit of McAdams in order to provide the same benefit in protecting the gates of transistors 12 and 13 that are included in the latch of McAdams.

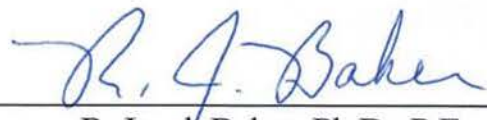
25. In the combination I discussed in my March 5, 2019 declaration, Uda is relied upon for its *teaching* that a diode can be used in circuits where fuses are programmed using a laser (like McAdams) in order to dissipate charge that

accumulates during such laser programming in order to prevent damage to transistors that are susceptible to such charge buildup. A person of ordinary skill in the art would have understood how to create a diode in the process used to form the programmable latch of McAdams and would have been capable of implementing such a diode in that process. Indeed, a diode is a very simple circuit element. The precise diode structure of Uda, including the materials used to construct it, need not be incorporated into McAdams as Mr. de la Iglesia suggests.

V. CONCLUSION

26. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 6, 2020



R. Jacob Baker, Ph.D., P.E.