

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES INC.
Patent Owner

Case: IPR2019-00780
U.S. Patent No. 6,163,492

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I. INTRODUCTION	1
II. CLAIM CONSTRUCTION.....	3
A. The Claims Do Not Support ProMOS’s Construction.....	4
B. The Specification Does Not Support ProMOS’s Construction.....	7
C. ProMOS’s Assertion That Claim 1 Includes Two Solutions Is Unsupported	12
III. THE PRIOR ART RENDERS CLAIMS 1-13 UNPATENTABLE.....	13
A. McAdams Discloses “A Terminal T1 For Providing A Signal Indicating A State Of The Programmable Latch”.....	13
1. McAdams Discloses the Claimed “Terminal T1” Under the Term’s Ordinary and Customary Meaning.....	13
2. McAdams Discloses the Claimed “Terminal T1” Under ProMOS’s Construction.....	14
B. A POSITA Would Have Found It Obvious to Combine McAdams and Uda.....	19
IV. CONCLUSION	25

TABLE OF AUTHORITIES**Page(s)****Cases**

<i>Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC</i> , 825 F.3d 1373 (Fed. Cir. 2016.)	23
<i>E-Pass Techs., Inc. v. 3COM Corp.</i> , 343 F.3d 1364 (Fed. Cir. 2003)	9
<i>Hewlett-Packard Co. v. Bausch & Lomb Inc.</i> , 909 F.2d 1464 (Fed. Cir. 1990)	18
<i>Homeland Housewares, LLC v. Whirlpool Corp.</i> , 865 F.3d 1372 (Fed. Cir. 2017)	4, 5
<i>Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.</i> , 540 F.3d 1337 (Fed. Cir. 2008)	9
<i>InterDigital Commc'ns, LLC v. Int'l Trade Comm'n</i> , 690 F.3d 1318 (Fed. Cir. 2012)	6
<i>Iridescent Networks, Inc. v. AT&T Mobility, LLC</i> , 933 F.3d 1345 (Fed. Cir. 2019)	4
<i>In re Nievelt</i> , 482 F. 2d 965 (CCPA 1973)	23
<i>ParkerVision, Inc. v. Qualcomm Inc.</i> , 903 F.3d 1354 (Fed. Cir. 2018)	18
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (en banc)	5, 6, 8
<i>Samsung Electronics, Co., Ltd. v. ProMOS Technologies, Inc.</i> , IPR2017-00040, Paper No. 41 (Mar. 21, 2018)	23
<i>In re Sneed</i> , 710 F. 2d 1544 (Fed. Cir. 1983)	23
<i>Thorner v. Sony Comput. Entm't Am. LLC</i> , 669 F.3d 1362 (Fed. Cir. 2012)	6, 7

<i>WesternGeco LLC v. PGS Geophysical AS,</i> IPR2015-00313, Paper No. 44 (Feb. 3, 2017)	8
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LIST OF EXHIBITS

Exhibit No.	Description	Previously Submitted
1001	U.S. Patent No. 6,163,492	X
1002	Declaration of R. Jacob Baker, Ph.D., P.E.	X
1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.	X
1004	Prosecution History of U.S. Patent No. 6,163,492	X
1005	RESERVED	
1006	U.S. Patent No. 4,621,346 (“McAdams”)	X
1007	U.S. Patent No. 5,519,658 (“Uda”)	X
1008	U.S. Patent No. 5,552,739 (“Keeth”)	X
1009	Neil Weste <i>et al.</i> , <u>Principles of CMOS VLSI Design: A Systems Perspective</u> , 2d. ed. 1993 (“Weste”)	X
1010	RESERVED	
1011	RESERVED	
1012	U.S. Patent No. 5,592,121 (“Jung”)	X
1013	U.S. Patent No. 5,604,710 (“Tomishima”)	X
1014	Neil Weste and Kamran Eshraghian, <u>Principles of CMOS VLSI Design: A Systems Perspective</u> , 2d. ed. 1993, including cover, series title page, title page, copyright page, about the author page, preface, table of contents, last numbered page, back cover, and spine	X
1015	Taur <i>et al.</i> , <u>Fundamentals of Modern VLSI Devices</u> , 2009 (“Taur”)	X
1016	Declaration of Ingrid Hsieh-Yee, Ph.D.	X
1017	Transcript of Deposition of Mr. Erik de la Inglesia	
1018	Rebuttal Declaration of R. Jacob Baker, Ph.D., P.E.	

Exhibit No.	Description	Previously Submitted
1019	<i>Samsung Electronics, Co., Ltd. v. ProMOS Technologies, Inc.</i> , IPR2019-00779, Paper No. 7 (Sep. 11, 2019)	

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) submits this Reply concerning claims 1-13 of U.S. Patent No. 6,163,492 (“the ’492 Patent”) (Ex. 1001). ProMOS Technologies, Inc.’s (“ProMOS”) arguments should be rejected and the claims found unpatentable for at least the reasons set forth in the Petition (Paper No. 1) and accompanying exhibits, the Board’s decision to institute *inter partes* review (“Decision”) (Paper No. 6), cross-examination testimony, and the additional reasons below.

In its Response (Paper No. 9), ProMOS makes two arguments. First, ProMOS contends that McAdams (Ex. 1006) does not disclose “a terminal T1 for providing a signal indicating a state of the programmable latch” based on a proposed construction of this limitation. Specifically, ProMOS seeks to construe this term as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” But ProMOS’s arguments in support of this construction conflict with black-letter claim construction law, which prohibits reading limitations from the specification into the claims and limiting claims beyond their ordinary meaning to achieve a perceived purpose of the invention. For instance, ProMOS fails to identify any disclaimer, disavowal, or definition in the specification or file history that would justify limiting the term beyond its ordinary and customary meaning. ProMOS’s arguments that the

proposed construction is consistent with solving the problems posited in the background section are legally insufficient to justify the construction and technically incorrect. The drafter of claim 1 chose broad language, and ProMOS cannot selectively narrow claim 1 at this stage to avoid unpatentability. In any event, even if ProMOS's construction were adopted, McAdams discloses the disputed limitation because McAdams explicitly discloses dissipating voltage from node 14, which is the claimed "terminal T1," as required by ProMOS's construction.

Second, ProMOS contends that a person of ordinary skill would not have combined the teachings of McAdams and Uda (Ex. 1007) because the combination would require combining Uda's diode, which is made using ECL technology, with McAdams's circuit, which involves CMOS technology. This argument fails for two reasons. First, Uda itself demonstrates that a POSITA could combine ECL and CMOS devices on the same integrated circuit. Second, ProMOS's argument is premised on a fundamental misunderstanding of Samsung's proposed combination. Specifically, even though Samsung's combination involves including *a* diode (not a particular type of diode) in McAdams' circuit in view of Uda's broad teaching that the use of a diode can prevent circuit damage due to charge accumulation, ProMOS incorrectly presumes that the combination involves *bodily incorporation* of Uda's diode into the latch circuit of McAdams. But as is well-settled, obviousness does not require bodily incorporation of the teachings of one reference into another.

The record supports the instituted grounds, and the Board should find each of the challenged claims unpatentable and cancel them.¹

II. CLAIM CONSTRUCTION

ProMOS seeks to construe “a terminal T1 for providing a signal indicating a state of the programmable latch” as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” (Response, 8-11.) This construction should be rejected because it is untethered to the plain language of claim 1 and seeks to limit claim 1 to one aspect of an exemplary embodiment of the specification even though nothing in the intrinsic evidence compels limiting the claim in such a manner.²

¹ Patent Owner offers certain background for the '492 patent on pages 3-7 of the Response. Petitioner does not acquiesce to any statements in those pages. In any event, Petitioner addresses them in the appropriate sections in this paper to the extent the statements are relevant to the issues here.

² Claim 14 of the '492 patent also recites the same limitation. (*See* Ex. 1001, 10:7-8.) In a parallel IPR proceeding (IPR2019-00789) involving claim 14 of the '492 patent, the Board preliminary rejected ProMOS's construction. (Ex. 1019, 8-10.)

A. The Claims Do Not Support ProMOS's Construction

The starting point for any claim construction analysis is the language of the claims. *See Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1375 (Fed. Cir. 2017); *Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1350 (Fed. Cir. 2019) (“We begin with the language of the claims.”) ProMOS’s analysis, however, simply ignores the language of the claims. As is evident from the claim itself, the “terminal T1” limitation simply requires a terminal capable of providing a signal that indicates the state of the programmable latch, which is also the ordinary and customary meaning of this claim term. (Ex. 1018, ¶¶3-4.) ProMOS’s construction conflicts with the claim language as it attempts to add an unclaimed limitation (“from which voltage is dissipated after programming”) to the “terminal T1” limitation.³ Here, no further construction beyond the ordinary

³ ProMOS’s proposed construction is odd to say the least. Claim 1 is an apparatus claim; thus it can only be distinguished from the prior art based on the recited structure, not the intended use or manner of operation of the structure. Yet, ProMOS seeks to constrain a simple structural element of the apparatus claim—a “terminal T1”—by its manner of operation. For instance, ProMOS does not seek a construction that limits the *structure* of “terminal T1”; instead, ProMOS seeks to

meaning is necessary because when the “ordinary meaning of [a] claim [is] readily apparent,” like here, “claim construction will involve little more than the application of the widely accepted meaning of commonly understood words.” *Homeland Housewares, LLC*, 865 F.3d at 1375 (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-14 (Fed. Cir. 2005) (en banc)).

Moreover, other limitations in claim 1 counsel against ProMOS’s construction. For example, claim 1 recites a diode that “keep[s] a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch.” (Ex. 1001, 8:55-57.) Thus, claim 1 explicitly defines what happens to the voltage at terminal T1—it is kept within a predetermined range of values. (Ex. 1018, ¶5.) If patentee wished to further define the voltage at terminal T1 in claim 1, as ProMOS’s construction proposes to do, patentee would have done so. Instead, patentee recited the claimed “terminal T1” in broad terms, and patentee’s choice of words should be given its full effect. Moreover, the claimed diode, which “prevent[s] the latch from assuming an incorrect state when power is supplied to the latch” (Ex. 1001, 8:55-58) undercuts ProMOS’s argument that its construction is

define the terminal by how it operates or functions (a terminal “from which voltage is dissipated after programming”).

required to ensure that terminal T1 does not indicate an incorrect state at power-up.
(Response, 9.)

As discussed above, the plain language of claim 1 and the diode limitation recited therein demonstrates the fallacy in ProMOS's construction. The "terminal T1" limitation should therefore be given its ordinary and customary meaning. Indeed, the "case law is clear, claim terms must be given their plain and ordinary meaning to one of skill in the art." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) (citing *Phillips*, 415 F.3d at 1316). Deviation from the ordinary meaning is proper in only two circumstances: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner*, 669 F.3d. at 1365 (internal citation omitted); *InterDigital Commc'ns, LLC v. Int'l Trade Comm'n*, 690 F.3d 1318, 1324 (Fed. Cir. 2012) ("the plain meaning of claim language ordinarily controls unless the patentee acts as his own lexicographer and provides a special definition for a particular claim term or the patentee disavows the ordinary scope of a claim term either in the specification or during prosecution") (citing *Phillips*, 415 F.3d at 1312-13). But, as explained below, ProMOS can point to no such definition or disavowal in the specification or the prosecution history that can compel its construction.

B. The Specification Does Not Support ProMOS's Construction

ProMOS does not contend that the specification defines or disavows the full scope of the “terminal T1” limitation. (Response, 8-11.) By itself, that renders irrelevant all of ProMOS's arguments regarding what the specification allegedly shows. *Thorner*, 669 F.3d at 1365 (holding that claim terms are afforded their plain and ordinary meaning in the absence of definition or disavowal). In any event and as explained below, ProMOS's arguments are without merit.

ProMOS first urges that its construction is supported by the specification of the '492 patent because in an exemplary embodiment (specifically, the one without the diode), terminal OUT is “at ground before power-up” and, per ProMOS, such grounding of the terminal OUT before power-up is necessary to achieve a correct state of the programmable latch. (Response, 10-11.) According to ProMOS, in this embodiment, the power is turned off after programming of the fuse and “any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated.” (*Id.*, citing Ex. 1001, 5:51-6:8.) None of this, however, is sufficient to limit the claim beyond its ordinary meaning.

As the Board correctly recognized in IPR2019-00779, ProMOS is asking “to import into the claim a requirement that terminal T1 be at ground voltage where one does not currently exist” and while an embodiment may have the terminal OUT at ground at power-up, “it is important not to import into a claim limitations that are

not part of the claim.” (Ex. 1019, 10.) Indeed, “[a]bsent a clear, deliberate, and precise definition, it is one of the ‘cardinal sins’ of patent law to import limitations from an embodiment in the specification into the claims.” *WesternGeco LLC v. PGS Geophysical AS*, IPR2015-00313, Paper No. 44 at 8 (Feb. 3, 2017) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1320 (Fed. Cir. 2005) (en banc)). Here, the statements to which ProMOS points merely reflect the operation of an exemplary embodiment and in no way serve to define the claimed “terminal” as “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” In fact, the ’492 patent recognizes that terminal OUT need not be at ground at power-up for the latch to indicate the correct state at power-up. (Ex. 1001, 2:51-55; Ex. 1018, ¶¶6-7.) Indeed, the ’492 patent explains and also *claims* techniques (e.g., increasing the trip point of the inverter connected to terminal OUT and/or decreasing the threshold voltage of the variable-impedance path connected to terminal OUT) that ensure proper latch operation without the need for ensuring that terminal OUT is at ground before power-up. (Ex. 1018, ¶¶6-7 (citing Ex. 1001, 6:8-32, claims 20 and 21).)

Lacking anything concrete in the specification that can serve as a definition or disclaimer, ProMOS turns to generalities arguing that its construction should be accepted because “the entire purpose of the invention is to eliminate the risk of a false output because of excess voltage at T1 accumulated from programming or from

capacitive coupling at the output” and “[i]f this voltage is not dissipated after programming, then the terminal T1 . . . may indicate a false state due to this programming voltage.” (Response, 10.) As explained above, the ’492 patent itself recognizes that dissipation of voltage from terminal T1 is not necessary for proper latch operation because it states that the latch can indicate the correct state even if the terminal T1 is not at ground at power-up. ProMOS’s argument is thus meritless for this and other reasons discussed below.

First, it is black-letter law that a claim will not be limited beyond its ordinary meaning in order to ensure that it serves “a perceived ‘purpose’ of the invention.” *Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1345 (Fed. Cir. 2008) (quoting *E-Pass Techs., Inc. v. 3COM Corp.*, 343 F.3d 1364, 1370 (Fed. Cir. 2003)).

Second, if the purpose of the invention, as ProMOS says, is to prevent the latch from assuming an incorrect state at power-up, other limitations recited in claim 1 of the ’492 patent already serve that purpose. Specifically, claim 1 explicitly recites a diode that “prevent[s] the latch from assuming an incorrect state when power is supplied to the latch.” (Ex. 1001, 8:55-58.) As acknowledged by ProMOS’s declarant, the claimed diode refers to diode 234 in figure 2A of the ’492 patent and diode 234 serves the purpose of dissipating voltage and preventing the latch from having a false state when power is applied to the latch after fuse

programming. (Ex. 1017, 47:11-48:12; Ex. 1018, ¶9; Ex. 1001, FIG. 2A, 3:33-49; *see also* Response, 5-6 (explaining that the diode solves the problems identified in the background of the '492 patent).) Thus, ProMOS is wrong that for claim 1 to accomplish the purpose of the invention, claim 1 must be limited in the manner ProMOS proposes.

Third, ProMOS's proposed construction should be rejected because, even though claim 1 is an *apparatus* claim, ProMOS omits from its construction any *structural* aspects that presumably solve the problems ProMOS alleges are addressed by the '492 patent. Specifically, ProMOS alleges that by simply turning off the power to the latch after blowing the fuse, the '492 patent solves the false state problem. (Response, 9-10.) But turning power off after programming is not included in ProMOS's construction. Nor does ProMOS explain how turning off the latch's power places any structural limitation on the claimed "terminal T1." In contrast to the diode limitation, which further defines the latch's structure, turning power off to the latch is a manner of operating the latch that adds no further structural limitation to the claimed "terminal T1."

Fourth, ProMOS's argument that turning off the power to the latch after fuse programming would solve the problems identified in the background of the '492 is technically incorrect. (Ex. 1018, ¶¶8-10.) ProMOS explains that the false state problem occurs in the prior art because terminal OUT is "floating" when power is

off or becomes unstable due to capacitive coupling during power up. (Response, 5-6, 10.) Per ProMOS, turning power off to the latch after programming resolves these issues. (*Id.*) But merely turning off the power to the latch does not prevent the terminal OUT from floating or from suffering from capacitive coupling. (Ex. 1018, ¶¶8-10.) To prevent terminal OUT from floating and suffering from capacitive coupling, a physical structure (e.g., a diode) is required. (*Id.*, ¶¶9-10.) Simply put, contrary to ProMOS’s assertions, turning off the power after fuse programming and prior to latch operation does not “solve” the problems posited in the background of the ’492 patent.⁴

⁴ ProMOS alleges that “[t]he background of the ’492 patent explains that the entire purpose of the invention is to eliminate the risk of a false output because of **excess voltage at T1 accumulated from programming** or from capacitive coupling at the output.” (Response, 10 (citing Ex. 1001 at 1:46-48, 1:38-47) (emphasis added); Ex. 2003, ¶29.) But the cited passages in the background of the ’492 patent do not indicate that excess voltage resulting **from programming** is the problem, and instead indicate the problem is that the “terminal OUT is floating”—a problem not solved by simply turning off the power after programming. (Ex. 1018, ¶8.)

ProMOS's argument that the specification compels its construction thus fails for the above reasons.

C. ProMOS's Assertion That Claim 1 Includes Two Solutions Is Unsupported

In rejecting ProMOS's construction in IPR2019-00779, the Board noted that claim 1, like claim 14, recites "a terminal T1 for providing a signal indicating a state of the programmable latch." (Ex. 1019, 8-9.) ProMOS criticizes the Board for assuming "that ProMOS was arguing for [] different constructions for the relevant term in the two different claims." (Response, 8.) But in this proceeding ProMOS did not file a preliminary response, thereby suggesting to the Board that construction of the term was not appropriate for claim 1 and the ordinary meaning of the term should apply.

ProMOS now states that it is not asking for different constructions and alleges that "[c]laim 1 addresses the stated 'false state' problem with two solutions – a diode and 'a terminal T1 from which voltage is dissipated after programming . . .'" (*Id.*, 8-9.) ProMOS's argument fails for at least two reasons. First, ProMOS provides no explanation why claim 1 recites two solutions when each of those two solutions standing alone resolves the "false state" problem. Second, if ProMOS's argument were true that claim 1 recites "two" distinct solutions to the "false state" problem, then claim 1 would be invalid for lack of written description support. This is because there is no embodiment in the '492 specification having both solutions. Specifically,

the only support for the first solution (turning off power to the latch) is an embodiment in which the diode is omitted. (Ex. 1019, 8 (“Patent Owner’s proposed construction, however, is limited to a described embodiment of the programmable latch that does not have a diode, and claim 1 requires the presence of a diode.”).) ProMOS’s arguments thus fail for this additional reason.

III. THE PRIOR ART RENDERS CLAIMS 1-13 UNPATENTABLE

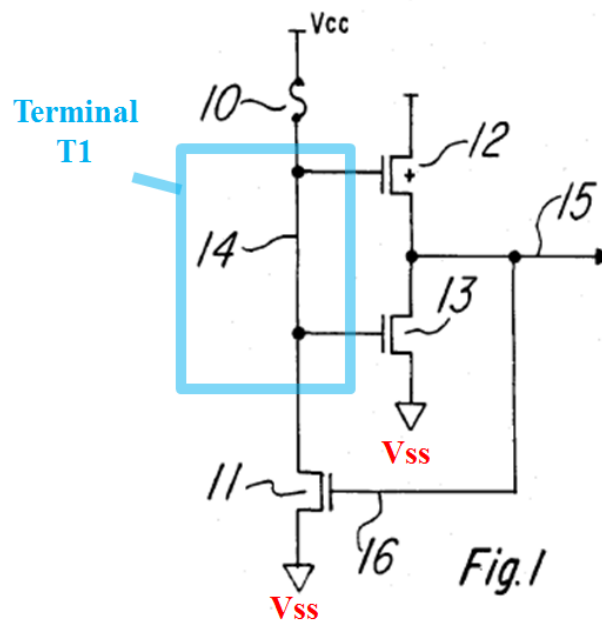
A. McAdams Discloses “A Terminal T1 For Providing A Signal Indicating A State Of The Programmable Latch”

Premised on its faulty construction, ProMOS contends that McAdams fails to disclose the claimed “terminal T1.” (Response, 15-16.) But that construction should be rejected and the claim term given its ordinary and customary meaning. (*See supra* Section II.) When the ordinary meaning is applied, there is no dispute that McAdams discloses the claimed “terminal T1.” Moreover, even if ProMOS’s faulty construction were adopted, McAdams discloses the claimed “terminal T1” as explained in detail below.

1. McAdams Discloses the Claimed “Terminal T1” Under the Term’s Ordinary and Customary Meaning

Claim 14 recites, *inter alia*, “a terminal T1 for providing a signal indicating a state of the programmable latch.” (Ex. 1001, 10:7-8.) Figure 1 of McAdams discloses a programmable latch and node 14 in that latch corresponds to the claimed “terminal T1.” (Petition, 18-20; Ex. 1002, ¶¶78-79.) If the fuse is intact, node 14 is at Vcc (high), but if the fuse is blown, node 14 is at Vss (low). (Ex. 1006, 2:8-24.)

Therefore, the voltage at node 14 provides a signal indicating a “state of the programmable latch” because the voltage at node 14 indicates whether the fuse is blown or not. (Petition, 18; Ex. 1002, ¶78.) Thus, McAdams discloses “a terminal T1 for providing a signal indicating a state of the programmable latch” when the term is given its ordinary and customary meaning.



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶78.)

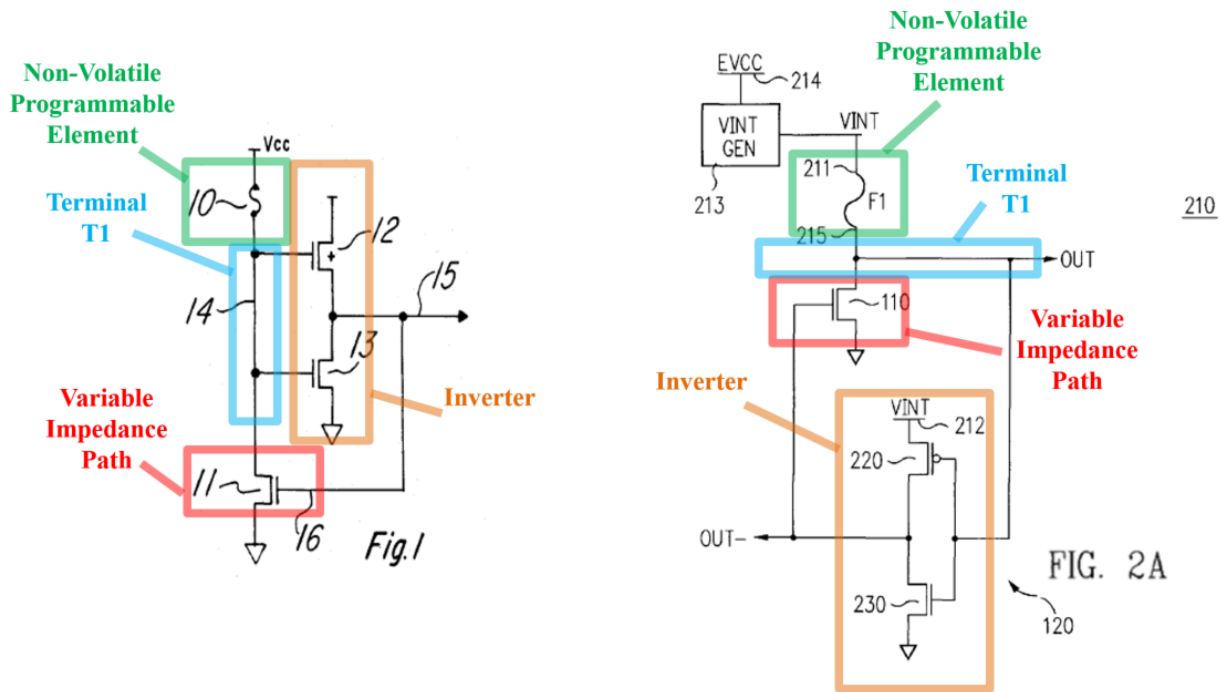
2. McAdams Discloses the Claimed “Terminal T1” Under ProMOS’s Construction

ProMOS’s construction requires “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” (Response, 8.) As discussed above (*supra* Section III.A.1), node 14 in figure 1 of McAdams corresponds to the claimed “terminal T1.” ProMOS does not contest that node 14 provides a signal indicating a state of the

programmable latch. (Response, 15-16.) Instead, ProMOS contends that “voltage [is not] dissipated after programming” from node 14, as required by ProMOS’s construction. (*Id.*, 16 (“McAdams does not state that voltage that accumulates on nodes 14 and 15 is dissipated after programming.”).) ProMOS’s declarant parrots this assertion without any further analysis. (See Ex. 2003, ¶35.) Contrary to ProMOS’s argument, McAdams explicitly discloses voltage dissipation from node 14 after fuse programming. (Ex. 1018, ¶¶11-18.)

In particular, McAdams discloses a scenario in which, after fuse 10 has been blown (i.e., programmed), “Vcc is powered up.” (Ex. 1006, 2:22-24; Ex. 1018, ¶13.) As Vcc increases, the voltage at node 14 could increase due to “capacitive coupling” between node 14 and the Vcc terminal. (Ex. 1006, 2:26-29; Ex. 1018, ¶13.) But McAdams discloses that any resulting voltage increase at node 14 due to capacitive coupling “is quickly discharged” via the drain of transistor 11 and node 14 “discharges to Vss” as a result. (Ex. 1006, 2:26-33; Ex. 1018, ¶13.) As explained by Dr. Baker, leakage via the drain of transistor 11 connected with node 14 is the same mechanism by which terminal OUT discharges to ground voltage after fuse programming in the embodiment of the ’492 patent that does not include a diode. (Ex. 1018, ¶13.) Indeed, as apparent from the demonstrative below, a comparison of figure 2A of the ’492 patent (modified to remove the diode) and figure 1 of McAdams shows that there is no structural difference between terminal OUT in the

'492 patent and node 14 in McAdams. (Ex. 1018, ¶¶14-15.) Thus, voltage must dissipate from node 14 in McAdams' circuit for the same reasons as it does in the '492 patent embodiment without the diode.



(Ex. 1006, FIG. 1 (left) (annotated); Ex. 1001, FIG. 2A (right) (annotated); Ex. 1018, ¶14.)

ProMOS's other arguments, for example that McAdams is "silent about" *turning power off after programming* (Response, 15-16), are simply irrelevant because they are not tied to the plain language of ProMOS's proposed construction, which merely requires voltage dissipation from terminal T1 after fuse programming. In any event, these arguments lack merit.

First, ProMOS's assertion that McAdams fails to disclose turning power off to the latch after programming the fuse is demonstrably false. McAdams explicitly

discloses that Vcc is powered from zero to +5V under both conditions: “if the fuse has not been blown” and “[if] the fuse 10 has been blown.” (Ex. 1006, 2:8-11, 2:21-24; Ex. 1018, ¶16.) With respect to the second scenario, McAdams discloses that the power to the latch is provided *after* the fuse 10 has been blown, thereby confirming that there is a period of time after programming of the fuse and before power is applied to the latch. (Ex. 1006, 2:21-24 (“If the fuse 10 has been blown, as Vcc is powered up”); Ex. 1018, ¶16.) This makes sense because programming of the latch by blowing fuse 10 typically occurs during testing of memory device following which the device is shipped to customers for use. (Ex. 1018, ¶17.) Of course, during shipping no power is applied to the latch. (*Id.*) Thus, between the testing and ultimate use of the memory device by the customer, the power to the latch is necessarily turned off in McAdams and power is resupplied to the latch when the memory device is used by the customer. (*Id.*; *see also* Ex. 1001, 5:57-62 (admitting that fuses in a memory device are blown as part of testing and the memory then shipped to the customer with device power being off).)

Second, ProMOS’s assertion that McAdams suffers from the same problem that the ’492 patent addresses is again false. (Ex. 2003, ¶35.) ProMOS contends that the ’492 patent solves the “false state” problem by ensuring that terminal OUT is at ground before power-up. (Response, 9-10; *see also* Ex. 1019, 10 (recognizing that ProMOS relies on the embodiment in which terminal OUT is at ground at

power-up).) But McAdams is just like the '492 patent in that node 14 is at ground at power-up in the scenario where fuse 10 has been blown. (Ex. 1006, 2:21-24; Ex. 1018, ¶18.)

Third, and most importantly, each of ProMOS's arguments fails because ProMOS cannot show that there is any *structural* difference between the elements recited in claim 14 and those shown in figure 1 of McAdams. It is well-settled that an apparatus claim, like claim 14, can only be distinguished over the prior art based on its structure. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d1464, 1468 (Fed. Cir. 1990) ("Apparatus claims cover what a device is, not what a device does."); *ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018) ("A prior art reference may anticipate or render obvious an apparatus claim—depending on the claim language—if the reference discloses an apparatus that is reasonably capable of operating so as to meet the claim limitations, even if it does not meet the claim limitations in all modes of operation.") None of ProMOS's arguments attempt to distinguish claim 14 from figure 1 of McAdams based on any claimed structural features.

For instance, ProMOS's arguments that the power is not turned off to the latch after programming or that voltage is not dissipated from node 14 after programming relate to the *manner of operating the latch*; they do not constrain the structure of the latch. (Ex. 1018, ¶15.) Indeed, as acknowledged by ProMOS's declarant, McAdams

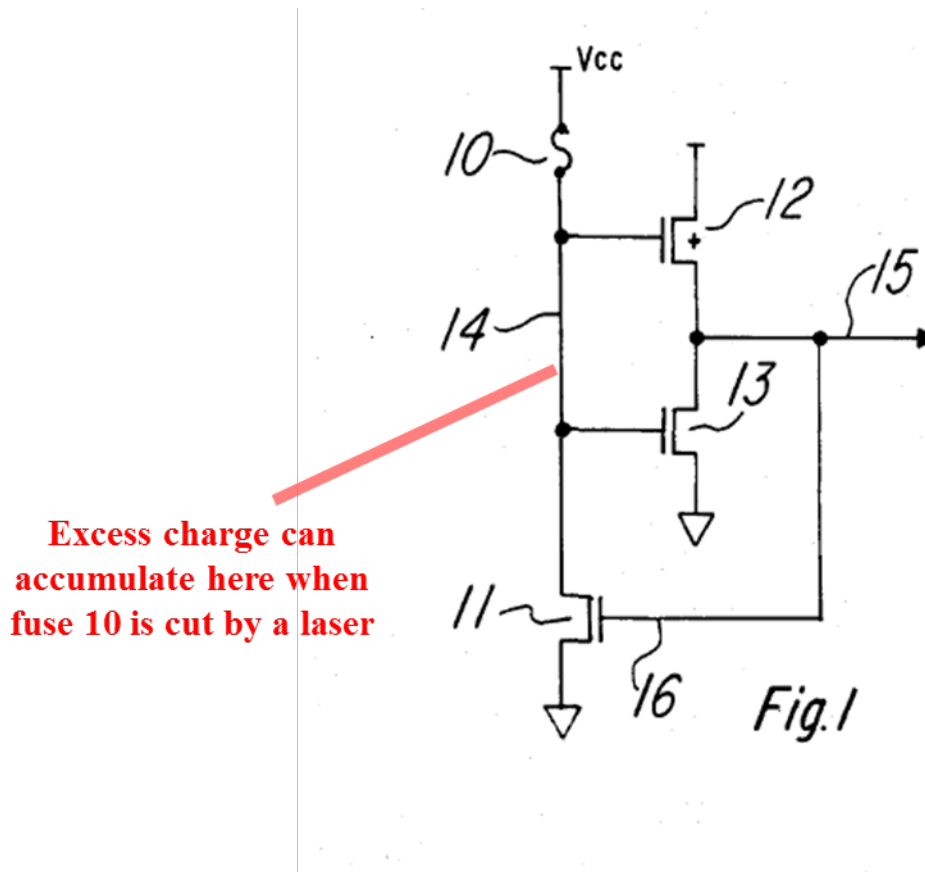
discloses all structural aspects of the disputed claim limitation — “terminal T1” (e.g., node 14 is a terminal and it is connected to “a non-volatile programmable element,” a “variable impedance path,” and an inverter). (Ex. 1017, 135:14-20, 136:9-137:5.) There is nothing special about the disclosed terminal T1 in the ’492 patent, and there is no “mechanism for dissipating voltage” attached to the terminal T1 in the relevant embodiment of the ’492 patent that is not also present in McAdams. (Ex. 1017, 96:16-97:3; Ex. 1018, ¶15.) As discussed above, just like the ’492 patent, charge would leak/dissipate from node 14 via the drain of the NMOS transistor connected to node 14.

For all of the above reasons, McAdams discloses the claimed “terminal T1” even under ProMOS’s erroneous construction.

B. A POSITA Would Have Found It Obvious to Combine McAdams and Uda

In the Institution Decision, the Board was persuaded that Samsung’s analysis of McAdams and Uda, including the motivation to combine their teachings, was “sufficient to establish a reasonable likelihood that the subject matter of independent claim 1 would have been obvious” (Decision, 11-14.) For instance, the Board acknowledged the testimony of Dr. Baker, Samsung’s expert, that excess charge could accumulate at node 14 in McAdams circuit when fuse 10 is blown. (*Id.*, 12 (citing Ex. 1002, ¶¶92-94).) The Board further acknowledged Dr. Baker’s testimony that if this excess charge is not removed, the gates of transistors 12 and 13 in

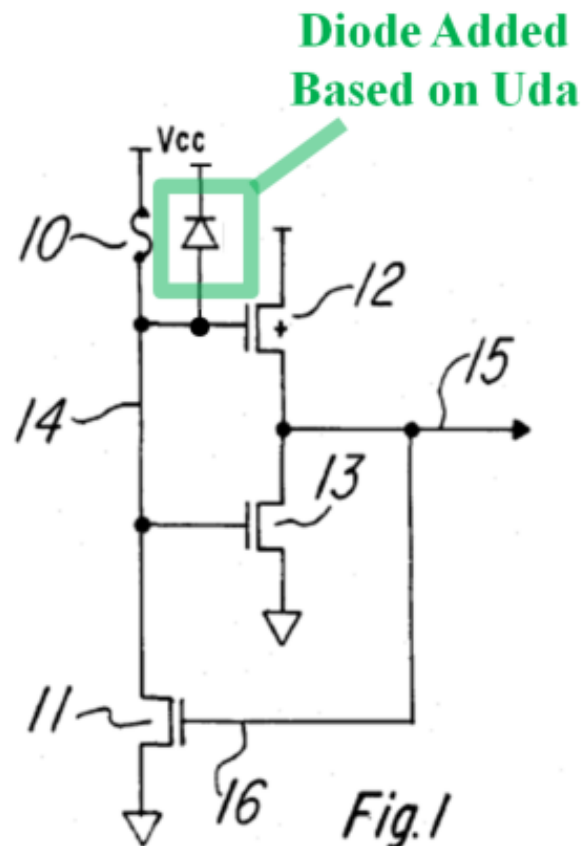
McAdams could be damaged. (Decision, 12 (citing Ex. 1002, ¶94).)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶94.)

The Board acknowledged Dr. Baker's testimony that Uda, a reference that "like McAdams, is in the field of semiconductor integrated devices, including redundancy circuits for memory devices that use fuses to enable such redundancy circuits," teaches the use of a diode to solve this problem of gate damage due to charge accumulation. (Decision, 12-13.) The Board then preliminarily agreed with Dr. Baker's detailed testimony that including a diode connected between node 14 and Vcc in McAdams latch, like in Uda, would solve this problem and prevent potential damage to the gates of transistors 12 and 13 because the diode would limit

the voltage at node 14 by dissipating the accumulated charge at node 14 to the Vcc terminal. (*Id.*, 13-14 (citing Ex. 1002, ¶¶95-103); *see also* Ex. 1002, ¶104.) The Board further preliminarily agreed with Dr. Baker that modifying McAdams' circuit to include a diode connected between node 14 and Vcc would have been within the capability of a POSITA. (*Id.*; Ex. 1002, ¶104.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶95.)

ProMOS does not dispute any of the above findings. For instance, ProMOS does not dispute that excess charge could accumulate at node 14 in McAdams, that such accumulation could damage the gates of transistors 12 and 13, and that

providing a diode connected between node 14 and Vcc would prevent this damage by limiting the voltage at node 14. (Response, 16-20.) Nor does ProMOS contest that a POSITA would have been capable of modifying McAdams' circuit to include a diode connected in the manner proposed by Dr. Baker. (*Id.*)

Instead, ProMOS contends that a POSITA would not have been able to combine the teachings of McAdams and Uda because the references disclose “fundamentally different process technolog[ies].” (Response, 2, 16-20.) Specifically, ProMOS contends that a “person of ordinary skill would not move the Uda diode to McAdams” because Uda’s diode is fabricated using “ECL logic” that is allegedly incompatible with the “CMOS technology used in McAdams.” (*Id.*, 18-20.) ProMOS’s argument fails for several reasons.

First, Uda itself demonstrates the fallacy in ProMOS’s argument because it combines ECL and CMOS circuit elements in figure 5, which is the circuit that Samsung relied upon in the petition. (Ex. 1007, FIG. 5; Petition, 25-27.) Specifically, figure 5 shows the diodes connected to the gate of an NMOS transistor 17, which ProMOS does not dispute is fabricated using CMOS technology. (Ex. 1007, FIG. 5; Ex. 2004, 49:20-50:9; Ex. 1018, ¶22.) Indeed, Uda repeatedly explains that the same device (e.g., a memory like SRAM) can include devices made using both ECL and CMOS devices. (Ex. 1007, 22:65-23:1 (“These switch circuits each

include the combination of an ECL (emitter coupled logic) circuit with a CMOS . . . circuit forming part of the static RAM”); Ex. 1018, ¶¶20-23.)

Second, ProMOS’s argument fails as a matter of law because it incorrectly presumes that Samsung had to demonstrate that a POSITA could *physically combine* the teachings of McAdams and Uda. (See Ex. 1017, 166:25-167:14.) As is well-settled, the “test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference but rather whether a skilled artisan would have been motivated to combine the teaching of the prior art references to achieve the claimed invention.” See *Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016.) Indeed, ProMOS’s argument that “[t]he Uda diode and McAdams circuit are so different that a person would not be motivated to combine them” and “[a] person of ordinary skill in the art would not move the Uda diode to McAdams because they are not technically compatible” is legally misplaced. “Physical incompatibility of specific disclosed parts between two references is essentially inconsequential.” *Samsung Electronics, Co., Ltd. v. ProMOS Technologies, Inc.*, IPR2017-00040, Paper No. 41 at 36 (Mar. 21, 2018) (citing *In re Sneed*, 710 F. 2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”), *In re Nievelt*, 482 F. 2d 965, 968 (CCPA 1973) (“Combining the teachings of references does not involve an

ability to combine their specific structures.”.)

Unable to challenge Samsung’s proffered motivation and the simplicity of Samsung’s combination, ProMOS resorts to misstating Samsung’s evidence. For instance, ProMOS incorrectly alleges that “Samsung has identified a diode in Uda’s schematic (figure 5), and based on that symbol alone has asserted that a person of ordinary skill in the art would just move the symbol into McAdams.” (Response, 16; Ex. 1017, 166:25-167:14.) But the McAdams-Uda combination presented in the Petition does not take the specifically-constructed diode from Uda and insert it into the latch circuit of McAdams; nor does the proposed combination merely move a diode “symbol” from Uda into McAdams. Instead, Dr. Baker’s extensive testimony (spanning 14 pages on this issue) walks through in excruciating detail the teachings a POSITA would glean from reading Uda and how a POSITA would modify McAdams’s circuit based on Uda. (Ex. 1002, ¶¶89-105.) As Dr. Baker explains, Uda is relied upon for its *teaching* that a diode can be used in circuits where fuses are programmed using laser (like McAdams) to dissipate charge that accumulates during such laser programming of a fuse and prevent damage to transistors that are susceptible to such charge buildup. (See Ex. 1002, ¶¶92-98; Ex. 1018, ¶¶24-25.) Nowhere did Dr. Baker suggest that the precise diode structure (including any materials) are incorporated into McAdams’ latch. ProMOS’s assertions that the proposed combination is based on “mere hindsight” (Response, 18) and that

Samsung “fail[ed] to adequately provide a motivation to combine” (*id.*, 20) are thus meritless.

IV. CONCLUSION

The Board should find claims 1-13 of the '492 patent unpatentable and cancel them.

Respectfully submitted,

Dated: March 6, 2020

By: /Naveen Modi/
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Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petitioner's Reply to Patent Owner's Response contains, as measured by the word-processing system used to prepare this paper, 5,309 words. This word count does not include the items excluded by 37 C.F.R. § 42.24(a).

Respectfully submitted,

Dated: March 6, 2020

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioner a true and correct copy of the foregoing Petitioner's Reply to Patent Owner's Response and supporting exhibits by electronic means at the following address of record:

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