

Case No. IPR2019-00780

Patent No. 6,163,492

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.

Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,

Patent Owner.

Case IPR2019-00780

Patent 6,163,492

**DECLARATION OF ERIK DE LA IGLESIA IN SUPPORT OF PATENT
OWNER PROMOS TECHNOLOGIES, INC.'S RESPONSE TO PETITION
FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 6,163,492**

I, Erik de la Iglesia, hereby declare as follows

I. INTRODUCTION

1. I have been retained as an expert on behalf of ProMOS Technologies, Inc. (“ProMOS”) for the above-captioned Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 6,163,492 (the “’492 patent”).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$650 per hour. My compensation is not dependent on the outcome of this proceeding, the results of my analysis, or on the substance of my opinions and testimony.

3. I have been asked to provide my opinion on certain issues identified by counsel for ProMOS, set forth below.

4. In preparing this Declaration, I have reviewed the ’492 patent, the file history of the ’492 patent, and certain prior art references. I have also reviewed the petition for *inter partes* review from Petitioners Samsung Electronics Co. Ltd. (“Petitioner” or “Samsung”), including the material contained therein.

5. In particular, I reviewed all claims at issue in the ’492 patent, including dependent claims, and Dr. Baker’s treatment of those claims. Dr. Baker’s opinions do not affect the outcome of my conclusions below.

6. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and I have considered the viewpoint of a person having ordinary skill in the relevant art at the time of the invention.

II. BACKGROUND AND QUALIFICATIONS

7. I hold a BS in Electrical Engineering from the University of Florida and an MS in Electrical Engineering from Stanford where I was an NSF Research Fellow. My graduate focus included VLSI CMOS architecture and high-speed circuit design. I have worked in several computer and electrical engineering related fields for over 20 years resulting in 68 issued US patents which have been cited over 1650 times in USPTO patent applications. Since 2003 I have served in a number of chief architect and founder roles of companies that have been acquired or gone public.

8. Between December 1997 and November 1999, the time period of the invention, I was a circuit design engineer at Intel Corporation within the Mobile and Handheld Products Group. My responsibilities included working on several aspects of mobile processors and chipsets including clock and power distribution, dynamic clock frequency selection and the circuit design, device simulation and validation of such features. Capabilities such as dynamic clock frequency selection included fuse-enabled functionality that allowed manufacturing engineers

to enable or disable the functionality for different product variants. My role included design, simulation and validation of the fuse structure and the fuse-enabled feature for release in the 1999 mobile Pentium III. Until March of 2000, I worked on similar functionality within the Microprocessor Products Group for the Itanium 3 and 4 products.

9. Between March 2000 and May 2003 I worked as a logic designer and architect for WebStacks and later, through acquisition, Extreme Networks. WebStacks built a fully hardware-based TCP stack for network processing functions including load balancing, proxy processing and content rewrite. Upon acquisition by Extreme Networks, I worked as a logic design manager.

10. Between August 2003 and August 2007 I worked as Founder, Chief Architect and Director of Engineering for Reconnex, later acquired by McAfee. Reconnex built a gigabit line-rate network security analyzer capable of classification, heuristic analysis and policy enforcement on arbitrary protocols and content types.

11. Between August 2007 and September 2008 I founded Strangways, a company focused on addressing messaging security for webmail and internet messaging protocols. Products and technology developed by Strangways were sold to SendMail Inc, Iron Port (Cisco) and other companies.

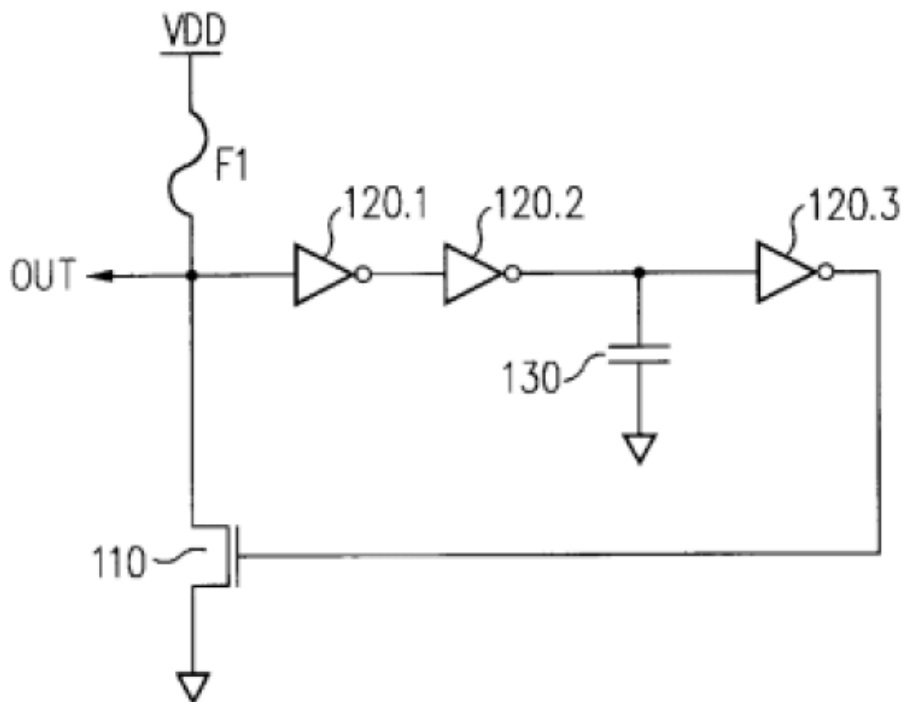
12. Between September 2008 and April 2014 I worked as Chief Architect for Gridiron Systems and through acquisition Sr. Director of Technology for Violin Memory before and after the IPO. My responsibilities included architecture and design of flash media controllers, adaptive caching design and machine learning for application behavior analytics.

III. BACKGROUND OF THE '492 PATENT

A. Brief Overview of the '492 Patent

13. The '492 patent, titled "Programmable latches that include nonvolatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

14. Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



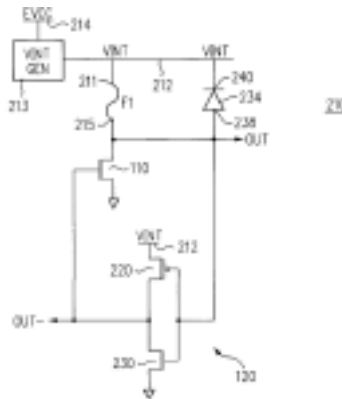
Ex. 1001 at Fig. 1.

15. Before power is applied to the latch at VDD, the terminal OUT may indicate the wrong state. Ex. 1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent: "when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal 'may tend to have its potential raised to a logic level '1'.' In addition, the terminal OUT potential may become 'unstable due to the capacitive coupling' in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown." *Id.* at col. 1:38-47. Attempting to address these situations through the use of capacitor 130 causes operation to be delay dependent and potentially faulty during slow powerup. *Id.* at col. 1:61-65.

16. The solution presented in the '492 patent accomplishes the twin goals of preventing the output node (terminal OUT) from floating above ground when power is off and from destabilizing through capacitive coupling during power-up. In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node.

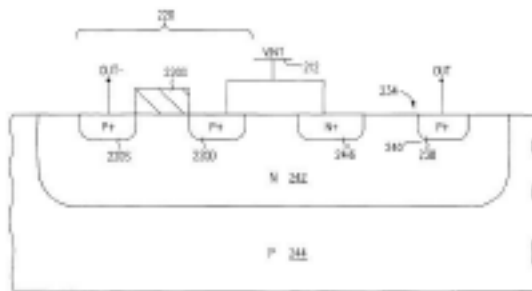
17. One prior attempt to address this problem described in the background of the '492 patent (at Fig. 1) is to place a capacitor 130 such that “[d]uring power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown. Then the ground voltage on terminal OUT propagates through the three inverters to keep transistor 110 on.” Ex. 1001 at col. 1:50-55. This design creates “delays provided by capacitor 130,” in particular when VDD rises slowly as the capacitor takes time to reach the correct voltage. *Id.* at col. 1:61-67.

18. The '492 patent solved these problems at power up through a first embodiment with a new circuit having a “diode that keeps a voltage on a latch output terminal within a predetermined range of values before power supplied is supplied to the latch.” Ex. 1001 at col. 2:1-4, claim 1. This first embodiment of the invention, including a diode, is shown in Fig. 2A:



Ex. 1001 at Fig. 2A.

19. The diode 234 in one preferred embodiment of the '492 patent is a CMOS diode constructed using a P-type anode and an N-type cathode. The conventional circuit diagram including the diode is shown in FIG. 2A wherein diode 234 has anode 238 (terminal at the flat-edge of the triangle) and cathode 240 (terminal at the pointed end of the triangle). Ex. 1001 at col. 3:34-36. In FIG. 2B, the anode is the P+ diffusion region 238 within an N-well 242 serving as cathode. *Id.* at col. 3:62-65.



Ex. 1001 at Fig. 2B.

20. Claim 1 is an example of an embodiment that utilizes a diode to discharge any voltage buildup on the terminal OUT:

- 1.pre) A programmable latch comprising:
 - 1.a) a first terminal for receiving a first voltage;
 - 1.b) a second terminal for receiving a second voltage;
 - 1.c) a terminal T1 for providing a signal indicating a state of the programmable latch;
 - 1.d) a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;
 - 1.e) a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and
 - 1.f) a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Ex. 1001 at Claim 1.

21. There are other embodiments that address the same problem – maintaining OUT at ground and preventing destabilization through capacitive coupling – without using a diode. In these embodiments, described below, any charge buildup at the output node must be allowed to dissipate from the circuit –

with power off – before the output of the latch is used. The specification describes this embodiment, without a diode:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse FI is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8.

22. In allowing excess voltage at the output node to dissipate before reading the latch, the risk of capacitive coupling at the terminal OUT is mitigated.

Claim 14 describes this embodiment which addresses the problem without using a diode:

14.pre) A programmable latch comprising:

14.a) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

14.b) a second terminal for receiving a voltage;

14.c) a terminal T1 for providing a signal indicating a state of the programmable latch;

14.d) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

14.e) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable impedance path; and

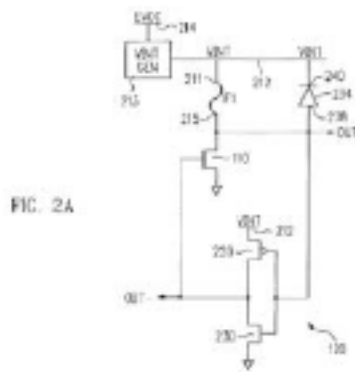
14.f) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are

connected to the inverter output.

Ex. 1001 at Claim 14.

23. By connecting a diode 234 to the OUT node (claim 1) or ensuring that the fuse is not programmed at run-time (claim 14), the '492 patent eliminates the possibility that increasing voltage or capacitive coupling at the OUT terminal causes that node to rise to a level that will turn on inverter 120 and cause a false state at the OUT terminal, in particular during power up.

24. Another aspect of the invention, shown for example in figure 2A below, is that the fuse connects the power source VINT to the output node OUT, whose value is read to indicate the state of the latch.



Ex. 1001 at Fig. 2A.

25. The fuse is claimed as a “non-volatile programmable element,” and each of claims 1 and 14 require that, when conductive, it connects the claimed “first terminal” (power) to the claimed “terminal T1” (terminal indicating the state of the latch). Ex. 1001 at claims 1, 14. Because of this structure, the fuse is directly

indicative of the state of the latch and is the only device which affects the output.

This concept was taken from the prior art embodiment in figure 1, stating

“consistent with one advantage of prior art latch Figure 1, which the specification describes: “Prior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch. The state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals. This advantage is preserved by some embodiments of the present invention.” Ex. 1001 at col. 2:22-27, 3:66-4:3.

IV. PERSON OF ORDINARY SKILL IN THE ART

26. I have adopted and applied Samsung’s level or ordinary skill in the art for purposes of this opinion.

V. CLAIM CONSTRUCTION

27. Other than the specific claim term discussed below, I have been asked to assume that the remaining claim terms have their ordinary customary meaning and that there are no specific constructions that I am to apply. For the claim construction discussed below, my opinion is based on what a person of ordinary skill in the art would understand the claim term to mean at the time the ’492 patent application was filed.

A. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch”

28. I understand that ProMOS has proposed a construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch” that is “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.” I believe that this construction is consistent with the ’492 invention.

29. The purpose of the ’492 patent is to avoid false states at the output, a condition that may occur if excess voltage is allowed to accumulate at the output node during programming (either due to buildup during fuse cutting, for example laser application, or from capacitive coupling at the output node). Ex. 1001 at col. 1:46-48, 1:38-47. After programming, in order to avoid false states, the embodiment claimed in claim 14 must allow that excess voltage to dissipate before reading out the latch – otherwise the latch may indicate a false state and the terminal T1 will not indicate the state of the programmable latch, as claimed.

30. The specification also describes this conclusion, stating that the embodiment without a diode must be operated such that power is turned off after programming to avoid this problem:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This

is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

31. Thus, this embodiment without a diode requires the claim term “providing a signal indicating a state of the programmable latch” to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal

indicating a state of the programmable latch.” And the same term appearing in claim 1 would mean the same thing, so I interpret the phrase “providing a signal indicating a state of the programable latch” in claim 1 as well to mean “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”

VI. INVALIDITY ANALYSIS

A. McAdams does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch”

32. It is my opinion that the McAdams reference does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

33. US4621346 to McAdams (McAdams) titled “Low power CMOS fuse circuit” was filed as application number 06/652,378 on September 20, 1984 and has an earliest priority date of September 20, 1984. The invention relates generally to a CMOS fuse designed for use in self-repairing memory devices. Ex. 1006 at Abstract.

34. The McAdams circuit is shown as Fig. 1 with fuse element 10 connected to the inverter formed by transistors 12 and 13. Ex. 1006 at col. 1:67-2:7.



35. McAdams describes the programming of the fuse (Ex. 1006 at col. 1:12-14) but does not disclose operation of the latch. Specifically, as discussed earlier, claim 1 requires restricting operation of the latch to such times that any residual programming charge above a threshold value has dissipated. Ex. 1001 at col. 5:62-65. And the McAdams has no specific mechanism for dissipating all voltage at nodes 14 and 15, falling prey to the same problem described in the '492 patent. For this reason, McAdams does not teach “a terminal T1 for providing a signal indicating a state of the programmable latch.”

B. A person of ordinary skill in the art would not combine McAdams with Uda because they are incompatible technologies

36. I understand that Samsung has suggested that a person of skill in the art would combine McAdams with Uda such that a diode would be extracted from Uda and placed in the McAdams circuit between node 14 and VCC. It is my opinion that a person of skill would not do so for several reasons:

37. As an initial matter, McAdams and Uda are designed using different technologies. McAdams is implemented in CMOS (McAdams @ 1:41-51) suitable for a traditional well process – using layers both within the substrate and on top of the substrate to form nmos and pmos transistors, among other structures. Uda is constructed using a combination of ECL and CMOS based on a buried and epitaxial layer. (Uda @ 8:19-32) The diodes cited by Baker are parasitic diodes formed by the junction of these buried and epitaxial layers when the epitaxial layer is used as a resistor (Uda @ 10:33-41) and cannot be integrated into the CMOS process of McAdams. These diodes are not direct PN junctions but rather weak parasitic junctions as the P doping of the resistive epitaxial layer is light. The parasitic diodes cannot be implemented in another design without including the resistive element. And further a person of skill in the art would not think to extract only the diode from Uda's diode-resistor combination, and to use that diode in another, CMOS, design.

38. The purpose of Uda is to protect underlying circuitry from damage during fuse programming (Uda @ 3:10-26) without sacrificing excessing area by restricting routing near the fuse. An exemplary construction is shown in FIG. 6. Uda protects the underlying circuitry from ion infiltration (Uda @ 4:30-41) and the associated damage which is a different problem than that addressed by the '492 patent and inapplicable to McAdams with respect to that problem. Uda offers no solution (or recognition) of the issue of accumulated charge on a node potentially causing faulty values to be read from a fuse.

39. For the above reasons, I believe that a person of skill in the art would not combine McAdams and Uda in the way suggested by Samsung.

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I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both. *See* 18 U.S.C. § 1001.

Dated: December 5, 2019

Respectfully submitted,

By:



Erik de la Iglesia