

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS, CO.,)
LTD.,)
Petitioner,)
vs.) Case No.
PROMOS TECHNOLOGIES, INC.,) IPR2019-00780
Patent Owner.) Patent 6,163,492

DEPOSITION OF R. JACOB BAKER, Ph.D., P.E.

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1 DEPOSITION OF R. JACOB BAKER, Ph.D., P.E.

2 October 25, 2019

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4

5 EXAMINATION

6 BY MR. JONES:

7 Q. Good morning.

8 A. Good morning.

9 Q. We've been through the same circus many
10 times, but again, it's Kevin Jones for ProMOS today.

11 Can you state your name for the record.

12 A. Russel, with one L, Jacob Baker.

13 Q. And is it your understanding that you are
14 here today to testify about declarations that you
15 submitted related to the, I'll call it '492 patent,
16 which is 6,163,492?

17 A. Yes.

18 Q. And you submitted three declarations
19 related to the '492 patent, correct?

20 A. Yes.

21 Q. And I'll just review a few of the basic
22 ground rules just basically to get them on the
23 record, although I know that you're well familiar
24 with them.

25 The general format is that I would like to

1 get answers to the questions I ask. And if you can
2 wait for me to complete my question before answering,
3 the record will be more clear. Okay?

4 A. Yes.

5 Q. And if you need a break at any time, just
6 say so. I'll generally take breaks every 60 or 90
7 minutes.

8 A. Okay.

9 Q. Is there any reason that you can't give
10 complete and accurate testimony today?

11 A. No.

12 Q. I see you have some papers in front of you.
13 Can you tell me what they are?

14 A. These are clean copies of my declarations
15 for these three IPRs.

16 Q. Do you mind if I take a ten-second look?

17 A. Nope.

18 Q. There you go.

19 A. Thank you.

20 Q. So I would like to start by handing you the
21 '492 patent, which is Exhibit 1001.

22 (Exhibit 1001 was identified.)

23 MR. ANDERSON: Do you have an extra one?
24 I'll take it.

25 MR. JONES: I have two copies of each.

1 MR. ANDERSON: Are you sure?

2 MR. JONES: I have mine. I brought it for
3 you guys.

4 MR. ANDERSON: Thank you.

5 MR. JONES: I'm not going to carry it home.

6 BY MR. JONES:

7 Q. Dr. Baker, are you familiar with the '492
8 patent?

9 A. Yes.

10 Q. And I would like to start by talking about
11 Figure 1.

12 A. Okay.

13 Q. And just generally ask -- and this may
14 relate to columns 1 and 2 as well, but I want to
15 generally ask what the problem that the '492
16 described was with the circuit of Figure 1 labeled
17 prior art?

18 A. It's not clearly described in the patent,
19 but I think that having read the patent, that they're
20 trying to solve the problem of the out voltage
21 remaining high after the fuse F-1 in Figure 1 has
22 been blown.

23 Q. And is that a problem that exists before
24 the circuit is being read or used?

25 MR. ANDERSON: Objection. Form.

1 THE WITNESS: I don't know how to answer
2 that. The problem is if OUT remains high after the
3 fuse is blown, there's no difference between the fuse
4 being blown and the fuse not being blown.

5 BY MR. JONES:

6 Q. Okay. What would be the reason or reasons
7 that OUT may go high if the fuse was blown?

8 A. So one reason is discussed in Column 1 of
9 the '492, roughly lines 43, that OUT may become
10 unstable due to capacitive coupling during
11 operations.

12 Q. Does the '492 state any other reasons that
13 the voltage on OUT may go high when the fuse was
14 blown?

15 A. I don't recall there being a specific
16 detailed discussion of why the voltage may remain
17 high when the fuse is blown in the patent. But if
18 you point me to it, I'll take a look.

19 Q. Okay. You did mention the concept of
20 capacitive coupling in Column 1, lines 43 and 44.

21 What does that mean in this context?

22 A. If we look at Figure 1, and the fuse is
23 programmed or blown, that as Vdd goes from say zero
24 to 5 volts, there may be a capacitance from Vdd to
25 the OUT node. And so by raising Vdd from zero to 5,

1 it could capacitively or couple to OUT, raising OUT
2 with Vdd.

3 Q. Other than from Vdd, is there capacitive
4 coupling from other sources that could affect voltage
5 at OUT?

6 A. I don't think so, but if you give me a
7 specific example, I'll think about it.

8 Q. For example, OUT connects to something down
9 the stream to the left of the circuit, correct?

10 A. Presumably, yes.

11 Q. And are there -- is there capacitive
12 coupling from whatever OUT connects to that will
13 affect the voltage on OUT?

14 A. That isn't related to Vdd changing?

15 Q. Yes, that is not related to Vdd changing.

16 A. I don't think so.

17 Q. Is there capacitive coupling from ground to
18 OUT that may affect the voltage on OUT?

19 A. There may be capacitive coupling from
20 ground to OUT, but it wouldn't have any influence
21 because ground doesn't vary.

22 Q. Does Vdd vary?

23 MR. ANDERSON: Objection. Form.

24 THE WITNESS: Vdd should remain constant.

25 But if there are circuits which all of a sudden pull

1 a lot of current, there could be some minor variation
2 in Vdd that's due to the large current that flows
3 from the circuits pulling current from Vdd.

4 But in general, the answer is no, Vdd
5 doesn't vary unless you're powering up the circuit
6 and turning it on.

7 BY MR. JONES:

8 Q. Okay. Now, I would like to look at
9 Figure 2A, and also with reference to the
10 specification, I'm sure, and ask you how Figure 2A is
11 an improvement in solving that problem that we talked
12 about in Figure 1?

13 A. I don't know if I would agree that Figure
14 2A is an improvement over Figure 1.

15 For example, the diode has more
16 capacitance, and so with the power supply voltage
17 VINT internal changing or going from zero to Vdd,
18 there would actually be more capacitive coupling to
19 OUT with the diode there.

20 So I don't know if I would agree that this
21 is necessarily an improvement over Figure 1.

22 Q. What does the specification say the purpose
23 of the diode 234 is?

24 A. So in Column 3, roughly lines starting at
25 33 roughly, the diode is connected to the terminal

1 OUT and to the internal power supply VINT terminal
2 212. So that when power is off, the diode will limit
3 OUT to one threshold roughly .6, .7. It will limit
4 OUT to .6, .7 of the internal power supply.

5 In this example where they're saying the
6 internal power supply is grounded, it would limit OUT
7 to the threshold above ground.

8 Q. And is that voltage limit which you said is
9 about .6 or .7 volts in this embodiment enough to
10 turn on transistor 230 in Figure 2A?

11 A. So we've kind of changed the subject. So
12 we've limited OUT to .6, .7, and now you're saying
13 the internal power supply is powered up, and you're
14 asking if with internal power supply powered up, if
15 .6, .7 volts is enough to turn transistor 230 on in
16 Figure 2A?

17 Q. Not exactly. So let me kind of strike the
18 last little discussion and start over.

19 A. Okay.

20 Q. Regardless of whether VINT is powered up or
21 not, I just want to know in this embodiment if the
22 value of OUT is .6 or .7 volts, will that turn on
23 transistor 230?

24 MR. ANDERSON: Objection. Form.

25 THE WITNESS: If I understand your question

1 correctly, the answer is no. It's too low of a
2 voltage.

3 BY MR. JONES:

4 Q. Just to make sure I understand your answer,
5 would your answer be different if I restricted it to
6 VINT to being powered up?

7 A. I think the answer would be the same, but
8 230 wouldn't turn on if the output is a low voltage
9 like .6 volts.

10 Q. And in Column 3, you pointed me to a
11 discussion sort of in the middle of the column about
12 the diode. And for example, the paragraph at 333 to
13 49, is this paragraph saying that the diode will keep
14 the value OUT low and avoid false states before VINT
15 is powered up?

16 MR. ANDERSON: Objection. Form.

17 THE WITNESS: I don't think you can talk
18 about false states before VINT is powered up. I
19 think you would have to power the circuit up before
20 you could actually look at the state of the circuit.

21 BY MR. JONES:

22 Q. Okay. So if VINT is powered up and the
23 fuse had been programmed, meaning blown, does the
24 diode then prevent OUT from taking high state?

25 A. No, not exactly. The diode is going to

1 limit the output voltage to the internal power supply
2 voltage VINT plus the diode's threshold voltage.

3 So with the circuit powered up, the diode
4 would still allow OUT to go high if the fuse wasn't
5 blown.

6 I think what the diode is doing is bleeding
7 off extra charge on OUT when VINT is at ground just
8 ensuring OUT starts up in a low voltage state.

9 But if the fuse isn't blown, then OUT can
10 go high just fine with the diode there, and the diode
11 won't limit the output voltage to a ground or a low
12 voltage.

13 **Q. And why -- if I understood correctly, why**
14 **do you want OUT to be low, in a low voltage state,**
15 **before VINT starts ramping up?**

16 A. Are we still focusing on the fuse being
17 blown or programmed?

18 **Q. Yes.**

19 A. So when the fuse isn't blown, OUT is pulled
20 high to VINT. However, if for some reason out has
21 some residual charge stored on it, the diode isn't
22 there, the circuit could -- the OUT could be a high
23 voltage because of that residual charge, and the
24 diode would -- using the diode would then allow the
25 output to be pulled low if the fuse is programmed.

1 Q. Okay. And in that case, if there wasn't a
2 diode and there was enough residual charge on OUT to
3 be read as a high value, still in the condition where
4 the fuse is programmed, why is that bad?

5 A. Are we assuming that power hasn't been shut
6 off so that output charge can just drain to ground
7 through the off transistor 110, for example?

8 Q. Correct. Before that.

9 A. So if I understand correctly, if we program
10 the fuse F-1 power still applied, then there's no way
11 for the output to be pulled low because, for example,
12 there's been nothing actively pulling OUT down.

13 In fact, the diode would leak the output to
14 a high voltage, and the circuit would be the same or
15 operate the same as if the fuse hadn't been
16 programmed.

17 Q. And is that the specification called a
18 false state?

19 A. Can you point me to where it says "false
20 state" in the spec?

21 Q. Well, we can forego that.

22 A. Okay.

23 Q. That last question.

24 Just before that, you made a statement, and
25 hopefully this makes sense, it's kind of out of

1 context, but what you said was are we assuming that
2 power hadn't been shut off so that output charge can
3 just drain to ground through the off transistor 110,
4 for example.

5 A. Yes.

6 Q. And can you explain to me what you meant by
7 that?

8 A. So if we look at Figure 2A, for example, if
9 the VINT is zero, and external Vcc is zero, and the
10 fuse is blown -- obviously, if the fuse isn't blown
11 then OUT gets shorted to VINT, which is zero. Then
12 if we have a charge on out, we have a leakage path
13 through 110, which will pull OUT to ground through
14 the leakage in 110. And of course, if we have the
15 diode, it will also get pulled out; it will also get
16 pulled to ground through the diode. But even without
17 the diode there, OUT will get pulled to ground
18 through transistor 110 and -- transistor 110.

19 Q. Just to clarify, at the end of that answer
20 you said the diode there OUT will get pulled to
21 ground with transistor 110 and transistor 110?

22 A. Just transistor 110.

23 Q. Will -- okay. If VINT is powered up, will
24 the voltage on OUT get pulled to ground through
25 transistor 110?

1 MR. ANDERSON: Objection. Form.

2 THE WITNESS: If VINT is powered up and OUT
3 is high, then OUT will stay high. If VINT is powered
4 up and OUT is low, then OUT will stay low.

5 BY MR. JONES:

6 Q. And in that answer, are you assuming that
7 the fuse has been programmed?

8 A. Yes. Because if the fuse hasn't been
9 programmed, there's a short from V OUT to VINT.

10 Q. And out will necessarily follow VINT in
11 that case?

12 A. When it's shorted through the fuse, yes.

13 Q. So still related to this discussion, I
14 would like to talk about claim 1, column 8. There is
15 an element, the third element that reads a terminal
16 T1. Do you see that element?

17 A. Yes.

18 Q. And I would like to ask first what your
19 understanding of this language is in the context of
20 Figure 2A: A terminal T1 for providing a signal
21 indicating a state of the programmable latch.

22 A. So terminal T1, my understanding is that
23 would be OUT in Figure 2A. Terminal T1.

24 Q. Okay. And what does the language "a state
25 of the programmable latch" mean?

1 A. The state of the programmable latch
2 indicates whether the fuse is blown or not blown. So
3 if OUT is a 1 or a zero.

4 **Q. So if the fuse is not blown, then OUT**
5 **should be high, right?**

6 A. Yes.

7 **Q. And if the fuse is blown, then OUT should**
8 **be low, right?**

9 MR. ANDERSON: Objection. Form.

10 THE WITNESS: If everything is working
11 right, yes.

12 BY MR. JONES:

13 **Q. And I thought previously when we set up the**
14 **condition that the fuse is programmed and VINT was**
15 **powered up, if OUT is high, then it will stay in that**
16 **state; is that correct?**

17 A. Can you repeat the first part of that
18 question?

19 **Q. Sure. If the fuse is programmed and VINT**
20 **is powered up, then if OUT is high, it will stay in**
21 **the high state?**

22 A. If the circuit is malfunctioning, yes,
23 that's what will happen.

24 **Q. Okay. What should happen if the fuse is**
25 **programmed and VINT is powered up, what state should**

1 **OUT be?**

2 A. If the fuse is blown or programmed, then
3 OUT should go to a zero if things are working right.

4 **Q. And if OUT doesn't go to a zero, then this**
5 **claim element is not met, right? Because the**
6 **terminal T1 does not provide a signal indicating a**
7 **state of the programmable latch?**

8 MR. ANDERSON: Objection. Form.

9 BY MR. JONES:

10 **Q. Right?**

11 A. If OUT stays high independent of the fuse,
12 then the circuit isn't working correctly.

13 However, the language of the claim says
14 that the T1 is the signal indicating the state of the
15 programmable latch. If the programmable latch is
16 high, I don't know if I would say that the claim
17 element is not being met because all we need to do is
18 show that T1 indicates the state of the latch.

19 Now, if the state of the latch doesn't
20 represent the state of the fuse, whether it's been
21 blown or not, I don't think -- I think the claim
22 element will still be met because it requires
23 terminal T1 to provide a signal indicating to state
24 the programmable latch. I think there's more to -- I
25 mean, I think you're asking something a little

1 different.

2 Q. I think I understand the point you're
3 making.

4 A. Okay.

5 Q. Let me ask a different question, then. If
6 the fuse is programmed and OUT is high, then that
7 terminal T1 OUT does not indicate the state of the
8 fuse; is that correct?

9 MR. ANDERSON: Objection. Form.

10 THE WITNESS: I think that's correct.
11 Terminal T1 would indicate the state of the latch in
12 that case, not the state of the fuse.

13 BY MR. JONES:

14 Q. And I mean, regardless of how the circuit
15 operates or what condition you're in, meaning whether
16 the fuse is programmed or not or VINT is powered up
17 or not, regardless of any of those conditions, your
18 understanding of this claim element is that terminal
19 T1 always indicates the state of the programmable
20 latch?

21 MR. ANDERSON: Objection. Form.

22 BY MR. JONES:

23 Q. Is that right?

24 A. I would have to qualify that with the other
25 parts of the claim that says a first terminal for

1 receiving a first voltage, a second terminal for
2 receiving a second voltage.

3 If, for example, the first terminal
4 received ground and the second terminal received
5 ground, then terminal T1 wouldn't be providing a
6 signal indicating a state of the programmable latch
7 because there's no power going to the latch.

8 So to the extent that the latch is powered
9 up and were meeting the earlier claim elements, then
10 yes, terminal T1 provides a signal indicating the
11 state of the latch.

12 Q. Okay. So I would like to shift gears a
13 little bit to the next element, which is a
14 programmable electrical path, including a nonvolatile
15 programmable element.

16 Is this element -- generally. We're
17 talking about the fuse, right, in Figure 2A?

18 A. Just in general? Because there's
19 additional discussion in Column 7. But in general, I
20 think that it's referring to the fuse, yes.

21 Q. And sort of to start at the finish line
22 here and see how this goes, but in every embodiment
23 in the '492, the fuse is the only thing that
24 determines whether the terminal T1 is connected to
25 the first terminal or not; is that correct?

1 MR. ANDERSON: Objection. Form.

2 THE WITNESS: I don't think that's exactly
3 correct if we look at column 7, lines 24 through 36.
4 But F1 is what determines if the terminal T1 connects
5 to the first terminal, and we can call F1 the
6 programmable path.

7 So I think loosely speaking that the
8 programmable path connects terminal T1 to the first
9 terminal, yes.

10 BY MR. JONES:

11 Q. And F1 is the only thing that determines
12 whether T1 connects to the first terminal or not,
13 right?

14 A. In the embodiment of Figure 2A, yes.

15 Q. Is there any other embodiment anywhere in
16 the patent where that is not true?

17 A. In Figure 8, F1 connects OUT to VINT if
18 it's not blown. In figure 7, F1 connects OUT to
19 VINT, or 212 if F1 is not blown.

20 Same thing in Figure 6 and Figure 2A, yes.

21 Q. So there are no embodiments -- well, let me
22 strike that and try to just ask you the same thing
23 again. I apologize.

24 F1 in every embodiment in the patent is the
25 only thing that determines whether T1 connects to the

1 first terminal or not, right?

2 MR. ANDERSON: Objection. Form.

3 THE WITNESS: If I understand what you're
4 saying, yes, F1 determines if the OUT or terminal 1
5 is connected to the internal power supply voltage
6 212, neglecting, though, leakage through the diode
7 that's added, for example, in parallel with the fuse
8 F1.

9 BY MR. JONES:

10 Q. And back to Claim 1 here at line 46 to 50,
11 does that claim term require that the nonvolatile
12 programmable element be the only thing that connects
13 T1 to the first terminal?

14 MR. ANDERSON: Objection. Form.

15 THE WITNESS: No, it doesn't require that's
16 the only thing.

17 BY MR. JONES:

18 Q. Okay. If there were -- in a hypothetical
19 here, if there were another fuse in series with the
20 first, then -- and let's say that other fuse was
21 programmed.

22 A. Okay.

23 Q. If the first fuse was not programmed,
24 meaning it was conductive, but again, the other fuse
25 is programmed, then the terminal T1 does not connect

1 to the first terminal, right?

2 A. If there are two fuses in the series, and
3 one of the fuses is blown, then if the two fuses are
4 between the internal voltage and OUT, having one of
5 the blown fuses would not allow a connection through
6 the fuses between VINT and OUT.

7 Q. And in that case, this claim element would
8 not be met; isn't that right?

9 A. So are we redefining programmable element
10 to be the series connection of two fuses?

11 Q. No. I'm still just defining it as the
12 original when I called it the first fuse.

13 A. I don't know. That doesn't make any sense
14 because when one fuse is blown, it doesn't do -- I
15 mean, it's no different than if you have two fuses
16 blown. And so I would need to think about that.

17 But -- yeah, I would need to think about
18 it. I didn't form an opinion on having two fuses in
19 a series.

20 Q. I'm going to hand you the Joo reference,
21 this discussion, if we just jump right into it.

22 So that's Exhibit 1010.

23 (Exhibit 1010 was marked for
24 identification.)

25

1 BY MR. JONES:

2 Q. And I see you're opening one of your
3 declarations. I assume the declaration will lead to
4 the Joo discussion, which will be in the 781 IPR.

5 A. Correct.

6 Q. Okay. Now, is it your opinion that in Joo
7 Figure 2, fuse 2 meets the claim element that we were
8 just talking about, the programmable electrical path
9 nonvolatile programmable element?

10 MR. ANDERSON: Objection. Form.

11 THE WITNESS: Yes, I discuss that starting
12 on page 45 of my declaration, the one concerning Joo.

13 BY MR. JONES:

14 Q. Now, in Joo Figure 2, if MP1 were
15 nonconductive, then the first terminal is necessarily
16 not connected to the terminal T1, right?

17 MR. ANDERSON: Objection. Form.

18 THE WITNESS: If the fuse, fuse 2 in Joo
19 Figure 2 is not blown, is not programmed, then
20 terminal T1 is connected to the first terminal. Here
21 Vcc, Figure 2 of Joo, through the variable impedance
22 electrical path MP1. So I don't think I would agree
23 with that because MP1 is not a fuse or something that
24 can be blown.

25

1 BY MR. JONES:

2 Q. What if the signal FENB were high?

3 A. Then the impedance of MP1 would be high.

4 But as discussed in the '492 transistor is a variable
5 impedance electrical path, so I still think that
6 terminal T1 would be connected to the first terminal,
7 Vcc, as long as fuse 2 is not blown.

8 Q. So is it your opinion that if FENB was a
9 high value, that a current flows across MP1?

10 A. MP1 would have a high impedance, and as
11 long as there's a potential across MP1, even if FENB
12 were high, then there would be a current flowing
13 through MP1 called the off current.

14 Q. But under that condition you would say that
15 MP is off, right?

16 A. It would have a high variable impedance.
17 It would have a high impedance, yes, so it would be
18 from transistor point of view off.

19 Q. So I would like to look at claim 2 in the
20 '492 patent. It says -- I'll wait a second for you
21 to find your spot in the declaration.

22 A. Okay. Thank you.

23 Q. Claim 2 says, "Wherein, during operation of
24 the latch." Do you have any opinion about what that
25 means? What does it mean to be during operation of

1 the latch?

2 A. I mean, just at a high level, the
3 operation of the latch during operation means that
4 you've powered up the latch, so you've applied the
5 first and second voltages that are talked about in
6 claim 1.

7 Q. Okay. So on that point, claim 1 is an
8 apparatus claim, right?

9 A. Yes.

10 Q. And so is it your understanding that the
11 limitations in claim 1 only needs to be met when the
12 voltages are applied? Or is it your understanding
13 that to meet all the elements of claim 1, a structure
14 must always have the claim language?

15 MR. ANDERSON: Objection. Form.

16 THE WITNESS: For claim 1 alone, my
17 understanding is that the apparatus has to have at
18 least the claimed elements, such as a first terminal
19 4 receiving a first voltage, terminal T1 for
20 providing a signal, et cetera.

21 However, in claim 2 it says the
22 programmable latch of claim 1 wherein during
23 operation of the latch. And I take operation of the
24 latch to mean that the apparatus is being used, not
25 just simply present.

1 BY MR. JONES:

2 Q. Okay. So back in claim 1, though, claim 1
3 doesn't say wherein during operation of the latch,
4 right?

5 A. I don't see that, correct.

6 Q. And so the elements in claim 1 have to be
7 present regardless of whether you're operating the
8 latch or not; isn't that right?

9 A. For claim 1, yes.

10 Q. And so isn't it true that the language of
11 claim 1 needs to be met even if you're not applying a
12 first and second voltage?

13 A. For claim 1, it simply requires, for
14 example, a first terminal for receiving a first
15 voltage, a second terminal for receiving a second
16 voltage. So it doesn't need to be operating,
17 correct. It's an apparatus claim.

18 Q. Okay. I'm going to turn to the McAdams
19 reference. So do you want a short break?

20 A. Yes, please.

21 (A recess was taken from 9:54 a.m.
22 to 9:59 a.m.)

23 BY MR. JONES:

24 Q. So I would like to hand you the McAdams
25 reference, 1006.

1 (Exhibit 1006 was identified.)

2 BY MR. JONES:

3 Q. Are you familiar with this reference,
4 Dr. Baker?

5 A. Yes.

6 Q. I would like to start in column 2, around
7 line 21.

8 A. Okay.

9 Q. And ask you if this paragraph here,
10 McAdams, is talking about the same -- the same
11 condition that the '492 background talked about?

12 MR. ANDERSON: Objection. Form.

13 THE WITNESS: There's some discussion in
14 column 1 of the '492 about -- roughly at lines 39 on
15 about OUT may tend to have a potential raise to lodge
16 a level 1. I think in general the discussions are
17 similar. I don't think they're exactly the same.

18 BY MR. JONES:

19 Q. Well, McAdams is also talking about
20 capacitive coupling to node 14; isn't that right?

21 A. Yes. It says in line 27, column 2 of
22 McAdams, "Any capacitive coupling of voltage to node
23 14 from the Vcc transition is quickly discharged."

24 Q. And where is it discharged in Figure 1 of
25 McAdams?

1 A. It's discharged through transistor 11.

2 Q. And that's an NMOS transistor, right?

3 A. Transistor 11 is NMOS, yes.

4 Q. And the other of -- strike that again.

5 Is node 14 the drain or the source of NMOS
6 11?

7 A. The drain.

8 Q. And the source is grounded, right?

9 A. Yes.

10 Q. And the transistor is off in this
11 condition; is that right?

12 MR. ANDERSON: Objection. Form.

13 THE WITNESS: I don't follow which
14 condition.

15 BY MR. JONES:

16 Q. The paragraph in column 2 that we're
17 talking about with node 14 having excess charge and
18 dissipating through transistor 11, does that occur
19 when transistor 11 is on or off?

20 MR. ANDERSON: Objection. Form.

21 THE WITNESS: My understanding is the
22 situation described in column 2, lines 21 through 34
23 of McAdams, the transistor 11 is on.

24 BY MR. JONES:

25 Q. Okay. And then there's a discussion that

1 goes from line 29 to 34 about the coupling to node 14
2 closely tracking Vcc.

3 Is that discussion a condition when
4 transistor 11 is on or off?

5 A. That discussion is talking about how if the
6 fuse is blown and Vcc rises quickly, coupling to node
7 14, that node 14 will eventually get pulled low
8 through transistor 11 due to leakage, and that will
9 in turn, although not discussed there, turn on
10 transistor 11 so the transistor 11 is on.

11 Q. So I'm looking at Figure 2A of the '492
12 patent.

13 A. Okay.

14 Q. Wouldn't the same be true here? In other
15 words, if the fuse were blown and VINT rose quickly
16 and caused capacitive coupling on OUT, wouldn't that
17 dissipate through transistor 110 to ground?

18 A. There will be leakage through transistor
19 110, just like in McAdams.

20 However, in Figure 2A of the '492, you also
21 have a diode. And if the diode leakage is greater
22 than the transistor leakage 110, then the diode will
23 keep leakage through the diode, will keep OUT high.
24 And so it's a little bit different than what's
25 described in McAdams, because in McAdams you don't

1 have that extra leakage path up through the diode
2 that you have in Figure 2A of the '492.

3 Q. Let's talk about Figure 1, then, of the
4 '492. If there's capacitive coupling on OUT, then
5 wouldn't that dissipate across transistor 110 to
6 ground, like McAdams described?

7 MR. ANDERSON: Objection. Form.

8 THE WITNESS: OUT will be pulled to ground
9 through 110 if fuse 1 is programmed or blown because
10 of the leakage through 110, yes, over time.

11 BY MR. JONES:

12 Q. Does that contradict what the inventors of
13 the '492 said in columns 1 and 2?

14 MR. ANDERSON: Objection. Form.

15 BY MR. JONES:

16 Q. And specifically, column 1 from line 40.

17 A. In column 1 of the '492 in line 40 or so,
18 they're not focusing or discussing the leakage
19 through transistor 110, which would discharge OUT to
20 ground if fuse F1 were blown.

21 Q. When I read these two references together,
22 it seems that both McAdams and the '492 are
23 recognizing the exact same condition, that being that
24 there's capacitive coupling on a node when the fuse
25 is blown.

1 But McAdams is saying don't worry about it,
2 it will dissipate across the NMOS, whereas the '492
3 says this is a big problem, we need to solve this
4 problem.

5 Is that a correct understanding of these
6 two references?

7 MR. ANDERSON: Objection. Form.

8 THE WITNESS: The '492 is neglecting the
9 leakage through transistor 110, which will pull out
10 to ground in Figure 1 of the prior art. The McAdams
11 reference is not neglecting that leakage current.
12 It's stating what will happen is that OUT will be
13 pulled to ground through transistor 11 in Figure 1,
14 which corresponds to transistor 110; figure 1 of the
15 '492.

16 In the '492, they've added the diode, which
17 will not only increase the capacitive coupling from
18 the internal power supply to OUT, but will also
19 provide a leakage path that pulls OUT up. That one
20 doesn't have a McAdams or Figure 1 of the prior art,
21 and that leakage path, if it's -- especially if it's
22 leaking greater than the leaking through transistor
23 110 in Figure 2A, could keep the output voltage high,
24 which wouldn't be a problem in Figure 1 of the prior
25 art, the '492 or Figure 1 of McAdams.

1 BY MR. JONES:

2 Q. Is it true that both McAdams and the '492
3 are describing the same condition?

4 MR. ANDERSON: Objection. Form.

5 THE WITNESS: Are you talking about when
6 they describe the capacitive coupling from Vdd to the
7 other side of the fuse?

8 BY MR. JONES:

9 Q. Yes.

10 A. They both describe them when Vdd powers up
11 that there will be capacitive coupling across the
12 fuse, yes.

13 Q. But McAdams in column 2 says that's not a
14 problem because that charge will dissipate across
15 transistor 11, right?

16 MR. ANDERSON: Objection. Form.

17 THE WITNESS: McAdams points out that the
18 transistor will pull node 14, the bottom side of the
19 fuse, to ground because transistor 11 leaks. And in
20 '492, they failed to point out that transistor 110 --
21 well, at least in the section we're focusing on, will
22 also leak and pull output -- the output to ground in
23 the prior art.

24 BY MR. JONES:

25 Q. Okay. Now, on the '492 patent, there's a

1 few places in the spec that talk about embodiments
2 with no diode. And one of those places, for example,
3 is at column 2, line 38.

4 Can you describe what would happen in this
5 embodiment with no diode if there were capacitive
6 coupling at node -- at the output node?

7 A. So --

8 MR. ANDERSON: Objection. Form.

9 THE WITNESS: Well, what's described there
10 in column 2 of the '492, some embodiments with only
11 one CMOS inverter and no capacitor operates
12 successfully even without a diode is exactly what's
13 seen in Figure 1 of McAdams, and as discussed in
14 McAdams the reason it operates successfully is since
15 there's no diode providing a leakage path up to the
16 power supply, that transistor 11 in McAdams or
17 transistor 110 in the '492 will provide a leakage
18 path pulling that node to ground and will get the
19 correct output.

20 BY MR. JONES:

21 Q. And that leakage current will only pull the
22 node to ground if the power is not turned on; is that
23 right?

24 A. No. It will always pull the node 14 and
25 346 to ground when the fuse is programmed or blown,

1 as it will in Figure 1 of the '492 or Figure 2A of
2 the '492 without the diode because there's no other
3 path for the output or no other path for pulling that
4 bottom side of the fuse up.

5 Q. So in the '492, column 2, line 47, it says
6 specifically that the power is turned off after
7 programming and the voltage on OUT is allowed to
8 return to ground.

9 And I'm paraphrasing that, but why do they
10 make the point that power is turned off in this
11 discussion?

12 MR. ANDERSON: Objection. Form.

13 THE WITNESS: Again, the patent seems to
14 neglect the leakage through transistor 110. And in
15 the embodiment discussed in that paragraph of using
16 one inverter and no diode, which is Figure 1 of
17 McAdams, if you don't recognize that transistor 110
18 leaks, then this is saying -- because it apparently
19 doesn't recognize that transistor 110 leaks -- that
20 it still doesn't matter because you're going to shut
21 the power off after programming, and so OUT will
22 start out as a zero.

23 BY MR. JONES:

24 Q. In that state when power is not on, if you
25 do not account for the leakage across 110, where does

1 any excess charge on the OUT node go?

2 A. Well, ultimately it will just drain to the
3 substrate and cause the voltage on the OUT node to go
4 to zero when there's no power applied.

5 Q. In the '492 at column 5, from line 51, are
6 they talking about the same embodiment that we just
7 talked about?

8 A. So this is -- this paragraph is talking
9 about Figures 2A and 6. And Figure 6 is the same as
10 Figure 1 of McAdams except Figure 6 adds a diode.

11 And in column 5 the discussion is that if
12 the diode is omitted, that because power is turned
13 off, the output will go to ground, that the diode may
14 be omitted. And so things would still work okay.

15 It's basically just repeating what's
16 already taught in McAdams with the difference that
17 McAdams teaches that we know they leak to ground
18 through transistor 11, which is equivalent to
19 transistor 110 in the '492, even if you don't have
20 the power shut off.

21 Q. So looking in '492, claims 1 and 14,
22 they're the only two independent claims, both
23 apparatus claims. And much of the language is
24 identical. But I'll say one difference is that claim
25 14 does not claim a diode, right?

1 A. A diode is not claimed in 14, correct.

2 **Q. And in claim 1 a diode is claimed, right?**

3 A. Correct. Claim 1 has a diode. Claim 14
4 may have a diode, but it's not required.

5 **Q. Now, do you think that claim 14 is claiming**
6 **the embodiment, for example, in column 5 from line 51**
7 **that we just talked about?**

8 MR. ANDERSON: Objection. Form.

9 THE WITNESS: I haven't done an analysis on
10 that. I think it could be. But again, there could
11 be a diode present in claim -- in the apparatus that
12 practices claim 14.

13 I mean, if you look at Figure 6 or Figure
14 8, which have similar topography, just different
15 polarity to power supplies. But if you look at
16 Figure 6, for example, I think Figure 6 would be an
17 embodiment that practices claim 14. And in that
18 embodiment, there is a diode, even though it's not
19 claimed.

20 BY MR. JONES:

21 **Q. Going back to McAdams.**

22 A. Okay.

23 **Q. I understood a prior answer of yours to be**
24 **that McAdams recognizes that charge on node 14 will**
25 **leak to ground through transistor 11 even if power is**

1 on; is that correct?

2 A. Yes.

3 Q. Does McAdams teach at all that if power is
4 off, a charge will make it across transistor 11?

5 A. Are you asking if McAdams teaches that if
6 power is off, that a node in the circuit will
7 discharge to ground?

8 Q. Yes.

9 A. I don't recall McAdams teaching that. But
10 that's something that a person of ordinary skill, or
11 I guess common sense would understand that if there's
12 no source of power connected to a circuit, over time
13 the charge or energy stored in the circuit will drain
14 to ground and go to -- everything in the circuit will
15 go to ground state.

16 So I guess I'm not entirely -- I kind of
17 wouldn't expect them to talk that if there's no power
18 applied to the circuit, that the circuit relaxes to
19 the ground state.

20 Q. To be more precise about that question,
21 does McAdams teach that power will dissipate across
22 transistor 11 specifically when power is off?

23 A. Transistor 11 will continue to leak even if
24 power is removed from the circuit, and I don't recall
25 McAdams teaching that.

1 Q. Okay. I would like to move on to the Uda
2 reference, which is Exhibit 1007.

3 (Exhibit 1007 was identified.)

4 BY MR. JONES:

5 Q. Focusing first on Figures 5 and 6.

6 A. Okay.

7 Q. Is it your understanding that Figure 6
8 relates to Figure 5 in some way? And you may refer
9 to like columns 9 and 10, 11 roughly.

10 A. Figure 5 is the circuit diagram showing the
11 fuse arrangement of Figure 2. And then Figure 6 is a
12 cross section of the fuse arrangement of Figure 2,
13 yes.

14 Q. And are you familiar with the term ECL
15 logic, emitter coupled logic?

16 A. Yes.

17 Q. What does that term describe?

18 A. It's a type of logic implemented using
19 bipolar junction transistors that was first created,
20 if I remember correctly, in the late 60s. The output
21 logic swings from roughly minus .8 to minus 1.5.

22 Q. Are figures -- I should say is Figure 6 ECL
23 logic?

24 A. No. Figure 6 is a cross-sectional view.
25 And I don't see any transistors that would be used to

1 implement ECL logic or emitter coupled logic in
2 Figure 6.

3 **Q. Does it make sense to talk about a**
4 **fabrication process using ECL design?**

5 MR. ANDERSON: Objection. Form.

6 THE WITNESS: It makes sense to talk about
7 a fabrication process used to implement ECL, yes.

8 BY MR. JONES:

9 **Q. And I assume you're familiar with the**
10 **concept of CMOS as well, right?**

11 A. Yes.

12 **Q. And can you tell by looking at Figure 6 if**
13 **this was made using a process that could also**
14 **implement ECL or CMOS?**

15 MR. ANDERSON: Objection. Form.

16 THE WITNESS: I haven't formed an opinion
17 on that. But just sitting here right now, I think
18 that the answer is yes. These metal layers and
19 interconnect could be used in either a CMOS or a
20 bipolar process that implements ECL.

21 BY MR. JONES:

22 **Q. So you could design a CMOS transistor in**
23 **this cross section of Figure 6?**

24 MR. ANDERSON: Objection. Form.

25 THE WITNESS: Again, I haven't studied that

1 in detail, but I think the answer is yes, because
2 what's being shown here in Figure 6 and the
3 interconnect layers and fuses and such corresponding
4 to Figure 5.

5 And the wires in a CMOS process, metal
6 interconnect layers -- I say wires, but the metal
7 interconnect layers are the same as in a -- are the
8 same between CMOS and ECL in general.

9 BY MR. JONES:

10 **Q. Figure 6 also has layers 18, 19 and 20,**
11 **which are not interconnect layers, right?**

12 A. 18, for example, is a semi-conductor
13 substrate. And that is not an interconnect layer.
14 And both CMOS and ECL technology utilize a
15 semi-conductor substrate.

16 Let me look at 19, which I think is the
17 other one you mentioned. And 19 is a buried layer of
18 doping. It looks like just a doping layer, and
19 that's common in both types of fabrication processes.

20 And 20 is an epitaxial layer, and that's
21 also common in both types of logic processes.

22 So I think that it's reasonable that this
23 cross-sectional view could be from a CMOS or a
24 bipolar process. I haven't studied it in detail, but
25 just looking at the cross-sectional view, I think it

1 could be for either type of process.

2 Q. Now, where does Vee in Figure 5, where does
3 that value connect in Figure 6?

4 MR. ANDERSON: Objection. Form.

5 THE WITNESS: I'm unsure. I would need to
6 spend some time reviewing this. But just looking at
7 it right here, if I had to point to something that I
8 think it might be where the Vee is connected in
9 Figure 6, I would point to 27A2. But I'm unsure.

10 But I can spend more time and read and see
11 if it's clear in the spec, but I think it would be
12 27A2.

13 And the reason I say that is if you look at
14 the metal connection 27A2, 26A2, that's connected now
15 to what looks like a highly doped area, 22A, which
16 goes over to what they have as a resistor. And I
17 think that that would likely be the resistor in
18 Figure 5.

19 And the connection to the resistor on the
20 right side shows it goes up through the metal stack.
21 But again, I'm unsure. I would need to spend some
22 time looking at that. That's not something I formed
23 an opinion on.

24 BY MR. JONES:

25 Q. Can you tell the resistor symbol that's

1 drawn, whether that corresponds with R1 or R2 of
2 Figure 5?

3 A. I don't know. I'm unsure even if that's
4 the one going to Vee, or if that's the one going to
5 the gate of 17.

6 And I scanned the specification, and I
7 didn't see anything jump out with a detailed
8 specification there. But again, I haven't formed any
9 opinion on this cross-sectional view and how it
10 relates to Figure 6 in my declaration.

11 Q. There's a symbol in Figure 5. Let's just
12 look at R2, for example. There's -- R2 is drawn as a
13 resistor. And then there's a horizontal line above
14 it going up to V2 and ground.

15 A. Yep.

16 Q. What is that symbol there? It's a resistor
17 with a horizontal line over it, what is that
18 representing?

19 A. That indicates that the resistor was made
20 with an implanted or diffused semi-conductor
21 material.

22 So in this case, the flat line corresponds
23 to P-type material. So the resistor R2, for example,
24 would be N-type material.

25 And so as you change the voltage on the

1 resistor R2, you change the -- this is going to sound
2 technical, but you change the width of the depletion
3 region between the N-type material that's used to
4 implement R2 and the P-type material adjacent to that
5 N-type material. So the resistance changes.

6 That P-type material is also used for the
7 anode of diode 2.

8 But in real simple terms, it just means
9 that R2 is implemented with a semi-conductor
10 material, and then its value will change with the
11 voltage applied across it.

12 Q. And if resistor R2 is the resistor shown in
13 Figure 6 -- I want you to assume that.

14 A. Okay.

15 Q. Then where is diode D2 in Figure 6?

16 A. Again, I haven't looked at this in detail.
17 But just looking at that and making that assumption,
18 material 20 would be N-type material. Material 19
19 would be P-type material. So the diode would be
20 between material 20 and 19.

21 Now, again I haven't looked at that, so it
22 may be between material 19 and material 18.

23 So for example, if material 18 were N-type,
24 then material 19 and 20 could be P-type. And that
25 would be the connection, would be a P-type material

1 would be the diode.

2 And so instead of having R2 as N-type, it
3 would simply be P-type, and then the other side of
4 diode D2 would be 18 or ground.

5 Again, I haven't looked at the specifics of
6 this, but I've looked at enough cross-sectional areas
7 to know generally what things are.

8 So that would mean R2 would be a P-type
9 resistor, and substrate would be N-type.

10 And if you want me to be more exact, I can
11 go read the specification and find out what the real
12 answer is.

13 **Q. I think what I'm interested in here is how**
14 **D2 connects to node T in Figure 6. So do we know --**
15 **I guess I haven't asked this, but do you know where**
16 **node T is in Figure 6?**

17 A. I don't know what the correspondence
18 between Figure 6 and Figure 5 is. For example,
19 Figure 5 shows two resistors.

20 And I see one resistor symbol there. I
21 think Figure 6 is just a representative
22 cross-sectional view of the semi-conductor process.
23 I don't think it necessarily directly corresponds to
24 Figure 5.

25 **Q. But based on Figure 5, and our discussion**

1 with that symbol there, do we know that the anode of
2 diode D2 is not connected to node T directly?

3 A. Well, I think it could be. So if R2 is a
4 P-type material, and that P-type material was the
5 anode of D2, then it would be directly connected to
6 T. And then the N-type material, which is the
7 cathode of D2, would be connected to ground.

8 Q. So in column 10 -- we may need to dig in, a
9 little bit at least, of details here. 10 line 20, it
10 says the substrate 18 is made of a P-type silicon
11 single crystal.

12 A. Okay.

13 Q. And you can read maybe the rest of that
14 paragraph. But from that, going back to Figure 6,
15 can you tell, I guess, where the anode of D2 is?

16 MR. ANDERSON: Objection. Form.

17 THE WITNESS: If 18 is a P-type material,
18 and again, we're assuming the resistor seen in
19 Figure 6 is the resistor R2 in Figure 5, then 20,
20 layer 20 may be P-type. Layer 19 would be N-type.

21 And then layer 19 would be connected to
22 ground form so the diode D2 is formed between P-type
23 layer 20 and N-type layer 19. Again, assuming that
24 the resistor symbol seen in Figure 6 is the resistor
25 D2 in Figure 5.

1 I don't know if you want to spend more
2 time. We can look at what specifically the layers 19
3 and 20, what types they are, N or P.

4 So if I look at column 10, it says layer 19
5 as illustrated is N-type impurities. So that's
6 exactly what I just said.

7 And then column epitaxial layer 20 is
8 P-type. Again, that's exactly what I just said
9 guessing. But that's confirmed in column 10, lines
10 20 through 22.

11 BY MR. JONES:

12 **Q. So with that understanding, let me try**
13 **again. But is the anode of D2 connected directly to**
14 **node T?**

15 MR. ANDERSON: Objection. Form.

16 THE WITNESS: Again, assuming that R2 is
17 the resistor seen in Figure 6, then yes, the P-type
18 material would be connected to node T. That would be
19 material 20.

20 And then 19 would be the cathode of diode
21 D2, which would be connected to ground.

22 BY MR. JONES:

23 **Q. In Figure 5, is the value of Vee a negative**
24 **value?**

25 A. I believe it is. That's my understanding.

1 Vee is a negative value, but I don't see it specified
2 in a specification with my quick glance.

3 **Q. Is Vee a signal notation that's commonly**
4 **used for the negative voltage for ECL circuits?**

5 A. Yes.

6 **Q. And I think you said that typically**
7 **operates in the range from negative .8 volts to**
8 **negative 1.5 volts?**

9 A. No. Vee is a terminating voltage that's
10 different than the logic swing voltages.

11 So if memory serves, for 100k ECL VE is
12 minus 2 and for 10k ECL VE is like minus 5. But it's
13 been like 30 years since I've designed something with
14 ECL.

15 **Q. Is that a term that's used in CMOS**
16 **circuits?**

17 A. In CMOS only, no. In circuits interfacing
18 CMOS and ECL, I would say could be.

19 **Q. Are you familiar with any major process**
20 **today that uses ECL process? Semi-conductor process.**

21 A. I mean, there's foundries that fabricate
22 the legacy ECL products. Fairchild is an example.
23 Motorola had fabs that fabricate ECL. I haven't kept
24 up on where they're doing the fabrication now. So I
25 can't say right off the top of my head.

1 **Q. Okay.**

2 A. And when we get a chance, can we take a
3 break?

4 **Q. Sure. Do you mind if I finish off like two**
5 **or three minutes?**

6 A. Yes.

7 **Q. Just say yes to everything. That's a joke.**

8 A. Yes.

9 **Q. I won't ask you yeses or nos just because I**
10 **said that.**

11 **Is it your understanding that most of the**
12 **major semi-conductor processes being used today are**
13 **done according to CMOS process?**

14 A. When you say -- the language is a little
15 awkward. When you say being used today, there's lots
16 of foundries that are fabricating chips that have
17 been around for 30, 40 years.

18 So are you talking about like process
19 development right now, or stuff that's already been
20 around for a while?

21 **Q. I meant new chips that are being made,**
22 **designed and made today. Not legacy production. Not**
23 **legacy products.**

24 MR. ANDERSON: Objection. Form.

25 THE WITNESS: In general, it's CMOS.

1 That's more than 90 percent of what the technology is
2 used for chips. But there are still semi-conductor
3 processes being developed for niche markets, like
4 silicon carbide, gadolinium nitride, some high-speed
5 bipolar process that might implement ECL.

6 But the majority of the process technology
7 focuses on fine line CMOS.

8 MR. JONES: So let's break here. We'll
9 have to continue this a little bit, but we can stop
10 and then come back.

11 (A recess was taken from 11:04 a.m.
12 to 11:11 a.m.)

13 BY MR. JONES:

14 Q. I would like to basically just get a list
15 of differences between ECL and CMOS.

16 Are you comfortable just answering that, or
17 should I walk you through?

18 A. With the technology differences?

19 Q. Sure.

20 A. Okay. So CMOS uses MOS transistors, like
21 17 in Figure 5 of Uda.

22 ECL uses bipolar junction transistors. Let
23 me see if I can find one of those in Uda.

24 So for example, in Uda, Figure 58, Q3 and
25 Q4, are bipolar junction transistors.

1 And then QP1 and QP3, for example, are PMOS
2 transistors. And then MN5 and MN7 are NMOS
3 transistors.

4 So if we have ECL only, we would only have
5 the bipolars. If we have CMOS only, we would only
6 have the NMOS and the PMOS transistors.

7 And if we have both, as in Uda in figure
8 58, we have both bipolar transistors, NMOS
9 transistors, and PMOS transistors.

10 **Q. Okay. You mentioned, when you were talking**
11 **about manufacturing of products in niche markets, I**
12 **think that ECL is typically faster than CMOS; is that**
13 **right?**

14 MR. ANDERSON: Objection. Form.

15 THE WITNESS: Well, it was true 30 years
16 ago or so. I don't think that's true nowadays.

17 BY MR. JONES:

18 **Q. Is there a difference in the power**
19 **consumption between circuits implemented using ECL**
20 **versus CMOS?**

21 MR. ANDERSON: Objection. Form.

22 THE WITNESS: I can't answer that. It
23 depends on the application.

24 BY MR. JONES:

25 **Q. Looking at Figure 5 of Uda, Figure 5 has a**

1 resistor R1. Can we turn to that.

2 A. Yes.

3 Q. And Vee, I think you said you understand to
4 be a negative voltage; is that right?

5 A. That's what I said, yes. I don't recall
6 seeing it discussed in the -- oh, it's there in
7 column 9 roughly, line 32, Vee with a negative
8 voltage of about minus 4 volts.

9 Q. Okay. And so whatever voltage exists on T,
10 it will be dissipated to Vee; is that right?

11 MR. ANDERSON: Objection. Form.

12 THE WITNESS: No. Can you give me a
13 specific example? Because if the power's off in the
14 circuit, then T, just like all voltages in the
15 circuit, will go to the resting or ground state.
16 Because that's the reference for voltage, is whether
17 it's positive or negative.

18 BY MR. JONES:

19 Q. So let me ask a little precise and
20 different question.

21 So if power is on in the circuit and the
22 fuse is not programmed, then resistor R1 will consume
23 power, right?

24 A. Yes. T will be shorted to ground through
25 fuse 16, Figure 5. And if Vee is nonzero, and R1 is

1 not infinite, then R1 will consume power.

2 Q. Couldn't the designers of Figure 5,
3 couldn't they have designed R1 as an NMOS or some
4 sort of switch that would be a lower power consuming
5 edition of the same functionality?

6 MR. ANDERSON: Objection. Form.

7 THE WITNESS: I think the answer is no. R1
8 is a terminating resistor used to transmit a
9 transmission line.

10 But let me look at the specification and
11 see how it describes R1 in Figure 5.

12 So if R1's resistance was made higher, then
13 it would dissipate less power, assuming everything
14 else is the same, with T being shorted to ground
15 through fuse 16 in Figure 5 of Uda.

16 BY MR. JONES:

17 Q. So let me make sure I understand the
18 relationship. The higher the resistance of R1 is,
19 the less power is consumed?

20 A. Assuming everything else is the same, yes.

21 Q. And the opposite is true, I assume?

22 A. Yes.

23 Q. I want to -- let me shift gears a little
24 bit. One thing on McAdams that I meant to ask
25 before -- do you have McAdams in front of you?

1 A. Yes.

2 Q. In column 1, the second paragraph is, when
3 talking about the goals of the patent or the problem
4 that it solved. Can you describe those to me,
5 generally.

6 A. So in semi-conductor memory, when they're
7 fabricated, there will be faulty rows and/or columns
8 in the memory.

9 And so what's done to ensure that the
10 memory still functions with all bits working is to
11 swap out the faulty row and/or column with a
12 redundant row and/or column, and the way this is done
13 is by remapping the address that's applied to the
14 part to do the remapping, a fuse is used.

15 In the prior way of implementing the
16 circuitry to read out the state of the fuse, it talks
17 about, in the second paragraph, using, for example, a
18 long channel MOS transistor to minimize the current
19 through the fuse.

20 Another way it talks about is using a clock
21 to gate an MOS transistor so that the value of the
22 fuse is clocked in.

23 And then the way McAdams teaches is to use
24 a latch that will latch or represent the state of the
25 fuse and, thus, not need an external signal, like a

1 clock, or dissipate any quiescent current as one
2 would get using a long L-transistor sensing the state
3 of the fuse.

4 Q. And doesn't it say that the one undesirable
5 result of the prior techniques at line 25 is that
6 they consume too much power?

7 A. It indicates that using the long
8 L-transistor or the external clock signal would
9 consume tens of micrograms of current. So that would
10 consume power, yes.

11 Q. And in fact, the next paragraph says it is
12 the principal object in the invention to reduce power
13 consumption, right?

14 A. Not precisely. But it says that the
15 principal objective of this invention is to improve
16 the performance by using less current so that the
17 stand-by power dissipation is lower.

18 Q. And McAdams is only teaching CMOS
19 circuitry, right?

20 A. Yes.

21 Q. Turning back to the '492 patent, claim 1,
22 the diode element.

23 A. Okay.

24 Q. There's some claim language which is a
25 predetermined range of values.

1 A. Yes. The last element of claim 1.

2 Q. Yes. And what is your understanding of
3 what it means to be within a predetermined range of
4 values?

5 A. That the diode would limit the voltage on
6 the terminal T1 to within a diode drop of the voltage
7 on Vcc.

8 So for example, if the voltage on Vcc were
9 ground, then T1 would be limited to .7, whereas if
10 the voltage on Vcc was 5, then T1 would be limited to
11 5.6, 5.7.

12 Q. Now, I understand that it's your opinion
13 that the VAP would meet the claim element. But I'm
14 wondering about the breadth of this claim term,
15 predetermined range of values.

16 If there's, for example, a diode in series
17 with a resistor, then the value of the voltage on T1
18 would be more than the diode threshold lower than the
19 VINT; isn't that right?

20 MR. ANDERSON: Objection. Form.

21 THE WITNESS: I haven't formed an opinion
22 on using a resistor in series with a diode, but just
23 sitting here right now, I don't think that would
24 work.

25 I mean, if you look at column 3, work to

1 meet the claim language, if you look at column 3, and
2 you look at the discussion around starting at the
3 paragraph on roughly line 33, talks about the PN
4 junction limiting the voltage on VINT to a threshold
5 voltage above -- I'm sorry, limiting the voltage on
6 T1 to a threshold voltage of VINT.

7 I think if you put a resistor in series
8 with a diode that when the current flows through the
9 resistor, then the voltage will change with the
10 current flowing in the resistor.

11 So I don't think that would meet the claim
12 language, but I haven't formed an opinion on that.

13 BY MR. JONES:

14 Q. I'm trying to understand your understanding
15 of this claim term, and whether it requires the
16 predetermined range of values to be precisely one
17 diode drop below the first voltage, or whether this
18 claim element is met for some other values other than
19 that one diode threshold drop.

20 MR. ANDERSON: Objection. Form.

21 THE WITNESS: The claim 13, for example,
22 talks about predetermined range consists of all
23 voltages below a predetermined value.

24 If you put a resistor in series with a
25 diode, then the value is going to change with the

1 voltage drop across the resistor.

2 Whereas, if you use just a diode or some
3 other clamping element, or two diodes, for example,
4 or three diodes, then the value will change. But it
5 will still be a predetermined value.

6 And then outside of that value, you're
7 limiting, or if you try to go outside that value,
8 you'll limit the node T1.

9 So I don't think it necessarily has to be
10 implemented with one diode. But it has to be below
11 some value. The value can't be changing so that the
12 range changes.

13 BY MR. JONES:

14 **Q. Okay. So your point is that the upper end**
15 **of the range is a particular value that does not**
16 **change. But that upper value, that upper end of the**
17 **range doesn't have to be exactly one diode threshold**
18 **below the first voltage?**

19 MR. ANDERSON: Objection. Form.

20 THE WITNESS: Well, kind of. I think, if
21 you want to be more precise, you could say that
22 the -- for example, the voltage on T1 needs to be one
23 diode threshold below the power supply voltage. But
24 I think if you have two diodes there, that would meet
25 the claim language as well.

1 But I think if you have a diode and a
2 resistor, it wouldn't meet the claim language because
3 then the upper bound would not be below a
4 predetermined value. Vcc plus .7, for example.

5 But variable depending on the resistance
6 and the current flowing through the resistance.

7 BY MR. JONES:

8 Q. And the same is true not just for resistor,
9 but for like a contact as well, right? That has an
10 inherent resistance to it, the voltage drop across
11 the contact would vary based on the current flowing
12 through it, right?

13 MR. ANDERSON: Objection. Form.

14 THE WITNESS: There might be a few
15 millivolts changed, but I don't think practically
16 that's an issue, because you could also argue that
17 wires have resistance.

18 And so there's a voltage drop across a
19 wire. I don't think that's really relevant, to be
20 honest.

21 BY MR. JONES:

22 Q. Okay. Let's talk about the Joo reference
23 again. I think I already gave it to you.

24 A. Yes.

25 Q. And these questions relate to your 781

1 **declaration.**

2 A. Okay.

3 **Q. Around page 56 of 120.**

4 A. Okay.

5 **Q. And then -- I'm looking across the table at**
6 **you, I think -- I guess seeing that number it would**
7 **be page 53.**

8 A. Oh, sorry. Okay.

9 **Q. That would make more sense that way.**
10 **So are you familiar with the term "body**
11 **diode"?**

12 A. Yes.

13 **Q. What is a body diode?**

14 A. If we look at the figure 4.35 on page 56 or
15 59 of 120. The body of the PMOS transistor is the
16 N-well seen in that figure 4.35. And the body diode
17 would be the diode that's formed between that N-well,
18 or the body of the PMOS, and the P-substrate.

19 **Q. Is the body diode shown in schematic form**
20 **on this figure?**

21 A. Yes.

22 **Q. Which symbol is it?**

23 A. It's the lowest diode on the right, just
24 slightly above and to the left of the P-substrate
25 label.

1 Q. Okay. And it's flowing up, right? The
2 anode is on the bottom, the cathode is on the top for
3 the one that you're talking about, right?

4 A. Yes.

5 Q. And what's happening at that interface
6 between the N-well and the P-substrate that makes it
7 a diode?

8 A. There's a PN junction.

9 Q. Okay. I understand that makes it a diode.
10 But what's happening with the flow of electrons, or
11 physically that makes that a diode?

12 MR. ANDERSON: Objection. Form.

13 THE WITNESS: If the P-substrate becomes
14 more positive than the N-well, the diode that we're
15 talking about turns on and conducts current.

16 Whereas, if the N-well is at a higher
17 potential than the P-substrate, which is normal
18 operation, then the diode is reverse biased, and no
19 current flows.

20 BY MR. JONES:

21 Q. And you also have drawn above that diode we
22 just talked about, you've drawn two other diodes,
23 which are facing the other way between the source and
24 drain of a transistor and the N-well that they're in;
25 is that correct?

1 A. Yes.

2 Q. Do you refer to those as body diodes?

3 A. One may refer to them as body diodes, but
4 generally they're referred to as the source body
5 diode or the drain body diode.

6 But I wouldn't be -- I mean, I don't think
7 it would be entirely incorrect to say it's a body
8 diode because the body is used as part of the diode.

9 Q. And at each of those interfaces, there's a
10 PN junction as well, right?

11 A. Yes.

12 Q. And that's why you say that each of those
13 interfaces creates a diode, right?

14 A. Yes.

15 Q. And on page -- well, three pages prior,
16 which is 56 of 120, you've drawn two diodes at the
17 interface between the source or drain and the body,
18 right?

19 A. Yes.

20 Q. Is that true for every PMOS transistor,
21 there's necessarily a source body diode and a drain
22 body diode?

23 A. Yes. And CMOS transistors, which are
24 fabricated in the bulk, or in a way for there has to
25 be a P plus N junction for the source and drain to

1 the body of the -- here the end substrate of the PMOS
2 device.

3 **Q. Just more fundamentally, is every PN**
4 **junction a diode necessarily?**

5 MR. ANDERSON: Objection. Form.

6 THE WITNESS: Yes. But if you give me some
7 example, I'll see if I can find some way that's not
8 true. But I think a PN junction is a diode, yes.

9 BY MR. JONES:

10 **Q. Is there any other way to form a diode**
11 **other than forming a PN junction?**

12 A. Yes.

13 **Q. Can you give me an example?**

14 A. Metal semi-conductor junction. If the
15 semi-conductor is lightly doped, it can form what's
16 called a Schottky or rectifying junction, which is a
17 diode.

18 **Q. Looking at page 54 of 120.**

19 A. Okay.

20 **Q. I want to make sure I understand your**
21 **opinion. Is it your opinion that Joo alone teaches**
22 **this element, this diode element, at the top of this**
23 **page?**

24 A. To the extent that the PMOS transistor in
25 Joo is laid out to include the diode, then Joo could

1 teach it alone.

2 But I don't think that's clearly detailed.
3 That's why I brought in Weste. And if we look at
4 figure -- I have a cross-sectional view of a figure
5 where I've used Weste to show the P-plus in an
6 N-well to implement the diode. And I'm trying to
7 find it.

8 **Q. Take your time. But I am interested in**
9 **seeing it and discussing it so...**

10 A. All right. I put this in the other
11 declaration, but it's in the McAdams declaration on
12 page 122 of 136, or page 119.

13 **Q. Okay. I have it here.**

14 A. So we see simply by putting the P-plus in
15 the N-well, that a diode is formed, which will
16 connect node 14 of McAdams to Vdd.

17 Also, with the '492 implementation, it
18 would be node out in Figure 2A to V internal.

19 So it's just simply adding the P-plus in
20 the N-well.

21 **Q. In this particular example, is the N-well**
22 **at Vdd?**

23 A. Yes. And the substrate is at ground.

24 **Q. And so the junction at the topmost**
25 **P-well -- I'm sorry, would you call it a P-well or**

1 a --

2 A. A P-plus region. The plus indicates that
3 it's heavily doped, so when you make a connection to
4 metal, it's not rectifying or a Schottky contact.

5 Q. Okay. So the interface between that
6 topmost P-plus region and the N-well that it's in,
7 that diode has an anode that's node 14 and a cathode
8 that's Vdd?

9 A. Yes. Power supply Vcc or Vdd.

10 Q. So I want to go back to 781, the Joo
11 discussion we were having.

12 A. Okay.

13 Q. And I mean, we were, I think, at page 54 of
14 120.

15 A. Okay.

16 Q. And ask if it's your opinion that Joo alone
17 teaches this element?

18 MR. ANDERSON: Objection. Form.

19 THE WITNESS: Joo alone doesn't teach
20 adding the diode as a detail. That would be
21 something that would just be adding an extra P-plus
22 region to the body of the NP1.

23 But Joo alone doesn't teach that. I mean,
24 a person of ordinary skill in the art would know how
25 to do that. It's simply adding P-plus to the N-well.

1 BY MR. JONES:

2 Q. The transistor MP1 in Joo does have, as we
3 talked about, two diodes, right? It has a source
4 body diode and a drain body diode?

5 A. Yes.

6 Q. And why would that, either of those diodes,
7 not meet this claim element?

8 A. Those are the source and drains of the
9 PMOS. So those are connected to the transistor.

10 So you would need to have the P-plus, as I
11 detailed in the other declaration, page 119 or page
12 122 of 136, where the N-well would have a P-plus for
13 a separate connection, because the source and drain
14 connections are already going to other places in the
15 circuit.

16 Q. I'm trying to understand how and perhaps --
17 this is page 59 of 120. The Joo, I'm trying to
18 understand what would need to change in the Joo
19 circuit in order to meet the claim element.

20 I know you tried to explain that, so I
21 apologize for the same thing. But can you help me
22 understand better, hopefully with reference to the
23 declaration, the Joo declaration, what manipulation
24 would need to occur?

25 A. It's quite simple.

1 **Q. Sure.**

2 A. I'll just draw it on the side here as a
3 P-plus. And that goes to Vcc. And then that would
4 provide a diode like this to Vcc.

5 So you just add a P-plus, just like it's
6 drawn in the other declaration. Of course the P-plus
7 would be at the top. I just kept it real simple.

8 **Q. And the diode, the anode of the diode is**
9 **always the P-type region? Is that right?**

10 A. I'm sorry. I mislabeled this. This
11 doesn't go to Vcc. It's already connected to Vcc.
12 It goes over to the input. We'll just call it X
13 here; X. It's simpler if you look at page 122 of 136
14 in the other declaration.

15 **Q. Okay. So in order to meet the claim**
16 **element, a person of skill in the art would need to**
17 **add a P-type region in the correct place near MP1 and**
18 **that P-type region would need to connect to the node**
19 **N2; is that correct?**

20 MR. ANDERSON: Objection. Form.

21 THE WITNESS: Well, it's discussed in the
22 declaration. But in real simple terms, all you do is
23 put a P-plus in the N-well. Tie that P-plus to node
24 14 in McAdams, for example. Or across the fuse to
25 node X in Figure 2.

1 Just in simple terms, you just add a P-plus
2 to the N-well.

3 And because I'm doing this on the fly, and
4 I haven't written this in the declaration, give me a
5 second, because the diode I've drawn here may
6 actually need to be connected there to connect to
7 meet the claim language.

8 And again, I haven't written this up here.
9 So give me a second and I'll -- I mean, the takeaway
10 is the P-plus. You just add a P-plus to the N-well.
11 BY MR. JONES:

12 Q. Sure. As you're doing that, and maybe this
13 is for Paul too, but it's important to get the
14 correct answer today.

15 And, Dr. Baker, you should understand
16 procedurally it's our position that Samsung's case
17 will be limited; that the 781 IPR concerning Joo will
18 be limited to specifically to what's written in your
19 781 declaration.

20 I'm sure Paul would object and argue
21 otherwise.

22 But at least today my purpose in this is to
23 at least get your full and accurate opinion on this.
24 So take the time you need. But hopefully, for your
25 sake, you can tie that into the 781 declaration

1 somehow in our discussion.

2 A. Oh, I thought I was. I was simply -- it
3 seems like the discussion is very clear here --

4 Q. Okay.

5 A. -- on how the combination of Joo and Weste
6 would be implemented.

7 I was simply trying to explain to you and
8 be helpful as to how P-plus would have been included
9 in another way that I've described in one of the
10 other declarations.

11 But I mean, we can stick to this
12 declaration, and I think that the combination is
13 clear. If we look at the figure on page 61 of 120,
14 that we can see the diodes that meet the claim
15 language, and the connection of the fuse and the fuse
16 to Vcc.

17 I was simply -- perhaps I shouldn't have
18 been, but I was trying to be helpful and explain how
19 another diode could be implemented based upon what I
20 did in the other declaration.

21 Q. Okay. So I must have misunderstood. I'm
22 not trying to push you into saying that it wasn't in
23 your declaration.

24 But let's talk about that. Page 61 of 120,
25 I think you've just referenced it.

1 A. Yes.

2 Q. And how that picture on the top of that
3 page meets the claim element, then. And I think that
4 would be more appropriate.

5 Which diode meets the claim element?

6 A. The diode that's in blue that's connected
7 from N2 to Vcc. That's labeled body diode.

8 Q. And does that diode exist in MP1 of Joo?

9 A. Yes.

10 Q. Okay. So is it your opinion that Joo alone
11 meets the claim element?

12 A. I think the answer is yes, but I think that
13 it may be more clear to bring in Weste to make sure
14 that it was really clear.

15 Q. I'm asking it another way. Is it possible
16 to make MP1 in such a way that there is not a diode
17 across the fuse?

18 MR. ANDERSON: Objection. Form.

19 THE WITNESS: If you look at MP1 in there,
20 it's not possible. There's a P-plus connected to N2.
21 There's the N-well and N-plus that are tied to Vcc,
22 which is the body of MP1. So the answer is no.

23 BY MR. JONES:

24 Q. So in Joo, for each of the transistors,
25 there's actually two PMOS, two NMOS, and an inverter,

1 which is presumably made of two or more transistors.

2 Each of the transistors in that circuit has
3 two diodes, right?

4 MR. ANDERSON: Objection. Form.

5 THE WITNESS: There's a parasitic diode
6 between the source and drain, and the body of all of
7 these MOS transistors, yes.

8 BY MR. JONES:

9 Q. I guess because you have a clean copy of
10 Joo, can I ask you to draw in where each of those
11 parasitic diodes would be on Joo Figure 2? And it
12 may be better on Figure 2 if you turn, just because
13 it's bigger.

14 A. (Witness complies.) Just for the PMOS?

15 Q. For the NMOS, too. For I guess all of the
16 transistors that are shown.

17 A. It's the same as what's drawn on page 61 of
18 my declaration. Sorry it's not as clear as I would
19 like. But also I'll just write...

20 Q. I'm going to take my pen back.

21 A. Oh, sorry.

22 Q. Thanks.

23 A. It's clearer on the figure that I have on
24 page 61 of 120 of the declaration, but I tried to
25 draw the same thing.

1 Q. Okay. And then I assume MN2 will have also
2 two diodes to ground?

3 A. Yep.

4 Q. Just for completeness.

5 A. (Witness complies.)

6 MR. JONES: So I said we wouldn't do this,
7 but I'm going to mark this as an exhibit because it's
8 a unique document now. So could we put Exhibit 1 on
9 this.

10 MR. ANDERSON: Unless you want to start
11 where you guys are going to be at for consistency.
12 You guys usually start with 2000.

13 MR. BANSAL: Do you want me to give you
14 your last exhibit number?

15 MR. JONES: Yeah. If it's handy and you
16 can pull it up.

17 MR. ANDERSON: Otherwise it gets kind of
18 weird.

19 MR. JONES: Actually, so I'm going to mark
20 it only in the 781 IPR because it's Joo, so I'll mark
21 it 2002.

22 MR. BANSAL: That's fine.

23 MR. JONES: Which I don't think we've used
24 yet.

25 MR. BANSAL: No. That's okay.

1 (Exhibit 2002 was marked for
2 identification.)

3 MR. JONES: And we indicated it's for the
4 781 IPR. It's on the record, so we'll be fine.

5 MR. ANDERSON: Yep.

6 MR. JONES: I think we're done with this
7 document, but here's the rest -- why don't we go off
8 the record.

9 (A recess was taken from 12:15 p.m.
10 to 12:25 p.m.)

11 MR. JONES: So I have no more questions.
12 Thank you, Dr. Baker.

13 MR. ANDERSON: I have no questions. Thank
14 you.

15 - - -

16 (The deposition was concluded at 12:25 p.m.)

17 - - -

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1 CERTIFICATE OF REPORTER

2 I, the undersigned, a Certified Shorthand
3 Reporter of the State of Nevada, do hereby certify:

4 That the foregoing proceedings were taken
5 before me at the time and place herein set forth;
6 that any witnesses in the foregoing proceedings,
7 prior to testifying, were duly sworn; that a record
8 of the proceedings was made by me using machine
9 shorthand which was thereafter transcribed under my
10 direction; that the foregoing transcript is a true
11 record of the testimony given to the best of my
12 ability.

13 Further, that before completion of the
14 proceedings, review of the transcript [X] was
15 [] was not requested pursuant to NRCP 30(e).

16 I further certify I am neither financially
17 interested in the action, nor a relative or employee
18 of any attorney or party to this action.

19 IN WITNESS WHEREOF, I have this date
20 subscribed my name.

21
22 Dated: October 28, 2019

23
24 

25 GALE SALERNO, RMR, CCR #542

DECLARATION UNDER PENALTY OF PERJURY

Case Name: Samsung Electronics vs. Promos Technologies

Date of Deposition: 10/25/2019

Job No.: 10061825

I, R. JACOB BAKER, PH.D., P.E., hereby certify
under penalty of perjury under the laws of the State of
NEVADA that the foregoing is true and correct.

Executed this 13th day of
NOVEMBER, 2019, at LAS VEGAS.



R. JACOB BAKER, PH.D., P.E.

NOTARIZATION (If Required)

State of _____

County of _____

Subscribed and sworn to (or affirmed) before me on
this ____ day of _____, 20__,

by _____, proved to me on the
basis of satisfactory evidence to be the person
who appeared before me.

Signature: _____ (Seal)

DEPOSITION ERRATA SHEET

Case Name: Samsung Electronics vs. Promos Technologies

Name of Witness: R. Jacob Baker, Ph.D., P.E.

Date of Deposition: 10/25/2019

Job No.: 10061825

Reason Codes: 1. To clarify the record.
2. To conform to the facts.
3. To correct transcription errors.

Page 14 Line 12 Reason 1From out (lowercase) to OUT (upper-case)Page 15 Line 9 Reason 1From V OUT to OUTPage 27 Line 15 Reason 1From raise to lodge to rise to latch???Page 36 Line 15 Reason 1From to to ofPage 49 Line 4 Reason 1From gadolinium to galliumPage 52 Line 8 Reason 3From TRANSMIT to TerminatePage 54 Line 9 Reason 3From Micrograms to MicroampsPage 57 Line 4 Reason 1From will change to will not change

Page _____ Line _____ Reason _____

From _____ to _____

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1 DEPOSITION ERRATA SHEET

2 Page _____ Line _____ Reason _____

3 From _____ to _____

4 Page _____ Line _____ Reason _____

5 From _____ to _____

6 Page _____ Line _____ Reason _____

7 From _____ to _____

8 Page _____ Line _____ Reason _____

9 From _____ to _____

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20 Page _____ Line _____ Reason _____

21 From _____ to _____

22 X Subject to the above changes, I certify that the
transcript is true and correct

23 _____ No changes have been made. I certify that the
transcript is true and correct.

24 _____

25 R. Jacob Baker
R. JACOB BAKER, PH.D., P.E.

1 1 6:11,14,16,21 7:8, 20,22 9:12,14,21 15:14 16:3 21:4,10 25:6,7,11,13,16,22 26:2,6,9,11,13 27:14,16,24 30:3,9, 13,16,17 31:10,13, 14,20,24,25 33:13 34:1,16 35:10,21 36:2,3 53:2 54:21 55:1 71:8 1.5 38:21 47:8 10 38:9 45:8,9 46:4,9 1001 5:21,22 1006 26:25 27:1 1007 38:2,3 100k 47:11 1010 22:22,23 10k 47:12 11 28:1,3,6,18,19,23 29:4,8,10 31:13 32:15,19 33:16 35:18 36:25 37:4,22, 23 38:9 110 13:7 14:3,13,14, 18,21,22,25 29:17, 19,22 30:5,9,10,19 31:9,14,23 32:20 33:17 34:14,17,19, 25 35:19 119 63:12 65:11 11:04 49:11 11:11 49:12 120 59:3,15 61:16 62:18 64:14 65:17 68:13,24 70:24	122 63:12 65:12 66:13 12:15 72:9 12:25 72:10,16 13 56:21 136 63:12 65:12 66:13 14 27:20,23 28:5,17 29:1,7 32:18 33:24 35:21,25 36:1,3,5, 12,17,24 63:16 64:7 66:24 16 51:25 52:15 17 42:5 49:21 18 40:10,12 43:22,23 44:4 45:10,17 19 40:10,16,17 43:18, 20,22,24 45:20,21, 23 46:2,4,20 2 2 6:14 23:7,14,18,19, 21 24:7,19,23 25:21 27:6,21 28:16,22 30:13 32:13 33:3,10 34:5 38:11,12 43:7 47:12 66:25 70:11, 12 20 40:10,20 43:18,20, 24 45:9,19,20,23 46:3,7,10,19 2000 71:12 2002 71:21 72:1 2019 4:2 21 27:7 28:22 212 10:2 20:19 21:6 22 46:10	22A 41:15 230 10:10,15,23 11:8 234 9:23 24 20:3 25 4:2 54:5 26A2 41:14 27 27:21 27A2 41:9,12,14 29 29:1 2A 9:9,10,14 10:10,16 14:8 15:20,23 19:17 20:14,20 29:11,20 30:2 31:23 34:1 35:9 63:18 3 3 9:24 11:10 55:25 56:1 30 47:13 48:17 50:15 32 51:7 33 9:25 56:3 333 11:12 34 28:22 29:1 346 33:25 36 20:3 38 33:3 39 27:14 4 4 25:19 51:8 4.35 59:14,16 40 30:16,17 48:17 43 7:9,20	44 7:20 45 23:12 46 21:10 47 34:5 49 11:13 492 4:15,19 5:21 6:7, 15 7:9,12 19:23 24:4,20 27:11,14 29:11,20 30:2,4,13, 17,22 31:2,8,15,16, 25 32:2,20,25 33:10, 17 34:1,2,5 35:5,19, 21 54:21 63:17 5 5 7:24,25 35:5,11 36:6 38:5,8,10 40:4 41:2,18 42:2,11 44:18,19,24,25 45:19,25 46:23 47:12 49:21 50:25 51:25 52:2,11,15 55:10 5.6 55:11 5.7 55:11 50 21:10 51 35:5 36:6 53 59:7 54 62:18 64:13 56 59:3,14 61:16 58 49:24 50:8 59 59:15 65:17 6 6 10:3,4,9,12,15,22 11:9 20:20 35:9,10
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