Trials@uspto.gov
571-272-7822

Paper 6
Entered: September 11, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2019-00780
Patent 6,163,492

Before KEVIN F. TURNER, JO-ANNE M. KOKOSKI, and JULIA HEANEY, *Administrative Patent Judges.*

KOKOSKI, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 1–13 of U.S. Patent No. 6,163,492 ("the '492 patent," Ex. 1001). Paper 1 ("Pet."). ProMOS Technologies, Inc. ("Patent Owner") did not file a Preliminary Response.

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314; *see* 37 C.F.R. § 42.4. Upon consideration of the Petition and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least 1 claim of the '492 patent. Accordingly, we institute an *inter partes* review of claims 1–13 of the '492 patent.

A. Related Proceedings

The parties indicate that the '492 patent is being asserted in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:18-cv-00307-RGA (D.Del.), and is the subject of IPR2019-00779 and IPR2019-00781, also filed by Petitioner. Pet. 1; Paper 5, 1.

B. The '492 Patent

The '492 patent is titled "Programmable Latches That Include Non-Volatile Programmable Elements." Ex. 1001, at [54]. According to the '492 patent, "[p]rogrammable latches with fuses are used in integrated circuits to enable modification of the circuits without changing the masks used for circuit fabrication." *Id*. at 1:19–21. An example of such a prior art latch is depicted in Figure 1 of the '492 patent. *Id.* at 1:24–25. The '492 patent

explains that during operation of the latch of Figure 1, the output terminal OUT will be pulled to VDD if fuse F1 is intact. *Id.* at 1:32. If fuse F1 is blown, then transistor 110 will be turned on and keep output terminal OUT at ground. *Id.* at 1:34–35. The '492 patent explains that when the power is off, output terminal OUT is floating and may provide an unstable or erroneous voltage. *Id.* at 1:38–47. In the prior art latch of Figure 1, bypass capacitor 130 is intended to avoid such malfunction and insure correct initialization of the latch on power-up. *Id.* at 1:36–55. "During power up, capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown." *Id.* at 1:49–52.

The '492 patent further describes how "[d]ependence on delays is undesirable because delay-dependent circuits may not operate properly if VDD rises slowly." *Id.* at 1:63–65. Thus, according to the '492 patent, programmable latches such as those described in the specification are more reliable "because they do not depend on delays such as delays provided by capacitor 130." *Id.* at 62–63. In particular, "[h]igh reliability is achieved in some embodiments by a diode that keeps a voltage on a latch output terminal within a predetermined range of values before power is supplied to the latch." *Id.* at 2:1–4.

Figure 2A of the ’492 patent is reproduced below.

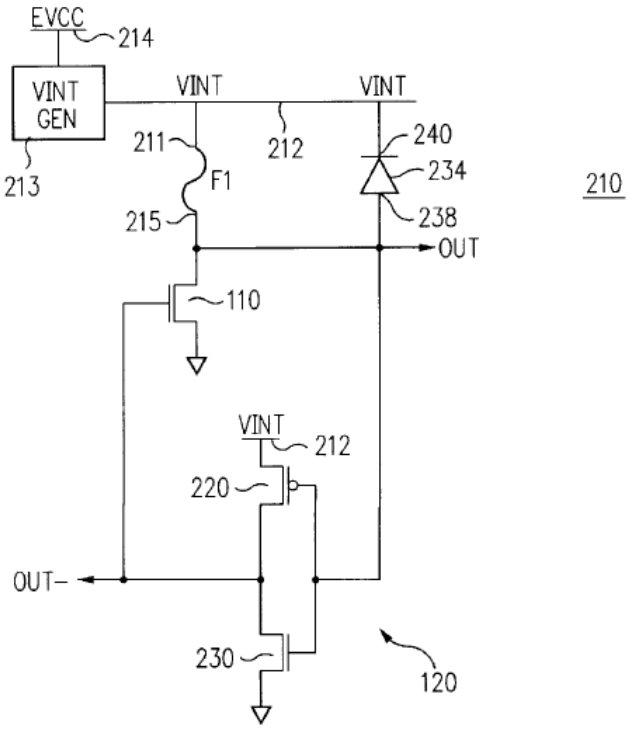

FIG. 2A

Figure 2A “is a circuit diagram of a programmable latch according to the present invention.” Ex. 1001, 2:64–65. Figure 2A shows a programmable latch 210 including a fuse F1, NMOS transistor 110, CMOS inverter 120, VINT generator 213, and diode 234. As depicted in Figure 2A, CMOS inverter 120 is formed by PMOS pull-up transistor 220 and NMOS pull-down transistor 230. *Id.* at 3:24–26.

In the embodiment of Figure 2A, output terminal OUT is connected to terminal 215 of fuse F1, the drain of NMOS[1] transistor 110, and anode terminal 238 of diode 234. *Id.* at 3:20–23. Thus, “[i]f fuse F1 is conductive, then terminal OUT is at VINT, and transistor 110 is turned off by inverter

[1] MOS stands for metal-oxide-semiconductor. Ex. 1015, 12.

120." *Id.* at 3:50–51. When the power is off, VINT terminal 212 is at ground, and diode 234 limits the voltage on terminal OUT to the threshold voltage of diode 234. *Id.* at 3:35–40. The threshold voltage of diode 234 is "below the trip voltage of inverter 120 and even below the threshold voltage of NMOS transistor 230." *Id.* at 3:42–43. "Therefore, if fuse F1 is blown, transistor 230 remains off when the power is turned on." *Id.* at 3:45–46. When the power is turned on, PMOS pull-up transistor 220 charges the gate of transistor 110 to its threshold voltage, and transistor 110 connects the terminal OUT to ground. *Id.* at 3:46–49.

C. Challenged Claims

Petitioner challenges claims 1–13 ("the challenged claims") of the '492 patent. Claim 1 is the only independent claim, and is reproduced below.

> 1. A programmable latch comprising:
>
> a first terminal for receiving a first voltage;
>
> a second terminal for receiving a voltage;
>
> a terminal T1 for providing a signal indicating a state of the programmable latch;
>
> a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;
>
> a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and

> a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Ex. 1001, 8:38–58.

D. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–13 of the '492 patent on the following grounds:

References	Basis	Challenged Claim(s)
McAdams[2] and Uda[3]	§ 103(a)	1–5, 8–10, 13
McAdams, Uda, and Keeth[4]	§ 103(a)	5–7
McAdams, Uda, and Weste[5]	§ 103(a)	11, 12
McAdams, Uda, and Tomishima[6]	§ 103(a)	9

Petitioner relies on the Declaration of R. Jacob Baker, Ph.D., P.E. ("Baker Declaration," Ex. 1002) in support of its contentions.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person having ordinary skill in the art ("POSITA") "would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design," and that "[m]ore education can supplement practical experience and vice versa." Pet. 5. For purposes of this Decision, we adopt

[2] U.S. Patent No. 4,621,346, issued Nov. 4, 1986 (Ex. 1006).
[3] U.S. Patent No. 5,519,658, issued May 21, 1996 (Ex. 1007).
[4] U.S. Patent No. 5,552,739, issued Sept. 3, 1996 (Ex. 1008).
[5] *Weste et al.*, Principles of CMOS VLSI Design: A Systems Perspective, 2d. ed. 1993 (Ex. 1009).
[6] U.S. Patent No. 5,604,710, issued Feb. 18, 1997 (Ex. 1013).

Petitioner's assessment of the level of ordinary skill in the art, which is consistent with the level of ordinary skill in the art at the time of the invention as reflected in the prior art in this proceeding. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Claim Interpretation

For petitions such as this one, filed after November 13, 2018, we apply the same claim construction standard "used in the federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), which is articulated in" *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 83 Fed. Reg. 51,340, 51,343 (Oct. 11, 2018). Under the *Phillips* standard, the "words of a claim 'are generally given their ordinary and customary meaning,'" which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312–13. Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner contends that "no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims." Pet. 9. For purposes of this Decision, based on the record before us, we determine that none of the claim terms requires an explicit construction.

C. Obviousness over McAdams and Uda

Petitioner contends that the subject matter of claims 1–5, 8–10, and 13 would have been obvious over the combined teachings of McAdams and Uda. Pet. 9–60. Petitioner relies on the Baker Declaration in support of its contentions. *Id.*

1. Overview of McAdams

McAdams "relates to semiconductor integrated circuit devices, and more particularly to fuse circuits of the type used in VLSI CMOS semiconductor memory devices or the like." Ex. 1006, 1:5–8. According to McAdams, the principal object of the invention is "to provide improved fuse circuits exhibiting a low current drain for use in semiconductor integrated circuits such as memory for microcomputer devices, particularly CMOS devices with low standby power dissipation and minimum complexity." *Id.* at 1:33–38.

Figure 1 of McAdams is reproduced below.

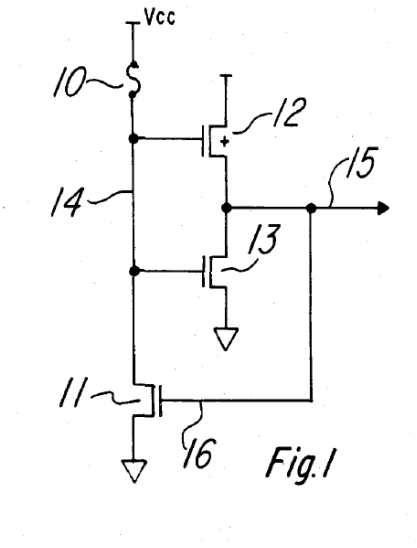

Figure 1 is an electrical circuit diagram of a CMOS fuse circuit according to one embodiment described in McAdams. *Id.* at 1:60–61. Fuse element 10 is

connected in series with N-channel feedback transistor 11, and this series circuit is connected between supply voltage Vcc and Vss. *Id.* at 1:67–2:3. A CMOS inverter including P-channel transistor 12 and N-channel transistor 13 has node 14 as an input and produces output 15. *Id.* at 2:3–6. "Feedback is provided from the output node 15 to the gate of transistor 11 by a line 16." *Id.* at 2:6–7.

McAdams explains that, as Vcc goes from zero to +5 volts during power-up, if the fuse has not been blown "node 14 follows Vcc since the node 15 starts at Vss potential and the transistor 11 is off." *Id.* at 2:8–11. Because node 14 follows Vcc, P-channel transistor 12 stays off, and as soon as Vcc and node 14 reach the N-channel threshold voltage Vtn, transistor 13 turns on, holding node 15 at Vss. *Id.* at 2:11–15. McAdams teaches that "[t]his quickly discharges to zero and capacitive coupling of voltage to the output node 15 at power-on due to the Vcc transition," and, "[t]hus the only current flowing through the fuse 10 from the Vcc supply is leakage current, on the order of nanoamps." *Id.* at 2:15–20. McAdams further explains that, when fuse 10 has been blown, node 14 is at Vss and P-channel transistor 12 turns on as soon as its threshold Vtp is reached, causing output node 15 to follow Vcc. *Id.* at 2:21–24. "Once the node 15 reaches the threshold Vtn, the transistor 11 turns on, keeping the node 14 at Vss," and "[a]ny capacitive coupling of voltage to node 14 from the Vcc transition is quickly discharged." *Id.* at 2:24–28.

2. Overview of Uda

Uda "relates to a semiconductor integrated circuit device having a redundancy circuit arrangement such as a static RAM (random access memory) incorporating redundancy technology, the RAM combining a

bipolar transistor with a CMIS (complementary metal-insulator-semiconductor) circuit arrangement." Ex. 1007, 1:12–17. Uda explains that "[i]f the semiconductor chip develops a faulty part, the backup element corresponding to that part takes over, thereby keeping the integrity of the chip intact." *Id.* at 1:34–37. Uda further explains that "switching between faulty parts and their backup elements in the semiconductor chip is accomplished by the melting of fuses constituting part of the redundancy circuit therein." *Id.* at 1:38–41.

Figure 5 of Uda is reproduced below.

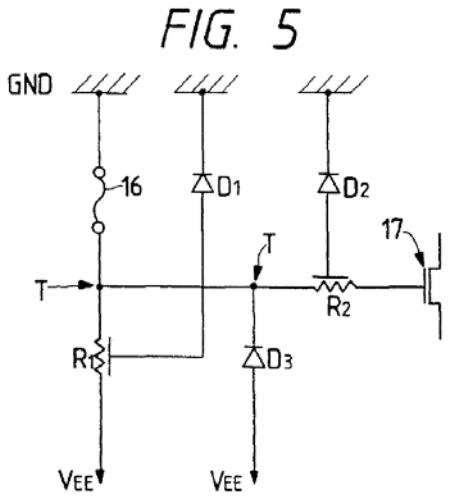

Figure 5 is a circuit diagram showing the fuse arrangement in one embodiment described in Uda. *Id.* at 5:25–26, 9:28–29. Fuse 16 and resistor R_1 are connected in series between ground line GND and power line V_{EE}. *Id.* at 9:29–31. Ground line GND is supplied illustratively with a voltage of about 0 V (Vcc), and power line V_{EE} is supplied with a negative voltage of about -4 V. *Id.* at 9:31–33. Terminals T between fuse 16 and resistor R_1 are connected to resistor R_2 and diode D_3, and resistors R_1 and R_2 are connected ground line GND via diodes D_1 and D_2. *Id.* at 9:37–40.

Terminals T "are further connected to the gate electrode of, for example, an n-channel MOSFET (called nMOS) 17 via the resistor R_2." *Id.* at 9:40–43.

Uda teaches that diodes D_1, D_2, and D_3 and resistor R_2 are provided "to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the MOS gate." *Id.* at 9:44–47. In that regard, Uda teaches that "[i]f a positive charge develops, the charge is led to the ground line GND via the diodes D_1 and D_2," and "if a negative charge occurs, the charge is to the power line V_{EE} via the diode D_3." *Id.* at 9:48–51. According to Uda, "[a]ny residual charge loses its energy when entering the resistor R_2, whereby the MOS gate is protected from destruction." *Id.* at 9:51–53.

3. Analysis

Petitioner asserts, with supporting testimony from Dr. Baker, that the combined teachings of McAdams and Uda teach or suggest all of the limitations of independent claim 1. Pet. 9–38. For example, Petitioner contends McAdams discloses "a first terminal for receiving a first voltage" (terminal Vcc, where Vcc is a supply voltage that is applied when power is applied to the circuit depicted in Figure 1 of McAdams), "a second terminal for receiving a voltage" (terminal for receiving Vss as shown in Figure 1 of McAdams), and "a terminal T1 for providing a signal indicating a state of the programmable latch" (node 14 in Figure 1 of McAdams that indicates the state of the fuse, which corresponds to the state of the programmable latch). *Id.* at 13–20. Petitioner concedes that "McAdams does not explicitly disclose 'a diode' for keeping the voltage on the terminal T1 within a predetermined range of values as recited in" claim 1, and contends that "Uda discloses such a feature." *Id.* at 25 (citing Ex. 1002 ¶ 89).

In particular, Petitioner contends that Uda teaches a fuse arrangement that works to replace a defective cell with the corresponding backup cell, and that, in such an arrangement, the fuse is melted by a laser or electrical means. *Id.* at 26. Petitioner contends that Uda teaches that diodes and a resistor are used to prevent gate destruction that would occur if an excess charge from laser cutting reaches the NMOS gate. *Id.* Petitioner further contends that because "Uda, like McAdams, is in the field of semiconductor integrated devices, including redundancy circuits for memory devices that use fuses to enable such redundancy circuits," "a POSITA implementing the circuit of McAdams would have had reason to look to Uda" (*id.* at 25 (citing Ex. 1002 ¶ 90)), and, "in view of Uda's teachings, a POSITA would have found it obvious to include a diode like that disclosed in Uda in McAdams' figure 1 circuit" (*id.* at 26–27 (citing Ex. 1002 ¶¶ 91–93)).

According to Petitioner, "implementing a diode in McAdams' circuit would have solved a potential problem that could arise in McAdams' circuit" because "McAdams, like Uda, discloses that a laser can be used to program the fuse 10 shown in figure 1 of McAdams." Pet. 27–28 (citing Ex. 1002 ¶ 92). Petitioner argues that a "POSITA would have recognized that when a laser is used to blow a fuse (i.e., program the fuse), charge from the laser can accumulate at various points in the circuit," and, "just like in Uda, one place in the McAdams' circuit where excess charge can accumulate is node 14, which is connected to the gates of transistors 12 and 13." *Id.* at 28 (citing Ex. 1002 ¶¶ 93–94). Petitioner argues that if the excess charge is not removed, "the gates of transistors 12 and 13 could be damaged," and "[i]ncluding a diode, like in Uda, would have been a

straightforward way of solving this problem, which a POSITA would have recognized based on Uda's teachings." *Id.* at 29 (citing Ex. 1002 ¶¶ 96–98).

Petitioner contends that "a POSITA would have been motivated to modify the circuit of figure 1 in McAdams to implement a diode like that disclosed in Uda in order to provide protection for the transistors 12 and 13, the gates of which are connected to node 14." Pet. 29–30 (citing Ex. 1002 ¶¶ 95–103). Petitioner contends that,

> in view of Uda, a POSITA and would have been motivated to implement, *inter alia*, a diode connected between the node 14 and the power supply voltage V_{CC} such that when the fuse 10 is programmed using a laser, any excess charge on node 14 stemming from the laser cutting of the fuse would be led to power supply node V_{CC} thereby limiting the maximum voltage experienced by the gates of transistors 12 and 13.

Id. at 30 (citing Ex. 1002 ¶¶ 95–103). Petitioner also contends that "[a] POSITA would have understood that when V_{CC} is at 0V (i.e., 'before power is supplied to the latch'), the diode in the combined McAdams-Uda circuit would not allow the voltage at node 14 to exceed 0 volts by more than a threshold voltage of the diode." *Id.* at 34 (citing Ex. 1002 ¶ 107). Petitioner further contends that modifying McAdams' circuit with Uda's diode would have been within the capability of a POSITA (*id.* at 31–32); a POSITA would have recognized that adding the diode in the McAdams' circuit would have made the circuit more robust and would not have negatively impacted the McAdams' circuit (*id.* at 33–34); and modifying "McAdams based on Uda would have been a predictable combination of known components according to known methods" and "would have been consistent with the expected result that it would be less likely that transistors 12 and 13 would be damaged when the laser is used to blow fuse 10" (*id.* at 34).

Based on the current record, we are persuaded that Petitioner's discussion of the particular structures in McAdams and Uda, and the explanations in the Petition and Baker Declaration, are sufficient to establish a reasonable likelihood that the subject matter of independent claim 1 would have been obvious over the combined teachings of McAdams and Uda. We also considered the arguments and evidence with respect to claims 2–5, 8–10, and 13 that directly depend from claim 1, and are likewise persuaded, on the current record, that Petitioner has demonstrated a reasonable likelihood that it would prevail as to those claims as well. *See* Pet. 38–60.

D. Remaining Grounds

Petitioner contends that the subject matter of (1) claims 5–7 would have been obvious over the combined teachings of McAdams, Uda, and Keeth (Pet. 61–71); (2) claims 11 and 12 would have been obvious over the combined teachings of McAdams, Uda, and Weste (*id.* at 71–79); and (3) claim 9 would have been obvious over the combined teachings of McAdams, Uda, and Tomishima (*id.* at 79–85). Having found that Petitioner has established a reasonable likelihood of prevailing with respect to its contentions that claims 1–5, 8–10, and 13 of the '492 patent would have been obvious over the combined teachings of McAdams and Uda, we institute review with respect to challenged claims 6, 7, 9, 11, and 12 as well. *See* United States Patent and Trademark Office, *Guidance on the Impact of SAS on AIA Trial Proceedings*, Patent Trial and Appeal Board (April 26, 2018) ("As required by [*SAS Institute Inc. v. Iancu*, 138 S.Ct. 1348 (2018)], the PTAB will institute as to all claims or none.").

III. CONCLUSION

Based on the arguments in the Petition and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail on its challenge to at least one claim of the '492 patent.

Although we exercise our discretion and institute review, we remind the parties that we have not yet made a final determination as to the patentability of any of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–13 of the '492 patent with respect to the grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this Decision.

PETITIONER:

Naveen Modi
Joseph E. Palys
Paul M. Anderson
Chetan R. Bansal
PAUL HASTINGS LLP
naveenmodi@paulhastings.com
josephpalys@paulhastings.com
paulanderson@paulhastings.com
chetanbansal@paulhastings.com

PATENT OWNER:

Craig R. Kauffman
Kevin C. Jones
TECHKNOWLEDGE LAW GROUP LLP
ckaufman@tklg-llp.com
kjones@tklg-llp.com