

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO. LTD.,  
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,  
Patent Owner.

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Case IPR2019-00780  
Patent 6,163,492

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**PATENT OWNER PROMOS TECHNOLOGIES, INC.'S RESPONSE TO  
PETITION FOR *INTER PARTES* REVIEW OF  
UNITED STATES PATENT NO. 6,163,492**

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Patent Trial and Appeal Board  
United States Patent and Trademark Office  
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## **I. INTRODUCTION.**

Patent Owner ProMOS Technologies, Inc. hereby responds to Samsung's Petition for *Inter Partes* Review seeking cancellation of claims 1-13 of U.S. Patent No. 6,163,492 (Ex. 1001). Samsung presented four grounds challenging validity in its petition:

1) that McAdams (Ex. 1006) and Uda (Ex. 1007) render obvious claims 1-5, 8-10, and 13;

2) that McAdams, Uda, and Keeth (Ex. 1008) render obvious claims 5-7;

3) that McAdams, Uda, and Weste (Ex. 1009) render obvious claims 11-12; and

4) that McAdams, Uda, and Tomishima (Ex. 1013) render obvious claim 9. Pet. at 3.

The Board instituted on all four grounds. Paper 6 at 14-15.

All four instituted grounds depend on a combination of McAdams and Uda.

First, McAdams does not teach the element “a terminal T1 for providing a signal indicating a state of the programmable latch” when that term is properly construed. That phrase means: “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch,” and McAdams does not discuss when the circuit is used with regard to when it is programmed. The ancillary references are used only for other

claim elements and therefore do not cure McAdams's deficiency in failing to teach this claim element.

Further, the McAdams and Uda references are directed to alternative technologies that are incompatible, and a person of skill in the art would not combine their teachings in the manner proposed by Samsung. McAdams is based on CMOS technology, a fundamentally different process technology than the ECL process described by Uda. Samsung concedes that McAdams does not include the claimed diode, yet the Uda diode that Samsung wishes to plug into McAdams's circuit has a structure that is incompatible with the CMOS technology used by McAdams. The Uda diode is formed at the junction of a resistive epitaxial p region and a buried n region. The resistive epitaxial p region does not exist in the McAdams CMOS technology, and further the Uda diode cannot be constructed using a CMOS process and cannot be separated from the resistive epitaxial region. Samsung's combination is based on impermissible hindsight that ignores the technical incompatibility between the references.

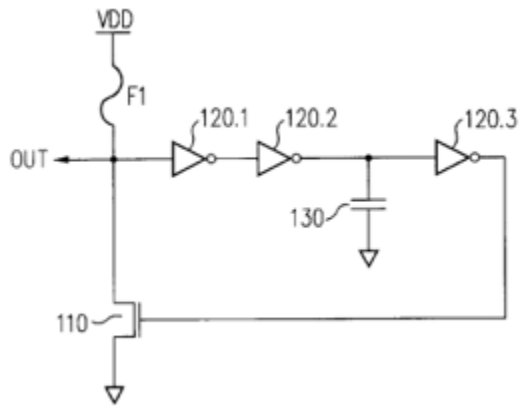
**I. RELIEF REQUESTED.**

ProMOS submits that the Board should conclude that claims 1-13 are patentable, and that Samsung has not met its burden to establish unpatentability for the four instituted grounds.

**II. OVERVIEW OF THE '492 PATENT.**

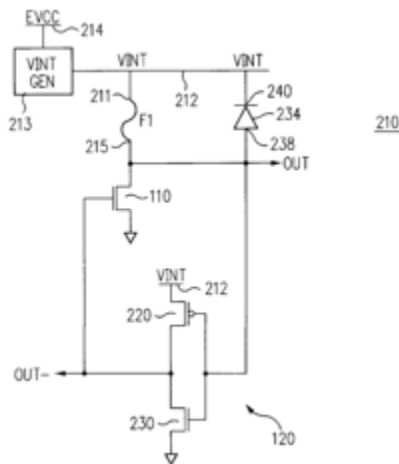
The '492 patent, titled "Programmable latches that include non-volatile programmable elements" was filed as application number 09/178,445 on October 23, 1998 and has an earliest priority date of October 23, 1998. The invention relates generally to improving the reliability of programmable latches during power-up. Ex. 1001 at col. 1:60-67, 2:1-4, 2:51-55, 5:51-65.

Programmable latches including non-volatile programmable elements, for example fuses, are used in integrated circuits to enable modification of the circuit during run-time, without changing the mask and re-fabricating the chip. Ex. 1001 at col. 1:15-23. Prior art figure 1 demonstrates one form of a traditional latch, with the OUT terminal indicating the fuse state which is provided to other circuitry. *Id.* at col. 1:32-35.



Ex. 1001 at Fig. 1.

One aspect of the invention, shown for example in figure 2A below, is that the fuse connects the power source VINT to the output node OUT, whose value is read to indicate the state of the latch.



Ex. 1001 at Fig. 2A.

The fuse is claimed as a “non-volatile programmable element,” and each of claims 1 and 14 require that, when conductive, it connects the claimed “first terminal” (power) to the claimed “terminal T1” (terminal indicating the state of the



latch). Ex. 1001 at claims 1, 14. Because of this structure, the fuse directly indicates the state of the latch and is the only device which affects the output. Ex. 1001 at col. 2:22-27, 3:66-4:3.

The '492 invention solved the problem that occurs when the terminal OUT may indicate the wrong state before power is applied to the latch at VDD. Ex. 1001 at col. 1:46-48. This problem may be caused by two situations, described in the background of the '492 patent:

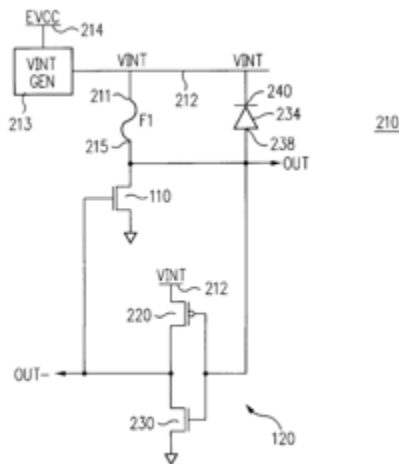
when the power is off, transistor 110 is non-conductive. Therefore, terminal OUT is floating . . . the terminal 'may tend to have its potential raised to a logic level '1'.' In addition, the terminal OUT potential may become 'unstable due to the capacitive coupling' in the integrated circuit. Consequently, during operation, transistor 110 could be off even if the fuse F1 were blown.

*Id.* at col. 1:38-47.

The '492 patent solves these problems by preventing the output node (terminal OUT) from floating above ground when power is off and from destabilizing through capacitive coupling during power up. Ex. 1001 at col. 1:36-47. In this latter scenario, the terminal may momentarily float even when power is initially applied as there is no device that is strongly driving the output node. *Id.*

One way that the '492 patent solved these problems is by including a "diode that keeps a voltage on a latch output terminal within a predetermined range of

values before power is supplied to the latch.” Ex. 1001 at col. 2:1-4, claim 1. One such embodiment is shown in Fig. 2A:



Ex. 1001 at Fig. 2A.

By connecting a diode 234 to the OUT node (claim 1), the '492 patent eliminates the possibility that increasing voltage or capacitive coupling at the OUT terminal causes that node to rise to a level that will turn on inverter 120 and cause a false state at the OUT terminal.

Another way of addressing these problems is to require that power be turned off after programming to allow any voltage that accumulated on the output node to dissipate. Ex. 1001 at col. 5:51-6:8. In this way, the risk of a false state caused by capacitive coupling or otherwise is eliminated.

Claim 1 is an example of an embodiment that utilizes a diode and also ensures that power is off after programming to discharge excess voltage buildup on

the terminal OUT, using the term “a terminal T1 for providing a signal indicating a state of the programmable latch.”

1. A programmable latch comprising:
  - a first terminal for receiving a first voltage;
  - a second terminal for receiving a second voltage;
  - a terminal T1 for providing a signal indicating a state of the programmable latch;
  - a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;
  - a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and
  - a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Ex. 1001 at Claim 1.

### III. PROMOS'S PROPOSED CLAIM CONSTRUCTION.

Samsung did not propose any constructions for the claims at issue. Pet. at 8-9.

ProMOS proposes a construction for the term “a terminal T1 for providing a signal indicating a state of the programmable latch.” In this proceeding, claim construction uses the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); see 83 Fed. Reg. 51340-58 (Oct. 11, 2018).

**A. “a terminal T1 for providing a signal indicating a state of the programmable latch” means “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”**

Claim 1 includes the following limitation: “a terminal T1 for providing a signal indicating a state of the programmable latch.” This limitation should be construed as follows: “a terminal T1 from which voltage is dissipated after programming in order to provide a signal indicating a state of the programmable latch.”

In its institution decision in IPR2019-00779, the Board did not adopt ProMOS's construction, and provided two reasons that ProMOS's construction was not appropriate on the existing record. Paper 7 at 8-10. First, the Board suggested that ProMOS's construction is incorrect because the term appears in both claims 1 (with a diode) and 14 (without a diode). *Id.* The Board assumed that ProMOS was arguing for different constructions for the relevant term in the two

different claims. IPR2019-00779, Paper 7 at 9. Not so. Claim 1 addresses the stated “false state” problem with two solutions – a diode and “a terminal T1 from which voltage is dissipated after programming . . .” Ex. 1001 at 2:13-21, 2:38-50. In contrast, claim 14 recites a single solution to the problem – embodied in the limitation at issue. That is precisely what the specification states at Ex. 1001 at col. 5:51-6:8, quoted below, and there is no inconsistency.

Second, the Board concluded that ProMOS was seeking to read a specific embodiment into the claim, because the ’492 patent discloses a number of embodiments. IPR2019-00779, Paper 7 at 9-10. But as discussed below, terminal T1 must be at ground voltage before power is applied to the circuit because otherwise the element “a terminal T1 for providing a signal indicating a state of the programmable latch” would not be met – the terminal T1 in that case would indicate the wrong state, which is the very problem that the ’492 patent is trying to solve.

As explained in ProMOS’s preliminary response in IPR2019-00779, and as set forth below, ProMOS’s proposed construction is supported by the intrinsic record. In particular, the concept that power to the latch is off between programming and use, is necessary because otherwise the terminal will not “indicate[ ] a state of the programmable latch.” That is, a terminal that does not operate in this way will suffer from the risk of false output that was discussed in

the background of the patent. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2003 at ¶29; *see e.g., MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1315 (Fed. Cir. 2017) (interpreting an apparatus claim with “presents,” “receives,” and “generates” terms as requiring “capability of the structure” or the “particular capabilities” of the structure) (citing *UltimatePointer, LLC v. Nintendo Co.*, 73 F. Supp. 3d 1305, 1308 (W.D. Wash. 2014)).

The background of the '492 patent explains that the entire purpose of the invention is to eliminate the risk of a false output because of excess voltage at T1 accumulated from programming or from capacitive coupling at the output. Ex. 1001 at col. 1:46-48, 1:38-47; Ex. 2003 at ¶29. If this voltage is not dissipated after programming, then the terminal T1 will not necessarily indicate the state of the latch because it may indicate a false state due to this programming voltage. Ex. 2003 at ¶29. Therefore, in order for the terminal T1 to “indicate[ ] a state of the programmable latch” as claimed, power must be turned off to allow voltage to dissipate from the output node after programming.

The specification goes on to explain that in the embodiments without a diode power must be turned off after programming:

“In some embodiments, diode 234 is omitted. Nevertheless, if fuse F1 is non-conductive, the terminal OUT is at ground before power-up. This is true even if the fuse was programmed electrically and some charge accumulated on terminal OUT during programming. Indeed, after the

fuse is programmed (that is, made non-conductive), the power is kept off for a while before the latch is used. For example, if the latch is part of a semiconductor memory, the memory fuses are typically programmed when the memory is tested. Then the power is turned off, and the memory is taken out of the testing equipment and shipped to a customer. By the time the customer supplies power to the memory, any charge which may have accumulated on terminal OUT when the fuse was being programmed has been dissipated. Therefore, the terminal OUT is at ground.

As soon as the terminal OUT- is charged by transistor 220 to a threshold voltage of transistor 110, transistor 110 turns on and keeps the node OUT at the ground voltage. Thus, even if the voltage on terminal OUT increased slightly at the beginning of the power-up operation (that is, when the supply voltage EVCC started rising from 0 volts towards its final value), the terminal OUT is quickly returned to ground. If the power is turned off and then turned on again, the terminal OUT is at zero volts before the power is turned on. Therefore, reliable operation is provided.”

Ex. 1001 at col. 5:51-6:8 (emphasis added).

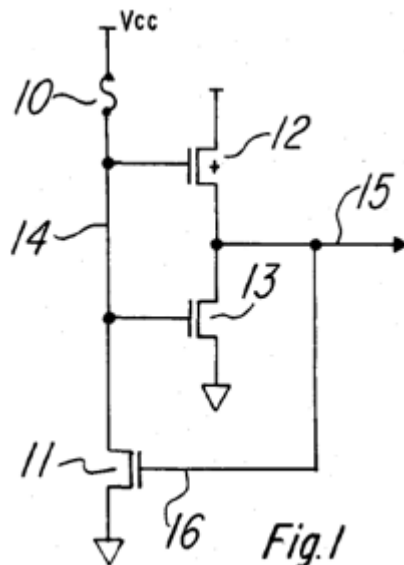
Thus, this term should be given ProMOS’s proposed construction.

#### **IV. THE PRIOR ART.**

##### **A. McAdams**

McAdams teaches a fuse circuit for selecting a new memory cell where one is defective. According to McAdams, less power is consumed using its Figure 1

circuit because of feedback transistor 11, which is connected to the output of inverter 12/13.



Ex. 1006 at Fig. 1.

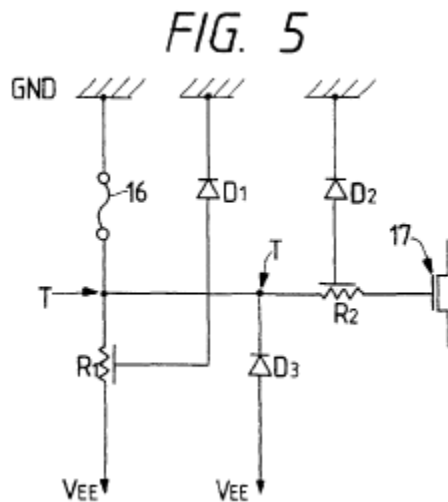
As Samsung's expert Dr. Baker confirmed in his deposition, McAdams is a CMOS circuit manufactured and designed according to CMOS techniques. Ex. 2003 at ¶33; Ex. 2004 at 54:18-20. This is evident in, for example, the use of nmos and pmos transistors in figure 1, and the title of McAdams: "Low power CMOS fuse circuit." Ex. 2003 at ¶33.

The McAdams circuit above does not discuss operation of the latch at all. More specifically, McAdams does not specify when the latch is operated with respect to programming and whether power is turned off in order to allow voltage to dissipate after programming. Ex. 2003 at ¶35.



**B. Uda**

Uda teaches fuse arrangements for redundancy circuits in semiconductor devices. One such arrangement is Figure 5. Ex. 1007 at col. 9:28-10:18.



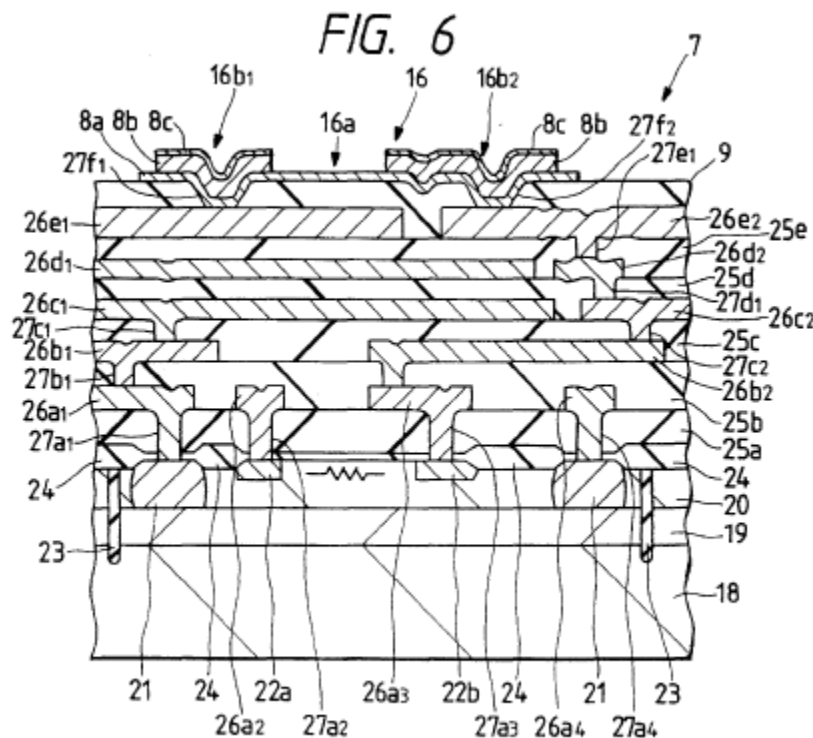
Ex. 1007 at Fig. 5.

Samsung relies on Uda because it purports to teach the use of diodes, a claim element that Samsung concedes is missing from the McAdams reference.

Samsung identifies the relevant diodes (D1-D3 in Ex. 1007 at Fig. 5) as those that are used to protect node T from high voltages when, for example, laser fuse cutting threatens to damage the gate of transistor 17. Pet. at 26-38; Ex. 1007 at col. 9:44-53. These diodes are each connected to a resistor (for example R1 and R2) through an epitaxial region, indicated in Figure 5 above.

This fuse arrangement has the structure shown in Figure 6 – emitter-coupled logic implemented using various layers and regions on top of the semiconductor

substrate 18. Ex. 1007 at col. 10:19-12:4; Ex. 2003 at ¶37. In Figure 6, a diode exists at the interface of region 19 and resistive epitaxial region 20, and the diode necessarily connects to the rest of the circuit through the resistive epitaxial region 20. Ex. 2003 at ¶37. Each of the three diodes in Figure 5, D1-D3, would be formed the same way, each inseparable from the resistor to which it connects. *Id.*



Ex. 1007 at Fig. 6.

### C. Keeth

Keeth teaches a power supply design for providing regulated power in an integrated circuit. Ex. 1008. Samsung cites Keeth for its teachings about providing VCC from a regulated power supply. Pet. 64-69.

**D. Weste**

Weste is a textbook containing, among many other things, generic discussions about various electronic components. Ex. 1009. For example, Weste contains a discussion about how transistors are formed and how they operate, including a discussion that the intrinsic nature of transistors means that each has two pn junctions, also called “body diodes.” Pet. at 72-77.

**E. Tomishima**

Tomishima teaches specific arrangements of power supply pads in semiconductor chips for high speed and stable operation. Ex. 1013. Samsung cites Tomishima for its teachings that an external power supply may be routed through pads on the chip and used. Pet. at 80-85.

**V. INVALIDITY ANALYSIS.**

**A. McAdams and Uda do not Render Obvious Claims 1-5, 8-10, and 13.**

**1. McAdams and Uda do not Teach “a terminal T1 for providing a signal indicating a state of the programmable latch,” when properly construed**

The term “a terminal T1 for providing a signal indicating a state of the programmable latch” requires that power be off after programming in order for voltage to dissipate. But McAdams – the only reference relied on for this element – is silent about this feature of claim 1.

McAdams does not state that voltage that accumulates on nodes 14 and 15 is dissipated after programming. Ex. 2003 at ¶35; Ex. 1006 generally. The capacitive coupling downstream from this circuit in McAdams allows the floating node 15 to stray far from its initialization state, and absent any teaching that the latch is programmed and left unpowered before being read, the McAdams circuit suffers from this capacitive coupling. *Id.* McAdams is silent about whether power is turned off after programming in order to allow power to dissipate, and therefore does not meet the proper construction of the term “a terminal T1 for providing a signal indicating a state of the programmable latch.”

Uda is not relied on for this element (Pet. at 18-20), and further does not teach it. Ex. 1007 generally. Therefore, Uda does not make up for McAdams’s shortcoming.

**2. A person of skill in the art would not combine McAdams and Uda because they are contradictory and incompatible technologies.**

Samsung admits that McAdams does not disclose the claimed diode. Pet. at 25 (“McAdams does not explicitly disclose ‘a diode’ for keeping the voltage on the terminal T1 within a predetermined range of values as recited in claim element 1[g].”). To cure this deficiency, Samsung has identified a diode in Uda’s schematic (figure 5), and based on that symbol alone has asserted that a person of ordinary skill in the art would just move the symbol into McAdams. However, a

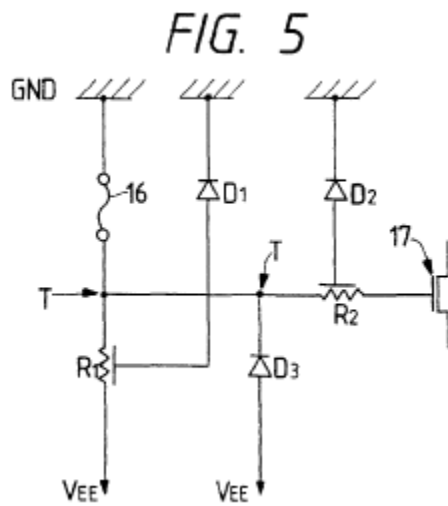
close examination of the diode structure (something that Samsung's expert did not do) demonstrates that Uda's structure is incompatible with McAdams, and thus a POSITA would not combine the references as proposed by Samsung.

“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). It is impermissible hindsight to consider only whether a person of skill in the art *could* combine references, as opposed to focusing on the reasons or motivations why a person of skill in the art *would* combine references. *InTouch Techs., Inc. v. VGO Commcn's, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014). It is also inappropriate to just do a “hindsight-guided combination of elements” to match the claim at issue, without considering whether there is some motivation or reason to combine the references in the way suggested. *Leo Pharma. Prods. Ltd. v. Rea*, 726 F.3d 1346, 1354-59 (Fed. Cir. 2013) (reversing PTAB finding of obviousness because the analysis was a “hindsight-guided combination of elements”); *see also Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354-55 (Fed. Cir. 2013). Because of the technical incompatibility of the references, the needed motivation to combine is absent here.

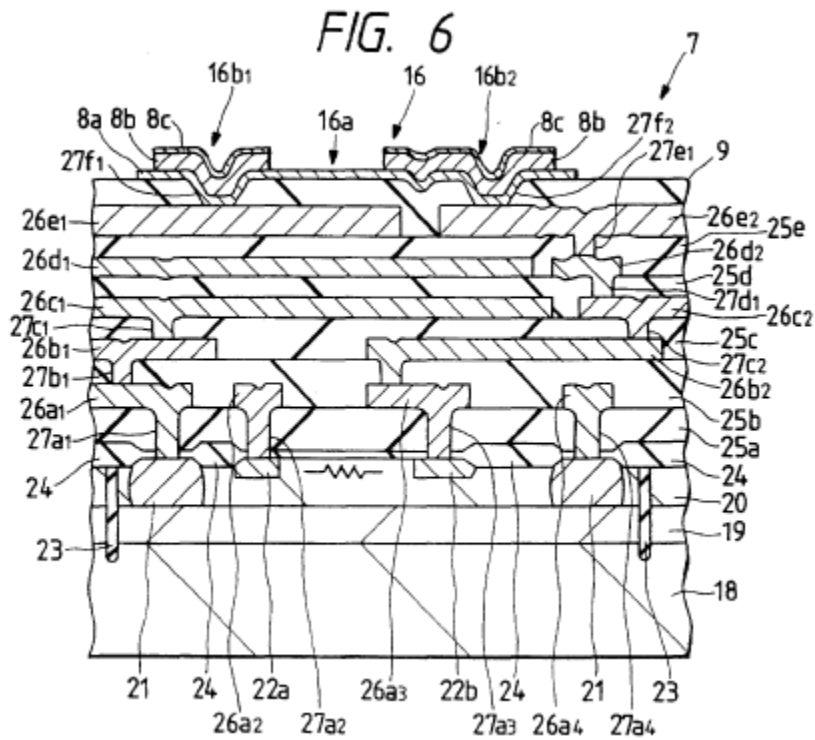
The Uda diode and McAdams circuit are so different that a person would not be motivated to combine them. ECL logic (like the Uda diode) differs from

CMOS in many ways, and importantly for purposes of this analysis, the CMOS technology used in McAdams does not include a resistive epitaxial region, which is the region that forms one side of the diode described in Uda. Ex. 2003 at ¶37. As set forth in more detail below, A person of skill in the art would not move the Uda diode to McAdams because they are not technically compatible, and Samsung's argument is mere hindsight guided by the '492 claim, without explaining why or how a POSITA would resolve the technical differences between the reference structures. *Belden*, 805 F.3d at 1073; *InTouch*, 751 F.3d at 1352; *Leo Pharma.*, 726 F.3d at 1354-59; *Plantronics*, 724 F.3d at 1354-55.

Uda's diode is constructed with a combination of a buried and epitaxial region (Uda figure 6), including a weak diode (the interface of layers 19 and 20) connected to the rest of the circuit through a resistive epitaxial region (region 19). Ex. 2003 at ¶37. Schematically this is shown in Uda figure 5 as a diode-resistor combination, and in figure 6 at the junction between a resistive epitaxial region 20 and the buried n region below it 19. Ex. 1007 at Figs. 5, 6.



Ex. 1007 at Fig. 5.



Ex. 1007 at Fig. 6.

Further, the diode in Uda is necessarily paired with a series resistor because of the way it is formed, and as a result a person of skill in the art would not think to just use the diode in another McAdams circuit. Ex. 2003 at ¶37. Again, the Uda diode is formed at the junction between that resistive epitaxial p region 20 and the buried n region 19, and epitaxial p region 20 necessarily forms a resistor in series with the diode. Ex. 2003 at ¶37. Not only does McAdams not have a resistive p region, but a person of skill in the art would not think to separate the Uda diode from its paired resistor. Ex. 2003 at ¶37; *Belden*, 805 F.3d at 1073; *InTouch*, 751 F.3d at 1352; *Leo Pharma.*, 726 F.3d at 1354-59; *Plantronics*, 724 F.3d at 1354-55. Put another way, Uda does not have a diode alone, it has a diode-resistor pair, and there is no way to form just the diode. Samsung's suggestion that a POSITA would simply use the Uda diode alone in the McAdams circuit is incorrect.

Finally, Samsung's expert did not account for these differences in CMOS and ECL technologies or explain why or how a POSITA could address the incompatibility of the structures. Dr. Baker did not even review figure 6 in detail or correlate the actual structure of the diode in figure 6 with the symbol that he plucked from figure 5. Ex. 2004 at 41:2-42:10, 43:15-44:24. This failure confirms that Samsung's combination is based on hindsight, and nothing more. Samsung's failure to adequately provide a motivation to combine the references is fatal to all of the invalidity theories presented in its petition.



**B. McAdams, Uda, and Keeth do not Render Obvious Claims 5-7.**

For at least the two reasons stated above, the McAdams and Uda references fail to teach all elements of claim 1, the independent claim underlying dependent claims 5-7. Keeth does not cure these deficiencies, nor does Samsung's petition so contend. Therefore, the combination of references cited by Samsung fail to render obvious claims 5-7.

**C. McAdams, Uda, and Weste do not Render Obvious Claims 11-12.**

For at least the two reasons stated above, the McAdams and Uda references fail to teach all elements of claim 1, the independent claim underlying dependent claims 11-12. Weste does not cure these deficiencies, nor does Samsung's petition so contend. Therefore, the combination of references cited by Samsung fail to render obvious claims 11-12.

**D. McAdams, Uda, and Tomishima do not Render Obvious Claim 9.**

For at least the two reasons stated above, the McAdams and Uda references fail to teach all elements of claim 1, the independent claim underlying dependent claim 9. Tomishima does not cure these deficiencies, nor does Samsung's petition so contend. Therefore, the combination of references cited by Samsung fail to render obvious claim 9.

**VI. CONCLUSION.**

For the reasons set forth above, the Board should issue a final written decision that challenged claims 1-13 are patentable over McAdams, Uda, Keeth, Weste, and Tomishima.

Dated: December 5, 2019

Respectfully submitted,

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**APPENDIX OF EXHIBITS**

<b>Exhibit No.</b>	<b>Description</b>
2001	Reserved
2002	Exhibit marked at the Deposition of Dr. Baker, October 25, 2019
2003	Declaration of Erik de la Iglesia in Support of Patent Owner ProMOS Technologies, Inc.'s Response to Petition
2004	Deposition Transcript of R. Jacob Baker, Ph.D., P.E., October 25, 2019

**CERTIFICATE OF SERVICE**

I hereby certify that on December 5, 2019, a true and correct copy of the foregoing *Patent Owner ProMOS Technologies, Inc. 's Response to Petition for Inter Partes Review of United States Patent No. 6,163,492* and all supporting exhibits were served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

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**CERTIFICATE OF COMPLIANCE WITH  
TYPE-VOLUME LIMITATION REQUIREMENTS**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned attorney of record, hereby  
certifies that:

This brief complies with the type-volume limitation of 37 C.F.R. § 42.24(b).  
The brief contains 3,935 words, excluding the parts of the brief exempted by 37  
C.F.R. § 42.24.

Date: December 5, 2019

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