

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

INSTITUTE OF MICROELECTRONICS, CHINESE ACADEMY OF
SCIENCES,
Patent Owner.

PTAB Case No. IPR2019-00834

Patent No. 9,070,719 B2

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,070,719 B2**

Claims 1-3, 6-7

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STATUTES

35 U.S.C. § 102	19, 21, 22, 23
35 U.S.C. § 314(a)	26, 29
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OTHER AUTHORITIES

37 C.F.R. § 42.1(b)	27
37 C.F.R. § 42.100	13

EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS

Petitioner's Exhibits	
Exhibit	Description
Ex. 1001	U.S. Patent No. 9,070,719 (the “'719 patent”)
Ex. 1002	RESERVED
Ex. 1003	U.S. Patent No. 9,362,290 (“Liaw”)
Ex. 1004	U.S. Patent No. 7,335,583 (“Chang”)
Ex. 1005	U.S. Patent Application Pub. No. 2009/0309141 (“Okuno”)
Ex. 1006	U.S. Patent Application Pub. No. 2008/0251934 (“Mandelman”)
Ex. 1007	File history for U.S. Patent No. 9,070,719
Ex. 1008	U.S. Patent Application Pub. No. 2006/0024940 (“Furukawa”)
Ex. 1009	H. Iwai, <i>Roadmap for 22 nm and beyond</i> , 86 Microelectronic Engineering, 1520-1528 (2009) (“Iwai”)
Ex. 1010	U.S. Patent Application Pub. No. 2006/0175669 (“Kim”)
Ex. 1011	U.S. Patent No. 8,278,175 (“Cheng ’175”)
Ex. 1012	U.S. Patent No. 9,293,377 (the “'377 patent”)
Ex. 1013	U.S. Patent Application Pub. No. 2007/0152266 (“Doyle”)
Ex. 1014	Chinese Patent No. 102956457B
Ex. 1015	U.S. Patent No. 7,531,437 (“Brask”)
Ex. 1016	Mike Smayling, <i>Gridded Design Rules-1 D Approach Enables Scaling of CMOS Logic</i> , 6 Nanochip Technology Journal, 33-37 (2008) (“Nanochip Technology Journal”)

**EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS
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Ex. 1017	Intel Technology Journal Vol. 12, Issue 2, 77-86, 121-130 (June 17, 2008) (“Intel Technology Journal”)
Ex. 1018	Linda Geppert, <i>The Amazing Vanishing Transistor Act</i> , IEEE Spectrum, 28-33 (Oct. 2002) (“Geppert”)
Ex. 1019	Jack Kavalieros et al., <i>Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering</i> , 2006 IEEE Symposium on VLSI Technology Digest of Technical Papers (2006) (“Kavalieros”)
Ex. 1020	U.S. Patent No. 7,524,727 (“Dewey”)
Ex. 1021	K. Mistry et al., <i>A 45nm Logic Technology with High-k + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 International Electron Devices Meeting Tech. Dig. 247-250 (2007) (“Mistry”)
Ex. 1022	A. Chatterjee et al., <i>Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process</i> , 1997 International Electron Devices Meeting Tech. Dig. 821-824 (Dec. 7-10, 1997) (“Chatterjee”)
Ex. 1023	U.S. Patent Application Pub. No. 2007/0138559 (“Bohr”)
Ex. 1024	U.S. Patent No. 5,960,270 (“Misra”)
Ex. 1025	U.S. Patent No. 6,664,195 (“Jang”)
Ex. 1026	U.S. Patent Application Pub. No. 2011/0068411 (“Sun”)
Ex. 1027	Scott E. Thompson, et. al., <i>A 90-nm Logic Technology Featuring Strained-Silicon</i> , 51 IEEE Tran. Electron Devices, 1790-1797 (Nov. 2004) (“Thompson”)

**EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS
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Ex. 1028	U.S. Patent No. 6,413,802 (“Hu”)
Ex. 1029	U.S. Patent Application Pub. No. 2011/0147831 (“Steigerwald”)
Ex. 1030	S. Natarajan, et al., <i>A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors Enhanced Channel Strain and 0.171μm² SRAM Cell Size in a 291Mb Array</i> , IEEE Electron Devices Meeting (2008) (“Natarajan”)
Ex. 1031	U.S. Patent No. 7,838,373 (“Giles”)
Ex. 1032	U.S. Patent Application Pub. No. 2007/0284671 (“Tsutsumi”)
Ex. 1033	Mark Bohr and Kaizad Mistry, <i>Intel’s Revolutionary 22nm Transistor Technology</i> , available at http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf (accessed through https://newsroom.intel.com/press-kits/intel-22nm-3-d-tri-gate-transistor-technology/), last visited August 27, 2018 (“Intel 22nm May 2011”)
Ex. 1034	Brian Doyle et al., <i>Tri-gate fully-depleted CMOS transistors: Fabrication, design and layout</i> , 2003 Symposium on VLSI Technology, Digest of Technical Papers 133-134 (2003) (“Doyle 2003”)
Ex. 1035	Z. Guo et al., <i>FinFET-based SRAM design</i> , Proceedings of the 2005 International Symposium on Low Power Electronics and Design 2-7 (2005) (“Guo”)
Ex. 1036	S. C. Song et al., <i>Systematic approach of FinFET based SRAM bitcell design for 32nm node and below</i> , IEEE International Conference on IC Design and Technology ICICDT'09, 165-168 (2009) (“Song”)

**EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS
(continued)**

Ex. 1037	Kelin J. Kuhn et al. <i>Process technology variation</i> , IEEE Transactions on Electron Devices 58.8 (2011) 2197-2208 (“Kuhn”)
Ex. 1038	RESERVED
Ex. 1039	RESERVED
Ex. 1040	WO International Patent Pub. No. 2008/114341 (“Okuno PCT (Japanese)”)
Ex. 1041	Certified English translation of WO International Patent Pub. No. 2008/114341 (“Okuno PCT”)
Ex. 1042	<i>Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha</i> , IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017)
Ex. 1043	<i>Agilent Techs., Inc. v. Thermo Fisher Sci. Inc.</i> , IPR2018-00313, Paper 23 (PTAB June 18, 2018)
Ex. 1044	<i>Intel Corp. v. Alacritech, Inc.</i> , IPR2018-00226, Paper 7 (PTAB June 5, 2018)
Ex. 1045	Declaration of Dr. Scott Thompson (“Thompson Decl.”)
Ex. 1046	Stanley Wolf, <i>Silicon Processing for the VLSI Era – Vol 4: Deep-Submicron Process Tech.</i> 1-16, 181-226 (Lattice Press 2002) (“Wolf 2002”)
Ex. 1047	Stanley Wolf, <i>Silicon Processing for the VLSI Era – Vol 2: Process Integration</i> 298-367 (Lattice Press 1990) (“Wolf 1990”)
Ex. 1048	Michael Quirk & Julian Serda, <i>Semiconductor Manufacturing Technology</i> 21-42, 199-224, 257-298, 475-514, 634 (Prentice Hall 2001) (“Quirk”)

**EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS
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Ex. 1049	Alan G. Lewis & John Y. Chen, <i>VLSI ELECTRONICS MICROSTRUCTURE SCIENCE - Vol 18: Advanced MOS Device Physics</i> 37-117 (Academic Press 1989) (“Lewis”)
Ex. 1050	U.S. Patent No. 4,234,362 (“Riseman”)
Ex. 1051	Sang H. Dhong & Edward J. Petrillo, <i>Sidewall Spacer Technology for MOS and Bipolar Devices</i> , 133 J. Electrochem. Soc., 389-396 (Feb. 1986) (“Dhong”)
Ex. 1052	Paul J. Tsang et al., <i>Fabrication of High-Performance LDDFET's with Oxide Sidewall-Spacer Technology</i> , 17 IEEE Journal of Solid-State Circuits, 220-226 (April 1982) (“Tsang”)
Ex. 1053	Cheng-Tung Huang et al., <i>New Negative-Bias-Temperature-Instability Improvement Using Buffer Layer under Highly Compressive Contact Etch Stop Layer for 45-nm-Node Complementary Metal-Oxide-Semiconductor and Beyond</i> , 46 Jpn. J. Appl. Phys., 2015-2018 (2007) (“Huang 2007”)
Ex. 1054	K. Sukegawa et al., <i>Dependable Integration of Full-Porous Low-k Interconnect and Low-leakage/ Low-cost Transistor for 45nm LSTP Platform</i> , 2007 IEEE Symposium on VLSI Technology, 174-175 (2007) (“Sukegawa”)
Ex. 1055	Badih El-Kareh, <i>Silicon Devices and Process Integration, Deep Submicron and Nano-Scale Technologies</i> 439-446 (Springer 2009) (“El-Kareh”)
Ex. 1056	Jakub Kedzierski et al., <i>High-performance symmetric-gate and CMOS-compatible V_{sub} t/ asymmetric-gate FinFET devices</i> , International Electron Devices Meeting, 437-440 (2001) (“Kedzierski”)

EXHIBIT LIST AND TABLE OF ABBREVIATIONS AND CONVENTIONS (continued)

Ex. 1057	Mayank Shrivastava et al., <i>Toward System on Chip (SoC) Development Using FinFET Technology: Challenges, Solutions, Process Co-Development & Optimization Guidelines</i> , IEEE Transactions on Electron Devices, 1597-1607 (June 2011) (“Shrivastava”)
Ex. 1058	Jean-Pierre Colinge, <i>FinFETs and Other Multi-Gate Transistors</i> 49-111 (Springer 2008) (“Colinge”)
Ex. 1059	Xuejue Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting, 67-70 (1999) (“Huang 1999”)
Ex. 1060	Digh Hisamoto et al., <i>A Folded-channel MOSFET for Deep-sub-tenth Micron Era</i> , International Electron Devices Meeting, 1032-1034 (1998) (“Hisamoto”)
Ex. 1061	<i>2001 International Technology Roadmap for Semiconductors - Front End Processes</i> , Semiconductor Industry Association (2001) (“2001 ITRS”)
Other Abbreviations and Conventions	
Petitioner	Intel Corporation
Patent Owner	Institute of Microelectronics, Chinese Academy of Sciences (IMECAS)

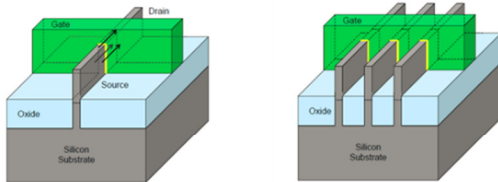
I. Introduction

The Institute of Microelectronics, Chinese Academy of Sciences (“IMECAS”) sued Petitioner Intel Corporation’s subsidiary for allegedly infringing the Chinese counterpart to U.S. Patent No. 9,070,719. Petitioner requests
5 institution of an IPR trial on claims 1-3 and 6-7 of the ’719 patent because prior art not before the examiner renders those claims unpatentable.

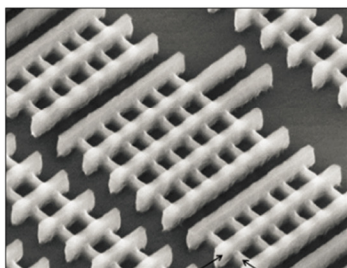
The ’719 patent is directed to cutting portions of gate lines during fabrication of semiconductor chips to form distinct gate electrodes for FinFETs (fin-based field effect transistors). As the ’719 patent concedes, IMECAS did not
10 invent FinFETs. Rather, Intel introduced the first commercial chips based on Tri-Gate FETs, which the ’719 patent identifies as a type of prior art FinFET. *See Ex.*

Intel 22nm Announcement (May 2011)

22 nm Tri-Gate Transistor 22 nm Tri-Gate Transistor



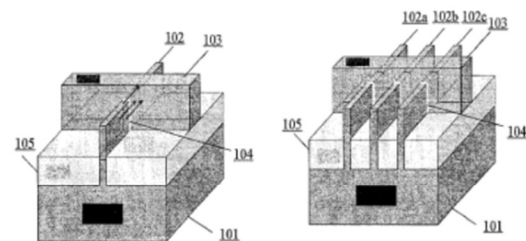
22 nm Tri-Gate Transistor



Gates Fins



IMECAS ’719 Patent Figures



(a)

(b)

Fig. 1

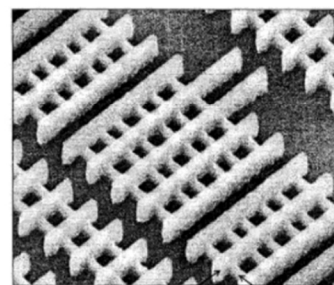


Fig. 2

1001, 1:48-51. In a tacit acknowledgement of that fact, the '719 patent copies illustrations and a micrograph from Intel's 2011 22nm Tri-Gate Transistor high-volume manufacturing press announcement while covering up Intel's labels.

Above, the '719 patent's Figures 1 and 2 are shown next to originals from Intel's public presentation (Ex. 1033 at 5, 7, 8).

The challenged claims require that sidewall spacers be formed around the sides of a gate line *before* it is cut at selected locations to form separated gate electrodes for different transistors. But several prior art references not previously before the patent office show that forming spacers on sidewalls of gate lines before cutting them into separate gate electrodes was known long before the alleged invention. The prior art also taught the '719 patent's reason for that spacer-before-cut sequence—to save space. None of that was new. Nor did the other concededly conventional claim limitations point to anything new.

Petitioner previously filed an IPR petition relating to the '719 patent that relied on Okuno's U.S. published application. IPR2018-01574, Paper 2. Patent Owner's preliminary response argued, without any expert support, that the sidewall spacers in Okuno's U.S. application are implanted regions in the substrate *below* the gate lines. While Petitioner and its expert believe that no skilled person would read the reference that way, the original Japanese PCT application publication makes even more clear that Okuno's sidewall spacers were, as denoted by the term

“sidewall spacer” itself, formed by an oxide layer deposited *over* the substrate surrounding the gate lines. In order to prevent future disputes regarding Okuno’s teachings about sidewall spacer formation, Petitioner submits grounds based on the Japanese PCT application (together with a translation) in this Petition.

5 II. Mandatory notices

A. Real party in interest

The real party in interest is Intel Corporation.

B. Related matters

Patent Owner has sued Petitioner’s subsidiary and others in China for patent
10 infringement of a counterpart Chinese patent in *Institute of Microelectronics of the Chinese Academy of Sciences v. Intel, Dell and Jingdong* (Beijing Higher People’s Court). Petitioner also has one other pending petition against claims 1-3 and 6-7 of the '719 patent in IPR2018-01574. That petition was filed on September 18, 2018.

C. Notice of counsel and service information

15 Petitioner’s counsel are:

Lead Counsel	Back-Up Counsel
Jonathan McFarland Reg. No. 61,109 PERKINS COIE LLP 1201 Third Avenue, Suite 4900 Seattle, WA 98101 206-359-8000 (phone) 206-359-9000 (fax) <i>Attorney for Intel Corporation</i>	Chad Campbell <i>Pro hac vice</i> to be submitted Tyler Bowen Reg. No. 60,461 PERKINS COIE LLP 2901 N. Central Ave, Suite 2000 Phoenix, AZ 85012 602-351-8000 (phone) 602-648-7000 (fax) <i>Attorneys for Intel Corporation</i>

Petitioner consents to electronic service. All service and communications to the above attorneys can be sent to: Intel-IMECAS-Service-IPR@perkinscoie.com.

A Power of Attorney for Petitioner will be filed concurrently with this Petition.

III. Requirements for *inter partes* review

5 A. Ground for standing

The '719 patent qualifies for IPR and Petitioner is not barred.

B. Identification of challenge

Claims 1-3 and 6-7 should be cancelled as obvious:

Ground	References	Challenged Claims
1	Okuno PCT ¹ & Liaw (Exs. 1041, 1003)	Claims 1-3, 6
2	Okuno PCT, Liaw & Kim (Exs. 1041, 1003, 1010)	Claim 7
3	Okuno PCT & Chang (Exs. 1041, 1004)	Claims 1-3, 6
4	Okuno PCT, Chang & Kim (Exs. 1041, 1004, 1010)	Claim 7

None of these references was before the patent office during examination of the '719 patent. Petitioner further relies on Dr. Scott Thompson's Declaration (Ex. 1045) and other supporting evidence in Petitioner's exhibit list.

¹ Okuno PCT refers to Exhibit 1041, which is a certified English translation of the Japanese PCT application publication separately submitted as Exhibit 1040.

IV. The '719 patent

The '719 patent issued on June 30, 2015 from a November 18, 2011 PCT application and claims priority to a Chinese patent application filed on August 22, 2011. Each of Petitioner's cited references predates August 22, 2011, but

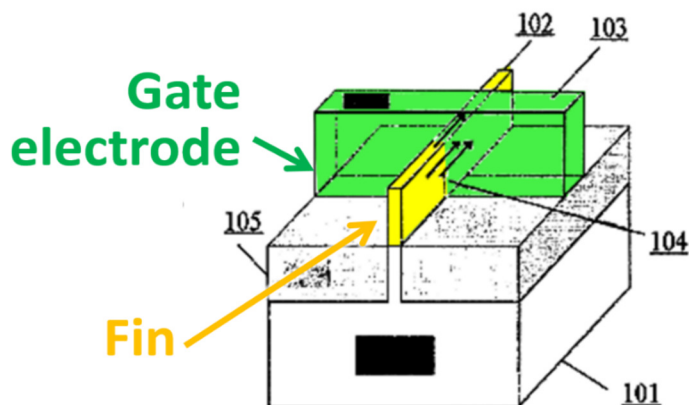
5 Petitioner reserves the right to challenge the claimed priority if it becomes relevant.

A. The '719 patent's disclosures

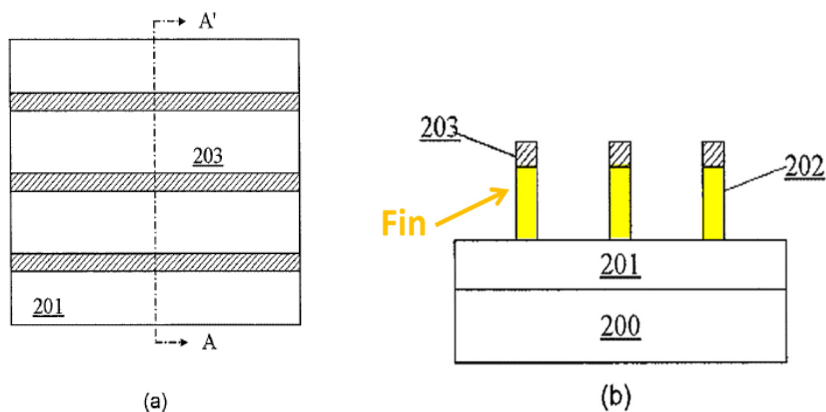
The '719 patent describes a semiconductor device having "fins" and a method for making the device. Ex. 1001, Abstract, 1:18-23. The patent explains that, as circuit density increased over time, transistors using vertical fin shapes (Fin
10 Field Effect Transistors or FinFETs) became common. *Id.*, 1:27-31. These vertical structures save space by allowing transistor count per area to increase. Ex. 1045 ¶¶ 54-55, 58-60.

1. Conventional FinFET structures and fabrication methods

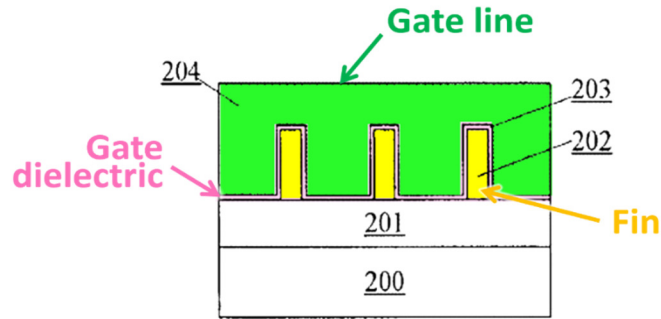
As described in the '719 patent, fabricating FinFETs was known and
15 conventional long before the alleged invention. Ex. 1001, 1:25-2:10. Annotated Figure 1(a) below (which Patent Owner took from Intel's press announcement (Ex. 1033)) shows a basic FinFET structure. Fin 102 (yellow) projects upward from silicon substrate 101, and gate electrode 103 (green) intersects the fin with dielectric layer 104 between them. *Id.*, 1:32-37. The gate acts as a switch that
20 turns the transistor on and off. Ex. 1045 ¶ 58.



The '719 patent explains that a benefit of FinFETs is their “compatibility with the conventional manufactur[ing] processes.” Ex. 1001, 1:30-31; Ex. 1045 ¶ 128. The patent describes many such “conventional” processing techniques. Ex. 1001, 3:49-5:30. First, fins 202 (yellow) are formed, as shown in annotated Figure 3 below. *Id.*, 3:51-63.

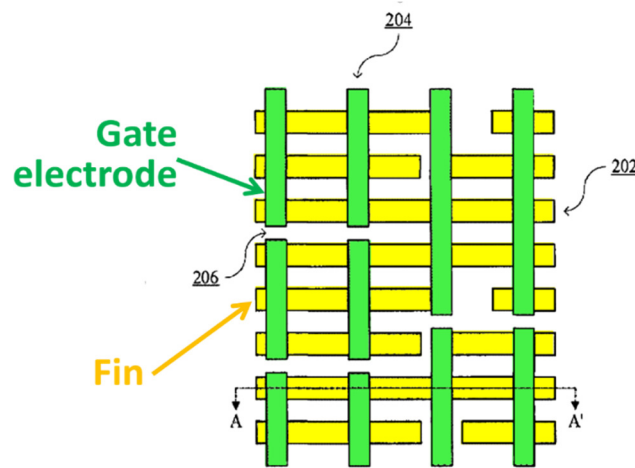


Next, gate dielectric layer 203 (pink) is deposited over the fins, and gate lines 204 (green) are formed across the fins and dielectric layer, as shown in annotated Figure 4's cross-section below.

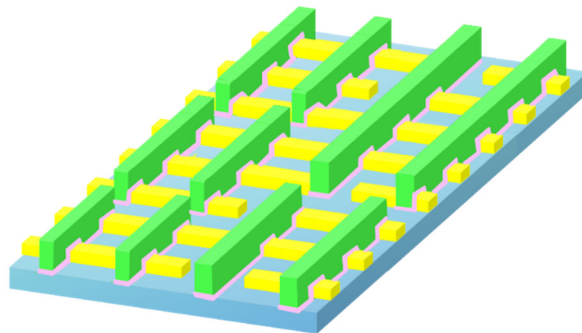


Gate lines 204 are then etched (i.e., cut) to isolate separate semiconductor devices, as shown below in Figure 7(a) and the related three-dimensional rendering.

Id., 4:46-53.



(a)



Finally, dielectric sidewall spacers 207 (blue) are formed to surround the individual gate electrodes, as shown in annotated Figure 8 below and the related three-dimensional rendering (with gate dielectric added in pink). Ex. 1045 ¶ 133.

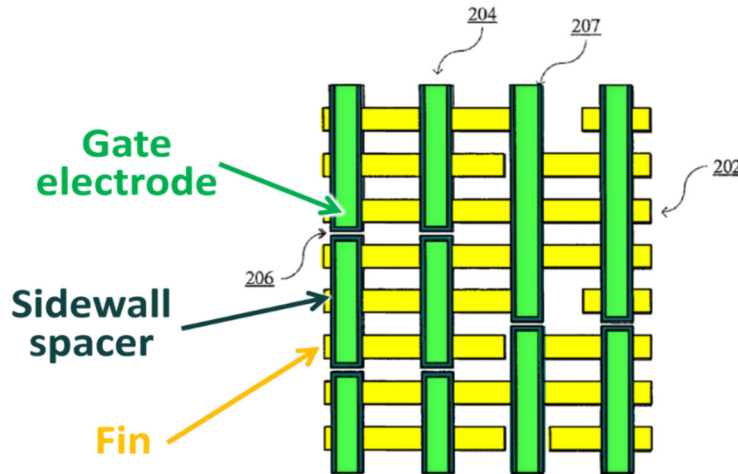
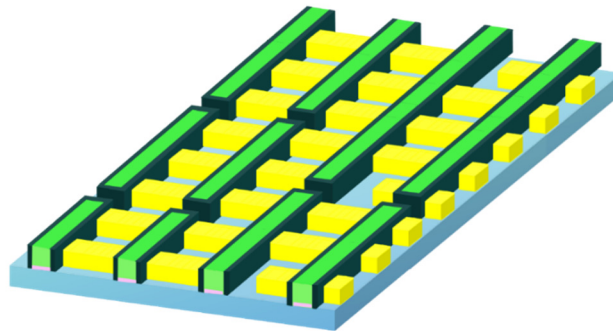


Fig. 8



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Known “conventional” processing approaches also included a “replacement gate process.” Ex. 1001, 5:21-28, 8:10-15. In it, “sacrificial” gate lines usually made of polysilicon were formed. The sacrificial gate lines were later removed and replaced with metal gate lines. *Id.*, 8:13-15, 8:20-26, 8:46-53. The process

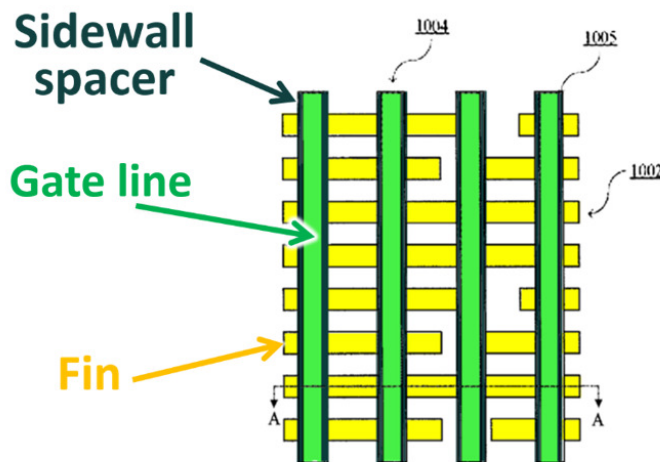
was sometimes called “gate last.” Ex. 1045 ¶¶ 116-126. The patent confirms that “[t]hose skilled in the art can devise various ways to implement the replacement process for the gate lines.” Ex. 1001, 8:53-54; Ex. 1045 ¶ 135.

2. The alleged point of novelty: gate isolation timing

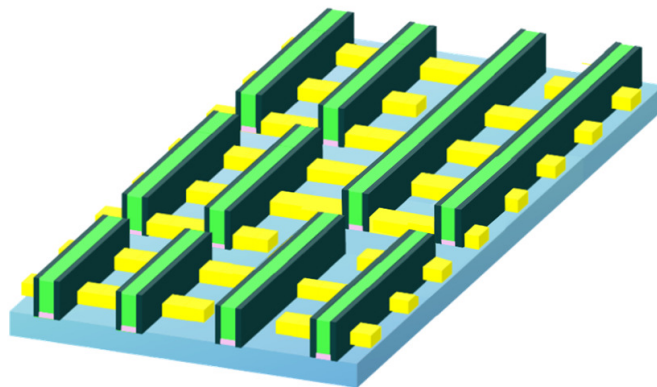
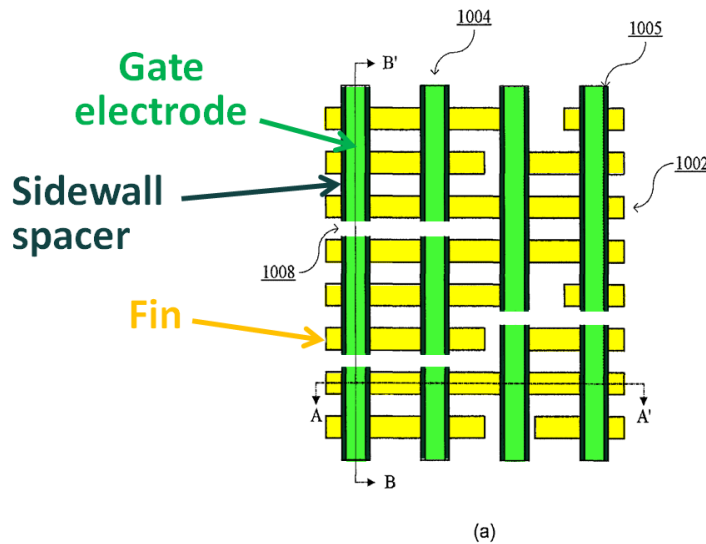
The '719 patent states that “as device feature sizes are becoming smaller continuously, it is more difficult to make gate electrodes for the fin transistors.” Ex. 1001, 1:66-2:3. Specifically, the patent says isolating gate lines *before* forming sidewall spacers could cause sidewall spacer material to enter the cut and, if cuts are very small, create voids in the dielectric. *Id.*, 5:10-20. To address this problem, the patent describes isolating (e.g., by cutting) different portions of gate lines *after* forming the sidewall spacers. *Id.*, 2:49-55, 5:29-30. Thus, the alleged invention simply reorders two conventional processing steps. Ex. 1045 ¶ 136.

In the patent’s approach, sidewall spacers (blue) are added to gate lines 1004 (green) before cutting, as shown in annotated Figure 10(a) below. Ex. 1001, 6:11-

28. The gate electrodes are then cut, as shown in annotated Figure 11(a) and the related three-dimensional rendering (with gate dielectric



added in pink) below. In this instance, the sidewall spacers (blue) do not enter the cuts between gate electrodes (green). *Id.*, 2:49-55.



5 Ex. 1045 ¶¶ 136-137.

The '719 patent says this approach reduces the “minimum electrical isolation space between the devices,” improving “integration density of the devices.” Ex. 1001, 2:55-58.

B. The '719 patent claims

10 Independent claim 1 reads:

1. A method for manufacturing a semiconductor device structure, comprising:

forming a fin in a first direction on a semiconductor substrate;

forming a gate line in a second direction, the second direction crossing the first direction on the semiconductor substrate, and the gate line intersecting the fin with a gate dielectric layer sandwiched between the gate line and the fin;

forming a dielectric spacer surrounding the gate line; and

performing inter-device electrical isolation at a predetermined position after forming the dielectric spacer, wherein isolated portions of the gate line form independent gate electrodes of respective devices.

Claim 1 recites several conventional steps for forming FinFET structures, such as a fin, a gate line crossing over the fin, a dielectric layer between the fin and the gate line, and gate line sidewall spacers. The claim also recites “performing inter-device electrical isolation at a predetermined position after forming the
5 dielectric spacer.”

Dependent claims 2-3 and 6-7 recite various conventional structures and processes:

- isolating gate line portions by cutting the gate line (claim 2),
- also cutting the sidewall spacers (claim 3),
- isolating before forming metal interconnections (claim 6), and

10

- inserting a replacement gate line after forming sidewall spacers on a sacrificial gate line but before isolation (claim 7).

C. '719 prosecution history

During prosecution, the applicant relied on performing gate line isolation

5 *after* sidewall spacer formation to distinguish the prior art.

The patent office initially rejected/objected to all 17 pending claims. Ex. 1007 at 128. The examiner found that Zhu anticipated six claims. Zhu disclosed fins, gate lines, a gate dielectric, sidewall spacers, and isolating portions of the gate line to form independent transistors, among other claim limitations. *Id.* at 129-31.

10 The examiner found that Wang anticipated two more claims and that two other claims were obvious over Zhu in view of Kawa because the latter taught isolation by cutting a gate line and filling the void with a dielectric material. *Id.* at 131-32. The examiner concluded that dependent claims 6-7 would be allowable if rewritten in independent form because “the prior art of record fails to teach forming the
15 dielectric spacers before performing device isolation.” *Id.* at 133.

The applicant then cancelled the three pending claims and amended independent claim 1 to add that isolation occurs “*after* forming the dielectric spacer.” *Id.* at 89-91 (emphasis added). The applicant argued that Zhu taught “devices resulting from the process where inter-device isolation is performed
20 *before* forming dielectric spacer[s].” *Id.* at 94 (emphasis added).

The examiner allowed claims 1-7, noting that “the prior art of record falls short with regards to teaching performing the device isolation *after* forming the dielectric spacers.” *Id.* at 72 (emphasis added). The same explanation appears in the notice of allowance. *Id.* at 36-37.

D. Level of ordinary skill in the art

A person of ordinary skill in the art as of the alleged invention (“skilled person”) would have had at least a Bachelor’s degree, Master’s degree, or Ph.D. in electrical engineering, chemical engineering, materials science engineering, physics, chemistry, or a similar field, and three years’ experience working in semiconductor design, manufacturing, development, and/or process architecture. Ex. 1045 ¶ 44.

E. Claim Construction

Claim terms in an IPR are construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100; *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). In a related IPR proceeding, Patent Owner argued that the phrase “a dielectric spacer surrounding the gate line” from claim 1 of the '719 patent should be construed as “a dielectric spacer enclosing the gate line on all side surfaces.” IPR2018-01574, Paper 11 at 9-10. As described below (at 39-41), Okuno PCT (and other prior art)

disclosed a dielectric spacer enclosing the gate line on all side surfaces, thus meeting Patent Owner's interpretation of the claimed phrase. Specifically, as Dr. Thompson explained, the prior art taught sidewall spacers "surrounding" the gate lines in the same way that term was used in the '719 patent by "depositing on the entire structure one or more layers of dielectric materials" and then etching. Ex. 1001, 6:11-17; Ex. 1045 ¶¶ 263-270. No further construction is required here because, as the Federal Circuit has explained, the Board need only construe terms "to the extent necessary to resolve [a] controversy" between parties. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (citation omitted).²

10 V. Prior art overview

A. Drive to increase transistor density

For decades, the semiconductor industry has been shrinking transistors to reduce fabrication costs and increase computing power and efficiency. Ex. 1045

² Though unnecessary for this Petition, Petitioner reserves the right to challenge Patent Owner's construction. Further, while the broadest reasonable interpretation (BRI) standard applied to claim construction in IPR2018-01574 and the *Phillips* standard applies here, the result is the same under either standard: the prior art taught the "surrounding" limitation under Patent Owner's narrow construction requiring sidewall spacers on the ends (in addition to the sides) of the gate line.

¶¶ 53-54. Rapid transistor shrinkage is called “Moore’s Law”—a rule of thumb named after Intel co-founder Gordon Moore positing that the number of transistors per circuit layout area will double every two years or so. *Id.* ¶ 53. In the 1990s and 2000s, prior art efforts to advance Moore’s Law made transistors and the isolation between them increasingly small. *Id.* ¶¶ 53-54. Moore’s Law in the decade before the ’719 patent is illustrated below:

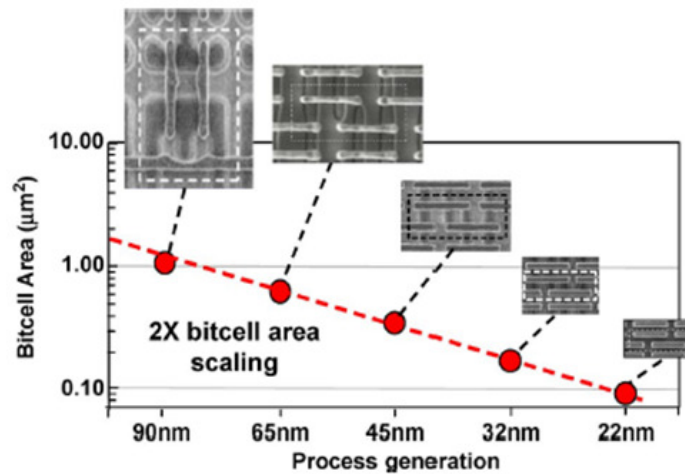


Fig. 1. SRAM cell design from 90 nm to 22 nm illustrates the combination of new innovations and continual improvement strategies for addressing variation challenges while maintaining a 2× area Moore’s Law scaling.

Id. ¶ 54 (citing Ex. 1037).

As transistor features shrank to one-billionth of a meter, new fabrication techniques were needed to form features smaller than the light wavelength used in lithography to form them. *Id.* ¶¶ 54-56. As one solution, manufacturers formed grids of individual layers such as active regions (including sources, drains, and channels) running in one direction on a semiconductor substrate and perpendicular gate lines intersecting those regions. *Id.* ¶¶ 56, 100-101. Masks and etching were

used to electrically isolate individual transistors by cutting away unwanted material from the resulting grid pattern. *Id.* ¶¶ 56, 101, 103. Known as “line” plus “cut” processing, this technique was well known before the alleged invention, as the '719 patent concedes by describing the line-and-cut method as part of the “conventional process.” *Id.* ¶¶ 101-103; Ex. 1001, 4:15-65, 5:21-28. It was often used to separate gate electrodes by cutting gate lines. Ex. 1045 ¶¶ 56, 101, 103.

The “line-and-cut” method required multiple known steps, including forming sidewall spacers on a gate line. *Id.* ¶¶ 104-107. It was known that the step sequences could vary in different process flows. *Id.* ¶ 111. For example, cutting gates (to electrically isolate them) could occur before or after forming sidewall spacers. *Id.* Both approaches were known. *Id.* ¶¶ 108-109, 111.

“Gate last” or replacement gate processing is another prior art technique for furthering Moore’s Law. In it, a dummy or sacrificial gate is removed and replaced with a metal gate material. *Id.* ¶¶ 116-126. Metal gates are inserted later because of susceptibility to damage during earlier process steps. *Id.* ¶ 123; Ex. 1025, 2:19-25. Metal gates facilitate smaller circuits. Ex. 1045 ¶¶ 121-122.

Historically, silicon dioxide was a popular gate dielectric material, but its performance degraded as layers became thinner. *Id.* ¶ 121; Ex. 1020, 1:20-25.

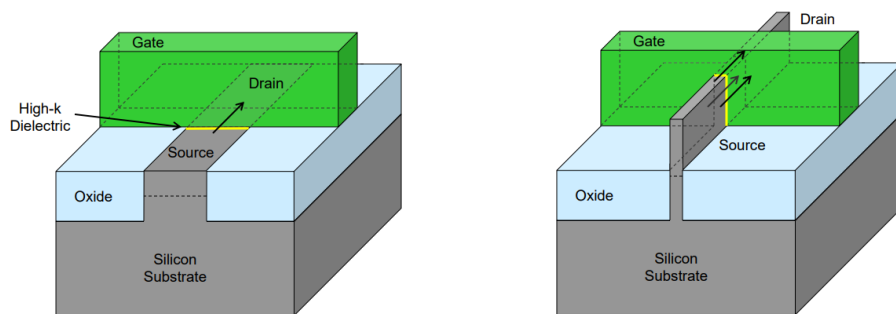
Thus, chip designers eventually turned to high dielectric constant materials (high-k dielectric) for high performance, electrically thinner gate dielectric layers. Ex.

1045 ¶ 121; Ex. 1020, 1:20-31. And because most high-k dielectrics and polysilicon are not compatible, designers also substituted metal for polysilicon as the gate material. Ex. 1045 ¶¶ 121-122; Ex. 1020, 1:32-37.

Finally, “FinFET” structures also emerged. Ex. 1045 ¶¶ 47, 55, 57-64.

5 FinFETs use three-dimensional fin-shaped active regions instead of planar (flat) ones. *Id.* ¶¶ 58-59. Intel’s 2011 announcement of imminent high-volume production of its 22nm Tri-Gate FinFETs schematically compared planar and Tri-Gate FinFET structures:

Traditional Planar Transistor 22 nm Tri-Gate Transistor



10 Ex. 1033 at 4-5. The vertical orientation of the fins permits the active regions to be placed more closely together. Ex. 1045 ¶ 60.

Petitioner was a pioneer of fin-based FET design, which Patent Owner tacitly acknowledged when it copied figures from Intel’s 2011 announcement (Ex. 1033) and pasted them into the '719 patent (without attribution) as Figures 1(a), 1(b), and 2. *Id.* ¶¶ 64-65. While Petitioner released high-volume manufacturing (HVM) commercial products with Tri-Gate FinFETs in 2011, FinFET structures

15

were made in lower volumes at least as early as 1998. *Id.* ¶ 62. There was no need to introduce Tri-Gate FinFETs in HVM commercial products before 2011 because planar devices were able to meet size reduction and performance enhancement requirements until that point. *Id.* ¶ 63. When the planar design reached its scaling limits, Petitioner and other manufacturers began to implement FinFETs in commercial HVM products to further pursue Moore's Law. *Id.* Patent Owner, by contrast, has never commercialized a single FinFET product.

Prior art FinFET designs leveraged the line-and-cut and replacement gate processes. *E.g.*, Ex. 1001, 4:54-61, 5:21-28 (line-and-cut method); Ex. 1003, 7:25-38, 4:58-61, 7:15-18, 8:5-17; Ex. 1004, 3:54-4:31, 4:40-49, Figs. 5, 6A (line-and-cut in FinFET designs); Ex. 1010 ¶¶ 3, 37-42; Ex. 1013 ¶¶ 13, 15, 26, 28; Ex. 1015, 3:8-59; Ex. 1019, 1 (FinFET replacement gate processing); Ex. 1045 ¶¶ 109, 125.

B. Prior art techniques described and claimed in the '719 patent

The following line-and-cut process flow steps for FinFETs mentioned in the '719 patent were well known in the prior art: forming fins, forming gate lines, forming a dielectric between a fin and a gate line, forming sidewall spacers, performing replacement gate processing, and cutting gates and spacers. Ex. 1045 ¶¶ 106, 154-160. The alleged point of novelty—electrically isolating gate electrodes after sidewall spacer formation (instead of before) and the benefits of

doing so—were also well known as shown in Liaw and Okuno PCT. Okuno PCT taught that isolation after sidewall spacer formation helped make circuits smaller: “since the gate is cut and separated last,” spacers are “not present between the two facing driver transistors,” which makes it “possible to shorten the distance ‘d’ between the active regions” and, thus, “contribute to miniaturization.” Ex. 1041 ¶ 26. That was the same problem the '719 patent purported to solve years later. Ex. 1001, 2:49-58; Ex. 1045 ¶ 136. Below, Petitioner briefly summarizes relevant teachings of the prior art.

C. Cutting gate lines after sidewall spacer formation (instead of the reverse) was well known in the prior art

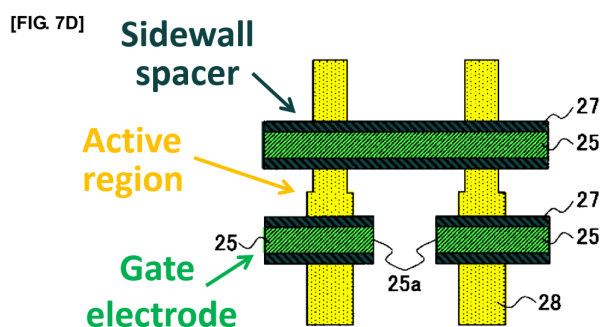
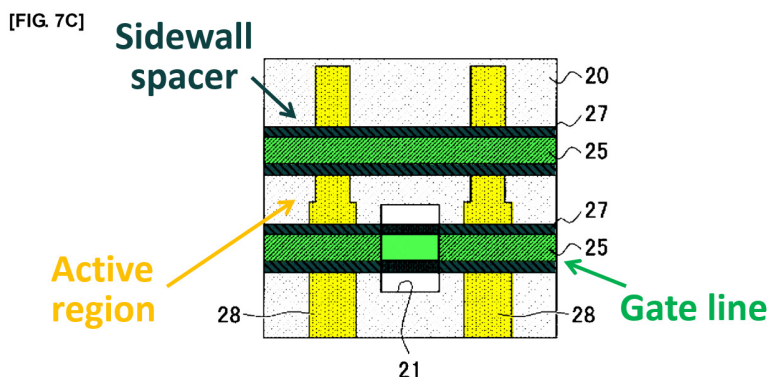
The references below disclosed performing electrical isolation (e.g., by cutting gate lines) after sidewall spacer formation, and other conventional structures and processes described in the '719 patent. The examiner did not have the benefit of these references during prosecution of the '719 patent.

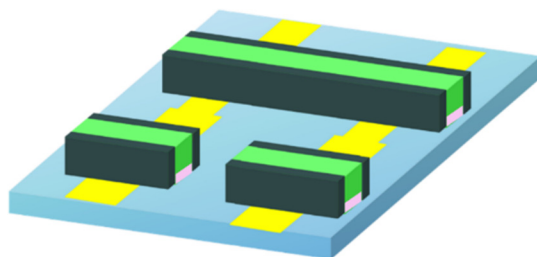
1. Okuno PCT (Ex. 1040 (Japanese)) / (Ex. 1041 (English translation))

Okuno PCT (Japanese) (published in 2008; prior art under 35 U.S.C. §§ 102(a) and (b)³) is directed to an SRAM circuit. Ex. 1040 ¶ 2; Ex. 1041 ¶ 2. As shown in annotated Figure 7C below, Okuno PCT disclosed active regions

³ All references to 35 U.S.C. § 102 are pre-AIA.

(yellow) including source/drain regions 28 crossed by gate lines 25 (green) having sidewall spacers 27 (blue). Ex. 1041 ¶¶ 24, 29-30. Okuno PCT also disclosed that a dielectric gate oxide layer (not shown in Figures 7C and 7D) is formed on the active regions before deposition of gate lines. *Id.* ¶¶ 29-30. And just like the '719 patent, Okuno PCT taught isolating gate electrodes *after* forming sidewall spacers on the gate line. Figure 7C shows mask 20 with opening 21 for etching the gate line 25 (green) on the bottom and its sidewall spacers 27 (blue). *Id.* ¶ 32. Below, annotated Figure 7D and the related three-dimensional rendering (with gate dielectric added in pink) show the resulting cut (i.e., isolation) between two gate electrodes 25 (green). *Id.* ¶ 33. Okuno PCT sought to continue Moore's Law by using line-and-cut techniques. Ex. 1045 ¶¶ 171-176.





2. Liaw (Ex. 1003)

Liaw (filed on February 8, 2010; prior art under at least 35 U.S.C. § 102(e))

is directed to an SRAM circuit. Ex. 1003, 1:5-8. As shown below in annotated

Figure 3K and the related three-dimensional rendering (with gate dielectric added

in pink), Liaw disclosed a FinFET device with fins 215, 217 (yellow) and gate

electrodes 311 (green) intersecting the fins. Liaw taught a gate dielectric layer 301

(not shown in Figure 3K) between the fins and gate electrodes. *Id.*, 5:33-36, Figs.

3A, 3I. And although not shown in Figure 3K, the specification described forming

“permanent spacers” on the uncut gate electrodes (which have been added in blue

to Figure 3K below for illustration). *Id.*, 7:25-38. **After** forming sidewall spacers,

Liaw taught etching the gate lines to “separate the different transistors,” as shown

in Figure 3K below. *Id.*, 8:10-17. Liaw’s techniques sought to advance Moore’s

Law by using both

FinFETs and line-
and-cut processing.

Ex. 1045 ¶¶ 163-

169.

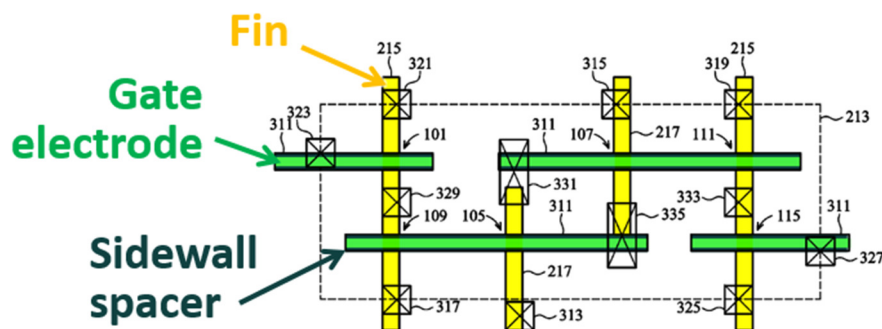
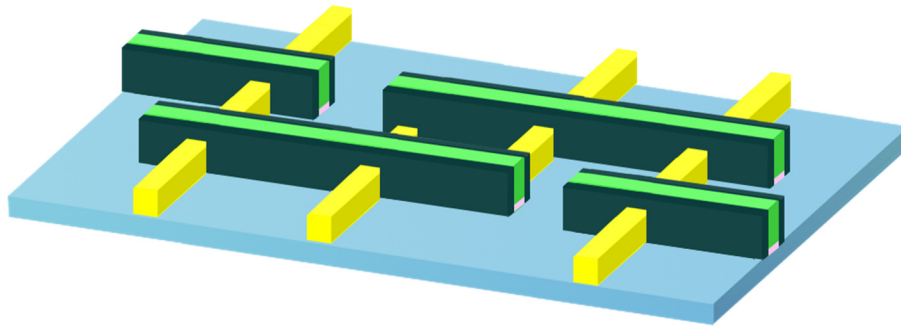


Figure 3K



3. Chang (Ex. 1004)

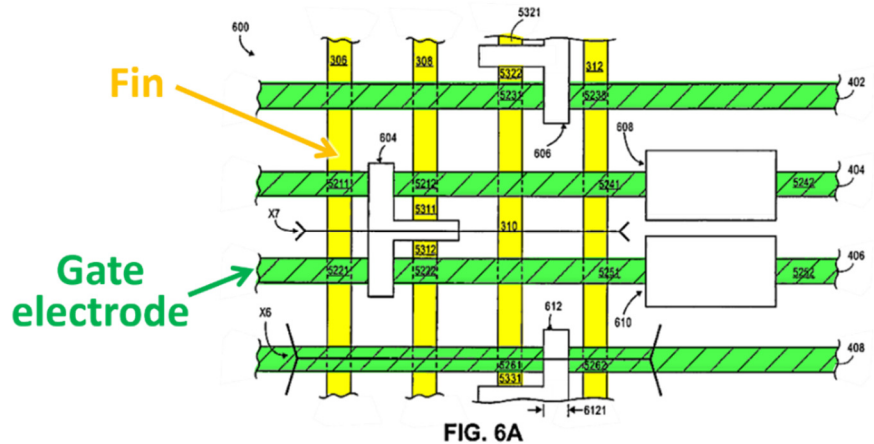
Electrically isolating separate FinFET devices was nothing new and was the natural byproduct of the line-and-cut process flow. Ex. 1045 ¶¶ 187-192. For example, Chang (issued in 2008; prior art under 35 U.S.C. §§ 102(a) and (b)) taught a method of fabricating smaller semiconductor devices that included both FinFETs and a line-and-cut technique to form individual gate electrodes. Ex. 1004, 1:5-23, 6:48-65.

As shown below in annotated Figure 6A, Chang disclosed forming diffusion regions (active regions) 306, 308, 310, 312 (yellow) on a substrate where the regions can consist of fins in tri-gate structures.⁴ *Id.*, 3:25-30 (disclosing a non-

⁴ The '719 patent refers to a "tri-gate" FET as a type of FinFET that includes channels on three surfaces of the fin instead of just two. Ex. 1001, 1:45-54, 3:65-4:9; Ex. 1045 ¶ 189.

planar embodiment where “subsequently patterned gate electrodes would wrap around the top and sidewalls of the diffusion regions, thereby forming tri-gates or similar structures”). Gate lines 402, 404, 406, 408 (green) were added across the fins. *Id.*, 3:40-53, Figs. 4, 6A. Chang also taught cutting the gate lines to form

openings 604, 606, 608, 610, 612 and “electrically isolate” discrete gate electrodes. *Id.*, 3:54-



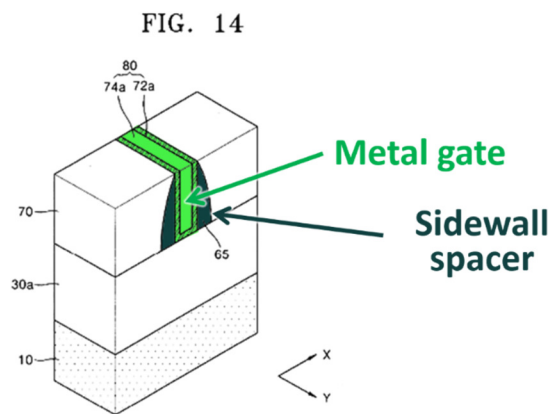
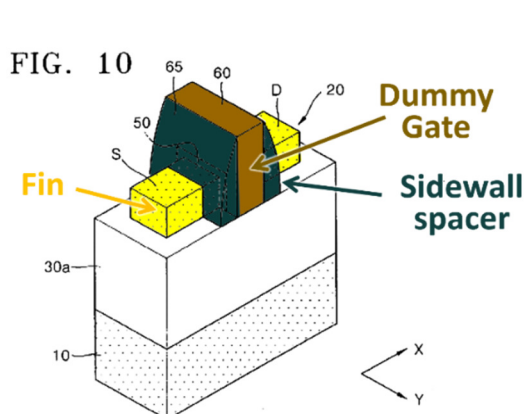
4:31, 4:40-49, Figs. 5, 6A; Ex. 1045 ¶¶ 190-191.

D. Replacement gate processing was conventional before the alleged invention

Replacement gate processing described in the '719 patent as “conventional” was well known and widely disclosed in the prior art. Ex. 1045 ¶¶ 193-202. That process was often performed after formation of sidewall spacers and advanced Moore’s law by allowing further scaling.

For example, Kim (published in 2006; prior art under 35 U.S.C. §§ 102(a) and (b)) disclosed a FinFET having a fin-shaped active area 20 (yellow), a gate insulting layer 50, a dummy gate 60 (brown), and sidewall spacers 65 (blue) around the dummy gate. Ex. 1010 ¶¶ 7, 10, 37-38. Kim taught initially forming

dummy gate 60 as shown in annotated Figure 10 below (*id.* ¶ 37) which was then removed and replaced with metal gate 80 (green) in annotated Figure 14 below (*id.* ¶¶ 41-42).



5 Ex. 1045 ¶¶ 195-198.

Petitioner is the assignee of several patents and published applications that disclose similar replacement gate processes. Two examples are Doyle (U.S. Patent Application Publication No. 2007/0152266, published in 2007) and Brask (U.S. Patent No. 7,531,437, issued in 2009). Doyle's process is depicted in annotated

10 Figures 4 and 7 below. Ex. 1013 ¶¶ 15, 19, 24, 26-28.

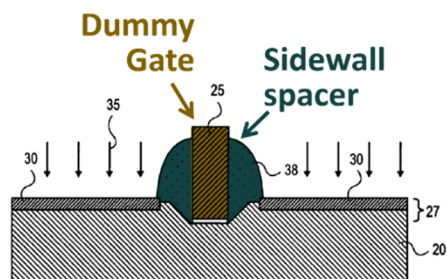


FIG. 4

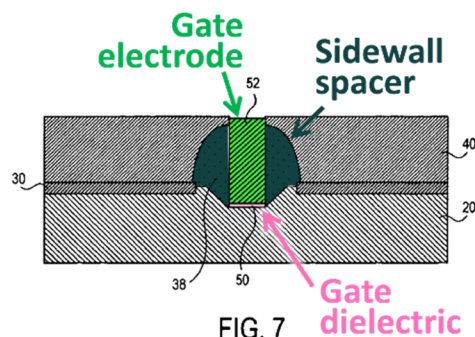


FIG. 7

Brask taught the same. Ex. 1015, 17:62-26:48. Ex. 1045 ¶¶ 199-201.

None of these references was before the examiner during prosecution of the '719 patent.

VI. The Petition raises unique arguments the Board should consider

A. Instituting review would be fair and avoid prejudice to Petitioner

5 Petitioner previously filed an IPR petition challenging the '719 patent based in part on Okuno's U.S. application (Ex. 1005). IPR2018-01574, Paper 2. In the preliminary response, Patent Owner argued that Okuno's U.S. application teaches that sidewall spacers are formed using a process called extension implantation such that the sidewalls are somehow down in the substrate, under the gate lines, not on
10 the sides of and surrounding the gate lines. IPR2018-01574, Paper 11 at 22-26. Although that reading of U.S. Okuno is untenable, Petitioner promptly obtained and analyzed a translation of Okuno's Japanese PCT (Ex. 1041), which is the parent of U.S. Okuno, and prepared this Petition. As described below (at 37-38), Okuno's Japanese PCT is clear that extension implantation (inserting atoms into
15 the substrate) and sidewall spacer formation (growing a film on the sides of the gate line) are separate processes and that Okuno's sidewall spacers are formed above the semiconductor substrate on the sides of and surrounding the gate lines as is widely taught in the prior art. The Board should institute review based on Okuno's Japanese PCT as incorporated in the grounds below because those
20 grounds are new to the patent office and doing so serves the interests of fairness.

The Board has discretion under 35 U.S.C. § 314(a) to institute review based on a second IPR petition challenging the same patent. The Board has explained that “there may be circumstances where multiple petitions by the same petitioner against the same claims of a patent should be permitted, and that such a

5 determination is dependent on the facts at issue in the case.” *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 18 (PTAB Sept. 6, 2017) (precedential) (Ex. 1042). A second petition is appropriate here under the *General Plastic* factors. Specifically, factors 3-7 justify a second petition, and factors 1 and 2 do not compel a different result.

10 Turning first to *General Plastic* factor 4, Petitioner acted quickly after learning of Patent Owner’s incorrect characterization of U.S. Okuno in Patent Owner’s January 28, 2019 preliminary response (Paper 11) in IPR2018-01574. Petitioner promptly obtained a translation of Okuno’s Japanese PCT and concluded that the Board should have access to it because the PCT application eviscerates

15 Patent Owner’s position. Because Petitioner acted quickly and before an institution decision on the first petition, factor 4 strongly favors institution here.

Under *General Plastic* factor 5, the interests of justice favor institution so that the Board may consider Okuno’s Japanese PCT, whose teachings cut through the confusion created by Patent Owner and provide additional information that

20 ensures a just resolution to the dispute between the parties. *See* 37 C.F.R.

§ 42.1(b). Although Petitioner maintains that U.S. Okuno taught what the '719 patent claimed, Okuno's Japanese PCT removes any doubt that sidewall spacer formation is separate from extension implantation, contrary to Patent Owner's argument. Ex. 1041 ¶ 9 ("extension implantation is performed, then sidewalls (SW) 27 are formed"), ¶ 24 ("extension implantation is performed, sidewall spacers (hereafter referred to simply as 'sidewalls' or 'SW') 27 are formed"), ¶ 31 ("pocket implantation and extension implantation are performed as was conventional, sidewalls 27 having a width of 30 nm to 80 nm are formed"), claim 11; Ex. 1045 ¶ 263. Okuno's Japanese PCT also taught that sidewall spacers are formed using a chemical vapor deposition (CVD) process that creates sidewalls above the substrate around the gate lines. Ex. 1041 ¶ 31 ("sidewalls 27 ... are formed, for example by a CVD oxide film"). Those teachings were well known in the prior art. Ex. 1045 ¶¶ 264-269.

General Plastic factor 6 further supports institution on this Petition, which will not meaningfully increase the burden on the Board. The grounds in this Petition resemble a subset of the grounds from the petition in IPR2018-01574, but replace U.S. Okuno with Okuno's Japanese PCT. This Petition thus tracks the petition in IPR2018-01574 in its discussion of the '719 patent, the overview of the prior art, and its citations to Liaw, Chang and Kim. To further ease any impact on the Board, Petitioner will file a motion to consolidate this IPR proceeding with

IPR2018-001574 so the Board can address the issues together. Consolidating this Petition with IPR2018-01574 will facilitate reaching the correct result and obviate the need for the Board to address any further disputes regarding the meaning of Okuno's sidewall spacers 27.

5 *General Plastic* factor 7 favors Petitioner because the Board has yet to decide whether to institute review in IPR2018-01574. The deadline for the institution decision is April 29, 2019. Accordingly, the one-year period for issuing any final written decision in that proceeding has yet to begin. In any consolidated proceeding, Petitioner is amenable to adjusting the schedule to eliminate or
10 minimize any impact on the Board's final written decision in IPR2018-01574.

General Plastic factor 3 also favors Petitioner. Although Petitioner received Patent Owner's preliminary response in IPR2018-01574 before filing this Petition, the Board has yet to issue its institution decision. Without access to that decision, it was not possible for Petitioner to "strategically stage [its] prior art and arguments
15 in multiple petitions," using a Board decision "as a roadmap"—which is the situation *General Plastic* sought to prevent. Ex. 1042 at 17. By contrast, the Petition here focuses on the disclosures of Okuno's Japanese PCT, which became material when Patent Owner presented its incorrect characterization of U.S. Okuno. It is important that the Board consider Okuno's Japanese PCT, as that
20 reference refutes Patent Owner's argument, providing the Board with more

complete information relating to the patentability of the claims of the '719 patent.

Moreover, Petitioner did not strategically withhold Okuno's Japanese PCT.

Rather, Petitioner obtained the translation promptly after Patent Owner made its incorrect argument and then quickly submitted this Petition to the Board for

5 consideration. Given these circumstances, it would be prejudicial to Petitioner if the Board did not consider Okuno's Japanese PCT.

General Plastic factors 1 and 2 are outweighed by the circumstances described above and do not dictate a different result. Overall, given the facts surrounding this proceeding, the *General Plastic* factors support institution. A

10 discretionary denial based on 35 U.S.C. § 314(a) does not make sense in this proceeding "where the typical hallmarks of abusive, strategic serial petitioning are absent." *Intel Corp. v. Alacritech, Inc.*, IPR2018-00226, Paper 7 at 14 (PTAB June 5, 2018) (Ex. 1044). Rather than withholding Okuno's Japanese PCT to use in a second petition, Petitioner submitted it to the Board promptly after obtaining a
15 translation and learning that it disproved Patent Owner's incorrect characterization of Okuno's sidewall spacers. Discretionary denial under 35 U.S.C. § 314(a) was not intended to provide cover for Patent Owner's incorrect characterization of a prior art reference.

Further, instituting review would not prejudice Patent Owner. Okuno's
20 Japanese PCT is a translation of the publication of the parent application listed on

the face of U.S. Okuno and therefore known to Patent Owner. Moreover, the number of grounds and claims at issue in the Petition is limited and the references relied upon are the same as or related to those Patent Owner already addressed in IPR2018-01574. *See Agilent Techs., Inc. v. Thermo Fisher Sci. Inc.*, IPR2018-00313, Paper 23 at 38 (PTAB June 18, 2018) (“[W]e do not find the number of grounds raised to be so onerous that it is prejudicial to or constitutes harassment of the Patent Owner, especially given the number and scope of the challenged claims.”) (Ex. 1043).

B. Petitioner’s prior art and arguments are new

Although U.S. Okuno incorporated by reference the “entire contents” of the initially-filed application relating to Okuno’s Japanese PCT, the patent office did not evaluate Okuno PCT’s disclosures or compare them to the claims of the ’719 patent during original prosecution or in IPR2018-01574. Moreover, Okuno’s Japanese PCT does not incorporate the language of U.S. Okuno, so the parties’ dispute regarding the meaning of U.S. Okuno’s disclosures is rendered moot in this Petition based on Okuno’s Japanese PCT.

The Petition relies on prior art references (Okuno’s Japanese PCT, Liaw, Chang, and Kim) that were not before the examiner during prosecution of the ’719 patent. These references are not cumulative of the art the examiner considered during original prosecution. For example, as described above (at 19-22), Okuno’s

PCT and Liaw each disclosed isolating gate electrodes after forming sidewall spacers, which is the allegedly novel aspect of the invention. Ex. 1007 at 36-37, 72. For these reasons, this Petition does not present “the same or substantially the same prior art or arguments previously presented” to the office, and 35 U.S.C.

5 § 325(d) does not apply to this Petition.

VII. Claims 1-3 and 6-7 of the '719 patent are unpatentable

A. Ground 1: Okuno PCT and Liaw render claims 1-3 and 6 obvious

As discussed above, the '719 patent identifies its alleged novelty as isolating portions of gate lines after forming sidewall spacers surrounding them. Okuno
10 PCT taught that step. And the combination of Okuno PCT and Liaw disclosed the other conventional limitations claimed in the '719 patent, rendering claims 1-3 and 6 obvious. Ex. 1045 ¶¶ 243-292.

A skilled person would have been motivated to combine the teachings of Okuno PCT and Liaw with a reasonable expectation of success because both relate
15 to the same technology—formation of six-transistor cell or “6T” cell SRAMs in semiconductor device fabrication—and described the same imperative to make SRAMs smaller. Ex. 1045 ¶¶ 203-220, 247-259. Okuno PCT was directed to achieving “miniaturization” through its teaching to form gate line sidewall spacers before cutting the gate line, thereby avoiding spacer material at the cut face and
20 allowing gate electrodes to be placed closer together. Ex. 1041 ¶¶ 24, 26. Liaw

taught what was by then widely known—that as SRAMs “are scaled down into the 32nm generations and beyond, ... FinFETs ... have become popular over the more standard planar transistors” used in Okuno PCT. Ex. 1003, 1:12-16.

Given the importance of reducing circuit size, a skilled person would have
5 used the FinFET techniques disclosed in Liaw (substituting fin-shaped active regions for Okuno PCT’s planar active regions) to further the size reduction objective of Okuno PCT. Ex. 1045 ¶¶ 205, 213, 250, 257. The '719 patent admits that such substitutions were already happening and that FinFET fabrication techniques were “conventional.” Ex. 1001, 1:27-31, 3:49-5:30. In fact, FinFETs
10 were first fabricated years before Okuno PCT was filed. Ex. 1045 ¶¶ 62, 256.

And FinFETs borrowed well-known techniques from planar transistor fabrication. Ex. 1028, abstract, 2:11-14; Ex. 1045 ¶¶ 207-212, 252-256. For example, Liaw confirmed that “standard lithographic techniques” were used to form the fins of FinFETs. Ex. 1003, 1:25-34. Patent Owner itself conceded that a
15 skilled person would have understood that planar elements could be formed using fins instead. Ex. 1012, 11:53-60 (“[I]t should be understood by those skilled in the art that the [planar] unit device may be formed as a non-planar Fin Field Effect Transistor (FinFET).”). In light of this evidence, a skilled person would have had a reasonable expectation of success when substituting Okuno PCT’s planar active
20 regions with the fin-shaped active regions taught in Liaw.

Fin substitution would have yielded a further circuit shrink over Okuno PCT, and as taught in Liaw, had several additional benefits, such as reducing current leakage and voltage variability across transistors, as was well known in the art. Ex. 1003, 1:17-23; Ex. 1028, 5:35-37; Ex. 1045 ¶¶ 206, 214, 250, 258-259.

1. Claim 1

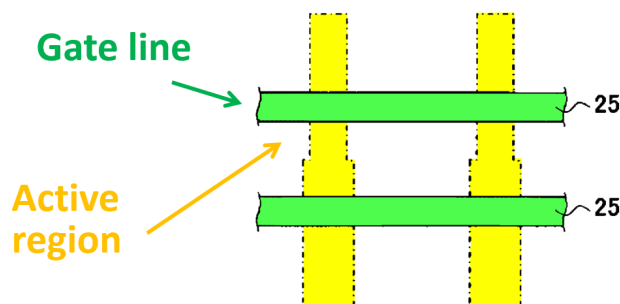
a. Preamble: “A method for manufacturing a semiconductor device structure, comprising”

Okuno PCT and Liaw each disclosed a method to manufacture a semiconductor device structure. Ex. 1041 ¶ 1 (“The present invention relates to a semiconductor device and a method of manufacturing the same, and particularly relates to a gate structure....”); Ex. 1003, 1:52-55 (“[A] method for manufacturing a semiconductor device comprises....”); Ex. 1045 ¶¶ 244-245.

b. 1[a]: “forming a fin in a first direction on a semiconductor substrate”

Okuno PCT disclosed forming active regions (yellow) on a semiconductor substrate running in a first direction, as shown in annotated Figure 7A below. Ex. 1041 ¶ 29.

[FIG. 7A]



To save space and increase transistor density, it would have been obvious to replace Okuno PCT's planar active regions with fin-shaped active regions.

The '719 patent recognized that fins were known in the prior art. Ex. 1001, 1:27-31, Figs. 1-2; *see also* above (at 1-2). Indeed, as explained above (at 17-18), using

5 fin-shaped active regions instead of planar ones was widely taught in the art. For example, Liaw taught forming fins in a first direction on a semiconductor

substrate. Liaw disclosed that its "method for manufacturing a semiconductor device comprises providing a fin" and that the fin can be formed by "providing a substrate and patterning the substrate to form a plurality of fins." Ex. 1003, 1:52-

10 64; *see also id.*, 4:43-44, Figs. 2F-2G; Ex. 1045 ¶¶ 246-247.

A skilled artisan would have been motivated to include fins (as taught in Liaw) in Okuno PCT's transistors to accomplish Okuno PCT's objective to reduce circuit size. Ex. 1041 ¶ 24 ("In the present invention, as a method of realizing further miniaturization...."); Ex. 1045 ¶¶ 250, 257.

15 A skilled person also would have incorporated fins into Okuno PCT's design to obtain other known FinFET benefits. Ex. 1045 ¶¶ 250, 258-259. Not only were FinFETs smaller than transistors with planar active regions, Liaw and others taught they improved performance: "FinFETs provide[d] for larger channel widths by using not only the top surface of the fin, as would be used in a planar transistor, but
20 also the sidewalls of the fin. By using these FinFET designs deleterious short-

channel effects, such as variability in the threshold voltage and excessive drain leakage currents, can be suppressed or reduced, thereby allowing for a more efficient device.” Ex. 1003, 1:17-23; *see also* Ex. 1028, 5:35-37 (“A FinFET structure ... not only reduces short channel effects, but also reduces leakage current through use of the double gates.”).

In a prior art patent, Patent Owner similarly acknowledged that skilled artisans knew the same semiconductor fabrication techniques applied to planar and fin-based designs. Ex. 1012, 11:53-60 (“[I]t should be understood by those skilled in the art that the [planar] unit device may be formed as a non-planar Fin Field Effect Transistor (FinFET).... It is understood by those skilled in the art that various measures in the prior art may be utilized to form the layers and regions in desired shapes.”). A skilled person would have replaced Okuno PCT’s planar active regions with fin-shaped active regions because “[t]hose two types of devices differ from each other just in that active regions are arranged differently and thus gates on the active regions are arranged differently.” Ex. 1012, 11:53-60; Ex. 1045 ¶ 252.

The evidence in the prior art that fin-shaped active regions substituted for planar active regions supports that a skilled person would have had a reasonable expectation of success in combining Okuno PCT with Liaw as described above.

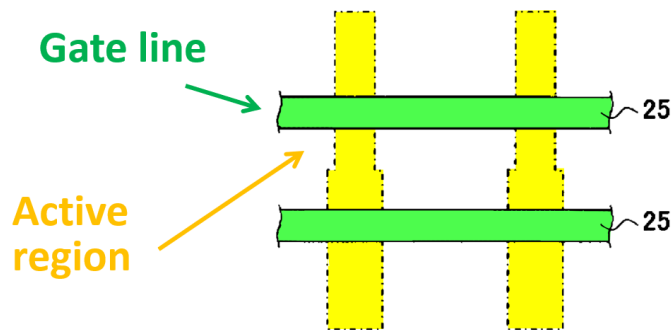
Ex. 1045 ¶¶ 251-256.

- c. 1[b]: “forming a gate line in a second direction, the second direction crossing the first direction on the semiconductor substrate, and the gate line intersecting the fin with a gate dielectric layer sandwiched between the gate line and the fin”

5

Okuno PCT disclosed forming multiple gate lines 25 (green) over active regions as shown in annotated Figure 7A below. Ex. 1041 ¶¶ 30.

[FIG. 7A]



Okuno PCT further disclosed forming a dielectric gate oxide layer (not shown) sandwiched between the active regions and the gate lines. *Id.* ¶ 29; Ex. 1045 ¶ 260. As explained above (at 34-35), it would have been obvious to substitute Liaw’s fin-shaped active regions for Okuno PCT’s planar active regions. Ex. 1045 ¶¶ 250-259.

Similar to Okuno PCT, Liaw disclosed forming gate lines (green) intersecting with perpendicular active regions that were configured as fins (yellow), with a gate dielectric layer between the fins and the gate lines (pink):

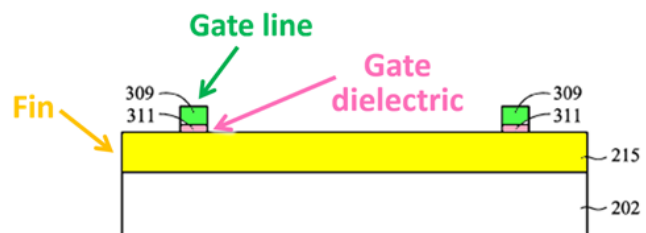
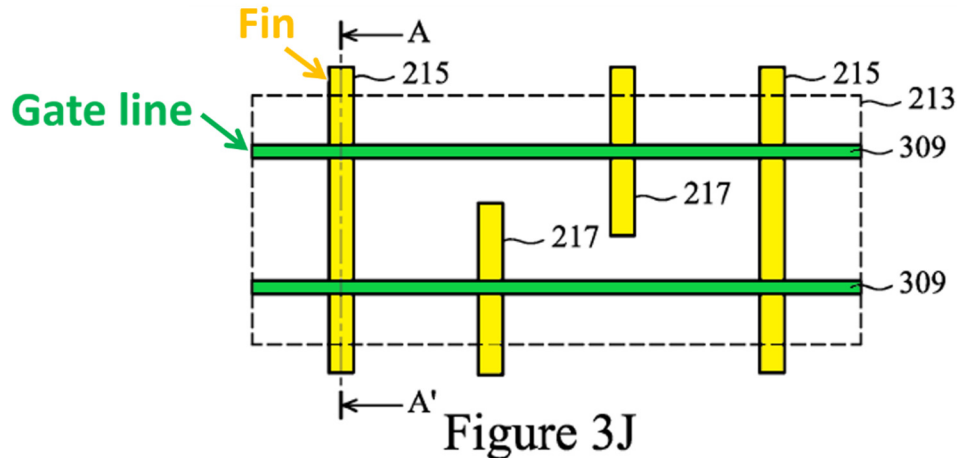


Figure 3I



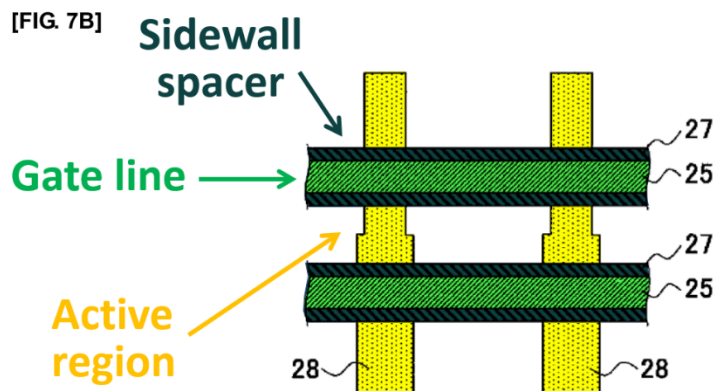
Ex. 1045 ¶¶ 261-262.

d. 1[c]: “forming a dielectric spacer surrounding the gate line; and”

5 Okuno PCT taught forming sidewall spacers 27 around gate lines 25. Ex. 1041 ¶¶ 9, 24, 31. The sidewall spacers were made from a dielectric oxide material. *Id.* ¶ 31 (“sidewalls 27 ... formed, for example by a CVD oxide film”). A skilled person would have understood that such a CVD oxide film would cover the entire surface of the semiconductor substrate, including the long sides and ends

10 of the gate lines. Ex. 1045 ¶¶ 263-264. The sidewall spacers (blue) are depicted in annotated Figure 7B below. Okuno PCT disclosed forming sidewall spacers after performing a different step known as extension

15 (“extension implantation is performed, then sidewalls



(SW) 27 are formed”), claim 11. These teachings eliminate any further dispute that extension implantation and sidewall spacer formation are separate steps. In the standard processing flow, extension implantation first implanted atoms *into* the substrate, and then deposition and etching sub-steps formed sidewall spacers on gate lines *above* the substrate. Ex. 1045 ¶¶ 81-97, 263. Extension implantation was a well-known technique for doping the substrate close to the gate to increase transistor reliability or resolve parasitic resistance issues. *Id.* ¶¶ 75-76, 81, 86. Forming sidewall spacers was a different process.

Okuno PCT disclosed other embodiments that used CVD to deposit optional sidewall spacers 29 *above* the substrate along the sides of either sidewall spacers 27 or gate electrodes 25, to form *thicker* combined sidewalls along the longer sides of the gate line, as shown below in Figure 7E. Ex. 1041 ¶ 34; *see also* Figs. 7F, 9, claim 12. Optional sidewall spacers 29 were added depending on conditions of a subsequent silicide process. *Id.* ¶¶ 33-34. Although this Petition relies on Okuno PCT’s embodiments without optional sidewall spacers 29 as prior art (e.g., Fig.

7D), the embodiments with them

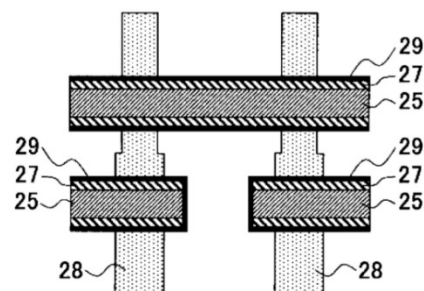
[FIG. 7E]

further confirm that sidewall spacers

27 were also formed above the

substrate and along the sidewalls of

the gate line. Ex. 1045 ¶ 263.



Okuno PCT Figure 7B above includes curvilinear ends to indicate that the gate lines continue to the left and right. Ex. 1045 ¶ 264. Okuno PCT disclosed that sidewall spacers are formed on the sidewalls of the gates. Ex. 1041 ¶ 24 (“with the gate electrode 25 still continuous, ... sidewall spacers (hereafter referred to simply as ‘sidewalls’ or ‘SW’) 27 are formed”). Given those disclosures, a skilled person would have understood that the sidewalls also surrounded the far ends of the gate lines (even though those ends are not shown in Figure 7B). Ex. 1045 ¶ 264. Then reactive ion etching (RIE) was used to cut the gates and sidewall spacers. Ex. 1041 ¶ 32, Figs. 7C, 7D; Ex. 1045 ¶ 276. *After* cutting, sidewall spacers are “provided only in the longitudinal direction” but not “between the two facing driver transistors.” Ex. 1041 ¶ 26.

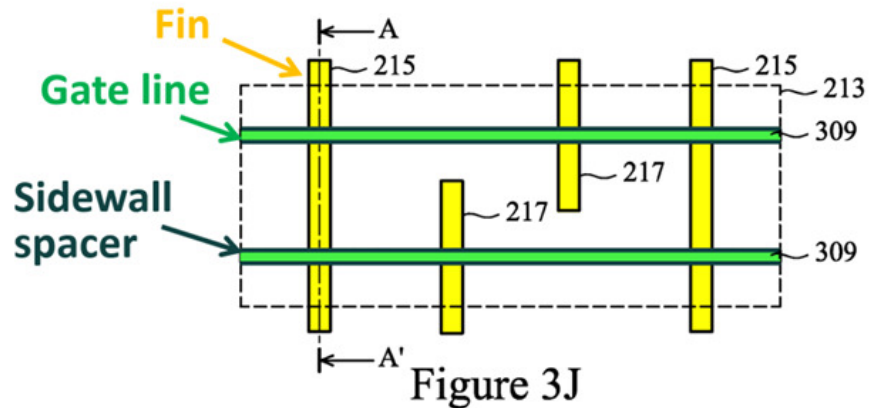
Liaw disclosed the same approach to forming sidewall spacers surrounding the gate line: “The memory device 100 may be completed through the formation of permanent spacers,” which are dielectric. Ex. 1003, 7:25-26. “The spacer layer may comprise SiN, oxynitride, SiC, SiON, oxide, and the like...” *Id.*, 7:31-32. “The permanent spacers are typically formed by blanket depositing a spacer layer (not shown) on the previously formed structure.” *Id.*, 7:29-31. The blanket deposition placed sidewall spacer material on all sides of the gate line. Ex. 1045 ¶¶ 265-266. “The permanent spacers are then patterned, such as by anisotropically etching to remove the spacer layer from the horizontal surfaces of the structure.”

Ex. 1003, 7:35-38. This procedure leaves dielectric sidewall spacer material on all vertical surfaces (or sidewalls) of the gate line, as shown in annotated Figure 3J at

right. Though not

shown in Figure 3J,

5 sidewall spacers have been added in blue for illustration purposes.



The same approach taught in Okuno PCT and Liaw is reflected in the '719 patent: “[A] dielectric spacer layer 1005 is formed to surround the respective gate

10 lines 1004. For example, the dielectric spacer layer 1005 may be formed by depositing on the entire structure one or more layers of dielectric materials, such as SiO₂, Si₃N₄, SiON, and the like, or any combination thereof, and then conducting Reactive Ion Etching (RIE) thereon.” Ex. 1001, 6:11-17. According to the '719 patent, this process produced sidewall spacers “surrounding” gate lines. *Id.*; Ex.

15 1045 ¶¶ 267-268. Similar to Okuno PCT, even though the sidewall spacers surround the gate line, the '719 patent includes figures that do not show the sidewall spacers on the ends of the gate lines “for [the] sake of simplification.” Ex. 1001, 5:5-9, Fig. 8.

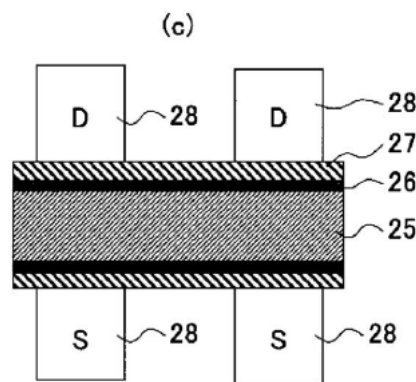
The '719 patent admits that this sidewall spacer formation technique was
20 “conventional” (*id.*, 8:5), which Liaw (see above) and other references confirm.

Ex. 1045 ¶¶ 263-270; Ex. 1006 ¶ 29 (directional (or “anisotropic”) etching technique “such as reactive ion etching (RIE) ... remove[s] portions of the blanket dielectric layer from substantially horizontal surfaces at a faster rate than from substantially vertical surfaces.”); Ex. 1031, 2:55-58, Fig. 1xy; Ex. 1032 ¶ 79, Fig.

5 17. Because sidewall spacers on the long lateral sides and the ends of the gate line are on substantially vertical surfaces, the above well-known etching technique resulted in sidewall spacers surrounding the gate lines. Ex. 1045 ¶ 270.

Patent Owner has previously incorrectly argued that Okuno PCT’s Figure 6(c) below shows that sidewall spacers are implanted within the substrate. As explained by Dr. Thompson, Figure 6(c) is simply an overhead view that shows gate electrodes 25, sidewall spacers 27, and pocket regions 26 in the same plan view for illustrative purposes, but a skilled person would have understood based on the well-known meanings of those terms in combination with Okuno PCT’s process that

10 “sidewall spacers 27” were *above* the substrate and along the sidewalls of the gate line, while pocket regions 26 were implanted within the substrate.



Ex. 1041 ¶ 24; Ex. 1045 ¶ 264.

For the reasons described above, Okuno PCT taught forming sidewall spacers above the substrate surrounding all sides of the gate line. But even without

20

those teachings in Okuno PCT, it would have been obvious to form such sidewall spacers. Ex. 1045 ¶ 273. First, a skilled person would have formed sidewall spacers above the substrate along the sidewalls of the gate lines. Liaw and many other prior art references taught doing so. *Id.* ¶¶ 265-272. The approach was beneficial because, as taught in Liaw, the spacers acted as masks when creating source and drain regions. Ex. 1003, 7:46-47. That widened the physical distance between source and drain regions, preventing shorts between the two. Ex. 1045 ¶ 274. Using sidewall spacers in this way was known and predictable. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (“a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results”).

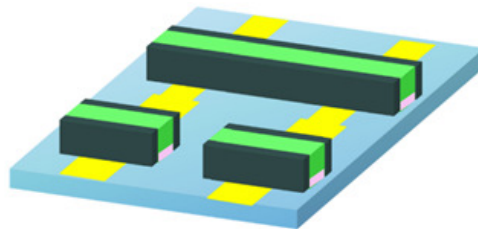
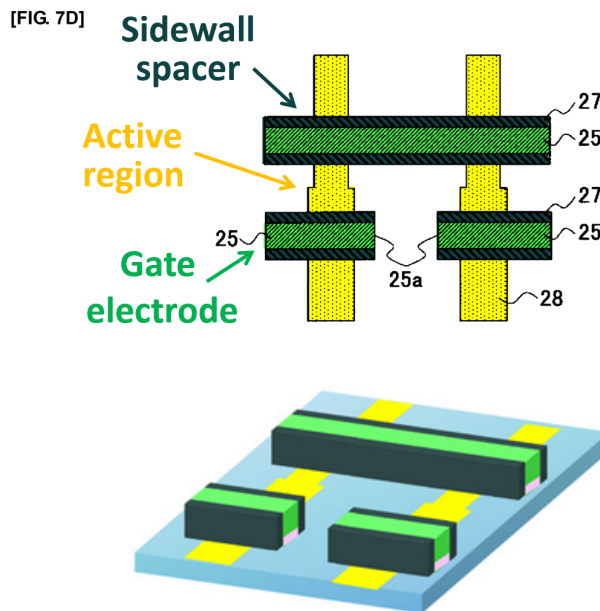
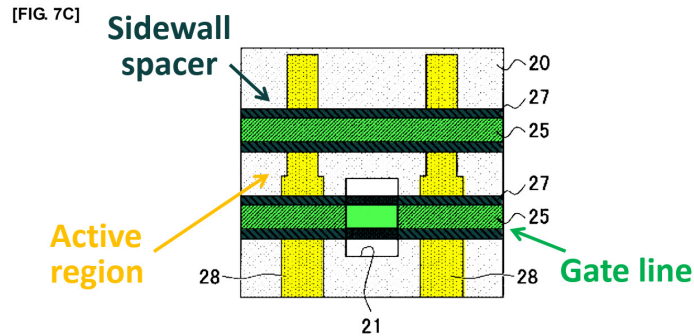
Second, it would have been obvious to form sidewall spacers on all sides of the gate lines. Ex. 1045 ¶ 275. That technique was known in the prior art. *Id.*; Ex. 1031, 2:55-58, Fig. 1xy; Ex. 1032 ¶ 79, Fig. 17. It was standard to form sidewall spacers by using blanket deposition to cover the entire surface area of a substrate and any structures on it and then etching the deposited layer from any horizontal surfaces to leave sidewall spacers on all vertical surfaces, including the ends of the gate lines. Ex. 1045 ¶¶ 87-93, 270; Ex. 1006 ¶ 29; Ex. 1050, 6:55-59, 7:10-14; Ex. 1052 at 221. Okuno PCT and Liaw disclosed these steps. Ex. 1041 ¶¶ 24, 31-32; Ex. 1003, 6:42-46. At minimum, it would have been obvious to perform the two

steps disclosed in Okuno PCT to create sidewall spacers surrounding the gate lines because preventing sidewall formation on the ends of the gate lines would have required additional unnecessary process steps at those ends, which would have been wasteful and departed from common industry practice. Ex. 1045 ¶ 275.

- 5 e. **1[d]: “performing inter-device electrical isolation at a predetermined position after forming the dielectric spacer, wherein isolated portions of the gate line form independent gate electrodes of respective devices”**

As described above, Okuno PCT disclosed forming sidewall spacers before
10 electrical isolation. Ex. 1041 ¶ 24 (forming sidewall spacers while gate line is “still continuous” before being cut). Okuno PCT explained that “the gate electrodes 25 and the sidewalls 27 are cut and separated last.” *Id.* ¶ 25. Okuno PCT disclosed using a gate-separating mask and etching to form separated gate electrodes and explained that the mask/etch process resulted in “gate electrodes 25
15 [that] are electrically insulated by the cut portion 33.” *Id.* ¶¶ 7, 36; Ex. 1045 ¶ 276.

Okuno PCT also taught isolation performed at a predetermined position. Specifically, Okuno PCT taught that the “gate structure [is] cut and separated into predetermined shapes.” Ex. 1041 ¶ 33. The resulting devices are shown in annotated Figures 7C and 7D below (along with the three-dimensional rendering
20 with gate dielectric added in pink). Figure 7C shows mask 20 having predetermined opening 21, where the gate cut portion is exposed and etching is then performed. *Id.* ¶ 32.



Ex. 1045 ¶ 276.

- 5 2. **Claim 2: “The method according to claim 1, wherein the inter-device electrical isolation is performed by cutting off the gate line at the predetermined position”**

As described above regarding claim 1 (at 31-44), a skilled person would have combined Okuno PCT and Liaw and those references render claim 1 obvious.

10 As explained above regarding limitation 1[d] (at 43-44), Okuno PCT disclosed claim 2 (isolation by cutting). Ex. 1045 ¶¶ 283-285.

3. Claim 3: “The method according to claim 2, wherein the method further comprises cutting off the dielectric spacer at the predetermined position”

As described above regarding claim 2 (at 44), a skilled person would have

5 combined Okuno PCT and Liaw and those references render claim 2 obvious.

Okuno PCT further taught claim 3. Okuno PCT disclosed cutting off sidewall spacers at the same time the gate line is cut. Ex. 1041 ¶ 25 (“the gate electrodes 25 and the sidewalls 27 are cut and separated last”). Figure 7D of Okuno PCT above (at 44) depicts sidewall spacers 27 (blue) after they have been cut. Ex. 1045

10 ¶¶ 286-287.

4. Claim 6: “The method according to claim 1, wherein the inter-device electrical isolation is performed after the dielectric spacer is formed and before metal interconnections of the semiconductor device structure are completed”

15

As described above regarding claim 1 (at 31-44), a skilled person would have combined Okuno PCT and Liaw and those references render claim 1 obvious, including performing electrical isolation after forming sidewall spacers. Okuno PCT further disclosed a sequential process in which gate lines are disposed on a semiconductor substrate, sidewall spacers are formed, source/drain regions are formed, and then the gate lines and surrounding sidewall spacers are electrically isolated (cut). Ex. 1041 ¶¶ 26, 31-34. Okuno PCT disclosed performing a silicidation process after cutting a gate line into separate electrodes. *Id.* ¶¶ 34-37.

20

Silicidation was the earliest possible step in forming metal interconnections, which must have been completed after silicidation. Ex. 1045 ¶ 288. Indeed, forming metal interconnections was necessary to create a working device and Okuno PCT did not disclose doing so at any time before silicidation. *Id.* ¶¶ 288-289, 292. Given Okuno
5 PCT's disclosures, a skilled person would have understood that metal interconnections were formed in Okuno PCT's process flow after gate electrical isolation. *Id.* ¶ 288.

In any event, as explained above regarding limitation 1[a] (at 34-35), Okuno PCT and Liaw were obvious to combine. Ex. 1045 ¶¶ 250-259. As part of that
10 combination, a skilled person would have formed metal interconnections (as taught in Liaw) in Okuno PCT's device. Liaw disclosed completing metal interconnections of the semiconductor devices after electrical isolation. Ex. 1003, 8:47-61 ("The drain of the first pull-up transistor 105, the drain of the first pull-down transistor 109, the drain of the first pass-gate transistor 101 and the gate
15 electrodes 311 of the second pull-up transistor 107 and the second pull-down transistor 111 are electrically coupled via an intra-cell connection (not shown) and plugs 329 and 331.... The intra-cell connections may be comprised of copper but optionally may be tungsten (W), an aluminum/copper (Al/Cu) alloy, Al, a refractory metal or metal compound, a metal silicide, combinations thereof, and the

like.”). Adding metal interconnections occurred after the cutting step. *Id.*, 8:5-17 (cutting), 8:47-61 (interconnections); Ex. 1045 ¶¶ 290-291.

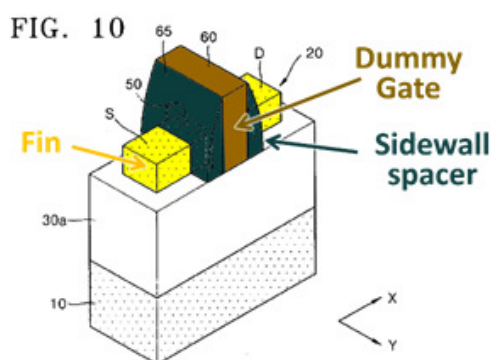
A skilled person would have applied Liaw’s metal interconnection technique to Okuno PCT because metal interconnections were necessary to create a functional circuit and Okuno PCT does not explicitly disclose making interconnections at any point in its processing flow. Ex. 1045 ¶¶ 289-292. It was known in the art to perform metal interconnections after gate electrical isolation. Ex. 1003, 8:5-17, 8:47-61; Ex. 1006 ¶¶ 30-37, 42-43, 46-47; Ex. 1045 ¶¶ 288, 290.

B. Ground 2: Okuno PCT, Liaw, and Kim render claim 7 obvious

Claim 7 recites a conventional replacement gate method where an initial sacrificial gate is removed and a replacement gate is formed in its place. As the '719 patent admits, “[t]hose skilled in the art can devise various ways to implement the replacement process for the gate lines.” Ex. 1001, 8:53-54. Indeed, the '719 patent describes replacement gate processing as known, “conventional” processing. *Id.*, 5:21-28, 8:10-15. Ex. 1045 ¶¶ 193-202, 294.

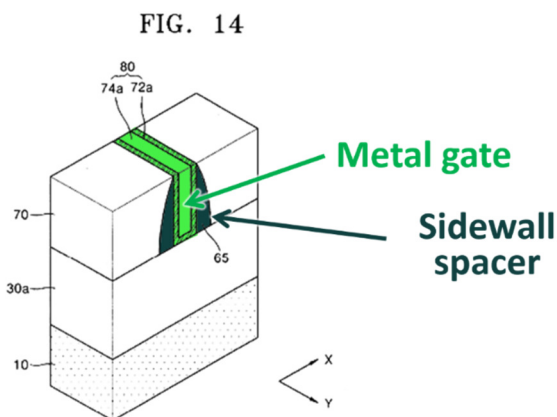
Kim shows that the replacement gate method was conventional: “[T]here is provided a method of fabricating a semiconductor device, including: ... forming a dummy gate electrode on the gate insulating layer; forming a gate spacer on a sidewall of the dummy gate electrode; ... removing the dummy gate electrode; and forming a metal gate electrode in an area in which the dummy gate electrode is

removed.” Ex. 1010 ¶ 11. Other references (including many assigned to
 Petitioner) taught “typical[]” replacement gate processing. *E.g.*, Ex. 1013 ¶¶ 15,
 19, 26, 28 (describing forming a “silicon nitride dummy gate structure” and
 “spacers,” noting “a wet etch is used to remove the dummy nitride gate 25, leaving
 5 the opening 45,” and explaining that “a gate electrode (metal) layer 52 is formed”
 in the opening 45); Ex. 1015, 18:23-24 (describing replacement gate processing in
 great detail, including forming a sacrificial gate electrode), 21:5-7 (forming
 sidewall spacers), 23:61-62 (removing the sacrificial gate electrode), 26:14-18
 (forming the replacement gate electrode); Ex. 1045 ¶ 295. As described above (at
 10 23-24), Kim taught forming dummy gate 60 (brown) and adding a gate sidewall
 spacer 65 (blue), as shown in annotated Figure 10 below. Ex. 1010 ¶¶ 37-38.



After forming sidewall spacers, Kim disclosed that dummy gate 60 is removed and
 replacement gate 80 (green) is added in its place, as shown in annotated Figure 14
 15 below. *Id.* ¶¶ 41-42 (“A metal layer 74 is formed of a W layer on the barrier layer
 72 so as to completely bury the area in which the dummy gate electrode 60 is

removed.... As shown in FIG. 14, the barrier layer 72 and the metal layer 74 are planarized using CMP to complete the metal gate electrode 80.”); Ex. 1045 ¶ 296.



As described above (at 31-44), Okuno PCT in combination with Liaw

renders claim 1 obvious, including isolating gate lines after forming sidewall spacers. *See* Ex. 1003, 8:10-17, Fig. 3K; Ex. 1041 ¶¶ 26-27, 34-36, Figs. 7C, 7D.

Performing sidewall spacer formation and gate isolation in that order was well

known. Ex. 1006 ¶¶ 33, 35; Ex. 1008 ¶¶ 38, 40, Fig. 9A; Ex. 1045 ¶¶ 281, 298. A skilled person would have understood Kim to teach isolation of gate electrodes following formation of replacement gates, as well as formation of sidewall spacers.

Indeed, the only way to create a useful semiconductor device would have been to isolate the gates into separate transistors. Ex. 1045 ¶ 297.

Although Kim did not disclose performing isolation before gate replacement (and it was known in the art to perform isolation after gate replacement), a skilled person would have known that isolation could be done before or after gate replacement. Ex. 1045 ¶ 299. As the '719 patent itself teaches, a skilled person would have faced two predictable options: performing electrical isolation before or after forming replacement gates. Ex. 1001, 8:66-9:8, 10:1-3; Ex. 1045 ¶¶ 186,

299. Each outcome was known, predictable, and taught by Cheng '175. Ex. 1045 ¶ 157; Ex. 1011, 4:42-47. Thus, by combining Kim with Okuno PCT and Liaw, it would have been obvious to isolate gate electrodes after forming replacement gates. Ex. 1045 ¶¶ 295-299.

5 A skilled person would have been motivated to combine Liaw and Kim. Both references relate to FinFET fabrication and, like Liaw, Kim taught the FinFET structures required by claim 1—fins, gate lines, gate dielectric layers, and dielectric spacers. *E.g.*, Ex. 1010, Abstract, ¶¶ 10-11, claims 1, 4; Ex. 1003, 7:25-38, Figs. 3I-3J. A skilled person would also have been motivated to combine
10 Okuno PCT, Liaw, and Kim because all methods disclosed in those references can be used for fabricating SRAM memory. Ex. 1041 ¶¶ 28-29; Ex. 1003, 1:5-8; Ex. 1010 ¶ 58 (“[a] pull-up p-channel FinFET and a pull-down n-channel FinFET of a 122M-SRAM were fabricated using the present invention.”); Ex. 1045 ¶ 300.

 Moreover, a skilled person would have been motivated to use Kim’s
15 replacement gate technique in Okuno PCT’s and Liaw’s processing method. As described above (at 16-17), replacement gate processing would have facilitated reductions in scale by allowing the use of high-k dielectric material to reduce transistor size. Ex. 1045 ¶¶ 226-228, 301; Ex. 1020, 1:20-34. That would have accomplished the objective of Okuno PCT in “miniaturization of a MOS type
20 semiconductor device.” Ex. 1041 ¶ 1; Ex. 1045 ¶¶ 224-227, 232, 303. That also

would have accomplished the objective of Liaw to “maintain the scaling that [would] be required for further reductions of FinFETs.” Ex. 1003, 1:35-37; Ex. 1045 ¶¶ 232, 303. In addition, incorporating Kim’s replacement gate process into Okuno PCT’s and Liaw’s process flow would have increased transistor speed by improving electrical performance (through preventing charge carrier depletion and facilitating the implementation of high-k dielectrics to reduce the electrical thickness of the gate dielectric) and enhancing the effects of channel strain to increase drive currents. Ex. 1045 ¶¶ 228, 230-231, 301; Ex. 1015, 2:18-33; Ex. 1023 ¶¶ 3, 36. It was known in the prior art to combine the benefits of FinFETs, high-k dielectrics, metal replacement gates, and channel strain. Ex. 1045 ¶¶ 233, 303.

C. Ground 3: Okuno PCT and Chang render claims 1-3 and 6 obvious

As discussed above, the '719 patent identifies its alleged novelty as isolating portions of gate lines after forming sidewall spacers around them. Okuno PCT taught that step. And the combination of Okuno PCT and Chang disclosed the other conventional limitations claimed in the '719 patent, rendering claims 1-3 and 6 obvious. Ex. 1045 ¶¶ 304-326.

A skilled person would have been motivated to combine the teachings of Okuno PCT and Chang with a reasonable expectation of success because both relate to semiconductor device fabrication of SRAMs and shared the objective of

making circuits smaller. Ex. 1045 ¶¶ 234-236. Okuno PCT disclosed “a method of realizing further miniaturization.” Ex. 1041 ¶ 24. Chang similarly recognized that “scaling is critical to fabricating advanced integrated circuits” and proposed a method to “facilitate using tighter design rules for smaller [semiconductor] layout areas.” Ex. 1004, 6:19, 6:49-52.

Given the importance of reducing circuit size, a skilled person would have used techniques disclosed in Chang to further Okuno PCT’s objective. As described below, doing so would have improved Okuno PCT by further reducing circuit size. Ex. 1045 ¶¶ 236-237, 307. In addition, adding fins to Okuno PCT’s design would have reduced current leakage and voltage variability, as was well known in the art. Ex. 1003, 1:17-23; Ex. 1028, 5:35-37; Ex. 1045 ¶¶ 236, 308.

1. Claim 1

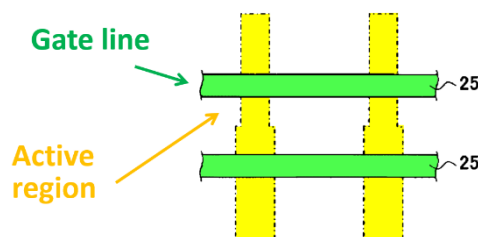
a. Preamble: “A method for manufacturing a semiconductor device structure, comprising”

Okuno PCT disclosed a method of manufacturing semiconductor devices. Ex. 1041 ¶ 1; Ex. 1045 ¶ 305.

b. 1[a]: “forming a fin in a first direction on a semiconductor substrate”

Okuno PCT disclosed forming active regions (yellow) on a semiconductor substrate, as shown in annotated Figure 7A at right. Ex. 1041 ¶ 29.

[FIG. 7A]



To save space and increase transistor density, it would have been obvious to replace Okuno PCT's planar active regions with fin-shaped active regions.

The '719 patent recognized that fins were known in the prior art. Ex. 1001, 1:27-

5 31. Indeed, as explained above (at 17-18), fins were widely taught in the prior art.

For example, Chang taught using fin-shaped active regions. In some embodiments, "the substrate surface would not be planar" and "subsequently patterned gate electrodes would wrap around the top and sidewalls of the diffusion regions, thereby forming tri-gates or similar structures." Ex. 1004, 3:27-30. A

10 "tri-gate" FET is a type of FinFET that includes channels on three surfaces of the fin instead of just two surfaces. Ex. 1001, 1:45-54, 3:65-4:9; Ex. 1045 ¶ 306.

Although Chang disclosed other embodiments with "isolation regions" for making the substrate more planar when desired, Chang taught that "[t]he presence of isolation region 314 is not a requirement of embodiments of the present invention."

15 Ex. 1004, 3:17-19.

A skilled artisan would have been motivated to include fins (as taught in Chang) in Okuno PCT's circuit structures to accomplish Okuno PCT's objective to

reduce circuit size. Ex. 1041 ¶ 24; Ex. 1045 ¶¶ 236-237, 307. A skilled person also would have incorporated fins into Okuno PCT's design to obtain other known FinFET benefits. Ex. 1045 ¶¶ 236, 308. Not only were FinFETs smaller than transistors with planar active regions, they also improved performance. Ex. 1003, 1:17-23; *see also* Ex. 1028, 5:35-37.

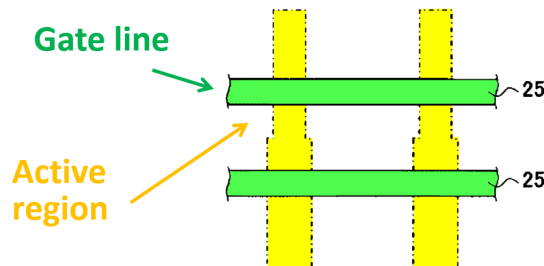
Chang also acknowledged the crossover between planar and FinFET semiconductor fabrication techniques. Ex. 1004, 3:25-30. The '719 Patent acknowledged that a benefit of FinFET fabrication is its "compatibility with the conventional manufactur[ing] processes." Ex. 1001, 1:27-31. In a prior art patent, Patent Owner similarly acknowledged that skilled artisans knew the same semiconductor fabrication techniques applied to planar and fin-based designs. Ex. 1012, 11:53-60. A skilled person would have replaced Okuno PCT's planar active regions with fin-shaped active regions because "[t]hose two types of devices differ from each other just in that active regions are arranged differently and thus gates on the active regions are arranged differently." *Id.*; Ex. 1045 ¶¶ 238, 308.

The evidence in the prior art that fin-shaped active regions substituted for planar active regions supports that a skilled person would have had a reasonable expectation of success in combining Okuno PCT with Chang as described above. Ex. 1045 ¶¶ 207-213, 238.

- c. **1[b]: “forming a gate line in a second direction, the second direction crossing the first direction on the semiconductor substrate, and the gate line intersecting the fin with a gate dielectric layer sandwiched between the gate line and the fin”**

Okuno PCT disclosed forming multiple gate lines 25 (green) over active regions as shown in annotated Figure 7A below. Ex. 1041 ¶ 30. Okuno PCT further disclosed forming a dielectric gate oxide layer (not shown) sandwiched between the active regions and the gate lines. *Id.* ¶ 29; Ex. 1045 ¶ 310. As explained above (at 53-54), it would have been obvious to substitute Chang’s fin-shaped active regions for Okuno PCT’s planar active regions. Ex. 1045 ¶¶ 234-238.

[FIG. 7A]



Like Okuno PCT, Chang disclosed forming gate lines (green) intersecting with active regions configured as fins in some embodiments (yellow), as shown in annotated Figure 6A below. Ex. 1004, 2:29-34, Fig. 4 (describing and depicting “a grid of continuous parallel gate electrode structures overlying a grid of continuous parallel diffusion regions”).

obvious. As explained above regarding limitation 1[d] (at 44-45), Okuno PCT disclosed claim 2 (isolation by cutting). Ex. 1045 ¶ 319.

5 **3. Claim 3: “The method according to claim 2, wherein the method further comprises cutting off the dielectric spacer at the predetermined position”**

As described above regarding claim 2 (at 56-57), a skilled person would have combined Okuno PCT and Chang and those references render claim 2 obvious. Okuno PCT further taught claim 3. Okuno PCT disclosed cutting off sidewall spacers at the same time the gate line is cut. Ex. 1041 ¶ 25. Figure 7D of
10 Okuno PCT above (at 44) depicts sidewall spacers 27 (blue) after they have been cut. Ex. 1045 ¶ 320.

15 **4. Claim 6: “The method according to claim 1, wherein the inter-device electrical isolation is performed after the dielectric spacer is formed and before metal interconnections of the semiconductor device structure are completed”**

As described above regarding claim 1 (at 51-56), a skilled person would have combined Okuno PCT and Chang and those references render claim 1 obvious, including performing electrical isolation after forming sidewall spacers.

20 As further described above in Ground 1 (at 45-46), given Okuno PCT’s disclosures, a skilled person would have understood that metal interconnections were formed in Okuno PCT’s process flow after gate electrical isolation. Ex. 1045 ¶ 321.

In any event, as described above (at 53-54), a skilled person would have combined Okuno PCT and Chang. As part of that combination, a skilled person would have formed metal interconnections (as taught in Chang) in Okuno PCT's device. Chang taught electrical isolation before forming and completing metal interconnections (i.e., before contact formation). Ex. 1004, 2:55-56 ("Source/drain and gate electrode contacts can be formed either before or after interconnecting regions are removed."). A skilled person would have applied Chang's metal interconnection technique to Okuno PCT because metal interconnections were necessary to create a functional circuit and Okuno PCT does not explicitly disclose making interconnections at any point in its processing flow. Ex. 1045 ¶¶ 322-325. It was known in the art to perform metal interconnections after gate electrical isolation. Ex. 1003, 8:5-17, 8:47-61; Ex. 1006 ¶¶ 30-37, 42-43, 46-47; Ex. 1045 ¶ 326.

D. Ground 4: Okuno PCT, Chang, and Kim render claim 7 obvious

- 1. Claim 7: "The method according to claim 1, wherein after the dielectric spacer is formed and before the inter-device electrical isolation is performed, the method further comprises: removing the gate line to form an opening inside the dielectric spacer; and forming a replacement gate line in the opening."**

Claim 7 recites a conventional replacement gate method where an initial gate line is removed and a replacement gate line is formed in its place. As the '719 patent admits, "[t]hose skilled in the art can devise various ways to implement the

replacement process for the gate lines.” Ex. 1001, 8:53-54. Indeed, the '719 patent describes replacement gate processing as already known and part of “conventional” processing. *Id.*, 5:21-28, 8:10-15. Ex. 1045 ¶ 328.

As described above in Ground 2 (at 47-48), Kim and other references demonstrate that the replacement gate method was conventional. Ex. 1010 ¶ 11; Ex. 1013 ¶¶ 15, 19, 26, 28; Ex. 1015, 17:62-19:51, 21:5-7, 23:61-62, 26:14-18; Ex. 1045 ¶ 329. As further described above in Ground 2 (at 47-49), Kim taught forming a dummy gate, adding gate sidewall spacers, and replacing the dummy gate with a replacement gate. Ex. 1010 ¶¶ 37-38, 41-42; Ex. 1045 ¶ 330.

As described above (at 51-56), Okuno PCT and Chang render claim 1 obvious, including isolating gate lines after sidewall spacer formation. *See* Ex. 1041 ¶¶ 26-27, 34-36, Figs. 7C, 7D. As described above in Ground 2 (at 49-50), a skilled person would have known that isolation could be done before or after gate replacement. Ex. 1045 ¶ 332. As the '719 patent itself teaches, a skilled person would have faced two predictable options: performing electrical isolation before or after forming replacement gates. Ex. 1001, 8:66-9:8, 10:1-3. Each outcome was known, predictable, and taught by Cheng '175. Ex. 1045 ¶¶ 332-333; Ex. 1011, 4:42-47. By combining Kim with Okuno PCT and Chang, it would have been obvious to isolate gate electrodes after forming replacement gates. Ex. 1045 ¶ 333.

A skilled person would have been motivated to combine Okuno PCT, Chang and Kim. Ex. 1045 ¶¶ 239-242, 334-337. Like Chang, Kim taught the FinFET structures recited in claim 1—fins, gate lines, gate dielectric layers, and sidewall spacers. *E.g.*, Ex. 1010, Abstract, ¶¶ 10-11, claims 1, 4. As described above (at 5 53-54), it would have been obvious to use fins in Okuno PCT's design to save space. And like Okuno PCT and Chang, Kim disclosed a method to fabricate SRAM cells. Ex. 1041 ¶¶ 28, 40; Ex. 1010 ¶ 58; Ex. 1045 ¶ 334.

In addition, a skilled person would have been motivated to use Kim's replacement gate technique with Okuno PCT's and Chang's fabrication method.

10 As described above (at 16-17), replacement gate processing would have allowed using high-k dielectric material to reduce transistor size. Ex. 1045 ¶¶ 241, 335; Ex. 1020, 1:20-34; Ex. 1021, 247. That would have furthered Okuno PCT's objective to "further miniaturization." Ex. 1041 ¶ 24; Ex. 1045 ¶¶ 242, 337. Moreover, incorporating Kim's replacement gate process into the combined Okuno PCT and 15 Chang process flow would have increased transistor speed by improving electrical performance (preventing charge carrier depletion and facilitating reduction of gate dielectric electrical thickness) and enhancing channel strain effects to increase drive currents. Ex. 1045 ¶¶ 241, 335; Ex. 1015, 2:18-33; Ex. 1023 ¶¶ 3, 36. It was known in the art to combine the benefits of FinFETs, high-k dielectrics, metal 20 replacement gates, and channel strain. Ex. 1045 ¶ 337.

VIII. Conclusion

Petitioner has shown a reasonable likelihood of prevailing in its challenge of claims 1-3 and 6-7 of the '719 patent and requests cancellation of those claims.

Dated: March 19, 2019

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CERTIFICATION OF WORD COUNT UNDER 37 C.F.R. § 42.24(d)

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,070,719 B2 CLAIMS 1-3, 6-7 totals 11,499 words, excluding the cover page, signature block, and parts exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,070,719 B2 CLAIMS 1-3, 6-7 and supporting materials (Exhibits 1001-1061 and Power of Attorney) have been served in their entirety this 19th day of March, 2019, by FedEx® mail delivery service on Patent Owner via its attorneys of record:

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