

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REC Solar Pte. Ltd. and JinkoSolar (U.S.) Inc.

Petitioners

v.

Hanwha Q CELLS & Advanced Materials Corporation

Patent Owner

Patent No. 9,893,215

Filing Date: November 6, 2008

Issue Date: February 13, 2018

Title: METHOD FOR MANUFACTURING A SOLAR CELL WITH A
SURFACE-PASSIVATING DIELECTRIC DOUBLE LAYER, AND
CORRESPONDING SOLAR CELL

Case No. IPR2019-01145

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

I.	PRELIMINARY STATEMENT	1
II.	THE '215 PATENT	4
A.	Overview of the '215 Patent.....	4
B.	Prosecution History of the '215 Patent	6
III.	LEVEL OF ORDINARY SKILL IN THE ART	7
IV.	CLAIM CONSTRUCTION.....	8
A.	“A solar cell” (Claim 12, preamble)	8
V.	CLAIMS 12-14 OF THE '215 PATENT ARE UNPATENTABLE.....	10
A.	Overview of the Prior Art.....	10
1.	<i>Agostinelli</i> '086	10
2.	<i>Nakano</i>	12
3.	<i>Hoex 2006</i>	14
4.	<i>Narwankar</i>	15
5.	<i>Tan</i>	16
B.	Ground 1: <i>Agostinelli</i> '086 Anticipates Claims 12-14 Under 35 U.S.C. § 102	17
1.	Claim 12	18
2.	Claim 13	27
3.	Claim 14	27
C.	Ground 2: Claims 12-14 Are Obvious Over <i>Agostinelli</i> '086 in View of <i>Nakano</i> and <i>Hoex 2006</i> Under 35 U.S.C. § 103	28
1.	Claim 12	29

2.	Claim 13	36
3.	Claim 14	36
D.	Ground 3: Claims 12-14 Are Obvious Over <i>Nakano</i> in View of <i>Hoex</i> 2006 and the Knowledge of a POSITA Under 35 U.S.C. § 103	37
1.	Claim 12	37
2.	Claim 13	45
3.	Claim 14	46
E.	Ground 4: <i>Narwankar</i> Anticipates Claims 12-14 Under 35 U.S.C. § 102	46
1.	Claim 12	46
2.	Claim 13	57
3.	Claim 14	58
F.	Ground 5: Claims 12-14 Are Obvious Over <i>Narwankar</i> alone or in view of <i>Tan</i>	59
1.	Claim 12	59
2.	Claim 13	66
3.	Claim 14	66
VI.	MANDATORY NOTICES	66
A.	Real Party-in-Interest	66
B.	Related Matters	67
C.	Lead and Back-Up Counsel and Service Information	67
VII.	CERTIFICATION UNDER 37 C.F.R. § 42.24(d)	68
VIII.	GROUNDS FOR STANDING	68

IX.	STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED	69
X.	CONCLUSION	69

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 9,893,215 to Jan Schmidt et al.
Ex. 1002	File History of U.S. Patent No. 9,893,215
Ex. 1003	Declaration of Dr. Bruce Clemens
Ex. 1004	Curriculum Vitae of Dr. Bruce Clemens
Ex. 1005	EP Patent Application No. 1,763,086 A1 to Agostinelli et al.
Ex. 1006	U.S. Patent No. 4,463,216 A to Nakano et al.
Ex. 1007	Hoex, B., et al. "Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited Al ₂ O ₃ ." <i>Applied Physics Letters</i> 89.4 (2006): 042112
Ex. 1008	U.S. Patent Publication No. 2005/0260347 A1 to Narwankar et al.
Ex. 1009	Gray, J. L., "The Physics of the Solar Cell," <i>Handbook of Photovoltaic Science and Engineering</i> (2003)
Ex. 1010	Lauinger, T., et al. "Record low surface recombination velocities on 1 Ω cm <i>p</i> -silicon using remote plasma silicon nitride passivation." <i>Applied Physics Letters</i> 68.9 (1996): 1232
Ex. 1011	Nicollian, E.H., "Surface Passivation of Semiconductors," <i>Journal of Vacuum Science and Technology</i> 8.5 (1971): S39
Ex. 1012	Hoex, B., et al., "Industrial High-rate (~5 nm/s) Deposited Silicon Nitride Yielding High-quality Bulk and Surface Passivation under Optimum Anti-reflection Coating Conditions," <i>Progress in Photovoltaics: Research and Applications</i> 13 (2005): 705
Ex. 1013	Hezel, R. "Silicon Nitride for the Improvement of Silicon Inversion Layer Solar Cells," <i>Solid-State Electronics</i> 24.9 (1981): 863
Ex. 1014	File History of U.S. Patent No. 9,548,405
Ex. 1015	Agostinelli, G., "Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge." <i>Solar Energy Materials & Solar Cells</i> (2006), 90, 3438-3443.
Ex. 1016	U.S. Patent No. 3,585,072
Ex. 1017	U.S. Patent No. 7,755,164
Ex. 1018	U.S. Patent No. 5,837,593
Ex. 1019	Schmidt, J. et al., "Record low surface recombination velocities on low-resistivity silicon solar cell substrates." Conference

	Record of the IEEE Photovoltaic Specialists Conference (1996), 25 th , 413-416.
Ex. 1020	Schmidt, J. et al., “Accurate method for the determination of bulk minority-carrier lifetimes of mono- and multicrystalline silicon wafers.” Journal of Applied Physics (1997), 81(9), 6186-6199.
Ex. 1021	Yang, Y., “Hydrogen Passivation Induced Dispersion of Multi-Walled Carbon Nanotubes.” Advanced Materials (2012), 24(7), 881-885.
Ex. 1022	Lim, S., “Carbon quantum dots and their applications.” Chemical Society Reviews (2015), 44(1), 362-381.
Ex. 1023	Hoex, B., et al., “Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al ₂ O ₃ .” Applied Physics Letters (2007), 91(11), 112107-1.
Ex. 1024	Heil, S., et al., “ <i>In situ</i> reaction mechanism studies of plasma-assisted atomic layer deposition of Al ₂ O ₃ .” Applied Physics Letters (2006), 89(3), 131505/1-131505/3.
Ex. 1025	Schmidt, J. “Carrier recombination at silicon-silicon nitride interfaces fabricated by plasma-enhanced chemical vapor deposition.” Journal of Applied Physics (1999), 85(7), 3626-3633.
Ex. 1026	Hezel, R. “Recent progress in MIS solar cells.” Progress in Photovoltaics (1997), 5(2), 109-120.
Ex. 1027	Declaration of Emily Florio
Ex. 1028	Shin, D., et al., “Effect of plasma and heat treatment on silicon dioxide films by plasma-enhanced atomic layer deposition.” Journal of Vacuum Science & Technology A (2019), 37, 020902.
Ex. 1029	Jin, H., et al., “Characterization of the Si-SiO ₂ Interface Following Room Temperature Ammonia Plasma Exposure.” Journal of the Electrochemical Society, (2007) 154 (6) H417-H421.
Ex. 1030	U.S. Patent No. 6,929,700 to Tan et al.
Ex. 1031	[Reserved]
Ex. 1032	U.S. Patent No. 6,930,052 B2 to Schwarzl et al.
Ex. 1033	Fujiwara, H., et al. “Application of Hydrogenated Amorphous Silicon Oxide Layers to c-Si Heterojunction Solar Cells.” Applied Physics Letters, (2007) 91 (13), 133508.
Ex. 1034	U.S. Patent No. 7,163,860 to Kamal et al.

Ex. 1035	U.S. Patent No. 6,933,245 to Lee et al.
Ex. 1036	Cho, Y., et al. “Effect of Hydrogen Content in Intrinsic a-Si:H on Performances of Heterojunction Solar Cells.” International Journal of Photoenergy (2013) 1–6.
Ex. 1037	Groner, M., et al. “Electrical Characterization of Thin Al ₂ O ₃ Films Grown by Atomic Layer Deposition on Silicon and Various Metal Substrates.” Thin Solid Films, (2002) 413(1-2), 186–197.
Ex. 1038	Baumvol, I. J. R. “Thermal Nitridation of SiO[Sub 2] Films in Ammonia: The Role of Hydrogen.” Journal of The Electrochemical Society, vol. 143, no. 4, 1996, p. 1426.
Ex. 1039-1042	[Reserved]
Ex. 1043	“Reference Table 0.2 Wavelength Conversions.” The Concise Handbook of Analytical Spectroscopy: Theory, Applications, and Reference Materials, by Jerry Workman, World Scientific, 2016, p. xiv.
Ex. 1044	Hoex, B., et al. “High-Rate Plasma-Deposited SiO ₂ Films for Surface Passivation of Crystalline Silicon.” Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 24, no. 5, 2006, pp. 1823–1830

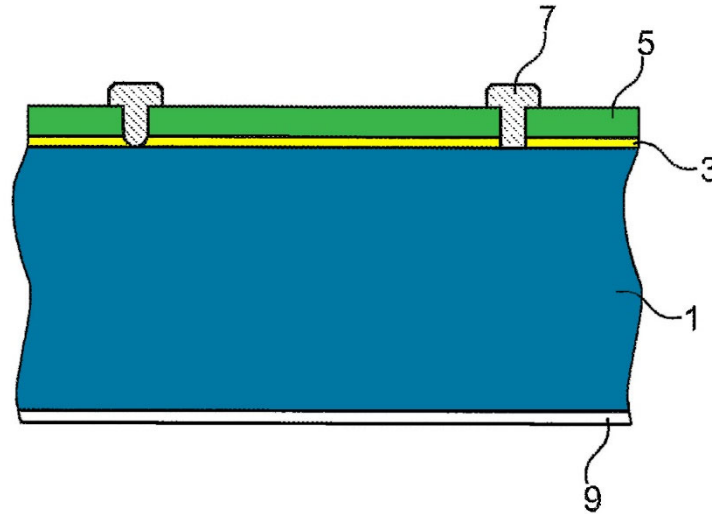
Petitioners request *inter partes* review and cancelation of claims 12-14 (“Challenged Claims”) of U.S. Patent No. 9,893,215 (“the ’215 patent”) (Ex. 1001), purportedly currently assigned to Hanwha Q CELLS & Advanced Materials Corporation (“Hanwha”).

I. PRELIMINARY STATEMENT

The ’215 patent relates to methods of manufacturing solar cells and the resulting structure. Ex. 1001, Abstract. Specifically, the ’215 patent seeks to improve the efficiency of traditional solar cells by combining known manufacturing techniques to form dielectric layers known to passivate solar cells by suppressing surface recombination losses. The Challenged Claims recite a cell structure comprising a three-layer stack of certain materials, which the inventors claim provides enhanced efficiency compared to previous cell structures.

Claim 12 of the ’215 patent, the only independent claim challenged, recites a cell structure comprising a silicon substrate **1** and two dielectric layers **3** and **5**. Ex. 1001, 9:34-10:9. The first dielectric layer **3**, which is on a surface of the silicon substrate **1**, comprises aluminium oxide and is less than 50 nm thick. *Id.*, 10:1-2, 7-9. This first dielectric layer **3** lies between the surface of the substrate **1** and the second dielectric layer **5**, which is made of a different material and contains embedded hydrogen. *Id.*, 10:3-6. While the specification addresses passivation, the

claim does not limit the functionality of the dielectric layers. The claimed three-layer structure is shown in annotated Fig. 1 below.



Ex. 1001, Fig. 1 (silicon substrate **1** (blue); first dielectric layer comprising aluminium oxide **3** (yellow); second dielectric layer with embedded hydrogen **5** (green))

This same layer structure was already known in the art and/or was obvious to a person of ordinary skill in the art (“POSITA”) at the time of the claimed invention based on the prior art presented herein. Accordingly, for the reasons discussed below, the Board should institute *inter partes* review and cancel claims 12-14.

These same claims are also being challenged in a petition recently filed by LONGi. See *LONGi Green Energy Tech. Co., Ltd. et al v. Hanwha Q CELLS & Advanced Materials Corp.*, IPR2019-01072 (P.T.A.B. 2019). The Petitioners here, like LONGi, are respondents in an ITC investigation filed by Hanwha. The present

petition is materially different from the LONGi petition, relying on different prior art and argumentation. Specifically, LONGi's petition asserts obviousness over combinations of: U.S. Patent Application Publication No. 2006/0102972 A1, U.S. Patent Application Publication No. 2004/0112426, Bram Hoex, et. al. "Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited Al_2O_3 " *Applied Physics Letters* 89.4 (2006): 042112 ("Hoex 2006"), and F. Duerinckx and J. Szlufcik, "Defect passivation of industrial multicrystalline solar cells based on PECVD silicon nitride," *Solar energy materials and solar cells* 72.1-4 (2002): 231-246. In contrast, the present petition relies on different primary references (*Agonstinelli '086*, *Nakano*, and *Narwankar*) and shares only one secondary reference, *Hoex 2006*. Furthermore, this petition is being filed by different parties and relies on the testimony of a different expert.

Thus, because the petitions are not redundant and because Hanwha sued multiple parties in the ITC and therefore should not be surprised by multiple IPR petitions, the Board should institute review here even if it also institutes review of the LONGi petition. *See Samsung Elecs. Amer., Inc. v. Uniloc Luxembourg S.A.*, Case IPR2017-01797, slip op. 33–34 (PTAB Feb. 6, 2018) (Paper 8).

II. THE '215 PATENT

A. Overview of the '215 Patent

The '215 patent issued from a PCT application filed on Nov. 6, 2008, claiming priority to a German application filed on November 14, 2007.¹ Ex. 1002, 1020. The '215 patent is generally directed to a “solar cell with a dielectric double layer” and “a method of the manufacture thereof.” Ex. 1001, Abstract.

Solar radiation creates electricity in a solar cell by facilitating the flow of electrons in silicon. Ex. 1003, Declaration of Dr. Bruce Clemens, ¶¶ 15-20; Ex. 1010, p. 61; *see also* Ex. 1004; Ex. 1011; Exs. 1019-1022. Photons hit the surface of the solar cell, freeing electrons from the atoms on its surface. *Id.* As explained in the '215 patent:

A key requirement for achieving high degrees of efficiency in solar cells is very effective suppression of surface recombination losses. For this purpose, the surface of solar cells should be passivated as effectively as possible, so that charge carrier pairs which are generated inside the solar cell by incident light and which diffuse to the surfaces of the solar cell substrates do not recombine at the solar cell surface, so that they would no longer be available to help improve the efficiency of the solar cell.

¹ Accordingly, assessment of patentability is based on pre-AIA 35 U.S.C. § 102.

Ex. 1001, 1:14-22. Known techniques for surface passivation using silicon nitride or silicon carbide layers are also referenced in the Background, as is the use of aluminium oxide layers deposited by atomic layer deposition (“ALD”) for good passivating results. Ex. 1001, 2:19-22.

The ’215 patent describes a “dielectric passivating layer . . . composed of two partial layers, of a very thin aluminium oxide-containing layer, which is formed by atomic layer deposition (ALD), and also of a thicker layer made of silicon oxide, silicon nitride or silicon carbide, for example, which can be deposited on the aluminium oxide layer by means of plasma enhanced chemical vapour deposition (PECVD), for example.” Ex. 1001, 2:61-67. The exemplary techniques used to deposit these two layers (e.g., ALD and PECVD) were well known and are not recited in claims 12-14, which are directed solely to structural elements, *not* manufacturing methods.

The patent further explains that two surface-passivating dielectric layers are allegedly an improvement over prior-art passivation layers. *Id.*, 3:21-30; *see also id.*, 5:19-22 (“The embedded hydrogen can diffuse at least in part through the first dielectric layer positioned there below and contribute to passivation there by saturating free bonds of the silicon (‘dangling bonds’).”).

B. Prosecution History of the '215 Patent

Much of the debate during prosecution focused on the achievable thinness of the dielectric layers using different manufacturing methods. *See, e.g.*, Ex. 1002, 89, 137, 216, 396 591, 660, and 756. During these exchanges, the Examiner relied in part on a PCT application by Agostinelli, WO 2006/097303 A1 (“*Agostinelli* ’303”). Ex. 1002, 459-487, 673. In contrast, European Patent Application No. EP 1,763,086 A1 to Agostinelli (“*Agostinelli* ’086”), although disclosed to the Examiner, was not specifically addressed or discussed by the Examiner. *Id.*, 267, 283. *Agostinelli* ’086 (relied upon herein by Petitioners for Grounds 1 and 2) has a materially different disclosure than *Agostinelli* ’303. *See* Section V.A.1., *infra*.

On February 12, 2015, one of the ’215 patent’s inventors, Dr. Jan Schmidt, submitted a declaration on objective indicia of non-obviousness in an effort to overcome *Agostinelli* ’303. Ex. 1002, 390-400, 498. In it, Dr. Schmidt argued that the Examiner’s rejections ignored that the invention (1) satisfied a long-felt need, (2) overcame the skepticism of experts, (3) provided unexpected results, (4) had significant commercial success, and (5) had been copied by others. *Id.*, 357-359. The Examiner found each of these arguments unpersuasive.² *Id.*, 357-359.

² Petitioners agree with the Examiner’s assessment. *See* Ex. 1003, Section XVII.

Following a final rejection, the Applicant appealed. *Id.*, 117. During the appeal, the Examiner offered amendments to the claims and received authorization for the amendments *Id.*, 60-63. In the Reasons for Allowance, the Examiner stated that the application was allowable in his view because, while the prior art including *Agostinelli* '303 taught or rendered obvious every other element of the claims, it “fails to explicitly teach a combination of all the claimed features including ‘depositing a second dielectric layer directly on a surface of the first dielectric layer, materials of the first dielectric layer and the second dielectric layer differing and hydrogen being embedded into the second dielectric layer,’ as claimed.” *Id.*, 63-64. As noted above, however, the Examiner provided no analysis regarding *Agostinelli* '086, which differs from *Agostinelli* '303 in disclosing these additional features, as well as features previously argued by the Applicant as missing from *Agostinelli* '303. Also, the Examiner did not have *Nakano* or *Narwankar* before him, which are relied upon herein for Grounds 2-5.

III. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '215 patent (i.e., semiconductor devices) would have been someone with an advanced degree involving the disciplines of electrical engineering, applied physics, chemistry, or materials science, or the like, and at least two years of experience designing, developing, or researching in the field. Ex. 1003, ¶¶ 12-14. Alternatively, that person would have had a bachelor's degree in involving

the disciplines of electrical engineering, applied physics, chemistry, or materials science, or the like, and at least three years designing, developing, or researching in the field. *Id.*

IV. CLAIM CONSTRUCTION

The following terms from the Challenged Claims of the '215 patent require construction for this proceeding. For the purposes of this Petition, no explicit construction is needed for any claim term not addressed below. Any claim term not addressed below should be given its ordinary and accustomed meaning as understood by one of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*).

A. “A solar cell” (Claim 12, preamble)

The preamble of claim 12, which recites a “solar cell,” is not limiting. The determination of whether a preamble limits a claim is made on a case-by-case basis. *Catalina Mktg. Int’l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). The Federal Circuit has instructed that “a preamble is not limiting ‘where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.’” *Id.* Specifically, a preamble is not limiting where it “merely identifies an intended use” for the claimed invention. *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019).

In *Arctic Cat*, the Federal Circuit affirmed the Board’s determination that the preamble did not limit the claim. *Arctic Cat*, 919 F.3d at 1328. The preamble in *Arctic Cat* recited: “1. A personal recreational vehicle comprising.” *Id.* at 1324. Neither the term “personal recreational vehicle” nor any variation of it appeared in the body of the claim. *Id.* No element of the claim implicated, referred to, or relied upon “personal recreational vehicle.” Thus, the court found that, as in *Catalina*, “deletion of the disputed phrase from the preamble . . . [would] not affect the structural definition or operation of the [invention] itself.” *Id.* at 1329, *quoting Catalina*, 289 F.3d at 810. The court affirmed the Board’s determination that the preamble was not limiting because the claim body described a “structurally complete invention.” *Id.* The court noted that the preamble language “merely identifie[d] an intended use for the claimed power distribution module.” *Id.* at 1328.

Here, the body of claim 12 describes a structurally complete invention. It recites, a silicon substrate, a first dielectric layer comprising aluminium oxide, and a second dielectric layer. Neither the term “solar cell” nor any variation appears in the body of claim 12. Ex. 1001, 9:35-10:9. Furthermore, no element of the claim implicates, refers to, or relies upon a “solar cell.” Instead, the claim recites a semiconductor structure that *may* be used as a solar cell but may also have other uses. Ex. 1003, ¶ 33. Because of this, claim 12 “describes a structurally complete

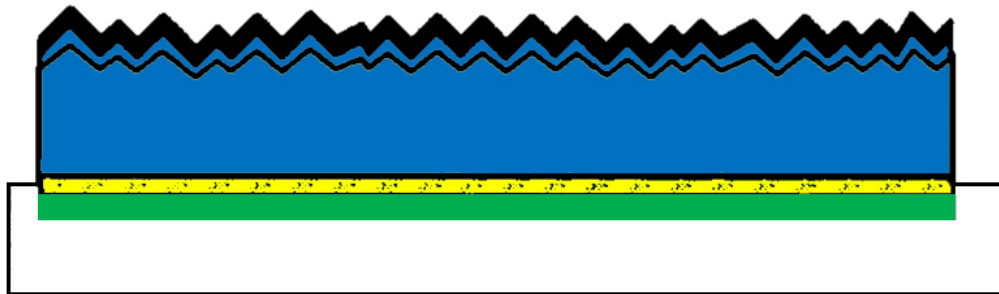
invention such that deletion of the preamble phrase does not affect the structure . . . of the claimed invention,” and should not be limiting. *Catalina*, 289 F.3d at 809.

V. CLAIMS 12-14 OF THE '215 PATENT ARE UNPATENTABLE

A. Overview of the Prior Art

1. *Agostinelli* '086

European Patent Application No. EP 1,763,086 A1 to Agostinelli (“*Agostinelli* '086”) published on March 14, 2007, more than a year before the PCT filing date of the '215 patent. Ex. 1005. It is prior art under 35 U.S.C. § 102. *Agostinelli* '086 discloses a solar cell device, depicted in annotated Fig. 1, below.



Specifically, *Agostinelli* '086 discloses “[a] solar cell device comprising a silicon substrate [shown in blue above] having a front main surface and a back main surface,” “[a] dielectric layer [yellow] on said back main surface” of the silicon substrate, and “a passivation layer [green] comprising hydrogenated SiN on top of said dielectric layer.” Ex. 1005, claim 18; *see also id.*, [0008]-[0010], [0037]-

[0041], [0043], [0045], [0053], [0059]-[0062]. The dielectric layer (yellow) can contain “SiO₂, SiO_x, SOG, TiO₂, *Al₂O₃*³ . . . or their pseudo-alloys.” *Id.*, [0056]. Various embodiments of the first dielectric layer (yellow) are disclosed having thicknesses less than 50 nm, “for instance more than 10nm, 40nm, 100nm, 200nm, 800nm of Oxides” *Id.*, [0053]. The passivation layer (green) contains “hydrogenated SiN,” a known dielectric material. *Id.* at claim 18; [0008], [0037], [0049], [0059]; *see also id.* at [0054] (“On top of [the first dielectric layer] a layer of SiN_x:H optimized for hydrogen release is deposited. The silicon surface passivation is improved by means of hydrogenation.”).

As noted above, *Agostinelli* '086 has a different disclosure than *Agostinelli* '303. The Examiner relied upon *Agostinelli* '303 in a rejection on March 13, 2014. Ex. 1002, 458-469. In response, the Applicant added a limitation requiring that the first dielectric layer have a thickness of less than 50 nm, arguing that *Agostinelli* '303 did not disclose that limitation. *Id.*, 445-449. In contrast, *Agostinelli* '086 discloses this limitation. Ex. 1005, [0019], [0044], [0053], [0064], claims 5 & 22.

Similarly, during prosecution, the Applicant argued that, unlike the claimed silicon substrate having a first and second dielectric layer, *Agostinelli* '303 disclosed

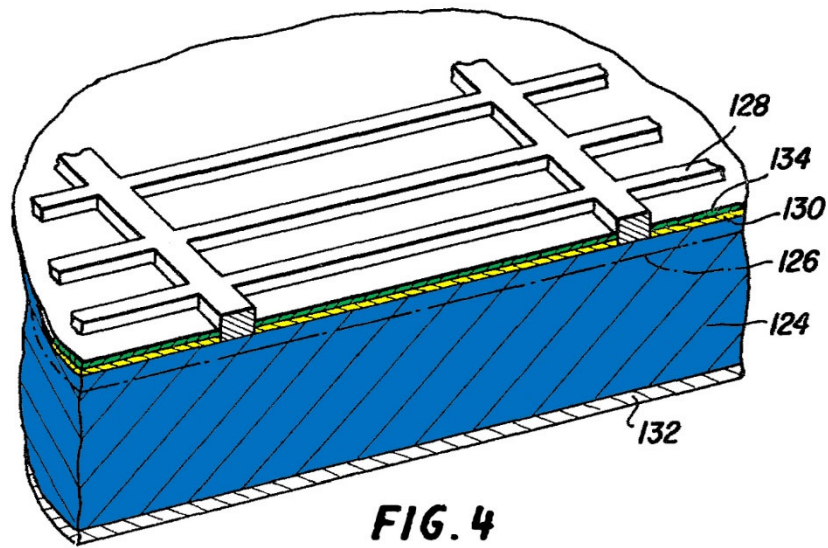
³ Unless noted otherwise, emphasis added to original.

a silicon substrate having three distinct dielectric layers. Namely, the Applicant asserted that *Agostinelli* '303 discloses first a “thick poor quality layer,” second, a “hydrogenated silicon nitride layer,” and third, a “high-quality aluminum oxide layer.” Ex. 1002, 449-452. Thus, the Applicant argued that *Agostinelli* '303 failed to teach a first dielectric layer that is “interposed between” the silicon substrate and the second dielectric layer, as claimed. By contrast, *Agostinelli* '086 discloses exactly that: a silicon substrate with a dielectric layer affixed to one of its surfaces and a second dielectric layer of a differing material having embedded hydrogen deposited directly on first dielectric oxide layer. Ex. 1005, claims 1& 18; *see also id.*, [0008]-[0010], and [0037]-[0039].

2. *Nakano*

U.S. Patent No. 4,463,216 to *Nakano*, et al. (“*Nakano*”) issued on July 31, 1984, more than a year before the PCT filing date of the '215 patent. Ex. 1006. It is prior art under 35 U.S.C. § 102. It was neither cited nor considered during prosecution.

Nakano discloses “[a] solar cell and a method of manufacturing the same.” Ex. 1006, Abstract.



The solar cell has “a semiconductor substrate having a major surface,” shown in blue above, “an aluminum oxide coating layer on said major surface,” shown in yellow, and “an antireflective layer further provided over said aluminum oxide coating layer,” shown in green. *Id.*, 10:19-29. In one embodiment, “the thickness of the aluminum oxide coating layer is about 80 Å,” which is about 8 nm. *Id.*, 3:33-35; Ex. 1003, ¶ 38. This thin aluminium oxide layer is formed using a dip coating method, where “[t]he thickness of the film or layer can be controlled by means of the lifting speed of the substrate.” Ex. 1006, 4:21-23. Figure 8 of *Nakano* shows that comparative examples were formed using this method having aluminium oxide thicknesses of approximately 8 nm, 30 nm, 50 nm, and 90 nm. *Id.*, Fig. 8.

The antireflective layer (green in Fig.4) may comprise a tantalum pentoxide layer, which is a known dielectric material. *Id.*, 3:31-32; Ex. 1003, ¶ 39; citing Ex.

1006 at 3:31-32. These dielectric layers “reduce the recombination velocity of the carriers at the interface between the aluminum oxide layer and a semiconductor substrate” thereby increasing the conversion efficiency through passivation. Ex. 1006, 2:33-38.

3. *Hoex 2006*

Bram Hoex, et. al. “Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited Al_2O_3 ” *Applied Physics Letters* 89:4 (2006): 042112 (“*Hoex 2006*”) was published in the journal Applied Physics Letters on July 27, 2006, and was publicly accessible no later than early September of 2006.⁴ Ex. 1009, 042112-1. It is prior art to the ’215 Patent under 35 U.S.C. § 102.⁵

Hoex 2006 describes improving silicon solar cell surface passivation by applying a 7-30 nm thick aluminium oxide film on the silicon substrate. *Id.* Like

⁴ Ex. 1009 was cited by others before November 2007. *See* Exs. 1023, 1024, and 1027.

⁵ During prosecution, the Examiner relied on a separate article by Hoex: “Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al_2O_3 .” This article is a separate disclosure from *Hoex 2006*.

Nakano, Hoex 2006 seeks to improve the efficiency of the solar cell by minimizing “surface recombination” on the silicon substrate via surface passivation. *Id.* *Hoex* 2006 explains that “[s]urface passivation of crystalline silicon (c-Si) is of key importance for the performance of high efficiency industrial solar cells.” *Id.*

Hoex 2006 discloses the use of “thin high bandgap dielectric Al_2O_3 as a surface passivation layer” and shows that it provides excellent passivation on both n and p-type silicon substrates. *Id.*, 042112-2. *Hoex* 2006 tested “ Al_2O_3 films with a thickness of 7-30 nm,” and showed that even a “7 nm thin Al_2O_3 film still yields an effective surface recombination velocity.” *Id.*, 042112-1.

4. *Narwankar*

U.S. Patent Application No. 10/851,561 to Narwankar et al. (“*Narwankar*”) (Ex. 1007) was published as U.S. Patent Application Publication No. 2005/0260347 on November 24, 2005, more than a year before the PCT filing date of the ’215 patent. It is prior art under 35 U.S.C. § 102. It was neither cited nor considered during prosecution.

Narwankar discloses “a method for depositing a capping layer on a dielectric layer . . . which includes depositing the dielectric layer on a substrate surface, depositing a silicon-containing layer by an ALD process.” Ex. 1007, Abstract. The dielectric layer can be Al_2O_3 or an $\text{Al}_2\text{O}_3/\text{TiO}_2$ pseudobinary alloy. *Id.*, [0024].

FIG. 2C



In one embodiment, depicted in annotated Fig. 2C above, this process may be used to deposit a silicon oxide layer 220, shown in green, on dielectric layer 210, shown in yellow, by an ALD process. *Id.*, [0025]. These layers are deposited on a substrate 200, shown in blue, which may comprise silicon. *Id.*, [0022]. The dielectric layer 210 “is generally deposited with a film thickness of about 10 Å [1 nm] to about 1,000 Å [100 nm], preferably from about 20 Å [2 nm] to about 500 Å [50 nm] and more preferably from 50 Å [5 nm] to about 200 Å [20 nm] . . .” *Id.*

5. *Tan*

U.S. Patent No. 6,929,700 (“*Tan*”) issued on August 16, 2005, more than a year before the PCT filing date of the ’215 patent. Ex. 1030. It is prior art under 35 U.S.C. § 102(b). It was neither cited nor considered during prosecution.

As depicted in Fig. 2 below, *Tan* discloses a method of depositing silicon oxide layers by forming a high density plasma from a process gas. Ex. 1030, 1:18 and 2:43-50. Specifically, *Tan* discloses forming an undoped silicon oxide layer from a process gas containing a SiH₄ gas, an oxygen-containing source such as O₂ gas, an inert gas such as Ar gas, and a hydrogen-containing source such as H₂ gas. *Id.*, 2:50-53 & 57-59.

Tan teaches that “deposition conditions for such a silicon oxide film are carefully controlled in order to minimize the amount of hydrogen incorporated into the film because as is known to those of skill in the art, hydrogen is a source of film instability.” *Id.*, 11:36-40. However, similar to Narwankar, *Tan* teaches using a hydrogen-containing gas in the deposition process because “adding a flow of a hydrogen containing gas in Step 200 can increase the gap-fill capability of the film without leading to film instability provided other deposition conditions are maintained within certain ranges.” *Id.*, Fig. 2, 40-45. This gap-filling capability is desirable because it ensures that the entire surface is covered by the silicon oxide layer. Ex. 1003, ¶ 45. This is increasingly important considering the decreasing semiconductor device geometries and the need to fill gaps with a high aspect ratio (i.e., ratio of the gap’s height or depth to its width). Ex. 1030, 1:35-41.

Tan discloses that the deposited silicon oxide layer has a hydrogen content of less than or equal to 2 atomic percent. *Id.*, 2:54-56.

B. Ground 1: *Agostinelli* ’086 Anticipates Claims 12-14 Under 35 U.S.C. § 102

Agostinelli ’086 discloses every limitation of claims 12-14 of the ’215 patent. Thus, it anticipates those claims and renders them unpatentable.

1. Claim 12

a. Element [12.0]: “A solar cell comprising:”

To the extent the preamble of claim 12 is limiting, *Agostinelli* '086 discloses a photovoltaic cell and embodiments directed to solar cells. *See, e.g.*, Ex. 1005, [0007] (“It is an aim of this invention to provide for a method for producing a photovoltaic cell . . .”). Indeed, *Agostinelli* '086 explicitly recites a “solar cell” in its claims. *Id.*, claims 1 & 18.

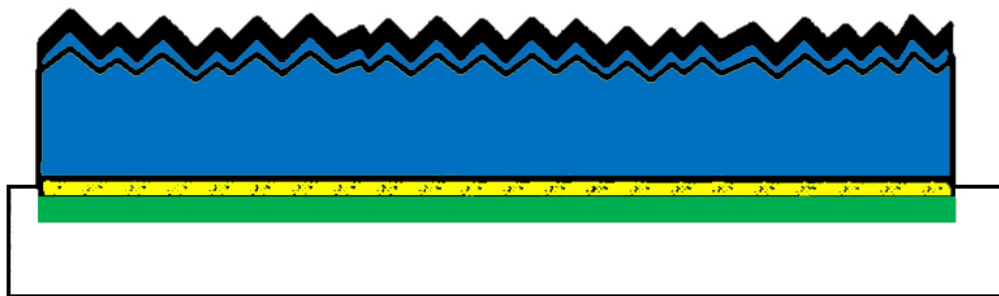
b. Element [12.1]: “a silicon substrate;”

Agostinelli '086 discloses “a solar cell device comprising . . . a silicon substrate.” Ex. 1005, 12:28-34. *Agostinelli* '086 states that “*Any* silicon substrate may be used” in practicing its invention. *Id.*, [0038]. Like the '215 patent, *Agostinelli* '086 describes the silicon substrate as having a “front” surface and a “back” surface. Ex. 1001, 3:37-38 and 3:45-46; *cf.* Ex. 1005, 12:30-31. *Agostinelli* '086 also provides examples of suitable silicon substrates that are nearly identical to those disclosed in the '215 patent. The '215 patent states that the silicon substrate “may be a thin monocrystalline or multicrystalline silicon wafer or else a silicon thin layer.” Ex. 1001, 3:34-36. Likewise, *Agostinelli* '086 teaches a “multicrystalline silicon wafer,” in addition to thin monocrystalline wafers and silicon thin layers. Ex. 1005, [0009]-[0010], [0038]-[0039].

- c. **Element [12.2]: “a first dielectric layer comprising aluminium oxide on a surface of the silicon substrate; and”**

Agostinelli '086 discloses “a silicon substrate . . . having a front main surface and a back main surface” and “a dielectric layer on the back main surface” of the silicon substrate. Ex. 1005 at [0037]; *see also id.* at [0008]-[0010], [0038-0041], [0043], [0045], [0053], [0059]-[0062], claims 1 & 18. This language notes that a silicon substrate has at least two surfaces and discloses a dielectric layer on the back surface. The specification explains that the oxide dielectric layer may be “deposited on the silicon surface.” Ex. 1005 at [0053].

Annotated figure 1 depicts an embodiment of *Agostinelli* '086, showing the silicon substrate (blue) and dielectric layer (yellow) in continuous contact, i.e., the dielectric layer is on the surface of the silicon substrate.



Agostinelli '086 discloses that the dielectric layer may comprise a “low quality amorphous oxide, for instance Al_2O_3 / TiO_2 pseudobinary alloys (PBAs).” Ex. 1005, [0041] and [0044]. A POSITA would understand that Al_2O_3 is the chemical formula

for aluminium oxide. Ex. 1003, ¶ 57. Indeed, the '215 patent uses Al_2O_3 for aluminium oxide. Ex. 1001, 3:21-27, 4:32-37. Furthermore, *Agostinelli* '086 explains that “[a] generic low quality amorphous Oxide was deposited (e.g., SiO_2 , SiO_x , SOG, TiO_2 , **Al_2O_3** . . . or their pseudo-alloys, SiON_x ,) on the solar cell’s rear side silicon surface . . .” Ex. 1005, [0056]; *see also* [0037], [0040], [0041], [0043], [0045]. Thus, *Agostinelli* '086 meets element [12.2]. Ex. 1003, at ¶ 58.

d. Element [12.3]: “a second dielectric layer directly on a surface of the first dielectric layer, materials of the first dielectric layer and the second dielectric layer differing and”

Agostinelli '086 discloses a passivation layer comprising hydrogenated SiN on top of the dielectric layer, which can comprise aluminium oxide. Ex. 1005, [0008], [0037], [0064], claims 1 & 18. Thus, it discloses a first dielectric layer comprising aluminium oxide with a second dielectric layer of hydrogenated SiN on top of the first layer. A POSITA would readily understand the “passivation layer” in *Agostinelli* to be a dielectric layer. *See* Ex. 1003, ¶ 61. Indeed, *Agostinelli* '086 explains that one problem it solves is “[e]ngineering a **dielectric** with surface passivation properties.” Ex. 1005, [0003]-[0004]. *Agostinelli* '086 refers to its $\text{SiN}_x\text{:H}$ passivation layer as “an optimized hydrogenated **dielectric layer**.” *Id.*, [0056]. This is also consistent with the '215 Patent, which specifically claims SiN

(i.e., silicon nitride) as the second dielectric layer. Ex. 1001, 4:64-5:5, claims 3, 10, 11, and 13.

Moreover, as can be seen in the annotated figure above, this passivation layer (green) is deposited directly on the top surface of the first dielectric layer (yellow). Ex. 1005, [0037].

Agostinelli '086 further notes that:

In the embodiments of the present invention, for instance more than 10 nm, 40nm, 100nm, 200nm, 800nm of Oxide are deposited on the silicon surface. ***On top of it, a layer of SiNx:H optimized for hydrogen release is deposited.***

The silicon surface passivation is improved by means of hydrogenation.

Id., [0053]. This language expressly discloses a dielectric oxide layer on a surface of a silicon substrate and a second dielectric layer, composed of hydrogenated silicon nitride, directly on top of the dielectric oxide layer. The configuration of these three layers in order, i.e., a silicon substrate, a first dielectric layer (comprising an oxide), and second dielectric layer (or “passivation layer,” *see* Ex. 1003, ¶ 61) satisfies the configuration of three layers claimed in claim 12.

Agostinelli '086 also discloses materials of the first dielectric layer and second dielectric layer differing because the first layer comprises aluminium oxide (see

discussion above), whereas the passivation layer on top of it comprises hydrogenated silicon nitride. Ex. 1005, [0008], [0037], [0049], and [0064]. These are different materials. Ex. 1003, ¶ 63.

e. Element [12.4]: “hydrogen being embedded into the second dielectric layer;”

To the extent this limitation is satisfied by the presence of hydrogen in the second dielectric layer, *Agostinelli* '086 meets this limitation because it discloses a passivation layer comprising hydrogenated SiN. *Id.*, [0008], [0037], [0059], [0064], claims 1 & 18. A POSITA would understand a passivation layer comprising hydrogenated silicon nitride to include hydrogen. Ex. 1003, ¶¶ 64-. Indeed, *Agostinelli* '086 expressly describes the passivation layer as having hydrogen because it notes that hydrogenated silicon nitride “can release hydrogen” in high temperature conditions. Ex. 1005, [0059]. *Agostinelli* '086 also proposes a mechanism for hydrogenated silicon nitride’s improvement of surface passivation relying on the fact that “the silicon nitride is used as a hydrogen source for the low quality oxide underneath.” *Id.*, [0060].

To the extent is limitation is satisfied by use of reactants that contain hydrogen to form the second dielectric layer, *Agostinelli* '086 discloses materials for forming the second layer nearly identical to those disclosed by the '215 patent. The second dielectric layer of the '215 Patent is created using “reactants such as for example

silane (SiH_4), dinitrogen oxide (N_2O), carbon dioxide (CO_2), *ammonia* (NH_4) and/or methane (CH_4).” Ex. 1001, 5:8-11. Similarly, *Agostinelli* ’086 discloses that “hydrogenated SiN_x deposited at 400 degrees from ***SiH₄ and NH₃*** precursors.”⁶ Ex. 1005, [0064].

- f. Element [12.5]: “wherein the first dielectric layer has a thickness of less than 50 nm and is interposed between the surface of the silicon substrate and the second dielectric layer.”**

Agostinelli ’086 discloses this limitation because it discloses a solar cell device “wherein said dielectric layer has a thickness between 40 and 1500 nm.” Ex. 1005 at [0044], claims 5 & 22. As explained for element [12.2], the “dielectric layer” in *Agostinelli* ’086 comprises aluminium oxide and corresponds to the “first dielectric layer.” *Agostinelli* ’086 further discloses this limitation in describing embodiments in which various thicknesses of Oxide were deposited, two of which anticipate the claimed “less than 50 nm” thickness: “for instance more than 10nm, 40nm, 100nm, 200nm, 800nm of Oxides . . . [i.e., the first dielectric layer] are deposited on the silicon surface.” *Id.* at [0053].

⁶ A POSITA would understand that NH_3 is the chemical formula for ammonia. Ex. 1003, ¶ 68.

A prior art range anticipates a species within the claimed range if the prior art “describes the claimed range with sufficient specificity such that a reasonable finder of fact could conclude that there is no reasonable difference in how the invention operates over the ranges.” *Ineos USA LLC v. Berry Plastics*, 783 F.3d 865, 869 (Fed. Cir. 2015). When evaluating whether a range anticipates a species, courts evaluate whether the claimed species is “critical.” *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1344-45 (Fed. Cir. 2012).

The disclosures in *Agostinelli* '086 of exemplary thickness of “more than 10nm, 40nm . . .”, as well as the range of “a thickness between 40 and 1500 nm” expressly describes the claimed thickness of less than 50 nm. Furthermore, there is no evidence in the disclosure of '215 patent that “less than 50 nm” is critical. In fact, the specification only suggests a first dielectric layer having a thickness of less than 50 nm in one embodiment. Ex. 1001 at 5:40-50. The specification states that “[t]he thinner the layer is, the more rapidly it can be deposited . . .” *Id.* at 5:47-48. But this alleged advantage pertains only to the manufacturing process, not the claimed cell structure itself. Thus, with respect to what is *claimed* (i.e., a particular cell structure), the '215 patent does not identify any criticality associated with the “less than 50 nm” structural limitation.

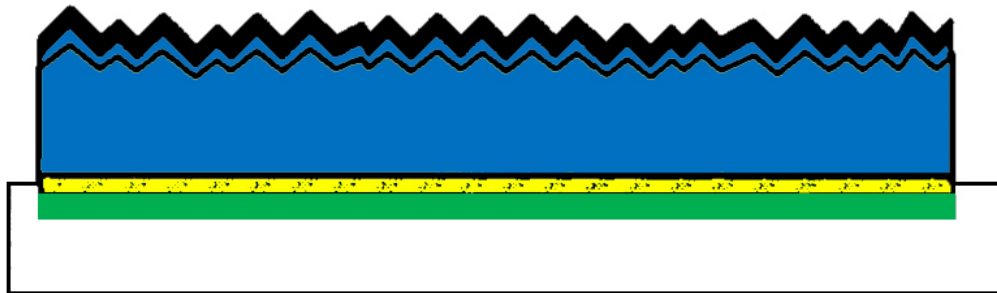
Moreover, the '215 patent's prosecution history indicates that this limitation was imported into the independent claim not because of any criticality for the range but merely to distinguish *Agostinelli* '303—a different reference that did not include the express thickness disclosures contained in *Agostinelli* '086. Specifically, in its June 12, 2014 amendment, claim 9, directed to the solar cell device, was amended to include the language of cancelled claim 12, reciting the device “wherein the first dielectric layer has a thickness of less than 50 nm.” Ex. 1002, 446-453. The accompanying remarks did not assert any criticality for the range of “less than 50 nm,” merely noting that *Agostinelli* '303 did not meet that limitation. Ex. 1002, 449-453.

A POSITA would have known how to create a dielectric layer comprising Al_2O_3 having a thickness of less than 50 nm as taught in *Agostinelli* '086. Ex. 1003, ¶ 70. For instance, Hanwha admitted during the prosecution of an application in the same field as the '215 patent, No. 13/140,282 to Engelhart (“*Engelhart*”) Ex. 1014, “one of ordinary skill in the art in the field of photovoltaics” would understand how to achieve an Al_2O_3 dielectric layer of less than 50 nm following the teachings of the relevant literature.” *Id.*, 40. During prosecution of *Engelhart*, Hanwha cited two 2006 articles that recite an Al_2O_3 passivation layer having a thickness of less than 50 nm. *Id.*, 40.

Table 1 Literature overview regarding Al ₂ O ₃ passivation of c-Si before the priority of our application			
Ref. no.		Al ₂ O ₃ thickness (nm)	Comment
1	G. Agostinelli et al. Sol. Energy Mat. & Solar Cells 90 (2006) 3438-3443	40 – 50 nm	Spin coated from sol gels (section 3)
2	B. Hoex et al. Appl. Phys. Lett. 89, 042112 (2006)	15 / 30 nm (Fig. 1)	Plasma-assisted ALD, 7 nm thickness only for n-type wafers

Each article, published before the earliest effective filing date of the '215 patent, teaches depositing Al₂O₃ passivation layers with thicknesses of < 50 nm deposited by means of either spin-coating or ALD. *See* Ex 1015; Ex. 1007. Thus, given *Agostinelli* '086 expressly disclosures and Hanwha's admission, a POSITA would have understood *Agostinelli* '086 as expressly disclosing an aluminium oxide layer less than 50 nm. Ex. 1003, ¶ 70.

As discussed above, *Agostinelli* '086 depicts a first dielectric layer “interposed between the surface of the silicon substrate and the second dielectric layer.” *See* Ex. 1005, Fig. 1 (annotated below with first dielectric layer (yellow); silicon substrate (blue); and the second dielectric layer (green)).



2. Claim 13

a. Element [13.0]: “The solar cell according to claim 12,”

See elements [12.0]-[12.5].

b. Element [13.1]: “wherein the second dielectric layer comprises a material selected from the group consisting of silicon nitride, silicon oxide, and silicon carbide.”

Agostinelli '086 discloses this limitation. As discussed for element [12.3], a second dielectric layer comprising hydrogenated silicon nitride is disclosed. Silicon nitride is one of the sub-elements recited in this limitation's *Markush* group. Limitations written in *Markush* form are anticipated if a reference discloses any one of the elements. *Fresenius USA, Inc. v. Baxter International, Inc.*, 582 F.3d 1288, 1298 (Fed. Cir. 2009).

3. Claim 14

a. Element [14.0]: “The solar cell according to claim 12,”

See elements [12.0]-[12.5].

b. Element [14.1]: “wherein the first dielectric layer has a thickness of less than 30 nm.”

Agostinelli '086 discloses examples of a dielectric layer with thicknesses of “more than 10 nm, 40nm” which can comprise aluminium oxide or “Al₂O₃/TiO₂ pseudobinary alloys.” Ex. 1005, [0053]; [0018]. This teaching of an exemplary layer having a thickness “more than 10 nm” and less than the next largest example

of “40 nm” would be understood by a POSITA, in context, as expressly disclosing the “less than 30 nm” limitation. Ex. 1003, ¶ 78.

Again, there is no evidence in the disclosure of ’215 patent that “less than 30 nm” is critical. In fact, the specification discloses a “minimum thickness of about 0.5 nm” Ex. 1001, 5:48-49 and a most preferred thickness of “less than 10 nm,” *id.* at 5:43, but no criticality is suggested at a thickness of less than 30 nm. The specification states that “[t]he thinner the layer is, the more rapidly it can be deposited . . .” *Id.*, 5:47-48. But this alleged advantage pertains only to the manufacturing process, not the claimed cell structure itself. Thus, with respect to what is *claimed* (i.e., a particular cell structure), the ’215 patent does not identify any criticality associated with the “less than 30 nm” structural limitation.

C. Ground 2: Claims 12-14 Are Obvious Over *Agostinelli* ’086 in View of *Nakano* and *Hoex* 2006 Under 35 U.S.C. § 103

As discussed above, *Agostinelli* ’086 recites every element of claims 12-14, anticipating and rendering these claims unpatentable. But if Hanwha argues or the Board finds that *Agostinelli* ’086 fails to teach (1) a dielectric layer having a thickness of less than 50 nm as recited in Element [12.5], and/or (2) a dielectric layer having a thickness of less than 30 nm as recited in Element [14.2], the claimed invention including these elements would have been obvious to a POSITA based on

the teachings of *Agostinelli* '086 in combination with *Nakano* in view of the teachings of *Hoex* 2006. Ex. 1003, ¶¶ 79-96.

1. Claim 12

- a. Element [12.5]: “wherein the first dielectric layer has a thickness of less than 50 nm and is interposed between the surface of the silicon substrate and the second dielectric layer.”**

For the reasons discussed for Ground 1, element [12.5], *Agostinelli* '086 discloses a solar cell device with a first dielectric layer having a thickness between 40 and 1500 nm. But if the overlapping range of *Agostinelli* '086 is insufficient to anticipate element [12.5], it would have been obvious to a POSITA based on the teachings of *Agostinelli* '086 in combination with *Nakano* in view of *Hoex* 2006. Ex. 1003, ¶ 79.

Hoex 2006 discloses “Excellent surface passivation” of silicon substrates by “Al₂O₃ films prepared by plasma-assisted atomic layer deposition.” Ex. 1009, Abstract. It discloses that “Al₂O₃ films with a thickness of 7-30 nm” were produced in an ALD reactor. *Id.*, 042112-2. It reports that these “ultrathin films of Al₂O₃ exhibit a similar level of surface passivation as annealed thermal silicon oxide on both *n*- and *p*-type silicon.” *Id.*, 042112-1. Specifically, the “results obtained for ~30 nm thick Al₂O₃ films are comparable to state-of-the-art results when employing thermal oxide as used in record-efficiency *c*-Si solar cells.” *Id.*, Abstract. Similarly,

“[a] 7 nm thin Al₂O₃ film still yields an effective surface recombination velocity of 5 cm/s on *n*-type silicon.” *Id.* It reports that these excellent results—on par with state-of-the-art cells exhibiting record efficiency—were obtained at Al₂O₃ thicknesses of 15 nm and 30 nm on *p*-type silicon substrates, and 7 nm on *n*-type silicon substrates. *Id.*, 042112-2.

Because *Agostinelli* '086 and *Hoex* 2006 are both directed to methods of improving solar cell efficiency by using an oxide passivation layer on a silicon substrate—i.e., the same goal as the '215 patent—a POSITA at the time of the invention would considered the teachings of both references. Ex. 1003, ¶ 85.

Agostinelli '086 discloses an aluminium oxide passivation layer having a thickness between 40-1500 nm. Ex. 1005 at [0044], claims 5 & 22. It further discloses that the oxide layer can be as thin as 10-40 nm, i.e., “more than 10 nm, 40 nm . . .” Ex. 1005, [0053]. Based on the teachings of *Hoex* 2006, a POSITA would understand that an aluminium oxide passivation layer with a thickness of 15 nm or 30 nm on a *p*-type silicon substrate, or 7 nm on an *n*-type silicon substrate, would yield “Excellent surface passivation” and efficiencies “comparable to state-of-the-art results” using annealed thermal silicon oxide. *Id.*, Abstract; Ex. 1003, ¶ 86. This would motivate a POSITA to use the lower end of the disclosed range in *Agostinelli*

(i.e., 10-40 nm) for the aluminium oxide layer on a *p*-type silicon substrate, and as low as 7 nm on an *n*-type silicon substrate. Ex. 1003, ¶ 86.

Although *Hoex* 2006 discloses the use of plasma-enhanced ALD to create the desired “ultrathin films of Al₂O₃,” *Nakano* teaches that ultra-thin films of Al₂O₃ can be created using a dip coating method, which is one of the methods expressly suggested in *Agostinelli* '086 Ex. 1005, [0018] (“The low-quality amorphous oxide can for instance be a . . . spin-on, spray-on *or dip oxide* . . .”); Ex. 1006 2:44-47. A POSITA desiring to practice *Agostinelli* '086 at the low end of its disclosed range for the aluminium oxide layer thickness (as suggested by *Hoex* 2006) would be motivated to follow the teaching of *Nakano* to do so.

Both *Agostinelli* '086 and *Nakano* are directed at improving silicon solar cell efficiency, by reducing surface recombination velocity and applying anti-reflective layers. Ex. 1005, ¶ 3; Ex. 1006, 2:28-37. Both disclose depositing two dielectric layers on the surface of the silicon substrate to reduce the recombination velocity at the silicon substrate. Ex. 1005, Fig. 1; Ex. 1006, Fig. 4. Both teach applying an aluminium oxide first dielectric layer on the silicon substrate. Ex. 1005, [0018]; Ex. 1006, 3:28-32. Thus, these are closely analogous references, and a POSITA would be aware of both. Ex. 1003, ¶ 88.

Nakano discloses an aluminium oxide dielectric layer having a thickness of about 80 Å, i.e., about 8 nm. Ex. 1006, 3:33-34. Additional embodiments disclose thicknesses of “less than 100 Å,” or 10 nm. 5:30-31; 5:57-58 and 10:30-32. *Nakano* discloses that these ultra-thin aluminium oxide layers can be achieved using a “dipping” method:

After the formation of electrode 128, the silicon substrate was dipped into and lifted from the aluminum oxide solution held at room temperature. . . The thickness of the film or layer can be controlled by means of the lifting speed of the substrate. The resultant thickness of the aluminum layer was selected to be 80 Å [8 nm].

Id., 4:16-24. A POSITA would readily understand that thicker layers can be formed (e.g., 15 nm or 30 nm) by controlling the “lifting speed of the substrate.” *Id.*; Ex. 1003, ¶ 89. Indeed, *Nakano* expressly discloses the correlation between lifting speed and aluminium oxide layer thickness in Figure 7:

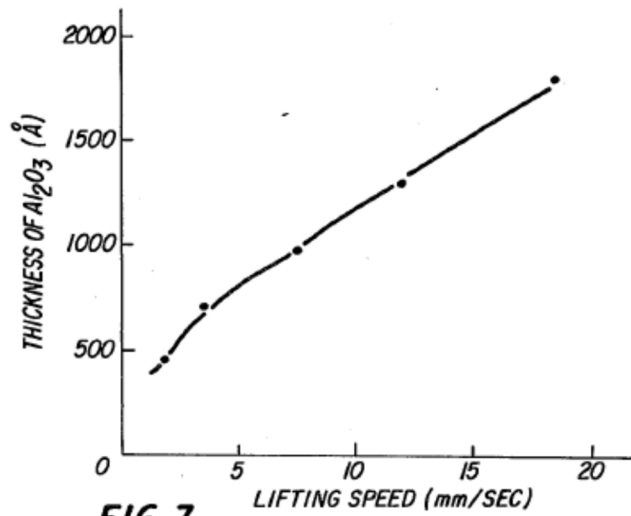


FIG. 7

Nakano also discloses in Figure 8 that comparative examples were prepared having aluminium oxide layer thicknesses of approximately 80 Å (8 nm), 300 Å (30 nm), 500 Å (50 nm), and 900 Å (90 nm):

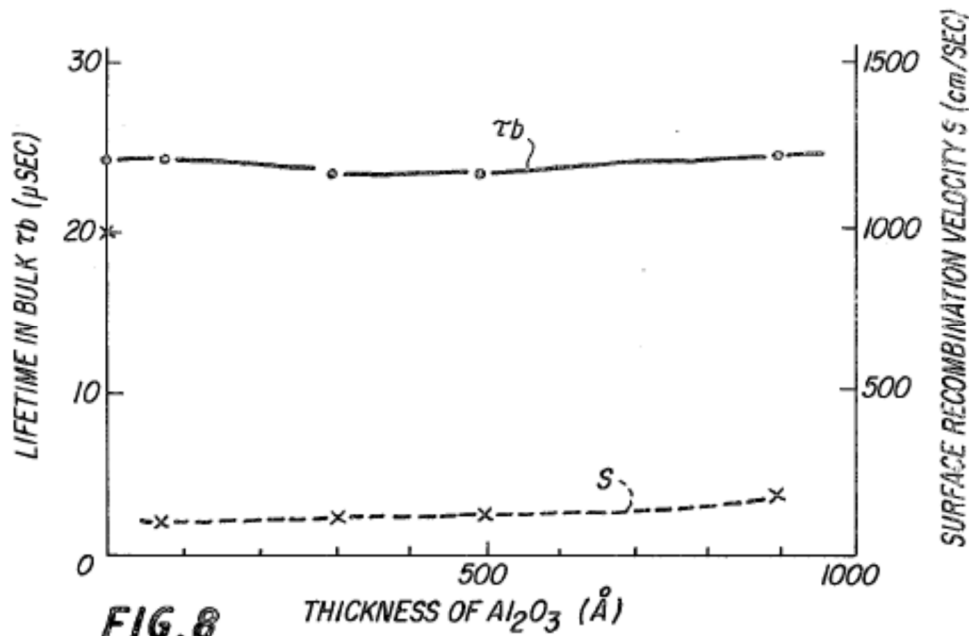


FIG. 8

Figure 8 illustrates the “relationship of the lifetime of . . . the surface recombination velocity with the thickness of the aluminum oxide coating layer.” Ex. 1006, 3:4-6. The x-axis, labelled “Thickness of Al₂O₃ (Å)” depicts a range of thicknesses between 0 Å (0 nm) and 1000 Å (100 nm), and examples are provided at approximately 8 nm, 30 nm, 50 nm, and 90 nm. *Nakano* discloses that producing an Al₂O₃ layer having a thickness of less than 50 nm is possible and that producing a thinner Al₂O₃ layer would not negatively impact surface recombination velocity. *Id.*, 7:34-50 (“As clearly shown in FIG. 8, S [surface recombination velocity] does not substantially depend upon the thickness of the aluminum oxide film.”)

Creating a photovoltaic cell as taught in *Agostinelli* '086, wherein the first dielectric layer has a thickness as low as 8 nm as disclosed in *Nakano*, or thicker (e.g., 10-40 nm), would have been obvious to a POSITA based on the teachings of each of these references. Ex. 1003, ¶¶ 90-94. First, *Agostinelli* '086 expressly discloses that dip coating at room temperature is a suitable technique for creating the first dielectric layer comprising aluminium oxide. *See* Ex. 1005 at [0018] (“The low-quality amorphous oxide can for instance be a Spin-on oxide or APCVD pyrolithic oxide (pyrox), spin-on, spray-on, or **dip oxide**...”). Thus, a POSITA would naturally look to references that teach dip coating to create an aluminium oxide layer, which *Nakano* expressly teaches. Second, because *Agostinelli* '086

expresses a desire to deposit the oxide layer at a thicknesses of “more than 10 nm, 40nm,” *id.* at [0053], and because *Hoex* 2016 teaches that aluminium oxide layers of 7 nm, 15 nm, and 30 nm yielded “excellent” results comparable to state-of-the-art cells with record efficiency, this would provide further motivation to create aluminium oxide layers in the 10-40 nm range, or even as low as 7 nm, which *Nakano* teaches. Thus, starting with the express teachings of *Agostinelli* '086 and finding a motivation in *Hoex* 2006 to practice the low end of the thickness range in *Agostinelli* '086, a POSITA would be further motivated to follow the teaching of *Nakano* to create such a layer using dip coating.

Moreover, a POSITA would have known that creating a thicker dielectric layer is more expensive than creating a thinner dielectric layer and would thus have been additionally motivated to create thinner aluminium oxide layers, which *Nakano* does. The creation of thinner dielectric layers requires less raw materials and is less time consuming, leading to process savings. Ex. 1003, ¶ 94. These are additional motivating factors, above and beyond those explained above.

A POSITA could have practiced *Agostinelli* '086 by creating an aluminium oxide layer with a thickness of 10-40 nm, or even as low as 7 nm, following the dip coating method that is taught generally in *Agostinelli* '086 and specifically in *Nakano*. Ex. 1003, ¶¶ 79-94. A POSITA would have expected success in doing so

because: (1) dip coating was a well-understood technique at the time; (2) *Agostinelli* '086 identifies dip coating as a suitable method for forming the oxide layer (Ex. 1005 ¶ [0018]); (3) *Nakano* provides an experimental example of a solar cell with an 8 nm aluminium oxide layer (*see* Ex. 1006 at 5:16-17); (4) a POSITA would understand that greater thicknesses, e.g., 15 nm or 30 nm, could be created by adjusting the “lifting speed of the substrate,” as specifically taught by *Nakano* including in Fig. 7; and (5) Figure 8 of *Nakano* shows comparative examples with aluminium oxide thicknesses of approximately 8 nm, 30 nm, 50 nm, and 90 nm. Ex. 1003, ¶¶ 79-94.

Further, *Agostinelli* '086 and *Nakano* in view of *Hoex* 2006 satisfy elements [12.0]-[12.4] and the remaining features of element [12.5] for the same reasons explained in Ground 1, claim 12.

2. Claim 13

Agostinelli '086 and *Nakano* in view of *Hoex* 2006 satisfy claim 13 for the same reasons explained in Ground 1, claim 13. Specifically, *Agostinelli* '086 discloses a second dielectric layer comprising hydrogenated silicon nitride is disclosed. Ex. 1003, ¶ 95.

3. Claim 14

Agostinelli '086 and *Nakano* in view of *Hoex* 2006 satisfy claim 14 for the same reasons explained in Ground 2, element [12.5]. Ex. 1005, ¶ 53.

D. Ground 3: Claims 12-14 Are Obvious Over *Nakano* in View of *Hoex* 2006 and the Knowledge of a POSITA Under 35 U.S.C. § 103

Nakano expressly discloses every element of claims 12-14 of the '215 patent, except the “embedded hydrogen” limitation of Element 12.4. *Hoex* 2016 and the knowledge of a POSITA at the time of the claimed invention cure this defect, rendering these claims obvious.

Both *Nakano* and *Hoex* 2006 are directed at improving silicon solar cell efficiency by reducing surface recombination velocity. Ex. 1006 at 2:29-38 and Ex. 1007 at 042112-1. Both disclose depositing two dielectric layers on the surface of the silicon substrate to achieve a reduced recombination velocity at the silicon substrate. . See Ex. 1006 at Fig 8. Thus, a POSITA at the time of the invention would have considered the teachings of both references. Ex., 1003, ¶ 105.

1. Claim 12

a. Element [12.0]: “A solar cell comprising:”

To the extent Element [12.0] is limiting, *Nakano* discloses “a solar cell having increased conversion efficiency.” Ex. 1006, 2:28-29. *Nakano*, titled “Solar cell,” discloses “[a] solar cell and a method of manufacturing the same.” *Id.*, Abstract. The disclosed solar cell has a “substrate having a major surface for receiving light, a p-n junction for photovoltaic generation therein and a thin alumina coating layer on the major surface of the semi-conductor substrate.” *Id.*, Abstract.

a. Element [12.1]: “a silicon substrate;”

Nakano discloses a solar cell with a semiconductor silicon substrate. Ex. 1006, 3:31-32. Specifically, *Nakano* discloses a solar cell comprising: “[s]*ilicon substrate*/aluminum oxide layer/tantalum pentoxide layer/(atmosphere).” *Id.* Silicon substrates are also used in other disclosed structures. *Id.*, 4:35-5:63.

b. Element [12.2]: “a first dielectric layer comprising aluminium oxide on a surface of the silicon substrate; and”

Nakano discloses a solar cell comprising an aluminium oxide layer on the surface of a silicon substrate. *Id.*, 3:31-32. As acknowledged in the '215 patent, aluminium oxide is a known dielectric material. Ex. 1001, 2:50-52. In *Nakano*'s preferred embodiment, the principal surface of the silicon substrate is “covered first with an aluminum oxide layer.” Ex. 1006, 3:22-24. When comparing the Preferred Embodiment (silicon substrate, aluminium oxide layer, and antireflective layer) with the Comparative Example (silicon substrate and antireflective layer only), *Nakano* concludes that the embodiment with the aluminium oxide layer “is superior to the Comparative Example having only the anti-reflective layer.” *Id.* at 5:12-16 and Table 1.

c. Element [12.3]: “a second dielectric layer directly on a surface of the first dielectric layer, materials of the first

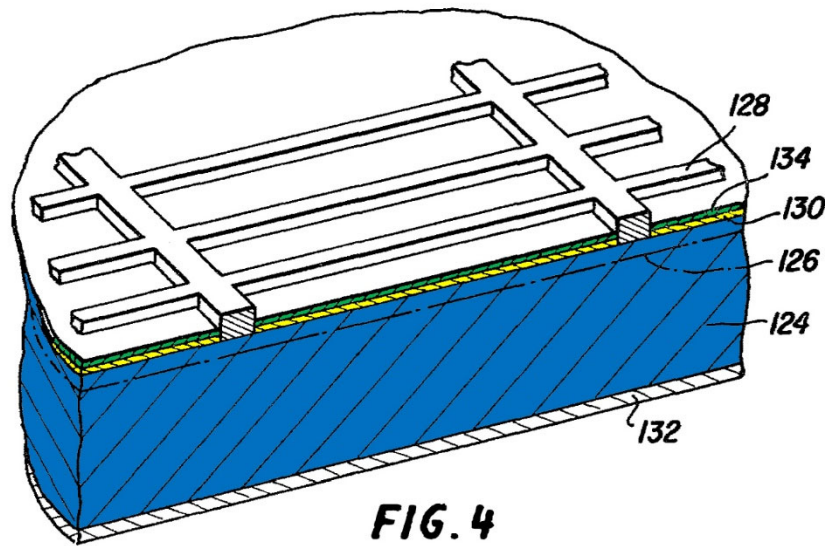
dielectric layer and the second dielectric layer differing and”

Nakano discloses a solar cell having a tantalum pentoxide layer directly on an aluminium oxide dielectric layer. Ex. 1006, 3:21-24, 5:26, and 5:51-55. Specifically, *Nakano* discloses “[a] solar cell comprising a semiconductor substrate,” “an aluminum oxide coating layer” on that substrate, and “an antireflective layer . . . over said aluminum oxide coating layer.” *Id.*, claim 1. In the preferred embodiment, the “antireflective layer” is a tantalum pentoxide layer. *Id.*, 3:28-32; *see also id.*, 4:53. 5:13-16 (comparing structure 1, comprising “Silicon substrate/aluminum oxide layer/tantalum pentoxide layer/(atmosphere), with “the Comparative Example having only the anti-reflective layer,” comprising only “Silicon substrate/tantalum pentoxide layer/air).”).

A POSITA would understand that this antireflective tantalum pentoxide layer is also a dielectric material. Ex. 1003, ¶ 109. Tantalum pentoxide has been known as a high dielectric material since at least the 1970s. *See, e.g.*, Ex. 1016 (U.S. Patent No. 3,585,072) at 1:51-56 (“The tantalum pentoxide is a dielectric”); Ex. 1017 (U.S. Patent No. 7,755,164) at 6:19-24 (“As tantalum pentoxide layer 314 is a dielectric layer and is between upper electrode 322 and lower electrode 302, tantalum pentoxide layer 314 electrically isolates upper electrode 322 from lower electrode 302 including tantalum layer 312 and titanium layer 310 thus forming capacitor

106.”); Ex. 1018 (U.S. Patent No. 5,837,593) at 1:50-60. (explaining that tantalum pentoxide has been investigated for its high dielectric constant).

Nakano discloses that this antireflective layer is “directly on” an aluminium oxide layer, as shown in annotated Figure 4 below.



Nakano Figure 4 shows a solar cell having “an aluminum oxide coating layer on said major surface” (yellow) and “an antireflective layer further provided over said aluminum oxide coating layer” (green). Ex. 1006, 10:19-29. I antireflective layer is directly on the aluminium oxide layer with no intervening elements present. *Nakano* describes this figure as a principle surface “covered first with an aluminum oxide layer (130), and then with a tantalum pentoxide layer (134). *Id.*, 3:22-25.

Nakano discloses five exemplary structures of solar cells comprising a silicon substrate, aluminium oxide, and an antireflective layer. *Id.*, 3:30-32, 4:53, 5:26, 5:51

and 5:55. Each of these structures discloses an antireflective dielectric layer comprising materials different from the first dielectric layer. For example, tantalum pentoxide Ta_2O_5 is a different material than aluminium oxide (Al_2O_3). Ex. 1003, ¶ 112.

d. Element [12.4]: “hydrogen being embedded into the second dielectric layer;”

Nakano as modified by the teaching of *Hoex* 2006 and the knowledge of a POSITA discloses this limitation.

To the extent this limitation is satisfied by use of reactants that contain hydrogen to form the second dielectric layer, *Nakano* discloses a tantalum pentoxide antireflective layer created by a chemical reaction between hydrogen-containing compounds. Ex. 1006, 4:7-15.

However, to the extent this limitation is satisfied by the presence of hydrogen in the second dielectric layer, *Nakano* does not expressly disclose whether the resulting tantalum pentoxide layer contains hydrogen. Nevertheless, this limitation would have been obvious based on the teachings of *Hoex* 2006 and the knowledge of a POSITA. Specifically, it would have been obvious to replace the tantalum pentoxide antireflective layer in *Nakano* with a “hydrogenated amorphous silicon nitride” anti-reflective layer as taught in *Hoex* 2006.

Nakano (published in 1984) discloses a tantalum pentoxide layer on a first dielectric layer for use as an “antireflective layer.” Ex. 1006, 3:21-24, 5:26, and 5:51-55. *Hoex* 2006 teaches that a “[h]ydrogenated amorphous silicon nitride (*a*-SiN_x:H) **is routinely applied in solar cell production as an antireflection coating.**” Ex. 1003, ¶ 118; Ex. 1007 at 042112-1 (emphasis added); *see also* Ex. 1012 and 1013; *see also* Ex. 1025-1026.

Thus, by 2006, hydrogenated amorphous silicon nitride was routinely used as an antireflective coating in solar cells and would have been an obvious substitute for the tantalum pentoxide layer taught in *Nakano* more than twenty years earlier. This simple substitution of one known element, a hydrogenated amorphous silicon nitride layer, for another, a tantalum pentoxide layer, to achieve predictable results, i.e., known antireflective properties, would have been obvious, or at least obvious to try. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (stating obviousness is appropriate where the claimed subject matter involves “simple substitution of one known element for another” to obtain predictable results.)

Based on the teachings of *Nakano* and *Hoex* 2006, a POSITA would be motivated to substitute the tantalum pentoxide layer of *Nakano* with the hydrogenated amorphous silicon nitride layer of *Hoex* 2006 because *Hoex* 2006 teaches that a hydrogenated amorphous silicon nitride layer drastically improves the

performance of solar cells. Ex. 1003, ¶¶ 118-120. *Hoex* 2006 teaches that hydrogenated amorphous silicon nitride ($a\text{-SiN}_x\text{:H}$) had become the industry standard at its time of publication because its desirable antireflective properties improve solar cell efficiency. Ex. 1007 at 042112-1. A POSITA reviewing *Nakano*, a patent issued over two decades before the publication of *Hoex* 2006, would be motivated to look to current disclosures to determine whether there is a more efficient antireflective coating than tantalum pentoxide, which *Hoex* 2006 does.

Thus, a POSITA practicing *Nakano* in 2006 would have been motivated to use the state-of-the-art antireflective material taught in *Hoex* 2006, i.e. hydrogenated amorphous silicon nitride, in place of *Nakano*'s tantalum pentoxide. Ex. 1003, ¶ 121. The proposed modification applies a known technique to improve a similar device in the same way, to achieve the same goals, with predictable results.

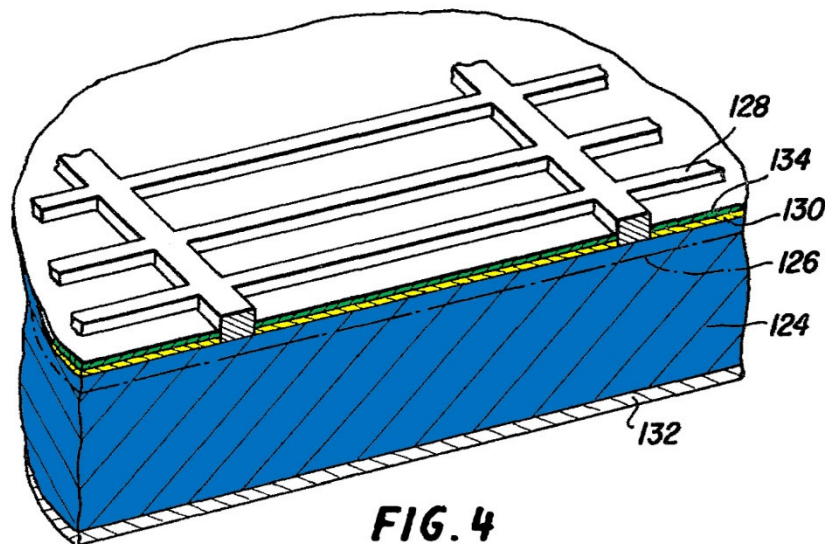
As modified in this manner, *Nakano* with the hydrogenated amorphous silicon nitride anti-reflective layer taught in *Hoex* 2006, would satisfy this limitation. As explained above in Ground 1, a POSITA would understand a layer comprising hydrogenated silicon nitride to be a dielectric layer that contains hydrogen. Ex. 1003, ¶ 120.

- e. **Element [12.5]: “wherein the first dielectric layer has a thickness of less than 50 nm and is interposed**

between the surface of the silicon substrate and the second dielectric layer.”

As discussed above, *Nakano*’s aluminium oxide layer is a first dielectric layer as recited in claim 12. In the preferred embodiment, *Nakano* discloses that this aluminium oxide layer may have a thickness of “about 80 Å,” or about 8 nm. Ex. 1006, 3:33-34; *see also* 4:21-24; and 5:16-17. Additional embodiments disclose thicknesses of “less than 100 Å,” or about < 10 nm. *Id.*, 5:30-31; 5:57-58 and 10:30-32. These disclosed thicknesses are less than 50 nm.

Nakano’s aluminium oxide dielectric layer is interposed between the surface of the silicon substrate and the second dielectric layer in every embodiment, including in the preferred embodiment, as depicted in Figure 4 below. *Id.*, 3:13-16.



Elements 122, 124, 126, and 128, highlighted in blue, are components of the silicon substrate. Ex. 1006 at 3:15-21; Ex. 1003, ¶ 123. Element 130, highlighted in yellow, is an “aluminum oxide layer.” *Id.*, 3:22-24. Element 134, highlighted in green, is a “tantalum pentoxide layer,” which would be substituted with an amorphous hydrogenated silicon nitride layer based on the teaching of *Hoex* 2006 and the knowledge of a POSITA. Because the first dielectric layer (yellow) is both on the surface of the silicon substrate (blue) and has a second dielectric layer (green) on its surface, the first dielectric layer is interposed between the surface of the silicon substrate and the second dielectric layer. Ex. 1003, ¶ 123.

2. Claim 13

a. Element [13.0]: “The solar cell according to claim 12,”

See elements [12.0]-[12.5].

b. Element [13.1]: “wherein the second dielectric layer comprises a material selected from the group consisting of silicon nitride, silicon oxide, and silicon carbide.”

For the same reasons discussed in elements [12.3] and [12.4], *Nakano* as modified by *Hoex* 2006 satisfies this limitation with a second dielectric layer comprising silicon nitride. Ex. 1003, ¶ 125.

3. Claim 14

a. Element [14.0]: “The solar cell according to claim 12,”

See Element [12.0]-[12.5].

b. Element [14.1]: “wherein the first dielectric layer has a thickness of less than 30 nm.”

For the same reasons discussed in element [12.5, *Nakano* as modified by *Hoex 2006* satisfies this limitation with a first dielectric layer having a thickness of less than 10nm, such as about 8 nm. Ex. 1003, ¶ 126. These disclosed thicknesses are less than 30 nm.

E. Ground 4: *Narwankar* Anticipates Claims 12-14 Under 35 U.S.C. § 102

1. Claim 12

(a) Element [12.0]: “A solar cell comprising:”

As explained above, the preamble is not limiting because “solar cell” is a statement of intended use and does not breathe life and meaning into the claim. Ex. 1003, ¶ 130. *Narwankar* addresses semiconductor processing techniques and semiconductor device structures. Ex. 1008, [0003] and Figs. 2A-2F. *Narwankar* anticipates because the structural elements recited in claim 12 are fully disclosed for the reasons provided below and the preamble is not limiting.

(b) Element [12.1]: “a silicon substrate;”

Narwankar discloses a substrate including silicon. Ex. 1003, ¶ 130; Ex. 1007, [0019]. For example, *Narwankar* teaches that the substrate includes materials such as silicon and doped silicon. Ex. 1008, [0019] *Narwankar* further discloses that “substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon e.g., Si<100> or Si<111>, silicon oxide, strained silicon, SOI, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers. *Id.*

(c) Element [12.2]: “a first dielectric layer comprising aluminium oxide on a surface of the silicon substrate; and”

Narwankar discloses a first dielectric layer comprising aluminium oxide on a surface of a substrate. Ex. 1003, ¶ 131-132; Ex. 1008, [0024]. *Narwankar* discloses a substrate including silicon. Ex. 1003, ¶ 130; Ex. 1008, [0019]. *Narwankar* describes a process in which a dielectric layer is deposited on a surface of the substrate. Ex. 1008, FIG. 1, [0020]-[0028]. As shown in annotated FIGS. 1 and 2B below, *Narwankar* deposits a first dielectric layer on a surface of the silicon substrate:

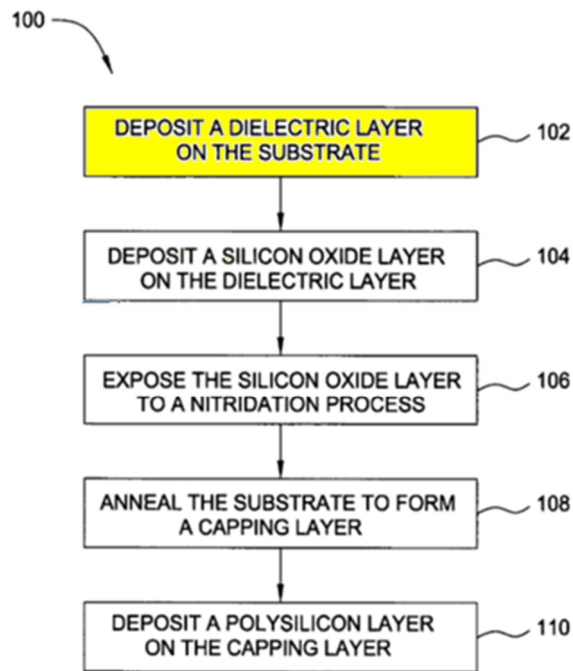
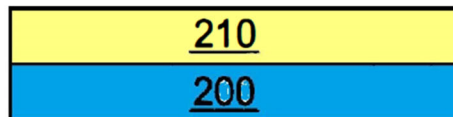


FIG. 1

FIG. 2B



The aluminium oxide dielectric layer 210 (yellow) is deposited on the silicon substrate 200 (blue). *Id.*, [0019], [0022] (“a dielectric layer 210 is deposited on a substrate 200, depicted in FIGS. 2A-2B”) and [0024] (“Dielectric layer 210 is deposited on the substrate surface”).

Narwankar further discloses that the dielectric layer “may have a variety of compositions” and “may include combinations of hafnium, . . . *aluminum*, silicon,

oxygen and/or nitrogen.” *Id.*, [0024]. Specific examples include “aluminum oxides (Al_2O_3 or AlO_x).” *Id.* Indeed, *Narwankar*’s Al_2O_3 layer is identical to the Al_2O_3 layer described in the ’215 patent as an example of the first dielectric layer. Ex. 1001, Abstract and 2:51-52; Ex. 1003, 132-133.

- (d) **Element [12.3]: “a second dielectric layer directly on a surface of the first dielectric layer, materials of the first dielectric layer and the second dielectric layer differing and”**

Narwankar discloses a silicon oxide layer (second dielectric layer) that is deposited directly on a surface of the first dielectric layer. Ex. 1003, ¶¶ 133-136; Ex. 1008 at FIG. 1, [0025]. As shown in annotated Figure 1, *Narwankar* deposits a second dielectric layer on a surface of the first dielectric layer:

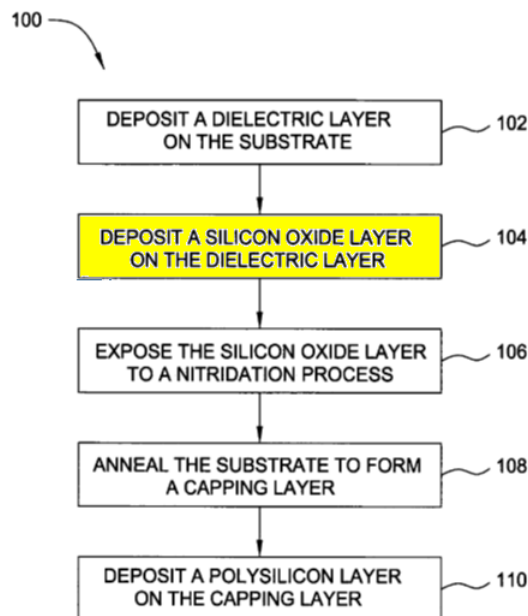


FIG. 1

Step 104 of FIG. 1, depicts the depositing of a silicon oxide layer (second dielectric layer) on a surface of the first dielectric layer, which is first deposited on the substrate as discussed above. As shown in FIGS. 2A-2C, a silicon oxide layer 220 is deposited on dielectric layer 210 by, e.g., an ALD process. See Ex. 1008, FIGs 2A-2C; [0025]-[0027].

The '215 patent recognizes and claims silicon oxide as a dielectric. Ex. 1001, 2:61-65 (“The dielectric passivating layer is composed of two partial layers, of a very thin aluminium oxide-containing layer, which is formed by atomic layer deposition (ALD), and also of a thicker layer made of *silicon oxide*, silicon nitride or silicon carbide.”); 4:64-66; claim 13. *Narwankar*’s silicon oxide layer is a second dielectric layer. Ex. 1003, ¶¶ 133-134, Ex. 1044 (“SiO₂ films synthesized by plasma enhanced chemical vapor deposition (PECVD) already have numerous technological applications. They are used as a dielectric.”).

As discussed above, *Narwankar* discloses that the first dielectric layer includes aluminium oxides (Al₂O₃ or AlO_x) and the second dielectric layer includes silicon oxide. Ex. 1008, [0024] and [0025]. Thus, *Narwankar* discloses a first dielectric layer (made of aluminium oxide) with materials different from the second dielectric layer (silicon oxide). Ex. 1003, ¶ 133-134.

Further, as shown in annotated Figure 2C, *Narwankar*'s silicon oxide layer is located directly on the first dielectric layer:



The silicon oxide layer 220 (green) is depicted as being directly on dielectric layer 210 (yellow). Ex. 1008, [0025]. This figure demonstrates that *Narwankar*'s silicon oxide layer covers the aluminium oxide layer with no intervening elements present. It is also consistent with FIG. 1, which shows the depositing of silicon dioxide on the first dielectric layer. *Id.*, FIG. 1, [0025]-[0027]. Thus, *Narwankar*'s second dielectric layer (silicon oxide layer) is located directly on a surface of the first dielectric layer (aluminium oxide layer). Ex. 1003, ¶¶ 136-137.

For the reasons discussed, *Narwankar*'s formation of silicon oxide layer 220 fully discloses a second dielectric layer that meets Element [12.3]. Additionally, *Narwankar* performs further processing on silicon oxide layer 220 to convert silicon oxide layer 220 to a capping layer 240. See Ex. 1008, [0040] and [0041]. *Narwankar*'s capping layer 240 also is a second dielectric layer that meets Element [12.3] because after nitridation and annealing, capping layer 240 still differs from

the first dielectric layer (aluminium oxide layer) and is still located directly on a surface of the first dielectric layer (aluminium oxide layer).

(e) **Element [12.4]: “hydrogen being embedded into the second dielectric layer;”**

To the extent is limitation is satisfied by use of reactants that contain hydrogen to form the second dielectric layer, *Narwankar* discloses that the process used to form the silicon oxide layer (i.e., second dielectric layer 220) uses hydrogen. Ex. 1003 at ¶ 137-138; Ex. 1008, [0027]. Annotated figure 3 illustrates the process for forming silicon oxide layer 220. *Id.* As shown below, *Narwankar*’s process makes use of gases in several steps:

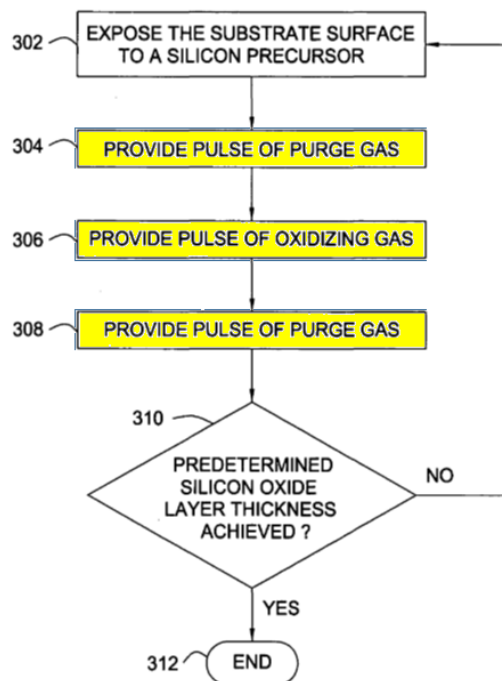


FIG. 3

For the oxidizing gas, *Narwankar* discloses several examples, including “agents, such as in-situ water, oxygen, or **hydrogen**.” *Id.* For the purge gas, *Narwankar* discloses gases that include “helium, argon, nitrogen, **hydrogen**, forming gas, oxygen and combinations thereof.” Ex. 1008, [0027]. *Narwankar* further discloses using silane as a silicon precursor. *Id.*, [0036] (“Exemplary silicon precursors include silanes”).

To the extent is limitation is satisfied by the presence of hydrogen in the second dielectric layer, *Narwankar*’s disclosure of using a silane precursor and using hydrogen gas as oxidizing and purge gases satisfies this limitation. Ex. 1003, ¶ 137-138. Specifically, the use of a silane precursor and hydrogen as an oxidizing gas in forming *Narwankar*’s silicon oxide layer (second dielectric layer) results in hydrogen being found in *Narwankar*’s silicon oxide layer (second dielectric layer). *Id.* Specifically, the presence of hydrogen in the processing chamber during the formation of the silicon oxide layer results in reactions that cause hydrogen to be embedded in the silicon oxide layer. *Id.* 157-160, *see also* Ex. 1030, 2:45-56 (“The silicon oxide layer is formed by flowing a process gas into the substrate processing chamber and forming a high density plasma (i.e., a plasma having an ion density of at least 1×10^{11} ions/cm³) from the process gas to deposit said silicon oxide layer over said substrate. The process gas includes a silane gas, an oxygen-containing source,

an inert gas and a hydrogen-containing source that is selected from the group of H_2 , H_2O , NH_3 , CH_4 , C_2H_6 , or a hydride gas that does not include silicon, boron or phosphorus. The deposited silicon oxide layer has a hydrogen content of less than or equal to 2 atomic percent.”). Thus, through disclosure of using hydrogen to form silicon oxide layer 220, *Narwankar* discloses hydrogen being embedded into the second dielectric layer. *Id.*

Narwankar’s process of using hydrogen containing compounds to form the second dielectric layer 220 is similar to the process described in the ’215 patent. *See* Ex. 1007, [0027] and [0036] (“Exemplary silicon precursors include silanes”). The ’215 Patent discloses the use of silane (SiH_4), ammonia (NH_3), and methane (CH_4) as reactants to create the second dielectric layer, (Ex. 1001, 5:6-14, 7:61-64), which is described as having embedded hydrogen. For these reasons, *Narwankar*’s silicon oxide layer 220 fully anticipates Element [12.4]. Ex. 1003, ¶ 137-138.

The hydrogen in *Narwankar*’s silicon oxide layer 220 (as discussed above) remains present in *Narwankar*’s capping layer 240 after conversion. Moreover, *Narwankar* also describes hydrogen being used in converting *Narwankar*’s silicon oxide layer 220 to capping layer 240. In particular, referencing silicon oxide layer 220 and the process of FIG.1, step 106, *Narwankar* indicates that “the silicon oxide layer is exposed to a nitridation process.” Ex. 1008, [0038]. *Narwankar* explains

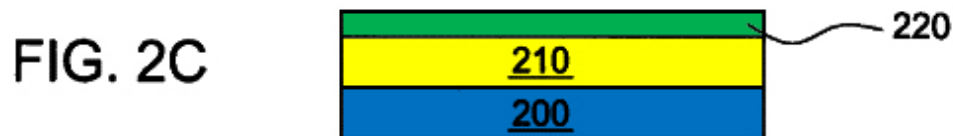
that, during the DPN (decoupled plasma nitridation) process, silicon oxide layer 220 is bombarded with gases that include hydrogen, such as NH_3 , hydrazines (e.g., N_2H_4 or MeN_2H_3), amines (e.g., Me_3N , Me_2NH or MeNH_2), and anilines (e.g., $\text{C}_6\text{H}_5\text{NH}_2$). *Id.*, [0039]. *Narwankar* also discloses a nitridation process by ALD using NH_3 . *Id.*, [0040]. The presence of hydrogen-containing compounds in the processing chamber during the formation of *Narwankar*'s capping layer 240 (second dielectric layer) results in hydrogen being found in the resulting dielectric layer. Ex. 1003 ¶ 139.

Again, *Narwankar*'s process of using hydrogen containing compounds to form the second dielectric layer 240 is similar to the process described in the '215 patent. *See* Ex. 1009, [0027], [0036] ("Exemplary silicon precursors include silanes") and [0039] ("other ***nitrogen-containing*** gases may be used to form the nitrogen plasma, such as NH_3 "). Specifically, the '215 Patent discloses the use of silane (SiH_4), ammonia (NH_3), and methane (CH_4) as reactants to create the second dielectric layer, Ex. 1001, 5:6-14, 7:61-64, which is described as having embedded hydrogen. For these reasons, *Narwankar*'s capping layer 240 also anticipates Element [12.4]. Ex. 1003, ¶ 140.

- (f) **Element [12.5]: “wherein the first dielectric layer has a thickness of less than 50 nm and is interposed between the surface of the silicon substrate and the second dielectric layer.”**

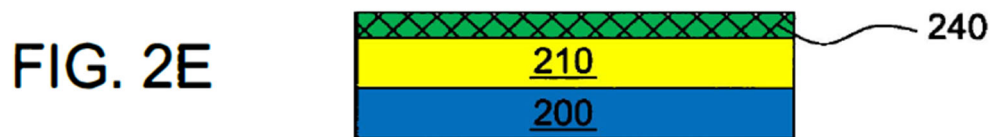
Narwankar discloses that the first dielectric layer 210 has a thickness from about 1 nm to 100 nm, i.e., 2 nm to 50 nm. Ex. 1003 ¶ 141; Ex. 1008, [0022]. For example, *Narwankar*’s first dielectric layer 210, produced according to the process of FIG. 1, has a thickness of less than 50 nm: “Dielectric layer 210 is generally deposited with a film thickness from about 10 Å to about 1,000 Å [1 nm to 100 nm], preferably from about 20 Å to about 500 Å [2 nm to 50 nm] and more preferably from about 50 Å to about 200 Å [5 nm to 20 nm], for example, about 100 Å [10 nm].” *Id.*; Ex. 1003 ¶ 141; *see also* Ex. 1043, xiv.

Narwankar’s first dielectric layer 210 also is interposed between the surface of the silicon substrate and the second dielectric layer (e.g., *Narwankar*’s silicon oxide layer 220 or capping layer 240). Ex. 1003, ¶ 142. As shown in FIG. 2C (reproduced below), *Narwankar*’s first dielectric layer 210 is interposed between the surface of silicon substrate 200 and silicon oxide layer 220:



Annotated FIG. 2C (above), shows the dielectric silicon oxide layer 220 (green) on the first dielectric layer 210 (yellow). Ex. 1008, FIG. 2C, [0025]-[0027]. These layers are deposited on a substrate 200 (blue). *Id.* at [0022]. Because the first dielectric layer 210 is directly underneath the second dielectric silicon oxide layer 220 and directly on the surface of the substrate 200, which comprises silicon (*see* Element [12.1]), the first dielectric layer 210 is interposed between the surface of the silicon substrate and the second dielectric layer. *Id.*, FIG. 2C, [0025]-[0027]; *see also id.*, FIG.1.

Additionally, as shown in FIG. 2E (reproduced below), *Narwankar's* first dielectric layer 210 is interposed between the surface of silicon substrate 200 and capping layer 240. *See* Ex. 1008, [0040] and [0041].



2. Claim 13

(a) **Element [13.0]: “The solar cell according to claim 12,”**

See Elements [12.0]-[12.5].

(b) **Element [13.1]: “wherein the second dielectric layer comprises a material selected from the group**

consisting of silicon nitride, silicon oxide, and silicon carbide.”

See Element [12.3]. *Narwankar* discloses this limitation because it discloses a silicon oxide second dielectric layer. Ex. 1003, ¶¶ 133-134 and 143; Ex. 1008, Figs. 1, 2C, and [0025]-[0027]. *Narwankar* discloses a second dielectric layer as silicon oxide layer 220. *Narwankar* discloses that this layer comprises silicon oxide. *Id.* Additionally, capping layer 240 also meets this limitation because it comprises silicon oxide and silicon nitride. *See* Ex. 1008, [0040] and [0041].

3. Claim 14

(a) **Element [14.0]: “The solar cell according to claim 12,”**

See Elements [12.0]-[12.5].

(b) **Element [14.1]: “wherein the first dielectric layer has a thickness of less than 30 nm.”**

See Element [12.5]. *Narwankar*’s first dielectric layer 210 has a thickness from about 1 nm to 100 nm. Ex. 1003, ¶ 144 and 144; Ex. 1008, [0022]. *Narwankar* also describes a preference for a thickness of less than 30 nm: “Dielectric layer 210 is generally deposited with a film thickness from about 10 Å to about 1,000 Å [1 nm to 100 nm], preferably from about 20 Å to about 500 Å [2 nm to 50 nm] and *more preferably* from about 50 Å to about 200 Å [5 nm to 20 nm], *for example, about 100 Å* [10 nm].” *Id.*, [0022]; Ex. 1003, ¶ 141 and 144; Ex. 1043, xiv.

F. Ground 5: Claims 12-14 Are Obvious Over *Narwankar* alone or in view of *Tan*

As discussed in Ground 4, *Narwankar* describes every element of claims 12-14, anticipating and rendering these claims unpatentable. If Hanwha argues that *Narwankar* fails to teach (1) a solar cell as recited in Element [12.0], and/or (2) hydrogen being embedded into the second dielectric layer as recited in Element [12.5], these elements would have been obvious to a POSITA based on the teachings of *Narwankar*, *Tan*, and the knowledge of a POSITA. Ex. 1003, ¶ 146.

1. Claim 12

a. Element [12.0]: “A solar cell comprising:”

As explained above, the preamble of claim 12 is not limiting. But if the preamble is construed to be limiting, it would have been obvious to a POSITA, based on the teachings of *Narwankar* and the knowledge of a POSITA, to apply *Narwankar*’s semiconductor design to solar cell.

Narwankar addresses semiconductor processing techniques and electronic device structures. Ex. 1008, [0003]. *Narwankar*, however, does not disclose a use for this semiconductor design including dielectric and silicon layers. Because *Narwankar* fails to disclose a use for this semiconductor design, a POSITA would have been motivated to explore potential uses for *Narwankar*’s design and would

have found it obvious to use *Narwankar*'s semiconductor device in a solar cell. Ex. 1003, ¶ 153.

Specifically, a POSITA would have known that semiconductor devices similar to *Narwankar*'s design were used in solar cells. Ex. 1003, ¶ 147-153. As discussed above in Ground 4, *Narwankar*'s semiconductor design includes a silicon substrate, covered by a first dielectric layer comprising aluminum oxide, which is in turn covered by a second dielectric layer differing from the first dielectric layer. As discussed above in Grounds 1 and 3, both *Agostinelli* '086 and *Nakano* disclose such a semiconductor design with a silicon substrate covered by a first dielectric layer comprising aluminum oxide, which is in turn covered by a second dielectric layer differing from the first dielectric layer. It would have been obvious for a POSITA to apply such a semiconductor design to a solar cell based on the teachings from *Agostinelli* '086 and *Nakano*. Ex. 1003, ¶¶ 147-153; Ex. 1005, [0007]; Ex. 1006, 2:28-29.

Because *Narwankar*'s semiconductor design was known to be used for solar cells, a POSITA would have found it obvious to employ *Narwankar*'s semiconductor design in a solar cell, particularly given *Narwankar*'s failure to describe a use for this design. Ex. 1003, ¶ 153. Indeed, a POSITA would have seen a solar cell as being one of the possible known semiconductor devices that would

have been available for using *Narwankar*'s semiconductor design. Ex.1003, ¶ 153. Thus, based on the teachings of *Narwankar* and the knowledge of a POSITA, a POSITA would have found it obvious to try using *Narwankar*'s semiconductor design in a solar cell and would have had a reasonable expectation of success. Ex. 1003, ¶¶ 147-153.

b. Element [12.4]: “hydrogen being embedded into the second dielectric layer;”

See Ground 4, Element [12.4]. As discussed in Ground 4, *Narwankar* discloses this limitation. To the extent *Narwankar* lacks explicit disclosure of the presence of hydrogen in the second dielectric layer, *Narwankar*'s disclosure of using a silane precursor and using hydrogen gas as oxidizing and purge gases at least implicitly discloses and renders obvious this limitation. *See* Ex. 1008, [0036] (“Exemplary Silicon precursors include Silanes”) and [0027] (The oxidizing gas may include several agents, such as in-situ water, oxygen or hydrogen...Suitable carrier gasses or purge gases may include helium, argon, nitrogen, hydrogen, forming gas, oxygen and combinations thereof.”) Specifically, a POSITA would have found it obvious that the use of a silane precursor and hydrogen gas would result in hydrogen being found in the second dielectric layer. Ex. 1003, ¶ 159-162.

For instance, a POSITA would have found it obvious that *Narwankar*'s silicon oxide layer 220 includes hydrogen. *See* Ex. 1003, 157; Ex. 1028-1029, As discussed

above, *Narwankar* describes using a silane precursor with hydrogen-containing gas to form silicon oxide layer 220. Ex. 1008, [0027], [0030]-[0036] and FIG. 3. A POSITA would have understood that the presence of hydrogen in the processing chamber during the formation of *Narwankar*'s silicon oxide layer 220 would result in reactions that would cause hydrogen to be found in the silicon oxide layer. Ex. 1003, ¶ 157-160; Ex. 1030, 2:45-56; Ex. 1032-1037. Because *Narwankar* discloses the use of hydrogen in forming silicon oxide layer 220 and it was known that hydrogen embeds into silicon oxide layers when present in the processing chamber, a POSITA would have found that *Narwankar* at least implicitly discloses or renders obvious embedded hydrogen in silicon oxide layer 220. Ex. 1003, ¶ 157-160. Thus, based on the teachings of *Narwankar* and the knowledge of a POSITA, a POSITA would have found it obvious that *Narwankar*'s silicon oxide layer 220 includes embedded hydrogen.

Both *Narwankar* and *Tan* are aimed at solving the same technical problem: how to better deposit a silicon oxide layer in view of the smaller feature sizes of modern semiconductor devices. See Ex. 1008, [0003] ("As the geometries of electronic devices continue to shrink and the density of devices continues to increase, the size and aspect ratio of the features are becoming more aggressive, e.g., feature sizes of 0.07 microns and aspect ratios of 10 or greater are being considered.

Accordingly, conformal deposition of materials to form these devices is becoming increasingly important.”) and Ex. 1030, 1:35-43 (“Semiconductor device geometries have dramatically decreased in size since such devices were first introduced several decades ago. Smaller feature sizes have resulted in the presence of increased aspect ratio gaps for some applications, for example, between adjacent conductive lines or in etched trenches. The aspect ratio of a gap is defined by the ratio of the gap’s height or depth to its width. These spaces are difficult to fill using conventional CVD methods.”) Additionally, both *Narwankar* and *Tan* teach forming a silicon oxide layer with a silane gas (SiH_4), an oxygen-containing source such as oxygen gas (O_2), an inert gas such as Argon gas (Ar) and a hydrogen-containing source such as hydrogen gas (H_2). Ex. 1008, [0036] (“Exemplary silicon precursors include silanes”), [0027] (“The oxidizing gas may include several agents, such as in-situ water, oxygen or hydrogen . . . Suitable carrier gasses or purge gases may include helium, argon, nitrogen, hydrogen, forming gas, oxygen and combinations thereof.”) and Ex. 1030, 2:57-59 (“the present invention forms an undoped silicon oxide layer (USG) from a process gas consisting of SiH_4 , O_2 , Ar and H_2 .”).

A POSITA would have found *Tan*’s process of forming a silicon oxide layer to be similar to *Narwankar*’s process of forming silicon oxide layer 220 and a suitable solution for forming *Narwankar*’s silicon oxide layer Ex. 1003, ¶ 161-162.

In fact, a POSITA would have seen substitution of *Narwankar*'s process for *Tan*'s process as being a simple substitution of one known process for another to obtain predictable results. Ex. 1003, ¶ 161-162. Indeed, as Dr. Clemens explains, a POSITA could have substituted *Tan*'s process of forming silicon oxide for *Narwankar*'s process of forming silicon oxide, and a POSITA would have found the results of the substitution to have been predictable. *Id.*

Moreover, *Tan* describes benefits of its process of forming a silicon oxide layer that would have motivated a POSITA to employ *Tan*'s process in forming *Narwankar*'s silicon oxide layer 220. Ex. 1003, ¶ 163-164 For example, *Tan* describes an “improved method of depositing silicon oxide films” that is “useful for the manufacture of integrated circuits having minimum feature sizes of 0.18 microns or less.” Ex. 1030, 2:35-56. *Tan*'s process “can increase the gap-fill capability of the film without leading to film instability.” Ex. 1030, 11:40-46. Indeed, *Tan*'s process uses flow rates that do not “lead to film instability” and avoid other disadvantages. Ex. 1030, 13:26-46. For example, with *Tan*'s process, the silicon oxide film does not become “silicon rich,” “exhibit[] poor electrical breakdown characteristics,” and does not have “an undesirably high refractive index.” *Id.* Thus, to achieve these benefits (e.g., film stability) of *Tan*'s process and to avoid the disadvantages mentioned above, a POSITA would have been motivated to employ

Tan's process in forming *Narwankar*'s silicon oxide layer 220, which results in a silicon oxide layer containing 1.5–1.6 atomic percent hydrogen. *See* Ex. 1003, ¶ 161-162; Ex. 1030, 13:54-57.

Narwankar also renders obvious embedding hydrogen in the nitridation process used in converting *Narwankar*'s silicon oxide layer 220 to *Narwankar*'s capping layer 240. In particular, referencing silicon oxide layer 220 and the process of FIG.1, step 106, *Narwankar* indicates that “the silicon oxide layer is exposed to a nitridation process.” Ex. 1008, [0038]. *Narwankar* explains that, during the DPN (decoupled plasma nitridation) process, “silicon oxide layer 220 is bombarded with gases with that include hydrogen, such as NH_3 , hydrazines (e.g., N_2H_4 or MeN_2H_3), amines (e.g., Me_3N , Me_2NH or MeNH_2), and anilines (e.g., $\text{C}_6\text{H}_5\text{NH}_2$.) *Id.* at [0039]. *Narwankar* also discloses, in another example, a nitridation process by ALD using NH_3 . *Id.* at [0040]. A POSITA would have understood that the presence of hydrogen in the form of ammonia (NH_3) during nitridation would cause the incorporation of hydrogen in the resulting layer. Ex. 1003, ¶ 163. For example, it was shown that nitridation with ammonia (NH_3) results in a silicon oxide layer with hydrogen. *See* Ex. 1029 and Ex. 1038.

Because *Narwankar* discloses the use of hydrogen in forming capping layer 240 and it was known that hydrogen is incorporated into silicon oxide layers when

performing a nitridation process, a POSITA would have found that *Narwankar* at least implicitly discloses or renders obvious embedded hydrogen in capping layer 240 for these additional reasons. Thus, based on the teachings of *Narwankar* and the knowledge of a POSITA, a POSITA would have found it obvious that *Narwankar*'s capping layer 240 also includes embedded hydrogen.

Further, *Narwankar* in view of *Tan* satisfy elements [12.1]-[12.3] and [12.5] for the same reasons explained in Ground 4, claim 12.

2. Claim 13

Narwankar in view of *Tan* satisfy claim 13 for the same reasons explained in Ground 4, claim 13.

3. Claim 14

Narwankar in view of *Tan* satisfy claim 13 for the same reasons explained in Ground 4, claim 14.

VI. MANDATORY NOTICES

A. Real Party-in-Interest

The real parties-in-interest are REC Americas, LLC, REC Solar Pte. Ltd., REC Solar Holdings AS, JinkoSolar Holding Co., Ltd., JinkoSolar (U.S.) Inc., Jinko Solar (U.S.) Industries Inc., Jinko Solar Co., Ltd., Zhejiang Jinko Solar Co., Ltd., and Jinko Solar Technology Sdn. Bhd.

B. Related Matters

The '215 patent is the subject of the following cases: *Certain Photovoltaic Cells and Products Containing Same*, Inv. No. 337-TA-1151 (U.S.I.T.C.), filed on March 4, 2019; *Hanwha Q CELLS & Advanced Materials Corp. v. JinkoSolar Holding Co. Ltd. et al*, No. 1:19-cv-00450-MN (D. Del.), filed March 5, 2019; *Hanwha Q CELLS & Advanced Materials Corp. v. LONGi Green Energy Technology Co., Ltd. et al.*, No. 1:19-cv-00451-MN (D. Del.), filed March 5, 2019; and *Hanwha Q CELLS & Advanced Materials Corp. v. REC Solar Holdings AS et al.*, No. 1:19-cv-00452-MN (D. Del.), filed March 5, 2019; and *LONGi Green Energy Technology Co., Ltd. et al v. Hanwha Q CELLS & Advanced Materials Corp.* IPR2019-01072 (P.T.A.B. 2019).

C. Lead and Back-Up Counsel and Service Information

Lead Counsel for REC Solar Petitioners

Joshua L. Goldberg (Reg. No. 59,369; Tel. (202) 408-6092; joshua.goldberg@finnegan.com), attorney at Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., 901 New York Avenue, N.W., Washington, DC 20001-4413.

Backup Counsel for REC Solar Petitioners

James R. Barney (Reg. No. 46,539; Tel. (202) 408-4412; james.barney@finnegan.com), attorney at Finnegan, Henderson, Farabow, Garrett

& Dunner, LLP, 901 New York Avenue, NW, Washington, DC 20001-4413;

Alexander Poonai (Reg. No. 76,577; Tel. (202) 408-4315; alexander.poonai@finnegan.com), attorney at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, 901 New York Avenue, NW, Washington, DC 20001-4413.

Backup Counsel for Jinko Solar Petitioners

Jeremy Monaldo (Reg. No. 58,680; Tel. (202) 626-7717; monaldo@fr.com), attorney at Fish & Richardson P.C., 1000 Maine Ave SW, Washington, DC 20024;

Linhong Zhang (Reg. No. 64,749; Tel. (202) 626-7786; lwzhang@fr.com), attorney at Fish & Richardson P.C., 1000 Maine Ave SW, Washington, DC 20024.

Petitioner consents to e-mail service at the above e-mail addresses.

VII. CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

This Petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word 2016, it contains 13,173, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, Certification Under §42.24(d), and Certificate of Service.

VIII. GROUNDS FOR STANDING

Petitioner certifies the '215 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the '215 patent challenging the patent claims on the grounds identified in this petition.

IX. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED

Petitioners request *inter partes* review and cancelation of claims 12-14. These claims are unpatentable under both 35 U.S.C. § 102 and 35 U.S.C. § 103 based on each of the grounds above. The claim construction, reasons for unpatentability, and specific evidence supporting this request are detailed herein.

X. CONCLUSION

For these reasons, claims 12-14 are unpatentable, so trial should be instituted and the claims should be cancelled. An electronic payment covering the request and post-institution fees is being made at the time of filing this petition. If there are any additional fees due in connection with the filing of this paper, please charge the required fees to Deposit Account No. 06-0916.

Date: June 3, 2019

Respectfully submitted,

/Joshua L. Goldberg/
Joshua L. Goldberg,
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that the foregoing **Petition for *Inter Partes* Review, the associated REC-Jinko Exhibits 1001-1030; 1032-1038; 1043-1044, and Petitioners' Powers of Attorney** were served on June 3, 2019, by overnight courier at the following address of record for the subject patent.

Birch, Stewart, Kolasch & Birch, LLP
Attn: Chad J. Billings, Esq.
8110 Gatehouse Road
Suite 100 East
Falls Church, VA 22042
Telephone: (703)205-8000

Dated: June 3, 2019

By: /Lauren K. Young/
Lauren K. Young
Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.