

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Seo et al.  
U.S. Pat. No.: 9,293,664 Attorney Docket No.: 38191-0005IP1  
Issue Date: Mar. 22, 2016  
Appl. Serial No.: 14/815,433  
Filing Date: Jul. 31, 2015  
Title: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE  
AND METHOD OF FABRICATING THE SAME

### **DECLARATION OF ERIC BRETSCHNEIDER, Ph.D.**

I, Eric Bretschneider, Ph.D., of Grapevine, TX, declare that:

#### **I. ASSIGNMENT**

1. I have been retained as a technical expert by counsel on behalf of LG Innotek Co., Ltd. (“LGI” or “Petitioner”). I understand that LGI is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 9,293,664 (“the ’664 patent”) (LGI1001).

2. I have been asked to provide my independent analysis of the ’664 patent in light of the prior art publications cited below.

3. I am not, and never have been, an employee of LGI. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’664 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added

compensation based on the outcome of any IPR or other proceeding involving the '664 patent.

## **II. QUALIFICATIONS**

4. My qualifications for forming the conclusions set forth in this report are summarized here and explained in more detail in my curriculum vitae, which is attached as Appendix A, and which includes a list of all publications authored in the previous 10 years.

5. I have over 25 years of experience with lighting and LEDs, including a comprehensive background on a full range of LED production and lighting technologies, including Metal-Organic Chemical Vapor Deposition (“MOCVD”) hardware/process design and development, epitaxial structure design and development, LED chip design and fabrication, LED chip and package testing and reliability, optical design, thermal management (including heat dissipation by free and forced convection, conduction and radiation), color conversion, and SSL fixture/lamp design, integration, reliability and manufacturing.

6. Throughout the course of my career I have designed and developed dozens of LED chip designs and packages. I have also designed and transferred into manufacturing over 150 different LED-based lighting products ranging from replacement bulbs to integrated fixtures and luminaires, and thermal management

of heat generated by the LEDs was a factor I addressed from both design and implementation standpoints for all of those products.

7. I am currently the Chief Technology Officer at EB Designs & Technology. In that capacity, I am (among other things) responsible for the design of solid-state lighting technologies and fixtures, new test development, reverse engineering of competitive products and reliability testing for clients ranging from startups to Fortune 100 companies. The span of this work ranges includes issues and development at the LED chip, LED package level as well as high levels of integration up to and including full fixtures. Other work includes test method development and reliability at the LED chip, package and fixture level.

8. I also serve as Chief Technology Officer for QuarkStar. QuarkStar is a technology development company that has developed a portfolio of over 150 patents related to various technologies related to solid state lighting. In this role I lead the development and refinement of technologies and manufacturing methods related to LED packages and fixtures. In this role I also, negotiate technology license agreements, and provide technical support to licensees.

9. I am also a member and current chair of the University of Florida Department of Chemical Engineering Advisory Board. I have been a Conference Chair for LED Measurement and Standards. I am also a member of a number of professional societies, including SPIE (International Society for Optics and

Photonics), MRS (Materials Research Society), OSA (Optical Society of America), ASABE (American Society of Agricultural and Biological Engineers), ASHS (America Society for Horticultural Science) and the IES (Illuminating Engineering Society). Inside the IES, I am a founding member of the Science Advisory Panel which has oversight over all testing and technical committees and work groups inside the IES. I am also a member of the Test Procedures Committee of the IES and the chair of the Solid-State Lighting subcommittee.

10. I have led a number of work groups in developing and improving standards related to solid-state lighting and testing procedures used for both traditional and solid-state lighting components, modules and fixtures. Notably, I developed the method of Differential Chromaticity Analysis which is the first predictive model for chromaticity shift behavior of LED packages and fixtures.

11. I also lead the work group responsible for increasing the scope of ANSI/IES TM-21 which is the internationally accepted standard for predicting flux maintenance of LED packages.

12. Prior to my position at EB Designs & Technology, I served as the Director of Engineering at HeathCo, LLC. In that capacity, I was responsible for advanced technology/product development related to solid-state lighting including LED lighting, sensors, notifications, and control products. In this role I was responsible for ensuring products met all requirements (light output/distribution

pattern, thermal management including convective heat dissipation arrangements, safety and control integration) for big box retailers.

13. Prior to my position as Director of Engineering at HeathCo, I was positioned at the Elec-Tech International Co., Ltd., a multi-billion dollar solid-state lighting startup company headquartered in mainland China. There I held the concurrent positions of Chief Engineer at ETi Lighting Research Institute and VP of Research and Development at ETi Solid State Lighting. In this capacity, my responsibilities included developing all technology and product roadmaps for markets in North America, China, Europe, and Japan. In this role, I led and trained a staff of over 100 engineers, technicians and designers in the methods and procedures for designing solid-state lighting products. This included determining proper light sources for desired spectral content, testing LED package reliability, designing strategies for thermal management of lamps and fixtures that utilized LED light sources, optical design, control integration and electrical drive circuits. I also had technical responsibility for LED chip design, package design and light engine design for products intended for the domestic Chinese market as well as markets in Japan, North America and Europe.

14. Between 2008 and 2011, I was positioned at Lighting Science Group Corp., first as a product development manager, then as VP of Research, and my responsibilities included developing advanced LED lighting models for LED

product development and production control. My responsibilities included thermal management design/analysis and optical design of LED lighting components and fixtures as well as testing/benchmarking internal and external products, and development of test and reliability procedures and equipment. I was also responsible for destructive testing and reverse engineering efforts as well as intellectual property (IP) review.

15. Upon the acquisition of Lamina, I assumed the role of technology lead for all Lamina products including LED packages and light engines.

16. Between 2004 and 2008, I was positioned at Toyoda Gosei North America, where I was a sales manager and was the sole technical support for Toyoda Gosei LED die and packages in the Western Hemisphere. My responsibilities included managing and developing LED die and package sales accounts in North America and Europe. In my role as technical support for the Western Hemisphere, I provided knowledge and experience necessary for customers to use LED die and packages. Regarding LED die, this included aiding and supporting customers with optical design and thermal-management design of LED packages as well as phosphor conversion materials and techniques. For LED packages, my responsibilities included testing protocols, reliability evaluation, as well as thermal-management analysis, design and testing as well as optical design

of LED light engines and fixtures. I also provided input and guidance to the research and development group for new LED chip and package design.

17. Between 2003 and 2004, I was Director of Solid State Lighting Engineering at Beeman Lighting, and my responsibilities included optical design and thermal-management design (including convective heat dissipation solutions) of LED light engines and fixtures.

18. Between 1998 and 2003 I held a position at Uniroyal Optoelectronics, where I was Team Leader for the Epitaxial Growth and Materials Characterization areas. I later held the position of Director of Intellectual Property, University Relations and Government contracts. From 1999 through 2003 I had a concurrent assignment as a Senior Epi Scientist. Throughout these roles I supported all sales efforts for LED die and package sales. I had primary responsibility for thermal-management design and analysis as well as optical design of LED die and packages. A part of my responsibility in supporting sales of LED die and packages included thermal-management design and analysis as well as optical design of packages for LED die customers and thermal-management modeling and optical modeling of LED modules and fixtures for LED package customers, and that work included analysis and consideration of all modes of heat dissipation including conduction, convection and radiation. My interactions with customers and potential customers included design work on a number of projects that would still

be considered technically challenging today. These included exterior lighting for the U.S. Navy DDX (Stealth Destroyer) program, a lighting module for the U.S. Air Force for use on the XSS-11 satellite, an implantable light source for the Paul Allen Foundation and linear chip on board (COB) lighting modules for the passenger cabin of the Boeing 737. I also worked on an internal project that developed a liquid based cooling system for LEDs that could dissipate more than 20 Watts of heat per square millimeter which is an order of magnitude greater heat flux than what is generated by current state of the art LEDs. Further, working with a sister company known as Norlux, I also helped design the "Hex" which was one of the first COB LED products released and which incorporated from 40 to well over 100 LED chips and operated with electrical power input of 1 to 5 watts. I was also responsible for reverse engineering and destructive testing of internal and competitive products.

19. From 1996 to 1998 I worked at Emcore Corporation as a Process Engineer. There I was responsible for qualifying MOCVD capital equipment for production and manufacturing process development for epitaxial structures. Here I developed an MOCVD tool qualification protocol that became the standard method used by all Field Engineers to quantify the performance characteristics of new or existing MOCVD growth systems. I also developed epitaxial structures and the



corresponding processes to produce the structures. Some of the processes I developed included both AlInGaP and GaN based LED structures.

20. I have also authored and presented a total of more than 30 publications, presentations, and seminars, and I am a named inventor on 30 issued patents and over 25 pending patent applications.

21. I earned a Ph.D. in Chemical Engineering from the University of Florida in 1997, where my graduate work focused on development of solid-state lighting devices and device structures, including novel silicon based visible LEDs and sulfide based TFELD structures and zinc selenide blue LEDs. During my time as a graduate student, I also completed fluid flow and thermal management studies while building custom or modifying commercial MOCVD systems for growth of specific compound semiconductor material systems.

22. As a graduate student I developed new developed epitaxial structures for both ZnSe based blue LEDs and silicon based LEDs. I also developed fabrication methods to produce finished LED die which could be tested and incorporated into LED package structures.

23. In 1989, I worked for Shell Oil Corporation in Norco, LA. I was tasked with modeling heat exchanger performance that used convective heat dissipation for the crude oil distillation column in order to identify cost saving opportunities. I developed an improved model for determining the operating

efficiency of heat exchange units that determined the economic impact on different operating conditions. The model was designed to be compatible with all major operating units on site and resulted in costs savings of over \$20 million/year at the Norco Facility. My work was quickly adopted throughout the entire corporation and has resulted in sustained annual cost savings of approximately \$500 million/year.

24. I am the current chair of the Solid-State Lighting subcommittee of the IES (Illuminating Engineering Society) Test Procedures Committee. This group developed the internationally accepted standards related to testing and reliability standards for LED lighting products.

25. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '664 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time.

### **III. LEGAL PRINCIPLES**

26. In forming my analysis and conclusions expressed in this declaration, I have applied the legal principles described in the following paragraphs, which were provided to me by counsel for the Petitioner.

**A. Anticipation**

27. I have been informed that a patent claim is invalid as anticipated if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, I understand that if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

28. I have been informed that a claim is invalid if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application. I have also been informed that a claim is invalid if an invention described by that claim was described in a U.S. patent granted on an application for a patent (or in a published application for a U.S. patent) that was filed by another in the U.S. before the date of invention for such a claim.

**B. Obviousness**

29. I have been informed that a patent claim is invalid as "obvious" in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"; refer to ¶ 34 below), taking into account (1) the scope and content of the prior art, (2) the

differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.

30. While I do not know the exact date that the alleged invention claimed in the '664 patent was made, I do know that the '664 patent claims priority to foreign applications filed as early as September 24, 2010 (LGI1001 at cover page). For purposes of my analysis here, I have applied a date of September 24, 2010 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than September 24, 2010 (especially given the earlier publication or filing dates of the prior art in ¶ 36, below).

31. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the

knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

### **C. Claim Construction**

32. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. *Id.* I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

33. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). Because I do not know at what date the alleged invention was made, I have generally used the date of September 24, 2010, for reasons explained in ¶ 30 (above). However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the late 2000s.

#### **IV. PERSON OF ORDINARY SKILL IN THE ART**

34. Based on my knowledge and experience in the field and my review of the '664 patent and its file history, I believe a person of ordinary skill in the art ("POSITA") at the time of the earliest possible priority date of the '664 patent would have had either a Bachelor of Science in electrical engineering, physics, or a related field, with at least 2-5 years of experience in research, design, or development of LED design and/or manufacturing. Additional education might substitute for some of the experience, and substantial experience might substitute for some of the educational background. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

## **V. MATERIALS CONSIDERED**

35. My analyses set forth in this declaration are based on my experience in the field of LED devices. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the late 2000s and specifically during the time before the alleged priority date (September 24, 2010) for the '664 patent, and I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

36. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the alleged priority date for the '664 patent; my own knowledge and experiences gained from my work experience in the fields of physics and LED devices generally; my experience in teaching and advising others in those subjects; and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 9,293,664 to Seo, et al. (“the '664 Patent”) (LGI1001)
- Prosecution History of the '664 Patent (LGI1003)
- Reexamination History of U.S. Patent No. 9,070,851 (LGI1004)

- U.S. Patent Pub. No. 2010/0117111 to Illek et al. (LGI1005)
- U.S. Patent No. 6,066,861 to Hohn et al. (LGI1006)
- U.S. Patent Pub. No. 2005/0194605 to Shelton et al. (LGI1007)
- U.S. Patent Pub. No. 2003/0021113 to Begemann (LGI1008)
- U.S. Patent Pub. No. 2009/0283787 to Donofrio et al. (LGI1009)
- JP Publication JP 2009-88299 to Sano et al. (LGI1010)
- Certified English Translation of Sano (LGI1011)<sup>1</sup>
- U.S. Patent No. 6,693,352 to Huang et al. (LGI1012)
- U.S. Patent No. 7,554,126 to Higashi et al. (LGI1013)
- Excerpt from ANSI/IES RP-16-10: Nomenclature and Definitions for Illuminating Engineering (LGI1014)
- U.S. Patent No. 6,448,657 to Dorleans (LGI1015)

37. Although this declaration refers to selected portions of the cited references for the sake of brevity, it should be understood that these are examples, and that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references

---

<sup>1</sup> Because Sano (LGI-1010) is in Japanese, I will refer to the English translation (LGI-1011) in my analysis.

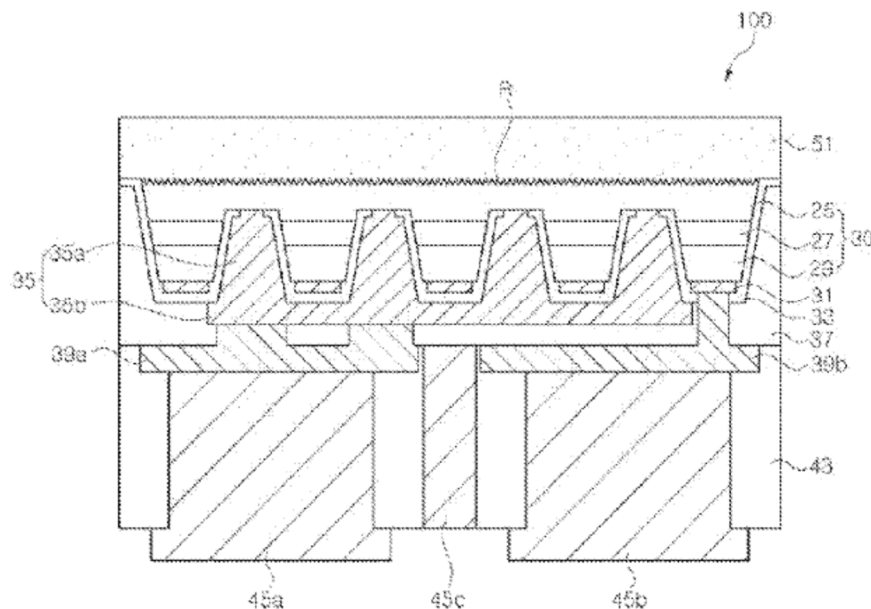


themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties.

## VI. BACKGROUND INFORMATION

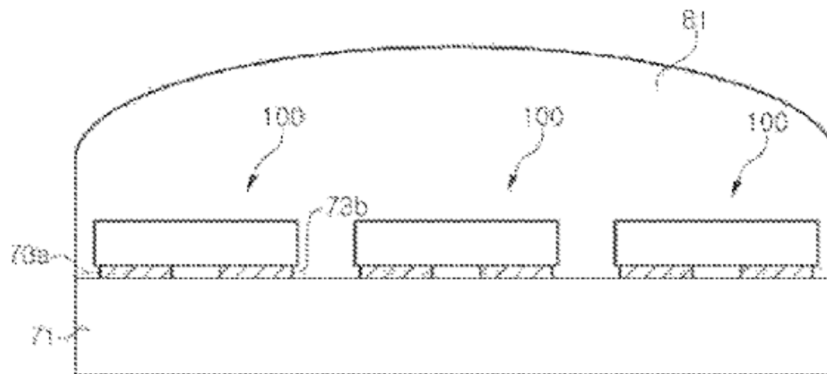
### A. Overview of the '664 Patent

38. The '664 Patent generally “relates to a light emitting diode package and a method of fabricating the same and, more particularly, to a wafer-level light emitting diode package and a method of fabricating the same.” LGI1001, 1:23-26. A light emitting diode (LED), as the '664 Patent recognizes, is a widely used “semiconductor device that includes an N-type semiconductor and a P-type semiconductor, and emits light through recombination of holes and electrons.” *Id.*, 1:28-31. An example configuration of the '664 Patent's LED is shown below:



LGI1001, FIG. 1. Here, light is generated in the semiconductor stack 30 and emitted upward through a wavelength convertor 51.

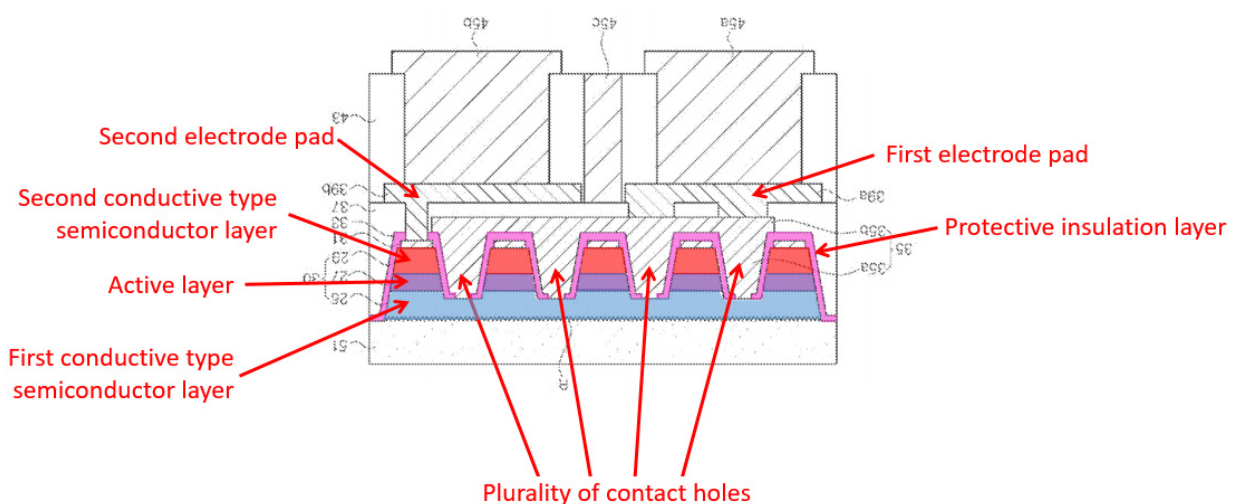
39. The particular configuration shown above is often referred to as a flip chip. The flip chip process was developed by IBM in the early 1960's and quickly gained popularity because it allowed the direct mounting of semiconductor chips without the use of bonding wires. In use, the chips are inverted—or “flipped”—and directly connected to an underlying substrate, such as a circuit board. An exemplary flip chip mounting of the '664 Patent's LED packages 100 is shown below:



LGI1001, FIG. 3.

40. Regarding its LED, the '664 Patent states that it “includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer” as well as “a plurality of contact holes arranged in the second conductive type semiconductor

layer and the active layer, the contact holes exposing the first conductive type semiconductor layer.” LGI1001, Abstract. First and second electrode pads are provided to establish electrical connections to the semiconductor layer. *Id.*, Claim 1. A protective insulation layer is provided to cover a sidewall of the semiconductor stack. *Id.*, Abstract. For illustration, I have labeled FIG. 1 of the ’664 Patent below to show the abovementioned features:



LGI1001, FIG. 1 (annotated).

41. This general description of the ’664 Patent’s LED lists various layers that, as would have been recognized by a POSITA, were well known and widely used in many LED components during the relevant time frame. In particular, a POSITA would have recognized that providing protective insulation layers over select portions were well-known not only in LED fabrication but generally in semiconductor processing. For example, with respect to the LED, such insulation is necessary to isolate the electrical contacts for the p-type and n-type

semiconductor layers from each other as well as from the semiconductor stack to prevent short-circuiting.

42. Some of the claims of the '664 Patent mentions that the protective insulation layer that covers the sidewalls of the semiconductor stack is made up of multiple layers, including those having different indices of refraction from each other. *See, e.g.*, LGI1001, Claims 1, 6, 12. But this, too, was a well-known feature during the relevant time period, as further discussed below with respect to Illek and Donofrio below.

43. Indeed, as demonstrated below, the claimed features of the '664 Patent were well-known and already in use prior to the earliest possible priority date of the '664 patent.

#### **B. File History of the '664 Patent**

44. As part of my preparation of this declaration, I reviewed the file history of the '664 patent (LGI1003). I understand that U.S. Application No. 14/815,433 (“the '443 Application”), which led to the '664 patent, was filed on July 31, 2015. LGI1001, Cover. I also understand that the '433 Application was allowed on November 12, 2015, without having received any rejections. *See generally* LGI1003.

### **C. Reexamination History of U.S. 9,070,851**

45. I understand that U.S. Patent No. 9,070,851 (“the ’851 Patent”), which is a parent to the ’664 Patent, was subject to an *ex parte* reexamination. *See generally* LGI1004.

46. During the reexamination, I understand that the Office rejected all claims over multiple grounds involving various references. LGI1004, 111-137. I understand that Donofrio, which I analyze in detail below, was one of the references used by the Office in the rejections. *See id.*, 125-130. I understand that, in order to overcome Donofrio, the Patent Owner chose to significantly narrow the issued claims to more narrowly recite “a protective insulation layer covering *each external side wall surface* of the semiconductor stack of each light emitting diode *facing externally* of the LED package *so that the protection insulation layer surrounds the LED package.*” *Id.*, 92. While I understand that these narrowing amendments formed the basis for patentability in the reexamination proceedings of the ’851 Patent, such language is absent from the issued claims in the ’664 Patent. *See id.*, 5-12.

### **VII. OVERVIEW OF CONCLUSIONS FORMED AND PRIOR ART REFERENCES**

47. This declaration explains the conclusions that I have formed based on my independent analysis. To summarize those conclusions:

- Claims 1-6, 8, 9, 11, and 12 of the ’664 Patent are anticipated by Illek.

- Claims 1-6 and 8-18 of the '664 Patent are obvious in view of Illek.
- Claims 7 and 19 of the '664 Patent are obvious in view of Illek and Begemann.
- Claims 1-19 are obvious in view of Donofrio and Sano.
- Claim 19 is obvious in view of Donofrio, Sano, and Begemann.

### **VIII. ANALYSIS OF ILLEK WITH RESPECT TO CLAIMS 1-6 AND 8-18**

48. For the reasons articulated in detail below, and based on my review of the '664 patent and the Illek reference, I am confident that a POSITA would have readily understood that Illek provides all elements of claims 1-6, 8, 9, 11, and 12, thereby rendering these claims anticipated by Illek. Furthermore, a POSITA would have recognized that claims 1-6 and 8-18 would have been obvious based on the teachings of Illek alone.

49. Illek, which has the title “Optoelectronic Component and Method for Producing a Plurality of Optoelectronic Components,” is directed to “an LED component to emit incoherent radiation.” LGI1005 at Title, [0095]. Illek’s LED component includes two semiconductor “regions 5, 6 having different types of conductivity (n-type or p-type)” as well as an active region 4 that is located between the semiconductor regions 5 and 6. *Id.*, [0085].

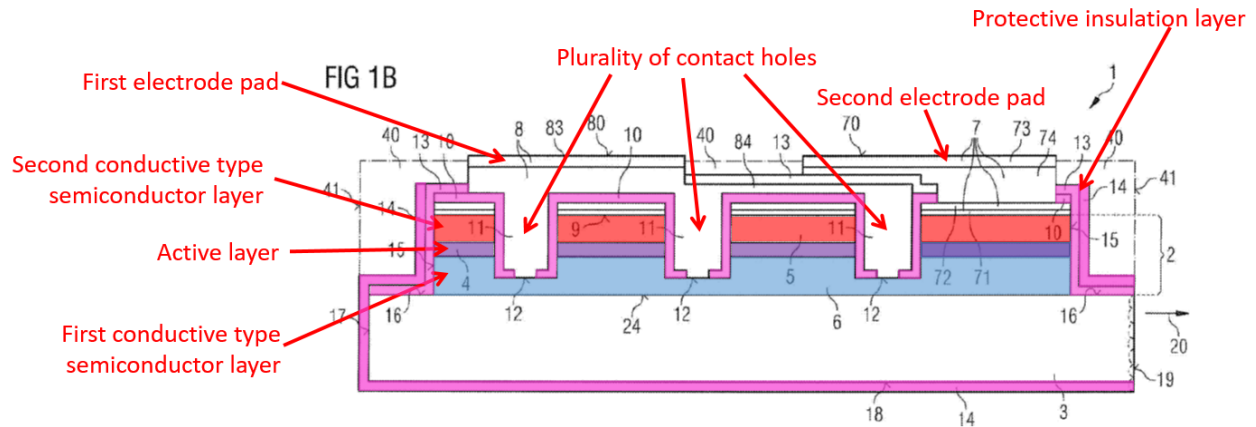
50. Illek teaches that “[a]n opening may be formed through the active region in the semiconductor body, through which opening the contact extends from

one side of the active region to the other side of the active region.” *Id.*, [0046].

Such an opening may “be formed by a recessed region of the semiconductor body that penetrates from the connection side into the semiconductor body and is filled with the contact material.” *Id.* Thus, “a plurality of openings through the active region, through which the contact can extend from one side of the active region to the other side of the active region” may be provided to Illek’s semiconductor stack. *Id.*, [0046].

51. Illek also teaches various insulation layers, such as “two insulation layers 10 and 13” and a “mirror layer 14” that covers various surfaces of its LED component. *Id.*, [0120], [0128]. The mirror layer 14 may be a “multilayer structure comprising exclusively dielectric layers, in particular, a sequence of a large number of dielectric layer pairs having layers with different refractive indices arranged alternately in the multilayer structure.” *Id.*, [0131].

52. To briefly summarize, as illustrated below, Illek’s LED component includes first and second conductive type semiconductor layers (regions 6 and 5, shown in blue and red), an active layer (active region 4, shown in purple), and a protective insulation layer (layers 10, 13, and 14, shown in pink).



LGI1005, FIG. 1B (annotated). As illustrated above, Illek provides a plurality of contact holes (recesses 11). Illek also discloses first and second electrode pads (contacts 8 and 7), as labeled above.

53. I have highlighted the structural similarities between the LED components as described by the '664 Patent and Illek below:

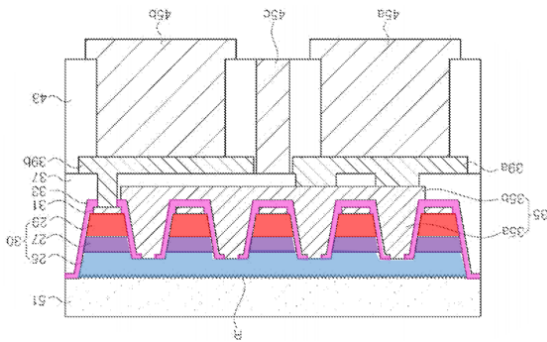


FIG. 1 of '664 Patent (annotated)

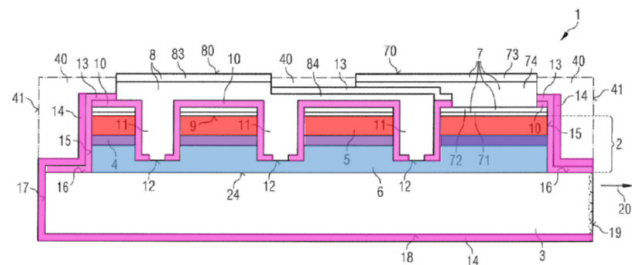


FIG. 1B of Illek (annotated)

54. Based on my review of the intrinsic record of the '664 patent and Illek, and my knowledge and experience in the field, it is my opinion that all the elements of claims 1-6 and 8-18 are disclosed by Illek. As part of my analysis, I will address each of the elements of claims 1-6 and 8-18, as follows.



***[1pre]: “A light emitting diode (LED) package, comprising:”***

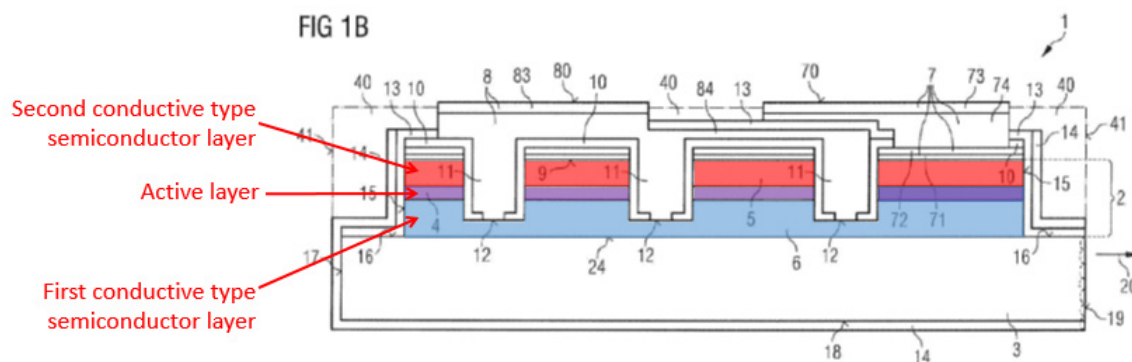
55. Even if the preamble here were considered to be a limiting element of claim 1, Illek discloses a light emitting diode (LED) package. For example, Illek teaches “an LED component” that is “designed to generate visible radiation.” LGI1005, [0095], [0015]. Moreover, the LED component of Illek, an example of which is shown in FIG. 1B, is an LED ***package***. In fact, the terms “LED component” and “LED package” both refer to an LED die—as shown in FIG. 1B of Illek—and are used interchangeably in the industry. *See* LGI1014, 4. Furthermore, a POSITA would have recognized that the LED component of Illek is indeed an LED package. Incidentally, a group of LED chips/components/packages that are mounted on a substrate is often referred to in the industry as either an LED array or an LED module. *Id.*

***[1a]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

56. Illek’s LED package includes a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer. For example, Illek teaches a “semiconductor body 2 compris[ing] a semiconductor layer sequence with an active region 4 capable of generating radiation.” LGI1005, [0084]-[0089]. Here, the semiconductor body 2 corresponds to the semiconductor stack. Further, Illek’s semiconductor body 2 is

made up of two semiconductor regions 5 and 6—which correspond to the two conductive type semiconductor layers as claimed—and an active region 4, which corresponds to the claimed active layer and is located between the two semiconductor regions 5 and 6. *Id.*, [0085]-[0086].

57. Illek further mentions that “[t]he region 6 of the semiconductor body is preferably implemented as n-type, while the region 5 of the semiconductor is p-type.” *Id.*, [0115]. Thus, based on the naming convention used in the ’664 Patent (*see, e.g.*, LGI1001, 5:35-36 (“The first conductive type may be an n-type and the second conductive type may be a p-type.”)), and as illustrated below, Illek’s region 6 (blue) corresponds to the first conductive type semiconductor layer and its region 5 (red) corresponds to the second conductive type semiconductor layer:

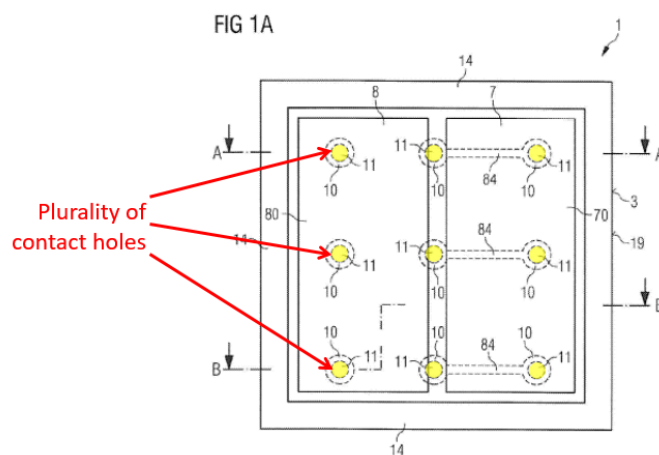


LGI1005, FIG. 1B (annotated). Illek’s active region 4 (purple) corresponds to the claimed active layer.

***[1b]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”***

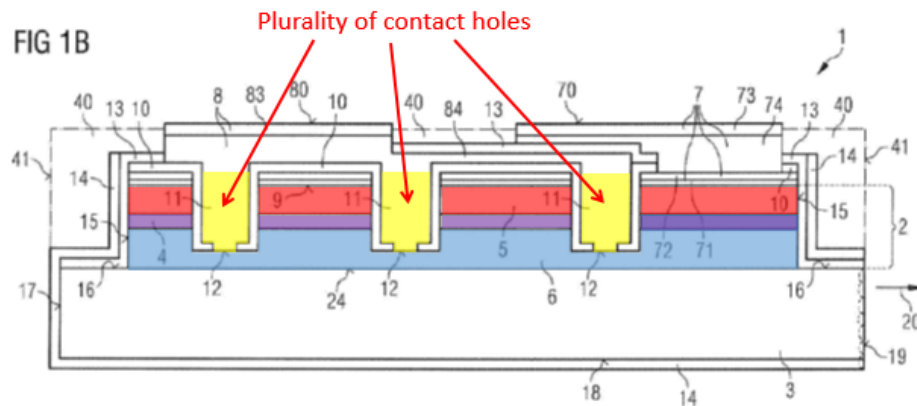
58. Illek's LED package includes a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer. For example, Illek discloses that “*an opening* may be formed through the active region in the semiconductor body” and particularly that “*a plurality of openings* through the active region can be present, through which the contact can extend from one side of the active region to the other side of the active region.” LGI1005, [0046]. That is, Illek teaches openings, or contact holes, that go through the second conductive type semiconductor layer and the active layer at one side of the semiconductor stack to expose the first conductive type semiconductor layer at the opposite side.

59. These plurality of contact holes, which Illek also refers to as “number of recesses 11,” are highlighted in yellow in the top-down view of Illek's LED package below:



LGI1005, FIG. 1A (annotated); [0110].

60. Referring to the cross-sectional view of the same LED package below, the contact holes of Illek (the general locations of which are highlighted in yellow) are provided through the semiconductor stack—including second conductive type semiconductor layer (red) and the active layer (purple)— and subsequently expose the first conductive type semiconductor layer (blue):



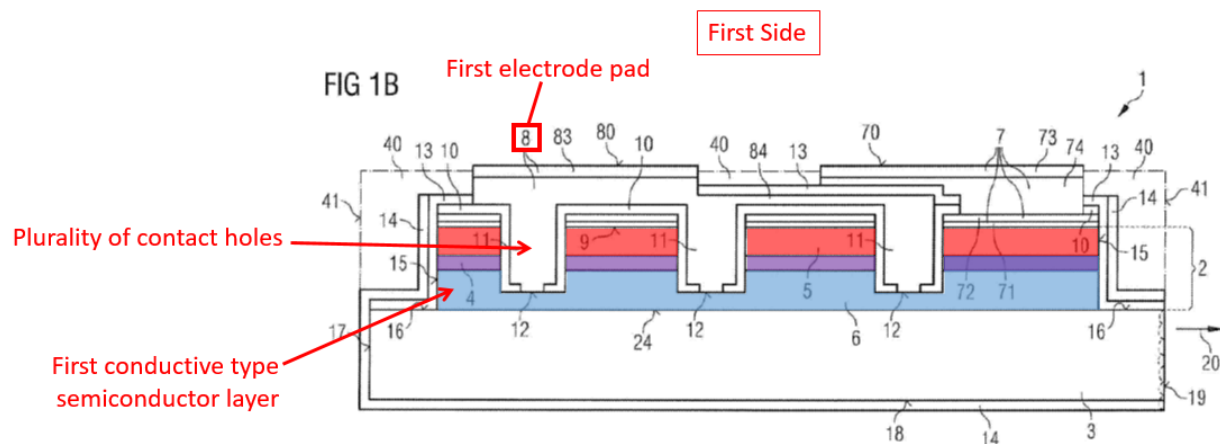
LGI1005, FIG. 1B (annotated). As is typically done in semiconductor fabrication, Illek’s FIG. 1B demonstrates the partial etching of the contact hole into the first conductive type semiconductor layer (blue), thereby ensuring reliable electrical contact to that layer.

***[1c]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”***

61. Illek’s LED package includes a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the

plurality of contact holes. For example, Illek discloses two electrode pads, contacts 7 and 8, which “are electrically conductively connected to the semiconductor body 2.” LGI1005, [0096]. Additionally, both contacts 7 and 8 are “arranged on the side of the semiconductor body that faces away from the carrier 3.” *Id.*, [0097].

62. Specifically, Illek’s “contact 8,” labeled in the annotated drawing below, corresponds to the claimed first electrode pad and is “electrically conductively connected to the semiconductor body 2 on the side of the active region that faces away from the connecting faces 70, 80, in particular to the region 6 of the semiconductor body 2”:



LGI1005, FIG. 1B (annotated); [0102]. That is, the first electrode pad of Illek “extends through one or, preferably, through a number of openings [that is, recesses 11] through the active region 4” to become electrically connected to the electrically connected to the first conductive type semiconductor layer. *Id.*, [0110]. The LED

device of Illek would not function if such electrical connection could not be established between the contact 8 and the first conductive type semiconductor layer. The side on which the first electrode pad is provided may be referred to as being the “first side” as labeled above.

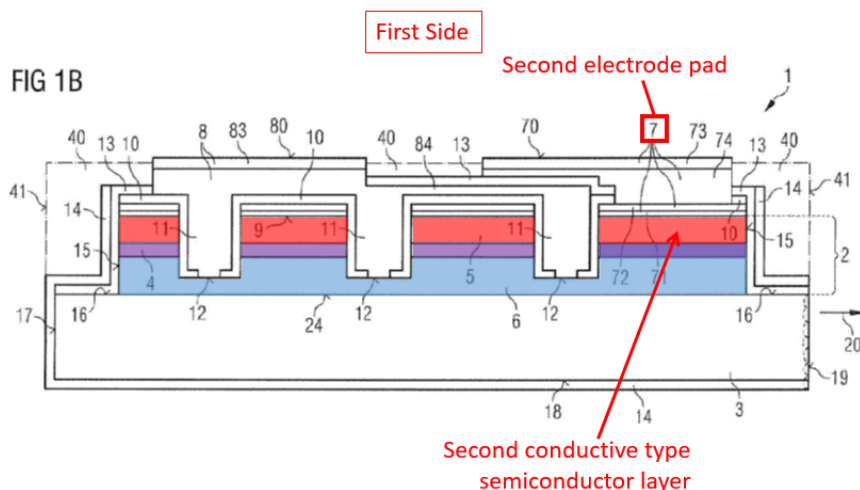
63. In conclusion, as indicated in the annotated drawing above, Illek’s first electrode pad (contact 8) is arranged over a first side of the semiconductor stack and electrically connected to the first conductive type semiconductor layer (region 6, shown in blue) via some of the plurality of contact holes (recesses 11).

***[1d]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

64. Illek’s LED package includes a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer. In particular, as I noted above for element [1d], Illek discloses “contacts 7 and 8 [that] are electrically conductively connected to the semiconductor body 2,” where both contacts are “arranged on the side of the semiconductor body that faces away from the carrier 3.” LGI1005, [0096]-[0097]. Here, Illek’s “contact 7,” which is “electrically conductively connected...to the region 5 of the semiconductor body,” corresponds to the claimed second electrode pad. *Id.*, [0102]. That is, the second

electrode pad of Illek is electrically connected to the second conductive type semiconductor layer.

65. As illustrated below, the second electrode pad of Illek (contact 7) is arranged over the first side of the semiconductor stack and is electrically connected to the second conductive type semiconductor layer (region 5, shown in red):

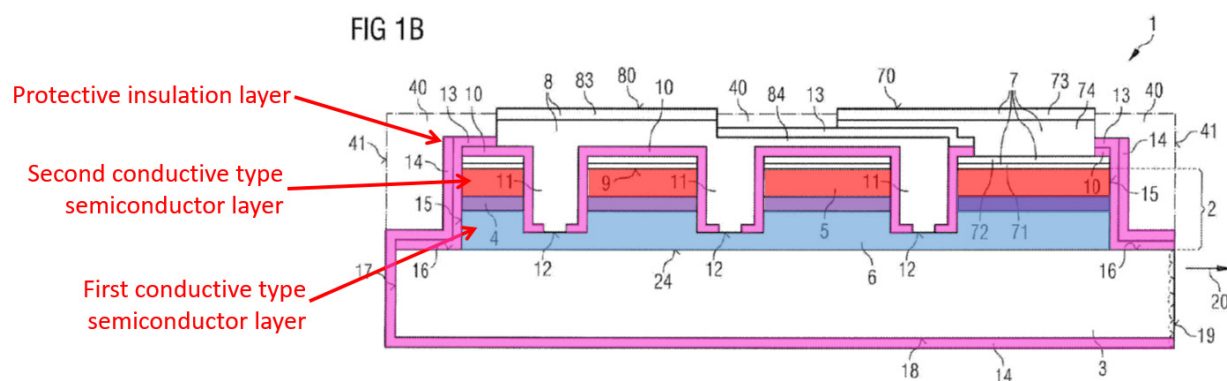


LGI1005, FIG. 1B (annotated). The LED device of Illek would not function if such electrical connection could not be established between the contact 7 and the second conductive type semiconductor layer.

***[1e]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”***

66. Illek’s LED package includes a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer. Specifically, referring to annotated FIG. 1B

below, Illek discloses various layers with insulating properties—in particular **layers 10, 13, and 14** that I have highlighted in pink—that are applied on the sidewalls of the LED component, including the sidewall of the first conductive type semiconductor layer (blue) and the second conductive type semiconductor layer (red):



LGI1005, FIG. 1B (annotated).

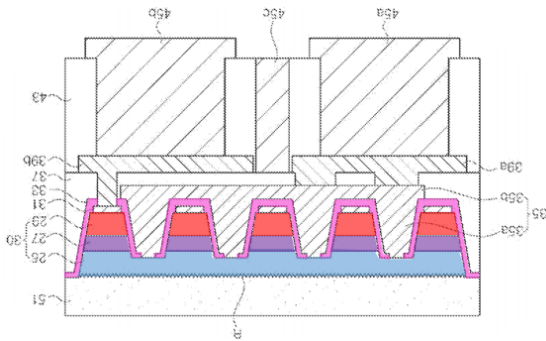
67. As an initial matter, the '664 Patent explains that more than a single distinct layer may make up the claimed protective insulation layer. For example, the '664 Patent expressly states that two separate insulation layers may be part of the protective insulation layer. *See* LGI1001, 7:16-29 (“The protective insulation layer may include, for example, the first insulation layer 33 and/or the second insulation layer 37.”). The '664 Patent further states that each of its separate insulation layers may each be made up of multiple layers. *See id.*, 6:1-7 (“The first insulation layer 33 may be composed of . . . multiple layers”); *id.*, 6:22-24 (“The second insulation layer 37 may be composed of a single layer or multiple layers.”).



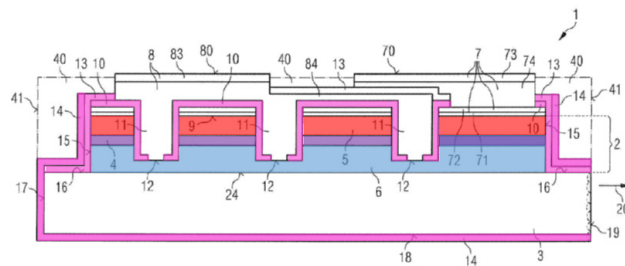
Thus, my mapping of Illek's layers 10, 13, and 14 to the claimed protective insulation layer is well-aligned with the use of the term "protective insulation layer" in the '664 Patent.

68. As for layers 10 and 13, Illek teaches that its first insulation layer 10 and second insulation layer 13 are made of insulating materials such as silicon nitride, silicon oxide, or silicon oxynitride and that they are selectively applied over the semiconductor stack to provide electrical isolation. LGI1005, [0109]-[0112], [0120]. As for layer 14, Illek teaches that its mirror layer 14 can be applied over various surfaces, and particularly outer faces, of the LED component. *Id.*, [0128]. Moreover, Illek teaches that the mirror layer 14 can be implemented as a dielectric mirror—that is, made of insulating dielectric materials such as silicon dioxide. *Id.*, [0130]-[0132].

69. Accordingly, the three insulating layers 10, 13, and 14 of Illek together correspond to the protective insulation layer as recited in the '664 Patent. Indeed, as I show in the side-by-side comparison below, the protective insulation layer 33 of the '664 Patent—shown on the left side in pink—is structurally and spatially analogous to the layers 10, 13, and 14 of Illek—shown on the right side in pink—in that, for instance, both layers provide a conformal coating that surrounds the semiconductor stack:



Annotated FIG. 1 of '664 Patent



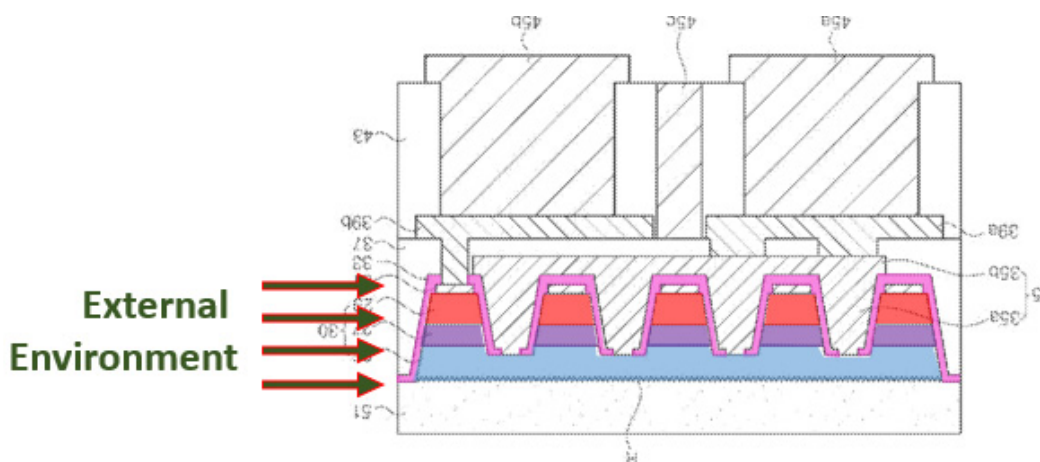
Anntoated FIG. 1B of Illek

70. Functionally speaking, because layers 10, 13, and 14 of Illek are insulating materials that are deposited directly onto the semiconductor stack, they act as a passivation layer, effectively providing a protective coating for the underlying semiconductor body to help reduce electrical and chemical reactivity at the surface as well as throughout the bulk. By way of illustration, semiconductors are technically molecular solids—essentially a giant molecule. Thus, the properties of a semiconductor are dependent on the addition or subtraction of electrons from bonds between atoms. At the edge of a layer there are free/dangling bonds, which are all missing electrons since there are no other atoms. This can change the electrical properties of the semiconductor at the edge because the region behaves like a huge reservoir or charge carriers. The addition of passivation layers on the sidewalls, therefore, eliminate dangling bonds at the edge and preserve the desired semiconducting properties.

71. Such passivation of the semiconductor body can further help protect against undesirable metal diffusion as well as short-circuits. In fact, Illek

expressly mentions that the insulations layers 10 and 13 help protect against short-circuits between the two contacts as well as between the contacts and the semiconductor body. *See* LGI1005, [0109].

72. Incidentally, the '664 Patent mentions that the protective insulation layer may help protect the LED chip from an “external environment.” LGI1001, 7:16-29. I’ve illustrated below how the '664 Patent’s LED chip may be exposed to such an external environment, which can include environmental factors such as moisture:



LGI1001, FIG. 1 (annotated).

73. Even if such protection from external factors were a required function of the “protective insulation layer” as claimed in the '664 Patent, which I don’t agree with, the insulating layers 10, 13, and 14 of Illek nevertheless provide such protection. Indeed, as illustrated below, the configuration of Illek’s layers 10/13/14 necessarily provide such protection by surrounding and facing externally

[illegible]

74. Notably, Illek expressly recognizes the need to protect the LED chip from “external influences such as moisture” and further contemplates the addition of an optional encapsulation 40 (shown in ghost lines above) as an added measure of providing protection from such external influences. *Id.*, [0147], [0148].

Nevertheless, even without the optional encapsulation layer, Illek’s layers 10/13/14 still provide protection from external influences due to their arrangement relative to the LED package.

36

described above, the '664 Patent similarly refers to multiple insulating layers as collectively making up the “protective insulation layer.”

***[1f]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”***

76. The protective insulation layer of Illek includes insulation layers having different indices of refraction from each other. Specifically, as I discussed above for element [1e], the protective insulation layer of Illek is made up of multiple layers, including the mirror layer 14. As for the mirror layer 14, Illek discloses that it may be “implemented as a multi-layer structure, incorporating dielectric layers with different refractive indices” and in particular as “a dielectric multi-layer structure.” LGI1005, [0013], [0131]. Thus, because at least a portion of Illek’s protective insulation layer is made from insulating dielectric layers with different refractive indices, the protective insulation layer of Illek includes insulation layers having different indices of refraction from each other.

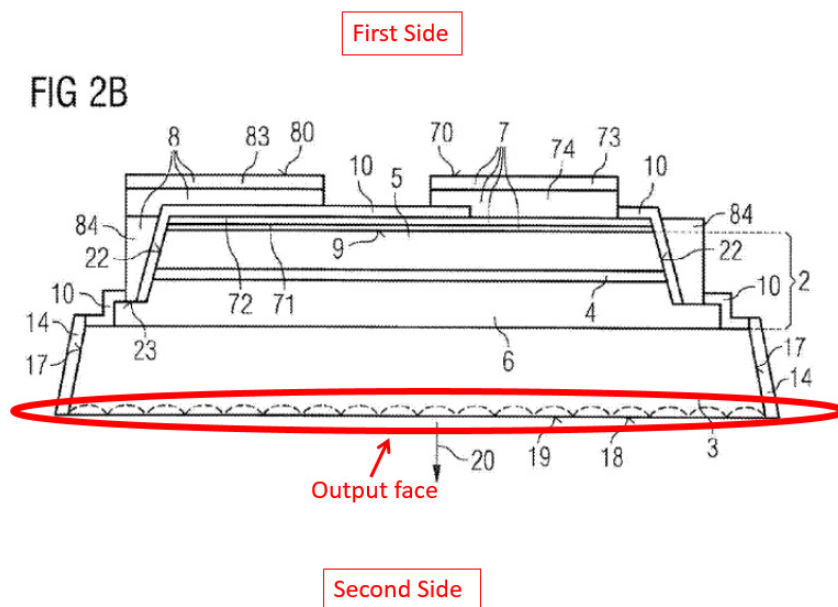
77. Similarly, the '664 Patent describes that its protective insulation layer may include a first insulation layer 33 and/or a second insulation layer 37, and further that one or both of these insulation layers 33 and 37 may be “formed by alternatively stacking insulation layers having different indices of refraction.” LGI1001, 7:17-21, 9:16-26, 9:39-45.

***[2a]: “The LED package of claim 1, further comprising a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side***

*of the semiconductor stack,”*

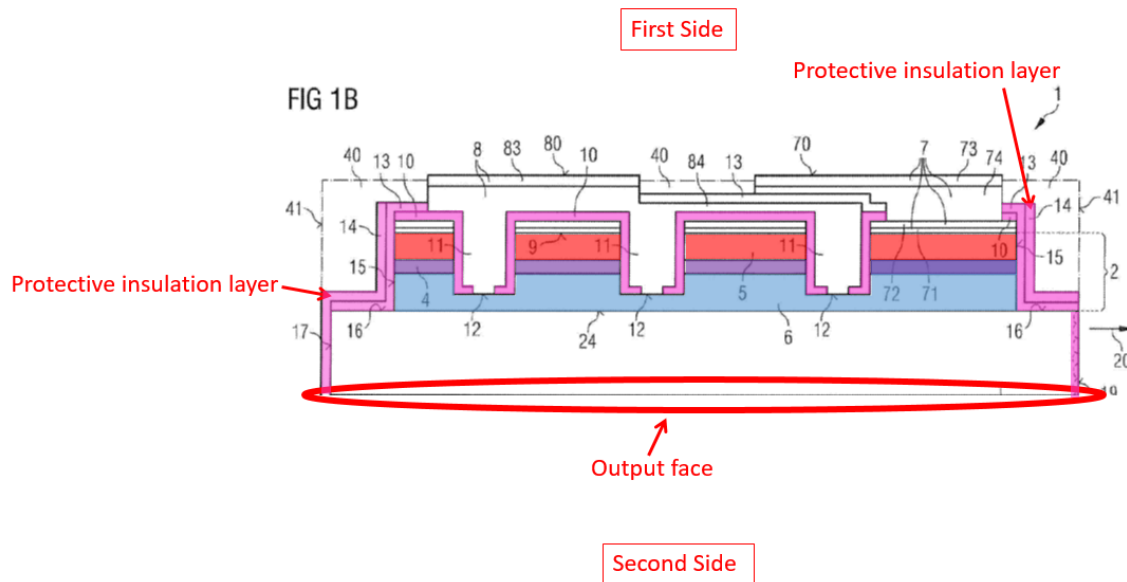
78. Illek’s LED package includes a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack. Specifically, Illek discloses that a “further element can be applied to the output face 19.” LGI1005, [0143]. According to Illek, such element can include a “luminescence conversion layer, for instance, containing a conversion material” that can “absorb radiation that is generated in the active region and convert it into radiation with a greater wavelength.” *Id.* Thus, Illek discloses the application of a wavelength convertor at the output face of the LED package.

79. As for the location of the output face at which the wavelength convertor is positioned, Illek teaches that the output face can be located at any desired surface where light emission is desired by simply “not applying a mirror layer to the desired face.” LGI1005, [0142], [0161]. For example, with reference to the “first side” as established above for elements [1c] and [1d], Illek teaches that the output face may be at the opposing side—or second side—as illustrated below:



LGI1005, FIG. 2B (annotated). Illek refers to this configuration shown in FIG. 2B as a “top-looker” and the configuration shown in FIG. 1B, where the output face is on the side surface, as a “side-looker.” *Id.*, [0161]. However, Illek teaches that “FIG. 1 can be implemented as a top-looker, while the component according to FIG. 2 can be implemented as a side-looker.” *Id.*

80. FIG. 1B of Illek, if implemented as a top-looker, would look as follows:



LGI1005, FIG. 1B (modified, annotated). Applying Illek's wavelength convertor the output face of the LED package as shown above would result in the wavelength convertor being arranged over a second side of the semiconductor stack, where the second side is opposite to the first side of the semiconductor stack.

81. To the extent the FIG. 1 implementation of Illek is considered to not explicitly teach the top-looker configuration by which the output face—and consequently the wavelength convertor—would be at the second side of the semiconductor stack, a POSITA would have recognized that Illek's LED package shown in FIG. 1B can be readily modified such that the output face is relocated from the side surface (*i.e.*, side-looker configuration) to the bottom surface (*i.e.*, top-looker configuration), which in turn would place the wavelength convertor over the second side of the semiconductor stack. Illek very explicitly teaches such relocation of the output face as a simple design choice, and such a modification



would merely constitute a simple substitution of a side-looker configuration with a top-looker configuration in order to obtain predictable results. *See* LGI1005, [0142]; [0161]; FIG. 2B.

***[2b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”***

82. The wavelength convertor of Illek comprises a phosphor sheet or an impurity-doped material. In particular, regarding further details about its wavelength convertor, Illek incorporates by reference U.S. Pat. No. 6,066,861 to Hohn (LGI1006, “Hohn”), *see* LGI1005, [0143], which explicitly teaches that the wavelength convertor can be made from a “transparent epoxy casting resin” containing “a phosphorous group of the general formula  $A_3B_5X_{12}:M$ .” LGI1006, Abstract. A layer of transparent epoxy that is made from a phosphorous group corresponds to the claimed wavelength convertor comprising a phosphor sheet.

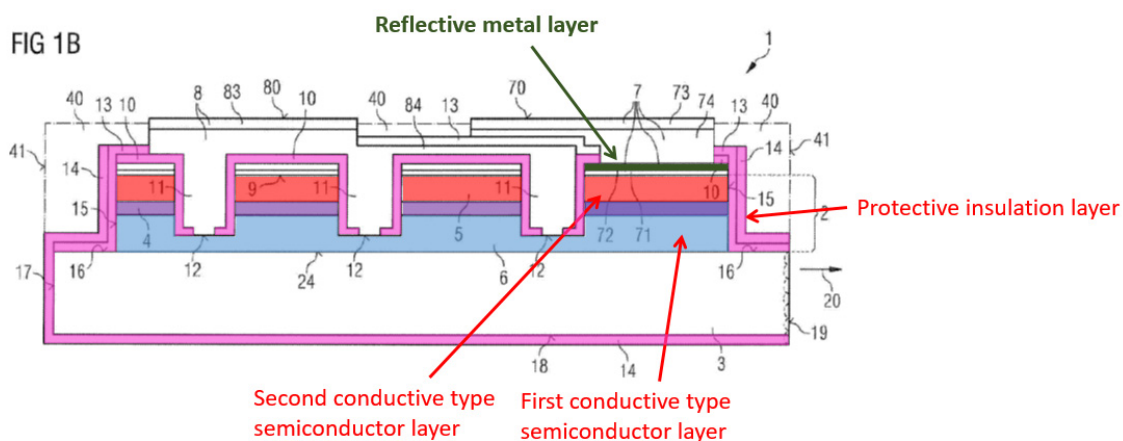
83. Hohn also teaches that the wavelength convertor can include “Ce-doped garnets.” LGI1006, Claim 6; 7:4-8. Because “Ce-doped garnets” is a material that has been doped with cerium, the wavelength convertor of Illek includes, as claimed, an impurity-doped material.

84. To the extent Illek is considered not to explicitly teach the wavelength convertor as claimed, a POSITA would have nonetheless found it obvious to make Illek’s luminescence conversion layer from a host of commonly used wavelength

conversion materials, including the claimed phosphor sheet or impurity-doped material as claimed. Indeed, Hohn, which was incorporated by reference by Illek, explicitly mentions that luminescence conversion layers as found in Illek can be made from a phosphor-containing epoxy (*i.e.*, phosphor sheet) or a Ce-doped garnet (*i.e.*, impurity-doped material) in such wavelength converting applications. LGI1006, Abstract; Claim 6.

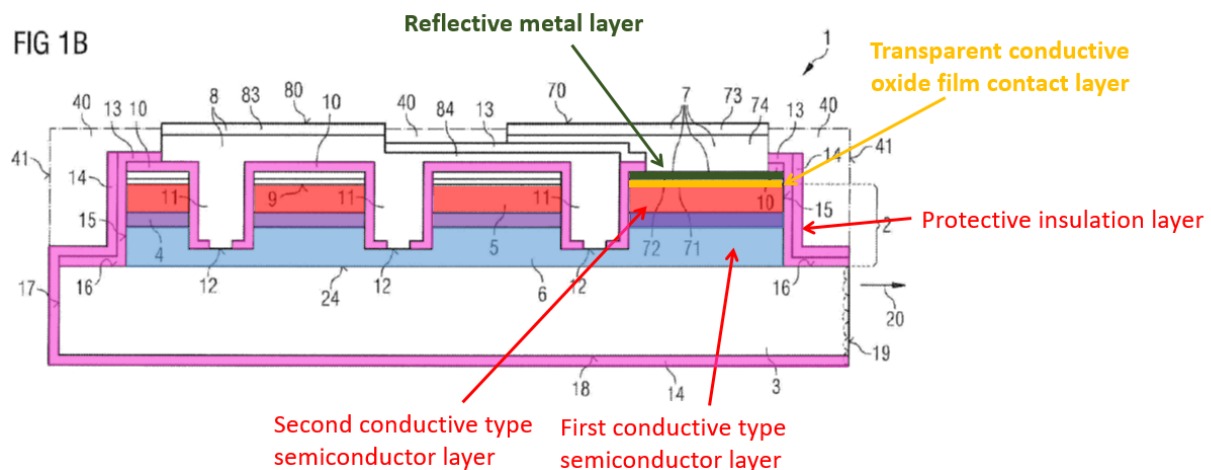
***[3a]: “The LED package of claim 1, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer”***

85. Illek’s LED package includes a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer. In particular, as indicated in green below, Illek includes a reflector layer—*i.e.*, reflective metal layer—that is over the second conductive type semiconductor layer (red):



LGI1005, FIG. 1B (annotated). Illek's reflective metal layer serves to reflect the light emission downward toward the output face. *Id.*, [0103]. To this end, a highly reflective material such as aluminum may be used to form Illek's reflector layer 72. *Id.*, [0107]. Based on this disclosure of the reflector layer 72, Illek satisfies claim element [3a], which requires a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer

86. Additionally, Illek discloses a semitransparent contact layer 71 (shown below in yellow), which is positioned between the reflector layer 72 (green) and the second conductive type semiconductor layer (red), and which corresponds to the claimed transparent conductive oxide film contact layer:



LGI1005, FIG. 1B (annotated); [0106]. In addition to being transparent, thereby allowing the light reflected off the reflector layer 72 to pass through toward the

output face, the contact layer 71 is also conductive to thereby enable electrical connectivity between the contact 7 and the underlying semiconductor region.

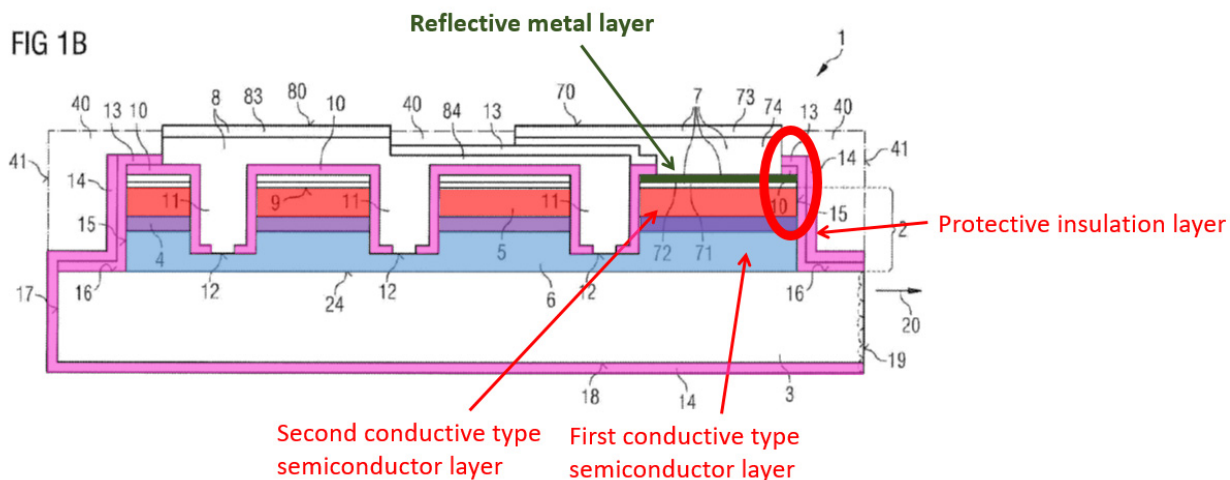
87. While Illek does not expressly disclose that its semitransparent contact layer 71 is an oxide material, a POSITA would have nevertheless known that a transparent/semitransparent contact layer as in Illek that is “optimized for electrical contact formation” would indeed be a conductive *oxide* film. LGI1005, [0106]. For example, as demonstrated in U.S. 6,693,352 to Huang (LGI1012), Indium Tin Oxide (ITO) was a well-known material that would have been commonly used during the time of the '664 Patent as well as Illek for forming transparent conductive oxide film contact layers in LED devices. *See, e.g.*, LGI1012, Abstract, 2:44-64; 7:26-35.

88. Thus, Illek’s disclosure of a semitransparent contact layer 71, along with the knowledge of a POSITA, further renders obvious the transparent conductive oxide film contact layer aspect of element [3a].

***[3b]: “a part of the transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer.”***

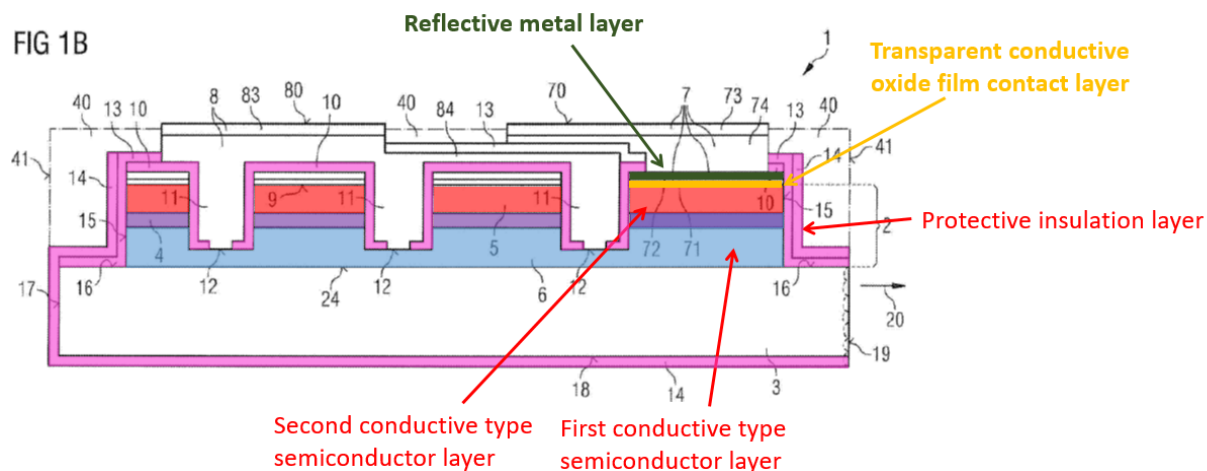
89. A part of Illek’s transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer. In particular, as shown below, the reflector layer 72 of Illek (green), which corresponds to the claimed reflective

metal layer, is positioned between Illek's second conductive type semiconductor layer (red) and the horizontal portion of Illek's protective insulation layer (pink):



LGI1005, FIG. 1B (annotated).

90. Additionally, as I described above for element [3a], Illek also renders obvious the claimed feature of a transparent conductive oxide film contact layer, as shown in yellow below:



LGI1005, FIG. 1B (annotated). As seen in the annotated drawing above, a part of Illek's transparent conductive oxide film contact layer (yellow) is also formed

between the second conductive type semiconductor layer (red) and the horizontal portion of Illek's protective insulation layer (pink).

***[4]: “The LED package of claim 3, wherein the transparent conductive oxide film contact layer includes an ITO (Indium Tin Oxide).”***

91. As I explained for element [3a], Illek's LED package includes a reflective metal layer, thus satisfying the claim's requirement of a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer. And because claim 4 doesn't place further restrictions on the reflective metal layer aspect of claim 3, which I explained is satisfied by Illek, claim 4 is also satisfied by extension.

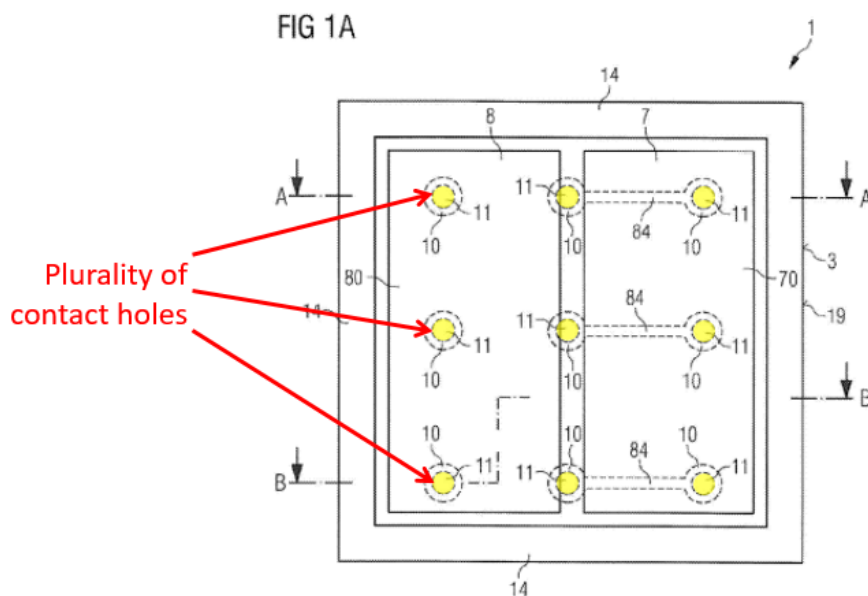
92. Moreover, as I also explained above for element [3a], a POSITA would have further recognized that Illek's semitransparent contact layer 71 would indeed be a transparent conductive oxide film. LGI1005, [0106]. And as demonstrated in the prior art, Indium Tin Oxide (ITO) was a well-known material that would have been commonly used during the time of the '664 Patent as well as Illek to form transparent conductive oxide film contact layers. *See, e.g.*, LGI1012, Abstract, 2:44-64; 7:26-35.

***[5a]: “The LED package of claim 4, wherein at least one of the contact holes has a circular shape, and”***

93. Illek's LED package discloses that at least one of the contact holes has a circular shape. In particular, as I explained above for element [1b], Illek

discloses “number of recesses 11” which correspond to the claimed contact holes.

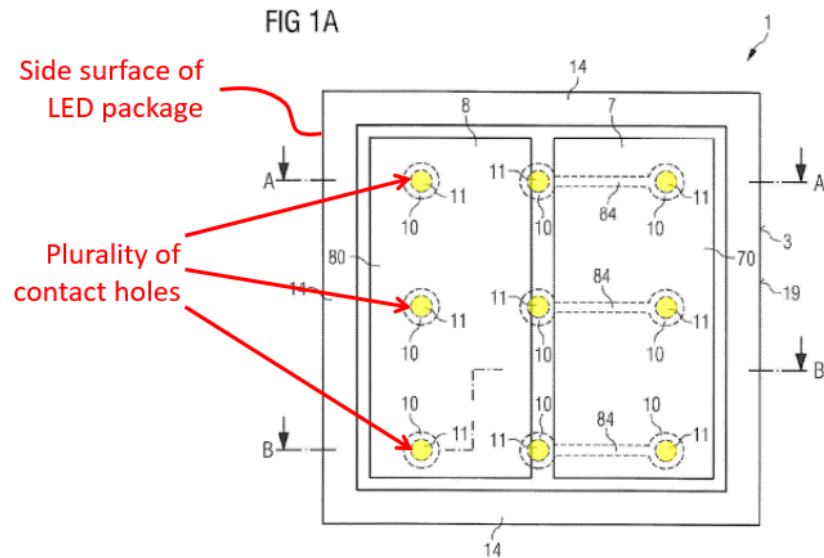
Moreover, as seen below in the top-down view of Illek’s LED package, the contact holes of Illek (shown in yellow) have a circular shape:



LGI1005, FIG. 1A (annotated).

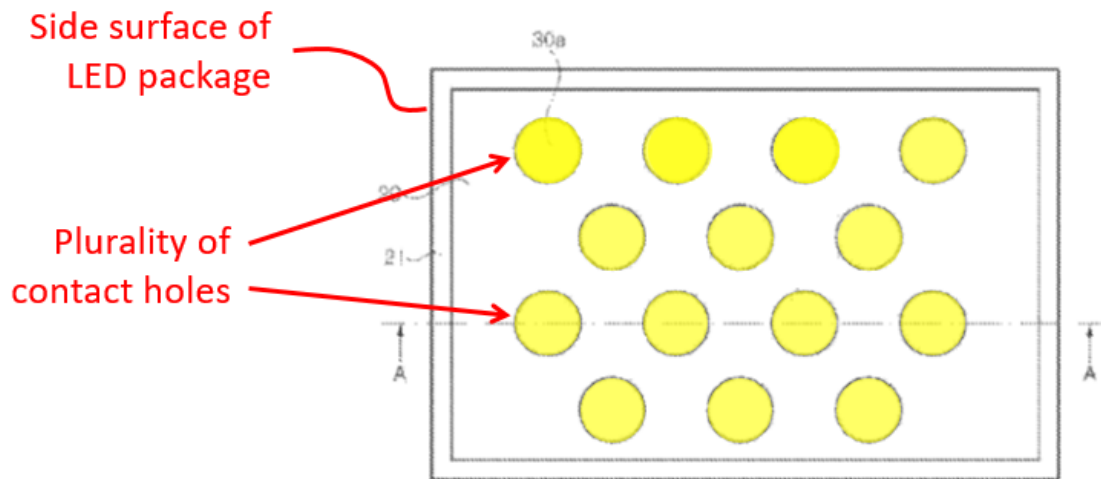
***[5b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”***

94. The plurality of contact holes in Illek’s LED package are arranged along at least one side surface of the LED package. Indeed, Illek’s LED package has four side surfaces stemming from its rectangular shape and the plurality of recesses 11—that is, the contact holes—are arranged along each of the four sides. I have annotated below one of the side surfaces of Illek’s LED package and the plurality of contact holes that are arranged along that side surface:



LGI1005, FIG. 1A (annotated).

95. The way that Illek’s contact holes are “arranged along at least one side surface” is analogous to the way the contact holes are arranged with respect to the side surface in the ’664 Patent, as illustrated below:



LGI1001, FIG. 5(a) (annotated).

**[6pre]: “A light emitting diode (LED) module, comprising:”**



96. Even if the preamble here were considered to be a limiting element of claim 6, Illek discloses a light emitting diode (LED) module. As an initial matter, as I explained above for element [1pre], Illek teaches an LED component. *See* LGI1005, [0015], [0095]; FIG. 1B. Further, Illek teaches that its LED component is mounted on an external carrier, for example a circuit board. *Id.*, [0019]; [0099]; [0122]. An LED component or package that is mounted on a circuit board is referred to in the industry as a LED module. *See* LGI1014, 4 (Defining “LED array or module” as “[a]n assembly of LED packages (components), or dies on a printed circuit board or substrate.”).

***[6a]: “a circuit board;”***

97. Illek discloses a circuit board. In particular, Illek discloses mounting its LED components on an “external connection carrier, preferably a connection carrier of large area such as ***a circuit board.***” LGI1005, [0019]; [0099]; [0122].

98. To the extent Illek is considered to not disclose a circuit board because, for instance, it doesn’t include a drawing of the LED package that has been mounted onto a circuit board, a POSITA would certainly have found it obvious—in view of Illek’s explicit disclosure about mounting its LED packages to a circuit board—to add the circuit board to Illek’s LED package to create a working LED module. *See* LGI1005, [0019]; [0099]; [0122].

***[6b]: “a LED package arranged over the circuit board without bonding wires, wherein the LED package includes:”***

99. Illek discloses that its LED package is arranged over the circuit board without bonding wires. As I mentioned above in ¶¶ 38-39, the LED chip in the '664 Patent is based on the well-known flip-chip design, which allows the chip to be mounted without the use of bonding wires. That is, the LED packages of Illek are surface mount packages that are directly mounted to the circuit board without the use of bonding wires. This is a very common way to mount LED chips, and not surprisingly, Illek also teaches that its LED package is “in the manner of a flip-chip, to be electrically conductively connected to external connection conductors, preferably directly, for instance by means of electrically conductive adhesive or solder.” LGI1005, [0127]. Such a flip-chip design doesn't require the use of bonding wires, and indeed, Illek explicitly mentions that “using bonding wires can be omitted” with its design. LGI1005, [0127].

***[6c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

100. Illek's LED package includes a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer. See Analysis of Element [1a], ¶¶ 56-57, *supra*; LGI1005, [0084]-[0089], [0115], FIG. 1B.

***[6d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”***

101. Illek's LED package includes a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer. *See* Analysis of Element [1b], ¶¶ 58-60, *supra*; LGI1005, [0046], [0110], FIGS. 1A, 1B.

***[6e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”***

102. Illek's LED package includes a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes. *See* Analysis of Element [1c], ¶¶ 61-63, *supra*; LGI1005, [0096], [0097], [0102], [0110], FIG. 1B.

***[6f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

103. Illek's LED package includes a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer. *See* Analysis of Element [1d], ¶¶ 64-65, *supra*; LGI1005, [0096], [0097], [0102], [0110], FIG. 1B.

***[6g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”***

104. Illek's LED package includes a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer. *See* Analysis of Element [1e], ¶¶ 66-75, *supra*; LGI1005, [0109]-[0112], [0120], [0128], [0130], [0147], [0148], FIG. 1B.

***[6h]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and”***

105. The protective insulation layer of Illek's LED package includes insulation layers having different indices of refraction from each other. *See* Analysis of Element [1f], ¶¶ 76-77, *supra*; LGI1005, [0013], [0131], FIG. 1B.

***[6i]: “a lens to adjust an orientation angle of light emitted from the LED package.”***

106. Illek's LED module includes a lens to adjust an orientation angle of light emitted from the LED package. Specifically, Illek disclose “an optical element such as *a refractive element for the beam shaping, in particular, a lens*, or a diffractive element can be located on the output face and, in particular, applied to the component.” LGI1005, [0143]. Because the refractive element (*i.e.*, lens) of Illek is positioned over the output face of the LED package, it serves to shape the light beam being emitted from the LED package through optical refraction. That is, the orientation angle of light emitted from the LED package is adjusted to create the desired beam shape.

***[8pre]: “A light emitting diode (LED) module, comprising:”***

107. To the extent the preamble here is limiting, Illek discloses a light emitting diode (LED) module. *See* Analysis of Element [6pre], ¶ 96, *supra*; LGI1005, [0015], [0019], [0095], [0099], [0122], FIG. 1B.

***[8a]: “a circuit board;”***

108. Illek discloses a circuit board. In particular, Illek discloses mounting its LED components on an “external connection carrier, preferably a connection carrier of large area such as *a circuit board*.” LGI1005, [0019]; [0099]; [0122].

109. To the extent Illek is considered to not disclose a circuit board because, for instance, it doesn’t include a drawing of the LED package that has been mounted onto a circuit board, a POSITA would certainly have found it obvious—in view of Illek’s explicit disclosure about mounting its LED packages to a circuit board—to add the circuit board to Illek’s LED package to create a working LED module. *See* LGI1005, [0019]; [0099]; [0122].

***[8b]: “a LED package bonded on the circuit board without bonding wires; wherein the LED package comprising”***

110. Illek disclose that its LED package is bonded on the circuit board without bonding wires. As I mentioned above in ¶¶ 38-39, the LED chip in the ’664 Patent is based on the well-known flip-chip design, which allows the chip to be bonded onto the circuit board without the use of bonding wires. This is a very common way to mount/bond LED chips, and not surprisingly, Illek also teaches that its LED package is “in the manner of a flip-chip, to be electrically

conductively connected to external connection conductors, preferably directly, for instance by means of electrically conductive adhesive or solder.” LGI1005, [0127]. That is, the LED packages of Illek are surface mount packages that are directly mounted to the circuit board without the use of bonding wires. Such a flip-chip design doesn’t require the use of bonding wires in order to bond the LED package to the circuit board, and indeed, Illek explicitly mentions that “using bonding wires can be omitted” with its design. LGI1005, [0127].

***[8c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

111. Illek’s LED package includes a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer. *See* Analysis of Element [1a], ¶¶ 56-57, *supra*; LGI1005, [0084]-[0089], [0115], FIG. 1B.

***[8d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”***

112. Illek’s LED package includes a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer. *See* Analysis of Element [1b], ¶¶ 58-60, *supra*; LGI1005, [0046], [0110], FIGS. 1A, 1B,

***[8e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically***

***connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”***

113. Illek’s LED package includes a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes. *See* Analysis of Element [1c], ¶¶ 61-63, *supra*; LGI1005, [0096], [0097], [0102], [0110], FIG. 1B.

***[8f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

114. Illek’s LED package includes a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer. *See* Analysis of Element [1d], ¶¶ 64-65, *supra*; LGI1005, [0096], [0097], [0102], [0110], FIG. 1B.

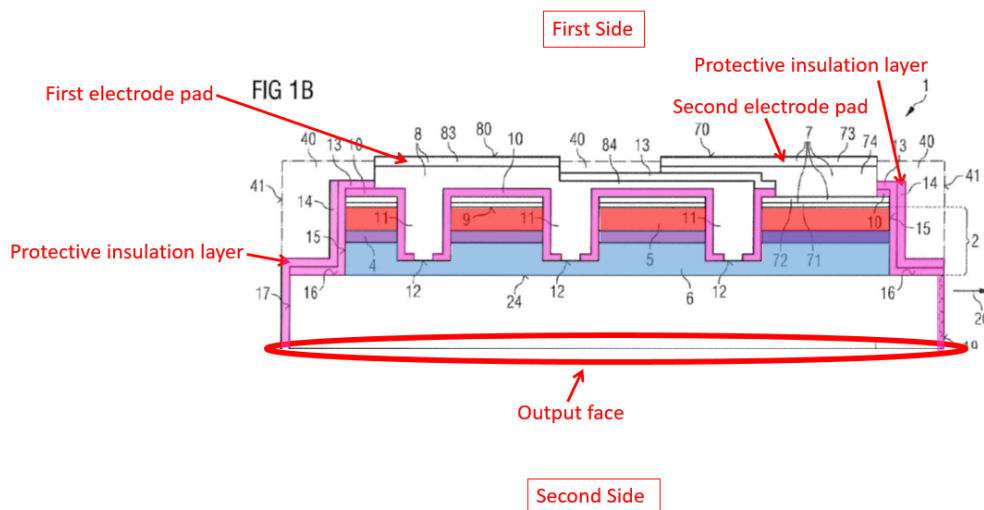
***[8g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer.”***

115. Illek’s LED package includes a protective insulation layer covering a sidewall of the first conductive type semiconductor layer. *See* Analysis of Element [1e], ¶¶ 66-75, *supra*; LGI1005, [0109]-[0112], [0120], [0128], [0130], [0147], [0148], FIG. 1B. According to my analysis for element [1e] above, the protective insulation layer of Illek covers the sidewall of ***both*** the first and second conductive

type semiconductor layers; therefore, Illek's protective insulation layer certainly covers a sidewall of the first conductive type semiconductor layer.

**[9a]: “The LED module of claim 8, further comprising a wavelength converter over the opposite side of the LED package to the first and second electrode pads,”**

116. Illek's LED module includes a wavelength converter over the opposite side of the LED package to the first and second electrode pads. Specifically, as I discussed above for element [2a], Illek discloses a wavelength converter over a second side of the semiconductor stack. *See* Analysis of Element [2a], ¶¶ 78-81, *supra*. Moreover, as illustrated below, Illek's wavelength converter over the second side of the semiconductor stack is positioned at the opposite side of the LED package to the first and second electrode pads:



LGI1005, FIG. 1B (annotated).

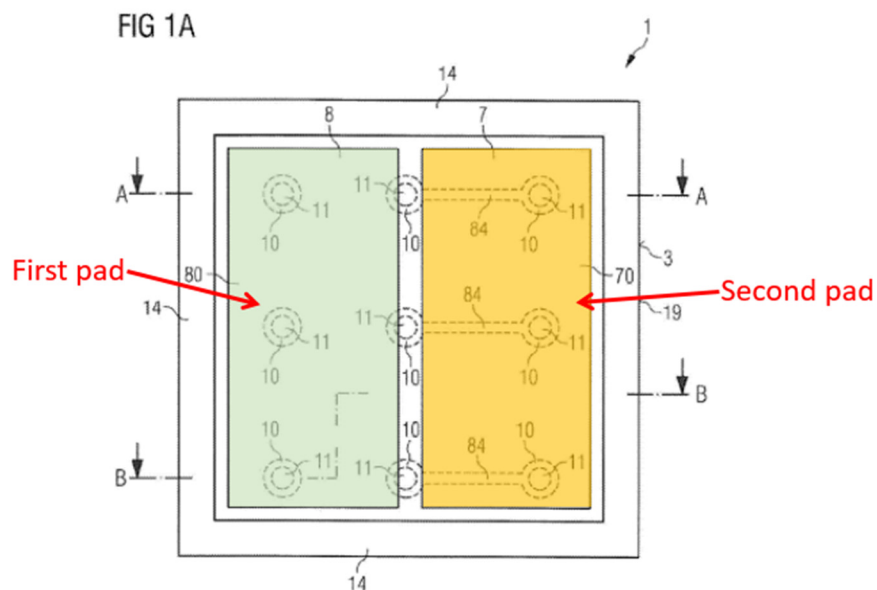
**[9b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”**



117. Illek's wavelength convertor comprises a phosphor sheet or an impurity-doped material. See Analysis of Element [2b], ¶¶ 82-84, *supra*; LGI1005, [0143]; LGI1006, Abstract, 7:4-8, Claim 6.

***[10a]: “The LED module of claim 9, wherein each area of the first and second pads has an area not less than  $\frac{1}{3}$  of the LE package.”***

118. Each area of the first and second pads in Illek's LED package has an area not less than  $\frac{1}{3}$  of the LED package.<sup>2</sup> Specifically, looking at the top-down image below of Illek's LED package, Illek's first pad (green) and second pad (yellow) can be seen taking up roughly half the area of the LED package:



LGI1005, FIG. 1A (annotated). While Illek does not provide precise numerical values for the areas of its electrode pads, nor is the drawing above expected to be

---

<sup>2</sup> “LE package” in claim 10 appears to be a typo and should instead read “LED package.”

drawn perfectly to scale, such electrode pads would have been made as large as possible in order to ensure that the pads are easily aligned during flip-chip mounting and further so that heat generated during the flip-chip bonding process may be more easily dissipated through the large surface area of the pads. *See, e.g.*, LGI1013, 10:47-54.

119. To the extent Illek does not explicitly teach the claimed areas of the first and second pads, a POSITA would have found it obvious to configure Illek's pads to have an area not less than  $\frac{1}{3}$  of the LED package. This is because it was well-known at the time of the '664 Patent as well as Illek to maximize the size of the electrode pads used in flip chips in order to, among other things, facilitate alignment of the pads to the circuit board during mounting and to better dissipate heat generated during the mounting process. Indeed, a POSITA would have found it to be an almost mandatory design choice to make the electrode pads as large as possible without them touching each other (*i.e.*, shorting) in order to gain the benefits noted above. Specifically, LEDs are known to generate significant amounts of heat from a small area. If this heat is not dissipated, both the operating efficiency and the lifetime of the LED would be significantly reduced. Therefore a POSITA would be expected to maximize the ability of the electrode pads to dissipate heat by making them as large as possible.

120. Since there are typically two electrode pads, maximizing their size would mean that each takes up greater than  $\frac{1}{3}$  of the total area available on the LED package. In fact, prior art from the relevant time period, for example U.S. 7,554,126 to Higashi (LGI1013), explicitly mentions that each of the electrode pads are “set to a size that covers about half the LED chip.” LGI1013, 10:47-54. Thus, it would have been a simple and routine design choice for a POSITA maximize the areas of the electrode pads so that each one covers approximately half the area of the LED package (*i.e.*, an area not less than  $\frac{1}{3}$  of the LED package).

***[11a]: “The LED module of claim 8, further comprises a lens to adjust an orientation angle of light emitted from the LED package.”***

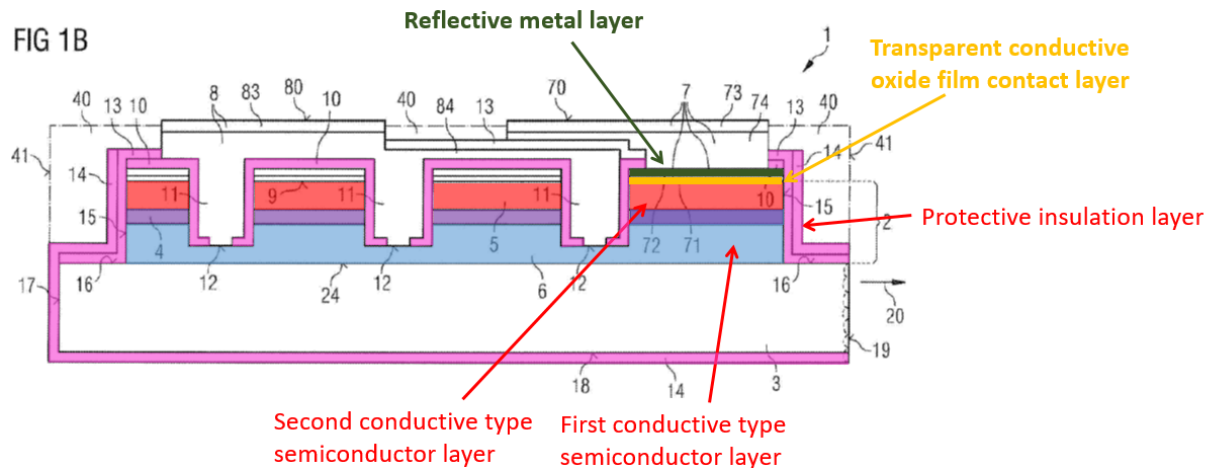
121. Illek’s LED module includes a lens to adjust an orientation angle of light emitted from the LED package. *See* Analysis of Element [6i], ¶ 106, *supra*; LGI1005, [0143].

***[12a]: “The LED module of claim 8, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”***

122. The protective insulation layer of Illek includes insulation layers having different indices of refraction from each other. *See* Analysis of Element [1f], ¶¶ 76-77, *supra*; LGI1005, [0013], [0131].

***[13a]: “The LED module of claim 12, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer; and”***

123. As I discussed above for claim 3, Illek's LED package includes a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer. *See* Analysis of Element [3a], ¶¶ 85-88, *supra*; LGI1005, FIG. 1B, [0103], [0106], [0107]; LGI1012, Abstract, 2:44-64, 7:26-35. The transparent conductive oxide film contact layer and the reflective metal layer over the second conductive type semiconductor layer has been labeled in the annotated drawing below:

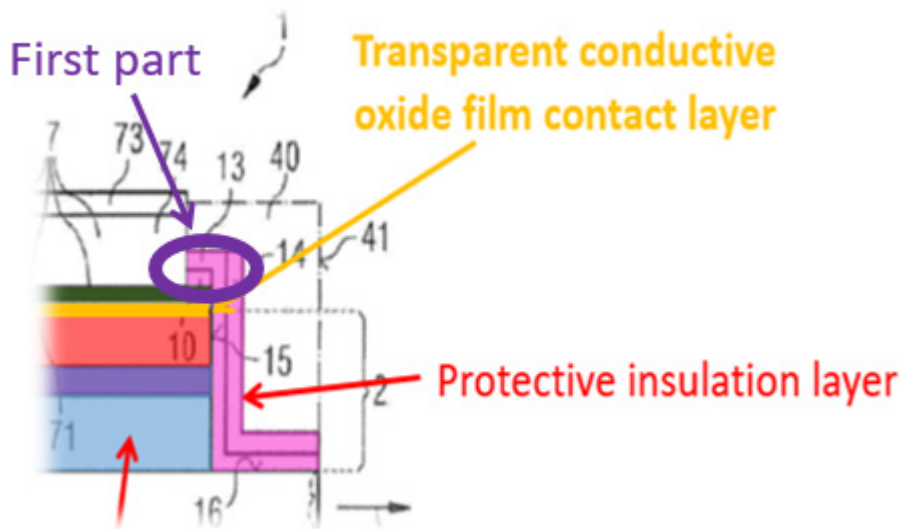


LGI1005, FIG. 1B (annotated).

***[13b]: “a first part of the protective insulation layer covering the contact layer.”***

124. Illek's LED package includes a first part of the protective insulation layer covering the contact layer. Specifically, as illustrated below, the protective insulation layer of Illek (layers 10, 13, and 14; pink) includes a horizontal portion, which I have labeled below as the “first part,” that covers the upper side of both the

transparent conductive oxide film contact layer (yellow) as well as the reflective metal layer (green):

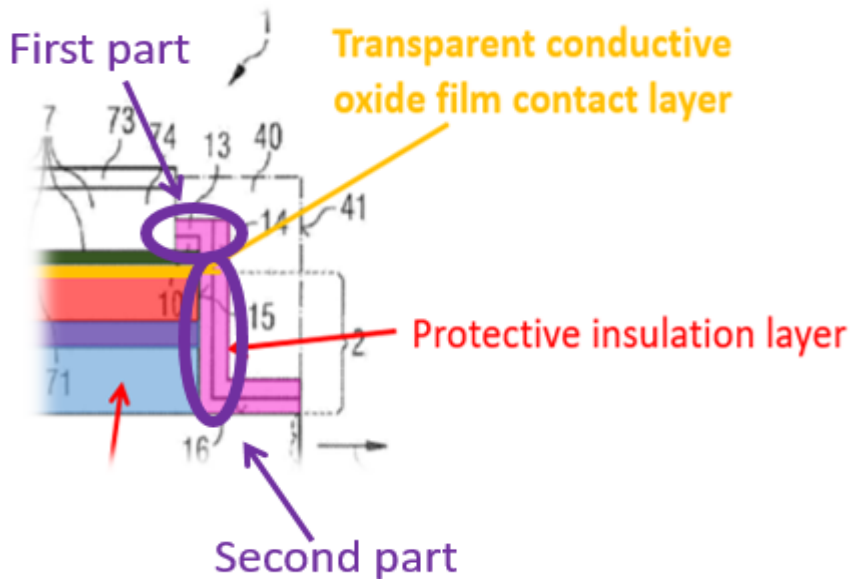


LGI1005, FIG. 1B (cropped, annotated).

***[14a]: “The LED module of claim 13, wherein a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer,”***

125. Illek's LED package includes a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer. Specifically, as illustrated below, the protective insulation layer of Illek (layers 10, 13, and 14; pink) includes a vertical portion, which I have labeled below as the “second part,” that covers the sidewall of the first conductive type semiconductor layer (blue):





LGI1005, FIG. 1B (cropped, annotated).

**[15a]: “The LED module of claim 14, wherein each area of the first and second pads is not less than  $\frac{1}{3}$  of area of the LED package.”**

127. In Illek’s LED module, each area of the first and second pads is not less than  $\frac{1}{3}$  of area of the LED package. See Analysis of Element [10a], ¶¶ 118-120, *supra*; LGI1005, FIG. 1A; LGI1013, 10:47-54.

**[16a]: “The LED module of claim 15, further comprising a wavelength convertor the opposite side of the LED package to the first and second electrode pads,”**

128. Illek’s LED module includes a wavelength convertor the opposite side of the LED package to the first and second electrode pads. See Analysis of Element [9a], ¶¶ 116, *supra*.

**[16b]: “wherein the wavelength converter comprises a phosphor sheet or an impurity-doped material.”**

129. Illek's wavelength converter includes a phosphor sheet or an impurity-doped material. *See* Analysis of Elements [2b], [9b], ¶¶ 82-84, 117 *supra*; LGI1005, [0143]; LGI1006, Abstract, 7:4-8, Claim 6.

***[17a]: "The LED module of claim 16, at least one of the contact holes has a circular shape, and"***

130. In Illek's LED module, at least one of the contact holes has a circular shape. *See* Analysis of Element [5a], ¶ 93, *supra*; LGI1005, FIG. 1A.

***[17b]: "wherein the plurality of the contact holes are arranged along at least one side surface of the LED package."***

131. In Illek's LED module, the plurality of the contact holes are arranged along at least one side surface of the LED package. *See* Analysis of Element [5b], ¶¶ 94-95, *supra*; LGI1005, FIG. 1A.

***[18a]: "The LED module of claim 17, further comprising a lens to adjust an orientation angle of light emitted from the LED package."***

132. Illek's LED module includes a lens to adjust an orientation angle of light emitted from the LED package. *See* Analysis of Element [6i], ¶ 106, *supra*.

## **IX. ANALYSIS OF ILLEK AND BEGEMANN WITH RESPECT TO CLAIMS 7 AND 19**

133. For the reasons articulated in detail below, and based on my review of the '664 patent and the Illek and Begemann references, I am confident that a POSITA would have readily understood that the predictable combination of Illek and Begemann provides all elements of claims 7 and 19.



134. An overview of Illek was provided above in ¶¶ 49-53 and is incorporated herein. Begemann, which is entitled “LED Lamp,” is generally directed to an LED lamp and discloses forming an LED array that is made up of a number of LED chips that are provided on a PCB. *See* LGI1008, Abstract, [0012].

135. I will now address each of the elements of claims 7 and 19, as follows.

***[7a]: “The LED module of claim 6, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and the LED packages is arranged over the MC-PCB.”***

136. Illek in view of Begemann discloses a metal core printed circuit board (MC-PCB) over which the LED package is arranged. As I explained above for element [6a], Illek generally teaches the use of a circuit board for mounting its LEDs. *See* Analysis of Element [6a], ¶¶ 97-98, *supra*; LGI1005, [0019]; [0099]; [0122]. However, Illek does not go into the details of which type of circuit boards should be used.

137. Begemann, which is similar to Illek as I discuss below, teaches a LED module in which LED chips are mounted on a PCB. LGI1008, [0012]. Furthermore, regarding the types of PCBs to be used in its LED application, Begemann explicitly describes that a metal core printed circuit board (MC-PCB) can be used. *Id.*, [0012], [0028].

138. Multiple reasons would have prompted a POSITA to incorporate Begemann’s MC-PCB to Illek’s LED module. As a first reason, I note that both

Illek and Begemann are structurally and functionally similar. For instance, both references are directed to an LED package that is mounted on a circuit board. Based on such similarities, a POSITA would have readily recognized that any advantages gained in Begemann by using an MC-PCB over a standard PCB would apply similarly to Illek. Among other things, Begemann mentions that MC-PCB is typically used in LED applications because they “have a relatively high heat conduction” and therefore provide “a very good heat dissipation from the LED arrays.” LGI1008, [0012]; *see also id.*, [0028].

139. A POSITA—recognizing the need for efficient thermal management in LED chips, which tend to generate a lot of heat—would have been motivated to use Begemann’s MC-PCB in Illek to help improve heat dissipation. In fact, Illek expressly recognizes the need to reduce “excessive internal temperatures within the [LED] component” to minimize “thermally induced damage to the [LED] component.” LGI1005, [0012]. In other words, a POSITA would have been motivated to mount Illek’s LED components onto an MC-PCB as taught by Begemann, instead of onto a standard PCB that exhibits less thermal conductivity, in order to provide improved heat dissipation to Illek’s LED components.

140. As a second reason, a POSITA would have considered the use of a specific type of PCB, such as Begemann’s MC-PCB, to be nothing more than a routine and conventional design choice. Indeed, given the widespread use of MC-

PCBs in LED applications during the relevant time period for improved heat dissipation, a POSITA would not have found anything new or inventive about choosing a particular type of PCB, namely an MC-PCB. *See, e.g.*, LGI1008, [0012]; LGI1009, [0093]. Adding the MC-PCB of Begemann to the LED module of Illek amounts to nothing more than combining well-known prior art elements from the same field according to known methods in order to yield predictable results.

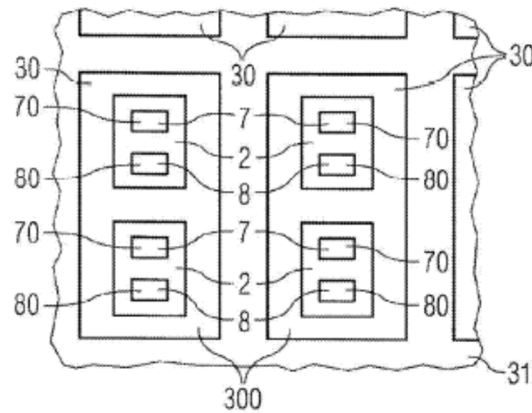
***[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”***

141. Illek in view of Begemann discloses wherein the circuit board comprises a metal core printed circuit board (MC-PCB). *See* Analysis of Element [7a], ¶¶ 136-140, *supra*.

***[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”***

142. Illek in view of Begemann discloses wherein a plurality of the LED packages is arranged on the MC-PCB. In particular, as illustrated below, Illek discloses arranging a plurality of LED packages over an auxiliary carrier (*i.e.*, a circuit board):

FIG 3A



LGI1005, FIG. 3A; [0169]. Moreover, as discussed above for element [7a], a POSITA would have found it obvious to use Begemann's MC-PCB with Illek's LEDs to improve heat dissipation. *See* Analysis of Element [7a], ¶¶ 136-140, *supra*.

143. Furthermore, Begemann expressly discloses arranging *a plurality of LED packages*, onto its MC-PCB, as shown below:

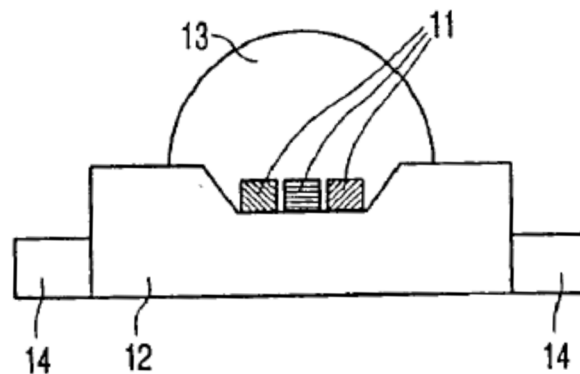


FIG. 3B

LGI1008, FIG. 3B; [0029]. Indeed, a POSITA would have found the act of mounting a plurality of LED packages onto an MC-PCB to be nothing more than a routine and conventional design choice. This is particularly true because, as Begemann demonstrates, the act of arranging a plurality of LED packages on an MC-PCB was commonly done in the field of LED design and manufacturing during the relevant time period. Incorporating the multiple-chip configuration of Begemann into the LED device of Illek amounts to nothing more than combining prior art elements from the same field according to known methods to yield predictable results.

#### **X. ANALYSIS OF DONOFRIO AND SANO WITH RESPECT TO CLAIMS 1-19**

144. For the reasons articulated in detail below, and based on my review of the '664 patent and the Donofrio and Sano references, I am confident that a POSITA would have readily understood that the predictable combination of Donofrio and Sano (“the Donofrio-Sano combination”) provides all elements of claims 1-19.

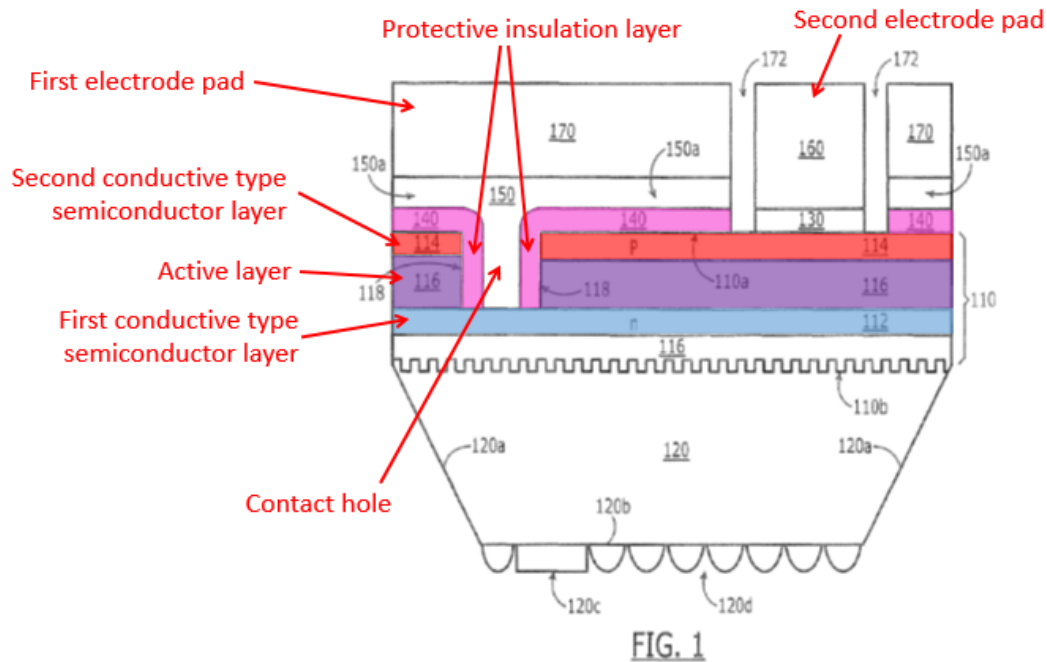
145. Donofrio, which has the title of “Semiconductor Light Emitting Diodes Having Reflective Structures and Methods of Fabricating Same,” generally describes LEDs having “a diode region having first and second opposing faces that include therein an n-type layer and a p-type layer, an anode contact that ohmically

contacts the p-type layer and extends on the first face, and a cathode contact that ohmically contacts the n-type layer and also extends on the first face.” LGI1009, Abstract.

146. Donofrio describes a conventional semiconductor stack made up of “an n-type layer 112 and a p-type layer 114” as well as an active region 116 that is positioned between those layers. *Id.*, [0040]-[0042]. Donofrio also teaches a via 118 that is etched to expose the underlying n-type layer 112. *Id.* Donofrio also teaches other conventional LED elements such as an anode pad 160 and a cathode pad 170. *Id.*, [0043].

147. Donofrio further teaches an insulating layer 140 that covers the sidewall of its via 118. In particular, the insulating layer 140 of Donofrio “may comprise multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector.” *Id.*, [0041].

148. As illustrated below, the overall resulting structure of Donofrio’s LED component is highly similar to the LED structure described in the ’664 Patent. Among other things, Donofrio’s LED component includes first and second conductive type semiconductor layers (n-type layer 112 and p-type layer 114, shown in blue and red, respectively), an active layer (active region 116, shown in purple), and a protective insulation layer (insulating layer 140, shown in pink).



LGI1009, FIG. 1 (annotated). As shown above, Donofrio also teaches a plurality of contact holes (vias 118) along with the first and second electrode pads (cathode pad 170 and anode pad 160).

149. Sano is entitled “Light Emitting Element and Light Emitting Device Provided with the Element” and is generally directed to “a light emitting device capable of emitting a light emitting wavelength with desired color in high power and which has excellent weather resistance.” LGI1011, Abstract. Similar to Donofrio, Sano discloses a protective insulation layer that covers a sidewall of the semiconductor stock, namely a “dielectric multilayer film 4” that is “a multilayer structure in which two or more types of material films having different refractive indexes are alternately laminated, and is provided in at least a part between the semiconductor structure 11 and the electrode 3.” LGI1011, [0030].

150. Based on my review of the intrinsic record of the '664 patent and Illek, and my knowledge and experience in the field, it is my opinion that all the elements of claims 1-19 are disclosed by the predictable combination of Donofrio and Sano. As part of my analysis, I will address each of the elements of claims 1-19, as follows.

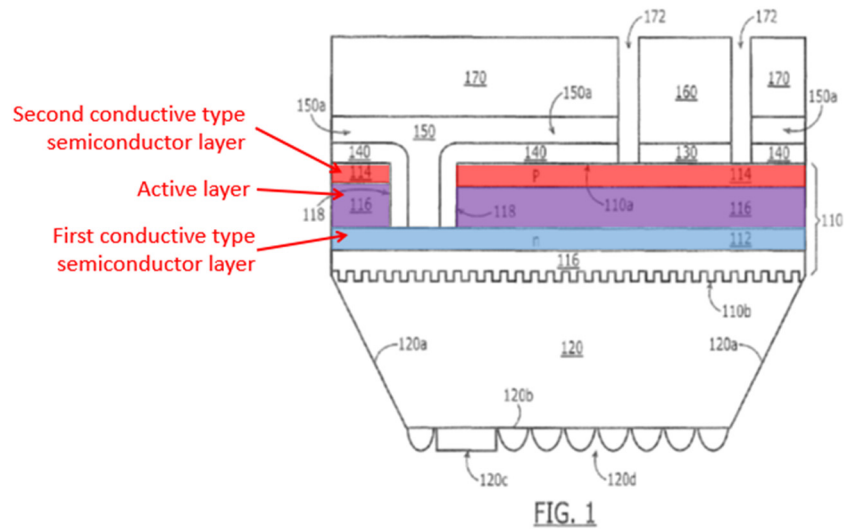
***[1pre]: “A light emitting diode (LED) package, comprising:”***

151. Even if the preamble here were considered to be a limiting element of claim 1, Donofrio discloses a light emitting diode (LED) package. For example, Donofrio teaches “an LED that is suitable for flip-chip mounting” and is generally directed to “LED chips.” LGI1009, [0046], [0050]. As used here, an LED chip is equivalent to an LED package.

***[1a]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

152. Donofrio’s LED package includes a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer. For example, as illustrated below, the diode region 110 of Donofrio is a semiconductor stack that includes an n-type semiconductor layer 112 (blue), a region 116 (purple), and a p-type semiconductor layer 114 (red):





LGI1009, FIG. 1 (annotated); [0040]; [0052]. The n-type semiconductor layer 112 (blue) and the p-type semiconductor layer 114 (red) very clearly refer to the claimed first conductive type semiconductor layer and the second conductive type semiconductor layer, respectively.

153. As for its region 116, Donofrio generally describes “[o]ther layers or regions 116” of the “diode region 110” that “need not be described herein.”

LGI1009, [0040]. Donofrio also talks elsewhere about an “active region” that emits light such that the LED emits “visible light from the diode region 110.”

LGI1009, [0052]; [0055]; [0059]; [0062]; [0064]; [0102]. So although Donofrio doesn’t use the term “active layer” to describe its layer 116, a POSITA would have clearly understood from Donofrio’s overall disclosure, in conjunction with a decades-old understanding of how LEDs work, that the layer 116, which is

sandwiched between Donofrio's n-type semiconductor layer 112 and the p-type semiconductor layer 114, is indeed the light emitting "active layer."

***[1b]: "a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;"***

154. Donofrio's LED package includes a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer. For example, Donofrio describes "a via 118 [that] extends into the first face 110a to expose the n-type layer 112." LGI1009, [0042]. The vias 118 of Donofrio, which I have marked below in yellow, correspond to the claimed "plurality of contact holes":

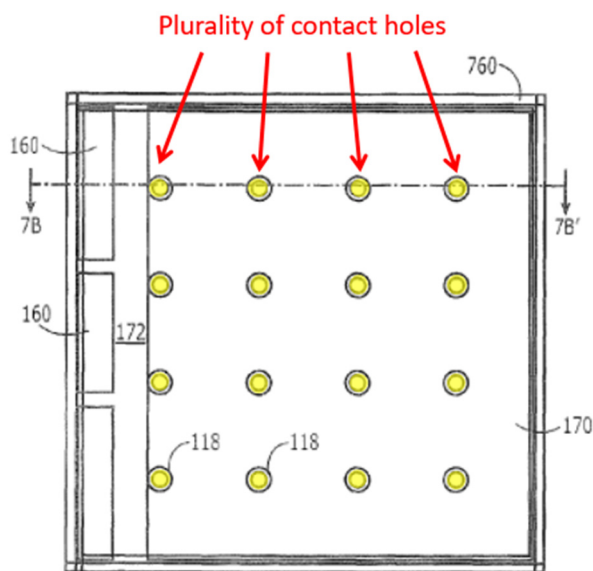


FIG. 7A

LGI1009, FIG. 7A (annotated); [0077]. And as clearly indicated in the drawing below, the plurality of contact holes of Donofrio (the general locations of which

are highlighted in yellow) are arranged in the second conductive type semiconductor layer (red) and the active layer (purple) and further expose the first conductive type semiconductor layer (blue):

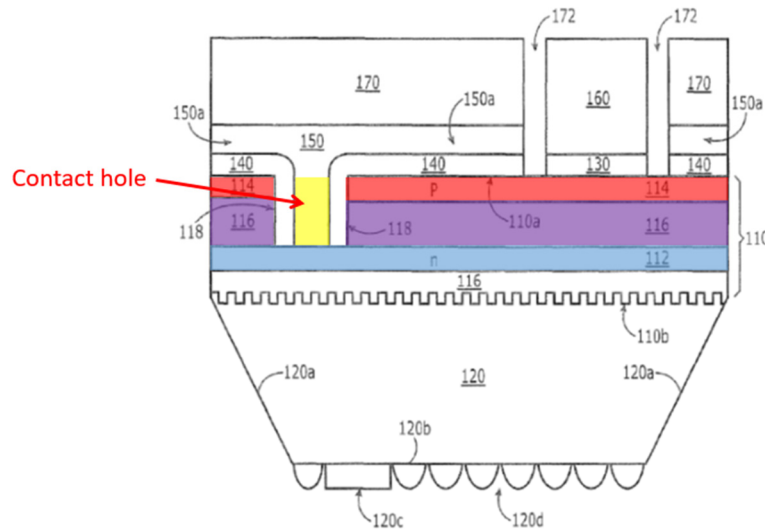


FIG. 1

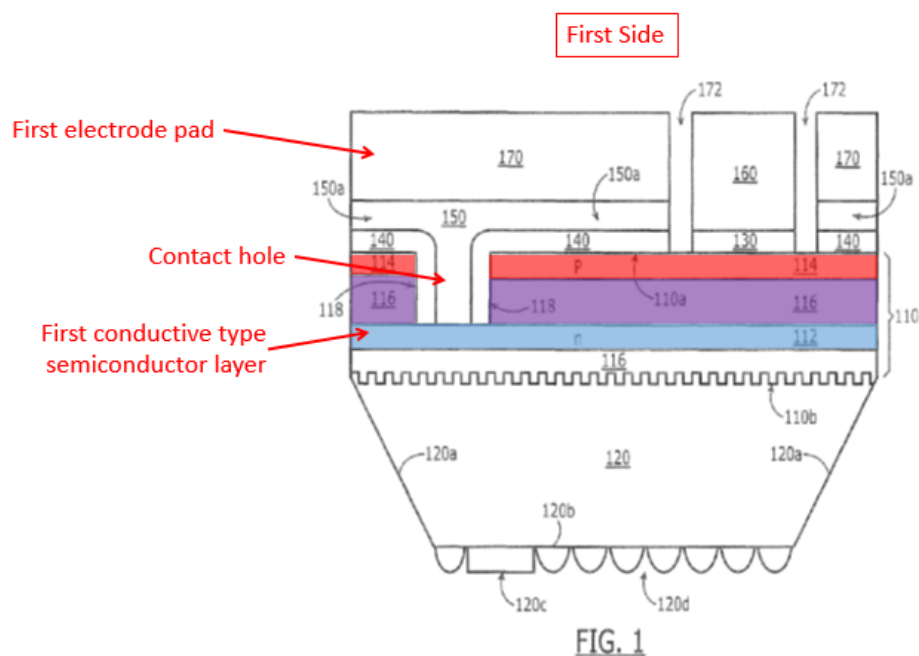
LGI1009, FIG. 1 (annotated); [0042].

**[1c]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”**

155. Donofrio’s LED package includes a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes. In particular, Donofrio teaches a “cathode pad 170” which corresponds to the claimed first electrode pad and which is electrically connected to the n-type layer 112 (*i.e.*, first conductive type semiconductor layer;

shown in blue) via a “cathode contact 150” that extends through the plurality of contact holes. LGI1009, [0041]-[0043].

156. In short, as I have shown in the annotated figure below, the first electrode pad of Donofrio (*i.e.*, cathode pad 170) is arranged over a first side of the semiconductor stack and electrically connected to the first conductive type semiconductor layer (*i.e.*, n-type layer 112) via some of the plurality of contact holes (*i.e.*, via 118):

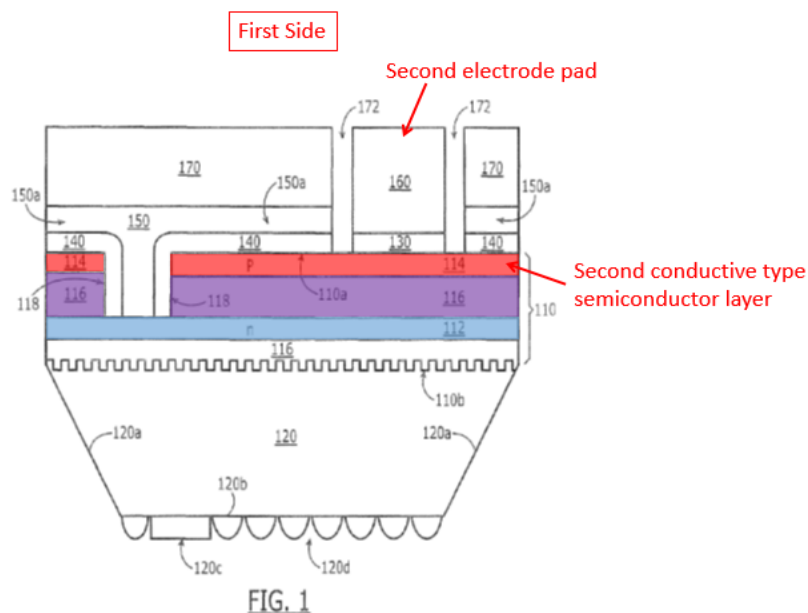


LGI1009, FIG. 1 (annotated). While Donofrio doesn’t use the term “first side,” I have marked above the side of Donofrio’s LED that corresponds to the claimed “first side.”

***[1d]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

157. Donofrio’s LED package includes a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer. In particular, Donofrio discloses an “anode pad 160” that is electrically connected to the p-type layer 114 via the anode contact 130.” LGI1009, [0041], [0043].

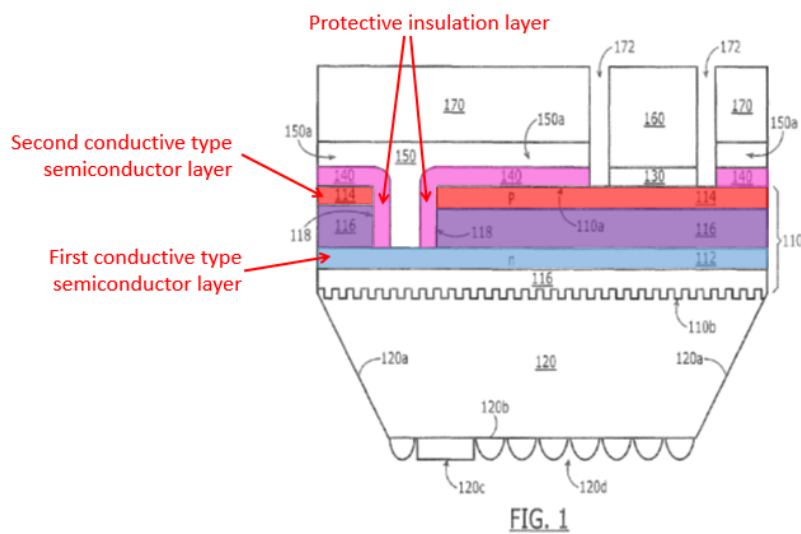
158. That is, as shown in the illustrated figure below, the second electrode pad of Donofrio (*i.e.*, anode pad 160) is arranged over a first side of the semiconductor stack and is further electrically connected to the second conductive type semiconductor layer (*i.e.*, p-type layer 114):



LGI1009, FIG. 1 (annotated).

***[1e]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”***

159. Donofrio’s LED package includes a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer. Specifically, referring to annotated FIG. 1 below, Donofrio discloses an “insulating layer 140 [that] extends into the via 118,” the via 118 having been etched through the semiconductor stack to expose the first conductive type semiconductor layer (*i.e.*, n-type layer 112; shown in blue):



LGI1009, FIG. 1 (annotated); [0042]; [0073].

160. That is, as shown in the drawing above, the “insulating layer 140 is provided on the sidewalls of the via 118” and clearly covers a sidewall of the semiconductor stack that is exposed at the via 118. LGI1009, [0061].

Accordingly, the insulating layer 140 (shown in pink above) acts as a passivation

layer, effectively providing a protective coating for the underlying semiconductor stack to help reduce electrical and chemical reactivity at the surface as well as throughout the bulk. Such passivation of the semiconductor body can help protect against undesirable metal diffusion as well as short-circuits, which would negatively affect performance and lifetime.

161. Here, I note that although Donofrio very clearly shows a protective insulation layer 140 that covers the sidewall of the semiconductor stack, including the active layer and the second conductive type semiconductor layer, Donofrio does not appear to explicitly show that sidewalls of both the first and second conductive type semiconductor layers, as recited in element [1e], are covered by the layer 140. That is, referring back to the annotated FIG. 1 above, the etched via 118 (and therefore the layer 114) is illustrated as stopping perfectly at the boundary between the active region 116 (purple) and the n-type layer 112 (blue). LGI1009, [0073].

162. A POSITA, however, would have recognized that the etching of a via 118 through multiple semiconductor layers as in Donofrio cannot be perfectly controlled such that the via 118 stops at the precise boundary between the active layer 116 and the n-type layer 112 (i.e. first conductive type semiconductor layer) as illustrated without at least partially etching into the layer 112 (which is trying to be exposed for electrical contact). In particular, a POSITA would understand that

it is impossible to perfectly control the processes used to deposit semiconductor films. Thus the exact etch depth to expose the first conductive type semiconductor layer will vary about an average value. Therefore in order to guarantee that the first conductive type layer is exposed the etch process would be designed to etch at least as much as the maximum thickness of the overlying semiconductor layers. In practice this means that some portion of the first conductive type semiconductor layer is also removed during the etch process.

163. U.S. Patent No. 6,448,657 to Dorleans (LGI1015) provides an illustration of this concept. Specifically, Dorleans, which is directed generally to the etching of a contact via as in the '664 patent, teaches that “[d]uring etching of contact vias, some degree of overetch into the underlying silicon substrate 12 *is necessary to ensure that the contacts are completely open.*” LGI1015 at 3:44-51.

164. Thus, not only would etching a recess that stops precisely at the surface of the layer being exposed (*e.g.*, Donofrio’s n-type layer 112) have been extremely difficult, if not impossible, to control during manufacturing, a POSITA would have in reality *purposely overetched* into the layer being exposed—in the case of Donofrio the n-type layer 112—in order to ensure that electrical contact will be made to the n-type layer 112. Without such overetch, parts of the active layer 116 may remain on top of the n-type layer 112 and in turn degrade LED performance.



165. Therefore, as I show in annotated FIG. 1 below which I have modified to more accurately depict the above-mentioned etching process, the via 118 would have been at least partially etched into the n-type layer 112 (blue), and the protective insulation layer (pink) would have extended into that region as well (circled in red):

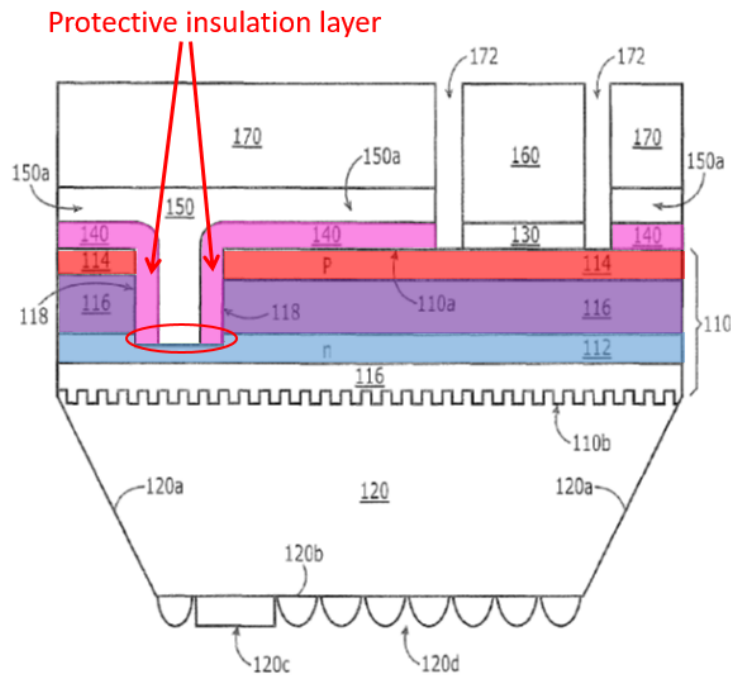
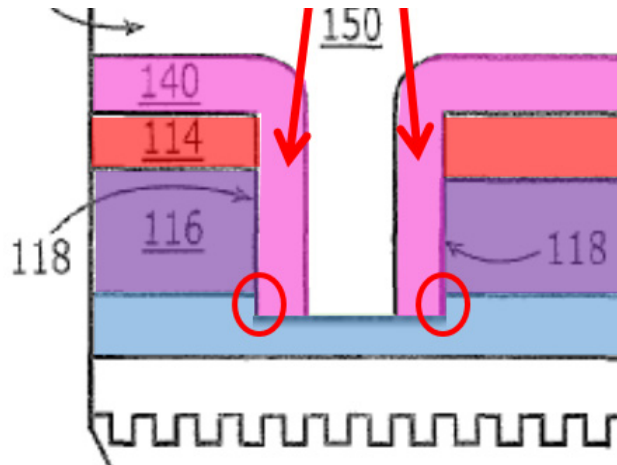


FIG. 1

LGI1009, FIG. 1 (modified, annotated). If not for this overetch into the n-type layer 112, parts of the active layer 116 may remain on top of the n-type layer 112 and prevent ohmic contact between the contact 150 and the n-type layer. A slight overetch into the n-type layer, as would have been commonly understood by a POSITA, would ensure good electrical contact and result in the following configuration:

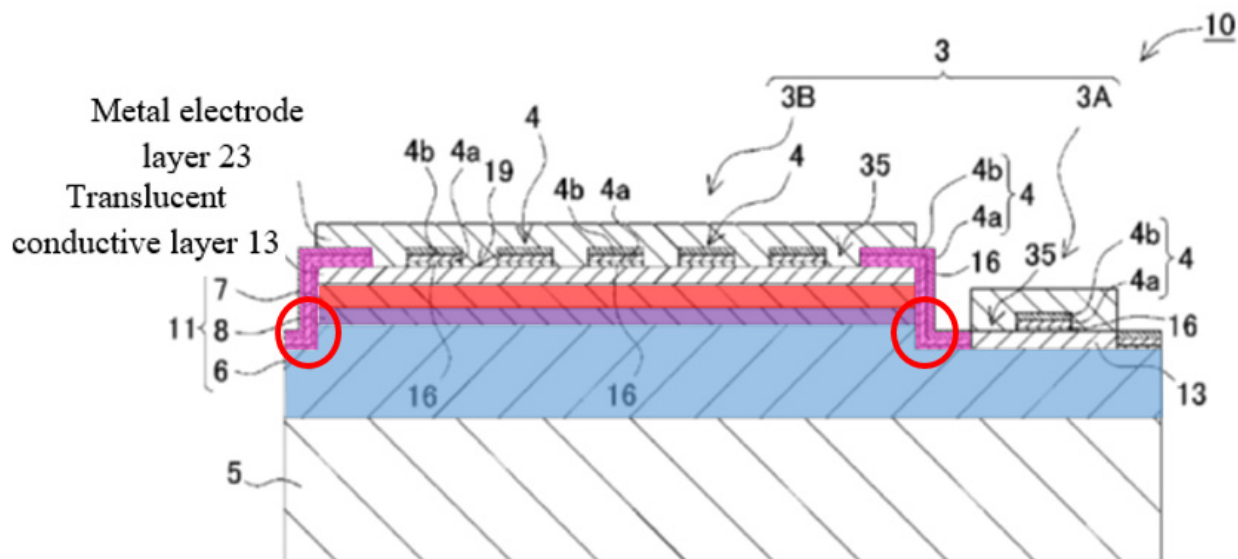


LGI1009, FIG. 1 (modified, cropped, annotated). In the figure above, it can be seen that the protective insulation layer 140 covers the sidewalls of both the p-type layer 114 (red) as well as the sidewall of the n-type layer 112 (blue).

166. Moreover, a plethora of prior art references during the relevant time period further demonstrate the obviousness of a protective insulation layer that covers a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer. For example, Sano (LGI1011) teaches an LED semiconductor stack where the “p-type semiconductor layer 7 [is] selectively etched and removed to expose a part of the n-type semiconductor layer 6.”

LGI1011, [0033]. This is analogous to the teaching in Donofrio where “a via, such as via 118, is etched through a p-type layer, such as a p-type layer 114...to expose an n-type layer, such as an n-type layer 11.” LGI1009, [0073].

167. Referring to the cross-section of Sano below, the aforementioned overetch that would have resulted in the protective insulation layer (pink) covering the sidewall of the n-type layer (blue) can be observed:



LGI1011, FIG. 3 (annotated). In other words, due to the expected overetching into the layer that is being exposed for electrical contact, the protective insulation layer (pink) ends up covering the sidewall of not just the p-type layer 7 (red) but that of the n-type layer 6 (blue) as well. LGI1011, [0030]; [0038]; *see also* LGI1015 at 3:44-51, FIG. 2.

168. Multiple reasons would have prompted a POSITA to incorporate Sano's etching into the n-type layer to Donofrio's via etching process. As a first reasons, I note that both Donofrio and Sano teach etching through the claimed semiconductor stack in order to expose and make electrical contact with the n-type layer. Given this shared structural and functional outcome, a POSITA would have

known that any advantages achieved by Sano's fabrication process would similarly improve Donofrio's. For instance, by overetching into the first semiconductor layer (*i.e.*, n-type layer 112) in Donofrio, as taught by Sano, a POSITA would have been able to more reliably establish electrical connection between the first electrode pad and the first semiconductor layer as in Sano. *See also* LGI1015 at 3:44-51. Otherwise, without such overetching, any minor variations in processing conditions could lead to the n-type layer not becoming exposed and subsequently result in no electrical connectivity to that region, which is undesirable.

169. As a second reason, a POSITA would have considered the partial etching of the layer being exposed for electrical contact, as shown in Sano, to be a routine and conventional design choice given the well-established nature of such overetching during the relevant time period.

170. Not surprisingly, many other references from the relevant time period that teach multi-layer etching to expose the bottom layer for electrical contact demonstrates that the bottom layer is indeed partially etched into. *See, e.g.*, LGI1005, FIG. 1B; LGI1013, FIG. 1. That is, there is nothing new or inventive about extending the contact hole into the first semiconductor layer and subsequently covering the resulting sidewall of the first semiconductor layer with the protective insulation layer. In other words, incorporating the overetching of Sano into the etching process of Donofrio amounts to nothing more than

combining well-known prior art elements from the same field according to known methods to yield predictable results.

***[1f]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”***

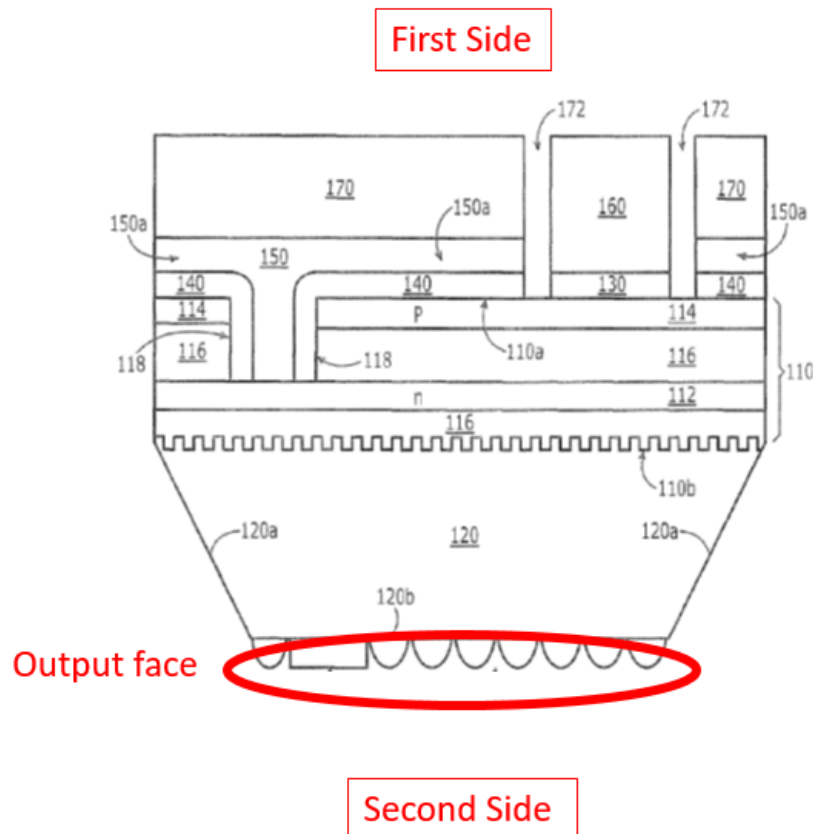
171. The protective insulation layer of Donofrio includes insulation layers having different indices of refraction from each other. Specifically, Donofrio’s insulating layer 140, which corresponds to the claimed protective insulation layer, can be made up of “multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector.” LGI1009, [0041].

Alternating layers of oxide and nitride, for instance, would certainly provide different indices of refraction from each other. Further, a “distributed Bragg reflector” is a well-known structure that is, as recognized by the ’664 Patent, “formed by alternately stacking insulation layers having different indices of refraction.” LGI1001, 6:3-7. Accordingly, the Donofrio-Sano combination renders obvious claim 1.

***[2a]: “The LED package of claim 1, further comprising a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack,”***

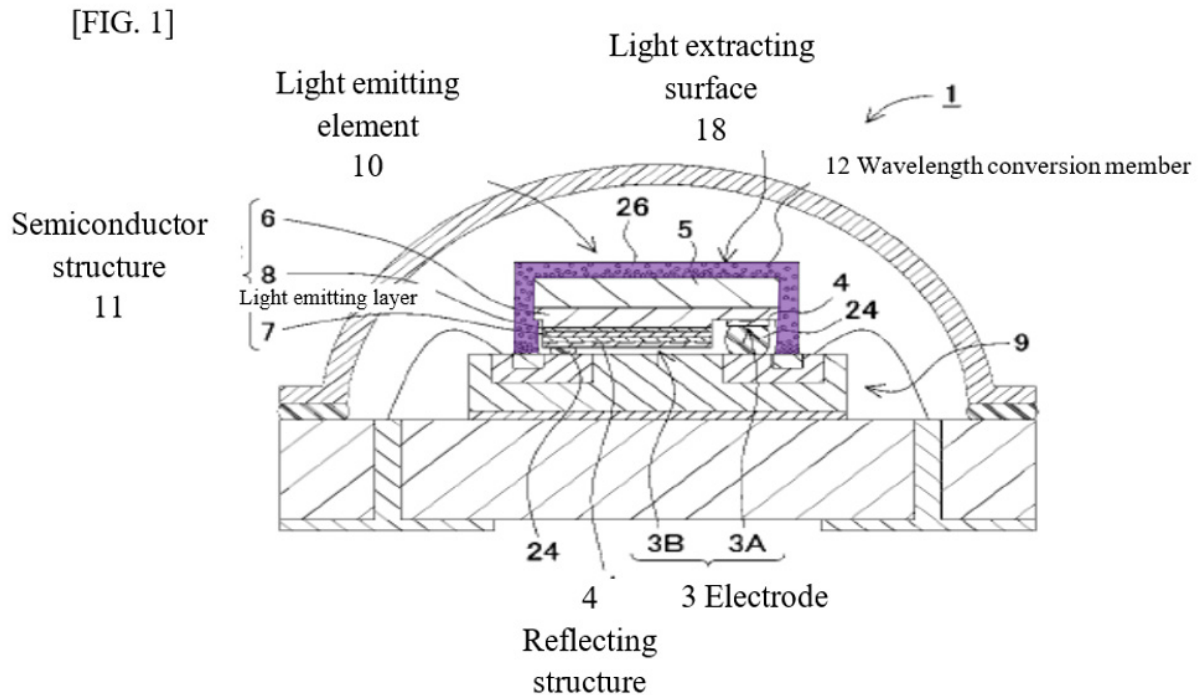
172. Donofrio’s LED package includes a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack. Specifically, Donofrio describes the use

of “wavelength conversion material such as phosphor.” LGI1009, [0004]. While Donofrio provide further details about where this wavelength conversion material would be located, a POSITA would have known that it would be arranged over the output face of the LED package, as illustrated below:



LGI1009, FIG. 1 (annotated). Illek, which I analyzed above, confirms that the wavelength conversion layer should be applied over the output face to convert the wavelength of outgoing light. LGI1005, [0143]. The same configuration would be applicable to Donofrio.

173. Additionally, Sano also teaches arranging a wavelength conversion member 12 over the light extracting surface 18 of a flip-chip mounted LED package:



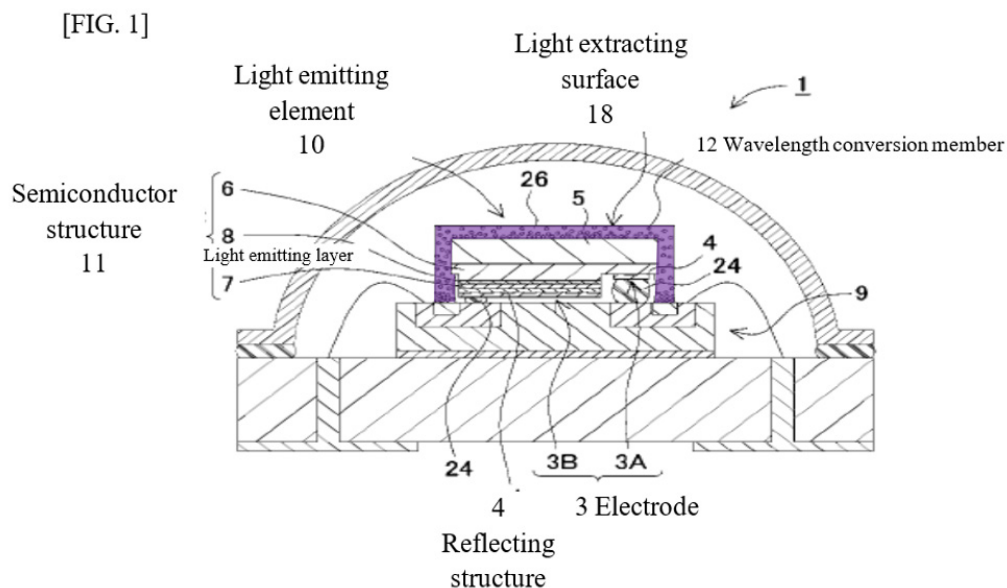
LGI1011, FIG. 1 (annotated); [0020]-[0022], [0028]. This configuration ensures that the “desired light” can be emitted from the LED device. *Id.*, [0028].

174. Based on this teaching of Sano, a POSITA would have found it obvious to implement Sano’s wavelength conversion member to Donofrio’s LED package. For instance, because Sano explicitly teaches that its wavelength conversion member can be applied to the output side (*i.e.*, “second side”) of flip-chip mounted LED devices, such as those of Donofrio, to emit the desired wavelength of light, a POSITA would have been able to readily incorporate Sano’s

wavelength conversion member to the output face of Donofrio’s flip-chip mounted LED chip to achieve the same result. LGI1011, [0028]. That is to say, because Donofrio already teaches the use of a wavelength conversion material, a POSITA would simply be relying on the compatible structure of Sano for details on how to actually implement the wavelength conversion material. Accordingly, element [2a] is rendered obvious in view of Donofrio and Sano.

***[2b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”***

175. The wavelength convertor of Donofrio comprises a phosphor sheet or an impurity-doped material. In particular, Donofrio discloses that “wavelength conversion material such as phosphor” may be used. LGI1009, [0004]. Furthermore, according to Sano, such phosphor-based wavelength converters can be applied in the form of a sheet, as highlighted in purple below:



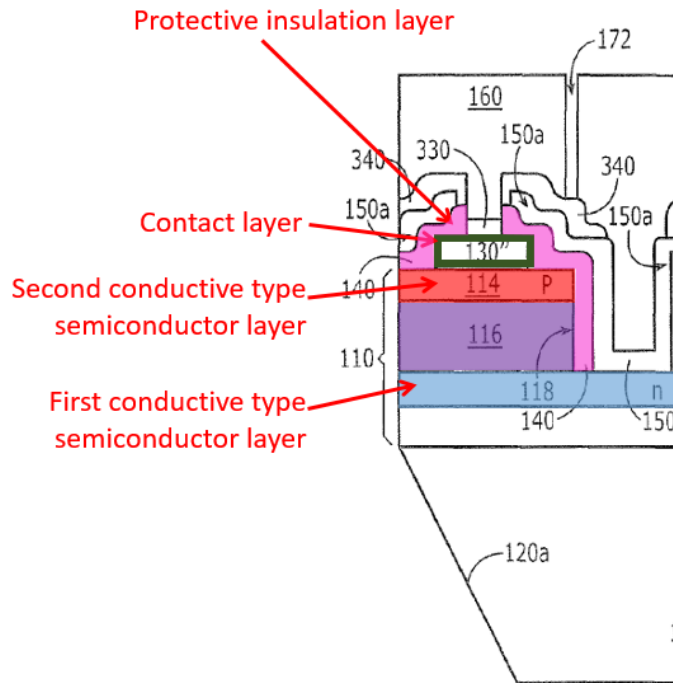


LGI1011, FIG. 1 (annotated); [0020]-[0022], [0028]. Thus, the Donofrio-Sano combination renders element [2b] obvious.

176. Sano additionally teaches that the wavelength convertor can include an impurity-doped material. For instance, Sano mentions that the following materials can be used to form the wavelength conversion member: BAM:Mn, CaAlSiN<sub>3</sub>:Eu, (Re<sub>1-x</sub>Sm<sub>x</sub>)<sub>3</sub>(AlGa)<sub>5</sub>O<sub>12</sub>:Ce ( $0 \leq x < 1$ ,  $0 \leq y \leq 1$ ), (Sr<sub>x</sub>Mae<sub>1-x</sub>)<sub>2</sub>SiO<sub>4</sub>:Eu, Sr-Ca-Si-N:Eu, Ca-Si-N:Eu, Sr-Si-N:Eu, Sr-Ca-Si-O-N:Eu, Ca-Si-O-N:Eu, Sr-Si-O-N:Eu, LSi<sub>2</sub>O<sub>2</sub>N<sub>2</sub>:Eu, L<sub>x</sub>Si<sub>y</sub>N<sub>(2/3x+4/3y)</sub>:Eu. LGI1011, [0022], [0075], [0077]. Each of these materials are indeed impurity doped materials, as indicated by their chemical formula. And for reasons I discussed above for element [2a], a POSITA would have been able to readily apply Sano's wavelength conversion member to Donofrio's LED device. Accordingly, the Donofrio-Sano combination renders obvious element [2b].

***[3a]: "The LED package of claim 1, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer"***

177. The Donofrio-Sano combination renders obvious element [3a]. In particular, Donofrio's LED package, as illustrated below, can include a "transparent anode contact 130" (*i.e.*, transparent conductive oxide film contact layer; highlighted in green) that is positioned over the second conductive type semiconductor layer 114 (red):



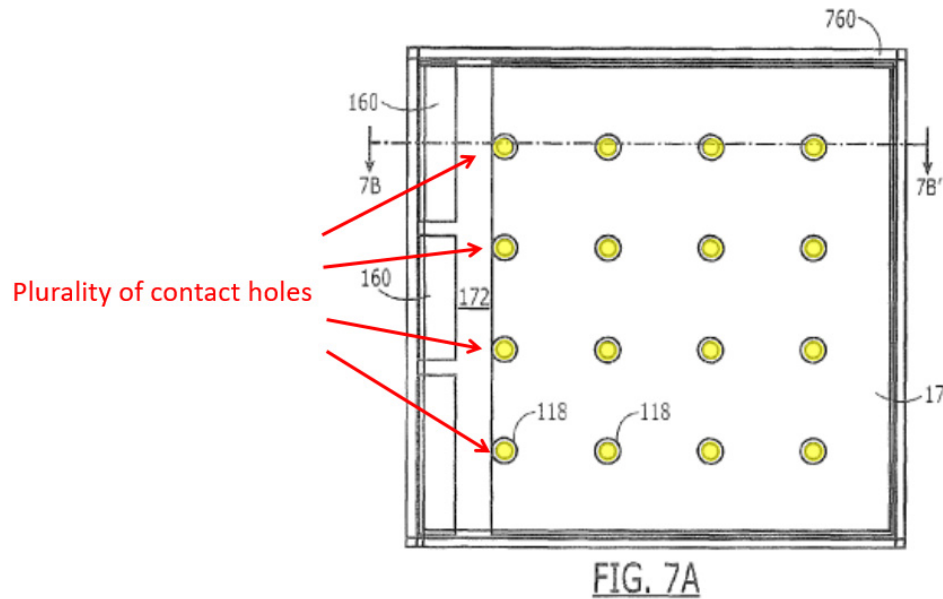
LGI1009, FIG. 3 (cropped, annotated); [0065]. Donofrio teaches that this transparent anode contact layer “may be a transparent conductive oxide, such as indium tin oxide (ITO).” LGI1009, [0065].

***[3b]: “a part of the transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer.”***

178. The Donofrio-Sano combinations renders obvious element [3b]. In particular, as illustrated below, Donofrio’s LED package can include a transparent conductive oxide film contact layer (green) that is partially located between the second conductive type semiconductor layer 114 (red) and a horizontal portion of the protective insulation layer 140 (pink):



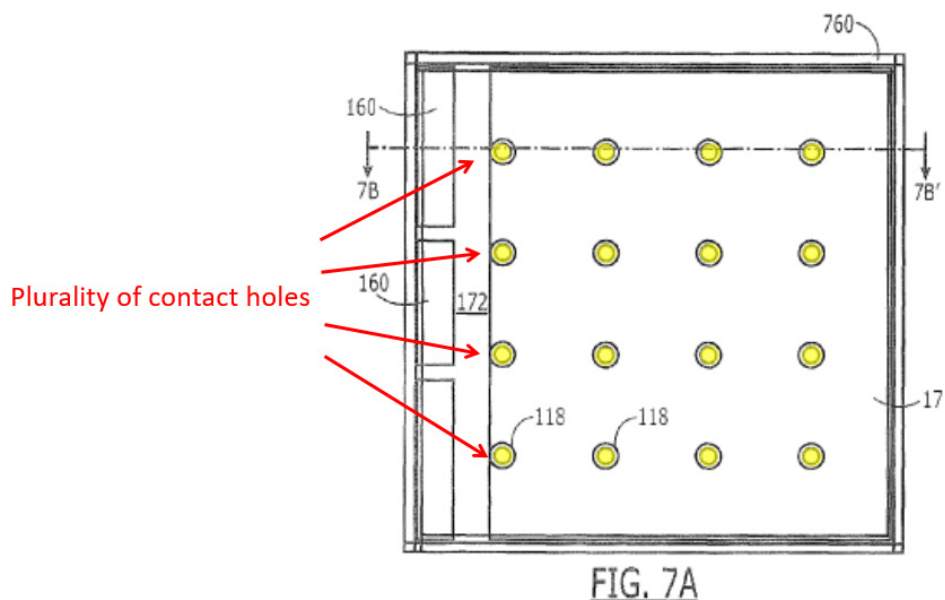
Donofrio's LED package below, the contact holes of Donofrio (vias 118, shown in yellow) are circular in shape:



LGI1009, FIG. 7A (annotated).

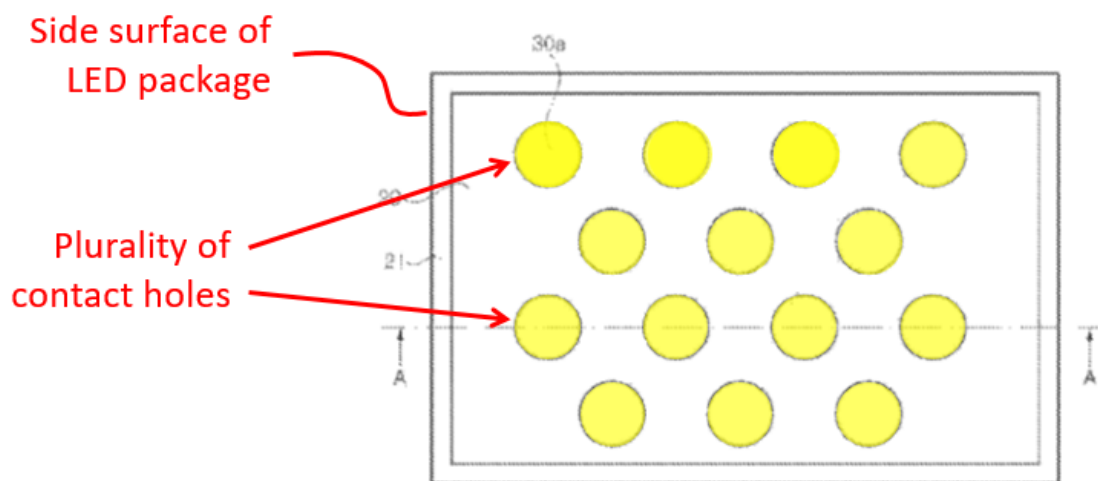
***[5b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”***

181. The Donofrio-Sano combination renders obvious that the plurality of the contact holes are arranged along at least one side surface of the LED package. Indeed, as seen in the top-down view of Donofrio's LED package below, the contact holes of Donofrio (vias 118, shown in yellow) are arranged along at least one side surface of the LED package:



LGI1005, FIG. 7A (annotated).

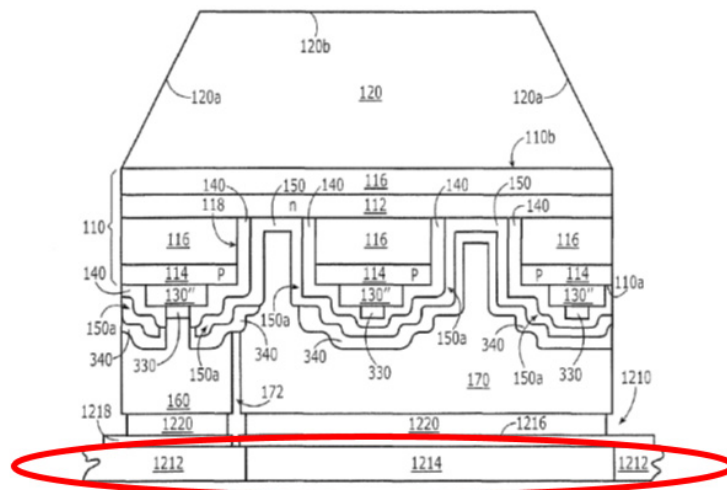
182. The way that Donofrio’s contact holes are “arranged along at least one side surface” is analogous to the way the contact holes are arranged with respect to the side surface in the ’664 Patent, as illustrated below:



LGI1001, FIG. 5(a) (annotated).

**[6pre]: “A light emitting diode (LED) module, comprising:”**

183. Even if the preamble here were considered to be a limiting element of claim 6, Donofrio discloses a light emitting diode (LED) module. As an initial matter, as I explained above for element [1pre], Donofrio teaches an LED component. LGI1009, [0046], [0050]. Moreover, Donofrio teaches that its LED component is “suitable for flip-chip mounting” and can be “mounted on a supporting substrate, such as a printed circuit board or other wiring board.” LGI1009, [0046]. An LED component or package that is mounted on a circuit board in this manner is referred to in the industry as a LED module. *See* LGI1014, 4 (Defining “LED array or module” as “[a]n assembly of LED packages (components), or dies on a printed circuit board or substrate.”). The LED component of Donofrio that has been mounted on a mounting substrate 1210 (circled in red) is shown below:



LGI1009, FIG. 12 (annotated); [0091].

***[6a]: “a circuit board;”***

184. The Donofrio-Sano combination renders obvious a circuit board. In particular, Donofrio expressly teaches that its LED package is to be “mounted on a supporting substrate, such as a printed circuit board or other wiring board.”

LGI1009, [0046]; FIG. 12. As explained in [6pre], the LED component of Donofrio may be mounted, for instance, on a mounting substrate 1210. *Id.*, [0091].

***[6b]: “a LED package arranged over the circuit board without bonding wires, wherein the LED package includes:”***

185. The Donofrio-Sano combination renders obvious a LED package arranged over the circuit board without bonding wires. In particular, Donofrio teaches that its LED package is “suitable for flip-chip mounting.” LGI1009, [0046]. A flip-chip architecture, which I explained above is a very common configuration that is used in Donofrio as well as the ’664 Patent, allows the LED package to be mounted directly to the substrate (*e.g.*, circuit board) without using any bonding wires. A POSITA would have readily recognized that a flip-chip device, like in Donofrio, dispenses with the need for bonding wires.

***[6c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

186. The Donofrio-Sano combination render obvious element [6c]. *See* Analysis of Element [1a], ¶¶ 152-153, *supra*.

***[6d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”***

187. The Donofrio-Sano combination renders obvious element [6d]. *See*

Analysis of Element [1b], ¶ 154, *supra*.

***[6e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”***

188. The Donofrio-Sano combination renders obvious element [6e]. *See*

Analysis of Element [1c], ¶¶ 155-156, *supra*.

***[6f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

189. The Donofrio-Sano combination renders obvious element [6f]. *See*

Analysis of Element [1d], ¶¶ 157-158, *supra*.

***[6g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”***

190. The Donofrio-Sano combination renders obvious element [6g]. *See*

Analysis of Element [1e], ¶¶ 159-170, *supra*.

***[6h]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and”***

191. The Donofrio-Sano combination renders obvious element [6h]. *See*

Analysis of Element [1f], ¶ 171, *supra*.





substrates, may be used to mount many of the embodiments described herein in a flip-chip configuration.” LGI1009, [0093].

***[8pre]: “A light emitting diode (LED) module, comprising:”***

194. To the extent the preamble here is limiting, the Donofrio-Sano combination renders obvious a light emitting diode (LED) module. *See* Analysis of Element [6pre], ¶ 183, *supra*.

***[8a]: “a circuit board;”***

195. The Donofrio-Sano combination renders obvious element [8a]. *See* Analysis of Element [6a], ¶ 184, *supra*.

***[8b]: “a LED package bonded on the circuit board without bonding wires; wherein the LED package comprising”***

196. The Donofrio-Sano combination renders obvious element [8b]. *See* Analysis of Element [6b], ¶ 185, *supra*. Indeed, a flip-chip architecture, as found in Donofrio allows the LED chip to be bonded directly on the circuit board without using wires.

***[8c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”***

197. The Donofrio-Sano combination renders obvious element [8c]. *See* Analysis of Elements [1a], [6c], ¶¶ 152-153, 186, *supra*.

***[8d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”***

198. The Donofrio-Sano combination renders obvious element [8d]. *See* Analysis of Elements [1b], [6d], ¶¶ 154, 187, *supra*.

***[8e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”***

199. The Donofrio-Sano combination renders obvious element [8e]. *See* Analysis of Elements [1c], [6e], ¶¶ 155-156, 188, *supra*.

***[8f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”***

200. The Donofrio-Sano combination renders obvious element [8f]. *See* Analysis of Elements [1d], [6f], ¶¶ 157-158, 189, *supra*.

***[8g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer.”***

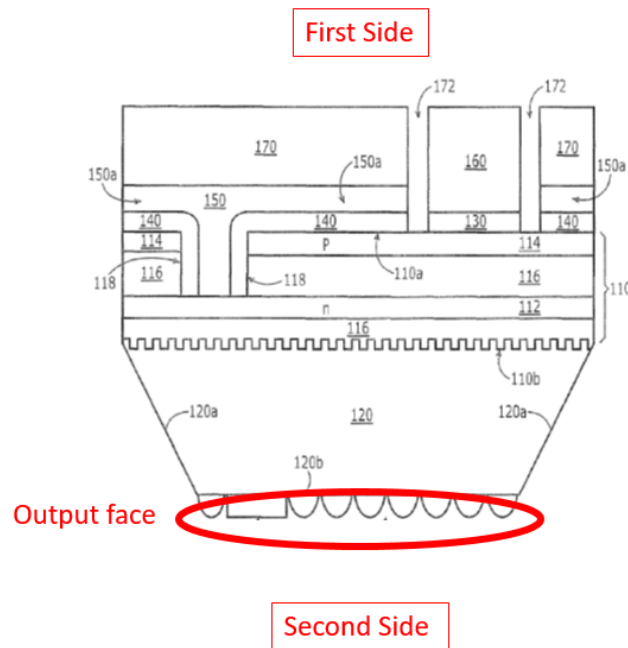
201. The Donofrio-Sano combination renders obvious element [8g]. *See* Analysis of Elements [1e], [6g], ¶¶ 159-170, 190, *supra*.

***[9a]: “The LED module of claim 8, further comprising a wavelength converter over the opposite side of the LED package to the first and second electrode pads,”***

202. The Donofrio-Sano combination includes a wavelength converter over the opposite side of the LED package to the first and second electrode pads.

Specifically, as I discussed above for element [2a], Donofrio discloses a wavelength converter over a second side of the semiconductor stack. *See* Analysis of Element [2a], ¶¶ 172-174, *supra*. Moreover, as illustrated below, Donofrio’s

wavelength converter that is over the second side of the semiconductor stack is positioned at the opposite side of the LED package to the first and second electrode pads 170/160:



LGI1009, FIG. 1 (annotated).

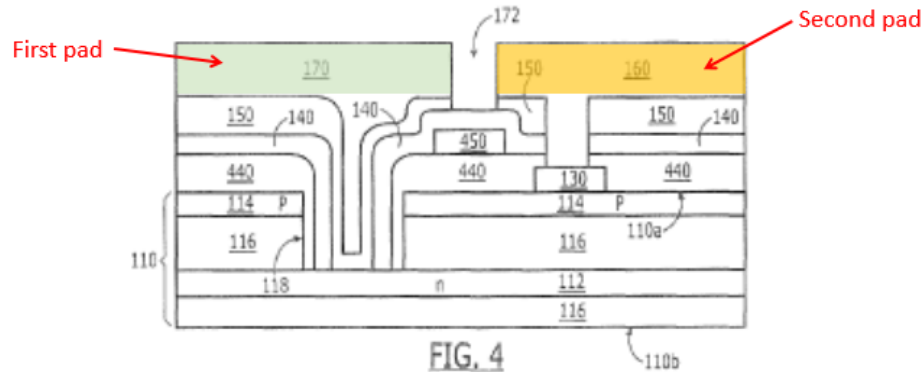
**[9b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”**

203. The Donofrio-Sano combination renders obvious element [9b]. *See* Analysis of Element [2b], ¶¶ 175-176, *supra*.

**[10a]: “The LED module of claim 9, wherein each area of the first and second pads has an area not less than  $\frac{1}{3}$  of the LE package.”**

204. The Donofrio-Sano combination renders obvious element [10a]. In particular, each area of the first and second pads in Donofrio’s LED package has an area not less than  $\frac{1}{3}$  of the LED package. Specifically, looking at the cross-

section of Donofrio's LED package below, Donofrio's first pad (green) and second pad (yellow) can be seen taking up roughly half the area of the LED package:



LGI1009, FIG. 4 (annotated). While Donofrio does not provide precise numerical values for the areas of its electrode pads, nor is the drawing above expected to be drawn perfectly to scale, such electrode pads would have been made as large as possible in order to ensure that the pads are easily aligned during flip-chip mounting and further so that heat generated during the flip-chip bonding process may be more easily dissipated through the large surface area of the pads. *See* LGI1013, 10:47-54.

205. To the extent Donofrio does not explicitly teach the claimed areas of the first and second pads, a POSITA would have found it obvious to configure Donofrio's pads to have an area not less than  $\frac{1}{3}$  of the LED package. This is because it was well-known at the time of the '664 Patent as well as Donofrio to maximize the size of the electrode pads used in flip chips in order to, among other things, facilitate alignment of the pads to the circuit board during mounting and to

better dissipate heat generated during the mounting process. In fact, Donofrio expressly recognizes that “various configurations of anode pads 160 and cathode pads 170” may be used as needed. LGI1009, [0071].

206. A POSITA, them, would have found it to be simple design choice to make the electrode pads as large as possible without them touching each other (*i.e.*, shorting) in order to gain the benefits noted above. And since there are typically two electrode pads, maximizing their size would mean that each takes up greater than  $\frac{1}{3}$  of the total area available on the LED package. In fact, prior art from the relevant time period, for example U.S. 7,554,126 to Higashi (LGI1013), explicitly mentions that each of the electrode pads are “set to a size that covers about half the LED chip.” LGI1013, 10:47-54. Thus, it would have been a simple and routine design choice for a POSITA maximize the areas of the electrode pads so that each one covers approximately half the area of the LED package (*i.e.*, an area not less than  $\frac{1}{3}$  of the LED package).

***[11a]: “The LED module of claim 8, further comprises a lens to adjust an orientation angle of light emitted from the LED package.”***

207. The Donofrio-Sano combination renders obvious element [11a]. See Analysis of Element [6i], ¶¶ 192, *supra*.

***[12a]: “The LED module of claim 8, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”***

*[13a]: “The LED module of claim 12, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer; and”*

**[13b]: “a first part of the protective insulation layer covering the contact layer.”**

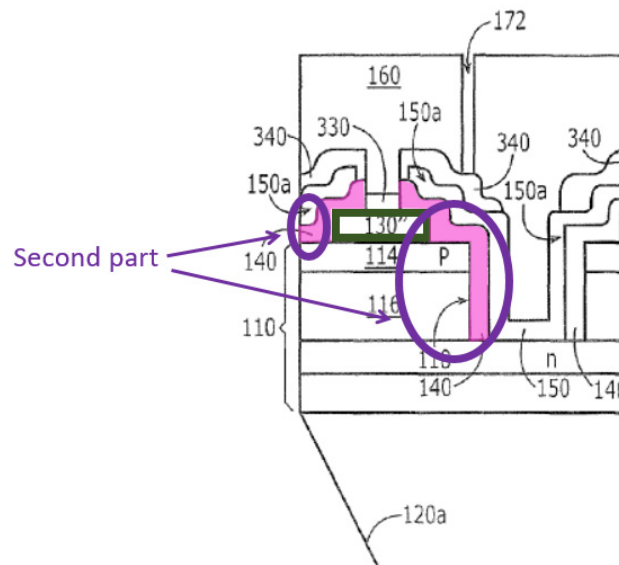
A cross-sectional view of a semiconductor device. The device consists of a substrate 110 with layers 116, 114, and 118. A pink region 140 is formed on the substrate. On top of 140, there are two circular features 150a, each containing a smaller circular feature 130. A green rectangular region 160 is located between the two 150a features. A label "First part" with two arrows points to the circular features 150a. Other labels include 172, 340, and 150.

103

***[14a]: “The LED module of claim 13, wherein a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer,”***

211. The Donofrio-Sano combination renders obvious element [14a].

Specifically, as illustrated below, Donofrio’s protective insulation layer (pink) includes vertical portions, labeled as “second part,” that covers the sidewall of the first conductive type semiconductor layer:



LGI1009, FIG. 3 (cropped, annotated).

***[14b]: “the second part of the protective insulation layer contacts the first part of the protective insulation layer.”***

212. The Donofrio-Sano combination renders obvious element [14b].

Specifically, as illustrated below, Donofrio’s protective insulation layer (pink) includes horizontal portions (labeled “first part”) and vertical portions (labeled “second part”) that contact each other:





***[17a]: “The LED module of claim 16, at least one of the contact holes has a circular shape, and”***

216. The Donofrio-Sano combination renders obvious element [17a]. See Analysis of Element [5a], ¶ 180, *supra*.

***[17b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”***

217. The Donofrio-Sano combination renders obvious element [17b]. See Analysis of Element [5b], ¶¶ 181-182, *supra*.

***[18a]: “The LED module of claim 17, further comprising a lens to adjust an orientation angle of light emitted from the LED package.”***

218. The Donofrio-Sano combination renders obvious element [18a]. See Analysis of Element [6i], ¶ 192, *supra*.

***[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”***

219. The Donofrio-Sano combination renders obvious element [19a]. See Analysis of Element [7a], ¶ 193, *supra*; LGI-1009, [0093].

***[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”***

220. The Donofrio-Sano combination renders obvious element [19b]. Specifically, Donofrio’s LED packages are mounted on LED chips on various types of mounting substrates, including MC-PCB. LGI1009, [0093]. It further would have been obvious, in view of Donofrio’s teachings, for a POSITA to mount

multiple chips on an MC-PCB to, for example, mix different types of LEDs and/or to maximize light output. *See, e.g.*, LGI1008, Abstract, [0012].

## **XI. ANALYSIS OF DONOFRIO, SANO, AND BEGEMANN WITH RESPECT TO CLAIM 19**

221. For the reasons articulated in detail below, and based on my review of the '664 patent as well as the Donofrio, Sano, and Begemann references, I am confident that a POSITA would have readily understood that the predictable combination of Donofrio, Sano, and Begemann provides all elements of claim 19.

222. Descriptions of Donofrio and Sano were provided above in ¶¶ 49-53, 145-149 and are incorporated herein. Begemann, which is entitled “LED Lamp,” is generally directed to an LED lamp and discloses forming an LED array that is made up of a number of LED chips that are provided on a PCB. *See* LGI1008, Abstract, [0012].

***[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”***

223. Donofrio in view of Sano renders obvious element [19a]. *See* Analysis of Element [7a], ¶ 193, *supra*.

***[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”***

224. Donofrio and Sano further in view of Begemann renders obvious element [19b]. Specifically, Donofrio teaches mounting LED chips on various

types of mounting substrates, including MC-PCB. LGI1009, [0093]. To the extent Donofrio doesn't expressly disclose arranging a *plurality of LED packages* on the MC-PCB, Begemann provides this feature.

225. For example, as shown below, Begemann explicitly teaches mounting multiple LED chips onto an MC-PCB:

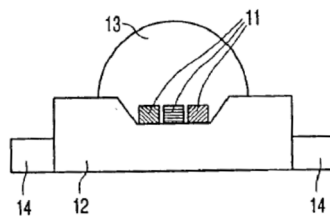


FIG. 3B


LGI1008, FIG. 3B; [0029]. A POSITA would have considered the mounting of multiple LED packages on an MC-PCB to be obvious and a routine and conventional design choice. Indeed, the arrangement of a plurality of LED packages on an MC-PCB, as evidenced by Begemann, was common practice in the field of LED design and manufacturing, and there was nothing new or inventive about changing the number of LED packages being mounted or even the type of circuit board being utilized at the time of the '664 Patent. Thus, incorporating the multiple-chip configuration of Begemann into the LED device of Donofrio in view of Sano amounts to merely combining prior art elements from the same field, according to known methods to yield predictable results.

## **XII. ADDITIONAL REMARKS**

226. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

227. I hereby declare that all statements made are of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: June 10, 2019

By:   
Eric Bretschneider, Ph.D.  
Grapevine, TX

# **APPENDIX A**

**Skills Summary**

- Successful Management and Team building with personnel at levels ranging from Sr. Scientists and Engineers to Technicians/Operators. Maximum Department size >100; Budget >\$25 million/yr.
- Strong New Product Development background; over 100 new SSL products taken from concept to manufacturing, including regulatory, Energy Star certification and DLC certification.
- Excellent communication skills sales and sale support experience as evidenced by development of new 8+ figure accounts for LED die, packages and applications. Proven ability to match customer demands/needs/desires with existing products.
- Comprehensive technical background in the full range of LED production technologies including MOCVD hardware/process, fabrication, LED chip/package test/reliability, optical design, thermal management, color conversion, SSL fixture/lamp design/integration and reliability.
- Direct Design and Development experience of LEDs (structures, die, packages) and SSL fixtures/components using TracePro and SolidWorks.

**Employment****CTO; EB Designs & Technology Grapevine, TX****2014 –**

- Design and development of innovative solid-state lighting technology and designs, with a primary focus on optical design, thermal design and production/assembly technologies.
- Manage technology roadmap and draft IP disclosures/patent filings.
- Provide technical support and conduct research/technology development for clients in the field of solid-state lighting. This work additionally includes serving as an expert witness.
- Developed the first method able to predict chromaticity shift of LED products over time. Method is being used as the basis for a new industry standard: IES TM-35-19 "Projecting Long-Term Chromaticity Coordinate Shift of LED Packages, Arrays and Modules."
- Developed the method for interpolating between drive currents for flux maintenance lifetime for LED based products that is being implemented in IES TM-21-19 "Projecting Long Term Lumen, Photon and Radiant Flux Maintenance of LED Light Sources."

**Director of Engineering; HeathCo, LLC Bowling Green, KY****2013 – 2014**

- Managed Engineering Department Staff (11 domestic, 14 international); Responsibilities included preparation and administration of the department budget (\$3.5 million annual). The department was charged with developed advanced technology/products related to: Solid State Lighting, Sensors, Notifications and Control Products and included regulatory/certifications for UL, FCC, Energy Star and DLC.
- Developed technology, IP and product roadmaps for all three business units (Lighting, Sensors, Notifications). Provided solid state lighting technology support for The Chamberlain Group.
- Additional responsibilities included establishing career development paths and training goals for all members of the department.
- Key accomplishments:
  - Led team for product recall issue dating back to 2006. Reduced recall scope (# units) by >80% and financial exposure by >85% through detailed investigation and analysis of production records and analysis of excess and obsolete inventory.
  - Completed review for entire product portfolio to comply with new cUL bi-lingual language requirements. Project required warning requirement changes to physical components (tooling), warning labels, documents and packaging on >400 products.

**Elec Tech International Zhuhai, Guangdong Province, P.R. China****Chief Engineer ETi Lighting Research Institute****VP Research & Development ETi Solid State Lighting****2011 – 2013**

- Managed Engineering and R&D staff for newly formed vertically integrated LED company (107 Engineering, Scientists, Designers); responsibilities included preparation and administration of the department budget (>\$25 million annual)
- Worked directly with President and CEO of the company to develop IP and product roadmaps for all LED based lighting products/projects for markets in the US, Europe, Japan and China.
- Key accomplishments:
  - Developed capability for fast turn functional prototypes (<2 weeks from concept to operating units). This was an improvement over the prior process that required 6+ weeks for a working prototype. Prior to this the company lost ~50% of all opportunities that required functional prototypes.
  - Supported product development and production ramps that enabled the company to increase sales from ~\$10 million to >\$40 million in one year.
  - Developed proprietary linear lamp technology capable of >1000 lumens/ft with a wall plug efficacy >100 lm/W, CRI>80 and L70>50,000 hrs (Ta = 25°C). Technology allows the same base units to be installed in fixtures as a replacement tube or used as individual luminaires with transverse spacing criteria ranging from 1.6 – 2.9.

#### **Lighting Science Group Corporation Satellite Beach, FL**

##### **2010 - 2011 VP of Research**

- Assembled and managed research and development teams for projects related to solid state lighting.
- Direct responsibility for design/development of customized photometric and radiometric characterization equipment.
- Direct responsibility for modeling and determining product and component lifetimes based on optical, thermal, mechanical and electrical analysis with respect to intended operating environments.
- Served as company representative on industry standards committees related to SSL technology (LM79, LM80, TM21, etc.)
- Key accomplishments:
  - Developed advanced LED models for product development and production control; including advanced color control schemes for multi-color applications. Methods capable of predicting average chromaticity to within a combined  $\Delta xy \leq 0.02$ ; production variation < 2 step MacAdam ellipse.
  - Developed and characterized wavelength conversion materials, methods and technology. Work included development of optics and materials for L-Prize entry.

##### **2008 – 2010 Product Development Manager**

- Tasked with developing Solid State Lighting products including: optical, mechanical and thermal design, design and process FMEA, oversight of initial production, development of quality system documents and requirements for internal production and out-sourced components. Projects ranged from individual efforts to team of 10+ employees
- Served as the primary technical resource for all OEM customers.
- Managed group responsible for all product certifications and standards requirements including UL, FCC, CE, Energy Star and DLC as well as IES lighting requirements for outdoor products.
- Responsible for development, calibration and maintenance of photometric equipment in development and production areas.
- Key accomplishments:
  - Completed fast track development and launch of OEM SSL acorn retrofit product (<5 months). Product exceeded all customer requirements including: lumen output, efficacy, thermal resistance and size. Developed second generation product with >100% increase in light output with now cost increase.
  - Completed design of Streetlight family (4 products) in 4 month time span. Products achieved >90 lumens/Watt efficacy at thermal stability with projected L70 lifetimes >80,000 hours at Ta=40°C (continuous).
  - Development replacement lamp family line (6 primary lamp types, 100+ variations). Product family included the first replacement LED lamps to achieve Energy Star certification. Product variations developed for LSG brand name and 3 OEM customers. Altogether the family accounted for >50% of the Energy Star certified LED lamps as of December 2011.

#### **2004 - 2008 Toyota Gosei North America Troy, MI Sales Manager**



- Primary responsibility for developing new and managing existing LED die and package customers for the Eastern region of North America. This required extensive communications with existing and potential customers to determine best fit products for their applications/requirements.
- Additional responsibility for search for and identifying new market opportunities for existing or newly developed products.
- Served as the primary technical resource for all customers in North/South America and Europe; provide engineering support for customers developing LED packages and LED lighting products.
- Key accomplishments:
  - Secured two new 8 figure accounts in a new market niche. These customers designated as the only two priority customers for Toyoda Gosei world-wide. Sales ramped from \$0 to >\$100 million/yr in less than 18 months.
  - Secured sole supplier status for LED backlights in Apple - 9.9" (iPad), 15.4", 17" and 22" displays. This was the culmination of an 18 month campaign with the Apple Display group to find the best fit product for their requirement and to train Apple personnel on potential technical barriers/issues with their application.
  - Addressed Microsoft concerns about blue light hazards related to development of a next generation optical mouse. After three months, I was able to conclusively show to Microsoft that it would be impossible for 14mil die products to present a photo-biological hazard under both IEC 62471 and IEC 60825.
  - Awarded business for all passenger lighting on the B787 Dreamliner. This award was made by Diehl which controls all lighting for Boeing, Airbus and Embraer and was achieved within 4 months of first contact with Diehl. At the time of first contact Diehl had no knowledge of Toyoda Gosei and had been working with 4 LED companies for over 12 months on the project.

### **2003 – 2004 Beeman Lighting Sarasota, FL**

#### **Director of Solid-State Lighting Engineering**

- Tasked with leading development of solid-state lighting systems and materials with primary focus on chip on board applications and devices. Product lines included RGB landscape lighting and minimal environmental impact fixtures and novel display/artwork fixtures.
- Managed all IP issues (competitor analysis, IP roadmap, patentability analysis).
- Worked with existing and potential customers to ensure new products meet or exceed requirements and expectations.
- Key accomplishment
  - Developed RGB LED based landscape light with minimal environmental impact. This was accomplished by establishing a research project with FAU and included studies that conclusively showed the products had no impact on the behavior of sea turtle hatchlings.

### **2003 University of South Florida Tampa, FL**

#### **Intellectual Property Manager**

- Managed IP portfolio of over 100 active patents and applications for University faculty/staff. Key portfolio items included: anti-cancer bioactive compounds, dendrimer synthesis and application technology, and spectral analysis of biological materials (blood analysis, surface and soluble protein analysis).
- Tasked with enhancing University reputation and revenue through negotiation of licensing agreements for IP
- Key accomplishments:
  - Negotiated license agreement for evaluation of new anti-cancer compounds derived from cold water tunicates.
  - Assembled team that included 3 corporate and 2 academic partners for the DARPA SUVOS program. This task was completed in one month and the resulting proposal was ranked 2<sup>nd</sup> overall out of a field of 34 entries and was noted by the reviewers as the only proposal to address each and every portion of the RFP.

### **1998 – 2003 Uniroyal Optoelectronics Tampa, FL**

#### **Director of Intellectual Property, University Relations & Government Contracts (2001 – 2003)**

- Concurrent assignment as Sr. Epi Scientist.
- Tasked with establishing IP roadmap and track patent landscape related to MOCVD growth, chip/package design and applications for LED technology.

- Reviewed all production and R&D activities to identify potential IP. This included drafting initial disclosures and working with external counsel for patent filings and responses to office actions. Activities with external counsel further included development of opinions of non-infringement.
- Oversight and management of a \$3.4 million multi-campus research program.
- Monitor and track RFP notices for externally funded research related to the company's core technology development roadmap.
- Key accomplishments:
  - Developed opinions of non-infringement with external counsel for 10 LED patents that had been the subject of numerous infringement suits against Tier 1 LED companies.
  - Assembled team that included 3 corporate and 2 academic partners for the DARPA SUVOS program. This task was completed in one month and the resulting proposal was ranked 2<sup>nd</sup> overall out of a field of 34 entries and was noted by the reviewers as the only proposal to address each and every portion of the RFP.

#### **Team Leader, Epitaxial Materials & Characterization (1999 – 2001)**

- Concurrent assignment as Sr. Epi Scientist.
- Oversaw start up and qualification of Epitaxial Growth & Characterization areas; role included training of Sr. Scientists, Engineers and Technicians for both areas in theory, application, process and maintenance procedures.
- Managed Epitaxial Growth & Characterization areas for production of InGaN and AlInGaP LED wafers. This included preparation and administration of the department budget (~\$25 million annual) as well as setting department performance goals (total good wafers, wafer yield, performance improvements and unit production costs).
- Coordinate inventory levels with purchasing department to minimize value of inventory necessary to support production plan. Additionally, negotiated key raw material specifications and prices.
- Served as Sr. member of Quality Team responsible for ISO9001 certification. Certification was achieved within a 12 month time span.
- Key accomplishments:
  - Completed process qualifications for all MOCVD systems within 3 months of CapEx delivery and established initial production yields 15% higher than the benchmark process transferred to UOE.
  - Managed departmental expansion and quality system efforts that allowed >250% increase in production capacity.
- Managed start up and qualification of Epitaxial Growth & Characterization areas; role included training of Engineers and technicians for both areas in theory, application, process and maintenance procedures.

#### **Sr. Epi Scientist (1999 – 2003)**

- Primary responsibility for MOCVD hardware and process modifications necessary to support performance improvements, yield enhancements and cost reductions.
- Served as primary technology liaison with customers and investors.
- Tasked with technical oversight of all photometric/radiometric characterization.
- Responsible for LED chip and package optical/thermal design including wavelength conversion materials.
- Key accomplishments:
  - Resolved gold corrosion issue in Fab area. Also eliminated transparent contact failure mechanism. Combined efforts increased fabrication yield by >30%.
  - Modified hardware and epitaxial growth process to increase throughput of Epitaxial Growth & Characterization areas by 80% (9 hour to 5 hour cycle time), while cutting unit cost by >30%. Also reduced surface and interfacial roughness by a factor of >3x while improving thickness uniformity from 4% to <2%, using DOE methods. Additional hardware modification increased throughput by another 20%.
  - Developed new test methods to verify performance of LED structures prior to Fabrication. Methods allowed verification of optical power to within 15% and wavelength within 2 nm prior to beginning of fabrication.

#### **Staff Engineer (1998 – 1999)**

- Designed/specified Epitaxial Growth & Characterization areas. This responsibility included specification and selection of all CapEx equipment for the Epitaxial Growth and Characterization areas and managing the construction, CapEx equipment installation and start up.
- Additional responsibilities included determining initial product cost and throughput based on installed CapEx tool base.

- Key accomplishments:
  - Implemented and validated new ammonia delivery system that allowed multiple MOCVD systems to draw from the same cylinder and eliminated downtime for cylinder changes. Implemented new exhaust management process for arsine/phosphine waste stream, extending maintenance interval by >300%.
  - Developed zero assumption cost and throughput models for LED facility. Cost estimate for 18 months post-start up proved accurate to within 10% of actual costs.

**1996 – 1998 Emcore Corporation Somerset, NJ**

**Process Engineer**

- Responsible for installation, materials demonstration and production process qualification and transition into manufacturing of MOCVD systems in an ISO9000 manufacturing environment (6 systems in 18 months).
- Tasked with identifying cost reduction and throughput/yield enhancements for epitaxial growth processes.
- Member of internal Quality System audit team.
- Key accomplishments:
  - Developed MOCVD Tool Qualification Procedure for benchmarking and qualifying all MOCVD systems installed for internal corporate use as well as at customer locations world-wide.
  - Completed Manufacturing Readiness Review for AlGaAs/Ge solar cell process in ~25% of standard time. Resulted in 3 year, \$15 million supply contract for company.
  - Scaled up and transferred of InSb magneto resistor process to a higher throughput system (single wafer D-180 to five wafer E-300). Increased wafer yield by from 65% to >95%.
  - Developed industry's first comprehensive cost and throughput model for epitaxial growth processes. The model typically allowed cost reductions of 10-20% and throughput increases of >10%.

**1990 AT&T Bell Labs**

**Holmdel, NJ**

**Visiting Researcher**

- Designed and built custom MOCVD/Mass spec system. System allowed tracking of precursor molecules, reaction intermediates and products over 12+ orders of magnitude of concentration.
- Implemented program to evaluate novel precursors for use in growth and doping of III-V and II-VI compound semiconductors. Data used to determine reaction and decomposition mechanisms for metal-organic sources. Successfully identified grow conditions for novel carbon doping source (norbornadiene) for III-V materials.

**1989 Shell Oil Norco, LA**

**Process Engineer**

- Developed and implemented new system for determining optimal time to clean heat exchangers on crude oil distillation column based on global economic metrics of unit and detailed process simulations.
- System exceeded system cost savings target of \$50,000/year by ~3 orders of magnitude. Project resulted in corporate-wide savings of >\$50 million/year. Cumulative corporate savings exceed \$1 billion.

**Education**

**Ph.D. in Chemical Engineering**

**University of Florida 1997**

**BSE in Chemical Engineering**

**Tulane University 1989**

- Graduate work focused on development of optoelectronic devices, including novel silicon based visible LEDs and sulfide based TFELD structures.
- Developed the world's first crystalline silicon based visible light LED. Utilized DOE methods to identify process conditions to allow first growth of epitaxial silicon on ZnS epi layers.
- Tested and verified efficacy of novel precursors for p-type doping of ZnSe materials in LED structures.
- Responsible for modification, operation and maintenance of MOCVD system for growth of wide bandgap compound semiconductor materials.
- Trained incoming post docs and graduate students in theory, operation and maintenance of MOCVD systems. Group comprised ~20 students and 6 post docs.

**References Available on request**

**Curricula Vitae**

**University of Florida, Department of Chemical Engineering Advisory Board**

Member 1998 –

Chair 2007 – 2009, 2017 -

**Professional Societies:**

- SPIE
- OSA
- Materials Research Society
- Illuminating Engineering Society (Science Advisory Panel, Test Procedures Committee, Chair of Solid-State Lighting Sub-Committee, Light Sources Committee, Color Committee)
- American Society of Horticultural Science (ASHS)
- American Society of Agricultural and Biological Engineers (ASABE)

**Conference Chair**

LED Measurement and Standards, San Diego, CA October 2-3 (2008).

**Patents (Granted)**

1 US Patent 7,093,956 "Method of Lighting for Protecting Sea Turtles." D. Miller, E. Bretschneider, issued August 22, 2006.

2 US Patent D650,519 "Pole for a Street Light Luminaire." F. Maxik, D. Henderson, E. Bretschneider, A. Widjaja, K. Bowen, J. Sundin, E. Peiniger, issued December 13, 2011.

3 US Patent 8,157,413 "Light Fixture and Associated LED Board and Monolithic Optic." F. Maxik, Z. Gibler, E. Bretschneider, D. Henderson, A. Widjaja, issued April 17, 2012.

4 US Patent D673,323 "Light Fixture." F. Maxik, D. Henderson, E. Bretschneider, A. Widjaja, K. Bowen, J. Sundin, E. Peiniger, issued December 25, 2012.

5 US Patent 8,360,607 "Lighting Unit with Heat Dissipating Chimney." E. Bretschneider, Z. Berkowitz, R. Sosnick, L. Pattison, P. Pattison, issued January 29, 2013.

6 US Patent 8,408,725 "Remote Wavelength Conversion Device and Associated Methods." F. Maxik, E. Bretschneider, R. Soler, D. Bartine, issued April 2, 2013.

7 US Patent D681,874 "Light Fixture." F. Maxik, D. Henderson, E. Bretschneider, A. Widjaja, K. Bowen, J. Sundin, E. Peiniger, issued May 7, 2013.

8 US Patent 8,439,515 "Remote Lighting Device and Associated Methods." F. Maxik, R. Soler, D. Bartine, E. Bretschneider, issued May 14, 2013.

9 US Patent 8,465,167 "Color Conversion Occlusion and Associated Methods." F. Maxik, E. Bretschneider, R. Soler, D. Bartine, issued June 18, 2013.

10 US Patent 8,491,165 "Lighting Unit Having Lighting Strips with Light Emitting Elements and a Remote Luminescent Material." E. Bretschneider, Z. Berkowitz, R. Sosnick, L. Pattison, P. Pattison, issued July 23, 2013.

11 US Patent 8,492,995 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued July 23, 2013.

12 US Patent 8,506,118 "Light Fixture and Associated LED Board and Monolithic Optic." F. Maxik, Z. Gibler, E. Bretschneider, D. Henderson, A. Widjaja, issued August 13, 2013.

13 US Patent 8,515,289 "Wavelength Sensing Lighting System and Associated Methods for National Security Application." F. Maxik, D. Bartine, P. Medelius, E. Bretschneider, issued August 20, 2013.

- 14 US Patent 8,547,391 "High Efficacy Lighting Signal Converter and Associated Methods." F. Maxik, R. Soler, D. Bartine, R. Zhou, V. Bastien, M. Regan, E. Grove, E. Bretschneider, issued October 1, 2013.
- 15 US Patent 8,616,715 "Remote Light Wavelength Conversion Device and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued December 31, 2013.
- 16 US Patent 8,680,457 "Motion Detection System and Associated Methods Having at Least One LED of a Second Set of LEDs to Vary Its Voltage." F. Maxik, issued March 25, 2014.
- 17 US Patent 8,686,641 "Tunable LED Lamp for Producing Biologically Adjusted Light." F. Maxik, D. Bartine, R. Soler, E. Grove, E. Bretschneider, issued April 1, 2014.
- 18 US Patent 8,684,566 "Light Emitting Unit With Indirect Light Source." E. Bretschneider, Z. Berkowitz, R. Sosnick, L. Pattison, M. Pattison, issued April 1, 2014.
- 19 US Patent 8,702,259 "Color Conversion Occlusion and Associated Methods." F. Maxik, E. Bretschneider, R. Soler, D. Bartine, issued April 22, 2014.
- 20 US Patent 8,818,202 "Wavelength Sensing Lighting System and Associated Methods for National Security Applications." F. Maxik, D. Bartine, P. Medelius, E. Bretschneider, issued August 26, 2014.
- 21 US D715467 "LED Linear Replacement Lamp Design." E. Bretschneider, Z. Berkowitz, R. Sosnick, issued October 14, 2014.
- 22 US 8,866,839 "High Efficacy Lighting Signal Converter and Associated Methods." F. Maxik, R. Soler, D. Bartine, M. Regan, E. Grove, E. Bretschneider, issued October 21, 2014.
- 23 US 8,941,329 "Tunable LED Lamp for Producing Biologically-Adjusted Light." F. Maxik, D. Bartine, R. Soler, E. Grove, E. Bretschneider, issued January 27, 2015.
- 24 US 9,024,536 "Tunable LED Lamp for Producing Biologically-Adjusted Light and Associated Methods." F. Maxik, D. Bartine, R. Soler, E. Grove, E. Bretschneider, issued May 5, 2015.
- 25 US 9,125,275 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued September 1, 2015.
- 26 US 9,172,199 "Electrical Fixture Connection." T. Birdwell, E. Bretschneider, J. Fitzgibbon, B. Moore, S. Tylicki, issued October 27, 2015.
- 27 US 9,289,574 "Three-channel Tuned LED Lamp for Producing Biologically-Adjusted Light." F. Maxik, D. Bartine, R. Soler, E. Grove, E. Bretschneider, issued March 22, 2016.
- 28 US 9,307,608 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued April 5, 2016.
- 29 US 9,578,710 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued February 21, 2017.
- 30 US 9,693,414 "LED Lamp for Producing Biologically-Adjusted Light." F. Maxik, D. Bartine, E. Bretschneider, issued June 27, 2017.
- 31 US 9,839,092 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued December 5, 2017.

32 US 9,913,341 "LED Lamp for Producing Biologically-Adjusted Light Including a Cyan LED." F. Maxik, D. Bartine, E. Bretschneider, issued March 6, 2018.

33 US 10,054,290 "Movable Barrier Operator Light Distribution." T. Birdwell, E. Bretschneider, J. Fitzgibbon, issued January 8, 2019.

34 US 10,177,287 "Gamut Broadened Displays with Narrow Band Green Phosphors." J. Melman, R. Nordsell, K. Baroudi, Y. Bok Go, E. Bretschneider, A. Thomas, E. Thomas, issued January 8, 2019.

35 US 10,177,287 "Wavelength Sensing Lighting System and Associated Methods." F. Maxik, E. Bretschneider, P. Medelius, D. Bartine, R. Soler, G. Flickinger, issued February 19, 2019.

## **Patents (Pending)**

>30 US and International Patents pending

## **Publications**

1. "Evaluation of  $\text{Zn}\{\text{N}[\text{Si}(\text{CH}_3)_3]_2\}_2$  as a p-Type Dopant in OMVPE Growth of ZnSe" W. S. Rees, D. M. Green, T. J. Anderson, E. Bretschneider, B. Pathangey, C. Park and J. Kim, J. Elec. Mat., vol. 21, pp. 361-366 (1992).
2. "OMVPE Growth of ZnSe Utilizing Zinc Amides as Source Compounds: Relevance to the Production of p-type Material" W. S. Rees, D. M. Green, T. J. Anderson and E. Bretschneider, Wide Bandgap Semiconductors, eds. T. D. Moustakas, J. I. Pankove and Y. Hamakawa, MRS Pub., vol. 242 (1992).
3. "Characterization of ZnS Layers Grown by MOCVD for Thin Film Electroluminescence (TFEL) Devices" J. E. Yu, K. S. Jones, B. Pathangey, E. Bretschneider, T. J. Anderson, J. Fang, P. H. Holloway, Wide Bandgap Semiconductors, eds. T. D. Moustakas, J. I. Pankove and Y. Hamakawa, MRS Pub., vol. 243 (1992).
4. "A Study of Nucleation of ZnS Thin Layers Grown by Low-Pressure MOCVD for Thin Film Electroluminescence (TFEL) Devices" J. E. Yu, E. Bretschneider, B. Pathangey, T. J. Anderson, J. Fang, P. H. Holloway and K. S. Jones, Mechanisms of Heteroepitaxial Growth, eds. M. F. Chisholm, B. J. Garrison, R. Hull and L. J. Schowalter, MRS Pub., vol. 263 (1992).
5. "MOCVD Growth of Non-Epitaxial and Epitaxial ZnS Thin Films" J. Fang, P. H. Holloway, J. E. Yu, K. S. Jones, B. Pathangey, E. Bretschneider and T. J. Anderson, Appl. Surf. Sci., vols. 70-71, pp. 701-706 (1993).
6. "Temperature and Flow Modulation Doping of Manganese in ZnS Electroluminescent Films by Low Pressure Metalorganic Chemical Vapor Deposition" J. E. Yu, K. S. Jones, P. H. Holloway, B. Pathangey, E. Bretschneider and T. J. Anderson, J. Elec. Mat., vol. 23, pp. 299-305 (1994).
7. "Evidence for Quantum Confinement Effects in MOCVD-Grown Si/ZnS Nanostructures," E. Bretschneider, A. Davydov, J. E. Yu, B. Pathangey, K. S. Jones and T. J. Anderson, submitted to Applied Physics Letter (1994).
8. "Carrier Confinement Effects in Epitaxial Silicon Quantum Wells Prepared by MOCVD," H. P. Maruska, R. Sudharsanan, E. Bretschneider, A. Davydov, J. E. Yu, Z. Huang, B. Pathangey, K. S. Jones and T. J. Anderson, Microcrystalline and Nanocrystalline Semiconductors, eds. R. W. Collins, C. C. Tsai, M. Hirose, F. Koch and L. Brus, MRS Pub., vol. 358 (1994).

9. "Cost of Ownership Issues in Hydrogen Gas Purification," E. Bretschneider, Semiconductor Fabtech, 16<sup>th</sup> ed., pp. 127-30 (2002).
10. "Bi-Chromatic to Polychromatic Photo- Conversion LEDs." W. Kennedy, E. Bretschneider, Proceedings of the SPIE, the International Society for Optical Engineering, vol. 5941, SPIE, Bellingham, WA (2005).
11. "Solid-State Lighting: Where Are We Going, What Are We Doing?" B. Kennedy, E. Bretschneider, Photonics Spectra, vol. 40, pp58-66. (2006).
12. "Efficacy Limits for Solid-State White Light Sources." E. Bretschneider, Photonics Spectra, vol. 47 (2007).
13. "Chasing Rainbows – Does SPD hold the key to future LED Performance?" E. Bretschneider, LEDs Magazine. (2018).

### **Presentations and Seminars**

1. "Alternative Group V Precursors for CVD Applications," R. M. Lum\*, J. K. Klingert, D. W. Kisker and E. Bretschneider. Presented at the Fifth International Conference on Metalorganic Vapor Phase Epitaxy and Workshop on MOMBE, CBE, GSMBE and Related Techniques, Aachen, Germany (1990).
2. "Synthesis and Characterization of New Compounds Useful in MOVPE of II-VI Compound Semiconductors," W. S. Rees\*, Jr., D. Green, T. J. Anderson, E. Bretschneider and J. Kim. Presented at the Fifth Biennial Workshop on Organometallic Vapor Phase Epitaxy, Panama City, FL (1991).
3. "Initial Stages Deposition of OMCVD ZnS on BaTa<sub>2</sub>O<sub>5</sub> and Si," E. Bretschneider\*, J. E. Yu, B. Pathangey, T. J. Anderson and K. Jones. Presented at Annual AIChE Meeting, Los Angeles, CA (1991).
4. "Growth and Properties of ZnS Layers for Thin Film Electroluminescence (TFEL) Devices," E. Bretschneider\*, J. E. Yu, J. Fang, B. Pathangey, K. S. Jones, P. H. Holloway and T. J. Anderson. Presented at 21st Ann. Symp. Appl. Vac. Sci. Technol., Clearwater, FL (1992).
5. "MOCVD Growth of Non Epitaxial and Epitaxial ZnS Thin Films," J. Fang, P. H. Holloway\*, J. E. Yu, K. S. Jones, B. Pathangey, E. Bretschneider and T. J. Anderson. Presented at 12<sup>th</sup> Internatl. Vac. Congress, Netherlands (1992).
6. "Microstructure of ZnS Layers Grown by MOCVD for Thin Film Electroluminescent Displays," J. E. Yu, K. S. Jones\*, E. Bretschneider, T. J. Anderson and P. H. Holloway. Presented at the 10th Annual Meeting of the Florida Chapter of Scanning Electron Microscopy Society, Crystal River, FL (1992).
7. "Research in Electroluminescent Thin Film Materials at the University of Florida," J. E. Yu, K. S. Jones, B. Pathangey, T. J. Anderson, E. Bretschneider and P. H. Holloway\*. Presented at Planar Systems Inc, Beaverton, OR (1992).
8. "Microstructure and Properties of MOCVD Grown ZnS Undoped and Doped with Terbium or Manganese," P. H. Holloway\*, J. Fang, J. E. Yu, K. S. Jones, E. Bretschneider, B. Pathangey and T. J. Anderson. Presented at Spring MRS Meeting, San Francisco, CA (1993).
9. "Effects of Substrate Preparation on the Interfacial Abruptness and Composition of ZnS/Si Heterostructures," J. E. Yu, E. Bretschneider, T. J. Anderson\* and K. S. Jones. Presented at Spring MRS Meeting, San Francisco, CA (1993).

10. "Microstructure, Modulation Doping, and Epitaxial Growth of Electroluminescent Films of ZnS," J. E. Yu, J. Fang, K. S. Jones, P. H. Holloway\*, E. Bretschneider, B. Pathangey and T. J. Anderson. Presented at the 40th Nat. Symp. and Topical Conf. of the Amer. Vac. Soc., Orlando, FL (1993).
11. "Blue and Green Light Emitting Phosphors for Thin Film Electroluminescent Displays," J. E. Yu, E. Bretschneider, B. Pathangey, S. Jones, T. Trottier, P. Rack, J. Sebastian, K. S. Jones, T. J. Anderson and P. H. Holloway\*. Presented at Spring MRS Meeting, San Francisco, CA (1994).
12. "Quantum Confinement Effects in Heteroepitaxial Si/ZnS Nanostructures Produced by MOCVD." E. Bretschneider\*, J. E. Yu, Z. Huang, B. Pathangey, K. S. Jones, T. J. Anderson, H. P. Maruska and R. Sudharsanan. Presented at the 41st National Symposium of the American Vacuum Society and 3rd International Conference on Nanometer-scale Science and Technology, Denver, CO (1994).
13. "MOCVD Growth of ZnS/Si Quantum Well Structures" E. Bretschneider\*, A. Davydov, C. McCreary, J. E. Yu, L. Wang, K. S. Jones, T. J. Anderson and P. Maruska. Presented at the TMS 7th Biennial Workshop on Organometallic Vapor Phase Epitaxy, Fort Myers, FL (1995).
14. "MOCVD Growth of ZnS Using Methyl Mercaptan as an Alternate Sulfur Source." C. McCreary\*, A. Davydov, E. Bretschneider and T. J. Anderson. Presented at the AIChE Conference on Electronic and Photonic Materials. Miami, FL (1995).
15. "ZnS/Si/ZnS Quantum Well Structures for Visible Light Emission." E. Bretschneider\*, C. McCreary, A. Davydov, T. J. Anderson, H. P. Maruska and P. Norris. Presented at the Fall MRS Meeting, Boston, MA (1995).
16. "MOCVD Growth of Si/ZnS Quantum Well Structures." E. Bretschneider\*, A. Davydov, C. McCreary, T. J. Anderson and H. P. Maruska. Presented at the TMS 8th Biennial Workshop on Organometallic Vapor Phase Epitaxy, Dana Point, CA (1997).
17. "Cost of Ownership Issues in Hydrogen Purification." E. Bretschneider\*, Presented at CS-MAX 2001, Boston, MA (2001).
18. "MOCVD Growth of High Brightness Light Emitting Diodes." E. Bretschneider\*, Invited Seminar, Department of Chemical Engineering, Tulane University, March 2002.
19. "Comparison of CDD and Photodiode Arrays for Measurement of High Brightness Light Emitting Diodes." E. Bretschneider\*, C. Dodds, Presented at CS-MAX 2002, San Jose, CA (2002).
20. "Angular Variations in Spectroradiometric Characterization of High Brightness Light Emitting Diodes." E. Bretschneider\*, C. Dodds, C. Narfgren, J. Ngafoe, Presented at CS-MAX 2002, San Jose, CA (2002).
21. "Solid-State Lighting for the 21<sup>st</sup> Century." E. Bretschneider\*, Invited Seminar, Department of Chemical Engineering, University of South Florida, September 2003.
22. "Bi-Chromatic to Polychromatic Photo-Conversion LEDs." W. Kennedy, E. Bretschneider\*, Presented at Fifth International Conference on Solid-State Lighting, Sand Diego, CA, August 1-4 (2005).
23. "Introduction to High Brightness LEDs." E. Bretschneider\*, Presented at SID-LEDs in Displays, Costa Mesa, CA (2006).
24. "High Brightness Side-View LEDs Review." E. Bretschneider\*, Presented at SID-LEDs in Displays, Costa Mesa, CA (2007).



25. "High Brightness Side-View LEDs: What It Takes to Deliver LEDs Suitable for Mid-Size LCD BLUs in Mass Production." E. Bretschneider\*, Presented at SID-LEDs in Displays, Costa Mesa, CA (2008).
26. "Color Rendering and Efficacy Limits for Solid State Lighting Technology." E. Bretschneider\*. Presented at SPIE 8<sup>th</sup> International Conference on Solid State Lighting, Los Angeles, CA (2008).
27. Conference Chair: "LED Measurement and Standards", San Diego, CA October 2-3 (2008).
28. "Public Lighting Case: New York City", E. Bretschneider\*, E. Peiniger, J. Sundin, Green Lighting 2009, Frankfurt, Germany, March 24-26 (2009).
29. "Honest Metrics for Energy Efficient Lighting", E. Bretschneider, Design Lights Consortium Stakeholders Meeting, Denver, CO August 2-3 (2016).
30. "Models for Predicting Color Point Stability", E. Bretschneider, Strategies in Light, Anaheim, CA February 28 - March 2 (2017).
31. "Models for Predicting LED Color Point Stability" - Invited paper, E. Bretschneider, CORM 2017, Troy, NY, July 31 - August 2 (2017).
32. "Chasing the Rainbow" Strategies in Light, Las Vegas, NV, February 27 – March 1 (2019).
33. "From Back Death to White Light: the LED Revolution that almost didn't happen." (Keynote speaker), Strategies in Light, Las Vegas, NV, February 27 – March 1 (2019).