



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/815,433	03/22/2016	9293664	114898-8005.US02	1096

97075 7590 03/02/2016
Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Won Cheol Seo, Ansan-si, KOREA, REPUBLIC OF;
Seoul Semiconductor Co., Ltd., Seoul, KOREA, REPUBLIC OF;
Dae Sung Cho, Ansan-si, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Won Cheol Seo et al.

Application No.: 14/815,433

Confirmation No.: 1096

Filed: July 31, 2015

Examiner: Cuong Quang Nguyen

For: WAFER-LEVEL LIGHT EMITTING DIODE
PACKAGE AND METHOD OF
FABRICATING THE SAME

Art Unit: 2811

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed November 12, 2015, enclosed is a completed Issue Fee Transmittal Form PTOL-85b.

COMMENTS ON EXAMINER'S REASONS FOR ALLOWANCE

It is recognized that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all of the details as to why the claims are allowed. In the above-referenced application, it is not conceded that the Examiner's stated reasons for allowance are the only reasons for which the claims are allowable. The Examiner's reasons for allowance indicate that particular claim elements are not disclosed or suggested by the prior art of record, yet the claims may be patentable for other reasons as well, including the inventive combination of all of the recited claim elements. It is not conceded that the specific limitations identified by the Examiner are necessary to distinguish the art of record or to satisfy the requirements of 35 U.S.C. § 112. Moreover, the Examiner does not assert, and it would not be conceded, that the Examiner's reasons have any bearing on the patentability of claims in any other applications directed to the disclosed subject matter.

Inventor : Won Cheol Seo et al.
Appl. No. : 14/815,433
Filed : July 31, 2015
Page : 2 of 2

Docket No.: 114898-8005.US02

In addition, each dependent claim stands on its own and may be allowable on its own merits. In particular, each dependent claim may be allowable on the basis of a combination of some of the features recited in the dependent claim and its base claim(s), which combination of features may not include all of the limitations identified in the Examiner's reasons for allowance.

Please apply the required fees in the amount of \$960.00, and any charges or credits, to Deposit Account No. 50-0665.

Respectfully submitted,

Date: February 10, 2016

/Bing Ai/
Bing Ai
Reg. No. 43,312

Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
Telephone: (858) 720-5700
Facsimile: (206) 359-7198

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

97075 7590 11/12/2015
Perkins Coie LLP - SDO General
P.O. Box 1247
Seattle, Washington 98111-1247

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/815,433	07/31/2015	Won Cheol Seo	114898-8005.US02	1096

TITLE OF INVENTION: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	02/12/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, CUONG QUANG	2811	257-098000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Perkins Coie LLP

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Seoul Semiconductor Co., Ltd.

Ansan-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
☒ Payment by credit card.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0665 (**DEFICIENCIES ONLY**).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Bing Ai/

Date February 10, 2016

Typed or printed name Bing Ai

Registration No. 43,312

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

129857582.1

Electronic Patent Application Fee Transmittal				
Application Number:		14815433		
Filing Date:		31-Jul-2015		
Title of Invention:		WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Won Cheol Seo		
Filer:		Bing Ai/Michelle Melendez		
Attorney Docket Number:		114898-8005.US02		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960


Electronic Acknowledgement Receipt	
EFS ID:	24884095
Application Number:	14815433
International Application Number:	
Confirmation Number:	1096
Title of Invention:	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME
First Named Inventor/Applicant Name:	Won Cheol Seo
Customer Number:	97075
Filer:	Bing Ai/Michelle Melendez
Filer Authorized By:	Bing Ai
Attorney Docket Number:	114898-8005.US02
Receipt Date:	10-FEB-2016
Filing Date:	31-JUL-2015
Time Stamp:	20:03:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	6660
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:


File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_Payment.pdf	48435 a0a44d3e0c8e3334af284f5d3ae8c2b089c e016	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30867 8157637a0b68bf4820a0cb6148eef8d24c7 e0378	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			79302		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Issue Classification 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.	
	Examiner CUONG Q NGUYEN	Art Unit 2811	

CPC					
Symbol				Type	Version
H01L	33	486		F	2013-01-01
H01L	33	42		I	2013-01-01
H01L	33	502		I	2013-01-01
H01L	33	44		I	2013-01-01
H01L	33	405		I	2013-01-01
H01L	27	153		I	2013-01-01
H01L	33	0079		A	2013-01-01
H01L	33	20		A	2013-01-01
H01L	33	38		I	2013-01-01
H01L	33	382		I	2013-01-01
H01L	33	46		I	2013-01-01
H01L	33	62		I	2013-01-01
H01L	2933	0016		A	2013-01-01
H01L	2924	0002		A	2013-01-01
H01L	33	10		I	2013-01-01
H01L	33	50		I	2013-01-01
H01L	33	24		I	2013-01-01
H01L	33	507		I	2013-01-01
H01L	33	642		I	2013-01-01
H01L	2933	0025		A	2013-01-01
H01L	2933	0033		A	2013-01-01
H01L	2933	0041		A	2013-01-01
H01L	2933	0075		A	2013-01-01
H01L	27	15		I	2013-01-01
H01L	33	22		I	2013-01-01
H01L	33	58		I	2013-01-01


CPC Combination Sets								
Symbol				Type	Set	Ranking	Version	
H01L		2924	/	0002	A	1	1	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/CUONG Q NGUYEN/ Primary Examiner.Art Unit 2811	12/09/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	52	1

Issue Classification 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.			
	Examiner CUONG Q NGUYEN	Art Unit 2811			

H01L		2924		00		A	1	2	2013-01-01
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/CUONG Q NGUYEN/ Primary Examiner.Art Unit 2811	12/09/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	52	1

Issue Classification 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED								
257			98			H	0	1	L	33 / 00 (2010.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
257	99																		

NONE		Total Claims Allowed:	
		19	
(Assistant Examiner)	(Date)		
/CUONG Q NGUYEN/ Primary Examiner. Art Unit 2811	12/09/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	52	1



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/815,433	07/31/2015	Won Cheol Seo	114898-8005.US02

CONFIRMATION NO. 1096

97075
Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

PUBLICATION NOTICE



OC00000078924807

Title: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

Publication No. US-2015-0340579-A1

Publication Date: 11/26/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

97075 7590 11/12/2015
Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 11/12/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/815,433	07/31/2015	Won Cheol Seo	114898-8005.US02	1096

TITLE OF INVENTION: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	02/12/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Perkins Coie LLP - SDO General
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/815,433	07/31/2015	Won Cheol Seo	114898-8005.US02	1096

TITLE OF INVENTION: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, CUONG QUANG	2811	257-098000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/815,433	07/31/2015	Won Cheol Seo	114898-8005.US02	1096

97075 7590 11/12/2015
Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/12/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/815,433	Applicant(s) SEO ET AL.	
	Examiner CUONG Q. NGUYEN	Art Unit 2811	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 52-70. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	5. <input type="checkbox"/> Examiner's Amendment/Comment
2. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>07/31/2015</u>	6. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance
3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. <input type="checkbox"/> Other _____.
4. <input type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date _____.	

/CUONG Q NGUYEN/ Primary Examiner, Art Unit 2811	
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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Reason for Allowance

1. Claims 52-70 are allowed.

The following is an examiner's statement of reasons for allowance: Prior art do not teach or render obvious a light emitting diode package having an arrangement as claimed such as “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other” (claim 52), “ a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and a lens to adjust an orientation angle of light emitted from the LED package” (claim 57), “a circuit board; a LED package bonded on the circuit board without bonding wires; wherein the LED package comprisinga first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes; a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the first conductive type semiconductor

Layer" (claim 59).

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. **Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the Fax Center number is (571) 273-8300. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989).**

4. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday. If attempts to reach the examiner by telephone are unsuccessful the examiner's supervisor Lynne Gurley who can be reached on (571) 272-1670.

/Cuong Q Nguyen/

Primary Examiner, Art Unit 2811

November 6, 2015

Notice of References Cited	Application/Control No. 14/815,433		Applicant(s)/Patent Under Reexamination SEO ET AL.	
	Examiner CUONG Q. NGUYEN		Art Unit 2811	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8,981,395 B2	03-2015	Choi; Pun Jae	H01L33/20	257/89
*	B	US-8,809,893 B2	08-2014	Choi; Pun Jae	H01L33/20	257/98
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				


FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 33/0079, 005, 385, 87	11/01/2015	CN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	88-103	11/01/2015	CN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST, EPO, JPO, inventor name (in eDAN)	11/01/2015	CN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
See search note		11/01/2015	CN

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UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1096

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/815,433	07/31/2015	257	2811	114898-8005.US02		
APPLICANTS Seoul Semiconductor Co., Ltd., Seoul, KOREA, REPUBLIC OF; INVENTORS Won Cheol Seo, Ansan-si, KOREA, REPUBLIC OF; Dae Sung Cho, Ansan-si, KOREA, REPUBLIC OF; ** CONTINUING DATA ***** This application is a CON of 14/708,029 05/08/2015 which is a CON of 13/194,317 07/29/2011 PAT 9070851 ** FOREIGN APPLICATIONS ***** REPUBLIC OF KOREA 10-2010-0092808 09/24/2010 REPUBLIC OF KOREA 10-2010-0092807 09/24/2010 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/17/2015						
Foreign Priority claimed <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No 35 USC 119(a-d) conditions met <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Verified and /CUONG QUANG NGUYEN/ Acknowledged Examiner's Signature		<input type="checkbox"/> Met after Allowance /CN/ Initials	STATE OR COUNTRY KOREA, REPUBLIC OF	SHEETS DRAWINGS 19	TOTAL CLAIMS 19	INDEPENDENT CLAIMS 3
ADDRESS Perkins Coie LLP - SDO General PO Box 1247 Seattle, WA 98111-1247 UNITED STATES						
TITLE WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.N./

Receipt date: 07/31/2015

Sheet 1 of 2

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 114898-8005.US02	Application No. Not yet assigned
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Seoul Semiconductor Co., Ltd.	
		14815433 - GAU: 2811	
		Filing Date Herewith	Group Art Unit Not yet assigned

U.S. Patent Documents							
Examiner Initial	Design ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	6876008	2005-04-05	Bhat et al.			
	2	7095061	2006-08-22	Steigerwald et al.			
	3	7417259	2008-08-26	Sakai et al.			
	4	7709849	2010-05-04	Kal et al.			
	5	7723736	2010-05-05	Lee et al.			
	6	7750469	2010-07-06	Cho et al.			
	7	7838891	2010-11-23	Lee et al.			
	8	7846755	2010-12-07	Kal et al.			
	9	7880181	2011-02-01	Yoon et al.			
	10	8319246	2012-11-27	Sugizaki			
	11	20080087902	2008-04-17	Lee et al.			
	12	20090039359	2009-02-12	Yoon et al.			
	13	20090085048	2009-04-02	Lee et al.			
	14	20090267085	2009-10-29	Lee et al.			
	15	20090283787	2009-11-19	Donofrio et al.			
	16	20100078656	2010-04-01	Seo et al.			
	17	20100078656	2010-04-01	Seo et al.			
	18	20100117111	2010-05-13	Illek et al.			
	19	20100148190	2010-06-17	Kim et al.			
	20	20100163887	2010-07-01	Kim et al.			
	21	20100163900	2010-07-01	Seo et al.			
	22	20100244060	2010-09-30	Lee et al.			
	23	20110101414	2011-05-05	Thompson et al.			
	24	20110140135	2011-06-16	Lee et al.			
	25	20110169040	2011-07-14	Seo et al.			
	26	20110175129	2011-07-21	Lee et al.			
	27	20120032218	2012-02-09	Choi et al.			

Examiner Signature /Cuong Nguyen/ (11/01/2015)	Date Considered 11/01/2015
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form (PTO-1449)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.N./

Receipt date: 07/31/2015

Sheet 2 of 2


Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 114898-8005.US02	Application No. Not yet assigned
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Seoul Semiconductor Co., Ltd.	
		14815433 - GAU: 2811	
		Filing Date Herewith	Group Art Unit Not yet assigned

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	28	100599012	2006-07-04	KR				
	29	100838197	2008-06-16	KR				
	30	2004006582	2004-01-08	JP				
	31	2004023568	2004-03-18	WO				
	32	2007001124	2007-01-04	WO				
	33	2008130656	2008-06-05	JP				
	34	2008141015	2008-06-19	JP				
	35	1020100016631	2010-02-12	KR				
	36	1020100036617	2010-04-08	KR				
	37	1020100079843	2010-07-08	KR				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	38	Notice of Allowance of US Patent Application No. 12/623,990 dated April 27, 2012
	39	Non-Final Office Action of US Patent Application No. 12/623,968 dated January 17, 2012
	40	Non-Final Office Action of US Patent Application No. 12/623,990 dated January 19, 2012
	41	Notice of Allowance of US Patent Application No. 12/624,011 dated January 24, 2012
	42	Non-Final Office Action of US Patent Application No. 12/123,162 dated August 5, 2010
	43	Notice of Allowance of US Patent Application No. 12/123,162 dated November 30, 2010
	44	Notice of Allowance of related US Patent Application No. 13/345,348 dated June 25, 2012
	45	Notice of Allowance of related US Patent Application No. 12/623,968 dated May 21, 2012
	46	Non-Final Office Action dated April 13, 2012 for US Patent Application No. 13/345,348.
	47	International Search Report and Written Opinion dated May 1, 2012, PCT/kr2011/006544
	48	Notice of Allowance dated January 11, 2013 issued for US Patent Application No. 13/482,851
	49	Non-Final Office Action issued on June 13, 2013, in US Patent Application No. 13/865,719
	50	Notice of Allowance issued on October 1, 2013, in US Patent Application No. 13/865,719


Examiner Signature /Cuong Nguyen/ (11/01/2015)	Date Considered 11/01/2015
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form (PTO-1449)

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47										
CLAIM		DATE								
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<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47										
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EAST Search History**EAST Search History (Interference)**


Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	5	((led or (light adj emitting)) and (contact adj hole) and (second adj electrode adj pad) and (protective adj insulation adj layer) and (semiconductor adj stack)).clm.	US-PGPUB; USPAT	OR	ON	2015/11/01 22:33

11/ 1/ 2015 10:34:46 PM**C:\ Users\ cnguyen4\ Documents\ EAST\ Workspaces\ EASTPush.wsp**

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1179	(led or (light adj emitting)) and (hole or via) and (electrode adj pad) and (package or packaging) and (@pd<="20120329" or @ad<="20120329" or @rlad<="20120329")	USPAT	OR	ON	2015/11/01 22:04
L2	1062	(led or (light adj emitting)) and (hole or via) and (electrode adj pad) and (package or packaging) and (@pd<="20110329" or @ad<="20110329" or @rlad<="20110329")	USPAT	OR	ON	2015/11/01 22:05
L3	1241	(led or (light adj emitting)) and (hole or via) and (electrode adj pad) and (package or packaging) and (@pd<="20110329" or @ad<="20110329" or @rlad<="20110329")	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/11/01 22:18

11/ 1/ 2015 10:29:48 PM**C:\ Users\ cnguyen4\ Documents\ EAST\ Workspaces\ EASTPush.wsp**

Issue Classification 	Application/Control No. 14815433	Applicant(s)/Patent Under Reexamination SEO ET AL.
	Examiner CUONG Q NGUYEN	Art Unit 2811

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED								
257			98			H	0	1	L	33 / 00 (2010.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
257	99																		

NONE		Total Claims Allowed:	
		19	
(Assistant Examiner)	(Date)		
/CUONG Q NGUYEN/ Primary Examiner, Art Unit 2811	11/01/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	52	1



별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual
Property Office

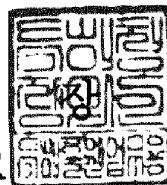
출 원 번 호 : 10-2010-0092807
Application Number

출 원 년 월 일 : 2010년 09월 24일
Filing Date SEP. 24, 2010

출 원 인 : 서울반도체 주식회사
Applicant(s) SEOUL SEMICONDUCTOR CO.,LTD

2015년 08월 20일

특 허 청
COMMISSIONER



제출 일자 : 2010-09-24

【서지사항】

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【지정된변리사】	이수완, 조진태, 윤종섭, 이성규, 이재웅
【포괄위임등록번호】	2009-036200-7
【발명의 국문명칭】	웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법
【발명의 영문명칭】	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME
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대리인 특허법인에이아이피 (서명 또는 인)

【수수료】

【출원료】	0 면	38,000 원
【가산출원료】	40 면	0 원
【우선권주장료】	0 건	0 원
【심사청구료】	25 항	1,130,000 원
【합계】		1,168,000 원

【명세서】

【발명의 명칭】

웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법{WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME}

【기술분야】

<1> 본 발명은 발광 다이오드 패키지 및 그것을 제조하는 방법에 관한 것으로, 더욱 상세하게는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법에 관한 것이다.

【배경기술】

<2> 발광 다이오드는 N형 반도체와 P형 반도체를 가지는 반도체 소자로서, 전자와 정공의 재결합에 의하여 빛을 발산한다. 이러한 발광 다이오드는 표시소자, 교통 신호기 및 백라이트로 널리 이용되고 있다. 또한, 발광 다이오드는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길어, 백열전구 및 형광등을 대체하여 일반 조명 용도로 그 사용 영역을 넓히고 있다.

<3> 발광 다이오드는 통상 최종적으로 발광 다이오드 모듈로서 사용된다. 발광 다이오드 모듈은 웨이퍼 레벨에서의 발광 다이오드 칩 제작 공정, 패키징 공정 및 모듈 공정을 거쳐 제작된다. 즉, 사파이어 기판과 같은 성장 기판 상에서 반도체층들을 성장시킨 후 웨이퍼 레벨에서 패터닝 공정 등을 거쳐 전극 패드들을 갖는 칩으로 제조되고, 개별 칩들로 분할된다(칩 제작 공정). 그 후, 개별 칩들을 리드 프

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레이프 또는 인쇄회로기 기판 등에 실장하고, 본딩 와이어를 이용하여 전극 패드들을 리드 단자들에 전기적으로 연결한 후, 몰딩 부재로 발광 다이오드 칩들을 몰딩함으로써 발광 다이오드 패키지가 제작된다(패키징 공정). 그 후, 상기 발광 다이오드 패키지를 MC-PCB와 같은 회로보드 상에 장착함으로써 광원 모듈과 같은 발광 다이오드 모듈이 완성된다(모듈 공정).

<4> 상기 패키징 공정에 의해 상기 발광 다이오드 칩은 하우징 및/또는 몰딩부재에 의해 외부 환경으로부터 보호된다. 나아가, 상기 몰딩 부재 내에 형광체를 함유시킴으로써, 백색 광원에 적합한 백색 발광 다이오드 패키지가 제공될 수 있다. 이러한 백색 발광 다이오드 패키지를 MC-PCB와 같은 회로보드 상에 장착하고 발광 다이오드 패키지에서 방출된 광의 지향 특성을 조절하기 위한 2차 렌즈를 발광 다이오드 패키지 상에 설치함으로써 특정 사용 용도에 적합한 백색 발광 다이오드 모듈이 제공될 수 있다.

<5> 그러나, 종래의 리드 프레임 또는 인쇄회로기판 등을 사용하는 발광 다이오드 패키지는 소형화가 어려울 뿐만 아니라, 방열 특성을 개선하는데 한계가 있다. 더욱이, 리드 프레임 또는 인쇄회로기판 등에 의한 광 흡수, 리드 단자에 의한 저항열 발생 등에 의해 발광 다이오드의 발광 효율이 감소되는 것은 잘 알려져 있다.

<6> 나아가, 칩 제작 공정, 패키징 공정 및 모듈화 공정이 각각 별도로 진행됨에 따라 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비용이 증가한다.

【발명의 내용】

【해결하려는 과제】

- <7> 본 발명이 해결하려는 과제는, 종래의 리드 프레임이나 인쇄회로기판 등을 이용할 필요없이 직접 회로보드에 모듈화할 수 있는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법을 제공하는 것이다.
- <8> 본 발명이 해결하려는 다른 과제는, 고효율 및 고방열 특성을 갖는 발광 다이오드 패키지 및 그것을 제조하는 방법을 제공하는 것이다.
- <9> 본 발명이 해결하려는 또 다른 과제는, 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비용을 절감할 수 있는 발광 다이오드 패키지 제조 방법을 제공하는 것이다.
- <10> 본 발명이 해결하려는 또 다른 과제는, 고효율 및 고방열 특성을 갖는 발광 다이오드 모듈 및 그것을 제조하는 방법을 제공하는 것이다.

【과제의 해결 수단】

- <11> 본 발명의 일 태양에 따른 발광 다이오드 패키지는, 제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 반도체 적층 구조체; 상기 제2 도전형 하부 반도체층 및 활성층을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들; 상기 반도체 적층 구조체 아래에 위치하고, 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 상부 반도체층에 전기적으로 접속된 제1 범프; 상기 반도체 적층 구조체 아래에 위치하고, 상기 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프; 및 상기 반도체 적층 구조체의 측면을 덮는

보호 절연층을 포함한다.

<12> 상기 보호 절연층은 상기 반도체 적층 구조체의 측벽 전면을 덮어 외부 환경, 예컨대 수분 등으로부터 상기 반도체 적층 구조체를 보호한다. 나아가, 상기 제1 범프 및 제2 범프는 서로 동일 높이를 갖고, 이들의 단면은 동일 평면 상에 위치할 수 있다. 상기 발광 다이오드 패키지는 상기 제1 범프 및 제2 범프를 통해 MC-PCB 등의 회로보드 상에 전기적으로 접속될 수 있다.

<13> 본 발명에 따른 발광 다이오드 패키지는 MC-PCB 등의 회로보드에 직접 장착하여 모듈화할 수 있는 웨이퍼 레벨 패키지로서, 리드프레임이나 인쇄회로기판 등을 사용하는 종래의 발광 다이오드 패키지와 구별되며, 또한, 리드프레임이나 인쇄회로기판 등을 이용하여 패키징되는 통상의 발광 다이오드 칩과 구별된다.

<14> 한편, 파장 변환기가 상기 제1 도전형 상부 반도체층 상에 위치할 수 있다. 파장 변환기는 보호절연층과 다른 재료로 구성되어 보호절연층과 구별된다. 상기 파장변환기는 형광체 시트 또는 불순물이 도핑된 단결정 기판일 수 있다. 상기 파장변환기의 측면은 상기 보호절연층과 나란할 수 있다. 즉, 상기 파장변환기는 상기 보호절연층의 윗면을 덮는다.

<15> 상기 보호절연층은 실리콘 산화막 또는 실리콘 질화막을 포함할 수 있으며, 단일층 또는 다중층으로 형성될 수 있다. 이와 달리, 상기 보호절연층은 굴절률이 서로 다른 절연층들을 반복 적층한 분포브래그 반사기일 수 있다.

<16> 한편, 상기 제1 도전형 상부 반도체층은 거칠어진 표면을 가질 수 있다. 거

질어진 표면은 광 추출 효율을 향상시킨다.

<17> 몇몇 실시예들에 있어서, 상기 제1 및 제2 범프들의 측면은 절연층에 의해 덮일 수 있다. 이 절연층은 상기 제1 및 제2 범프들의 측면의 적어도 일부를 덮는다. 또한, 더미 범프가 상기 제1 및 제2 범프들 사이에 위치할 수 있다. 더미 범프는 반도체 적층 구조체에서 생성된 열을 방출한다.

<18> 몇몇 실시예들에 있어서, 상기 발광 다이오드 패키지는 관통홀들을 갖는 절연 기판을 더 포함할 수 있으며, 상기 제1 및 제2 범프들은 상기 절연 기판의 관통홀에 형성될 수 있다. 상기 절연 기판은 사파이어 또는 실리콘 기판일 수 있다.

<19> 한편, 상기 발광 다이오드 패키지는, 상기 제2 도전형 하부 반도체층에 접촉하는 제2 콘택층; 상기 복수개의 콘택홀들 내에서 상기 제1 도전형 상부 반도체층에 전기적으로 접촉하는 제1 접촉부들 및 상기 제1 접촉부들을 서로 연결하는 연결부를 포함하는 제1 콘택층; 상기 제1 콘택층과 상기 제2 콘택층 사이에 개재되어 상기 제2 콘택층을 덮는 제1 절연층; 및 상기 제1 콘택층 아래에서 상기 제1 콘택층을 덮는 제2 절연층을 더 포함할 수 있다. 상기 제1 범프는 상기 제2 절연층 아래에 위치하여 상기 제1 콘택층에 전기적으로 접속될 수 있으며, 상기 제2 범프는 상기 제2 절연층 아래에 위치하여 상기 제2 콘택층에 전기적으로 접속될 수 있다.

<20> 상기 보호절연층은 상기 제1 절연층 및/또는 제2 절연층에 의해 형성될 수 있다. 따라서, 상기 보호절연층은 상기 제1 절연층 및/또는 상기 제2 절연층을 포함할 수 있다.

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- <21> 나아가, 상기 발광 다이오드 패키지는, 상기 제2 절연층 아래에 위치하고, 상기 제2 절연층을 관통하여 상기 제1 콘택층에 접속하는 제1 전극 패드; 및 상기 제2 절연층 아래에 위치하고, 상기 제2 절연층 및 상기 제1 절연층을 관통하여 상기 제2 콘택층에 접속하는 제2 전극패드를 더 포함할 수 있다. 상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드 아래에서 이들에 전기적으로 접속될 수 있다.
- <22> 또한, 상기 제1 절연층 및 제2 절연층 중 적어도 하나는 분포 브래그 반사기일 수 있다.
- <23> 본 발명의 또 다른 태양에 따르면, 앞서 설명한 발광 다이오드 패키지를 포함하는 발광 다이오드 모듈이 제공된다. 이 모듈은 회로 보드; 상기 회로보드에 장착된 상기 발광 다이오드 패키지 및 상기 발광 다이오드 패키지에서 방출된 광의 지향각을 조절하기 위한 렌즈를 포함할 수 있다. 나아가, 상기 회로보드는 MC-PCB일 수 있으며, 상기 MC-PCB 상에 복수개의 상기 발광 다이오드 패키지들이 장착될 수 있다.
- <24> 본 발명의 또 다른 태양에 따르면, 발광 다이오드 패키지 제조방법이 제공된다. 이 방법은, 성장 기판 상에 제1 도전형 반도체층, 활성층 및 제2 도전형 반도체층을 포함하는 반도체 적층 구조체를 형성하고, 상기 반도체 적층 구조체를 패터닝하여 칩 분리 영역을 형성함과 아울러, 상기 제2 도전형 반도체층 및 활성층을 패터닝하여 상기 제1 도전형 반도체층을 노출시키는 복수개의 콘택홀들을 형성하고, 상기 칩 분리 영역 내의 반도체 적층 구조체의 측면을 덮는 보호 절연층

을 형성하고, 상기 반도체 적층 구조체 상부에 제1 범프 및 제2 범프를 형성하는 것을 포함한다. 상기 제1 범프는 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 반도체층에 전기적으로 접속되고, 상기 제2 범프는 상기 제2 도전형 반도체층에 전기적으로 접속된다.

<25> 몇몇 실시예들에 있어서, 상기 성장 기판은 상기 활성층에서 생성된 광의 파장을 변환하기 위한 불순물을 포함할 수 있다. 상기 성장 기판은 사파이어 또는 실리콘 기판일 수 있다.

<26> 몇몇 실시예들에 있어서, 상기 방법은, 상기 성장 기판을 제거하여 제1 도전형 반도체층을 노출시키고, 상기 노출된 제1 도전형 반도체층 상에 형광체 시트를 부착하는 것을 더 포함할 수 있다. 상기 보호 절연층은 칩 분리 영역을 따라 개별 패키지로 분할하는 공정에서 상기 형광체 시트와 함께 분할될 수 있다.

<27> 상기 방법은 또한, 상기 제2 도전형 반도체층 상에 제2 콘택층을 형성하고, 상기 제2 콘택층 및 상기 복수개의 콘택홀의 측벽을 덮는 제1 절연층을 형성하되, 상기 제1 절연층은 상기 복수개의 콘택홀 내의 제1 도전형 반도체층을 노출시키는 개구부들을 갖고, 상기 제1 절연층 상에 제1 콘택층을 형성하되, 상기 제1 콘택층은 상기 복수개의 콘택홀 내에 노출된 제1 도전형 반도체층에 접촉하는 접촉부들 및 상기 접촉부들을 연결하는 연결부를 갖고, 상기 제1 콘택층을 덮는 제2 절연층을 형성하고, 상기 제1 및 제2 절연층을 패터닝하여 상기 제1 콘택층을 노출시키는 개구부를 형성함과 아울러, 상기 제2 콘택층을 노출시키는 개구부를 형성하고, 상기 제2 절연층 상에 상기 개구부들을 통해 상기 제1 콘택층에 접속하는 제1 전극

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패드 및 제2 콘택층에 접속하는 제2 전극 패드를 형성하는 것을 더 포함할 수 있다. 상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드에 전기적으로 접속된다.

<28> 몇몇 실시예들에 있어서, 상기 제1 범프 및 제2 범프를 형성하는 것은, 상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 개구부들을 갖는 절연층 패턴을 형성하고, 상기 노출된 상기 제1 전극 패드 및 제2 전극 패드 상에 금속 재료를 도금하는 것을 포함할 수 있다. 나아가, 상기 제1 범프 및 제2 범프를 형성하는 동안, 상기 제1 범프 및 제2 범프 사이에 더미 범프를 형성하는 것을 더 포함할 수 있다.

<29> 또 다른 실시예들에 있어서, 상기 제1 범프 및 제2 범프를 형성하는 것은, 절연 기판 내에 관통홀들을 형성하고, 상기 관통홀들을 금속재료로 채우고, 상기 금속재료를 갖는 절연 기판을 상기 제1 전극 패드 및 제2 전극 패드 상에 본딩하는 것을 포함할 수 있다. 나아가, 상기 절연기판을 본딩하기 전에, 상기 제1 전극 패드 및 제2 전극 패드를 덮는 절연층을 형성하고, 상기 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 것을 더 포함할 수 있다.

【발명의 효과】

<30> 본 발명에 따르면, 종래의 리드 프레임이나 인쇄회로기판 등을 이용할 필요 없이 직접 회로보드에 모듈화할 수 있는 웨이퍼 레벨(또는 칩 레벨) 발광 다이오드 패키지가 제공될 수 있다. 이에 따라, 고효율 및 고방열 특성을 갖는 발광 다이오드 패키지가 제공되며, 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비

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용을 절감할 수 있다. 또한, 상기 발광 다이오드 패키지를 장착함으로써, 고효율 및 고방열 특성을 갖는 발광 다이오드 모듈이 제공될 수 있다.

【도면의 간단한 설명】

<31> 도 1은 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 설명하기 위한 개략적인 단면도이다.

도 2는 본 발명의 다른 실시예에 따른 발광 다이오드 패키지를 설명하기 위한 개략적인 단면도이다.

도 3은 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 장착한 발광 다이오드 모듈을 설명하기 위한 단면도이다.

도 4 내지 도 12는 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 제조하는 방법을 설명하기 위한 도면들이다. 도 5 내지 도 10에서 (a)는 평면도를 나타내고, (b)는 (a)의 절취선 A-A를 따라 취해진 단면도를 나타낸다.

도 13은 본 발명의 다른 실시예에 따른 발광 다이오드 패키지를 제조하는 방법을 설명하기 위한 단면도이다.

【발명을 실시하기 위한 구체적인 내용】

<32> 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서,

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구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<33> 도 1은 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)를 설명하기 위한 단면도이다.

<34> 도 1을 참조하면, 상기 발광 다이오드 패키지(10)는 반도체 적층 구조체(30), 제1 콘택층(35), 제2 콘택층(31), 제1 절연층(33), 제2 절연층(37), 제1 전극 패드(39a), 제2 전극 패드(39b), 제1 범프(43a) 및 제2 범프(43b)를 포함한다. 또한, 상기 발광 다이오드 패키지(10)는 절연층(41), 더미 범프(43c) 및 파장 변환기(45)를 포함할 수 있다.

<35> 상기 반도체 적층 구조체(30)는 제1 도전형의 상부 반도체층(25), 활성층(27) 및 제2 도전형의 하부 반도체층(29)을 포함한다. 상기 활성층(27)은 상기 상부 및 하부 반도체층들(25, 29) 사이에 개재된다.

<36> 상기 활성층(27), 상기 상부 및 하부 반도체층들(25, 29)은 III-N 계열의 화합물 반도체, 예컨대 (Al, Ga, In)N 반도체로 형성될 수 있다. 상기 상부 및 하부 반도체층들(25, 29)은 각각 단일층 또는 다중층일 수 있다. 예를 들어, 상기 상부 및/또는 하부 반도체층(25, 29)은 콘택층과 클래드층을 포함할 수 있으며, 또한 초격자층을 포함할 수 있다. 상기 활성층(27)은 단일 양자우물 구조 또는 다중 양자우물 구조일 수 있다. 바람직하게, 상기 제1 도전형은 n형이고, 상기 제2 도전형은 p형이다. 저항이 상대적으로 작은 n형 반도체층으로 상부 반도체층(25)을 형성할 수 있어, 상부 반도체층(25)의 두께를 상대적으로 두껍게 형성할 수 있다. 따라서,

상기 상부 반도체층(25)의 상부면에 거칠어진 면(R)을 형성하는 것이 용이하며, 거칠어진 면(R)은 활성층(27)에서 발생된 광의 추출 효율을 향상시킨다.

<37> 상기 반도체 적층 구조체(30)는 상기 제2 도전형 하부 반도체층(29) 및 활성층(27)을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들(도 5(b), 30a 참조)을 가지며, 제1 콘택층(35)이 상기 복수개의 콘택홀들에 노출된 제1 도전형 상부 반도체층(25)에 접촉한다.

<38> 한편, 제2 콘택층(31)은 상기 제2 도전형 하부 반도체층(29)에 접촉한다. 제2 콘택층(31)은 반사 금속층을 포함하며, 활성층(25)에서 생성된 광을 반사시킨다. 또한, 상기 제2 콘택층(31)은 제2 도전형 하부 반도체층(29)에 오믹 콘택할 수 있다.

<39> 제1 절연층(33)은 제2 콘택층(31)을 덮는다. 또한, 상기 제1 절연층(33)은 복수개의 콘택홀들(30a)에 노출된 반도체 적층 구조체의 측벽을 덮는다. 나아가, 상기 제1 절연층(33)은 반도체 적층 구조체(30)의 측면을 덮을 수 있다. 제1 절연층(33)은 제1 콘택층(35)을 제2 콘택층(31)으로부터 절연시키며, 나아가, 복수개의 콘택홀들(30a) 내에 노출된 제2 도전형 하부 반도체층(29)과 활성층(27)을 제1 콘택층(35)으로부터 절연시킨다. 제1 절연층(33)은 실리콘 산화막 또는 실리콘 질화막의 단일층으로 형성될 수 있으나, 이에 한정되는 것은 아니며 다중층으로 형성될 수 있다. 더욱이, 상기 제1 절연층(33)은 굴절률이 서로 다른 절연층들, 예컨대 SiO₂/TiO₂ 또는 SiO₂/Nb₂O₅를 반복하여 적층한 분포 브래그 반사기일 수 있다.

<40> 상기 제1 콘택층(35)은 상기 제1 절연층(33) 아래에 위치하며, 상기 복수개

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의 콘택홀들(30a) 내에서 상기 제1 절연층(33)을 관통하여 제1 도전형 상부 반도체층(25)에 접촉한다. 제1 콘택층(35)은 제1 도전형 상부 반도체층(25)에 접촉하는 접촉부들(35a) 및 접촉부들(35a)을 서로 연결하는 연결부(35b)를 포함한다. 따라서, 연결부(35b)에 의해 접촉부들(35a)이 서로 전기적으로 연결된다. 상기 제1 콘택층(35)은 제1 절연층(33)의 일부 영역 아래에 형성되며, 반사 금속층으로 형성될 수 있다.

<41> 상기 제2 절연층(37)은 제1 콘택층(35) 아래에서 제1 콘택층(35)을 덮는다. 나아가, 상기 제2 절연층(37)은 제1 절연층(33)을 덮으며, 반도체 적층 구조체(30)의 측면을 덮을 수 있다. 상기 제2 절연층(37)은 단일층 또는 다중층으로 형성될 수 있으며, 분포 브래그 반사기일 수 있다.

<42> 상기 제1 전극 패드(39a) 및 제2 전극 패드(39b)는 상기 제2 절연층(37) 아래에 위치한다. 제1 전극 패드(39a)는 제2 절연층(37)을 관통하여 제1 콘택층(35)에 접속될 수 있다. 또한, 제2 전극 패드(39b)는 제2 절연층(39) 및 제1 절연층(33)을 관통하여 제1 콘택층(31)에 접속될 수 있다.

<43> 제1 범프(43a) 및 제2 범프(43b)는 각각 상기 제1 및 제2 전극 패드(39a, 39b) 아래에 접속한다. 제1 범프(43a) 및 제2 범프(43b)는 도금 기술에 의해 형성될 수 있다. 제1 및 제2 범프(43a, 43b)는 MC-PCB와 같은 회로보드에 전기적으로 접속하는 단자들로서, 그 끝 단면들이 동일면에 나란할 수 있다. 나아가, 제1 전극 패드(39a)와 제2 전극 패드(39b)가 동일 레벨에 형성될 수 있으며, 따라서, 제1 범프(43a)와 제2 범프(43b) 또한 동일면 상에 형성될 수 있다. 이에 따라, 제1 및 제

2 범프(43a, 43b)는 동일한 높이를 가질 수 있다.

<44> 한편, 상기 제1 범프(43a)와 제2 범프(43b) 사이에 더미 범프(43c)가 위치할 수 있다. 더미 범프(43c)는 제1 및 제2 범프(43a, 43b)를 형성하는 동안 함께 형성될 수 있으며, 제1 및 제2 범프(43a, 43b)와 함께 반도체 적층 구조체(30)에서 생성된 열을 방출하기 위한 열 경로를 제공할 수 있다.

<45> 절연층(41)은 제1 범프(43a) 및 제2 범프(43b)의 측면을 덮을 수 있다. 절연층(41)은 또한 더미 범프(43c)의 측면을 덮을 수 있다. 나아가, 상기 절연층(41)은 제1 범프(43a), 제2 범프(43b) 및 더미 범프(43c) 사이의 영역을 채워 외부로부터 반도체 적층 구조체(30)로 수분이 침투하는 것을 방지한다. 절연층(41)은 또한 제1 전극 패드(39a) 및 제2 전극 패드(39b)의 측면을 덮어 제1 및 제2 전극 패드들(39a, 39b)을 외부 환경으로부터 보호한다. 절연층(41)은 제1 및 제2 범프(43a, 43b)의 측면 전체를 덮을 수 있으나, 이에 한정되는 것은 아니며, 제1 및 제2 범프(43a, 43b)의 끝 단면 근처의 일부 측면을 제외하고 나머지 측면을 덮을 수 있다.

<46> 절연층(41)이 제1 전극 패드(39a) 및 제2 전극 패드(39b)의 측면을 덮는 것으로 설명하였지만, 이에 한정되는 것은 아니며, 다른 절연층을 이용하여 제1 및 제2 전극 패드(39a, 39b)를 덮을 수 있으며, 상기 절연층(41)은 상기 다른 절연층 아래에 형성될 수 있다. 이 경우, 제1 및 제2 범프들(43a, 43b)은 상기 다른 절연층을 관통하여 상기 제1 및 제2 전극 패드(39a, 39b)에 접촉할 수 있다.

<47> 한편, 상기 제1 도전형 상부 반도체층(25) 상에 파장 변환기(45)가 위치한다. 파장 변환기(45)는 제1 도전형 상부 반도체층(25)의 상부면에 접촉할 수

있다. 파장 변환기(45)는 균일한 두께를 갖는 형광체 시트일 수 있으나, 이에 한정되는 것은 아니며, 파장 변환을 위한 불순물이 도핑된 기관, 예컨대 사파이어 또는 실리콘 기관일 수 있다.

<48> 본 실시예에 있어서, 반도체 적층 구조체(30)의 측면은 보호 절연층으로 덮인다. 상기 보호 절연층은 예컨대, 상기 제1 절연층(33) 및/또는 제2 절연층(37)을 포함할 수 있다. 나아가, 제1 콘택층(35)은 상기 제2 절연층(37)으로 덮여 외부 환경으로부터 보호되며, 제2 콘택층(31)은 제1 절연층(33) 및 제2 절연층(37)으로 덮여 외부 환경으로부터 보호될 수 있다. 또한, 제1 전극 패드(39a) 및 제2 전극 패드(39b) 또한 예컨대 절연층(41)에 의해 보호된다. 이에 따라, 외부 환경으로부터 수분 등에 의해 반도체 적층 구조체(30)가 열화되는 것을 방지할 수 있다.

<49> 한편, 상기 파장 변환기(45)는 웨이퍼 레벨에서 제1 도전형 상부 반도체층(25) 상에 부착될 수 있으며, 그 후 칩 분리 공정에서 보호절연층과 함께 분할될 수 있다. 따라서, 상기 파장 변환기(45)의 측면은 보호절연층과 나란할 수 있다. 또한, 상기 파장 변환기(45)의 측면은 절연층(41)의 측면과도 나란할 수 있다.

<50> 도 2는 본 발명의 또 다른 실시예에 따른 발광 다이오드 패키지(20)를 설명하기 위한 개략적인 단면도이다.

<51> 도 2를 참조하면, 상기 발광 다이오드 패키지(20)는 앞서 설명한 발광 다이오드 패키지(10)와 대체로 동일하나, 제1 및 제2 범프들(53a, 53b)이 기관(51) 내에 형성된 것에 차이가 있다.

<52> 즉, 기관(51)은 관통홀들을 포함하며, 제1 및 제2 범프들(53a, 53b)이 각각 관통홀 내에 형성된다. 상기 기관(61)은 절연 기관으로서, 사파이어 또는 실리콘 기관일 수 있으나, 이에 한정되는 것은 아니다. 상기 제1 및 제2 범프들(53a, 53b)과 함께 기관(51)이 제1 전극 패드(39a) 및 제2 전극 패드(39b)에 부착될 수 있다. 이때, 제1 및 제2 전극 패드들(39a, 39b)이 외부에 노출되는 것을 방지하기 위해, 절연층(49)이 제1 및 제2 전극 패드들(39a, 39b)의 측면 및 하부면을 덮을 수 있다. 또한, 상기 절연층(49)은 제1 및 제2 전극 패드들(39a, 39b)을 노출시키는 개구부들을 가질 수 있으며, 이들 개구부들 내에 추가 금속층(55a, 55b)이 위치할 수 있다. 상기 추가 금속층(55a, 55b)은 본딩 메탈일 수 있다.

<53> 도 3은 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)들을 회로보드 상에 장착한 발광 다이오드 모듈을 설명하기 위한 단면도이다.

<54> 도 3을 참조하면, 상기 발광 다이오드 모듈은 회로보드(61), 예컨대 MC-PCB, 발광 다이오드 패키지(10) 및 렌즈(71)를 포함한다. 상기 회로보드(61), 예컨대 MC-PCB는 발광 다이오드 패키지(10)를 장착하기 위한 접속 패드들(63a, 63b)을 갖는다. 상기 접속 패드들(63a, 63b) 상에 각각 발광 다이오드 패키지(10)의 제1 및 제2 범프들(도 1의 43a, 43b)이 접속된다.

<55> 상기 회로보드(61) 상에 복수개의 발광 다이오드 패키지들(10)이 장착될 수 있으며, 렌즈(71)가 상기 발광 다이오드 패키지들(10)의 지향각 등 광 특성을 조절하도록 발광 다이오드 패키지들(10) 상에 설치된다.

<56> 또 다른 실시예에서, 상기 발광 다이오드 패키지들(10) 대신에 발광 다이오

드 패키지들(20)이 장착될 수 있다.

<57> 도 4 내지 도 12는 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)를 제조하는 방법을 설명하기 위한 도면들이다. 도 5 내지 도 10에서 (a)는 평면도를 나타내고, (b)는 (a)의 절취선 A-A를 따라 취해진 단면도를 나타낸다.

<58> 도 4를 참조하면, 성장 기판(21) 상에 제1 도전형 반도체층(25), 활성층(27) 및 제2 도전형 반도체층(29)을 포함하는 반도체 적층 구조체(30)가 형성된다. 성장 기판(21)은 사파이어 기판일 수 있으나, 이에 한정되는 것은 아니며, 다른 이종기판, 예컨대 실리콘 기판일 수 있다. 상기 제1 및 제2 도전형 반도체층들(25, 29)은 각각 단일층 또는 다중층으로 형성될 수 있다. 또한, 상기 활성층(27)은 단일 양자우물 구조 또는 다중 양자우물 구조로 형성될 수 있다.

<59> 상기 화합물 반도체층들은 III-N 계열의 화합물 반도체로 형성될 수 있으며, 금속유기화학기상증착법(MOCVD) 또는 분자선 증착법(molecular beam epitaxy; MBE) 등의 공정에 의해 성장 기판(21) 상에 성장될 수 있다.

<60> 한편, 화합물 반도체층들을 형성하기 전, 버퍼층(미도시됨)이 형성될 수 있다. 버퍼층은 희생 기판(21)과 화합물 반도체층들의 격자 부정합을 완화하기 위해 채택되며, 질화갈륨 또는 질화알루미늄 등의 질화갈륨 계열의 물질층일 수 있다.

<61> 도 5 (a) 및 (b)를 참조하면, 상기 반도체 적층 구조체(30)를 패터닝하여 칩(패키지) 분리 영역(30b)을 형성함과 아울러, 상기 제2 도전형 반도체층(29) 및 활성층(27)을 패터닝하여 상기 제1 도전형 반도체층(25)을 노출시키는 복수개의 콘택

홀들(30a)을 형성한다. 상기 반도체 적층 구조체(30)는 사진 및 식각 공정을 사용하여 패터닝될 수 있다.

<62> 칩 분리 영역(30b)은 나중에 개별 발광 다이오드 패키지로 분할하는 영역으로, 칩 분리 영역(30b)에 제1 도전형 반도체층(25), 활성층(27) 및 제2 도전형 반도체층(29)의 측면이 노출된다. 상기 칩 분리 영역(30b)은 바람직하게 기판(21)면을 노출시키도록 형성될 수 있으나, 반드시 이에 한정되는 것은 아니다.

<63> 한편, 상기 복수개의 콘택홀들(30a)은 원형일 수 있으나, 이에 한정되는 것은 아니며 다양한 형상을 가질 수 있다. 제2 도전형 반도체층(29) 및 활성층(27)이 복수개의 콘택홀들(30a)의 측벽에 노출된다. 상기 콘택홀들(30a)의 측벽은 도시한 바와 같이 경사지게 형성될 수 있다.

<64> 도 6 (a) 및 (b)를 참조하면, 제2 도전형 반도체층(29) 상에 제2 콘택층(31)이 형성된다. 제2 콘택층(31)은 복수개의 콘택홀들(30a)을 제외한 반도체 적층 구조체(30) 상에 형성된다.

<65> 제2 콘택층(31)은 예컨대 ITO와 같은 투명 도전성 산화막 또는 은(Ag) 또는 Al과 같은 반사 금속층을 포함할 수 있으며, 단일층 또는 다중층으로 형성될 수 있다. 제2 콘택층(31)은 또한 제2 도전형 반도체층(29)에 오픈 접촉하도록 형성된다.

<66> 제2 콘택층(31)은 복수개의 콘택홀들(30a)을 형성한 후에 형성될 수 있으나, 이에 한정되는 것은 아니며, 복수개의 콘택홀들(30a)을 형성하기 전에 미리 형성될 수도 있다.

<67> 도 7 (a) 및 (b)를 참조하면, 제2 콘택층(31)을 덮는 제1 절연층(33)이 형성된다. 제1 절연층(33)은 칩 분리 영역(30b)에 노출된 반도체 적층 구조체(30)의 측면을 덮을 수 있으며, 또한, 복수개의 콘택홀들(30a)의 측벽을 덮을 수 있다. 다만, 상기 제1 절연층(33)은 복수개의 콘택홀들(30a) 내에서 상기 제1 도전형 반도체층(25)을 노출시키는 개구부들(33a)을 갖는다.

<68> 제1 절연층(33)은 실리콘 산화막 또는 실리콘 질화막과 같은 절연물질의 단일층 또는 다중층으로 형성될 수 있다. 나아가, 상기 제1 절연층(33)은 굴절률이 서로 다른 절연층을 반복 적층한 분포 브래그 반사기로 형성될 수 있다. 예컨대, 상기 제1 절연층(33)은 $\text{SiO}_2/\text{TiO}_2$ 또는 $\text{SiO}_2/\text{Nb}_2\text{O}_5$ 를 반복 적층하여 형성할 수 있다. 또한, 상기 제1 절연층(33)을 형성하는 각 절연층의 두께를 조절함으로써 청색광, 녹색광 및 적색광의 넓은 파장 범위에 걸쳐 반사율이 높은 분포 브래그 반사기가 형성될 수 있다.

<69> 도 8 (a) 및 (b)를 참조하면, 상기 제1 절연층(33) 상에 제1 콘택층(35)이 형성된다. 제1 콘택층(35)은 콘택홀들(30a) 내에 노출된 제1 도전형 반도체층(25)에 접촉하는 접촉부들(35a) 및 접촉부들(35a)을 서로 연결하는 연결부(35b)를 포함한다. 제1 콘택층(35)은 반사 금속층으로 형성될 수 있으나, 이에 한정되는 것은 아니다.

<70> 제1 콘택층(35)은 반도체 적층 구조체(30)의 일부 영역 상에 형성되며, 제1 콘택층(35)이 형성된 영역 이외의 영역에는 제1 절연층(33)이 노출된다.

<71> 도 9 (a) 및 (b)를 참조하면, 상기 제1 콘택층(35) 상에 제2 절연층(37)이

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형성된다. 제2 절연층(37)은 실리콘 산화막 또는 실리콘 질화막 등의 단일층 또는 다중층으로 형성될 수 있으며, 또한 굴절률이 서로 다른 절연층을 반복 적층한 분포 브래그 반사기로 형성될 수 있다.

<72> 제2 절연층(37)은 제1 콘택층(35)을 덮으며 또한 제1 절연층(33)을 덮을 수 있다. 제2 절연층(37)은 또한 칩 분리 영역(30b)에서 반도체 적층 구조체(30)의 측면을 덮을 수 있다.

<73> 한편, 상기 제2 절연층(37)은 제1 콘택층(35)을 노출시키는 개구부(37a)를 갖는다. 또한, 상기 제2 절연층(37) 및 제1 절연층(33)에 제2 콘택층(31)을 노출시키는 개구부(37b)가 형성된다.

<74> 도 10 (a) 및 (b)를 참조하면, 상기 제2 절연층(37) 상에 제1 및 제2 전극 패드들(39a, 39b)이 형성된다. 제1 전극 패드(39a)는 개구부(37a)를 통해 제1 콘택층(35)에 접속되고, 제2 전극 패드(39b)는 개구부(37b)를 통해 제2 콘택층(31)에 접속된다.

<75> 상기 제1 전극 패드(39a)와 제2 전극 패드(39b)는 서로 이격되며, 상기 제1 및 제2 전극 패드들(39a, 39b)은 각각 상대적으로 넓은 면적, 예컨대 발광 다이오드 패키지 면적의 1/2 미만이며 1/3 이상의 면적을 가질 수 있다.

<76> 도 11을 참조하면, 상기 제1 및 제2 전극 패드(39a, 39b) 상에 절연층(41)이 형성된다. 절연층(41)은 제1 및 제2 전극 패드(39a, 39b)를 덮으며, 이들 전극 패드들(39a, 39b)의 상부면을 노출시키는 홈을 갖는다. 또한, 상기 제1 전극 패드

(39a)와 제2 전극 패드(39b) 사이에서 제2 절연층(37)을 노출시키는 홈을 가질 수 있다.

<77> 이어서, 상기 절연층(41) 내의 홈들에 제1 및 제2 범프(43a, 43b)가 형성되고 또한, 제1 범프와 제2 범프 사이에 더미 범프(43c)가 형성될 수 있다.

<78> 상기 범프들은 도금, 예컨대 전기 도금을 사용하여 형성될 수 있다. 필요한 경우, 도금을 위한 시드층이 형성될 수도 있다.

<79> 한편, 상기 제1 및 제2 범프(43a, 43b)가 형성된 후, 상기 절연층(41)은 제거될 수도 있다. 예를 들어, 상기 절연층(41)은 포토레지스트와 같은 폴리머로 형성될 수 있으며, 범프들이 완성된 후 제거될 수 있다. 이와 달리, 상기 절연층(41)은 제1 범프 및 제2 범프(43a, 43b)의 측면을 보호하기 위해 남겨질 수도 있다.

<80> 본 실시예에 있어서, 제1 전극 패드 및 제2 전극 패드(39a, 39b) 상에 절연층(41)을 바로 형성하는 것으로 도시 및 설명하였으나, 제1 전극 패드 및 제2 전극 패드(39a, 39b)를 덮는 다른 절연층을 형성할 수도 있다. 상기 다른 절연층은 제1 전극 패드(39a) 및 제2 전극 패드(39b)를 노출시키는 개구부들을 갖도록 형성된다. 이어서, 상기 절연층(41) 및 범프 형성 공정이 수행될 수 있다.

<81> 도 12를 참조하면, 상기 성장 기관(21)이 제거되고 파장 변환기(45)가 제1 도전형 반도체층(25)에 부착된다. 성장 기관(21)은 레이저 리프트 오프(Laser lift-off; LLO)와 같은 광학적 기술 또는 기계적 연마 또는 화학적 에칭 기술을 이용하여 제거될 수 있다.

- <82> 그 후, 노출된 제1 도전형 반도체층(25)의 표면에 PEC 에칭 등에 의한 이방성 에칭에 의해 거칠어진 면이 형성될 수 있다.
- <83> 한편, 형광체를 함유하는 형광체 시트 등의 파장 변환기가 상기 제1 도전형 반도체층(25)에 부착될 수 있다.
- <84> 이와 달리, 상기 성장 기관(21)은 활성층(27)에서 생성된 광의 파장을 변환하기 위한 불순물을 함유할 수 있으며, 이 경우, 상기 성장 기관(21)이 파장 변환기(45)로 사용될 수 있다.
- <85> 그 후, 칩 분리 영역(30b)을 따라 개별 패키지로 분할함으로써 발광 다이오드 패키지(10)가 완성된다. 이때, 상기 파장 변환기(45)와 함께 제2 절연층(37)이 함께 절단됨으로써 절단면이 서로 나란하게 형성될 수 있다.
- <86> 도 13은 본 발명의 또 다른 실시예에 따른 발광 다이오드 패키지(20)를 제조하기 위한 방법을 설명하기 위한 단면도이다.
- <87> 도 13을 참조하면, 본 실시예에 따른 발광 다이오드 패키지(20) 제조 방법은 제1 전극 패드(39a) 및 제2 전극 패드(39b)를 형성하는 공정까지는 앞서 설명한 발광 다이오드 패키지(10) 제조방법(도 10 (a) 및 (b))과 동일하다.
- <88> 제1 전극 패드(39a) 및 제2 전극 패드(39b)가 형성된 후, 상기 제1 및 제2 전극 패드들(39a, 39b)을 덮는 절연층(49)이 형성된다. 절연층(49)은 제1 및 제2 전극 패드들(39a, 39b)의 측면을 덮어 이들을 보호할 수 있다. 상기 절연층(49)은 제1 및 제2 전극 패드들(39a, 39b)을 노출시키는 개구부를 갖는다. 이어서, 상기

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개구부들 내에 추가 금속층(55a, 55b)이 형성된다. 추가 금속층(55a, 55b)은 예컨대 본딩 메탈일 수 있다.

<89> 한편, 기판(51)이 상기 제1 전극 패드(39a) 및 제2 전극 패드(39b) 상에 본딩된다. 기판(51)은 관통홀들을 가질 수 있으며, 관통홀들 내에 제1 및 제2 범프들(53a, 53b)이 형성될 수 있다. 또한, 상기 제1 및 제2 범프의 끝 단부에 패드들(57a, 57b)가 형성될 수 있다. 상기 제1 및 제2 범프들(53a, 53b) 및 패드들(57a, 57b)을 갖는 기판(51)이 별도로 제작되어 제1 및 제2 전극 패드들(39a, 39b)을 갖는 웨이퍼 상에 본딩될 수 있다.

<90> 그 후, 도 12를 참조하여 설명한 바와 같이, 성장 기판(21)이 제거되고 파장 변환기(45)가 제1 도전형 반도체층(25)에 부착될 수 있으며, 이어서 개별 패키지로 분할될 수 있다. 이에 따라, 도 2에 도시된 발광 다이오드 패키지(20)가 완성된다.

【특허 청구범위】

【청구항 1】

제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 반도체 적층 구조체;

상기 제2 도전형 하부 반도체층 및 활성층을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들;

상기 반도체 적층 구조체 아래에 위치하고, 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 상부 반도체층에 전기적으로 접속된 제1 범프;

상기 반도체 적층 구조체 아래에 위치하고, 상기 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프; 및

상기 반도체 적층 구조체의 측면을 덮는 보호 절연층을 포함하는 발광 다이오드 패키지.

【청구항 2】

청구항 1에 있어서,

상기 제1 도전형 상부 반도체층 상에 위치하는 파장변환기를 더 포함하는 발광 다이오드 패키지.

【청구항 3】

청구항 2에 있어서,

상기 파장변환기는 형광제 시트 또는 불순물이 도핑된 단결정 기판인 발광

다이오드 패키지.

【청구항 4】

청구항 2에 있어서,

상기 파장변환기의 측면은 상기 보호절연층과 나란한 발광 다이오드 패키지.

【청구항 5】

청구항 1에 있어서,

상기 보호절연층은 분포브래그 반사기인 발광 다이오드 패키지.

【청구항 6】

청구항 1에 있어서,

상기 제1 도전형 상부 반도체층은 거칠어진 표면을 갖는 발광 다이오드 패키지.

【청구항 7】

청구항 1에 있어서,

상기 제1 및 제2 범프들의 측면을 덮는 절연층을 더 포함하는 발광 다이오드 패키지.

【청구항 8】

청구항 7에 있어서,

상기 제1 및 제2 범프들 사이에 위치하는 더미 범프를 더 포함하는 발광 다이오드 패키지.

【청구항 9】

청구항 1에 있어서,

관통홀들을 갖는 절연 기판을 더 포함하되,

상기 제1 및 제2 범프들은 상기 절연 기판의 관통홀에 형성된 발광 다이오드 패키지.

【청구항 10】

청구항 9에 있어서,

상기 절연 기판은 사파이어 또는 실리콘 기판인 발광 다이오드 패키지.

【청구항 11】

청구항 1에 있어서,

상기 제2 도전형 하부 반도체층에 접촉하는 제2 콘택층;

상기 복수개의 콘택홀들 내에서 상기 제1 도전형 상부 반도체층에 전기적으로 접촉하는 제1 접촉부들 및 상기 제1 접촉부들을 서로 연결하는 연결부를 포함하는 제1 콘택층;

상기 제1 콘택층과 상기 제2 콘택층 사이에 개재되어 상기 제2 콘택층을 덮는 제1 절연층; 및

상기 제1 콘택층 아래에서 상기 제1 콘택층을 덮는 제2 절연층을 더 포함하고,

상기 제1 범프는 상기 제2 절연층 아래에 위치하여 상기 제1 콘택층에 전기

적으로 접속되고,

상기 제2 범프는 상기 제2 절연층 아래에 위치하여 상기 제2 콘택층에 전기적으로 접속된 발광 다이오드 패키지.

【청구항 12】

청구항 11에 있어서,

상기 보호절연층은 상기 제1 절연층을 포함하는 발광 다이오드 패키지.

【청구항 13】

청구항 11에 있어서,

상기 보호절연층은 상기 제2 절연층을 포함하는 발광 다이오드 패키지.

【청구항 14】

청구항 11에 있어서,

상기 제2 절연층 아래에 위치하고, 상기 제2 절연층을 관통하여 상기 제1 콘택층에 접속하는 제1 전극 패드; 및

상기 제2 절연층 아래에 위치하고, 상기 제2 절연층 및 상기 제1 절연층을 관통하여 상기 제2 콘택층에 접속하는 제2 전극패드를 더 포함하고,

상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드 아래에서 이들에 전기적으로 접속된 발광 다이오드 패키지.

【청구항 15】

청구항 11에 있어서,

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상기 제1 절연층 및 제2 절연층 중 적어도 하나는 분포 브래그 반사기인 발광 다이오드 패키지.

【청구항 16】

회로 보드;

상기 회로 보드 상에 장착된 청구항 1 내지 15의 어느 한 항에 기재된 발광 다이오드 패키지; 및

상기 발광 다이오드 패키지에서 방출된 광의 지향각을 조절하기 위한 렌즈를 포함하는 발광 다이오드 모듈.

【청구항 17】

청구항 16에 있어서,

상기 회로보드는 MC-PCB이고,

상기 MC-PCB 상에 복수개의 상기 발광 다이오드 패키지들이 장착된 발광 다이오드 모듈.

【청구항 18】

성장 기판 상에 제1 도전형 반도체층, 활성층 및 제2 도전형 반도체층을 포함하는 반도체 적층 구조체를 형성하고,

상기 반도체 적층 구조체를 패터닝하여 칩 분리 영역을 형성함과 아울러, 상기 제2 도전형 반도체층 및 활성층을 패터닝하여 상기 제1 도전형 반도체층을 노출시키는 복수개의 콘택홀들을 형성하고,

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상기 칩 분리 영역 내의 반도체 적층 구조체의 측면을 덮는 보호 절연층을 형성하고,

상기 반도체 적층 구조체 상부에 제1 범프 및 제2 범프를 형성하는 것을 포함하되,

상기 제1 범프는 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 반도체층에 전기적으로 접속되고, 상기 제2 범프는 상기 제2 도전형 반도체층에 전기적으로 접속되는 발광 다이오드 패키지 제조 방법.

【청구항 19】

청구항 18에 있어서,

상기 성장 기판은 상기 활성층에서 생성된 광의 파장을 변환하기 위한 불순물을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 20】

청구항 18에 있어서,

상기 성장 기판을 제거하여 제1 도전형 반도체층을 노출시키고,

상기 노출된 제1 도전형 반도체층 상에 형광체 시트를 부착하는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 21】

청구항 18에 있어서,

상기 제2 도전형 반도체층 상에 제2 콘택층을 형성하고,

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상기 제2 콘택층 및 상기 복수개의 콘택홀의 측벽을 덮는 제1 절연층을 형성하되, 상기 제1 절연층은 상기 복수개의 콘택홀 내의 제1 도전형 반도체층을 노출시키는 개구부들을 갖고,

상기 제1 절연층 상에 제1 콘택층을 형성하되, 상기 제1 콘택층은 상기 복수개의 콘택홀 내에 노출된 제1 도전형 반도체층에 접촉하는 접촉부들 및 상기 접촉부들을 연결하는 연결부를 갖고,

상기 제1 콘택층을 덮는 제2 절연층을 형성하고,

상기 제1 및 제2 절연층을 패터닝하여 상기 제1 콘택층을 노출시키는 개구부를 형성함과 아울러, 상기 제2 콘택층을 노출시키는 개구부를 형성하고,

상기 제2 절연층 상에 상기 개구부들을 통해 상기 제1 콘택층에 접속하는 제1 전극 패드 및 제2 콘택층에 접속하는 제2 전극 패드를 형성하는 것을 더 포함하고,

상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드에 전기적으로 접속된 발광 다이오드 패키지 제조 방법.

【청구항 22】

청구항 21에 있어서,

상기 제1 범프 및 제2 범프를 형성하는 것은,

상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 개구부들을 갖는 절연층 패턴을 형성하고,

제출 일자 : 2010-09-24

상기 노출된 상기 제1 전극 패드 및 제2 전극 패드 상에 금속 재료를 도금하는 것을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 23】

청구항 22에 있어서,

상기 제1 범프 및 제2 범프를 형성하는 동안, 상기 제1 범프 및 제2 범프 사이에 더미 범프를 형성하는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 24】

청구항 21에 있어서,

상기 제1 범프 및 제2 범프를 형성하는 것은

절연 기판 내에 관통홀들을 형성하고,

상기 관통홀들을 금속재료로 채우고,

상기 금속재료를 갖는 절연 기판을 상기 제1 전극 패드 및 제2 전극 패드 상에 본딩하는 것을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 25】

청구항 24에 있어서,

상기 절연기판을 본딩하기 전에, 상기 제1 전극 패드 및 제2 전극 패드를 덮는 절연층을 형성하고,

상기 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

제출 일자 : 2010-09-24

【요약서】

【요약】

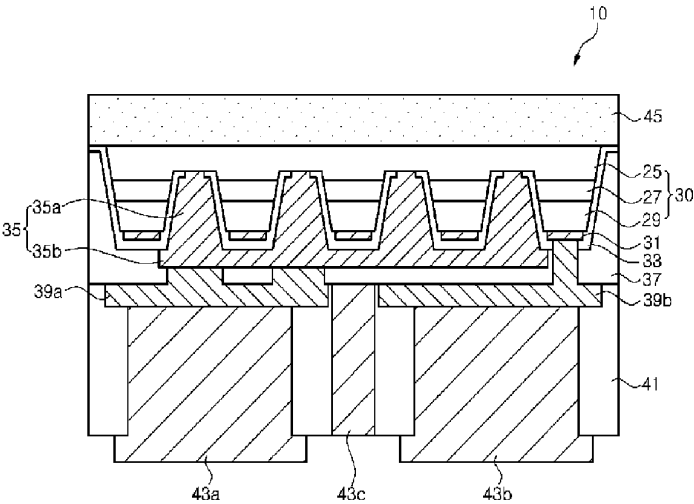
웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법이 개시된다. 이 발광 다이오드 패키지는, 제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 반도체 적층 구조체; 제2 도전형 하부 반도체층 및 활성층을 관통하여 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들; 반도체 적층 구조체 아래에 위치하고, 복수개의 콘택홀들에 노출된 제1 도전형 상부 반도체층에 전기적으로 접속된 제1 범프; 반도체 적층 구조체 아래에 위치하고, 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프; 및 반도체 적층 구조체의 측면을 덮는 보호 절연층을 포함한다.

【대표도】

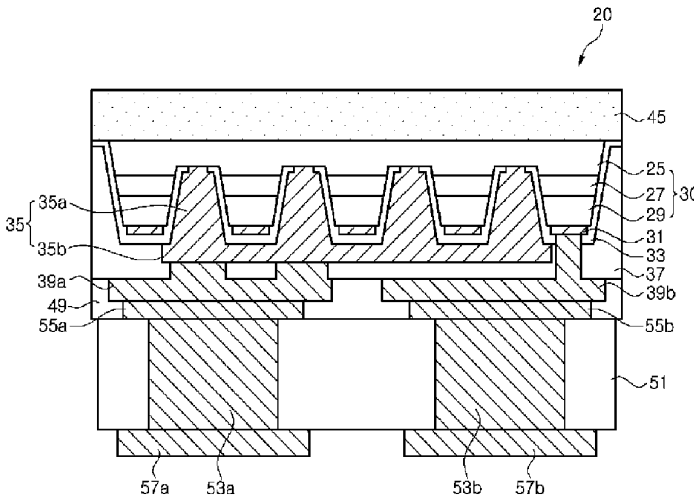
도 1

【도면】

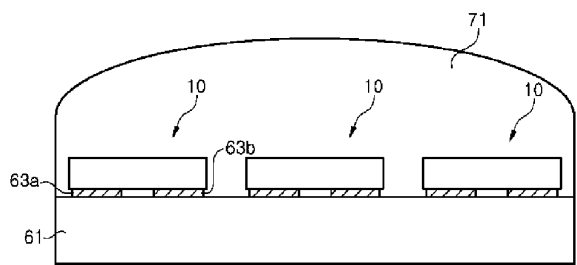
【도 1】



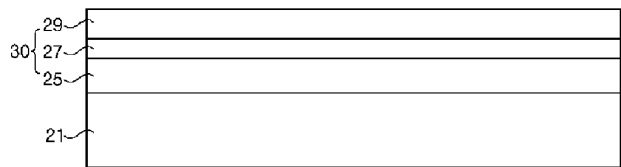
【도 2】



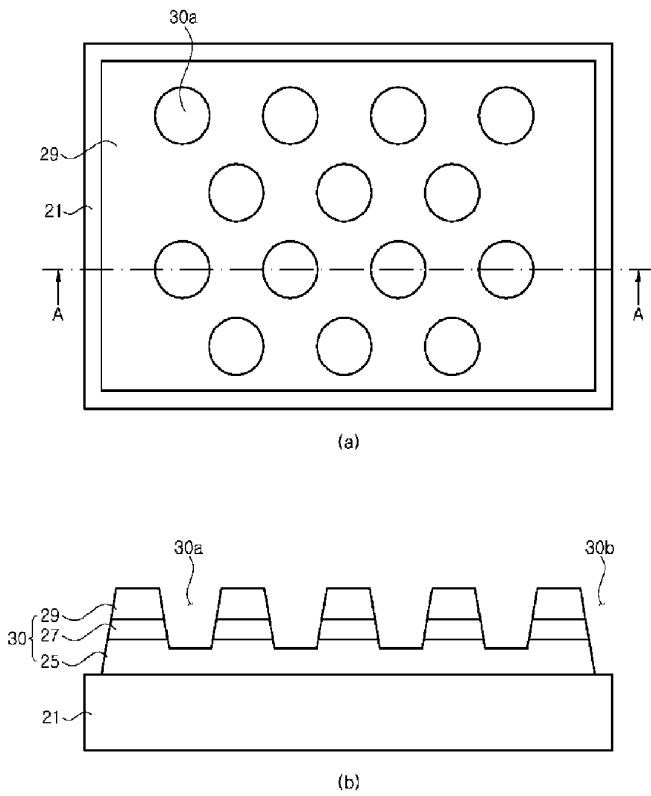
【도 3】



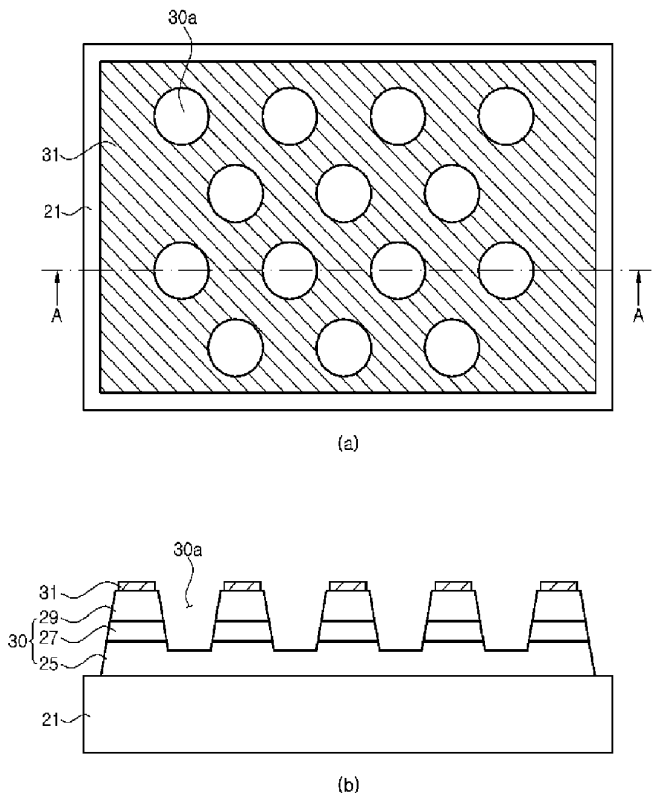
【도 4】



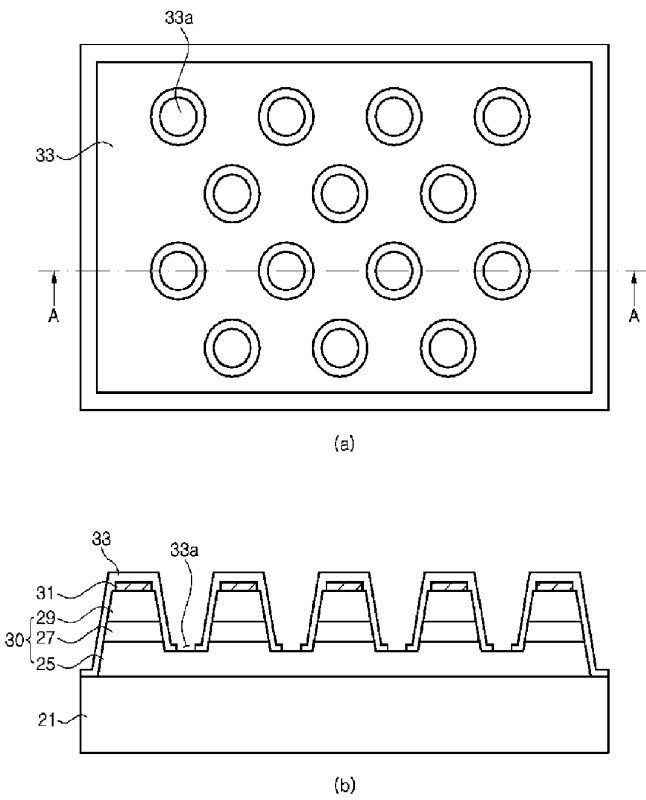
【도 5】



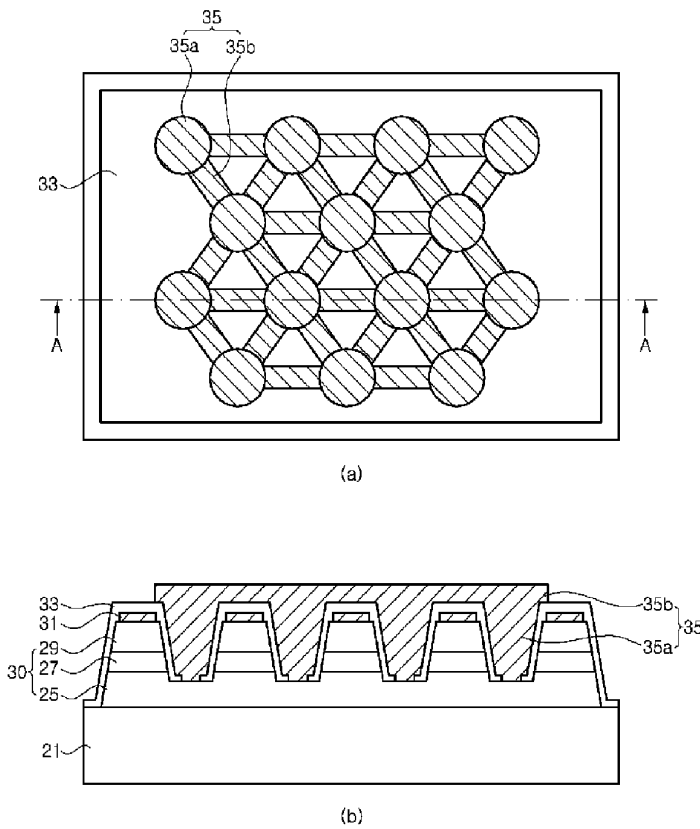
【도 6】



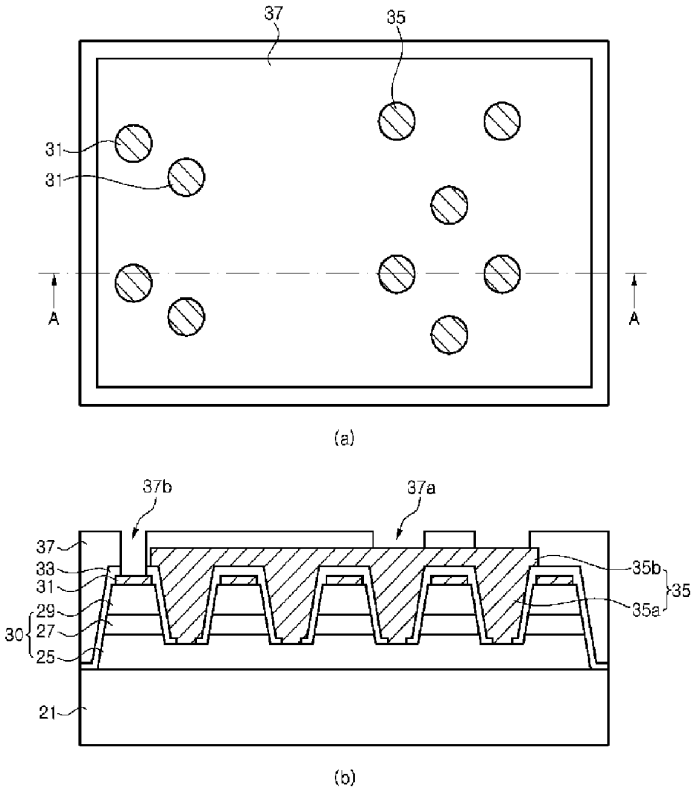
【도 7】



【도 8】

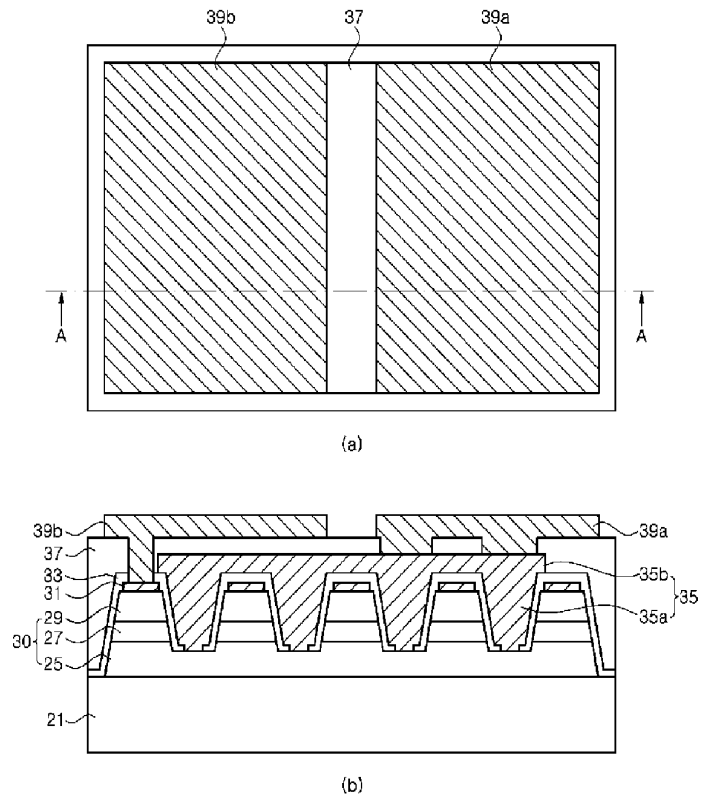


【도 9】

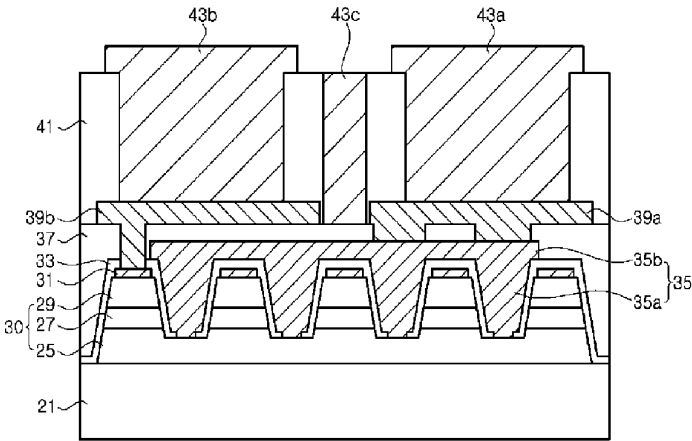


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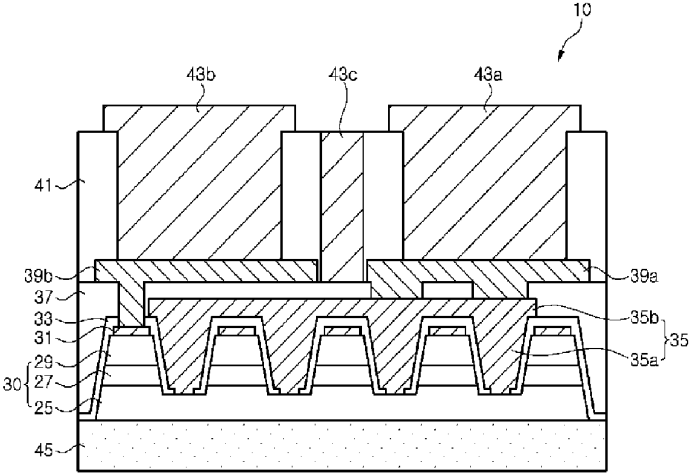
【도 10】



【도 11】



【도 12】





별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual
Property Office

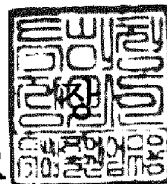
출 원 번 호 : 10-2010-0092808
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출 원 인 : 서울바이오시스 주식회사
Applicant(s) SEOUL VIOSYS CO., LTD.

2015년 08월 20일

특 허 청
COMMISSIONER



제출 일자 : 2010-09-24

【서지사항】

【서류명】	특허출원서
【참조번호】	0581
【출원구분】	특허출원
【출원인】	
【명칭】	서울옵토디바이스주식회사
【출원인코드】	1-2003-032642-0
【대리인】	
【명칭】	특허법인에이아이피
【대리인코드】	9-2009-100021-4
【지정된변리사】	이수완, 조진태, 윤종섭, 이성규, 이재웅
【포괄위임등록번호】	2009-036197-0
【발명의 국문명칭】	복수개의 발광셀들을 갖는 웨이퍼 레벨 발광 다이오드 패키 지 및 그것을 제조하는 방법
【발명의 영문명칭】	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE HAVING PLURALITY OF LIGHT EMITTING CELLS AND METHOD OF FABRICATING THE SAME
【발명자】	
【성명】	서원철
【성명의 영문표기】	SE0, Won Cheol
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【우편번호】	425-851
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【성명】	갈대성

제출 일자 : 2010-09-24

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【국적】 KR
【심사청구】 청구
【취지】 위와 같이 특허청장에게 제출합니다.

대리인 특허법인에이아이피 (서명 또는 인)

【수수료】

【출원료】 0 면 38,000 원
【가산출원료】 45 면 0 원
【우선권주장료】 0 건 0 원
【심사청구료】 28 항 1,250,000 원
【합계】 1,288,000 원
【감면사유】 중기업
【감면후 수수료】 386,400 원

【첨부서류】 1. 중소기업기본법 제2조의 규정에 따른 중기업에 해당함을
증명하는 서류_1통

【명세서】

【발명의 명칭】

복수개의 발광셀들을 갖는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법{WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE HAVING PLURALITY OF LIGHT EMITTING CELLS AND METHOD OF FABRICATING THE SAME}

【기술분야】

<1> 본 발명은 발광 다이오드 패키지 및 그것을 제조하는 방법에 관한 것으로, 더욱 상세하게는 복수개의 발광셀들을 갖는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법에 관한 것이다.

【배경기술】

<2> 발광 다이오드는 N형 반도체와 P형 반도체를 가지는 반도체 소자로서, 전자와 정공의 재결합에 의하여 빛을 발산한다. 이러한 발광 다이오드는 표시소자, 교통 신호기 및 백라이트로 널리 이용되고 있다. 또한, 발광 다이오드는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길어, 백열전구 및 형광등을 대체하여 일반 조명 용도로 그 사용 영역을 넓히고 있다.

<3> 최근, 발광 다이오드를 교류전원에 직접 연결하여 연속적으로 빛을 방출하는 교류용 발광 다이오드가 제품화되고 있다. 고전압 교류전원에 직접 연결하여 사용할 수 있는 발광 다이오드는, 예를 들어, 국제공개번호 WO 2004/023568(A1)호에 "발광 성분들을 갖는 발광소자"(LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING

ELEMENTS)라는 제목으로 사카이 등(SAKAI et. al.)에 의해 개시되어 있다.

<4> 상기 WO 2004/023568(A1)호에 따르면, LED들이 사파이어 기판과 같은 절연성 기판 상에 2차원적으로 연결된 직렬 LED 어레이들이 형성된다. LED 어레이들이 직렬 연결됨으로써 고전압에서 구동될 수 있는 발광 다이오드가 제공될 수 있다. 또한, 이러한 LED 어레이들이 상기 사파이어 기판 상에서 역병렬로 연결되어, AC 파워 서플라이에 의해 구동될 수 있는 단일칩 발광소자가 제공된다.

<5> 상기 AC-LED는 성장 기판으로 사용된 기판, 예컨대 사파이어 기판 상에 발광 셀들을 형성하므로, 발광셀들의 구조에 제한이 따르며, 광추출 효율을 향상시키는 데 한계가 있다. 이러한 문제점을 해결하기 위해 기판 분리 공정을 적용하여 직렬 연결된 발광셀들을 갖는 발광 다이오드, 예컨대 AC-LED를 제조하는 방법이 연구되고 있다.

<6> 한편, 발광 다이오드는 통상 최종적으로 발광 다이오드 모듈로서 사용된다. 발광 다이오드 모듈은 웨이퍼 레벨에서의 발광 다이오드 칩 제작 공정, 패키징 공정 및 모듈 공정을 거쳐 제작된다. 즉, 사파이어 기판과 같은 성장 기판 상에서 반도체층들을 성장시킨 후 웨이퍼 레벨에서 패터닝 공정 등을 거쳐 전극 패드들을 갖는 칩으로 제조되고, 개별 칩들로 분할된다(칩 제작 공정). 그 후, 개별 칩들을 리드 프레임 또는 인쇄회로기 기판 등에 실장하고, 본딩 와이어를 이용하여 전극 패드들을 리드 단자들에 전기적으로 연결한 후, 몰딩 부재로 발광 다이오드 칩들을 몰딩함으로써 발광 다이오드 패키지가 제작된다(패키징 공정). 그 후, 상기 발광 다이오드 패키지를 MC-PCB와 같은 회로보드 상에 장착함으로써 광원 모듈과 같은

발광 다이오드 모듈이 완성된다(모듈 공정).

<7> 상기 패키징 공정에 의해 상기 발광 다이오드 칩은 하우징 및/또는 몰딩부재에 의해 외부 환경으로부터 보호된다. 나아가, 상기 몰딩 부재 내에 형광체를 함유 시킴으로써, 백색 광원에 적합한 백색 발광 다이오드 패키지가 제공될 수 있다. 이러한 백색 발광 다이오드 패키지를 MC-PCB와 같은 회로보드 상에 장착하고 발광 다이오드 패키지에서 방출된 광의 지향 특성을 조절하기 위한 2차 렌즈를 발광 다이오드 패키지 상에 설치함으로써 특정 사용 용도에 적합한 백색 발광 다이오드 모듈이 제공될 수 있다.

<8> 그러나, 종래의 리드 프레임 또는 인쇄회로기판 등을 사용하는 발광 다이오드 패키지는 소형화가 어려울 뿐만 아니라, 방열 특성을 개선하는데 한계가 있다. 더욱이, 리드 프레임 또는 인쇄회로기판 등에 의한 광 흡수, 리드 단자에 의한 저항열 발생 등에 의해 발광 다이오드의 발광 효율이 감소되는 것은 잘 알려져 있다.

<9> 나아가, 칩 제작 공정, 패키징 공정 및 모듈화 공정이 각각 별도로 진행됨에 따라 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비용이 증가한다.

【선행기술문헌】

【특허문헌】

<10> (특허문헌 0001) 특허문헌 1: 국제공개번호 WO 2004/023568(A1)호

【발명의 내용】

【해결하려는 과제】

- <11> 본 발명이 해결하려는 과제는, 종래의 리드 프레임이나 인쇄회로기판 등을 이용할 필요없이 직접 회로보드에 모듈화할 수 있는 복수개의 발광셀들을 갖는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법을 제공하는 것이다.
- <12> 본 발명이 해결하려는 다른 과제는, 고효율 및 고방열 특성을 갖는 발광 다이오드 패키지 및 그것을 제조하는 방법을 제공하는 것이다.
- <13> 본 발명이 해결하려는 또 다른 과제는, 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비용을 절감할 수 있는 발광 다이오드 패키지 제조 방법을 제공하는 것이다.
- <14> 본 발명이 해결하려는 또 다른 과제는, 고효율 및 고방열 특성을 갖는 발광 다이오드 모듈 및 그것을 제조하는 방법을 제공하는 것이다.

【과제의 해결 수단】

- <15> 본 발명의 일 태양에 따른 발광 다이오드 패키지는, 각각 제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 복수개의 발광셀들; 상기 각 발광셀의 상기 제2 도전형 하부 반도체층 및 활성층을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들; 상기 각 발광셀의 측면을 덮는 보호 절연층; 상기 발광셀들 아래에 위치하고, 인접한 두개의 발광셀들을 전기적으로 직렬 연결하는 연결부; 상기 발광셀들 아래에 위치하고, 상기 발광셀들 중 제1 발광셀의 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 상부 반도체층에

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전기적으로 접속된 제1 범프; 및 상기 복수개의 발광셀들 아래에 위치하고, 상기 발광셀들 중 제2 발광셀의 상기 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프를 포함한다.

<16> 상기 보호 절연층은 상기 발광셀들의 측벽 전면을 덮어 외부 환경, 예컨대 수분 등으로부터 상기 발광셀들을 보호한다. 나아가, 상기 제1 범프 및 제2 범프는 서로 동일 높이를 갖고, 이들의 단면은 동일 평면 상에 위치할 수 있다. 상기 발광 다이오드 패키지는 상기 제1 범프 및 제2 범프를 통해 MC-PCB 등의 회로보드 상에 전기적으로 접속될 수 있다.

<17> 본 발명에 따른 발광 다이오드 패키지는 MC-PCB 등의 회로보드에 직접 장착하여 모듈화할 수 있는 웨이퍼 레벨 패키지로서, 리드프레임이나 인쇄회로기판 등을 사용하는 종래의 발광 다이오드 패키지와 구별되며, 또한, 리드프레임이나 인쇄회로기판 등을 이용하여 패키징되는 통상의 발광 다이오드 칩과 구별된다.

<18> 한편, 파장 변환기가 상기 복수개의 발광셀들 상에 위치할 수 있다. 파장 변환기는 보호절연층과 다른 재료로 구성되어 보호절연층과 구별된다. 상기 파장변환기는 형광체 시트 또는 불순물이 도핑된 단결정 기판일 수 있다. 상기 파장변환기의 측면은 상기 보호절연층과 나란할 수 있다. 즉, 상기 파장변환기는 상기 보호절연층의 윗면을 덮는다.

<19> 상기 보호절연층은 실리콘 산화막 또는 실리콘 질화막을 포함할 수 있으며, 단일층 또는 다중층으로 형성될 수 있다. 이와 달리, 상기 보호절연층은 굴절률이 서로 다른 절연층들을 반복 적층한 분포브래그 반사기를 포함할 수 있다.

- <20> 한편, 상기 각 발광셀의 제1 도전형 상부 반도체층은 거칠어진 표면을 가질 수 있다. 거칠어진 표면은 광 추출 효율을 향상시킨다.
- <21> 몇몇 실시예들에 있어서, 상기 제1 및 제2 범프들의 측면은 절연층에 의해 덮일 수 있다. 이 절연층은 상기 제1 및 제2 범프들의 측면의 적어도 일부를 덮는다. 또한, 더미 범프가 상기 제1 및 제2 범프들 사이에 위치할 수 있다. 더미 범프는 반도체 적층 구조체에서 생성된 열을 방출한다.
- <22> 몇몇 실시예들에 있어서, 상기 발광 다이오드 패키지는 관통홀들을 갖는 절연 기판을 더 포함할 수 있으며, 상기 제1 및 제2 범프들은 상기 절연 기판의 관통홀에 형성될 수 있다. 상기 절연 기판은 사파이어 또는 실리콘 기판일 수 있다.
- <23> 또한, 상기 절연 기판은 그 하부면에 부분적으로 형성된 홈들을 갖고, 상기 홈들은 금속물질로 채워질 수 있다. 상기 금속물질에 의해 상기 기판의 방열 특성이 개선된다.
- <24> 한편, 상기 발광 다이오드 패키지는, 상기 각 발광셀의 상기 제2 도전형 하부 반도체층에 접촉하는 제2 콘택층; 상기 복수개의 콘택홀들 내에서 상기 각 발광셀의 상기 제1 도전형 상부 반도체층에 전기적으로 접촉하는 제1 접촉부들 및 상기 제1 접촉부들을 서로 연결하는 연결부를 포함하는 제1 콘택층; 상기 제1 콘택층과 상기 제2 콘택층 사이에 개재되어 상기 제2 콘택층을 덮는 제1 절연층; 및 상기 제1 콘택층 아래에서 상기 제1 콘택층을 덮는 제2 절연층을 더 포함할 수 있다. 상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제2 절연층 바로 아래에 위치하여

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상기 제1 콘택층과 제2 콘택층을 연결할 수 있다. 또한, 상기 제1 범프는 상기 제2 절연층 아래에 위치하여 상기 제1 발광셀의 상기 제1 콘택층에 전기적으로 접속되고, 상기 제2 범프는 상기 제2 절연층 아래에 위치하여 상기 제2 발광셀의 상기 제2 콘택층에 전기적으로 접속될 수 있다.

<25> 상기 보호절연층은 상기 제1 절연층 및/또는 제2 절연층에 의해 형성될 수 있다. 따라서, 상기 보호절연층은 상기 제1 절연층 및/또는 상기 제2 절연층을 포함할 수 있다.

<26> 나아가, 상기 발광 다이오드 패키지는, 상기 제2 절연층 아래에 위치하고, 상기 제2 절연층을 관통하여 상기 제1 발광셀의 제1 콘택층에 접속하는 제1 전극패드; 및 상기 제2 절연층 아래에 위치하고, 상기 제2 절연층 및 상기 제1 절연층을 관통하여 상기 제2 발광셀의 상기 제2 콘택층에 접속하는 제2 전극패드를 더 포함할 수 있다. 상기 제1 범프 및 제2 범프는 각각 상기 제1 전극패드 및 제2 전극패드 아래에서 이들에 전기적으로 접속될 수 있다.

<27> 한편, 상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제1 및 제2 전극패드와 동일 레벨에 위치할 수 있다. 즉, 상기 연결부는 상기 제1 및 제2 전극패드와 동일 공정에서 형성될 수 있다.

<28> 또한, 상기 인접한 발광셀들을 직렬 연결하는 연결부와 상기 더미 범프 사이에 제3 절연층이 개재될 수 있다. 제3 절연층은 제1 전극패드 및 제2 전극패드의 측면을 덮을 수 있다.

<29> 또한, 상기 제1 절연층 및 제2 절연층 중 적어도 하나는 분포 브래그 반사기 일 수 있다.

<30> 본 발명의 또 다른 태양에 따르면, 앞서 설명한 발광 다이오드 패키지를 포함하는 발광 다이오드 모듈이 제공된다. 이 모듈은 회로 보드; 상기 회로보드에 장착된 상기 발광 다이오드 패키지 및 상기 발광 다이오드 패키지에서 방출된 광의 지향각을 조절하기 위한 렌즈를 포함할 수 있다. 나아가, 상기 회로보드는 MC-PCB일 수 있으며, 상기 MC-PCB 상에 복수개의 상기 발광 다이오드 패키지들이 장착될 수 있다.

<31> 본 발명의 또 다른 태양에 따르면, 복수개의 발광셀들을 갖는 발광 다이오드 패키지 제조방법이 제공된다. 이 방법은, 성장 기판 상에 제1 도전형 반도체층, 활성층 및 제2 도전형 반도체층을 포함하는 반도체 적층 구조체를 형성하고; 상기 반도체 적층 구조체를 패터닝하여 칩 분리 영역 및 발광셀 분리 영역을 형성함과 아울러, 상기 제2 도전형 반도체층 및 활성층을 패터닝하여 상기 제1 도전형 반도체층을 노출시키는 복수개의 콘택홀들을 갖는 복수개의 발광셀들을 형성하고; 상기 칩 분리 영역 및 발광셀 분리 영역 내의 반도체 적층 구조체의 측면을 덮는 보호 절연층을 형성하고; 인접한 발광셀들을 직렬 연결하는 연결부를 형성하고; 상기 복수개의 발광셀들 상부에 제1 범프 및 제2 범프를 형성하는 것을 포함한다. 여기서, 상기 제1 범프는 상기 발광셀들 중 제1 발광셀의 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 반도체층에 전기적으로 접속되고, 상기 제2 범프는 상기 발광셀들 중 제2 발광셀의 상기 제2 도전형 반도체층에 전기적으로 접속된다.

<32> 몇몇 실시예들에 있어서, 상기 성장 기판은 상기 활성층에서 생성된 광의 파장을 변환하기 위한 불순물을 포함할 수 있다. 상기 성장 기판은 사파이어 또는 실리콘 기판일 수 있다.

<33> 몇몇 실시예들에 있어서, 상기 방법은, 상기 성장 기판을 제거하여 상기 발광셀들을 노출시키고, 상기 노출된 발광셀들 상에 형광체 시트를 부착하는 것을 더 포함할 수 있다. 상기 보호 절연층은 칩 분리 영역을 따라 개별 패키지로 분할하는 공정에서 상기 형광체 시트와 함께 분할될 수 있다.

<34> 상기 방법은 또한, 상기 각 발광셀의 제2 도전형 반도체층 상에 제2 콘택층을 형성하고; 상기 각 발광셀의 상기 제2 콘택층 및 상기 복수개의 콘택홀의 측벽을 덮는 제1 절연층을 형성하되, 상기 제1 절연층은 상기 복수개의 콘택홀 내의 제1 도전형 반도체층을 노출시키는 개구부들을 갖고; 상기 각 발광셀의 상기 제1 절연층 상에 제1 콘택층을 형성하되, 상기 제1 콘택층은 상기 복수개의 콘택홀 내에 노출된 제1 도전형 반도체층에 접촉하는 접촉부들 및 상기 접촉부들을 연결하는 연결부를 갖고; 상기 각 발광셀의 상기 제1 콘택층을 덮는 제2 절연층을 형성하고; 상기 제1 및 제2 절연층을 패터닝하여 상기 각 발광셀의 상기 제1 콘택층을 노출시키는 개구부를 형성함과 아울러, 상기 제2 콘택층을 노출시키는 개구부를 형성하고; 상기 제2 절연층 상에 상기 개구부들을 통해 상기 제1 발광셀의 상기 제1 콘택층에 접속하는 제1 전극 패드 및 상기 제2 발광셀의 상기 제2 콘택층에 접속하는 제2 전극 패드를 형성하는 것을 더 포함할 수 있다. 상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제2 절연층 상에 형성됨과 아울러 상기 개구부들을

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통해 인접한 발광셀들의 제1 콘택층 및 제2 콘택층에 접속할 수 있다. 또한, 상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드에 전기적으로 접속될 수 있다.

<35> 몇몇 실시예들에 있어서, 상기 제1 범프 및 제2 범프를 형성하는 것은, 상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 개구부들을 갖는 절연층 패턴을 형성하고; 상기 노출된 상기 제1 전극 패드 및 제2 전극 패드 상에 금속 재료를 도금하는 것을 포함할 수 있다. 나아가, 상기 제1 범프 및 제2 범프를 형성하는 동안, 더미 범프를 형성하는 것을 더 포함할 수 있다.

<36> 또한, 상기 더미 범프를 형성하기 전에, 상기 제1 전극 패드, 제2 전극 패드 및 상기 인접한 발광셀들을 연결하는 연결부를 덮는 제3 절연층이 형성될 수 있다. 그 후, 상기 제3 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출시킬 수 있다.

<37> 또 다른 실시예들에 있어서, 상기 제1 범프 및 제2 범프를 형성하는 것은, 절연 기판 내에 관통홀들을 형성하고; 상기 관통홀들을 금속재료로 채우고; 상기 금속재료를 갖는 절연 기판을 상기 제1 전극 패드 및 제2 전극 패드 상에 본딩하는 것을 포함할 수 있다.

<38> 또한, 상기 절연기판을 본딩하기 전에, 상기 제1 전극 패드, 제2 전극 패드 및 상기 인접한 발광셀들을 직렬 연결하는 연결부를 덮는 제3 절연층이 형성될 수 있다. 그 후, 상기 제3 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출시킬 수 있다.

【발명의 효과】

<39> 본 발명에 따르면, 종래의 리드 프레임이나 인쇄회로기판 등을 이용할 필요 없이 직접 회로보드에 모듈화할 수 있는 웨이퍼 레벨(또는 칩 레벨) 발광 다이오드 패키지가 제공될 수 있다. 이에 따라, 고효율 및 고방열 특성을 갖는 발광 다이오드 패키지가 제공되며, 발광 다이오드 모듈을 제작하는데 필요한 작업 시간 및 비용을 절감할 수 있다. 또한, 상기 발광 다이오드 패키지를 장착함으로써, 고효율 및 고방열 특성을 갖는 발광 다이오드 모듈이 제공될 수 있다.

<40> 더욱이, 상기 발광 다이오드 패키지는 직렬 연결된 복수개의 발광셀들을 가지며, 나아가 역병렬 연결된 어레이들을 가질 수 있다. 또한, 상기 복수개의 발광셀들은 브리지 정류기에 연결되어 사용될 수도 있으며, 발광셀들을 이용하여 브리지 정류기를 구현할 수도 있다. 이에 따라, 상기 발광 다이오드 패키지를 장착한 발광 다이오드 모듈은 별도의 AC-DC 컨버터 없이 교류 전원하에서 구동될 수 있다.

【도면의 간단한 설명】

<41> 도 1은 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 설명하기 위한 개략적인 단면도이다.

도 2는 본 발명의 다른 실시예에 따른 발광 다이오드 모듈 패키지를 설명하기 위한 개략적인 단면도이다.

도 3은 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 장착한 발광 다이오드 모듈을 설명하기 위한 단면도이다.

도 4 내지 도 13은 본 발명의 일 실시예에 따른 발광 다이오드 패키지를 제조하는 방법을 설명하기 위한 도면들이다. 도 5 내지 도 10에서 (a)는 평면도를 나타내고, (b)는 (a)의 절취선 A-A를 따라 취해진 단면도를 나타낸다.

도 14는 본 발명의 다른 실시예에 따른 발광 다이오드 패키지를 제조하는 방법을 설명하기 위한 단면도이다.

【발명을 실시하기 위한 구체적인 내용】

<42> 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서, 구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<43> 도 1은 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)를 설명하기 위한 단면도이다.

<44> 도 1을 참조하면, 상기 발광 다이오드 패키지(10)는 복수개의 발광셀들(2개만 도시함, S1, S2)로 분리된 반도체 적층 구조체(30), 제1 콘택층(35), 제2 콘택층(31), 제1 절연층(33), 제2 절연층(37), 제1 전극 패드(39a), 제2 전극 패드(39b), 인접한 발광셀들을 직렬 연결하는 연결부(39c), 제1 범프(45a) 및 제2 범프(45b)를 포함한다. 또한, 상기 발광 다이오드 패키지(10)는 제3 절연층(41), 절연

층(43), 더미 범프(45c), 파장 변환기(51) 및 추가 금속층(40a, 40b)을 포함할 수 있다.

<45> 상기 반도체 적층 구조체(30)는 제1 도전형의 상부 반도체층(25), 활성층(27) 및 제2 도전형의 하부 반도체층(29)을 포함한다. 상기 활성층(27)은 상기 상부 및 하부 반도체층들(25, 29) 사이에 개재된다.

<46> 상기 활성층(27), 상기 상부 및 하부 반도체층들(25, 29)은 III-N 계열의 화합물 반도체, 예컨대 (Al, Ga, In)N 반도체로 형성될 수 있다. 상기 상부 및 하부 반도체층들(25, 29)은 각각 단일층 또는 다중층일 수 있다. 예를 들어, 상기 상부 및/또는 하부 반도체층(25, 29)은 콘택층과 클래드층을 포함할 수 있으며, 또한 초격자층을 포함할 수 있다. 상기 활성층(27)은 단일 양자우물 구조 또는 다중 양자우물 구조일 수 있다. 바람직하게, 상기 제1 도전형은 n형이고, 상기 제2 도전형은 p형이다. 저항이 상대적으로 작은 n형 반도체층으로 상부 반도체층(25)을 형성할 수 있어, 상부 반도체층(25)의 두께를 상대적으로 두껍게 형성할 수 있다. 따라서, 상기 상부 반도체층(25)의 상부면에 거칠어진 면(R)을 형성하는 것이 용이하며, 거칠어진 면(R)은 활성층(27)에서 발생된 광의 추출 효율을 향상시킨다.

<47> 상기 각 발광셀(S1, S2)은 상기 제2 도전형 하부 반도체층(29) 및 활성층(27)을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들(도 5(b), 30a 참조)을 가지며, 제1 콘택층(35)이 상기 복수개의 콘택홀들에 노출된 제1 도전형 상부 반도체층(25)에 접촉한다. 상기 각 발광셀(S1, S2)은 또한 셀 분리 영역(도 5(b)의 30b 참조)에 의해 서로 분리된다.

<48> 한편, 제2 콘택층(31)은 상기 각 발광셀(S1, S2)의 상기 제2 도전형 하부 반도체층(29)에 접촉한다. 제2 콘택층(31)은 반사 금속층을 포함하며, 활성층(25)에서 생성된 광을 반사시킨다. 또한, 상기 제2 콘택층(31)은 제2 도전형 하부 반도체층(29)에 오믹 콘택할 수 있다.

<49> 제1 절연층(33)은 제2 콘택층(31)을 덮는다. 또한, 상기 제1 절연층(33)은 복수개의 콘택홀들(30a)에 노출된 반도체 적층 구조체(30)의 측벽을 덮는다. 나아가, 상기 제1 절연층(33)은 발광셀들(S1, S2)의 측면을 덮을 수 있다. 제1 절연층(33)은 제1 콘택층(35)을 제2 콘택층(31)으로부터 절연시키며, 나아가, 복수개의 콘택홀들(30a) 내에 노출된 제2 도전형 하부 반도체층(29)과 활성층(27)을 제1 콘택층(35)으로부터 절연시킨다. 제1 절연층(33)은 실리콘 산화막 또는 실리콘 질화막의 단일층으로 형성될 수 있으나, 이에 한정되는 것은 아니며 다중층으로 형성될 수 있다. 더욱이, 상기 제1 절연층(33)은 굴절률이 서로 다른 절연층들, 예컨대 SiO₂/TiO₂ 또는 SiO₂/Nb₂O₅를 반복하여 적층한 분포 브래그 반사기일 수 있다.

<50> 상기 제1 콘택층(35)은 상기 제1 절연층(33) 아래에 위치하며, 상기 각 발광셀(S1, S2)의 상기 복수개의 콘택홀들(30a) 내에서 상기 제1 절연층(33)을 관통하여 제1 도전형 상부 반도체층(25)에 접촉한다. 제1 콘택층(35)은 제1 도전형 상부 반도체층(25)에 접촉하는 접촉부들(35a) 및 접촉부들(35a)을 서로 연결하는 연결부(35b)를 포함한다. 따라서, 연결부(35b)에 의해 접촉부들(35a)이 서로 전기적으로 연결된다. 각 발광셀(S1, S2) 아래에 위치하는 제1 콘택층들(35)은 서로 이격되어 위치하며, 각 발광셀(S1, S2)에 접촉하는 상기 제1 콘택층(35)은 제1 절연층(33)의

일부 영역 아래에 형성된다. 제1 콘택층(35)은 반사 금속층으로 형성될 수 있다.

<51> 상기 제2 절연층(37)은 제1 콘택층(35) 아래에서 제1 콘택층(35)을 덮는다. 나아가, 상기 제2 절연층(37)은 제1 절연층(33)을 덮으며, 각 발광셀(S1, S2)의 측면을 덮을 수 있다. 상기 제2 절연층(37)은 단일층 또는 다중층으로 형성될 수 있으며, 분포 브래그 반사기일 수 있다.

<52> 상기 제1 전극 패드(39a) 및 제2 전극 패드(39b)는 상기 제2 절연층(37) 아래에 위치한다. 제1 전극 패드(39a)는 제2 절연층(37)을 관통하여 제1 발광셀(S1)의 제1 콘택층(35)에 접속될 수 있다. 또한, 제2 전극 패드(39b)는 제2 절연층(39) 및 제1 절연층(33)을 관통하여 제2 발광셀(S2)의 제1 콘택층(31)에 접속될 수 있다.

<53> 한편, 연결부(39c)가 상기 제2 절연층(37) 아래에 위치하며, 제2 절연층(37)을 관통하여 인접한 두개의 발광셀들(S1, S2)을 전기적으로 연결한다. 상기 연결부(39c)는 하나의 발광셀(S1)의 제2 콘택층(31)과 그것에 인접한 발광셀(S2)의 제1 콘택층(35)에 접속할 수 있으며, 이에 따라 두개의 발광셀들(S1, S2)이 직렬 연결된다.

<54> 본 실시예에 있어서, 두 개의 발광셀들(S1, S2)만이 도시되어 있지만, 더 많은 수의 발광셀들이 복수의 연결부들(39c)에 의해 서로 직렬 연결될 수 있으며, 제1 및 제2 전극 패드들(39a, 39b)은 이러한 직렬 어레이의 양끝에 위치하는 발광셀들(S1, S2)에 각각 전기적으로 연결될 수 있다.

<55> 한편, 제3 절연층(41)이 제1 전극 패드(39a), 제2 전극 패드(39b) 및 연결부(39c) 아래에서 이들을 덮을 수 있다. 상기 제3 절연층(41)은 제1 전극 패드(39a) 및 제2 전극 패드(39b)를 노출시키는 개구부를 가질 수 있다. 제3 절연층(41)은 실리콘 산화막 또는 실리콘 질화막으로 형성될 수 있다.

<56> 제1 범프(45a) 및 제2 범프(45b)는 각각 상기 제1 및 제2 전극 패드(39a, 39b) 아래에 위치한다. 제1 범프(45a) 및 제2 범프(45b)는 도금 기술에 의해 형성될 수 있다. 제1 및 제2 범프(45a, 45b)는 MC-PCB와 같은 회로보드에 전기적으로 접속하는 단자들로서, 그 끝 단면들이 동일면에 나란할 수 있다. 나아가, 제1 전극 패드(39a)와 제2 전극 패드(39b)가 동일 레벨에 형성될 수 있으며, 따라서, 제1 범프(45a)와 제2 범프(45b) 또한 동일면 상에 형성될 수 있다. 이에 따라, 제1 및 제2 범프(45a, 45b)는 동일한 높이를 가질 수 있다.

<57> 상기 제1 범프(45a) 및 상기 제2 범프(45b)와 제1 전극 패드(39a, 39b) 사이에 추가 금속층(40a, 40b)이 개재될 수 있다. 여기서, 상기 추가 금속층(40a, 40b)은 제1 및 제2 전극 패드들(39a, 39b)을 연결부(39c)에 비해 더 높게 형성하기 위한 것으로, 제3 절연층(41)의 개구부들 내에 형성될 수 있다. 상기 제1 및 제2 전극 패드(39a, 39b)와 상기 추가 금속층(40a, 40b)이 최종 전극 패드들을 구성할 수 있다.

<58> 한편, 상기 제1 범프(45a)와 제2 범프(45b) 사이에 더미 범프(45c)가 위치할 수 있다. 더미 범프(45c)는 제1 및 제2 범프(45a, 45b)를 형성하는 동안 함께 형성될 수 있으며, 제1 및 제2 범프(45a, 45b)와 함께 발광셀들(S1, S2)에서 생성된 열

을 방출하기 위한 열 경로를 제공할 수 있다. 상기 더미 범프(45c)는 제3 절연층(41)에 의해 연결부(39c)로부터 이격된다.

<59> 한편, 절연층(43)은 제1 범프(45a) 및 제2 범프(45b)의 측면을 덮을 수 있다. 절연층(43)은 또한 더미 범프(45c)의 측면을 덮을 수 있다. 나아가, 상기 절연층(43)은 제1 범프(45a), 제2 범프(45b) 및 더미 범프(45c) 사이의 영역을 채워 외부로부터 반도체 적층 구조체(30)로 수분이 침투하는 것을 방지한다. 절연층(43)은 제1 및 제2 범프(45a, 45b)의 측면 전체를 덮을 수 있으나, 이에 한정되는 것은 아니며, 제1 및 제2 범프(45a, 45b)의 끝 단면 근처의 일부 측면을 제외하고 나머지 측면을 덮을 수 있다.

<60> 한편, 상기 발광셀들(S1, S2) 상에 파장 변환기(51)가 위치한다. 파장 변환기(51)는 제1 도전형 상부 반도체층(25)의 상부면에 접촉할 수 있다. 파장 변환기(51)는 또한 셀 분리 영역(30b) 및 칩 분리 영역을 덮는다. 파장 변환기(45)는 균일한 두께를 갖는 형광체 시트일 수 있으나, 이에 한정되는 것은 아니며, 파장 변환을 위한 불순물이 도핑된 기판, 예컨대 사파이어 또는 실리콘 기판일 수 있다.

<61> 본 실시예에 있어서, 발광셀들(S1, S2)의 측면은 보호 절연층으로 덮인다. 상기 보호 절연층은 예컨대, 상기 제1 절연층(33) 및/또는 제2 절연층(37)을 포함할 수 있다. 나아가, 제1 콘택층(35)은 상기 제2 절연층(37)으로 덮여 외부 환경으로부터 보호되며, 제2 콘택층(31)은 제1 절연층(33) 및 제2 절연층(37)으로 덮여 외부 환경으로부터 보호될 수 있다. 또한, 제1 전극 패드(39a) 및 제2 전극 패드(39b)는 예컨대 제3 절연층(41)에 의해 보호된다. 이에 따라, 외부 환경으로부터

수분 등에 의해 발광셀들(S1, S2)가 열화되는 것을 방지할 수 있다.

<62> 한편, 상기 파장 변환기(51)는 웨이퍼 레벨에서 제1 도전형 상부 반도체층(25) 상에 부착될 수 있으며, 그 후 칩 분리 공정(혹은 패키지 분리 공정)에서 보호절연층과 함께 분할될 수 있다. 따라서, 상기 파장 변환기(51)의 측면은 보호절연층과 나란할 수 있다. 또한, 상기 파장 변환기(51)의 측면은 제3 절연층(41) 및 절연층(43)의 측면과도 나란할 수 있다.

<63> 도 2는 본 발명의 또 다른 실시예에 따른 발광 다이오드 패키지(20)를 설명하기 위한 개략적인 단면도이다.

<64> 도 2를 참조하면, 상기 발광 다이오드 패키지(20)는 앞서 설명한 발광 다이오드 패키지(10)와 대체로 동일하나, 제1 및 제2 범프들(65a, 65b)이 기판(61) 내에 형성된 것에 차이가 있다.

<65> 즉, 기판(61)은 관통홀들을 포함하며, 제1 및 제2 범프들(65a, 65b)이 각각 관통홀 내에 형성된다. 상기 기판(61)은 절연 기판으로서, 사파이어 또는 실리콘 기판일 수 있으나, 이에 한정되는 것은 아니다. 또한, 상기 절연 기판(61)은 그 하부면에 부분적으로 형성된 홈들을 갖고, 상기 홈들은 금속물질(65c)로 채워질 수 있다. 상기 금속물질(65c)에 의해 상기 기판의 방열 특성이 개선된다.

<66> 상기 제1 및 제2 범프들(65a, 65b)과 함께 기판(61)이 제3 절연층(41) 상에 부착될 수 있으며, 제1 및 제2 범프들(65a, 65b)이 각각 제1 전극 패드(39a) 및 제2 전극 패드(39b)에 접속될 수 있다. 여기서, 상기 추가 금속층(40a, 40b)에 상기

제1 및 제2 범프들(65a, 65b)이 본딩될 수 있다.

<67> 도 3은 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)들을 회로보드 상에 장착한 발광 다이오드 모듈을 설명하기 위한 단면도이다.

<68> 도 3을 참조하면, 상기 발광 다이오드 모듈은 회로보드(61), 예컨대 MC-PCB, 발광 다이오드 패키지(10) 및 렌즈(71)를 포함한다. 상기 회로보드(61), 예컨대 MC-PCB는 발광 다이오드 패키지(10)를 장착하기 위한 접속 패드들(63a, 63b)을 갖는다. 상기 접속 패드들(63a, 63b) 상에 각각 발광 다이오드 패키지(10)의 제1 및 제2 범프들(도 1의 45a, 45b)이 접속된다.

<69> 상기 회로보드(61) 상에 복수개의 발광 다이오드 패키지들(10)이 장착될 수 있으며, 렌즈(71)가 상기 발광 다이오드 패키지들(10)의 지향각 등의 광 특성을 조절하도록 발광 다이오드 패키지들(10) 상에 설치된다.

<70> 또 다른 실시예에서, 상기 발광 다이오드 패키지들(10) 대신에 발광 다이오드 패키지들(20)이 장착될 수 있다.

<71> 도 4 내지 도 12는 본 발명의 일 실시예에 따른 발광 다이오드 패키지(10)를 제조하는 방법을 설명하기 위한 도면들이다. 도 5 내지 도 10에서 (a)는 평면도를 나타내고, (b)는 (a)의 절취선 A-A를 따라 취해진 단면도를 나타낸다.

<72> 도 4를 참조하면, 성장 기판(21) 상에 제1 도전형 반도체층(25), 활성층(27) 및 제2 도전형 반도체층(29)을 포함하는 반도체 적층 구조체(30)가 형성된다. 성장 기판(21)은 사파이어 기판일 수 있으나, 이에 한정되는 것은 아니며, 다른 이종기

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판, 예컨대 실리콘 기판일 수 있다. 상기 제1 및 제2 도전형 반도체층들(25, 29)은 각각 단일층 또는 다중층으로 형성될 수 있다. 또한, 상기 활성층(27)은 단일 양자 우물 구조 또는 다중 양자우물 구조로 형성될 수 있다.

<73> 상기 화합물 반도체층들은 III-N 계열의 화합물 반도체로 형성될 수 있으며, 금속유기화학기상증착법(MOCVD) 또는 분자선 증착법(molecular beam epitaxy; MBE) 등의 공정에 의해 성장 기판(21) 상에 성장될 수 있다.

<74> 한편, 화합물 반도체층들을 형성하기 전, 버퍼층(미도시됨)이 형성될 수 있다. 버퍼층은 희생 기판(21)과 화합물 반도체층들의 격자 부정합을 완화하기 위해 채택되며, 질화갈륨 또는 질화알루미늄 등의 질화갈륨 계열의 물질층일 수 있다.

<75> 도 5 (a) 및 (b)를 참조하면, 상기 반도체 적층 구조체(30)를 패터닝하여 칩 (패키지) 분리 영역(30c) 및 셀 분리 영역(30b)을 형성함과 아울러, 상기 제2 도전형 반도체층(29) 및 활성층(27)을 패터닝하여 상기 제1 도전형 반도체층(25)을 노출시키는 복수개의 콘택홀들(30a)을 갖는 발광셀들(S1, S2)을 형성한다. 상기 반도체 적층 구조체(30)는 사진 및 식각 공정을 사용하여 패터닝될 수 있다.

<76> 칩 분리 영역(30c)은 나중에 개별 발광 다이오드 패키지로 분할하는 영역으로, 칩 분리 영역(30c)에 제1 도전형 반도체층(25), 활성층(27) 및 제2 도전형 반도체층(29)의 측면이 노출된다. 상기 칩 분리 영역(30c) 및 셀 분리 영역(30b)은 바람직하게 기판(21)면을 노출시키도록 형성될 수 있으며, 반드시 이에 한정되는 것은 아니다.

<77> 한편, 상기 복수개의 콘택홀들(30a)은 원형일 수 있으나, 이에 한정되는 것은 아니며 다양한 형상을 가질 수 있다. 상기 제2 도전형 반도체층(29) 및 활성층(27)이 복수개의 콘택홀들(30a)의 측벽에 노출된다. 상기 콘택홀들(30a)의 측벽은 도식한 바와 같이 경사지게 형성될 수 있다.

<78> 도 6 (a) 및 (b)를 참조하면, 제2 도전형 반도체층(29) 상에 제2 콘택층(31)이 형성된다. 제2 콘택층(31)은 복수개의 콘택홀들(30a)을 제외한 반도체 적층 구조체(30) 상에 형성되며, 각 발광셀(S1, S2) 상에 형성된다.

<79> 제2 콘택층(31)은 예컨대 ITO와 같은 투명 도전성 산화막 또는 은(Ag) 또는 알루미늄(Al)과 같은 반사 금속층을 포함할 수 있으며, 단일층 또는 다중층으로 형성될 수 있다. 제2 콘택층(31)은 또한 제2 도전형 반도체층(29)에 오믹 접촉하도록 형성된다.

<80> 제2 콘택층(31)은 복수개의 콘택홀들(30a)을 형성한 후에 형성될 수 있으나, 이에 한정되는 것은 아니며, 복수개의 콘택홀들(30a)을 형성하기 전에 미리 형성될 수도 있다.

<81> 도 7 (a) 및 (b)를 참조하면, 제2 콘택층(31)을 덮는 제1 절연층(33)이 형성된다. 제1 절연층(33)은 각 발광셀(S1, S2)의 측면을 덮을 수 있으며, 또한, 복수개의 콘택홀들(30a)의 측벽을 덮을 수 있다. 다만, 상기 제1 절연층(33)은 복수개의 콘택홀들(30a) 내에서 상기 제1 도전형 반도체층(25)을 노출시키는 개구부들(33a)을 갖는다.

<82> 제1 절연층(33)은 실리콘 산화막 또는 실리콘 질화막과 같은 절연물질의 단일층 또는 다중층으로 형성될 수 있다. 나아가, 상기 제1 절연층(33)은 굴절률이 서로 다른 절연층을 반복 적층한 분포 브래그 반사기로 형성될 수 있다. 예컨대, 상기 제1 절연층(33)은 $\text{SiO}_2/\text{TiO}_2$ 또는 $\text{SiO}_2/\text{Nb}_2\text{O}_5$ 를 반복 적층하여 형성할 수 있다. 또한, 상기 제1 절연층(33)을 형성하는 각 절연층의 두께를 조절함으로써 청색광, 녹색광 및 적색광의 넓은 파장 범위에 걸쳐 반사율이 높은 분포 브래그 반사기가 형성될 수 있다.

<83> 도 8 (a) 및 (b)를 참조하면, 상기 제1 절연층(33) 상에 제1 콘택층(35)이 형성된다. 제1 콘택층(35)은 각 발광셀(S1, S2) 상에 형성되며, 콘택홀들(30a) 내에 노출된 제1 도전형 반도체층(25)에 접촉하는 접촉부들(35a) 및 접촉부들(35a)을 서로 연결하는 연결부(35b)를 포함한다. 제1 콘택층(35)은 반사 금속층으로 형성될 수 있으나, 이에 한정되는 것은 아니다.

<84> 제1 콘택층(35)은 각 발광셀(S1, S2)의 일부 영역 상에 형성되며, 제1 콘택층(35)이 형성된 영역 이외의 영역에는 제1 절연층(33)이 노출된다.

<85> 도 9 (a) 및 (b)를 참조하면, 상기 제1 콘택층(35) 상에 제2 절연층(37)이 형성된다. 제2 절연층(37)은 실리콘 산화막 또는 실리콘 질화막 등의 단일층 또는 다중층으로 형성될 수 있으며, 또한 굴절률이 서로 다른 절연층을 반복 적층한 분포 브래그 반사기로 형성될 수 있다.

<86> 제2 절연층(37)은 제1 콘택층(35)을 덮으며 또한 제1 절연층(33)을 덮을 수

있다. 제2 절연층(37)은 또한 각 발광셀(S1, S2)의 측면을 덮을 수 있다. 나아가, 상기 제2 절연층(37)은 칩 분리 영역(30c) 및 셀 분리 영역(30b)을 채울 수 있다.

<87> 한편, 상기 제2 절연층(37)은 각 발광셀(S1, S2)의 제1 콘택층(35)을 노출시키는 개구부(37a)를 갖는다. 또한, 상기 제2 절연층(37) 및 제1 절연층(33)에 제2 콘택층(31)을 노출시키는 개구부(37b)가 형성된다.

<88> 도 10 (a) 및 (b)를 참조하면, 상기 제2 절연층(37) 상에 제1 및 제2 전극 패드들(39a, 39b)과 함께 연결부(39c)가 형성된다. 제1 전극 패드(39a)는 개구부(37a)를 통해 제1 발광셀(S1)의 제1 콘택층(35)에 접속되고, 제2 전극 패드(39b)는 개구부(37b)를 통해 제2 발광셀(S2)의 제2 콘택층(31)에 접속된다. 또한, 상기 연결부(39c)는 개구부들(37a, 37b)을 통해 인접한 발광셀들(S1, S2)의 제1 콘택층(35)과 제2 콘택층(31)을 직접 연결한다.

<89> 도 11을 참조하면, 상기 제1 및 제2 전극 패드(39a, 39b)와 연결부(39c) 상에 제3 절연층(41)이 형성된다. 제3 절연층(41)은 제1 및 제2 전극 패드(39a, 39b)와 연결부(39c)를 덮으며, 이들 전극 패드들(39a, 39b)의 상부면을 노출시키는 홈들을 갖는다. 한편, 상기 제3 절연층(41)의 홈 내에 추가 금속층(40a, 40b)이 형성될 수 있다. 추가 금속층(40a, 40b)은 전극 패드들(39a, 39b)의 높이를 증가시켜 연결부(39c)에 비해 상대적으로 높은 최종 전극 패드를 형성할 수 있다. 상기 추가 금속층(40a, 40b)은 제3 절연층(41)을 형성하기 전에 형성될 수도 있다. 상기 추가 금속층(40a, 40b)의 상부면은 상기 제3 절연층(41)의 상부면과 실질적으로 동일할 수 있다.

- <90> 도 12를 참조하면, 상기 제3 절연층(41) 상에 절연층(43) 패턴이 형성된다. 절연층(43) 패턴은 제1 및 제2 전극 패드(39a, 39b)의 상부, 예컨대 추가 금속층들(40a, 40b)을 노출시키는 홈을 갖는다. 또한, 상기 제1 전극 패드(39a)와 제2 전극 패드(39b) 사이에서 제3 절연층(41)을 노출시키는 홈을 가질 수 있다.
- <91> 이어서, 상기 절연층(43) 내의 홈들에 제1 및 제2 범프(45a, 45b)가 형성되고 또한, 제1 범프와 제2 범프 사이에 더미 범프(45c)가 형성될 수 있다.
- <92> 상기 범프들은 도금, 예컨대 전기 도금을 사용하여 형성될 수 있다. 필요한 경우, 도금을 위한 시드층이 형성될 수도 있다.
- <93> 한편, 상기 제1 및 제2 범프(45a, 45b)가 형성된 후, 상기 절연층(43)은 제거될 수도 있다. 예를 들어, 상기 절연층(43)은 포토레지스트와 같은 폴리머로 형성될 수 있으며, 범프들이 완성된 후 제거될 수 있다. 이와 달리, 상기 절연층(43)은 제1 범프 및 제2 범프(45a, 45b)의 측면을 보호하기 위해 남겨질 수도 있다.
- <94> 도 13을 참조하면, 상기 성장 기관(21)이 제거되고 파장 변환기(51)가 발광 셀들(S1, S2)에 부착된다. 성장 기관(21)은 레이저 리프트 오프(Laser lift-off; LLO)와 같은 광학적 기술 또는 기계적 연마 또는 화학적 에칭 기술을 이용하여 제거될 수 있다.
- <95> 그 후, 노출된 제1 도전형 반도체층(25)의 표면에 PEC 에칭 등에 의한 이방성 에칭에 의해 거칠어진 면이 형성될 수 있다.
- <96> 한편, 형광체를 함유하는 형광체 시트 등의 파장 변환기(51)가 상기 제1 도

전형 반도체층(25)에 부착될 수 있다.

<97> 이와 달리, 상기 성장 기판(21)은 활성층(27)에서 생성된 광의 파장을 변환하기 위한 불순물을 함유할 수 있으며, 이 경우, 상기 성장 기판(21)이 파장 변환기(51)로 사용될 수 있다.

<98> 그 후, 칩 분리 영역(30c)을 따라 개별 패키지로 분할함으로써 발광 다이오드 패키지(10)가 완성된다. 이때, 상기 파장 변환기(51)와 함께 제2 절연층(37)이 함께 절단됨으로써 절단면이 서로 나란하게 형성될 수 있다.

<99> 도 14는 본 발명의 또 다른 실시예에 따른 발광 다이오드 패키지(20)를 제조하기 위한 방법을 설명하기 위한 단면도이다.

<100> 도 14를 참조하면, 본 실시예에 따른 발광 다이오드 패키지(20) 제조 방법은 제3 절연층(41) 및 추가 금속층들(40a, 40b)을 형성하는 공정까지는 앞서 설명한 발광 다이오드 패키지(10) 제조방법(도 11)과 동일하다.

<101> 한편, 절연 기판(61)이 제3 절연층(41) 상에 본딩된다. 기판(61)은 관통홀들을 가질 수 있으며, 관통홀들 내에 제1 및 제2 범프들(65a, 65b)이 형성될 수 있다. 또한, 상기 제1 및 제2 범프의 끝 단부에 패드들(도시하지 않음)이 형성될 수 있다. 나아가, 상기 절연 기판(61)은 그 하부면에 부분적으로 형성된 홈들을 갖고, 상기 홈들은 금속물질(65c)로 채워질 수 있다. 상기 금속물질(65c)에 의해 상기 기판(61)의 방열 특성이 개선된다.

<102> 상기 제1 및 제2 범프들(65a, 65b)을 갖는 기판(61)이 별도로 제작되어 제1

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및 제2 전극 패드들(39a, 39b)을 갖는 웨이퍼 상에 본딩될 수 있다. 상기 제1 및 제2 범프들(65a, 65b)은 각각 제1 및 제2 전극 패드들(39a, 39b)에 전기적으로 연결된다.

<103> 그 후, 도 13을 참조하여 설명한 바와 같이, 성장 기판(21)이 제거되고 파장 변환기(51)가 발광셀들(S1, S2)에 부착될 수 있으며, 이어서 개별 패키지로 분할될 수 있다. 이에 따라, 도 2에 도시된 발광 다이오드 패키지(20)가 완성된다.

【특허 청구범위】

【청구항 1】

각각 제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 복수개의 발광셀들;

상기 각 발광셀의 상기 제2 도전형 하부 반도체층 및 활성층을 관통하여 상기 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들;

상기 각 발광셀의 측벽을 덮는 보호 절연층;

상기 발광셀들 아래에 위치하고, 인접한 두개의 발광셀들을 전기적으로 직렬 연결하는 연결부;

상기 발광셀들 아래에 위치하고, 상기 발광셀들 중 제1 발광셀의 상기 복수개의 콘택홀들에 노출된 상기 제1 도전형 상부 반도체층에 전기적으로 접속된 제1 범프; 및

상기 복수개의 발광셀들 아래에 위치하고, 상기 발광셀들 중 제2 발광셀의 상기 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프를 포함하는 발광 다이오드 패키지.

【청구항 2】

청구항 1에 있어서,

상기 복수의 발광셀들 상에 위치하는 과장변환기를 더 포함하는 발광 다이오드 패키지.

【청구항 3】

청구항 2에 있어서,

상기 과장변환기는 형광체 시트 또는 불순물이 도핑된 단결정 기관인 발광 다이오드 패키지.

【청구항 4】

청구항 2에 있어서,

상기 과장변환기의 측면은 상기 보호절연층과 나란한 발광 다이오드 패키지.

【청구항 5】

청구항 1에 있어서,

상기 보호절연층은 분포브래그 반사기를 포함하는 발광 다이오드 패키지.

【청구항 6】

청구항 1에 있어서,

상기 각 발광셀의 제1 도전형 상부 반도체층은 거칠어진 표면을 갖는 발광 다이오드 패키지.

【청구항 7】

청구항 1에 있어서,

상기 제1 및 제2 범프들의 측면을 덮는 절연층을 더 포함하는 발광 다이오드 패키지.

【청구항 8】

청구항 7에 있어서,

상기 제1 및 제2 범프들 사이에 위치하는 더미 범프를 더 포함하는 발광 다이오드 패키지.

【청구항 9】

청구항 1에 있어서,

관통홀들을 갖는 절연 기판을 더 포함하되,

상기 제1 및 제2 범프들은 상기 절연 기판의 관통홀에 형성된 발광 다이오드 패키지.

【청구항 10】

청구항 9에 있어서,

상기 절연 기판은 그 하부면에 부분적으로 형성된 홈들을 갖고, 상기 홈들은 금속물질로 채워진 발광 다이오드 패키지.

【청구항 11】

청구항 1에 있어서,

상기 각 발광셀의 상기 제2 도전형 하부 반도체층에 접촉하는 제2 콘택층;

상기 복수개의 콘택홀들 내에서 상기 각 발광셀의 상기 제1 도전형 상부 반도체층에 전기적으로 접촉하는 제1 접촉부들 및 상기 제1 접촉부들을 서로 연결하는 연결부를 포함하는 제1 콘택층;

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상기 제1 콘택층과 상기 제2 콘택층 사이에 개재되어 상기 제2 콘택층을 덮는 제1 절연층; 및

상기 제1 콘택층 아래에서 상기 제1 콘택층을 덮는 제2 절연층을 더 포함하고,

상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제2 절연층 바로 아래에 위치하여 상기 제1 콘택층과 제2 콘택층을 연결하고,

상기 제1 범프는 상기 제2 절연층 아래에 위치하여 상기 제1 발광셀의 상기 제1 콘택층에 전기적으로 접속되고,

상기 제2 범프는 상기 제2 절연층 아래에 위치하여 상기 제2 발광셀의 상기 제2 콘택층에 전기적으로 접속된 발광 다이오드 패키지.

【청구항 12】

청구항 11에 있어서,

상기 보호절연층은 상기 제1 절연층을 포함하는 발광 다이오드 패키지.

【청구항 13】

청구항 11에 있어서,

상기 보호절연층은 상기 제2 절연층을 포함하는 발광 다이오드 패키지.

【청구항 14】

청구항 11에 있어서,

상기 제2 절연층 아래에 위치하고, 상기 제2 절연층을 관통하여 상기 제1 발

광셀의 제1 콘택층에 접속하는 제1 전극 패드; 및

상기 제2 절연층 아래에 위치하고, 상기 제2 절연층 및 상기 제1 절연층을 관통하여 상기 제2 발광셀의 상기 제2 콘택층에 접속하는 제2 전극패드를 더 포함하고,

상기 제1 범프 및 제2 범프는 각각 상기 제1 전극 패드 및 제2 전극 패드 아래에서 이들에 전기적으로 접속된 발광 다이오드 패키지.

【청구항 15】

청구항 14에 있어서,

상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제1 및 제2 전극 패드와 동일 레벨에 위치하는 발광 다이오드 패키지.

【청구항 16】

청구항 14에 있어서,

상기 인접한 발광셀들을 직렬 연결하는 연결부와 상기 더미 범프 사이에 개재된 제3 절연층을 더 포함하는 발광 다이오드 패키지.

【청구항 17】

청구항 11에 있어서,

상기 제1 절연층 및 제2 절연층 중 적어도 하나는 분포 브래그 반사기인 발광 다이오드 패키지.

【청구항 18】

회로 보드;

상기 회로 보드 상에 장착된 청구항 1 내지 17의 어느 한 항에 기재된 발광 다이오드 패키지; 및

상기 발광 다이오드 패키지에서 방출된 광의 지향각을 조절하기 위한 렌즈를 포함하는 발광 다이오드 모듈.

【청구항 19】

청구항 18에 있어서,

상기 회로보드는 MC-PCB이고,

상기 MC-PCB 상에 복수개의 상기 발광 다이오드 패키지들이 장착된 발광 다이오드 모듈.

【청구항 20】

성장 기판 상에 제1 도전형 반도체층, 활성층 및 제2 도전형 반도체층을 포함하는 반도체 적층 구조체를 형성하고,

상기 반도체 적층 구조체를 패터닝하여 칩 분리 영역 및 발광셀 분리 영역을 형성함과 아울러, 상기 제2 도전형 반도체층 및 활성층을 패터닝하여 상기 제1 도전형 반도체층을 노출시키는 복수개의 콘택홀들을 갖는 복수개의 발광셀들을 형성하고,

상기 칩 분리 영역 및 발광셀 분리 영역 내의 반도체 적층 구조체의 측면을

덮는 보호 절연층을 형성하고,

인접한 발광셀들을 직렬 연결하는 연결부를 형성하고,

상기 복수개의 발광셀들 상부에 제1 범프 및 제2 범프를 형성하는 것을 포함
하되,

상기 제1 범프는 상기 발광셀들 중 제1 발광셀의 상기 복수개의 콘택홀들에
노출된 상기 제1 도전형 반도체층에 전기적으로 접속되고, 상기 제2 범프는 상기
발광셀들 중 제2 발광셀의 상기 제2 도전형 반도체층에 전기적으로 접속되는 발광
다이오드 패키지 제조 방법.

【청구항 21】

청구항 20에 있어서,

상기 성장 기판은 상기 활성층에서 생성된 광의 파장을 변환하기 위한 불순
물을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 22】

청구항 20에 있어서,

상기 성장 기판을 제거하여 상기 발광셀들을 노출시키고,

상기 노출된 발광셀들 상에 형광체 시트를 부착하는 것을 더 포함하는 발광
다이오드 패키지 제조 방법.

【청구항 23】

청구항 20에 있어서,

제출 일자 : 2010-09-24

상기 각 발광셀의 제2 도전형 반도체층 상에 제2 콘택층을 형성하고,

상기 각 발광셀의 상기 제2 콘택층 및 상기 복수개의 콘택홀의 측벽을 덮는 제1 절연층을 형성하되, 상기 제1 절연층은 상기 복수개의 콘택홀 내의 제1 도전형 반도체층을 노출시키는 개구부들을 갖고,

상기 각 발광셀의 상기 제1 절연층 상에 제1 콘택층을 형성하되, 상기 제1 콘택층은 상기 복수개의 콘택홀 내에 노출된 제1 도전형 반도체층에 접촉하는 접촉 부들 및 상기 접촉부들을 연결하는 연결부를 갖고,

상기 각 발광셀의 상기 제1 콘택층을 덮는 제2 절연층을 형성하고,

상기 제1 및 제2 절연층을 패터닝하여 상기 각 발광셀의 상기 제1 콘택층을 노출시키는 개구부를 형성함과 아울러, 상기 제2 콘택층을 노출시키는 개구부를 형성하고,

상기 제2 절연층 상에 상기 개구부들을 통해 상기 제1 발광셀의 상기 제1 콘택층에 접속하는 제1 전극 패드 및 상기 제2 발광셀의 상기 제2 콘택층에 접속하는 제2 전극 패드를 형성하는 것을 더 포함하고,

상기 인접한 발광셀들을 직렬 연결하는 연결부는 상기 제2 절연층 상에 형성됨과 아울러 상기 개구부들을 통해 인접한 발광셀들의 제1 콘택층 및 제2 콘택층에 접속하고,

상기 제1 뱀프 및 제2 뱀프는 각각 상기 제1 전극 패드 및 제2 전극 패드에 전기적으로 접속된 발광 다이오드 패키지 제조 방법.

【청구항 24】

청구항 23에 있어서,

상기 제1 범프 및 제2 범프를 형성하는 것은,

상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 개구부들을 갖는 절연층 패턴을 형성하고,

상기 노출된 상기 제1 전극 패드 및 제2 전극 패드 상에 금속 재료를 도금하는 것을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 25】

청구항 24에 있어서,

상기 제1 범프 및 제2 범프를 형성하는 동안, 더미 범프를 형성하는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 26】

청구항 25에 있어서,

상기 더미 범프를 형성하기 전에, 상기 제1 전극 패드, 제2 전극 패드 및 상기 인접한 발광셀들을 연결하는 연결부를 덮는 제3 절연층을 형성하고,

상기 제3 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출시키는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 27】

청구항 23에 있어서,

제출 일자 : 2010-09-24

상기 제1 범프 및 제2 범프를 형성하는 것은
절연 기판 내에 관통홀들을 형성하고,
상기 관통홀들을 금속재료로 채우고,
상기 금속재료를 갖는 절연 기판을 상기 제1 전극 패드 및 제2 전극 패드 상
에 본딩하는 것을 포함하는 발광 다이오드 패키지 제조 방법.

【청구항 28】

청구항 27에 있어서,
상기 절연기판을 본딩하기 전에, 상기 제1 전극 패드, 제2 전극 패드 및 상
기 인접한 발광셀들을 직렬 연결하는 연결부를 덮는 제3 절연층을 형성하고,
상기 제3 절연층을 패터닝하여 상기 제1 전극 패드 및 제2 전극 패드를 노출
시키는 것을 더 포함하는 발광 다이오드 패키지 제조 방법.

【요약서】

【요약】

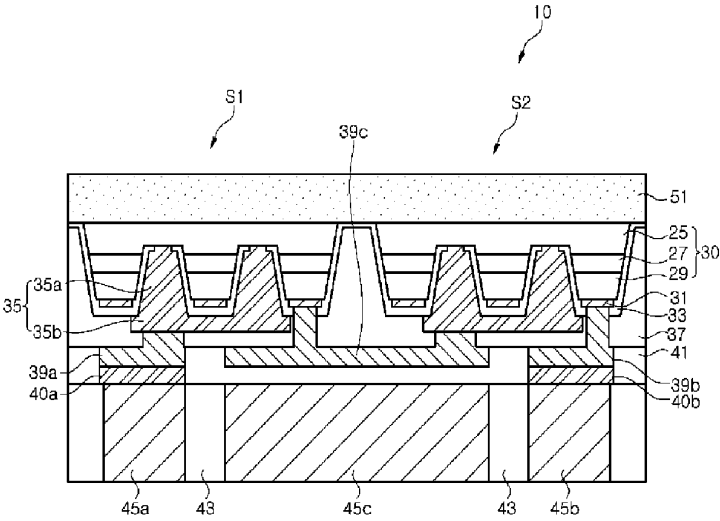
복수개의 발광셀들을 갖는 웨이퍼 레벨 발광 다이오드 패키지 및 그것을 제조하는 방법이 개시된다. 이 발광 다이오드 패키지는, 각각 제1 도전형 상부 반도체층, 활성층 및 제2 도전형 하부 반도체층을 포함하는 복수개의 발광셀들; 각 발광셀의 제2 도전형 하부 반도체층 및 활성층을 관통하여 제1 도전형 상부 반도체층을 노출시키는 복수개의 콘택홀들; 각 발광셀의 측벽을 덮는 보호 절연층; 발광셀들 아래에 위치하고, 인접한 두개의 발광셀들을 전기적으로 직렬 연결하는 연결부; 발광셀들 아래에 위치하고, 발광셀들 중 제1 발광셀의 복수개의 콘택홀들에 노출된 제1 도전형 상부 반도체층에 전기적으로 접속된 제1 범프; 및 복수개의 발광셀들 아래에 위치하고, 발광셀들 중 제2 발광셀의 상기 제2 도전형 하부 반도체층에 전기적으로 접속된 제2 범프를 포함한다.

【대표도】

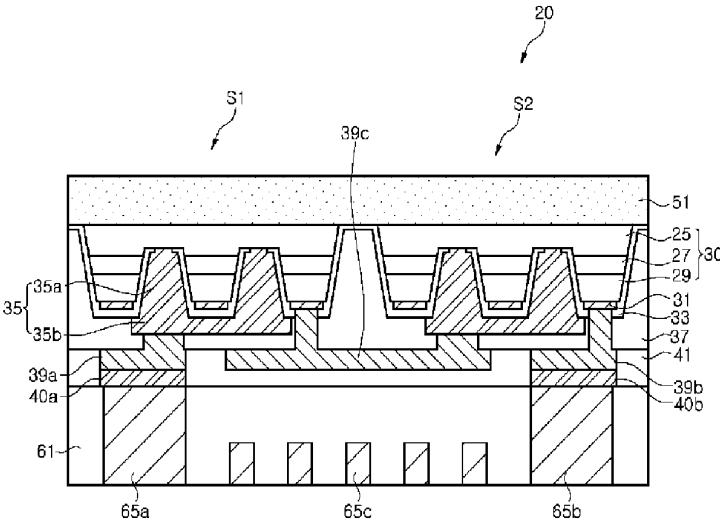
도 1

【도면】

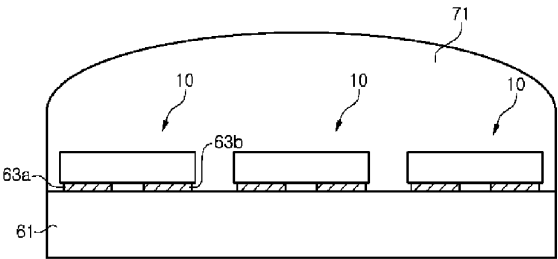
【도 1】



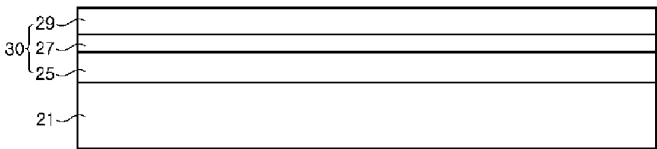
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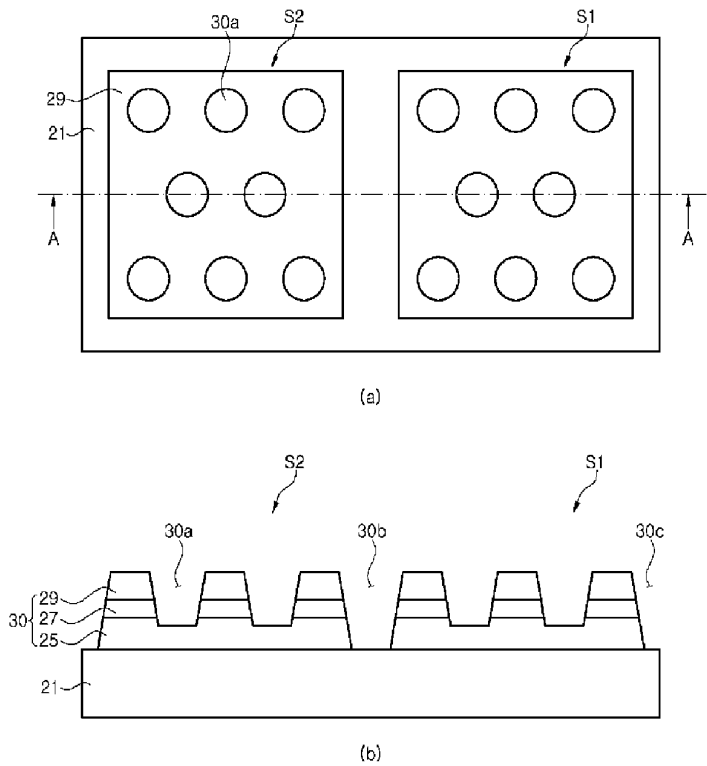
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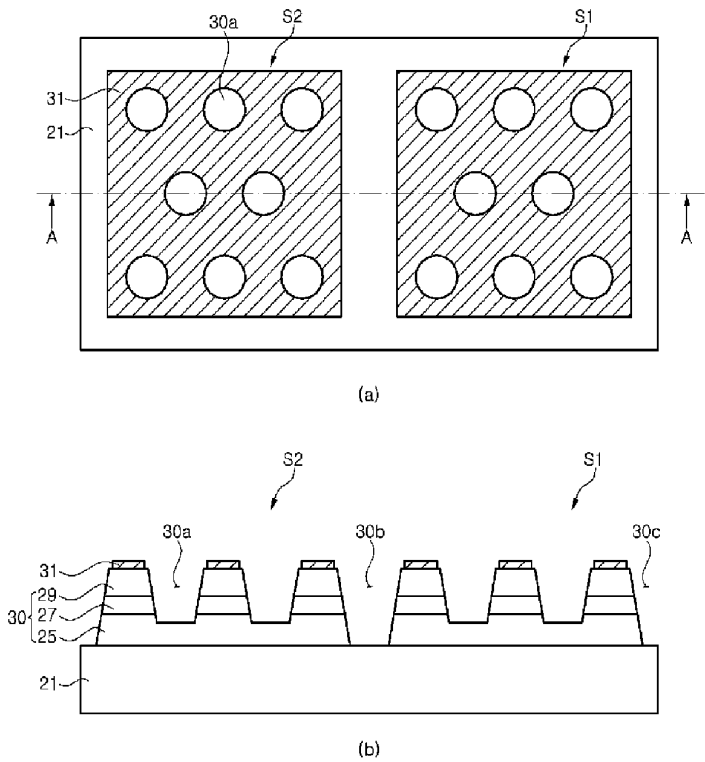
【도 4】



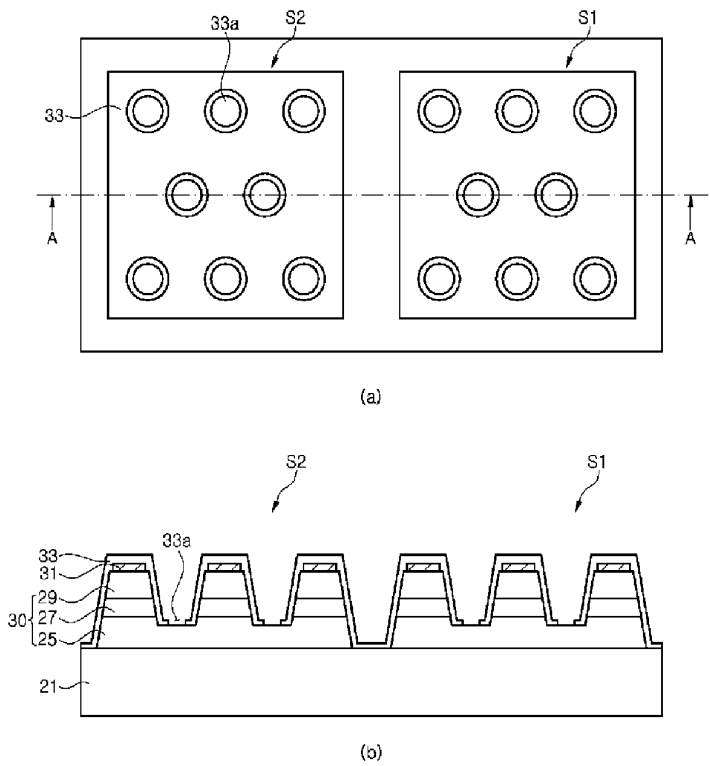
【도 5】



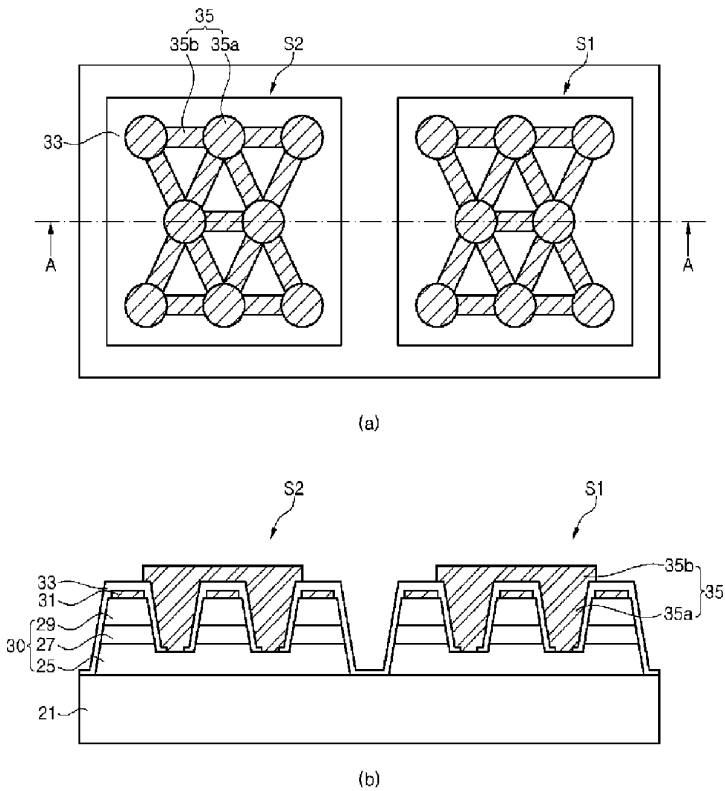
【도 6】



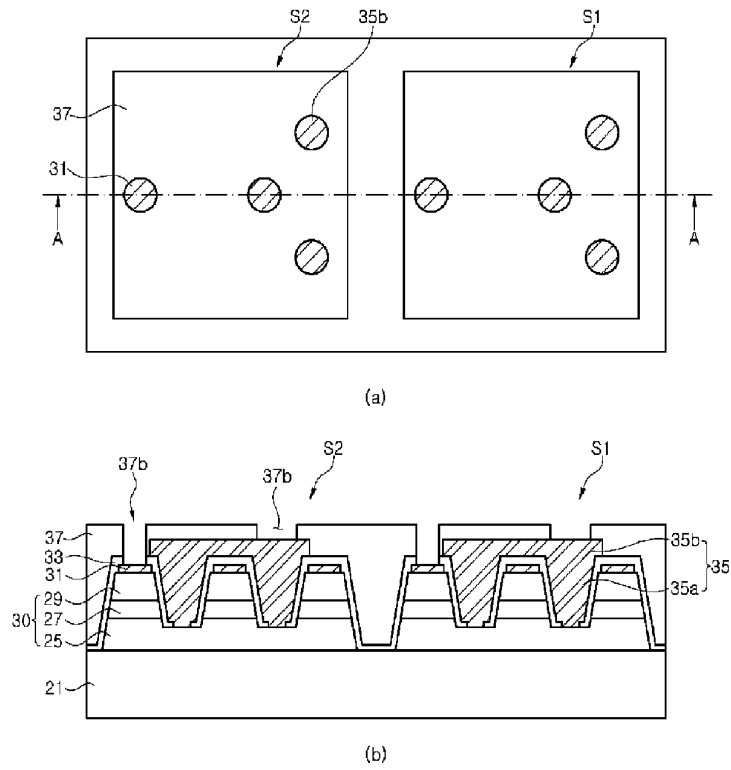
【도 7】



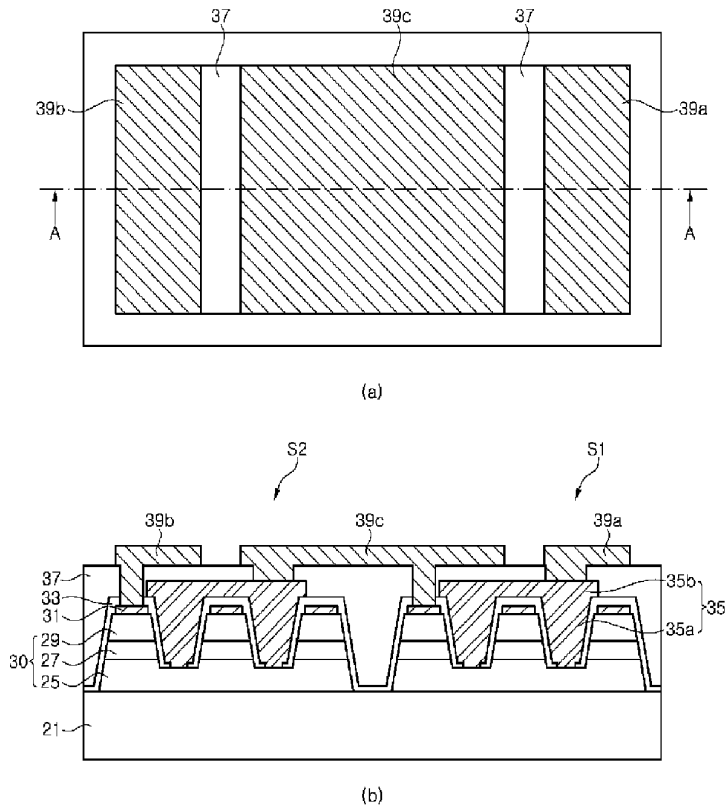
【도 8】



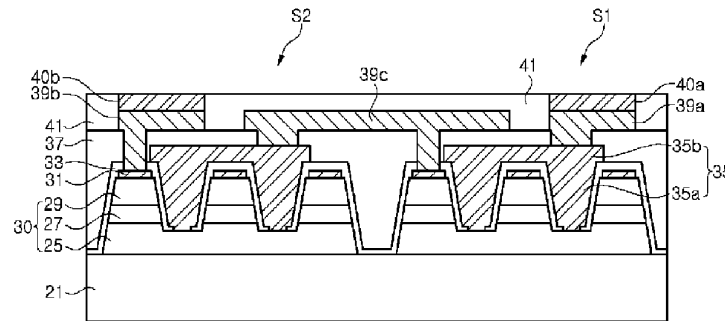
【도 9】



【도 10】



【도 11】



PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/815,433	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	19	minus 20 = *				x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1600
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/815,433	07/31/2015	2811	1600	114898-8005.US02	19	3

CONFIRMATION NO. 1096

97075

Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

FILING RECEIPT



0000000078913822

Date Mailed: 08/19/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Won Cheol Seo, Ansan-si, KOREA, REPUBLIC OF;
Dae Sung Cho, Ansan-si, KOREA, REPUBLIC OF;

Applicant(s)

Seoul Semiconductor Co., Ltd., Seoul, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 97075

Domestic Priority data as claimed by applicant

This application is a CON of 14/708,029 05/08/2015
which is a CON of 13/194,317 07/29/2011 PAT 9070851

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

REPUBLIC OF KOREA 10-2010-0092808 09/24/2010
REPUBLIC OF KOREA 10-2010-0092807 09/24/2010

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/17/2015

page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/815,433**

Projected Publication Date: 11/26/2015

Non-Publication Request: No

Early Publication Request: No
Title

WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

97075

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☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

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Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box).

SEOUL SEMICONDUCTOR CO., LTD.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

2015. Feb. 19

Name

Hyuck Jung CHOI

Title

Chief IP Counsel, SEOUL SEMICONDUCTOR CO., LTD.

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

Electronic Acknowledgement Receipt	
EFS ID:	23102279
Application Number:	14815433
International Application Number:	
Confirmation Number:	1096
Title of Invention:	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME
First Named Inventor/Applicant Name:	Won Cheol Seo
Customer Number:	97075
Filer:	Hwa C. Lee/Michelle Melendez
Filer Authorized By:	Hwa C. Lee
Attorney Docket Number:	114898-8005.US02
Receipt Date:	03-AUG-2015
Filing Date:	
Time Stamp:	19:05:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	Transmittal.pdf	60292 d571ec6bdd782fe91b6120fd15c954ada399f12f	no	1
Warnings:					
Information:					

2	Power of Attorney	POA.pdf	811491	no	1
			3130509ff4ef6e4f58760457e21163cf9f4363a4		
Warnings:					
Information:					
Total Files Size (in bytes):				871783	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82A (07-13)

Approved for use through 11/30/2014. OMB 0651-0051

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/815,433 (Conf. No. 1096)		
Filing Date	July 31, 2015		
First Named Inventor	Won Cheol Seo		
Title	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
Art Unit	n/a		
Examiner Name	n/a		
Attorney Docket Number	114898-8005.US02		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/Hwa C. Lee 59747/	Date (Optional)	August 3, 2015
Name	Hwa C. Lee	Registration Number	59,747
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
<p>NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.</p>			
<input checked="checked" type="checkbox"/> *Total of <u>1</u> forms are submitted.			

July 31, 2015

Attorney Docket No.: 114898-8005.US02

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Presented for filing is a continuation patent application of:

Title: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF
 FABRICATING THE SAME

Inventor(s): Won Cheol Seo, Dae Sung Cho

Applicant(s): Seoul Semiconductor Co., Ltd.

Enclosed are the following papers, including those required to receive a filing date under 37
C.F.R. § 1.53(b):

	<u>Pages</u>
Specification	34
Claims	13
Abstract	1
Drawings	19
Declaration	6

Enclosures:

- Application Data Sheet (7 pages).
- Information Disclosure Statement with Disclosure Form (4 pages).
- Preliminary Amendment (8 pages).

LEGAL127006076.1

ANCHORAGE • BEIJING • BELLEVUE • BOISE • CHICAGO • DALLAS • DENVER • LOS ANGELES • MADISON • NEW YORK
PALO ALTO • PHOENIX • PORTLAND • SAN DIEGO • SAN FRANCISCO • SEATTLE • SHANGHAI • WASHINGTON, D.C.

Perkins Coie LLP

Commissioner for Patents
U.S. Patent & Trademark Office
Page 2

Under 35 U.S.C. §120, this application is a continuation of, and claims the benefits and priorities to, co-pending U.S. Patent Application No. 14/708,029, filed on May 8, 2015, which is a continuation of U.S. Patent Application No. 13/194,317, filed on July 29, 2011. The U.S. Patent Application No. 13/194,317 further claims the benefits and priorities to Korean Patent Application No. 10-2010-0092807, filed on September 24, 2010, and Korean Patent Application No. 10-2010-0092808, filed on September 24, 2010. The entire content of the before-mentioned patent applications is incorporated by reference as part of the disclosure of this application.

The specification of this application as filed herewith is the original specification filed for U.S. Patent Application No. 13/194,317 on July 29, 2011. A preliminary amendment is concurrently filed herewith to reflect the priority claims for this filing and to add new claims for this continuation filing.

Basic Filing Fee			\$280.00
Search Fee			\$600.00
Examination Fee			\$720.00
Total Claims 19	over 20	0 x \$80	\$0.00
Independent Claims 3	over 3	0 x \$420	\$0.00
Fee for Multiple Dependent Claims			\$0.00
Surcharge for Late Oath or Declaration			\$0.00
Fee for each additional 50 pages of Specification and Drawings over 100			\$0.00
Total Filing fee			\$1,600.00

Please apply the required fees in the amount of \$1,600.00, and any charges or credits, to Deposit Account No. 50-5252.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 720-5700.

Please direct all correspondence to the following:

97075
PTO Customer Number

Respectfully submitted,
/Bing Ai/

Bing Ai
Reg. No. 43,312

Enclosures
BA/msm

LEGAL127006076.1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Won Cheol		Seo			
Residence Information (Select One) <input type="radio"/> US Residency <input checked="" type="radio"/> Non US Residency <input type="radio"/> Active US Military Service						
City	Ansan-si	Country of Residence i			KR	
Mailing Address of Inventor:						
Address 1		1B-36, 727-5 Wonsi-dong, Danwon-gu				
Address 2		Gyeonggi-do				
City	Ansan-si	State/Province				
Postal Code	425-851	Country i	KR			
Inventor 2					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Dae Sung		Cho			
Residence Information (Select One) <input type="radio"/> US Residency <input checked="" type="radio"/> Non US Residency <input type="radio"/> Active US Military Service						
City	Ansan-si	Country of Residence i			KR	
Mailing Address of Inventor:						
Address 1		1B-36, 727-5 Wonsi-dong, Danwon-gu				
Address 2		Gyeonggi-do				
City	Ansan-si	State/Province				
Postal Code	425-851	Country i	KR			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.						
						Add

Correspondence Information:

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence information of this application.**

Customer Number	97075		
Email Address	patentprocurement@perkinscoie.com	<input type="button" value="Add Email"/>	<input type="button" value="Remove Email"/>

Application Information:

Title of the Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
Attorney Docket Number	114898-8005.US02	Small Entity Status Claimed	<input type="checkbox"/>
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	19	Suggested Figure for Publication (if any)	2

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	<input checked="" type="radio"/> Customer Number	<input type="radio"/> US Patent Practitioner	<input type="radio"/> Limited Recognition (37 CFR 11.9)
Customer Number	97075		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
	Continuation of	14708029	2015-05-08		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14708029	Continuation of	13194317	2011-07-29	9070851	2015-06-30
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
10-2010-0092808	KR	2010-09-24	
Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
10-2010-0092807	KR	2010-09-24	
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p><input type="checkbox"/> NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
--

Authorization to Permit Access:

<input checked="" type="checkbox"/> Authorization to Permit Access to the Instant Application by the Participating Offices
<p>If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.</p> <p>In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.</p> <p>In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.</p>

Applicant Information:

<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>
--

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		

Applicant 1				Remove	
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p>					
Clear					
<input checked="" type="radio"/> Assignee		<input type="radio"/> Legal Representative under 35 U.S.C. 117		<input type="radio"/> Joint Inventor	
<input type="radio"/> Person to whom the inventor is obligated to assign.			<input type="radio"/> Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:					
Name of the Deceased or Legally Incapacitated Inventor :					
If the Applicant is an Organization check here. <input checked="" type="checkbox"/>					
Organization Name		Seoul Semiconductor Co., Ltd.			
Mailing Address Information:					
Address 1		148-29, GASAN-DONG			
Address 2		GEUMCHEON-GU			
City		Seoul	State/Province		
Country	KR	Postal Code		158-801	
Phone Number		Fax Number			
Email Address					
Additional Applicant Data may be generated within this form by selecting the Add button. Add					

Assignee Information including Non-Applicant Assignee Information:

<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>	
Assignee 1	
<p>Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.</p>	
Remove	
<p>If the Assignee or Non-Applicant Assignee is an Organization check here. <input type="checkbox"/></p>	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	114898-8005.US02
		Application Number	
Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Bing Ai/		Date (YYYY-MM-DD)	2015-07-31
First Name	Bing	Last Name	Ai	Registration Number
				43312

Additional Signature may be generated within this form by selecting the Add button.

Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY
OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)**

Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
This statement is directed to:			
<input checked="" type="checkbox"/> The attached application,			
OR			
<input type="checkbox"/> United States application or PCT international application number _____ filed on _____.			
LEGAL NAME of inventor to whom this substitute statement applies:			
(E.g., Given Name (first and middle (if any)) and Family Name or Surname)			
Dae Sung CHO			
Residence (except for a deceased or legally incapacitated inventor):			
City	Ansan-si	State	Country Republic of Korea
Mailing Address (except for a deceased or legally incapacitated inventor):			
City	Ansan-si	State	Zip 425-851 Country KR
I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.			
The above-identified application was made or authorized to be made by me.			
I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.			
Relationship to the inventor to whom this substitute statement applies:			
<input type="checkbox"/> Legal Representative (for deceased or legally incapacitated inventor only),			
<input checked="" type="checkbox"/> Assignee,			
<input type="checkbox"/> Person to whom the inventor is under an obligation to assign,			
<input type="checkbox"/> Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or			
<input type="checkbox"/> Joint Inventor.			

[Page 1 of 2]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☐ Inventor is deceased.
- ☐ Inventor is under legal incapacity.
- ☒ Inventor cannot be found or reached after diligent effort, or
- ☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

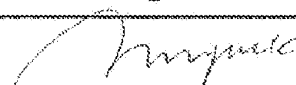
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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Hyuck Jung CHOI for Seoul Semiconductor Co., Ltd.		Date (Optional): 2014. Aug. 14	
Signature: 		Manager of IP Department	
Residence (unless provided in an application data sheet, PTO/AIA/14 or equivalent):			
City: Ansan-si	State:	Country: Republic of Korea	
Mailing Address (unless provided in an application data sheet, PTO/AIA/14 or equivalent):			
Seoul Semiconductor Co., Ltd. 1B-25, 727, Wonsi-dong, Danwon-gu, Gyeonggi-do			
City: Ansan-si	State:	Zip: 425-851	Country: KR

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 161. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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**SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY
OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)**

Title of Invention	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME		
This statement is directed to:			
<input checked="" type="checkbox"/> The attached application,			
OR			
<input type="checkbox"/> United States application or PCT international application number _____ filed on _____			
LEGAL NAME of inventor to whom this substitute statement applies:			
(E.g., Given Name (first and middle (if any)) and Family Name or Surname)			
Won Cheol SEO			
Residence (except for a deceased or legally incapacitated inventor):			
City	Ansan-si	State	Country Republic of Korea
Mailing Address (except for a deceased or legally incapacitated inventor):			
City	Ansan-si	State	Zip 425-851 Country KR
I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.			
The above-identified application was made or authorized to be made by me.			
I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.			
Relationship to the inventor to whom this substitute statement applies:			
<input type="checkbox"/> Legal Representative (for deceased or legally incapacitated inventor only),			
<input checked="" type="checkbox"/> Assignee,			
<input type="checkbox"/> Person to whom the inventor is under an obligation to assign,			
<input type="checkbox"/> Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or			
<input type="checkbox"/> Joint Inventor.			

[Page 1 of 2]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

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☒ Inventor cannot be found or reached after diligent effort, or
☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Hyuck Jung CHOI for Seoul Semiconductor Co., Ltd.		Date (Optional): 2014. Aug. 24
Signature:		Manager of IP Department
Residence (unless provided in an application data sheet, PTO/AIA/14 or equivalent):		
City: Ansan-si	State:	Country: Republic of Korea
Mailing Address (unless provided in an application data sheet, PTO/AIA/14 or equivalent):		
Seoul Semiconductor Co., Ltd. 1B-25, 727, Wonsi-dong, Danwon-gu, Gyeonggi-do		
City: Ansan-si	State:	Zip: 425-851
Country: KR		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Won Cheol Seo et al.

Application No.: Not yet assigned

Filed: Herewith

For: WAFER-LEVEL LIGHT EMITTING DIODE
PACKAGE AND METHOD OF FABRICATING THE
SAME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Please consider the references listed on the attached disclosure form. Each document listed on the disclosure form (3 pages) was cited in the parent application, U.S. Patent Application Nos. 14/708,029, filed on May 8, 2015 and 13/194,317, filed on July 29, 2011, thus copies of the documents are not provided.

This Information Disclosure Statement is not to be construed as a representation that: (i) a search has been made; (ii) additional information that may be material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the cited information is, or is considered to be, material to patentability. In addition, applicant does not admit that any enclosed item of information constitutes prior art to the subject invention and specifically reserves the right to demonstrate that any such reference is not prior art.

Consideration of the references listed plus the return of a copy of the enclosed disclosure form with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Inventor : Won Cheol Seo et al.
Appl. No. : Not yet assigned
Filed : Herewith
Page : 2 of 2

Docket No. 114898-8005.US02

This statement is being filed within three months of the filing date of the application or before receipt of a first Office Action on the merits. No fee is required.

Respectfully submitted,

Date: July 31, 2015

/Bing Ai/
Bing Ai
Reg. No. 43,312

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Facsimile: (206) 359-7198

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 114898-8005.US02	Application No. Not yet assigned
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Seoul Semiconductor Co., Ltd.	
		Filing Date Herewith	Group Art Unit Not yet assigned

U.S. Patent Documents							
Examiner Initial	Design ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	6876008	2005-04-05	Bhat et al.			
	2	7095061	2006-08-22	Steigerwald et al.			
	3	7417259	2008-08-26	Sakai et al.			
	4	7709849	2010-05-04	Kal et al.			
	5	7723736	2010-05-05	Lee et al.			
	6	7750469	2010-07-06	Cho et al.			
	7	7838891	2010-11-23	Lee et al.			
	8	7846755	2010-12-07	Kal et al.			
	9	7880181	2011-02-01	Yoon et al.			
	10	8319246	2012-11-27	Sugizaki			
	11	20080087902	2008-04-17	Lee et al.			
	12	20090039359	2009-02-12	Yoon et al.			
	13	20090085048	2009-04-02	Lee et al.			
	14	20090267085	2009-10-29	Lee et al.			
	15	20090283787	2009-11-19	Donofrio et al.			
	16	20100078656	2010-04-01	Seo et al.			
	17	20100078656	2010-04-01	Seo et al.			
	18	20100117111	2010-05-13	Illek et al.			
	19	20100148190	2010-06-17	Kim et al.			
	20	20100163887	2010-07-01	Kim et al.			
	21	20100163900	2010-07-01	Seo et al.			
	22	20100244060	2010-09-30	Lee et al.			
	23	20110101414	2011-05-05	Thompson et al.			
	24	20110140135	2011-06-16	Lee et al.			
	25	20110169040	2011-07-14	Seo et al.			
	26	20110175129	2011-07-21	Lee et al.			
	27	20120032218	2012-02-09	Choi et al.			

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 114898-8005.US02	Application No. Not yet assigned
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Seoul Semiconductor Co., Ltd.	
		Filing Date Herewith	Group Art Unit Not yet assigned

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	28	100599012	2006-07-04	KR				
	29	100838197	2008-06-16	KR				
	30	2004006582	2004-01-08	JP				
	31	2004023568	2004-03-18	WO				
	32	2007001124	2007-01-04	WO				
	33	2008130656	2008-06-05	JP				
	34	2008141015	2008-06-19	JP				
	35	1020100016631	2010-02-12	KR				
	36	1020100036617	2010-04-08	KR				
	37	1020100079843	2010-07-08	KR				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	38	Notice of Allowance of US Patent Application No. 12/623,990 dated April 27, 2012
	39	Non-Final Office Action of US Patent Application No. 12/623,968 dated January 17, 2012
	40	Non-Final Office Action of US Patent Application No. 12/623,990 dated January 19, 2012
	41	Notice of Allowance of US Patent Application No. 12/624,011 dated January 24, 2012
	42	Non-Final Office Action of US Patent Application No. 12/123,162 dated August 5, 2010
	43	Notice of Allowance of US Patent Application No. 12/123,162 dated November 30, 2010
	44	Notice of Allowance of related US Patent Application No. 13/345,348 dated June 25, 2012
	45	Notice of Allowance of related US Patent Application No. 12/623,968 dated May 21, 2012
	46	Non-Final Office Action dated April 13, 2012 for US Patent Application No. 13/345,348.
	47	International Search Report and Written Opinion dated May 1, 2012, PCT/kr2011/006544
	48	Notice of Allowance dated January 11, 2013 issued for US Patent Application No. 13/482,851
	49	Non-Final Office Action issued on June 13, 2013, in US Patent Application No. 13/865,719
	50	Notice of Allowance issued on October 1, 2013, in US Patent Application No. 13/865,719

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF
FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** This application claims priority from and the benefit of Korean Patent Application
No. 10-2010-0092807, filed on September 24, 2010, and Korean Patent Application No. 10-
2010-0092808, filed on September 24, 2010, which are hereby incorporated by reference for all
purposes as if fully set forth herein.

10 BACKGROUND OF THE INVENTION

[0002] FIELD OF THE INVENTION

[0003] The invention relates to a light emitting diode package and a method of
fabricating the same and, more particularly, to a wafer-level light emitting diode package and a
method of fabricating the same.

15 **[0004]** DESCRIPTION OF THE BACKGROUND

[0005] A light emitting diode (LED) is a semiconductor device that includes an N-type
semiconductor and a P-type semiconductor, and emits light through recombination of holes and
electrons. Such an LED has been used in a wide range of applications such as display devices,
traffic lights, and backlight units. Further, considering the potential merits of lower power
consumption and longer lifespan than existing electric bulbs or fluorescent lamps, the application
20 range of LEDs has been expanded to general lighting by replacing existing incandescent lamps
and fluorescent lamps.

[0006] The LED may be used in an LED module. The LED module is manufactured

through a process of fabricating an LED chip at a wafer level, a packaging process, and a modulation process. Specifically, semiconductor layers are grown on a substrate such as a sapphire substrate, and subjected to a wafer-level patterning process to fabricate LED chips having electrode pads, followed by division into individual chips (chip fabrication process). Then, after mounting the individual chips on a lead frame or a printed circuit board, the electrode pads are electrically connected to lead terminals via bonding wires, and the LED chips are covered by a molding member, thereby providing an LED package (packaging process). Then, the LED package is mounted on a circuit board such as a metal core printed circuit board (MC-PCB), thereby providing an LED module such as a light source module (modulation process).

[0007] In the packaging process, a housing and/or the molding member may be provided to the LED chip to protect the LED chip from the external environment. In addition, a phosphor may be contained in the molding member to convert light emitted by the LED chip so that the LED package may emit a white light, thereby providing a white LED package. Such a white LED package may be mounted on the circuit board such as the MC-PCB and a secondary lens may be provided to the LED package to adjust orientation characteristics of light emitted from the LED package, thereby providing a desired white LED module.

[0008] However, it may be difficult to achieve miniaturization and satisfactory heat dissipation of the conventional LED package including the lead frame or printed circuit board. Furthermore, luminous efficiency of the LED may be deteriorated due to absorption of light by the lead frame or the printed circuit board, electric resistance heating by the lead terminals, and the like.

[0009] In addition, the chip fabrication process, the packaging process, and the modulation process may be separately carried out, thereby increasing time and costs for

manufacturing the LED module.

[0010] Meanwhile, alternating current (AC) LEDs have been produced and marketed. The AC LED includes an LED directly connected to an AC power source to permit continuous emission of light. One example of AC LEDs, which can be used by being directly connected to a high voltage AC power source, is disclosed in U.S. Patent No. 7,417,259, issued to Sakai, *et. al.*

[0011] According to U.S. Patent No. 7,417,259, LED elements are arranged in a two-dimensional pattern on an insulating substrate, for example, a sapphire substrate, and are connected in series to form LED arrays. The LED arrays are connected in series to each other, thereby providing a light emitting device that can be operated at high voltage. Further, such LED arrays may be connected in reverse parallel to each other on the sapphire substrate, thereby providing a single-chip light emitting device that can be operated to continuously emit light using an AC power supply.

[0012] Since the AC-LED includes light emitting cells on a growth substrate, for example, on a sapphire substrate, the AC-LED restricts the structure of the light emitting cells and may limit improvement of light extraction efficiency. Thus, investigation has been made into a light emitting diode, for example, an AC-LED that is based on a substrate separation process and includes light emitting cells connected in series to each other.

SUMMARY OF THE INVENTION

[0013] Exemplary embodiments of the invention provide a wafer-level LED package and a method of fabricating the same, which can be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board.

[0014] Exemplary embodiments of the invention also provide a wafer-level LED package.

and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

[0015] Exemplary embodiments of the invention also provide a method of fabricating an LED package, which may reduce manufacturing time and cost of an LED module.

5 [0016] Exemplary embodiments of the invention also provide an LED module and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

[0017] Exemplary embodiments of the invention also provide a wafer-level light emitting diode package and a method of fabricating the same, which includes a plurality of light emitting cells and may be directly formed in a module on a circuit board without using a conventional
10 lead frame or printed circuit board.

[0018] Additional features of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention.

[0019] An exemplary embodiment of the present invention discloses an LED package
15 including: a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type
20 semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

[0020] An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package according to the aforementioned exemplary embodiments. The LED module may include a circuit board; the LED package mounted on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

5 [0021] An exemplary embodiment of the present invention also discloses a method of fabricating an LED package. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of contact holes exposing the first conductive type semiconductor layer; 10 forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region; and forming a first bump and a second bump on the semiconductor stack. The first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes, and the second bump is electrically connected to the second 15 conductive type semiconductor layer.

[0022] An exemplary embodiment of the present invention also discloses a light emitting diode package. The LED package includes a plurality of light emitting cells each including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type 20 semiconductor layer and the active layer of each of the light emitting cells, the contact holes exposing the first conductive type semiconductor layer thereof; a protective insulation layer covering a sidewall of each of the light emitting cells; a connector located arranged on a first side of the light emitting cells and electrically connecting two adjacent light emitting cells to each

other; a first bump arranged on the first side of the light emitting cells and electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells; and a second bump arranged in the first side of the light emitting cells and electrically connected to the second conductive type semiconductor layer of a second light emitting cell of the light emitting cells.

[0023] An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package described above. The module includes a circuit board; the LED package arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

[0024] An exemplary embodiment of the present invention also discloses a method of fabricating an LED package including a plurality of light emitting cells. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region and a light emitting cell separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of light emitting cells, each light emitting cell having a plurality of contact holes exposing the first conductive type semiconductor layer; forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region and the light emitting cell separation region; forming a connector connecting adjacent light emitting cells in series to each other; and forming a first bump and a second bump on the plurality of light emitting cells. Here, the first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells, and the second bump is electrically connected to the second conductive type

semiconductor layer of a second light emitting cell of the light emitting cells.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

5

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to
10 explain the principles of the invention.

[0027] Figure 1 is a schematic sectional view of a light emitting diode package according to a first exemplary embodiment of the invention.

[0028] Figure 2 is a schematic sectional view of a light emitting diode package according to a second exemplary embodiment of the invention.

15 [0029] Figure 3 is a sectional view of a light emitting diode module including the light emitting diode package according to the first exemplary embodiment.

[0030] Figure 4 to Figure 12 show a method of fabricating the light emitting diode package according to the first exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in Figure 5 to Figure 10.

20 [0031] Figure 13 is a sectional view showing a method of fabricating the light emitting diode package according to the second exemplary embodiment of the invention.

[0032] Figure 14 is a schematic sectional view of a light emitting diode package according to a third exemplary embodiment of the invention.

[0033] Figure 15 is a schematic sectional view of a light emitting diode package according to a fourth exemplary embodiment of the invention.

[0034] Figure 16 is a sectional view of a light emitting diode module including the light emitting diode package according to the third exemplary embodiment.

5 [0035] Figure 17 to Figure 26 show a method of fabricating the light emitting diode package according to the third exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in Figure 18 to Figure 23.

[0036] Figure 27 is a sectional view showing a method of fabricating the light emitting diode package according to the fourth exemplary embodiment of the invention.

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DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0037] The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as
15 limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough and will fully convey the scope of the invention to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0038] It will be understood that when an element such as a layer, film, region or
20 substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0039] Figure 1 is a schematic sectional view of an LED package 100 according to a first

exemplary embodiment of the invention.

[0040] Referring to Figure 1, the LED package 100 may include a semiconductor stack 30, a first contact layer 35, a second contact layer 31, a first insulation layer 33, a second insulation layer 37, a first electrode pad 39a, a second electrode pad 39b, a first bump 45a, and a second bump 45b. The LED package 100 may further include an insulation layer 43, a dummy bump 45c, and a wavelength convertor 51.

[0041] The semiconductor stack 30 includes a first conductive type upper semiconductor layer 25, an active layer 27, and a second conductive type lower semiconductor layer 29. The active layer 27 is interposed between the upper and lower semiconductor layers 25, 29.

[0042] The active layer 27 and the upper and lower semiconductor layers 25, 29 may be composed of a III-N based compound semiconductor, for example, (Al, Ga, In)N semiconductor. Each of the upper and lower semiconductor layers 25, 29 may be a single layer or multiple layers. For example, the upper and/or lower semiconductor layers 25, 29 may include a super lattice layer in addition to a contact layer and a clad layer. The active layer 27 may have a single quantum well structure or a multi-quantum well structure. The first conductive type may be an n-type and the second conductive type may be a p-type. Alternatively, the first conductive type may be a p-type and the second conductive type may be an n-type. Since the upper semiconductor layer 25 can be formed of an n-type semiconductor layer having relatively low specific resistance, the upper semiconductor layer 25 may have a relatively high thickness. Therefore, a roughened surface R may be formed on an upper surface of the upper semiconductor layer 25, in which the roughened surface R enhances extraction efficiency of light generated in the active layer 27.

[0043] The semiconductor stack 30 has a plurality of contact holes 30a (see Figure 5(b))

formed through the second conductive type lower semiconductor layer 29 and the active layer 27 to expose the first conductive type upper semiconductor layer, and the first contact layer 35 contacts the first conductive type upper semiconductor layer 25 exposed in the plurality of contact holes.

5 **[0044]** The second contact layer 31 contacts the second conductive type lower semiconductor layer 29. The second contact layer 31 includes a reflective metal layer to reflect light generated in the active layer 27. Further, the second contact layer 31 may form an ohmic contact with the second conductive type lower semiconductor layer 29.

10 **[0045]** The first insulation layer 33 covers the second contact layer 31. Further, the first insulation layer 33 covers a sidewall of the semiconductor stack 30 exposed in the plurality of contact holes 30a. In addition, the first insulation layer 33 may cover a side surface of the semiconductor stack 30. The first insulation layer 33 insulates the first contact layer 35 from the second contact layer 31 while insulating the second conductive type lower semiconductor layer 29 and the active layer 27 exposed in the plurality of contact holes 30a from the first contact
15 layer 35. The first insulation layer 33 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation layer 33 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$.

20 **[0046]** The first contact layer 35 is located under the first insulation layer 33 and contacts the first conductive type upper semiconductor layer 25 through the first insulation layer 33 in the plurality of contact holes 30a. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25, and a connecting section 35b connecting the contact sections 35a to each other. Therefore, the contact sections 35a are electrically

connected to each other by the connecting section 35b. The first contact layer 35 is formed under some regions of the first insulation layer 33 and may be composed of a reflective metal layer.

[0047] The second insulation layer 37 covers the first contact layer 35 under the first contact layer 35. In addition, the second insulation layer 37 covers the first insulation layer 33 while covering a side surface of the semiconductor stack 30. The second insulation layer 37 may be composed of a single layer or multiple layers. Further, the second insulation layer 37 may be a distributed Bragg reflector.

[0048] The first and second electrode pads 39a, 39b are located under the second insulation layer 37. The first electrode pad 39a may be connected to the first contact layer 35 through the second insulation layer 37. Further, the second electrode pad 39b may be connected to the second contact layer 31 through the second insulation layer 37 and the first insulation layer 33.

[0049] The first bump 45a and the second bump 45b are located under the first and second electrode pads 39a, 39b to be connected thereto, respectively. The first and second bumps 45a, 45b may be formed by plating. The first and second bumps 45a, 45b are terminals electrically connected to a circuit board such as an MC-PCB and have coplanar distal ends. In addition, the first electrode pad 39a may be formed at the same level as that of the second electrode pad 39b, so that the first bump 45a and the second bump 45b may also be formed on the same plane. Therefore, the first and second bumps 45a, 45b may have the same height.

[0050] Meanwhile, the dummy bump 45c may be located between the first bump 45a and the second bump 45b. The dummy bump 45c may be formed together with the first and second bumps 45a and 45b to provide a heat passage for discharging heat from the semiconductor stack 30.

[0051] The insulation layer 43 may cover side surfaces of the first and second bumps 45a, 45b. The insulation layer 43 may also cover a side surface of the dummy bump 45c. In addition, the insulation layer 43 fills spaces between the first bump 45a, the second bump 45b and the dummy bump 45c to prevent moisture from entering the semiconductor stack 30 from outside. The insulation layer 43 also covers side surfaces of the first and second electrode pads 39a, 39b to protect the first and second electrode pads 39a, 39b from external environmental factors such as moisture. Although the insulation layer 43 may be configured to cover the overall side surfaces of the first and second bumps 45a, 45b, the invention is not limited thereto. Alternatively, the insulation layer 43 may cover the side surfaces of the first and second bumps 45a, 45b except for some regions of the side surface near distal ends of the first and second bumps,

[0052] In the present exemplary embodiment, the insulation layer 43 is illustrated as covering the side surfaces of the first and second electrode pads 39a and 39b, but the invention is not limited thereto. Alternatively, another insulation layer may be used to cover the first and second electrode pads 39a, 39b and the insulation layer 43 may be formed under the other insulation layer. In this case, the first and second bumps 45a, 45b may be connected to the first and second electrode pads 39a, 39b through the other insulation layer.

[0053] The wavelength convertor 51 may be located on the first conductive type upper semiconductor layer 25 opposite to the rest of the semiconductor stack 30. The wavelength convertor 51 may contact an upper surface of the first conductive type upper semiconductor layer 25. The wavelength convertor 51 may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength converter 51 may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength

conversion.

[0054] In the present exemplary embodiment, the side surface of the semiconductor stack 30 is covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer 33 and/or the second insulation layer 37. In addition, the first contact layer 35 may be covered with the second insulation layer 37 to be protected from an external environment and the second contact layer 31 may be covered with the first insulation layer 33 and the second insulation layer 37 to be protected from an external environment. The first and second electrode pads 39a, 39b are also protected by, for example, the insulation layer 43. Accordingly, it is possible to prevent deterioration of the semiconductor stack 30 due to moisture.

[0055] The wavelength convertor 51 may be attached to the first conductive type upper semiconductor layer 25 at a wafer-level, and then divided together with the protective insulation layer during a chip separation process. Therefore, a side surface of the wavelength convertor 51 may be in a line with the protective insulation layer. That is, the side surface of the wavelength convertor 51 may be flush along a straight line with a side surface of the protective insulation layer. Further, the side surface of the wavelength convertor 51 may be in a line with a side surface of the insulation layer 43. Thus, the side surfaces of the wavelength convertor 51, the protective insulation layer, and the insulation layer 43 may all be flush along a straight line.

[0056] Figure 2 is a schematic sectional view of a light emitting diode package 200 according to a second exemplary embodiment of the invention.

[0057] Referring to Figure 2, the LED package 200 is similar to the LED package 100 according to the above exemplary embodiment. In the present exemplary embodiment, however, first and second bumps 65a, 65b are formed in a substrate 61.

[0058] Specifically, the substrate 61 includes through-holes, which have the first and second bumps 65a, 65b formed therein, respectively. The substrate 61 is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto. The substrate 61 having the first and second bumps 65a, 65b may be attached to a first electrode pad 39a and a second electrode pad 39b. In this case, to prevent the first and second electrode pads 39a, 39b from being exposed to the outside, an insulation layer 49 may cover side surfaces and bottom surfaces of the first and second electrode pads 39a, 39b. Further, the insulation layer 49 may have openings, which expose the first and second electrode pads 39a, 39b, and additional metal layers 67a, 67b are then formed in the openings. The additional metal layers 67a, 67b may be composed of a bonding metal.

[0059] Figure 3 is a sectional view of a light emitting diode module including the LED package 100 according to the first exemplary embodiment.

[0060] Referring to Figure 3, the LED module includes a circuit board 71, for example, an MC-PCB, the LED package 100, and a lens 81. The circuit board 71, for example, the MC-PCB, has connection pads 73a, 73b for mounting the LED packages 100 thereon. The first and second bumps 45a, 45b (see Figure 1) of the LED package 100 are connected to the connection pads 73a, 73b, respectively.

[0061] A plurality of LED packages 100 may be mounted on the circuit board 71 and the lens 81 may be disposed on the LED packages 100 to adjust an orientation angle of light emitted from the LED packages 100.

[0062] In accordance with the second exemplary embodiment, the light emitting diode packages 200 may be mounted on the circuit board instead of the LED packages 100.

[0063] Figure 4 to Figure 12 show a method of fabricating the LED package 100 according to the first exemplary embodiment. In Figure 5 to Figure 10, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

[0064] Referring to Figure 4, a semiconductor stack 30, which includes a first conductive type semiconductor layer 25, an active layer 27 and a second conductive type semiconductor layer 29, is formed on a growth substrate 21. The growth substrate 21 may be a sapphire substrate but is not limited thereto. Alternatively, the growth substrate 21 may be another kind of heterogeneous substrate, for example, a silicon substrate. Each of the first and second conductive type semiconductor layers 25, 29 may be composed of a single layer or multiple layers. Further, the active layer 27 may have a single-quantum well structure or multi-quantum well structure.

[0065] The compound semiconductor layers may be formed of III-N based compound semiconductor on the growth substrate 21 by metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE).

[0066] A buffer layer (not shown) may be formed before forming the compound semiconductor layers. The buffer layer is formed to relieve lattice mismatch between the growth substrate 21 and the compound semiconductor layers and may be formed of a GaN-based material layer such as gallium nitride or aluminum nitride.

[0067] Referring to (a) and (b) of Figure 5, the semiconductor stack 30 is patterned to form a chip (package) separation region 30b while patterning the second conductive type semiconductor layer 29 and the active layer 27 to form a plurality of contact holes 30a exposing the first conductive type semiconductor layer 25. The semiconductor stack 30 may be patterned by photolithography and etching processes.

[0068] The chip separation region 30b is a region for dividing the LED package structure

into individual LED packages and side surfaces of the first conductive type semiconductor layer 25, the active layer 27 and the second conductive type semiconductor layer 29 are exposed on the chip separation region 30b. Advantageously, the chip separation region 30b may be configured to expose the substrate 21 without being limited thereto.

5 **[0069]** The plurality of contact holes 30a may have a circular shape, but is not limited thereto. The contact holes 30 may have a variety of shapes. The second conductive type semiconductor layer 29 and the active layer 27 are exposed to sidewalls of the plurality of contact holes 30a. As shown, the contact holes 30a may have slanted sidewalls.

10 **[0070]** Referring to (a) and (b) of Figure 6, a second contact layer 31 is formed on the second conductive type semiconductor layer 29. The second contact layer 31 is formed on the semiconductor stack 30 except for regions corresponding to the plurality of contact holes 30a.

15 **[0071]** The second contact layer 31 may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al). The second contact layer 31 may be composed of a single layer or multiple layers. The second contact layer 31 may also be configured to form an ohmic contact with the second conductive type semiconductor layer 29.

[0072] The second contact layer 31 may be formed before or after formation of the plurality of contact holes 30a.

20 **[0073]** Referring to (a) and (b) of Figure 7, a first insulation layer 33 is formed to cover the second contact layer 31. The first insulation layer 33 may cover the side surface of the semiconductor stack 30 exposed to the chip separation region 30b while covering the sidewalls of the plurality of contact holes 30a. Here, the first insulation layer 33 may have openings 33a, which expose the first conductive type semiconductor layer 25 in the plurality of contact holes

30a.

[0074] The first insulation layer 33 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation layer 33 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation
5 layers having different indices of refraction. For example, the first insulation layer 33 may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$. Further, the first insulation layer 33 may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

10 [0075] Referring to (a) and (b) of Figure 8, a first contact layer 35 is formed on the first insulation layer 33. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25 exposed in the contact holes 30a, and a connecting section 35b connecting the contact sections 35a to each other. The first contact layer 35 may be composed of a reflective metal layer, but is not limited thereto.

15 [0076] The first contact layer 35 is formed on some regions of the semiconductor stack 30, so that the first insulation layer 33 is exposed on other regions of the semiconductor stack 30 where the first contact layer 35 is not formed.

[0077] Referring to (a) and (b) of Figure 9, a second insulation layer 37 is formed on the first contact layer 35. The second insulation layer 37 may be composed of a single layer or
20 multiple layers, such as a silicon oxide or silicon nitride film. Further, the second insulation layer 37 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

[0078] The second insulation layer 37 may cover the first contact layer 35 while covering

the first insulation layer 33. The second insulation layer 37 may also cover the side surface of the semiconductor stack 30 in the chip separation region 30b.

[0079] The second insulation layer 37 has an opening 37a which exposes the first contact layer 35. Further, the second insulation layer 37 and the first insulation layer 33 are formed with an opening 37b, which exposes the second contact layer 31.

[0080] Referring to (a) and (b) of Figure 10, first and second electrode pads 39a, 39b are formed on the second insulation layer 37. The first electrode pad 39a is connected to the first contact layer 35 through the opening 37a and the second electrode pad 39b is connected to the second contact layer 31 through the opening 37b.

[0081] The first electrode pad 39a is separated from the second electrode pad 39b and each of the first and second electrode pads 39a, 39b may have a relatively large area from a top perspective, for example, an area not less than 1/3 of the area of the LED package.

[0082] Referring to Figure 11, an insulation layer 43 is formed on the first and second electrode pads 39a, 39b. The insulation layer 43 covers the first and second electrode pads 39a, 39b and has grooves which expose upper surfaces of the electrode pads 39a, 39b. Further, the insulation layer 43 may have a groove which exposes the second insulation layer 37 between the first and second electrode pads 39a, 39b.

[0083] Then, first and second bump 45a, 45b are formed in the grooves of the insulation layer 43, and a dummy bump 45c may be formed between the first bump and the second bump.

[0084] The bumps may be formed by plating, for example, electroplating, using a metallic material. If necessary, a seed layer for plating may also be formed.

[0085] After the first and second bumps 45a, 45b are formed, the insulation layer 43 may be removed. For example, the insulation layer 43 may be formed of a polymer such as

photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer 43 may remain to protect the side surfaces of the first and second bumps 45a, 45b.

[0086] In the present exemplary embodiment, the insulation layer 43 is illustrated as being directly formed on the first and second electrode pads 39a, 39b. In other exemplary
5 embodiments, another insulation layer may be formed to cover the first and second electrode pads 39a, 39b. The other insulation layer may be configured to have openings exposing the first and second electrode pads 39a, 39b. Then, the processes of forming the insulation layer 43 and the bumps may be carried out.

[0087] Referring to Figure 12, the growth substrate 21 is removed and a wavelength
10 converter 51 is attached to the first conductive type semiconductor layer 25. The growth substrate 21 may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

[0088] Then, the exposed surface of the first conductive type semiconductor layer 25 is subjected to anisotropic etching such as photoelectrochemical (PEC) etching to form a
15 roughened surface on the exposed first conductive type semiconductor layer 25.

[0089] Meanwhile, the wavelength converter such as a phosphor sheet containing phosphors may be attached to the first conductive type semiconductor layer 25.

[0090] Alternatively, the growth substrate 21 may contain an impurity for converting a wavelength of light generated in the active layer 27. In this case, the growth substrate 21 may be
20 used as the wavelength converter 51.

[0091] Then, the LED package structure is divided into individual packages along the chip separation region 30b, thereby providing finished LED packages 100. At this time, the second insulation layer 37 is cut together with the wavelength converter 51 so that cut planes

thereof can be formed in a line.

[0092] Figure 13 is a sectional view showing a method of fabricating the LED package 200 according to the second exemplary embodiment of the present invention.

[0093] Referring to Figure 13, in the method of fabricating the LED package 200 according to the present exemplary embodiment, the processes until the first and second electrode pads 39a, 39b are formed are the same as those of the method of fabricating the LED package 100 described above (Figures 10 (a) and (b)).

[0094] After the first and second electrode pads 39a, 39b are formed, an insulation layer 49 is formed to cover the first and second electrode pads 39a, 39b. The insulation layer 49 may cover side surfaces of the first and second electrode pads 39a, 39b to protect the first and second electrode pads 39a, 39b. The insulation layer 49 has openings which expose the first and second electrode pads 39a, 39b. Additional metal layers 67a, 67b are then formed in the openings. The additional metal layers 67a, 67b may be composed of a bonding metal.

[0095] The substrate 61 is bonded to the first and second electrode pads 39a, 39b. The substrate 61 may have through-holes, in which the first and second bumps 65a, 65b may be formed. Further, the first and second bumps may be formed at distal ends thereof with pads 69a, 69b. The substrate 61 having the first and second bumps 65a, 65b and the pads 69a, 69b may be separately prepared and bonded to a wafer having the first and second electrode pads 39a, 39b.

[0096] Then, as described with reference to Figure 12, the growth substrate 21 is removed and a wavelength convertor 51 may be attached to the first conductive type semiconductor layer 25, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages 200 as described in Figure 2 are provided.

[0097] Figure 14 is a sectional view of an LED package 300 according to a third

exemplary embodiment of the present invention.

[0098] Referring to Figure 14, the LED package 300 may include a semiconductor stack 130, which is divided into a plurality of light emitting cells (only two light emitting cells S1, S2 are shown herein), a first contact layer 135, a second contact layer 131, a first insulation layer 133, a second insulation layer 137, a first electrode pad 139a, a second electrode pad 139b, a connector 139c connecting adjacent light emitting cells to each other in series, a first bump 145a and a second bump 145b. Further, the LED package 300 may include a third insulation layer 141, an insulation layer 143, a dummy bump 145c, a wavelength convertor 151, and additional metal layers 140a, 140b.

[0099] The semiconductor stack 130 includes a first conductive type upper semiconductor layer 125, an active layer 127, and a second conductive type lower semiconductor layer 129. The semiconductor stack 130 of the present exemplary embodiment is similar to the semiconductor stack 30 described in Figure 1, and a detailed description thereof will be omitted herein.

[0100] Each of the light emitting cells S1, S2 has a plurality of contact holes 130a (see Figure 18(b)) extending through the second conductive type lower semiconductor layer 129 and the active layer 127 to expose the first conductive type upper semiconductor layer, and the first contact layer 135 contacts the first conductive type upper semiconductor layer 125 exposed in the plurality of contact holes. The light emitting cells S1, S2 are separated from each other by a cell separation region 130b (see Figure 18(b)).

[0101] The second contact layer 131 contacts the second conductive type lower semiconductor layer 129 of each of the light emitting cells S1, S2. The second contact layer 131 includes a reflective metal layer to reflect light generated in the active layer 127. Further, the

second contact layer 131 may form an ohmic contact with the second conductive type lower semiconductor layer 129.

[0102] The first insulation layer 133 covers the second contact layer 131. Further, the first insulation layer 133 covers a sidewall of the semiconductor stack 130 exposed in the plurality of contact holes 130a. In addition, the first insulation layer 133 may cover a side surface of each of the light emitting cells S1, S2. The first insulation layer 133 insulates the first contact layer 135 from the second contact layer 131 while insulating the second conductive type lower semiconductor layer 129 and the active layer 127 exposed in the plurality of contact holes 130a from the first contact layer 35. The first insulation layer 133 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Furthermore, the first insulation layer 133 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$.

[0103] The first contact layer 135 is located under the first insulation layer 133 and contacts the first conductive type upper semiconductor layer 125 through the first insulation layer 133 in the plurality of contact holes 130a in each of the light emitting cells S1, S2. The first contact layer 135 includes contact sections 135a contacting the first conductive type upper semiconductor layer 125, and a connecting section 135b connecting the contact sections 135a to each other. Therefore, the contact sections 135a are electrically connected to each other by the connecting section 135b. The first contact layers 135 located under the respective light emitting cells S1, S2 are separated from each other and formed under some regions of the first insulation layer 133. The first contact layer 135 may be composed of a reflective metal layer.

[0104] The second insulation layer 137 covers the first contact layer 135 under the first contact layer 135. In addition, the second insulation layer 137 may cover the first insulation layer 133 while covering the side surface of each of the light emitting cells S1, S2. The second insulation layer 137 may be composed of a single layer or multiple layers. Alternatively, the second insulation layer 37 may be composed of a distributed Bragg reflector.

[0105] The first electrode pad 139a and the second electrode pad 139b are located under the second insulation layer 137. The first electrode pad 139a may be connected to the first contact layer 135 of a first light emitting cell S1 through the second insulation layer 137. Further, the second electrode pad 139b may be connected to the second contact layer 31 of a second light emitting cell S2 through the second insulation layer 137 and the first insulation layer 133.

[0106] The connector 139c is located under the second insulation layer 137 and electrically connects two adjacent light emitting cells S1, S2 to each other through the second insulation layer 137. The connector 139c may connect the second contact layer 131 of one light emitting cell S1 to the first contact layer 135 of another light emitting cell S2 adjacent thereto, so that the two light emitting cells S1, S2 are connected in series to each other.

[0107] In the present exemplary embodiment, two light emitting cells S1, S2 are illustrated. However, it should be understood that two or more light emitting cells may be connected in series to each other by a plurality of connectors 139c. Here, the first and second electrode pads 139a, 139b may be connected in series to the light emitting cells S1, S2 located at opposite ends of such series array.

[0108] Meanwhile, the third insulation layer 141 may cover the first electrode pad 139a, the second electrode pad 139b and the connector 139c under the first electrode pad 139a, the second electrode pad 139b and the connector 139c. The third insulation layer 141 may have an

opening exposing the first electrode pad 139a and the second electrode pad 139b. The third insulation layer 141 may be formed of a silicon oxide or silicon nitride film.

[0109] The first bump 145a and the second bump 145b are located under the first and second electrode pads 139a, 139b, respectively. The first and second bumps 145a, 145b may be formed by plating. The first and second bumps 145a, 145b are terminals electrically connected to a circuit board such as an MC-PCB and have distal ends coplanar with each other. In addition, the first electrode pad 139a may be formed at the same level as that of the second electrode pad 139b, so that the first bump 45a and the second bump 45b may also be formed on the same plane. Therefore, the first and second bumps 45a, 45b may have the same height.

[0110] The additional metal layers 140a, 140b may be interposed between the first bump 145a and the first electrode pad 139a and between the second bump 145b and the second electrode pad 139b. Here, the additional metal layers 140a, 140b are provided to form the first and second electrode pads 139a, 139b to be higher than the connector 139c and may be located inside openings of the third insulation layer 141. The first and second electrode pads 139a, 139b and the additional metal layers 140a, 140b may constitute final electrode pads.

[0111] Meanwhile, the dummy bump 145c may be located between the first bump 145a and the second bump 145b. The dummy bump 145c may be formed together with the first and second bump 145a, 145b to provide a heat passage for discharging heat from the light emitting cells S1, S2. The dummy bump 145c is separated from the connector 139c by the third insulation layer 141.

[0112] The insulation layer 143 may cover side surfaces of the first and second bumps 145a, 145b. The insulation layer 143 may also cover a side surface of the dummy bump 145c. In addition, the insulation layer 143 fills spaces between the first bump 145a, the second bump

145b and the dummy bump 145c to prevent moisture from entering the semiconductor stack 130 from outside. Although the insulation layer 143 may be configured to cover the overall side surfaces of the first and second bumps 145a, 145b, the invention is not limited thereto.

Alternatively, the insulation layer 143 may cover the side surfaces of the first and second bumps 145a, 145b except for some regions of the side surface near distal ends of the first and second bumps.

[0113] The wavelength convertor 151 may be located on the light emitting cells S1, S2. The wavelength convertor 151 may contact an upper surface of the first conductive type upper semiconductor layer 125. The wavelength convertor 151 also covers a cell separation region 130b and a chip separation region. The wavelength convertor 151 may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength convertor 51 may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength conversion.

[0114] In the present embodiment, the side surfaces of the light emitting cells S1, S2 are covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer 133 and/or the second insulation layer 137. In addition, the first contact layer 135 may be covered with the second insulation layer 137 to be protected from external environment and the second contact layer 131 may be covered with the first insulation layer 133 and the second insulation layer 137 to be protected from external environment. Further, the first and second electrode pads 139a, 139b are also protected by, for example, the third insulation layer 141. Accordingly, it is possible to prevent deterioration of the light emitting cells S1, S2 due to moisture.

[0115] The wavelength convertor 151 may be attached to the first conductive type upper semiconductor layer 125 at a wafer-level, and then divided together with the protective insulation layer during a chip separation process (or package separation process). Therefore, a side surface of the wavelength convertor 151 may be in a line with the protective insulation layer. Further, the side surface of the wavelength convertor 151 may be in a line with a side surface of the insulation layer 143.

[0116] Figure 15 is a schematic sectional view of a light emitting diode package 400 according to a fourth exemplary embodiment of the present invention.

[0117] Referring to Figure 15, the LED package 400 is similar to the LED package 300 according to the above exemplary embodiment. In present exemplary embodiment, however, first and second bumps 165a, 165b are formed in a substrate 161.

[0118] Specifically, the substrate 161 includes through-holes, which have the first and second bumps 165a, 165b formed therein, respectively. The substrate 161 is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto.

[0119] The substrate 161 having the first and second bumps 165a, 165b may be attached to a third insulation layer 141, and the first and second bumps 165a, 165b may be connected to first and second electrode pads 139a, 139b, respectively. Here, the first and second bumps 165a, 165b may be bonded to additional metal layers 140a, 140b, respectively.

[0120] Figure 16 is a sectional view of a light emitting diode module including the LED packages 300 according to the third exemplary embodiment on a circuit board.

[0121] Referring to Figure 16, the LED module includes a circuit board 171, for example, an MC-PCB, the LED package 300, and a lens 181. The circuit board 171, for example, the MC-PCB, has connection pads 173a, 173b for mounting the LED packages 300 thereon. The first and

second bumps 145a, 145b (see Figure 14) of the LED package 300 are connected to the connection pads 73a, 73b, respectively.

[0122] A plurality of LED packages 300 may be mounted on the circuit board 171 and the lens 181 may be disposed on the LED packages 300 to adjust an orientation angle of light emitted from the LED packages 300.

[0123] In other exemplary embodiments, instead of the LED packages 300, the light emitting diode packages 400 may be mounted on the circuit board.

[0124] Figure 17 to Figure 25 show a method of fabricating the LED package 300 according to the third exemplary embodiment. In Figure 18 to Figure 23, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

[0125] Referring to Figure 17, a semiconductor stack 130, which includes a first conductive type semiconductor layer 125, an active layer 127 and a second conductive type semiconductor layer 129, is formed on a growth substrate 121. The growth substrate 121 and the semiconductor stack 130 are similar to the substrate 21 and the semiconductor stack 30 described with reference to Figure 4, and a detailed description thereof will thus be omitted herein.

[0126] Referring to (a) and (b) of Figure 18, the semiconductor stack 130 is patterned to form a chip (package) separation region 130c and a cell separation region 130b while patterning the second conductive type semiconductor layer 129 and the active layer 127 to form light emitting cells S1, S2, each having a plurality of contact holes 130a exposing the first conductive type semiconductor layer 125. The semiconductor stack 130 may be patterned by photolithography and etching processes.

[0127] The chip separation region 130c is a region for dividing the LED package structure into individual LED packages and side surfaces of the first conductive type

semiconductor layer 125, the active layer 127 and the second conductive type semiconductor layer 129 are exposed at the chip separation region 130c. Advantageously, the chip separation region 130c and the cell separation region 130b may be configured to expose the substrate 121 without being limited thereto.

5 **[0128]** The plurality of contact holes 130a may have a circular shape, but is not limited thereto. The contact holes 130 may have a variety of shapes. The second conductive type semiconductor layer 129 and the active layer 127 are exposed to sidewalls of the plurality of contact holes 130a. The contact holes 130a may have slanted sidewalls.

10 **[0129]** Referring to (a) and (b) of Figure 19, a second contact layer 131 is formed on the second conductive type semiconductor layer 129. The second contact layer 131 is formed on the semiconductor stack 130 in each of the light emitting cells S1, S2 except for regions corresponding to the plurality of contact holes 130a.

15 **[0130]** The second contact layer 131 may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al). The second contact layer 131 may be composed of a single layer or multiple layers. The second contact layer 131 may also be configured to form an ohmic contact with the second conductive type semiconductor layer 129.

[0131] The second contact layer 131 may be formed before or after the formation of the plurality of contact holes 130a

20 **[0132]** Referring to (a) and (b) of Figure 20, a first insulation layer 133 is formed to cover the second contact layer 131. The first insulation layer 133 may cover the side surface of each of the light emitting cells S1, S2 while covering the sidewalls of the plurality of contact

holes 130a. Here, the first insulation layer 133 may have openings 133a, which expose the first conductive type semiconductor layer 125 in the plurality of contact holes 130a.

[0133] The first insulation layer 133 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. In addition, the first insulation layer 133 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction. For example, the first insulation layer 133 may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$. Further, the first insulation layer 133 may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

[0134] Referring to (a) and (b) of Figure 21, a first contact layer 135 is formed on the first insulation layer 133. The first contact layer 135 is formed on each of the light emitting cells S1, S2, and includes contact sections 35a contacting the first conductive type upper semiconductor layer 125 exposed in the contact holes 130a and a connecting section 135b connecting the contact sections 135a to each other. The first contact layer 135 may be composed of a reflective metal layer, but is not limited thereto.

[0135] The first contact layer 135 is formed on some regions of each of the light emitting cells S1, S2, so that the first insulation layer 133 is exposed at other regions of the semiconductor stack 130 where the first contact layer 135 is not formed.

[0136] Referring to (a) and (b) of Figure 22, a second insulation layer 137 is formed on the first contact layer 135. The second insulation layer 137 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the second insulation

layer 137 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

[0137] The second insulation layer 137 may cover the first contact layer 135 while covering the first insulation layer 133. The second insulation layer 137 may also cover the side surface of the each of the light emitting cells S1, S2. In addition, the second insulation layer 137 may fill in the chip separation region 130c and the cell separation region 130b.

[0138] The second insulation layer 137 has an opening 137a which exposes the first contact layer 135 of each of the light emitting cells S1, S2. Further, the second insulation layer 137 and the first insulation layer 133 are formed with an opening 137b, which exposes the second contact layer 131.

[0139] Referring to (a) and (b) of Figure 23, a connector 139c and first and second electrode pads 139a, 139b are formed on the second insulation layer 137. The first electrode pad 139a is connected to the first contact layer 135 of a first light emitting cell S1 through the opening 137a and the second electrode pad 139b is connected to the second contact layer 131 of a second light emitting cell S2 through the opening 137b. Further, the connector 139c connects the first contact layer 135 and the second contact layer 131 of adjacent light emitting cells S1, S2 to each other in series through the openings 137a, 137b.

[0140] Referring to Figure 24, a third insulation layer 141 is formed on the first and second electrode pads 139a, 139b and the connector 139c. The third insulation layer 141 covers the first and second electrode pads 139a, 139b and the connector 139c, and has grooves which expose upper surfaces of the electrode pads 139a, 139b. Meanwhile, the third insulation layer 141 may have additional metal layers 140a, 140b formed in the grooves thereof. The additional metal layers 140a, 140b increase the height of the electrode pads 139a, 139b, such that final

electrode pads may have a greater height than the connector 139c. The additional metal layers 140a, 140b may be formed before the formation of the third insulation layer 141. Upper surfaces of the additional metal layers 140a, 140b may be substantially coplanar with an upper surface of the third insulation layer 141.

5 **[0141]** Referring to Figure 25, a patterned insulation layer 143 is formed on the third insulation layer 141. The patterned insulation layer 143 has grooves, which expose the upper side of the first and second electrode pads 139a, 139b, for example, the additional metal layers 140a, 140b. Further, the patterned insulation layer 143 may have a groove exposing the third insulation layer 141 between the first electrode pad 139a and the second electrode pad 139b.

10 **[0142]** Then, first and second bumps 145a, 145b are formed in the grooves of the insulation layer 143 and a dummy bump 145c may be formed between the first and second bumps.

[0143] The bumps may be formed by plating, for example, electroplating. As needed, a seed layer for plating may also be formed.

15 **[0144]** After the first and second bumps 145a, 145b are formed, the insulation layer 143 may be removed. For example, the insulation layer 143 may be formed of a polymer such as photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer 143 may remain to protect the side surfaces of the first and second bumps 145a, 145b.

[0145] Referring to Figure 26, the growth substrate 121 is removed and a wavelength
20 converter 151 is attached to the light emitting cells S1, S2. The growth substrate 21 may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

[0146] Then, the exposed surface of the first conductive type semiconductor layer 125 is subjected to anisotropic etching such as PEC etching to form a roughened surface on the exposed first conductive type semiconductor layer 125.

[0147] Meanwhile, the wavelength convertor 151, such as a phosphor sheet containing phosphors, may be attached to the first conductive type semiconductor layer 125

[0148] Alternatively, the growth substrate 121 may contain an impurity for converting a wavelength of light generated in the active layer 127. In this case, the growth substrate 121 may be used as the wavelength convertor 151.

[0149] Then, the LED package structure is divided into individual packages along the chip separation region 130c, thereby providing finished LED packages 300. At this time, the second insulation layer 137 is cut together with the wavelength convertor 151 so that cut planes thereof can be formed in a line.

[0150] Figure 27 is a sectional view explaining a method of fabricating the LED package 400 according to the fourth exemplary embodiment of the invention.

[0151] Referring to Figure 27, in the method of fabricating the LED package 400 according to this embodiment, the processes until the third insulation layer 141 and the additional metal layers 140a, 140b are formed are the same as those of the method of fabricating the LED package 300 described above (Figure 24).

[0152] In the present exemplary embodiment, the substrate 161 is bonded to the third insulation layer 141. The substrate 161 may have through-holes, in which the first and second bumps 165a, 165b may be formed. Further, the first and second bumps 165a, 165b may be formed at distal ends thereof with pads (not shown). In addition, the substrate 161 may have

grooves partially formed on a lower surface thereof and filled with a metallic material 165c. The metallic material 165c improves substrate heat dissipation.

[0153] Alternatively, the substrate 161 having the first and second bumps 165a, 165b may be separately prepared and bonded to a wafer having the first and second electrode pads 139a, 139b. The first and second bumps 165a, 165b may be electrically connected to first and second electrode pads 139a, 139b, respectively.

[0154] Then, as described with reference to Figure 26, the growth substrate 121 is removed and the wavelength converter 151 may be attached to the light emitting cells S1, S2, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages 400 as described in Figure 15 are provided.

[0155] As such, the exemplary embodiments of the invention provide wafer-level LED packages which can be directly formed on a circuit board for a module without using a conventional lead frame or printed circuit board. Accordingly, the LED package may have high efficiency and exhibit improved heat dissipation while reducing time and cost for fabrication of the LED package. In addition, an LED module having the LED package mounted thereon may have high efficiency and exhibit improved heat dissipation.

[0156] Further, the LED package may include a plurality of light emitting cells connected in series to each other and arrays connected in reverse parallel to each other. Further, the plurality of light emitting cells may be connected to a bridge rectifier and may be used to form a bridge rectifier. Therefore, the LED module including the LED package may be operated by AC power without a separate AC/DC converter.

[0157] Although the invention has been illustrated with reference to some exemplary embodiments in conjunction with the drawings, it will be apparent to those skilled in the art that

various modifications and changes can be made to the invention without departing from the spirit and scope of the invention. Further, it should be understood that some features of a certain embodiment may also be applied to other embodiment without departing from the spirit and scope of the invention. Therefore, it should be understood that the embodiments are provided by way of illustration only and are given to provide complete disclosure of the invention and to provide thorough understanding of the invention to those skilled in the art. Thus, it is intended that the invention covers the modifications and variations provided they fall within the scope of the appended claims and their equivalents.

WHAT IS CLAIMED IS:

- 1 1. A light emitting diode (LED) package, comprising:
2 a semiconductor stack comprising a first conductive type semiconductor layer, an active
3 layer, and a second conductive type semiconductor layer;
4 a plurality of contact holes arranged in the second conductive type semiconductor layer
5 and the active layer, the contact holes exposing the first conductive type semiconductor layer;
6 a first bump arranged on a first side of the semiconductor stack, the first bump being
7 electrically connected to the first conductive type semiconductor layer via the plurality of contact
8 holes;
9 a second bump arranged on the first side of the semiconductor stack, the second bump
10 being electrically connected to the second conductive type semiconductor layer; and
11 a protective insulation layer covering a sidewall of the semiconductor stack.
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1 2. The LED package of claim 1, further comprising a wavelength converter arranged
2 on a second side of the semiconductor stack, the second side being opposite to the first side of
3 the semiconductor stack.
1

1 3. The LED package of claim 2, wherein the wavelength converter comprises a
2 phosphor sheet or an impurity-doped single crystal substrate.
1

1 4. The LED package of claim 2, wherein the wavelength converter comprises a side
2 surface flush with a side surface of the protective insulation layer.
1

1 5. The LED package of claim 1, wherein the protective insulation layer comprises a
2 distributed Bragg reflector.

1 6. The LED package of claim 1, wherein the first conductive type semiconductor
2 layer comprises a roughened surface.

1 7. The LED package of claim 1, further comprising an insulation layer arranged on
2 side surfaces of the first bump and the second bump.

1 8. The LED package of claim 7, further comprising a dummy bump arranged
2 between the first bump and the second bump.

1 9. The LED package of claim 1, further comprising a substrate comprising a first
2 through-hole and a second through-hole, the first bump and the second bump being arranged in
3 the first through-hole and the second through-hole, respectively.

1 10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.

1 11. The LED package of claim 1, further comprising:
2 a first contact layer comprising first contact sections contacting the first conductive type
3 semiconductor layer in the plurality of contact holes and a connecting section connecting the first
4 contact sections to each other; and
5 a second contact layer contacting the second conductive type semiconductor layer,

6 wherein the protective insulation layer comprises a first insulation layer and a second
7 insulation layer, the first insulation layer being arranged between the first contact layer and the
8 second contact layer and covering the second contact layer, and the second insulation layer being
9 arranged between the semiconductor stack and the first contact layer and covering the first
10 contact layer,

11 wherein the first bump is electrically connected to the first contact layer, and the second
12 bump is electrically connected to the second contact layer.

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1 12. The LED package of claim 11, further comprising:
2 a first electrode pad contacting the first contact layer through a first contact hole arranged
3 in the second insulation layer; and
4 a second electrode pad contacting the second contact layer through a second contact hole
5 arranged in the second insulation layer and the first insulation layer,

6 wherein the first bump and the second bump contact the first electrode pad and the
7 second electrode pad, respectively.

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1 13. The LED package of claim 11, wherein at least one of the first insulation layer
2 and the second insulation layer comprises a distributed Bragg reflector.

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1 14. A light emitting diode (LED) module, comprising:
2 a circuit board;
3 the LED package of claim 1 arranged on the circuit board; and
4 a lens to adjust an orientation angle of light emitted from the LED package.

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1 15. The LED module of claim 14, wherein the circuit board comprises a metal core
2 printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-
3 PCB.

1 16. A method of fabricating a light emitting diode (LED) package, the method
2 comprising:
3 forming a semiconductor stack on a first substrate, the semiconductor stack comprising a
4 first conductive type semiconductor layer, an active layer, and a second conductive type
5 semiconductor layer;
6 patterning the semiconductor stack to form a chip separation region;
7 patterning the second conductive type semiconductor layer and the active layer to form a
8 plurality of contact holes exposing the first conductive type semiconductor layer;
9 forming a protective insulation layer covering a sidewall of the semiconductor stack in
10 the chip separation region; and
11 forming a first bump and a second bump on the semiconductor stack,
12 wherein the first bump is electrically connected to the first conductive type
13 semiconductor layer via the plurality of contact holes, and the second bump is electrically
14 connected to the second conductive type semiconductor layer.

1 17. The method of claim 16, wherein the first substrate comprises an impurity for
2 converting a wavelength of light generated in the active layer.

1 18. The method of claim 16, further comprising:

removing the first substrate to expose the first conductive type semiconductor layer; and
attaching a phosphor sheet to the exposed first conductive type semiconductor layer.

19. The method of claim 16, wherein forming the protective insulation layer
comprises forming a first insulation layer and a second insulation layer.

20. The method of claim 19, further comprising:
forming a second contact layer on the second conductive type semiconductor layer;
forming the first insulation layer to cover the second contact layer and sidewalls of the
plurality of contact holes, the first insulation layer comprising openings exposing the first
conductive type semiconductor layer in the plurality of contact holes;
forming a first contact layer on the first insulation layer, the first contact layer
comprising:
contact sections contacting the first conductive type semiconductor layer exposed
in the plurality of contact holes; and
a connecting section connecting the contact sections to each other;
forming the second insulation layer to cover the first contact layer;
patterning the first insulation layer and the second insulation layer to form an opening
exposing the first contact layer;
forming an opening exposing the second contact layer; and
forming a first electrode pad and a second electrode pad on the second insulation layer,
the first electrode pad and the second electrode pad to be respectively connected to the first
contact layer and the second contact layer through the openings,

18 wherein the first bump and the second bump are electrically connected to the first
19 electrode pad and the second electrode pad, respectively.

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1 21. The method of claim 20, wherein forming the first bump and the second bump
2 comprises forming an insulation layer pattern having openings exposing regions of the first
3 electrode pad and the second electrode pad, and plating the exposed regions of the first electrode
4 pad and the second electrode pad with a metallic material.

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1 22. The method of claim 21, further comprising:
2 forming a dummy bump between the first bump and the second bump.

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1 23. The method of claim 20, further comprising bonding a second substrate on the
2 first electrode pad and the second electrode pad before forming the first bump and the second
3 bump, wherein forming the first bump and the second bump comprises forming a plurality of
4 through-holes in the second substrate, filling the through-holes with a metallic material, and
5 bonding the metallic material to the first electrode pad and the second electrode pad.

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1 24. The method of claim 23, further comprising: before bonding the second substrate,
2 forming an insulation layer covering the first electrode pad and the second electrode pads, and
3 patterning the insulation layer to expose the first electrode pad and the second electrode pad.

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1 25. A light emitting diode (LED) package, comprising:
2 a plurality of light emitting cells each comprising a first conductive type semiconductor

3 layer, an active layer, and a second conductive type semiconductor layer;

4 a plurality of contact holes arranged in the second conductive type semiconductor layer
5 and the active layer of each of the light emitting cells, the contact holes exposing the first
6 conductive type semiconductor layer of each of the light emitting cells;

7 a protective insulation layer covering a sidewall of each of the light emitting cells;

8 a connector located arranged on a first side of the light emitting cells and electrically
9 connecting two adjacent light emitting cells to each other;

10 a first bump arranged on the first side of the light emitting cells and electrically
11 connected to the first conductive type semiconductor layer via the plurality of contact holes of a
12 first light emitting cell of the light emitting cells; and

13 a second bump arranged on the first side of the light emitting cells and electrically
14 connected to the second conductive type semiconductor layer of a second light emitting cell of
15 the light emitting cells.

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1 26. The LED package of claim 25, further comprising a wavelength converter
2 arranged on a second side of the plurality of light emitting cells, the second side being opposite
3 to the first side of the plurality of light emitting cells.

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1 27. The LED package of claim 26, wherein the wavelength converter comprises a
2 phosphor sheet or an impurity-doped single crystal substrate.

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1 28. The LED package of claim 26, wherein the wavelength converter has a side
2 surface flush with a side surface of the protective insulation layer.

1 29. The LED package of claim 25, wherein the protective insulation layer comprises a
2 distributed Bragg reflector.

1 30. The LED package of claim 25, wherein the first conductive type semiconductor
2 layer of each of the light emitting cells comprises a roughened surface.

1 31. The LED package of claim 25, further comprising an insulation layer arranged on
2 side surfaces of the first bump and the second bump.

1 32. The LED package of claim 31, further comprising a dummy bump arranged
2 between the first bump and the second bump.

1 33. The LED package of claim 25, further comprising a substrate comprising a first
2 through-hole and a second through-hole, the first bump and the second bump being arranged in
3 the first through-hole and the second through-hole, respectively.

1 34. The LED package of claim 33, wherein the substrate comprises grooves arranged
2 in a lower surface thereof and filled with a metallic material.

1 35. The LED package of claim 25, further comprising:
2 a first contact layer comprising first contact sections contacting the first conductive type
3 semiconductor layer of each of the light emitting cells in the plurality of contact holes and a
4 connecting section connecting the first contact sections to each other; and

5 a second contact layer contacting the second conductive type semiconductor layer of each
6 of the light emitting cells,

7 wherein the protective insulation layer comprises a first insulation layer and a second
8 insulation layer, the first insulation layer being arranged between the first contact layer and the
9 second contact layer and covering the second contact layer, and a second insulation layer being
10 arranged between the semiconductor stack and the first contact layer and covering the first
11 contact layer,

12 wherein the connector is arranged directly under the second insulation layer, the
13 connector to connect the first contact layer and the second contact layer to each other, the first
14 bump contacting the first contact layer of the first light emitting cell, and the second bump is
15 contacting the second contact layer of the second light emitting cell.

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2 36. The LED package of claim 35, further comprising:

3 a first electrode pad contacting the first contact layer of the first light emitting cell
4 through a first contact hole arranged in the second insulation layer; and

5 a second electrode pad contacting the second contact layer of the second light emitting
6 cell through a second contact hole arranged in the second insulation layer and the first insulation
7 layer,

8 wherein the first bump and the second bump contact the first electrode pad and the
9 second electrode pad, respectively.

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2 37. The LED package of claim 36, wherein the connector is arranged at a same level
3 as the first electrode pad and the second electrode pad.

1 38. The LED package of claim 36, further comprising a third insulation layer being
2 arranged between the dummy bump and the connector.

1 39. The LED package of claim 35, wherein at least one of the first insulation layer
2 and second insulation layer comprises a distributed Bragg reflector.

1 40. A light emitting diode module, comprising:
2 a circuit board;
3 the LED package of claim 25 arranged on the circuit board; and
4 a lens to adjust an orientation angle of light emitted from the LED package.

1 41. The LED module of claim 40, wherein the circuit board comprises a metal core
2 printed circuit board (MC-PCB), and a plurality of the LED packages are mounted on the MC-
3 PCB.

1 42. A method of fabricating a light emitting diode (LED) package, the method
2 comprising:
3 forming a semiconductor stack on a first substrate, the semiconductor stack comprising a
4 first conductive type semiconductor layer, an active layer, and a second conductive type
5 semiconductor layer;
6 patterning the semiconductor stack to form a chip separation region and a light emitting
7 cell separation region;
8 patterning the second conductive type semiconductor layer and the active layer to form a

9 plurality of light emitting cells, each light emitting cell comprising a plurality of contact holes
10 exposing the first conductive type semiconductor layer;
11 forming a protective insulation layer covering a sidewall of the semiconductor stack in
12 the chip separation region and the light emitting cell separation region;
13 forming a connector connecting adjacent light emitting cells to each other in series; and
14 forming a first bump and a second bump on the plurality of light emitting cells,
15 wherein the first bump is electrically connected to the first conductive type
16 semiconductor layer via the plurality of contact holes of a first light emitting cell of the light
17 emitting cells, and the second bump being electrically connected to the second conductive type
18 semiconductor layer of a second light emitting cell of the light emitting cells.

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1 43. The method of claim 42, wherein the first substrate comprises an impurity for
2 converting a wavelength of light generated in the active layer

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1 44. The method of claim 42, further comprising:
2 removing the first substrate to expose the light emitting cells; and
3 attaching a phosphor sheet to the exposed light emitting cells.

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1 45. The method of claim 42, wherein forming the protective insulation layer
2 comprises forming a first insulation layer and a second insulation layer.

1

1 46. The method of claim 45, further comprising:
2 forming a second contact layer on the second conductive type semiconductor layer of

each of the light emitting cells;

forming the first insulation layer to cover the second contact layer of each of the light emitting cells and sidewalls of the plurality of contact holes, the first insulation layer comprising openings exposing the first conductive type semiconductor layer in the plurality of contact holes;

forming a first contact layer on the first insulation layer of each of the light emitting cells, the first contact layer comprising:

contact sections contacting the first conductive type semiconductor layer exposed in the plurality of contact holes; and

a connecting section connecting the contact sections to each other;

forming the second insulation layer to cover the first contact layer of each of the light emitting cells;

patterning the first insulation layer and the second insulation layer of each of the light emitting cells to form an opening exposing the first contact layer;

forming an opening exposing the second contact layer; and

forming a first electrode pad and a second electrode pad on the second insulation layer, the first electrode pad and the second electrode pad to be respectively connected to the first contact layer of the first light emitting cell and the second contact layer of the second light emitting cell through the openings,

wherein the connector is formed on the second insulation layer and contacts the first contact layer and second contact layer of each of the adjacent light emitting cells through the openings, and the first bump and the second bump are electrically connected to the first electrode pad and the second electrode pad, respectively.

1 47. The method of claim 46, wherein forming the first bump and the second bump
2 comprises forming an insulation layer pattern having openings exposing regions of the first
3 electrode pad and the second electrode pad, and plating the exposed regions of the first electrode
4 pad and the second electrode pad with a metallic material.

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1 48. The method of claim 47, further comprising:
2 forming a dummy bump between the first bump and the second bump.

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1 49. The method of claim 48, further comprising: before forming the dummy bump,
2 forming a third insulation layer to cover the first electrode pad, the second electrode pad, and the
3 connector, and patterning the third insulation layer to expose the first electrode pad and the
4 second electrode pad.

1
1 50. The method of claim 46, wherein forming the first bump and the second bump
2 comprises forming a plurality of through-holes in the insulation substrate, filling the through-
3 holes with a metallic material, and bonding the metallic material to the first electrode pad and the
4 second electrode pad.

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1 51. The method of claim 50, further comprising: before forming the dummy bump,
2 forming a third insulation layer to cover the first electrode pad, the second electrode pad, and the
3 connector, and patterning the third insulation layer to expose the first electrode pad and the
4 second electrode pad.

ABSTRACT

Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

Figure 1

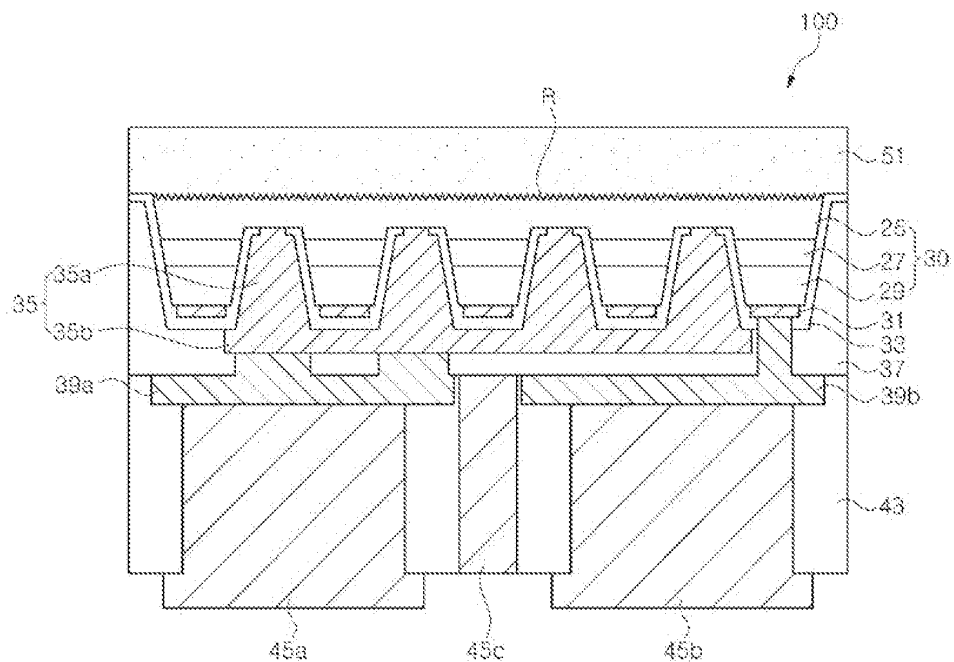


Figure 2

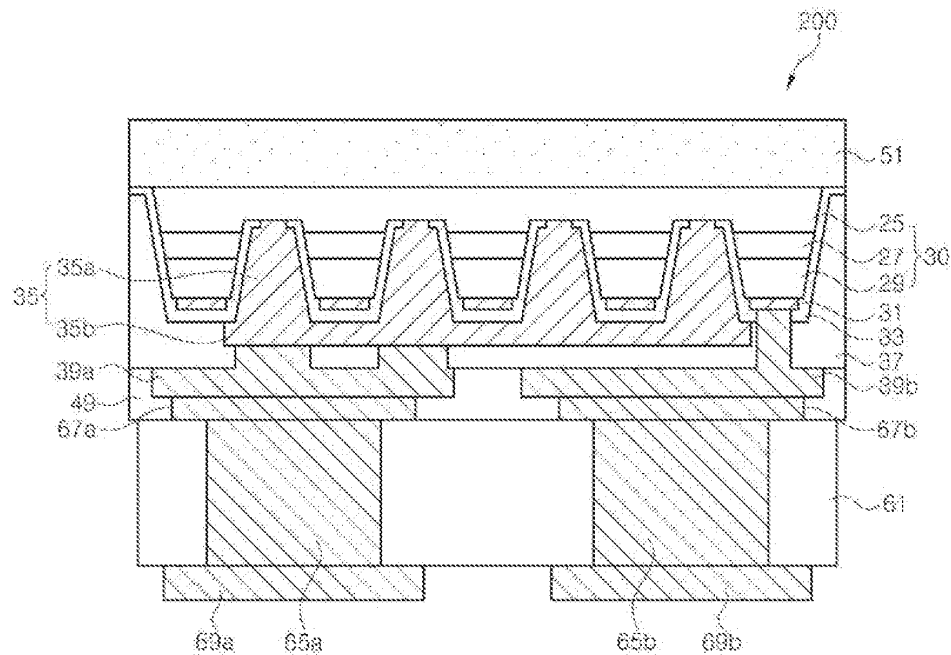


Figure 3

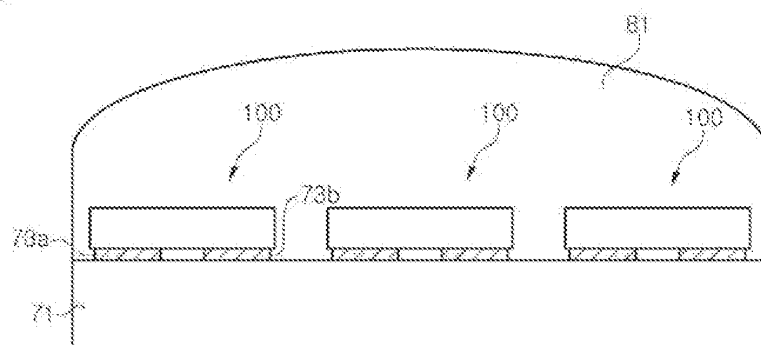


Figure 4

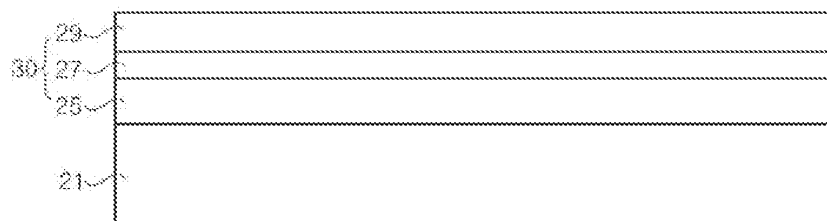


Figure 5

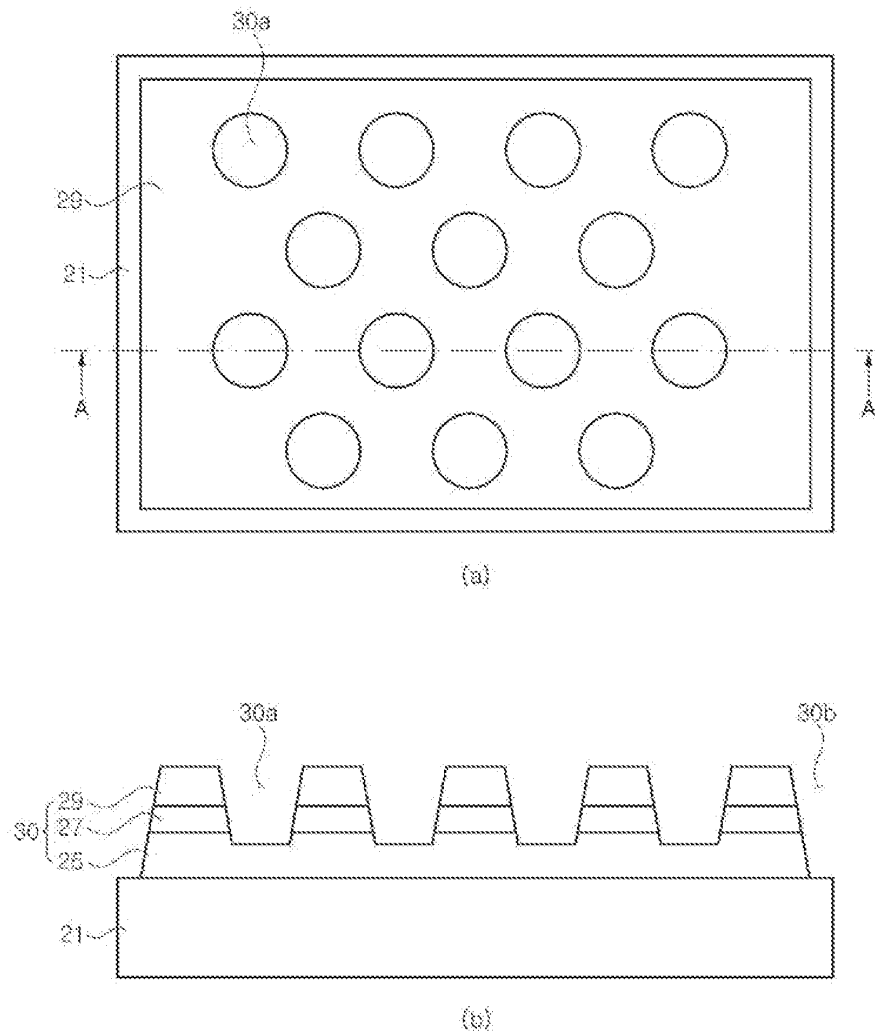


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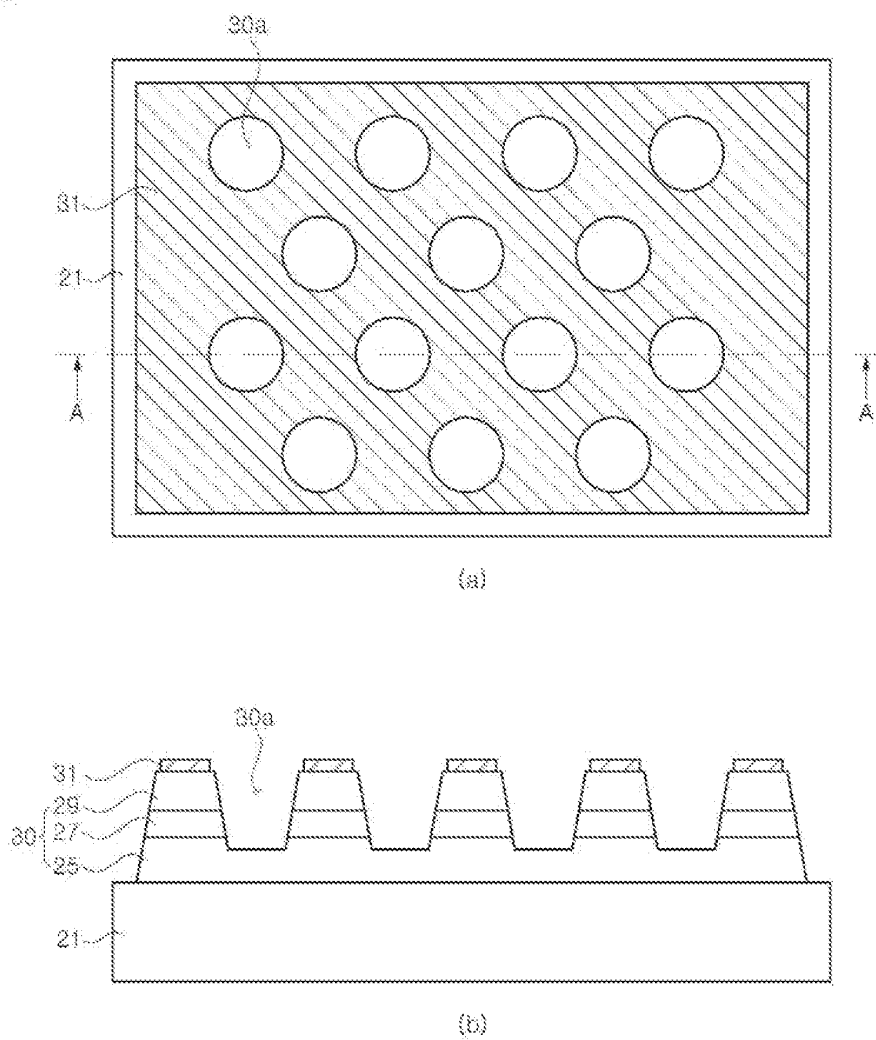


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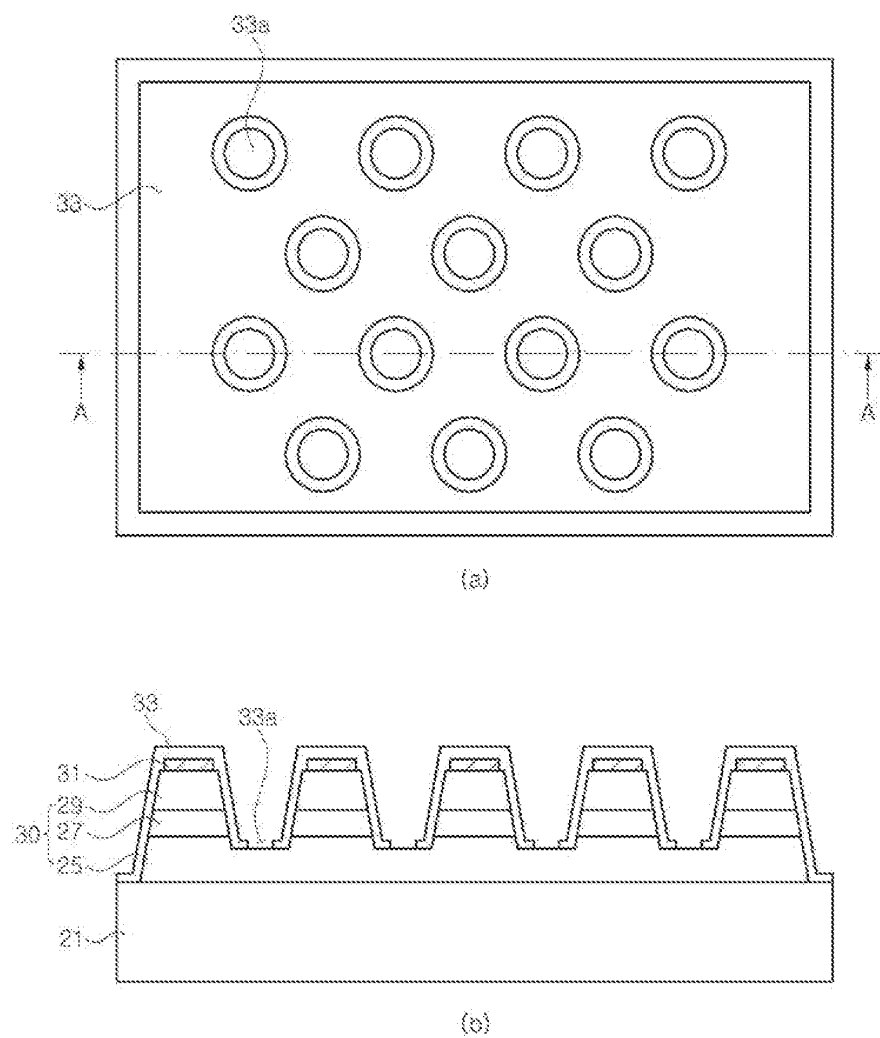


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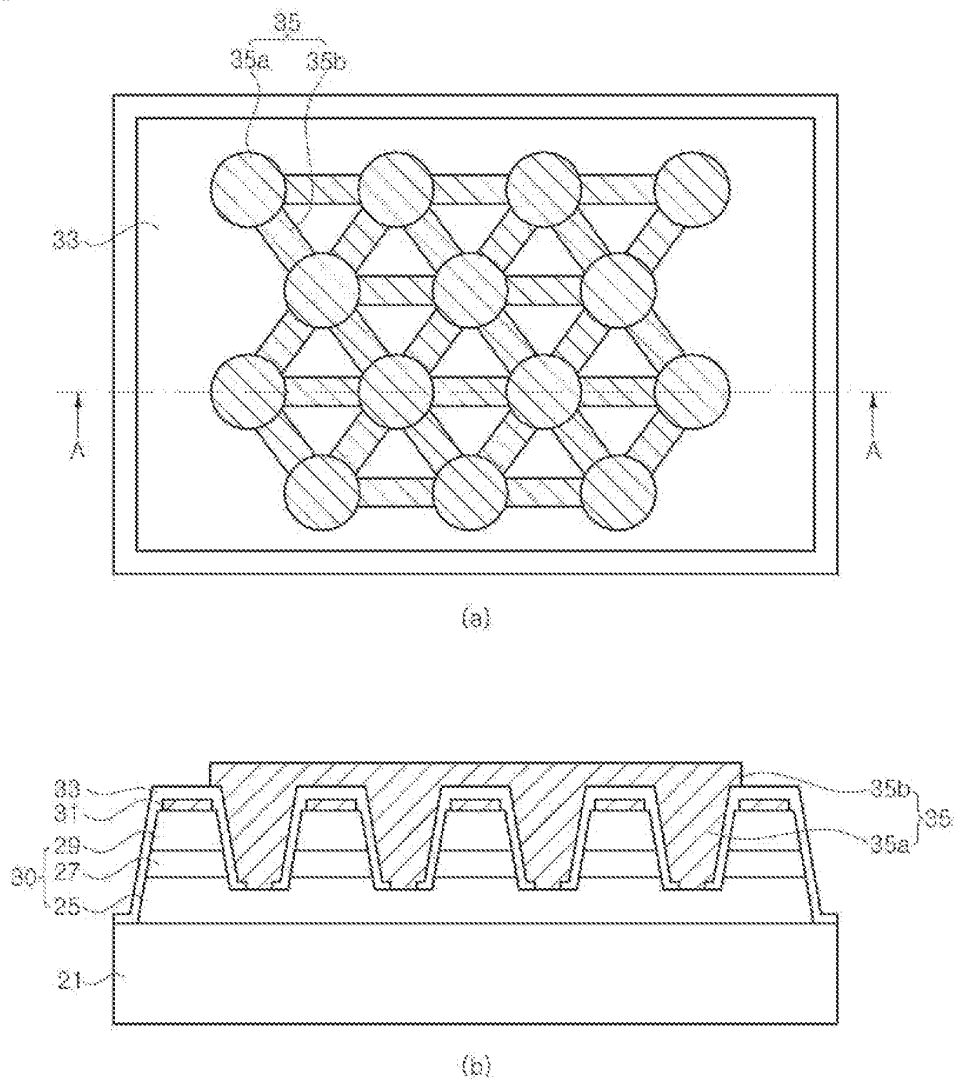


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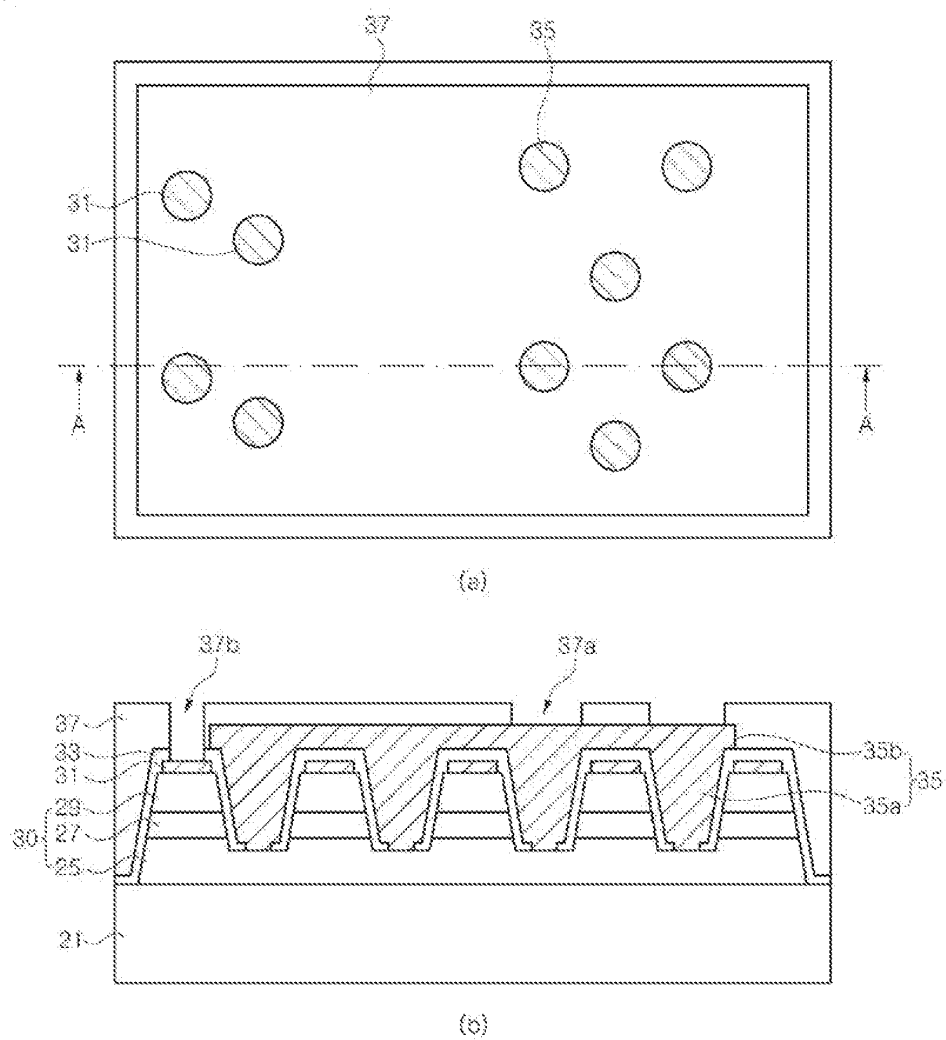


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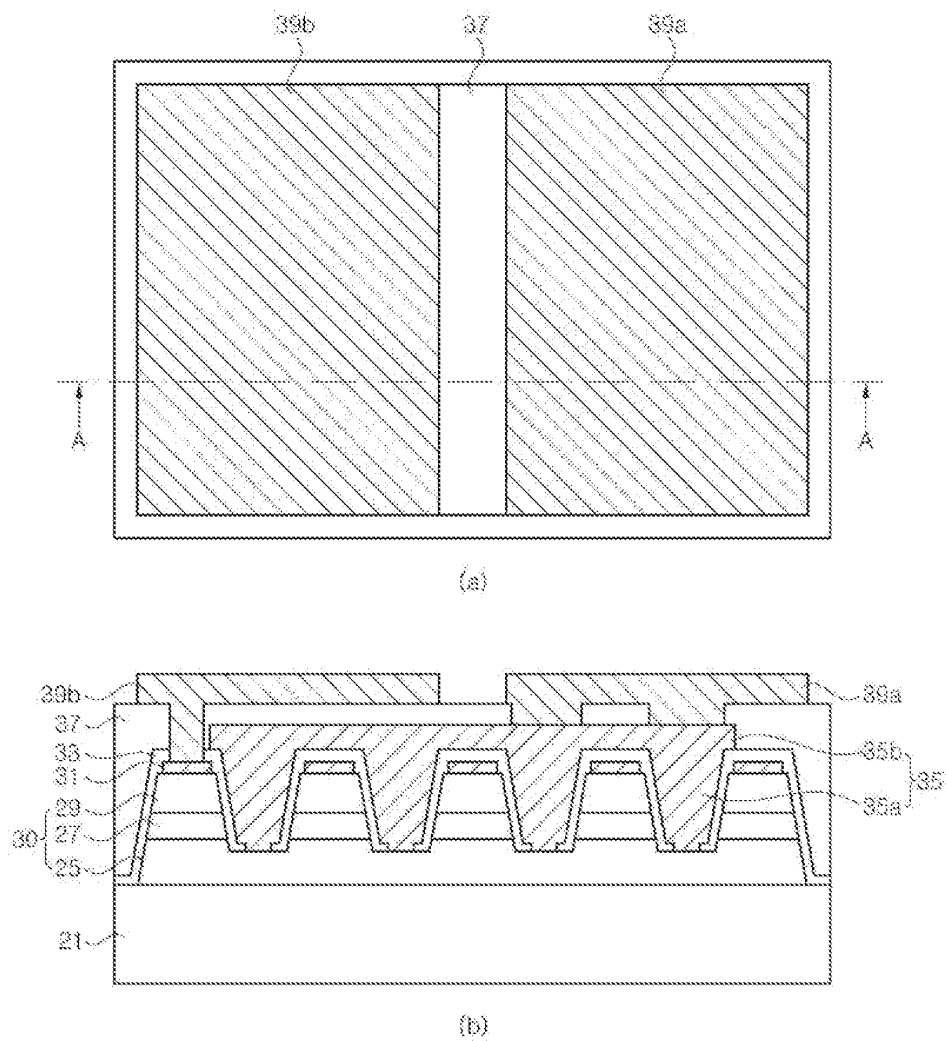


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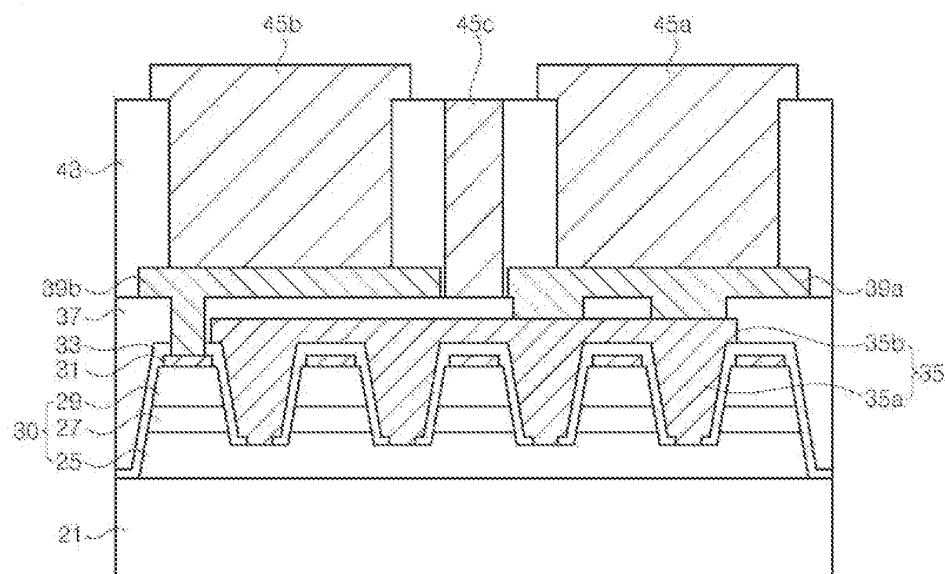


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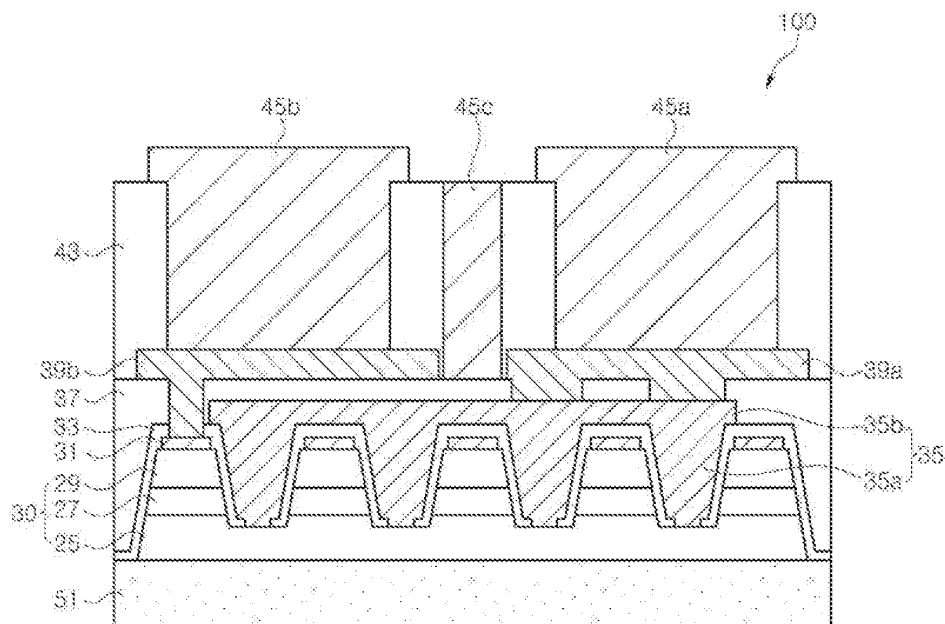


Figure 13

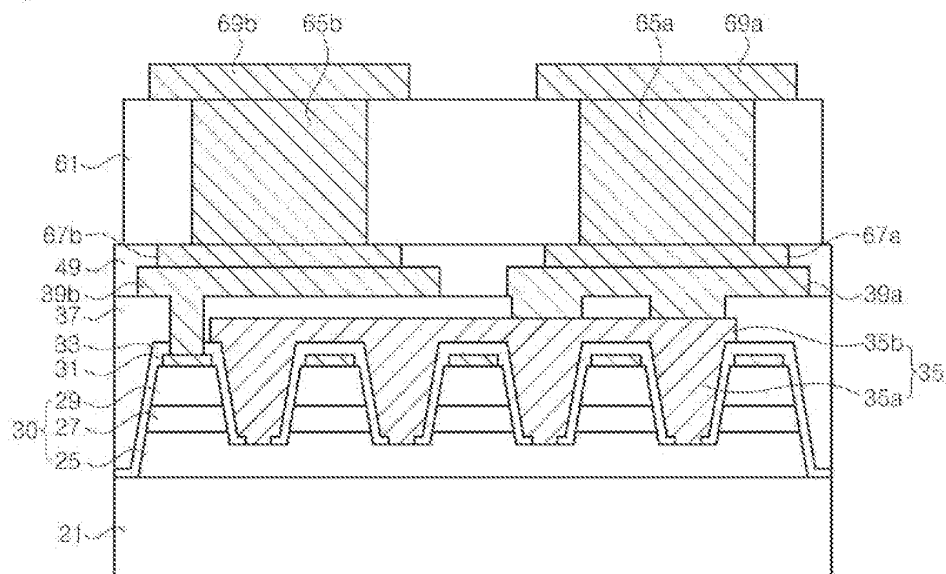


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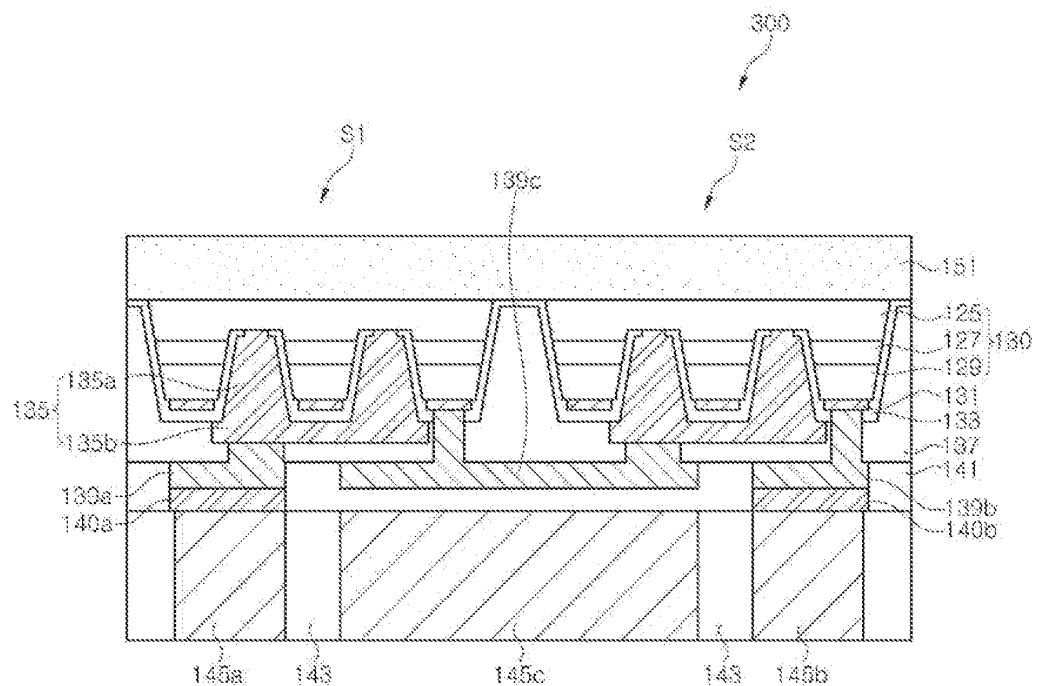


Figure 15

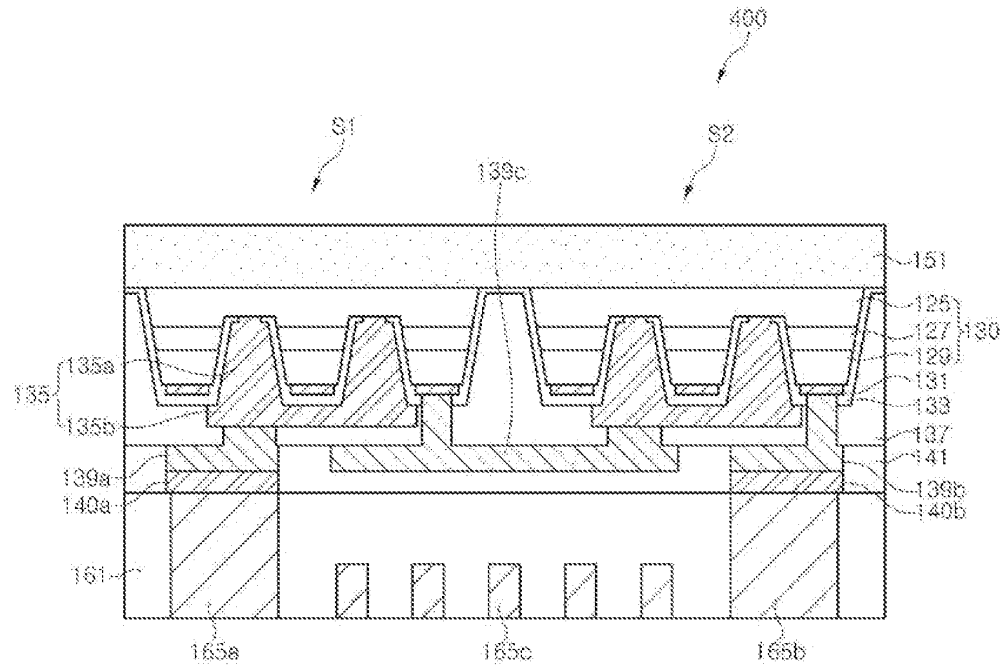


Figure 16

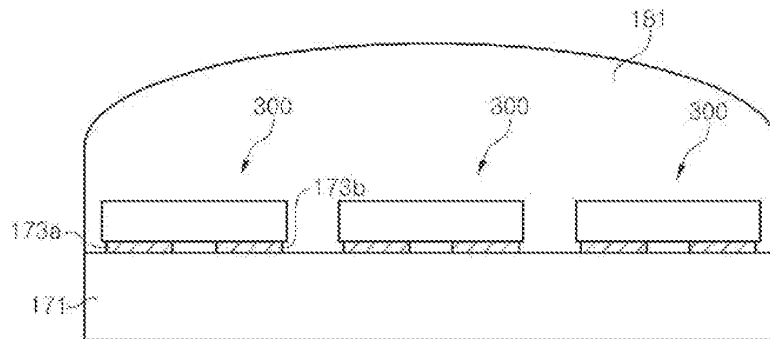


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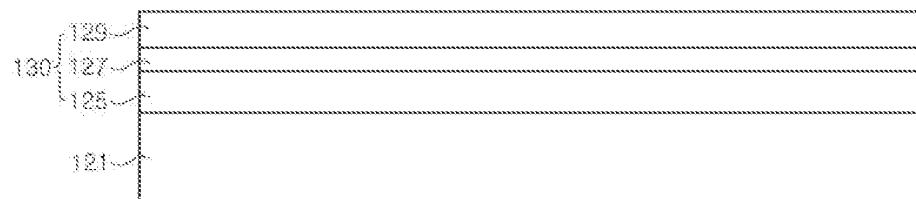


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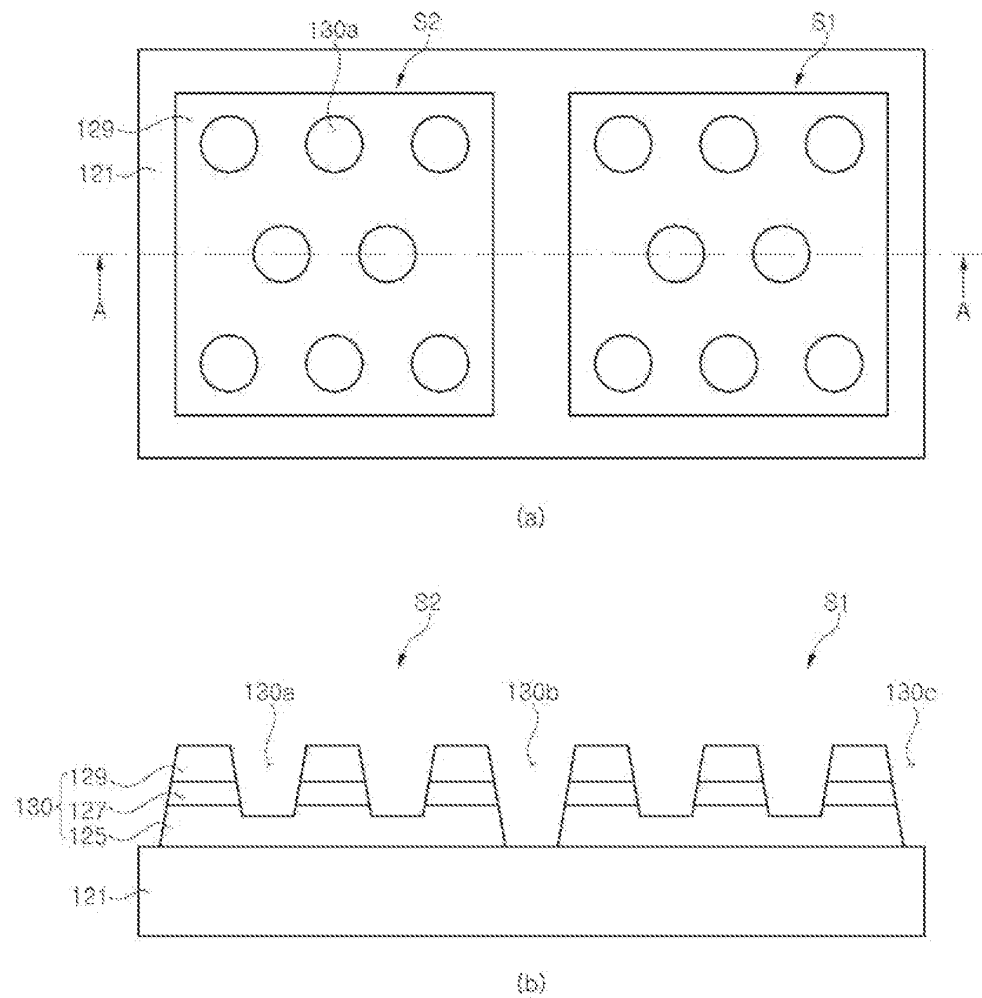


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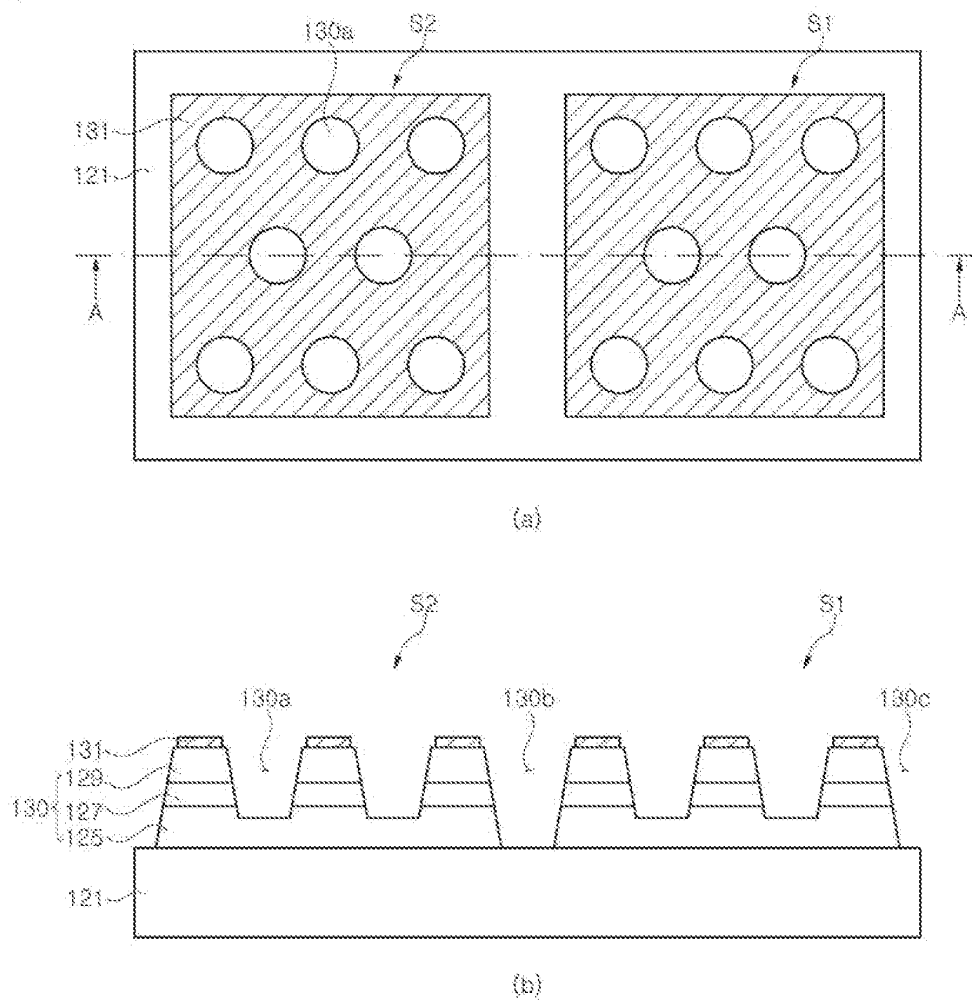


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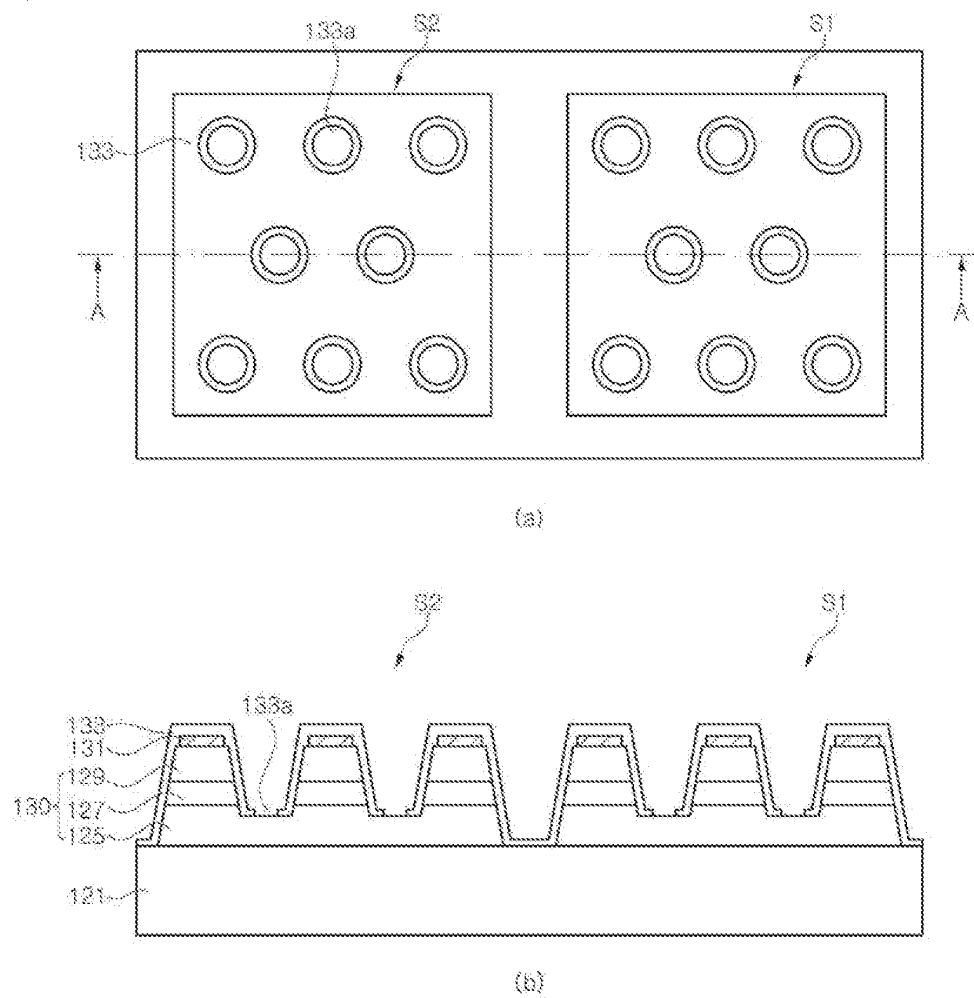


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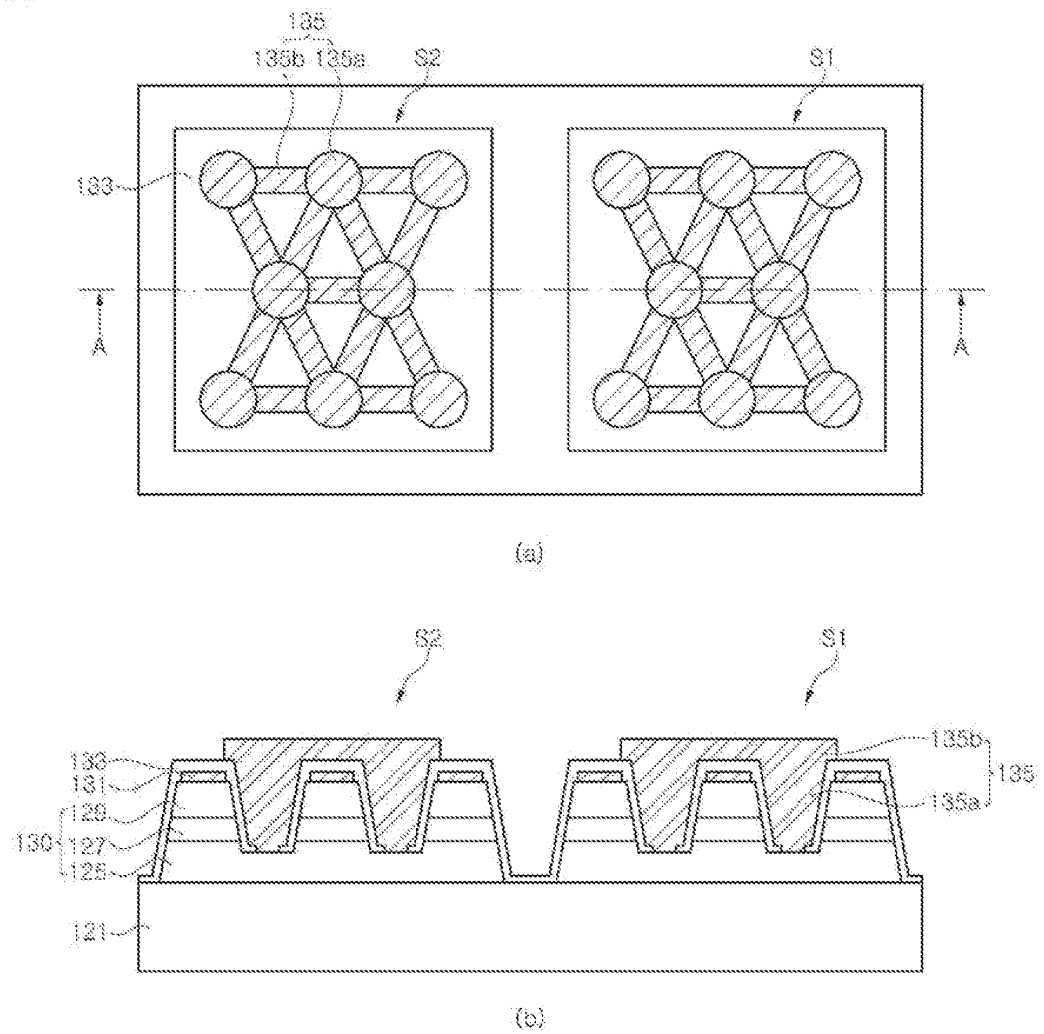


Figure 22

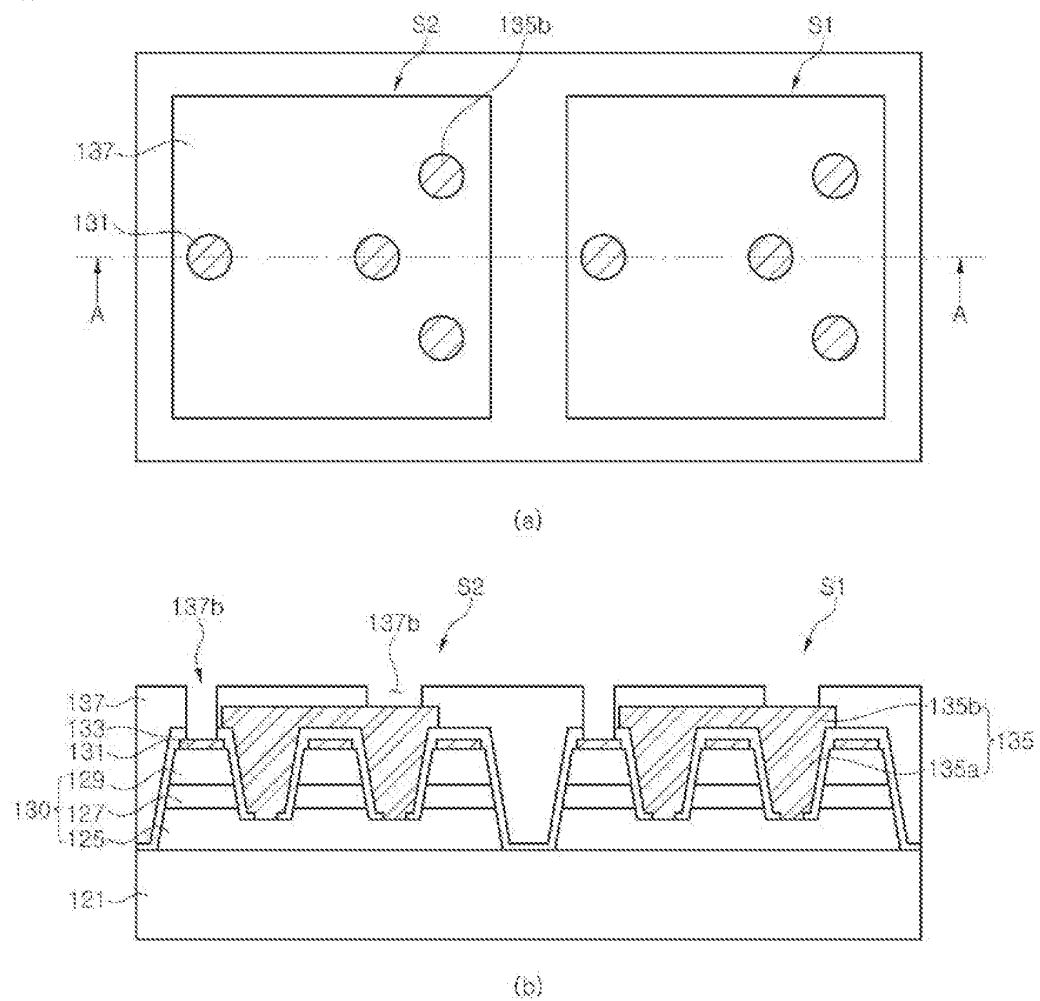


Figure 23

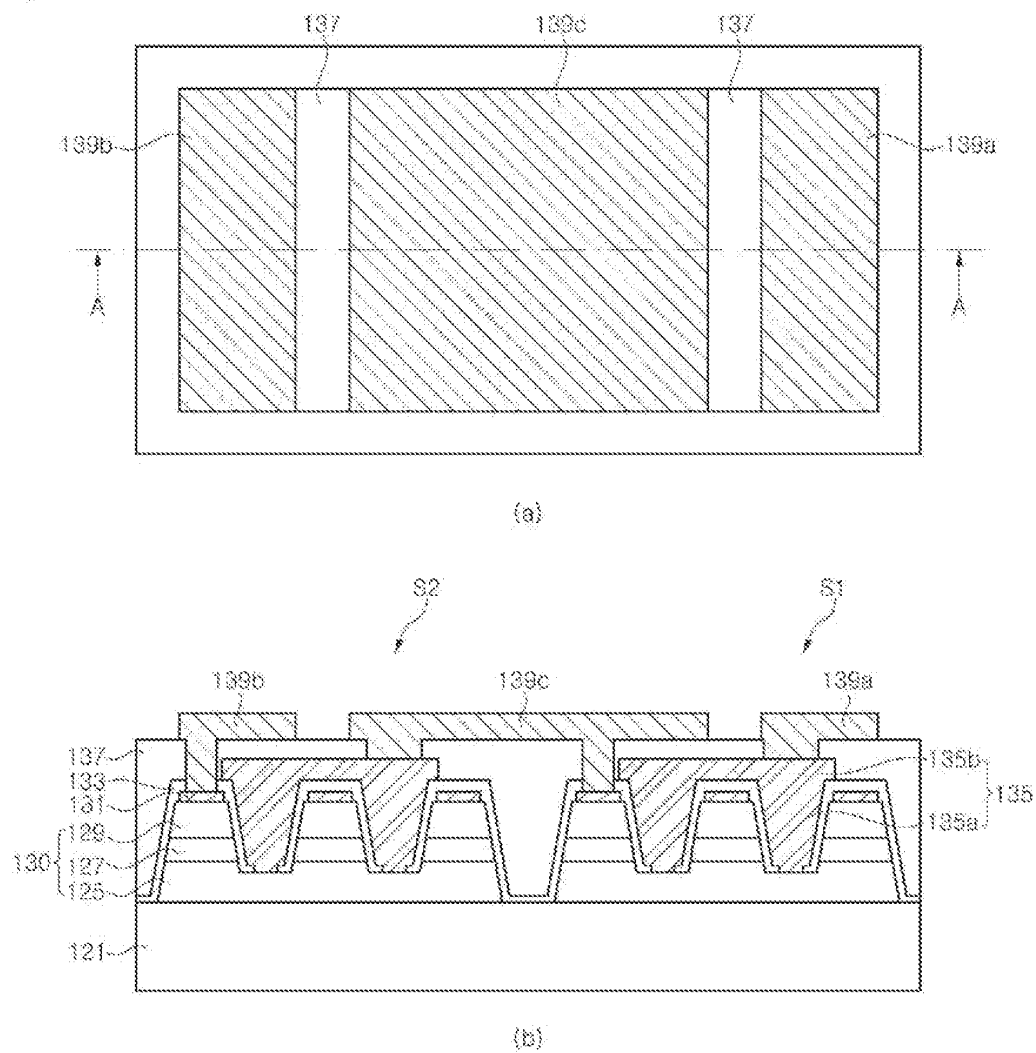


Figure 26

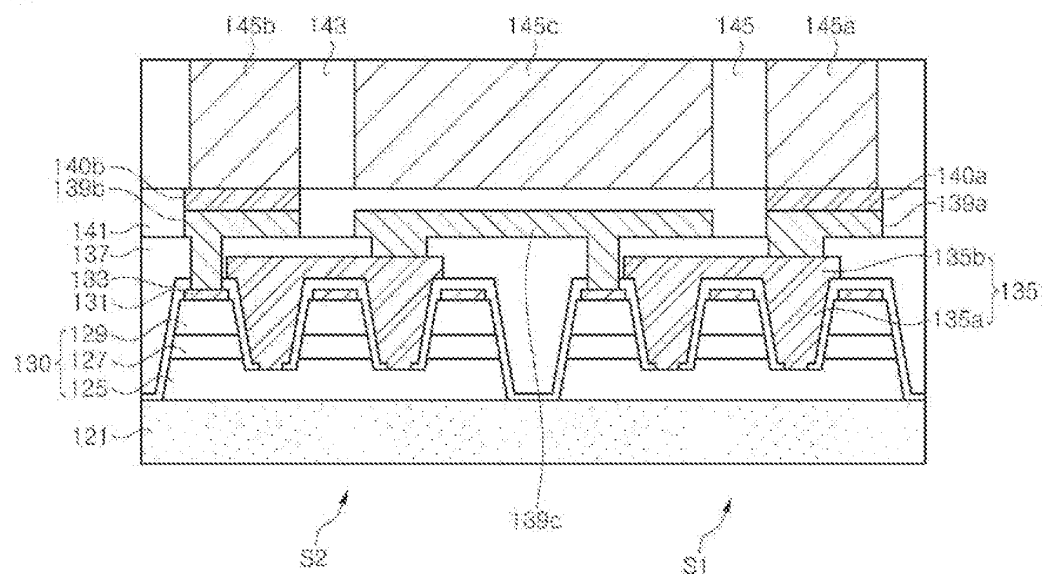
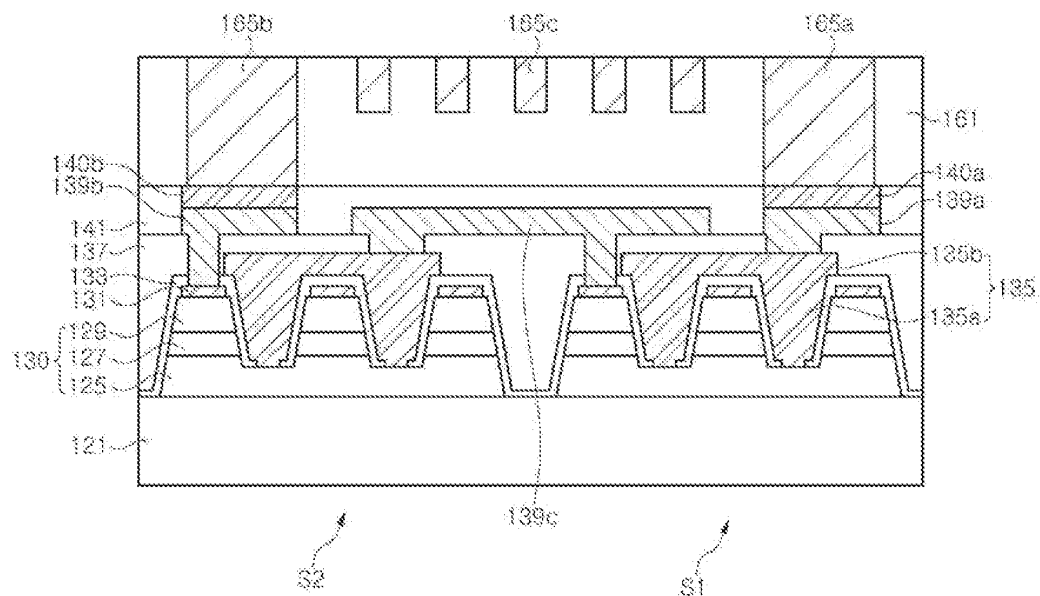


Figure 27



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Won Cheol Seo et al.

Application No.: Not yet assigned

Confirmation No.: Not yet assigned

Filed: Herewith

Examiner: Not yet assigned

For: WAFER-LEVEL LIGHT EMITTING DIODE
PACKAGE AND METHOD OF FABRICATING THE
SAME

Art Unit: Not yet assigned

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

Amendments to the Specification begin on page **2** of this paper.

Amendments to the Claims begin on page **3** of this paper.

Remarks/Arguments begin on page **8** of this paper.

Applicants: Won Cheol Seo et al.
Appl. No. : Not yet assigned
Filed : Herewith
Page : 2 of 8

Docket No. 114896-8005.US02

AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0001] as indicated below:

[0001] This application is a continuation of, and claims the benefits and priority to, U.S. Patent Application No. 14/708,029, filed on May 8, 2015, which is a continuation of , and claims the benefits and priority to, U.S. Patent Application No. 13/194,317, filed on July 29, 2011, which further claims priority~~priorities and benefits~~ from and the benefits of Korean Patent Application No. 10-2010-0092807, filed on September 24, 2010, and Korean Patent Application No. 10-2010-0092808, filed on September 24, 2010, ~~which~~ The above patent applications are hereby incorporated by reference for all purposes as if fully set forth herein.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-51: Canceled.

52. (New) A light emitting diode (LED) package, comprising:

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;

a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;

a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer;
and

a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,

wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.

53. (New) The LED package of claim 52, further comprising a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack,

wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.

54. (New) The LED package of claim 52, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer

a part of the transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer.

55. (New) The LED package of claim 54, wherein the transparent conductive oxide film contact layer includes an ITO (Indium Tin Oxide).

56. (New) The LED package of claim 55, wherein at least one of the contact holes has a circular shape, and

wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.

57. (New) A light emitting diode (LED) module, comprising:

a circuit board; a LED package arranged over the circuit board without bonding wires, wherein the LED package includes:

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;

a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;

a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and

a protective insulation layer covering a sidewall of the first conductive type

semiconductor layer and the second conductive type semiconductor layer,
wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and
a lens to adjust an orientation angle of light emitted from the LED package.

58. (New) The LED module of claim 57, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and the LED packages is arranged over the MC-PCB.

59. (New) A light emitting diode (LED) module, comprising:
a circuit board;
a LED package bonded on the circuit board without bonding wires;
wherein the LED package comprising
a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;
a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;
a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;
a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer;
and
a protective insulation layer covering a sidewall of the first conductive type semiconductor layer.

60. (New) The LED module of claim 59, further comprising a wavelength converter over the opposite side of the LED package to the first and second electrode pads,
wherein the wavelength converter comprises a phosphor sheet or an impurity-doped material.

61. (New) The LED module of claim 60, wherein each area of the first and second pads has an area not less than $\frac{1}{3}$ of the LED package.

62. (New) The LED module of claim 59, further comprises a lens to adjust an orientation angle of light emitted from the LED package.

63. (New) The LED module of claim 59, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.

64. (New) The LED module of claim 63, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer; and
a first part of the protective insulation layer covering the contact layer.

65. (New) The LED module of claim 64, wherein a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer, the second part of the protective insulation layer contacts the first part of the protective insulation layer.

66. (New) The LED module of claim 65, wherein each area of the first and second pads is not less than $\frac{1}{3}$ of area of the LED package.

67. (New) The LED module of claim 66, further comprising a wavelength convertor the opposite side of the LED package to the first and second electrode pads,
wherein the wavelength converter comprises a phosphor sheet or an impurity-doped material.

68. (New) The LED module of claim 67, at least one of the contact holes has a circular shape, and
wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.

69. (New) The LED module of claim 68, further comprising a lens to adjust an orientation angle of light emitted from the LED package.

70. (New) The LED module of claim 69, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.

Applicants: Won Cheol Seo et al.
Appl. No. : Not yet assigned
Filed : Herewith
Page : 8 of 8

Docket No. 114896-8005.US02

REMARKS

This application is a continuation of, and claims the benefits and priorities to, co-pending U.S. Patent Application No. 14/708,029, filed on May 8, 2015, which is a continuation of U.S. Patent Application No. 13/194,317, filed on July 29, 2011. The U.S. Patent Application No. 13/194,317 further claims the benefits and priorities to Korean Patent Application No. 10-2010-0092807, filed on September 24, 2010, and Korean Patent Application No. 10-2010-0092808, filed on September 24, 2010.

The specification of this application as filed herewith is the original specification filed for U.S. Patent Application No. 13/194,317 on July 29, 2011. The above preliminary amendment is made to reflect the priority claims for this filing, to cancel original claims 1-51 and to add new claims, Claims 52-70 . Claims 52-70 are supported by the original specification and thus no new matter has been added.

Entry and consideration of the preliminary amendment is respectfully requested before examination.

Please apply any necessary charges or credits, to Deposit Account No. 50-5252.

Respectfully submitted,

Date: July 31, 2015

/Bing Ai/
Bing Ai
Reg. No. 43,312

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAM		
First Named Inventor/Applicant Name:		Won Cheol Seo		
Filer:		Bing Ai/Michelle Melendez		
Attorney Docket Number:		114898-8005.US02		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	23086688
Application Number:	14815433
International Application Number:	
Confirmation Number:	1096
Title of Invention:	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAM
First Named Inventor/Applicant Name:	Won Cheol Seo
Customer Number:	97075
Filer:	Bing Ai/Michelle Melendez
Filer Authorized By:	Bing Ai
Attorney Docket Number:	114898-8005.US02
Receipt Date:	31-JUL-2015
Filing Date:	
Time Stamp:	16:44:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

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Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	3362
Deposit Account	505252
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Information:					
2	Application Data Sheet	2_ADS.pdf	1561752 15ea680b8d63759c5c4dcb3bdc9f36a60c44e3	no	7
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3	Oath or Declaration filed	3_Sub_Stmt.pdf	10031193 1ec1728964aa36198af1a031eeef699eeef1e89	no	6
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4	Transmittal Letter	4_IDS_Transmittal.pdf	81903 e7d88b6de0a454e421566589675c4bba4350a32e	no	2
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