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(12) **EX PARTE REEXAMINATION CERTIFICATE** (11128th)
United States Patent
Seo et al.

(10) **Number:** **US 9,070,851 C1**(45) **Certificate Issued:** **Jun. 16, 2017**

(54) **WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME**

(75) Inventors: **Won Cheol Seo**, Ansan-si (KR); **Dae Sung Kal**, Ansan-si (KR)

(73) Assignee: **Seoul Semiconductor Co., Ltd.**

Reexamination Request:

No. 90/013,725, Apr. 15, 2016

Reexamination Certificate for:

Patent No.: **9,070,851**

Issued: **Jun. 30, 2015**

Appl. No.: **13/194,317**

Filed: **Jul. 29, 2011**

(30) **Foreign Application Priority Data**

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Sep. 24, 2010 (KR) 20-2010-0092807

(51) **Int. Cl.**
H01L 33/62 (2010.01)
H01L 33/20 (2010.01)

(52) **U.S. Cl.**
CPC **H01L 33/62** (2013.01); **H01L 33/20** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

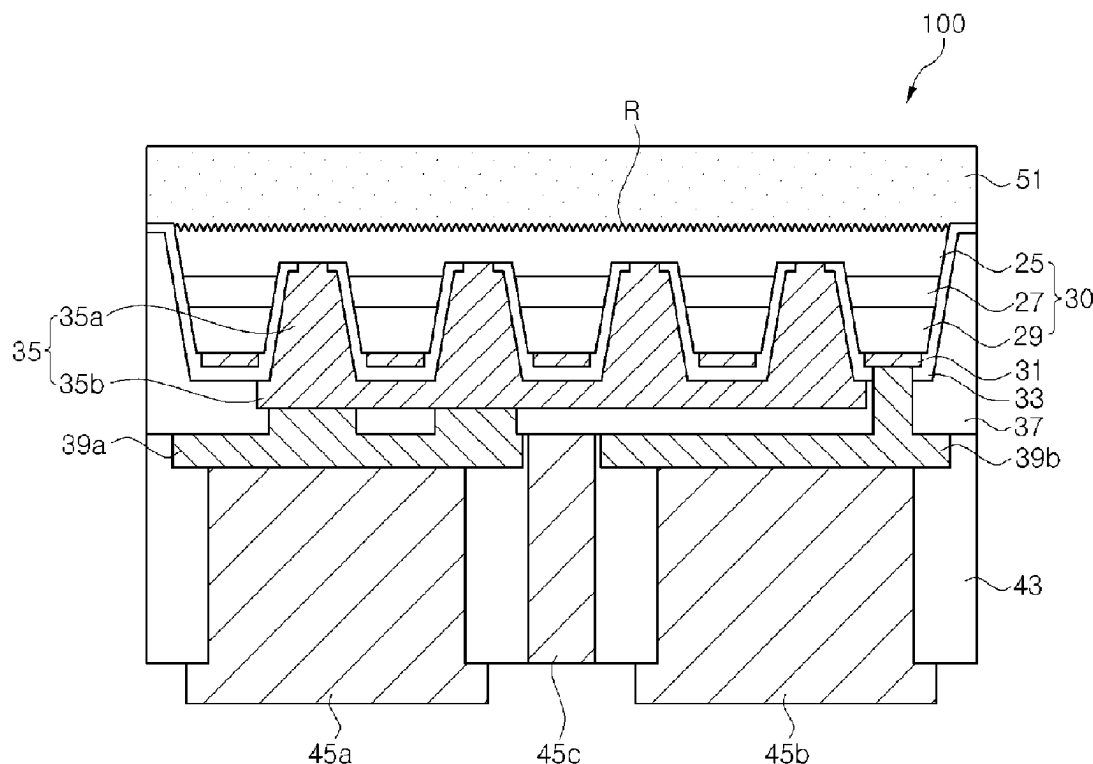
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 90/013,725, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — Tuan H Nguyen

(57) **ABSTRACT**

Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.



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EX PARTE REEXAMINATION CERTIFICATE

THE PATENT IS HEREBY AMENDED AS
INDICATED BELOW.

Matter enclosed in heavy brackets [] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claim 1 is determined to be patentable as amended.

Claims 2-15, dependent on an amended claim, are determined to be patentable.

New claims 16-35 are added and determined to be patentable.

1. A light emitting diode (LED) package, comprising *one or more light emitting diodes to emit light, wherein each single light emitting diode includes:*

- a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;
- a plurality of contact holes arranged in *and surrounded by* the second conductive type semiconductor layer and the active layer, *[the contact holes exposing] to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;*
- a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; *and*
- a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; *and*

wherein the LED package further includes a protective insulation layer covering [a sidewall] each external side wall surface of the semiconductor stack facing externally of the LED package so that the protection insulation layer surrounds the LED package.

16. A structure having light emitting diode (LED) packages, comprising:

- a stack of layers formed over one another and patterned to include an array of LED package regions, each LED package region including (1) a LED package formed in the stack of layers in a central region of the LED package region and (2) a protective insulation structure formed to surround and protect the LED package from surroundings outside the protective insulation structure and to separate from adjacent LED packages, wherein each LED package formed in the stack of layers includes:

- a semiconductor stack including a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack;

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contact holes formed as through holes in each semiconductor stack and surrounded by the second conductive type semiconductor layer and the active layer to pass therethrough so as to expose the first conductive type semiconductor layer;

a first electrical contact layer material filling in the contact holes to be electrically coupled to the first conductive type semiconductor layer and connecting the first contact holes;

a first bump on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the first electrical contact layer material; and

a second bump on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor layer, and

wherein the protective insulation structure includes a two-layer protective structure having a first protective insulation layer that surrounds and covers each external side wall surface of the semiconductor stack and a second protective insulation layer that forms on the first protective insulation layer to protect the semiconductor stack from an external environment.

17. The structure as in claim 16, comprising a wafer on which the stack of layers is formed and is patterned to include the array of LED package regions.

18. The structure as in claim 16, wherein each of the contact holes is tapered to have a larger end facing the second side and a smaller end facing the first side.

19. The structure as in claim 16, wherein:
the protective insulation structure further covers an entirety of each external side surface of an electrical contact structure that includes the first and second bumps on the first side of the semiconductor stack to protect the electrical contact structure from an external environment.

20. The structure as in claim 16, wherein:
each contact hole is formed to extend into a portion of the first conductive type semiconductor layer so that a portion of the first electrical contact material reaches into the portion of the first conductive type semiconductor layer to be in contact with the first conductive type semiconductor layer.

21. The structure as in claim 16, wherein each LED package formed in the stack of layers includes:

- a dummy bump that is electrically conductive, formed on the first side of the semiconductor stack between the first and second bumps to be electrically insulated from the first and second bumps to dissipate heat from the LED package.

22. A light emitting diode (LED) package, comprising:
a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack, and wherein the first side is closer to the second conductive type semiconductor layer than the first conductive type semiconductor layer and the second side is closer to the first conductive type semiconductor layer than the second conductive type semiconductor layer;

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contact holes formed as through holes in the semiconductor stack within an area for a single light emitting diode to be surrounded by the second conductive type semiconductor layer and the active layer to pass there-through so as to expose the first conductive type semiconductor layer within openings created by the contact holes;

an electrical contact structure on the first side of the semiconductor stack and electrically coupled to supply the electrical signal to the first and second type semiconductor layers via the contact holes, the electrical contact structure including (1) a first bump formed of an electrically conductive material and arranged on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer as part of a first electrical contact path to the semiconductor stack via the contact holes, (2) a first electrical contact layer material disposed to fill in the contact holes and to electrically couple the first conductive type semiconductor layer and the first bump via the contact holes, (3) a second bump formed of the electrically conductive material of the first bump and arranged on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor, and (4) a second electrical contact layer material electrically coupled between the second bump and the second conductive type semiconductor layer; and

an external structure that covers (1) the second side of the semiconductor stack that exports light generated in the active layer outside the LED package, and (2) side wall surfaces of the semiconductor stack.

23. The LED package as in claim 22, wherein the external structure includes:

- a first stacked protective insulation structure positioned to cover the entirety of each external side wall surface of the semiconductor stack to protect the semiconductor stack from an external environment and
- a second stacked protective insulation structure stacked over the first stacked protective insulation structure and located on the first side of the semiconductor stack to cover an entirety of each external side surface of the electrical contact structure to protect the electrical contact structure from an external environment.

24. The LED package as in claim 22, wherein: the external structure further covers external side wall surfaces of the electrical contact structure on the first side of the semiconductor stack.

25. The LED package as in claim 22, wherein the external structure includes:

- a first protective insulation layer covering an entirety of each external side wall surface of the semiconductor stack; and
- a second protective insulation layer that surrounds the semiconductor stack and forms on the first protective insulation layer so that the second protective insulation layer and the first protective insulation collectively form a two-layer protection structure to cover the entirety of each external side wall surface of the semiconductor stack and to enclose external sides of the semiconductor stack.

26. The LED package as in claim 22, wherein the composite insulation structure includes a phosphor structure that is formed of a phosphor composition that converts light

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emitted from the active layer into light at a different wavelength to be exported on the second side out of the LED package.

27. The LED package as in claim 22, further comprising: a dummy bump formed of the electrically conductive material and arranged on the first side of the semiconductor stack near the first bump or second bump to dissipate heat from the LED package, wherein the dummy bump is not electrically connected to the first bump or the second bump.

28. A light emitting diode (LED) package, comprising one or more light emitting diodes to emit light, wherein each single light emitting diode includes:

- a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, the first conductive type semiconductor layer shaped to include an inclined side wall;
- a plurality of contact holes arranged in, and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;
- a first bump arranged on a first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the plurality of contact holes;
- a second bump arranged on the first side of the semiconductor stack and electrically coupled to the second conductive type semiconductor layer; and
- a protective insulation layer covering a sidewall of the semiconductor stack of each light emitting diode and having a thickness that varies along the sidewall of the semiconductor stack.

29. The LED package of claim 28, wherein the protective insulation layer includes a two-layer protective structure having a first protective insulation layer that includes a uniform thickness along the sidewall of the semiconductor stack and a second protective insulation layer that has a varying thickness along the sidewall of the semiconductor stack.

30. The LED package of claim 28, wherein the second protective insulation layer is formed on the first protective insulation layer.

31. The LED package of claim 28, wherein the protective insulation layer covers side walls of the first conductive type semiconductor layer, the active layer, and the second conductive type semiconductor layer.

32. The LED package of claim 28, wherein each single light emitting diode further includes:

- a first contact layer electrically coupling the first conductive type semiconductor layer and the first bump via the contact holes; and
- a second contact layer electrically coupled between the second conductive type semiconductor layer and the second bump,

wherein the protective insulation layer extends to cover the second contact layer, the extended portion of the protective insulation layer having a size greater than that of the second contact layer.

33. The LED package of claim 28, wherein the protective insulation layer includes an optically reflective structure to

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reflect light towards a second side of the semiconductor stack that is opposite to the first side of the semiconductor stack.

34. The LED package of claim 28, wherein the protective insulation layer has an inclined shape along the sidewall of 5 the semiconductor stack.

35. The LED package as in claim 28, wherein each light emitting diode further includes:

a dummy bump formed of an electrically conductive material and arranged on the first side of the semicon- 10 ductor stack between the first and second bumps to dissipate heat from the LED package, wherein the dummy bump is electrically insulated from the first and second bumps.

* * * * *

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,725	04/15/2016	9070851	MT100	7313
97075 7590 05/22/2017 Perkins Coie LLP - SDO General PO Box 1247 Seattle, WA 98111-1247			EXAMINER NGUYEN, TUAN H	
			ART UNIT 3992	PAPER NUMBER
			MAIL DATE 05/22/2017	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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***EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM**

REEXAMINATION CONTROL NO. 90/013,725.

PATENT NO. 9070851.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No.	Patent Under Reexamination	
	90/013,725	9070851	
	Examiner	Art Unit	AIA (First Inventor to File) Status
	TUAN H. NGUYEN	3992	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
 - (a) ☒ Patent owner's communication(s) filed: 10 March 2017.
 - (b) ☐ Patent owner's failure to file an appropriate timely response to the Office action mailed: _____.
 - (c) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
 - (d) ☐ The decision on appeal by the ☐ Board of Patent Appeals and Interferences ☐ Court dated _____
 - (e) ☐ Other: _____.
2. The Reexamination Certificate will indicate the following:
 - (a) Change in the Specification: ☐ Yes ☒ No
 - (b) Change in the Drawing(s): ☐ Yes ☒ No
 - (c) Status of the Claim(s):
 - (1) Patent claim(s) confirmed: 2-15.
 - (2) Patent claim(s) amended (including dependent on amended claim(s)): 1
 - (3) Patent claim(s) canceled: _____.
 - (4) Newly presented claim(s) patentable: 16-35.
 - (5) Newly presented canceled claims: _____.
 - (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____
 - (7) Patent claim(s) not subject to reexamination: _____.
3. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
4. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
5. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
6. ☐ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).
7. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.
8. ☒ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the certified copies have
 - ☐ been received.
 - ☐ not been received.
 - ☒ been filed in Application No. 13/194,317.
 - ☐ been filed in reexamination Control No. _____.
 - ☐ been received by the International Bureau in PCT Application No. _____.

* Certified copies not received: _____.
9. ☐ Note attached Examiner's Amendment.
10. ☐ Note attached Interview Summary (PTO-474).
11. ☐ Other: _____.

All correspondence relating to this reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

cc: Requester (if third party requester)

U.S. Patent and Trademark Office
PTOL-469 (Rev. 08-13)

Notice of Intent to Issue Ex Parte Reexamination Certificate

Part of Paper No 20170329

DETAILED ACTION

The Patent Owner's amendment filed on March 10, 2017 have been considered and persuasive. Accordingly, the amendment is entered and the prior rejections are hereby withdrawn.

Claim Status

Claims 1, 16-35 are patentable.

Claims 2-15 are confirmed.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

None of the references of record teaches or suggests the claimed LED package wherein each single LED includes among other thing, a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor; and wherein the LED package further includes a protective insulation layer covering each external side wall surface of the semiconductor stack facing externally of the LED package so that the protection insulating layer surrounds the LED package as recited in claims 1, 16, 22, and 28.

Claims 2-15, 17-21, 23-27, 29-35 are confirmed as patentable because of their dependency from claims 1, 16, 22 and 28 respectively.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Remarks.

Conclusion

EXTENSIONS OF TIME

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that ex parte reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in ex parte reexamination proceedings are provided for in 37 CFR-1.550(c).

AMENDMENT IN REEXAMINATION PROCEEDINGS

Patent owner is notified that any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be

formally presented pursuant to 37 CFR § 1.52(a) and (b), and must contain any fees required by 37 CFR § 1.20(c). See MPEP § 2250(IV) for examples to assist in the preparation of proper proposed amendments in reexamination proceedings.

SERVICE OF PAPERS

After the filing of a request for reexamination by a third party requester, any document filed by either the patent owner or the third party requester must be served on the other party (or parties where two or more third party requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. See 37 CFR 1.550(f).

SUBMISSIONS

This NIRC informs the patent owner and any third party requester that the reexamination prosecution has been terminated. The rules do not provide for an amendment to be filed in a reexamination proceeding after prosecution has been terminated. The provisions of 37 CFR 1.312 do not apply in reexamination. Any amendment, information disclosure statement, or other paper related to the merits of the reexamination proceeding filed after prosecution has been terminated must be accompanied by a petition under 37 CFR 1.182 to have the amendment considered.

NOTIFICATION OF CONCURRENT PROCEEDINGS

The patent owner is reminded of the continuing responsibility under 37 CFR

11565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 9,070,851 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

All correspondence relating to this *ex parte* reexamination proceeding should be directed: By Mail to:

Mail Stop "Ex Parte Reexam"
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Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding should be directed to the Central Reexamination Unit at telephone number 571-272-7705.

Signed:

/Tuan H. Nguyen/
Primary Examiner
Central Reexamination Unit
Art Unit 3992

Conferees:

/Minh Nguyen/
Primary Examiner
CRU, Art Unit 3992

/Timothy M. Speer/
SPRS, AU 3992

Search Notes 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Examiner TUAN H NGUYEN	Art Unit 3992

CPC- SEARCHED		
Symbol	Date	Examiner
None	3/29/2017	TN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
None		3/29/2017	TN

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed of patented file's prosecution history	5/5/2016	TN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Issue Classification 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Examiner TUAN H NGUYEN	Art Unit 3992

CPC						
Symbol					Type	Version
H01L		33		62	F	2013-01-01
H01L		33		20	A	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 35	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 3992 (Primary Examiner) _____ (Date) _____		3/29/2017 (Date)	O.G. Print Claim(s) 1 O.G. Print Figure 1

Issue Classification 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Examiner TUAN H NGUYEN	Art Unit 3992

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED									
257			88			H	0	1	L	33 / 62 (2010.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			
257	99																			

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 35	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 3992 (Primary Examiner) _____ (Date) _____		3/29/2017 (Date) _____	O.G. Print Claim(s) 1
			O.G. Print Figure 1

Issue Classification 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
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☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33										
	2		18		34										
	3		19		35										
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	16		32												

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 35	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 3992 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 1

Reexamination 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Certificate Date	Certificate Number C1

Requester Correspondence Address:	☐ Patent Owner	☒ Third Party
ALAN TABOADA - MOSER TABOADA 1030 BROAD STREET, SUITE 203 SHREWSBURY, NJ 07702		

LITIGATION REVIEW ☒	TN (examiner initials)	04/04/2017 (date)
Case Name		Director Initials
None		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
1. No concurrent proceeding	



EIC 2600 SEARCH REPORT

STIC Database Tracking Number: 539412

To: Minh Dieu Nguyen
Location: MDE-4C01
Art Unit: N/A
Tuesday, April 04, 2017

Case Serial Number: 15/172840

From: Kimberly Johnson
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June 30, 2015

Wafer-level light emitting diode package and method of fabricating the same

REEXAM-LITIGATE:

Reexamination requested April 15, 2016 by Alan Taboada, Moser Taboada, Shrewsbury, NJ, Reexamination No. 90/013,725 (O.G. June 21, 2016) Ex. Gp.: 3992 April 15, 2016

APPL-NO: 194317 (13)

FILED-DATE: July 29, 2011

GRANTED-DATE: June 30, 2015

ASSIGNEE-PRE-ISSUE:

August 2, 2011 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., SEOUL SEMICONDUCTOR CO., LTD., 148-29, GASAN-DONG, GEUMCHEON-GU, SEOUL, KOREA, REPUBLIC OF (), 158-801, Reel and Frame Number: 026688/0805

ASSIGNEE-AT-ISSUE:

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CORE TERMS: layer, insulation, semiconductor, bump, conductive, package, pad, emitting, electrode, cell, substrate, stack, holes, exemplary, region, wavelength, chip, convertor, composed, module, fabricating, exposed, silicon, electrically, expose, diode, protective, connector, connecting, sidewall

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Ex Parte* reexamination of:
U.S. Patent No. 9,070,851 B2

Inventor: Won Cheol Seo et al.

Confirmation No.: 7313

Control No.: 90/013,725

Examiner: Nguyen, Tuan H.

Filed: April 15, 2016

Art Unit: 3992

For: WAFER-LEVEL LIGHT EMITTING DIODE
PACKAGE AND METHOD OF FABRICATING THE
SAME

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CORRECTION TO INFORMALITY IN PATENT OWNER'S RESPONSE
TO OFFICE ACTION FILED ON DECEMBER 19, 2016

In response to the First Office Action dated September 19, 2016, Patent Owner submits the following amendments and explanations:

Amendments to the Claims are reflected in the listing of claims that begin on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A light emitting diode (LED) package, comprising one or more light emitting diodes to emit light, wherein each single light emitting diode includes:

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, [the contact holes exposing] to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;

a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; and

a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and

wherein the LED package further includes a protective insulation layer covering each external side wall surface [a sidewall] of the semiconductor stack facing externally of the LED package so that the protection insulation layer surrounds the LED package.

2. (Original) The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.

3. (Original) The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped single crystal substrate.

4. (Original) The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.

5. (Original) The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.

6. (Original) The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.

7. (Original) The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.

8. (Original) The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.

9. (Original) The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.

10. (Original) The LED package of claim 9, wherein the substrate comprises sapphire or silicon.

11. (Original) The LED package of claim 1, further comprising:
a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and
a second contact layer contacting the second conductive type semiconductor layer,
wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer,
wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.

12. (Original) The LED package of claim 11, further comprising:
a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and
a second electrode pad contacting the second contact layer through a second contact hole

arranged in the second insulation layer and the first insulation layer,
wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.

13. (Original) The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.

14. (Original) A light emitting diode (LED) module, comprising:
a circuit board;
the LED package of claim 1 arranged on the circuit board; and
a lens to adjust an orientation angle of light emitted from the LED package.

15. (Original) The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.

16. (New) A structure having light emitting diode (LED) packages, comprising:
a stack of layers formed over one another and patterned to include an array of LED package regions, each LED package region including (1) a LED package formed in the stack of layers in a central region of the LED package region and (2) a protective insulation structure formed to surround and protect the LED package from surroundings outside the protective insulation structure and to separate from adjacent LED packages,

wherein each LED package formed in the stack of layers includes:

a semiconductor stack including a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack;

contact holes formed as through holes in each semiconductor stack and surrounded by the second conductive type semiconductor layer and the active layer to pass therethrough so as to expose the first conductive type semiconductor layer;

a first electrical contact layer material filling in the contact holes to be electrically coupled to the first conductive type semiconductor layer and connecting the first contact holes;
a first bump on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the first electrical contact layer material; and
a second bump on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor layer, and
wherein the protective insulation structure includes a two-layer protective structure having a first protective insulation layer that surrounds and covers each external side wall surface of the semiconductor stack and a second protective insulation layer that forms on the first protective insulation layer to protect the semiconductor stack from an external environment.

17. (New) The structure as in claim 16, comprising a wafer on which the stack of layers is formed and is patterned to include the array of LED package regions.

18. (New) The structure as in claim 16, wherein each of the contact holes is tapered to have a larger end facing the second side and a smaller end facing the first side.

19. (New) The structure as in claim 16, wherein:
the protective insulation structure further covers an entirety of each external side surface of an electrical contact structure that includes the first and second bumps on the first side of the semiconductor stack to protect the electrical contact structure from an external environment.

20. (New) The structure as in claim 16, wherein:
each contact hole is formed to extend into a portion of the first conductive type semiconductor layer so that a portion of the first electrical contact material reaches into the portion of the first conductive type semiconductor layer to be in contact with the first conductive type semiconductor layer.

21. (New) The structure as in claim 16, wherein each LED package formed in the stack of layers includes:
a dummy bump that is electrically conductive, formed on the first side of the

semiconductor stack between the first and second bumps to be electrically insulated from the first and second bumps to dissipate heat from the LED package.

22. (New) A light emitting diode (LED) package, comprising:

a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack, and wherein the first side is closer to the second conductive type semiconductor layer than the first conductive type semiconductor layer and the second side is closer to the first conductive type semiconductor layer than the second conductive type semiconductor layer;

contact holes formed as through holes in the semiconductor stack within an area for a single light emitting diode to be surrounded by the second conductive type semiconductor layer and the active layer to pass therethrough so as to expose the first conductive type semiconductor layer within openings created by the contact holes;

an electrical contact structure on the first side of the semiconductor stack and electrically coupled to supply the electrical signal to the first and second type semiconductor layers via the contact holes, the electrical contact structure including (1) a first bump formed of an electrically conductive material and arranged on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer as part of a first electrical contact path to the semiconductor stack via the contact holes, (2) a first electrical contact layer material disposed to fill in the contact holes and to electrically couple the first conductive type semiconductor layer and the first bump via the contact holes, (3) a second bump formed of the electrically conductive material of the first bump and arranged on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor, and (4) a second electrical contact layer material electrically coupled between the second bump and the second conductive type semiconductor layer; and

an external structure that covers (1) the second side of the semiconductor stack that

exports light generated in the active layer outside the LED package, and (2) side wall surfaces of the semiconductor stack.

23. (New) The LED package as in claim 22, wherein the external structure includes:
a first stacked protective insulation structure positioned to cover the entirety of each
external side wall surface of the semiconductor stack to protect the semiconductor stack from an
external environment; and

a second stacked protective insulation structure stacked over the first stacked protective
insulation structure and located on the first side of the semiconductor stack to cover an entirety
of each external side surface of the electrical contact structure to protect the electrical contact
structure from an external environment.

24. (New) The LED package as in claim 22, wherein:
the external structure further covers external side wall surfaces of the electrical contact
structure on the first side of the semiconductor stack.

25. (New) The LED package as in claim 22, wherein the external structure includes:
a first protective insulation layer covering an entirety of each external side wall surface of
the semiconductor stack; and

a second protective insulation layer that surrounds the semiconductor stack and forms on
the first protective insulation layer so that the second protective insulation layer and the first
protective insulation collectively form a two-layer protection structure to cover the entirety of
each external side wall surface of the semiconductor stack and to enclose external sides of the
semiconductor stack.

26. (New) The LED package as in claim 22, wherein the composite insulation structure
includes a phosphor structure that is formed of a phosphor composition that converts light emitted
from the active layer into light at a different wavelength to be exported on the second side out of
the LED package.

27. (New) The LED package as in claim 22, further comprising:
a dummy bump formed of the electrically conductive material and arranged on the first
side of the semiconductor stack near the first bump or second bump to dissipate heat from the

LED package, wherein the dummy bump is not electrically connected to the first bump or the second bump.

28. (New) A light emitting diode (LED) package, comprising one or more light emitting diodes to emit light, wherein each single light emitting diode includes:

a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, the first conductive type semiconductor layer shaped to include an inclined side wall;

a plurality of contact holes arranged in, and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;

a first bump arranged on a first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the plurality of contact holes;

a second bump arranged on the first side of the semiconductor stack and electrically coupled to the second conductive type semiconductor layer; and

a protective insulation layer covering a sidewall of the semiconductor stack of each light emitting diode and having a thickness that varies along the sidewall of the semiconductor stack.

29. (New) The LED package of claim 28, wherein the protective insulation layer includes a two-layer protective structure having a first protective insulation layer that includes a uniform thickness along the sidewall of the semiconductor stack and a second protective insulation layer that has a varying thickness along the sidewall of the semiconductor stack.

30. (New) The LED package of claim 28, wherein the second protective insulation layer is formed on the first protective insulation layer.

31. (New) The LED package of claim 28, wherein the protective insulation layer covers side walls of the first conductive type semiconductor layer, the active layer, and the second conductive type semiconductor layer.

32. (New) The LED package of claim 28, wherein each single light emitting diode further includes:

a first contact layer electrically coupling the first conductive type semiconductor layer and the first bump via the contact holes; and

a second contact layer electrically coupled between the second conductive type semiconductor layer and the second bump,

wherein the protective insulation layer extends to cover the second contact layer, the extended portion of the protective insulation layer having a size greater than that of the second contact layer.

33. (New) The LED package of claim 28, wherein the protective insulation layer includes an optically reflective structure to reflect light towards a second side of the semiconductor stack that is opposite to the first side of the semiconductor stack.

34. (New) The LED package of claim 28, wherein the protective insulation layer has an inclined shape along the sidewall of the semiconductor stack.

35. (New) The LED package as in claim 28, wherein each light emitting diode further includes:

a dummy bump formed of an electrically conductive material and arranged on the first side of the semiconductor stack between the first and second bumps to dissipate heat from the LED package, wherein the dummy bump is electrically insulated from the first and second bumps.

REMARKS

Patent Owner acknowledges the helpful written explanations by Examiner Mr. Tuan Nguyen with respect to the rejections to Claims 1-15 of the U. S. Patent No. 9,070,851 B2 (“the ‘851 Patent”) in the First Office Action dated September 19, 2016. Additionally, Patent Owner thanks Mr. Tuan Nguyen, Mr. Minh Nguyen and Mr. Timothy Speer for the telephonic interview with Patent Owner’s counsel on November 17, 2016.

In response, Patent Owner has amended Claims 1-15 by amending Claim 1 and respectfully requests the Office to reconsider and withdraw the outstanding rejections in light of the teachings in the cited prior art and the analyses of such teachings presented in this filing. Specifically, Claims 1-15 as amended and presented in this filing are distinctly different from the prior art teachings relied upon in the First Office Action and are patentable over the cited prior art under the grounds raised.

As part of this response, in addition to amending Claim 1, Patent Owner submits additional Claims 16-35 based on the original specification for consideration by the Office in this proceeding and requests the Office to allow those claims in light of the facts and analyses presented for Claims 1-15 and further in light of the additional features recited in those claims.

The Office sets a shortened statutory period of three months for Applicant’s response by December 19, 2016 (Page 1 of the First Office Action). Accordingly, this response is filed timely.

SUMMARY OF THE EXAMINER’S INTERVIEW INITIATED BY PATENT OWNER

On November 17, 2016, in response to Patent Owner’s request, Mr. Tuan Nguyen, Mr. Minh Nguyen and Mr. Timothy Speer conducted an interview with Patent Owner’s counsel to discuss the cited prior art and rejections in the First Office Action. During the interview, the teachings in cited Seiichiro, Shelton and Donofrio and technical features disclosed and claimed in the ‘851 Patent were discussed. In addition, technical features disclosed in the ‘851 Patent for potential claim amendments to Claim 1 and other claims were discussed. No specific agreements were reached at the interview.

See also “Ex Parte Reexamination Interview Summary” issued by the Office with a mailing date of November 25, 2016.

STATUS OF CLAIMS

Claims 1-15 as originally issued in the '851 Patent are subject to reexamination and are rejected in the First Office Action in response to a third party request.

Patent Owner has amended the claims: Claim 1 has been amended based on the original specification of the '851 Patent; and Claims 16-35 have been newly added based on the original specification of the '851 Patent, including, e.g., Figures 1-27 and associated textual description. No new matter has been added.

Upon entry of the claim amendments, Claims 1-35 are under consideration in this proceeding.

APPLICABLE LAW ON PATENTABILITY

The '851 Patent is based on the U.S. Patent Application No. 13/194,317 filed on July 29, 2011 which was timely filed to claim priorities from Korean Patent Application Nos. 10-2010-0092807 and 10-2010-0092808, both filed on September 24, 2010. Therefore, pre-AIA 35 U.S.C. §102 and 103 are applicable to the patentability of each claim of the '851 Patent in this proceeding.

OVERVIEW OF CERTAIN ASPECTS OF THE '851 PATENT

The '851 Patent, entitled "Wafer-level light emitting diode package and method of fabricating the same," describes wafer-level LED structures with LED package regions to provide protective insulation structure designs as part of the wafer-level structures to protect each individual LED package region from its surroundings and neighboring LED package regions at the wafer level before dividing the wafer into individual LED packages or chips for subsequent packaging processes.

The '851 Patent includes aspects of the disclosed technology regarding dividing the monolithically formed LED package regions grown on a wafer for further processing. When the divided LED package regions are not properly protected, this dividing operation can expose the diced LED packages to the surrounding environment in subsequent processes such as mounting each individual LED package on a circuit board, forming electrical contacts to the mounted circuit board and placing a covering molding member and other steps to form final LED devices. An unprotected diced LED package can be inadvertently contaminated by external

environmental factors and such contamination can cause the LED layers or structure to deteriorate and adversely affect the device operation, device performance and/or device lifetime, especially considering that LED package devices may operate under high voltages or currents and at elevated high temperatures. See, e.g., ‘the 851 Patent at 1:33-60; 2:30-55; 6:40-60; 7:13-25; 10:9-23; 14:45-52; 17:26-42.

In this regard, the ‘851 Patent discloses the recognitions of the above technical issues in fabricating LED devices by the inventors and include Figures 1-27 to illustrate features of its protective insulation layer designs as part of the wafer-level structures. Specifically, the ‘851 Patent show four exemplary embodiments wafer-level protective insulation layer designs in Figures 1, 2, 14 and 15.

For easy reference, Patent Owner reproduces below the annotated versions of Figures 1, 2, 14 and 15 with added colors to illustrate how each LED package region among an array of LED package regions is surrounded by an individual “protective cage” at the wafer level processing and is separated from neighboring LED package regions before being diced into individual LED chips for further packaging.

Figure 1 in the ‘851 Patent shows a cross section view of one LED package region 100 where the protective insulation structure surrounding the LED package region is shown by components in blue, red and orange colors.

Figure 1

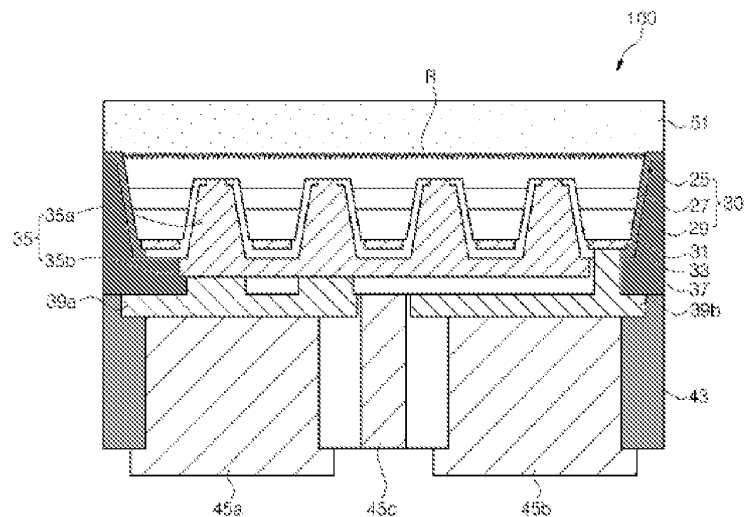


Figure 1 of the ‘851 Patent (Annotated)

In the LED package 100 in Figure 1, the semiconductor stack 30 includes a first conductive type upper semiconductor layer 25, an active layer 27, and a second conductive type lower semiconductor layer 29. The active layer 27 is interposed between the upper and lower semiconductor layers 25, 29. *Id.* at 5:12-23. In this example, four contact holes are formed inside the semiconductor stack 30 and are surrounded by the second conductive type lower semiconductor layer 29 and the active layer 27 to pass through the layers 29 and 27 so as to reach and expose the first conductive type upper semiconductor layer 25. See also, *Id.* at Figures 5(a) and 5(b). Those four contact holes are filled with contact sections 35a contacting the first conductive type upper semiconductor layer 25. *Id.* at 5:24-49. The LED package 100 may include a first contact layer 35, a second contact layer 31, a first insulation layer 33 (in blue), a second insulation layer 37 (in red), a first electrode pad 39a, a second electrode pad 39b, a first bump 45a, and a second bump 45b. The LED package 100 may further include an insulation layer 43 (in orange), a dummy bump 45c, and a wavelength convertor 51. *Id.* at 5: 12-18.

The first contact layer 35 is located under the first insulation layer 33 and contacts the first conductive type upper semiconductor layer 25 through the first insulation layer 33 in the plurality of contact holes 30a. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25, and a connecting section 35b connecting the contact sections 35a to each other. Therefore, the contact sections 35a are electrically connected to each other by the connecting section 35b. The first contact layer 35 is formed under some regions of the first insulation layer 33 and may be composed of a reflective metal layer. *Id.* at 6:5-22.

Notably, Figure 1 shows that, in the specific embodiment as illustrated, the entire external side surfaces surrounding the LED package 100 are covered by and surrounded by the protective insulation structure. The external side surfaces of the top part of the LED package 100 are slanted external surfaces of the semiconductor stack 30 and are fully covered by the first insulation layer 33 (with its external part being shown in blue) as the first protective insulation layer and is further covered by the top part of the second insulation layer 37 (with its external part being shown in red) over the first insulation layer (with its external part being shown in blue). This is an example of a two-layer protective structure outside the semiconductor stack 30.

In addition, in the embodiment in Figure 1, the external side surfaces of the middle part of the LED package 100 are the external side surfaces of the connecting section 35b and the first

electrode pad 39a (on the left-hand side external surface), and the external side surfaces of the second electrode pad 39b (on the right-hand side external surface) that are located in and under the second insulation layer 37. *Id.* at 6:23-39. As illustrated in Figure 1, those middle part external side surfaces are covered, and surrounded by external parts of the first and second insulation layers 33 and 37 as shown in blue and red and the top external part of the insulation layer 43 as shown in orange.

Furthermore, in the specific embodiment in Figure 1, the external side surfaces of the lower part of the LED package 100 shown in Figure 1 are the external side surfaces of the external surfaces of the first bump (on the left-hand side external surface), and the external side surfaces of the second bump 45b (on the right-hand side external surface). The entire exposed external side surfaces of the bumps 45a and 45b are covered and surrounded by external parts of the insulation layer 43 as shown in orange. In Figure 1, the bottom parts of the bumps 45a and 45b have protruded sections that are used to connect to the circuit board for the LED package 100.

Therefore, Figure 1 shows an example of a protective insulation structure formed together with the semiconductor stack 30 during wafer-level fabrication of the semiconductor stack for the LED package 100 to include external parts of the first and second insulation layers 33 (in blue) and 37 (in red) and the external part of the insulation layer 43 (in orange) to surround and cover the entire side wall surfaces of the LED package 100 below the wavelength converter 51 to protect, the semiconductor stack 30 and the underlying electrical contact parts (35b, 39a, 39b, 45a and 45b) from an external environment.

Specifically, the disclosed protective insulation layer designs in the '851 Patent are built into the wafer-level structures to have built-in protection as an individual protective cage or structure for surrounding each LED package region on a wafer from external environmental factors. This protective structure for each LED package region is formed as part of the wafer-level fabrication for forming the LED semiconductor stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and will protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent packaging processes, and during the normal use of the LED package device after the fabrication.

Therefore, the disclosed protective insulation layer designs in the '851 Patent protect the individual LED packages or devices in both fabrication phase and the product use phase.

In light of the above example of a protective insulation structure in Figure 1 in the '851 Patent, the other three examples shown in Figures 2, 14 and 15 are different designs based on the similar basic protection concept illustrated in Figure 1 but provide an additional protective insulation layer 49 or 141 to the protective insulation structure shown in a purple color. The insulation substrate 61 in Figure 2 and the insulation substrate 161 in Figures 14 and 15 correspond to the insulation layer 43 in Figure 1.

Figure 2

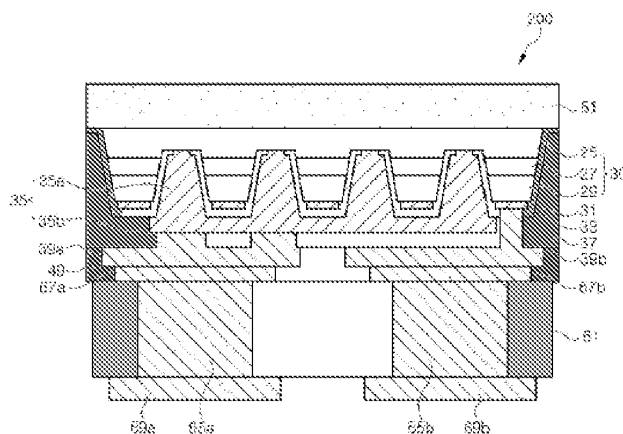


Figure 2 of the '851 Patent (Annotated)

Figure 14

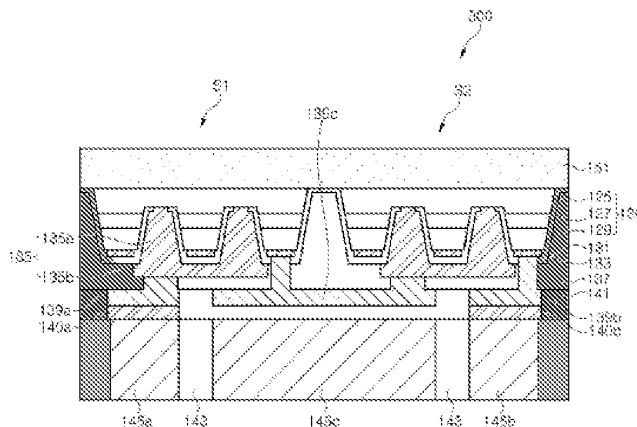


Figure 14 of the '851 Patent (Annotated)

[illegible]

In the exemplary design in Figure 2, to prevent the first and second electrode pads 39a, 39b from being exposed to the outside, the '851 Patent teaches a use of an insulation layer 49 to cover side surfaces and bottom surfaces of the first and second electrode pads 39a, 39b. The insulation layer 49 may have openings, which expose the first and second electrode pads 39a, 39b, and additional metal layers 67a, 67b are then formed in the openings. *Id.* at 7: 46-60. The external parts of the insulation layer 49 is located between the insulation layer 37 and the insulation substrate 61. Therefore, similar to the protective insulation structure shown in colors in Figure 1, the protective insulation structure shown in colored parts of the insulation layers 33, 37, and 49 and the insulation substrate 61 provides built-in protection as an individual protective cage for each LED package region on a wafer from external environmental factors. The designs in Figures 14 and 15 are similar in this regard.

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technical disclosures and the LED package designs and the above protective insulation structure designs and is patentable over the prior art teachings cited in the First Office Action.

In another aspect, the '851 Patent discloses built-in heat dissipation bumps that are distinct from the electrical bumps, e.g., the bump 45c between the electrical bumps 45a and 45b in Figure 1, the bump 145c between the electrical bumps 145a and 145b in Figure 14, and bumps 165c between the electrical bumps 165a and 165b in Figure 15. The bumps 45c, 65c and 165c are electrically "dummy" bumps that do not function as electrical paths or connections but are provided to dissipate heat generated in the LED packages. In some LED package designs, such as the examples in Figures 1, 14 and 15, the built-in heat dissipation bumps can be implemented along with the protective insulation structure designs to improve the performance of the LED packages.

The following sections discuss each of the rejections from Page 5 through Page 21 of the First Office Action in the order as appeared therein.

REJECTIONS TO CLAIMS 1-4, 7, 9 AND 11 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER SEIICHIRO

The rejections to Claims 1-4, 7, 9 and 11 over Seiichiro in the First Office Action at Page 5 should be withdrawn because the cited teachings in Seiichiro fail to anticipate those claims as presented in this filing.

The analysis of Claim 1 in the First Office Action at Page 5 is reproduced below:

Regarding to claim 1:

Seiichiro, Figs. 1-3 as shown below, discloses a light emitting diode package including a semiconductor stack comprising a first conductivity type (i.e. n-type) semiconductor layer 12, an active layer 13, and a second conductive type (i.e. p-type) semiconductor layer 14, a plurality of contact holes arranged in the second conductive type semiconductor layer 14 and the active layer 13, the contact holes exposing the first conductive type semiconductor layer 12; a first bump 21, 24 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 12 via the plurality of contact holes; a second bump 26 arranged on the first side of the of the conductor stack, the second bump 26 being electrically connected to the second conductive type semiconductor layer 14; and a protective insulation layer 17, 30 covering a sidewall of the semiconductor stack.

Based on a review of the above cited portions in Seiichiro, Patent Owner respectfully submits that the cited teachings in Seiichiro are different from the subject matter in Claim 1 as

amended and thus do not support the contended mapping between Seiichiro and Claim 1 as amended.

Claim 1 as amended recites a light emitting diode (LED) package that includes, among others, “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer” and “a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” within each single light emitting diode.

The recited “contact holes” are supported by the specification of the ‘851 Patent, including, e.g., the contact holes 35a that are surrounded by the layers 29 and 27 to pass through layers 29 and 27 to reach and expose the layer 28, as illustrated in an example in Figures 5(a) and 5(b) which are reproduced below.

Figure 5

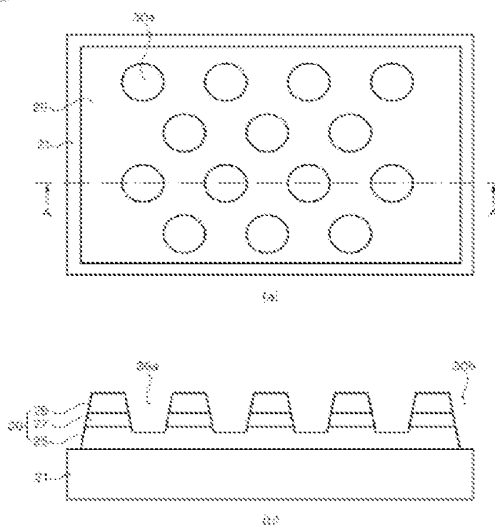


Figure 5 of the ‘851 Patent

The First Office Action generally mentions openings in layers 13 and 10 in Figures 1-3 of Seiichiro to expose the layer 12. However, the First Office Action fails to support this position by a specific illustration or text description in Seiichiro. Figures 2 and 3 in Seiichiro show cross sectional views of the different layers in Seiichiro and thus are reproduced below.

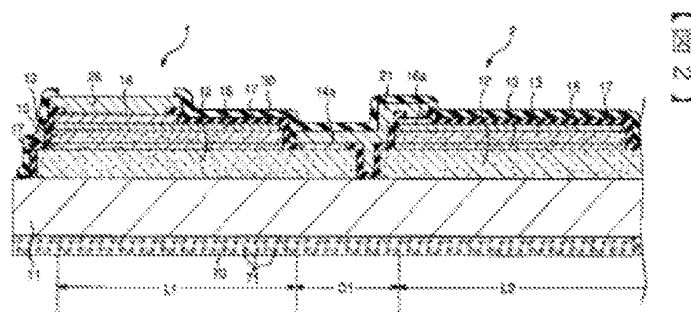


Figure 2 of Seichiro

Figure 2 of Seichiro shows a cross sectional view of two adjacent LED elements 1 and 2. In each LED element 1 or 2, Seichiro does not teach two or more contact holes in layers 13 and 10 to expose the layer 12. Figure 3 shows a cross sectional view of the LED element 3 and does not disclose two or more contact holes in layers 13 and 10 to expose the layer 12.

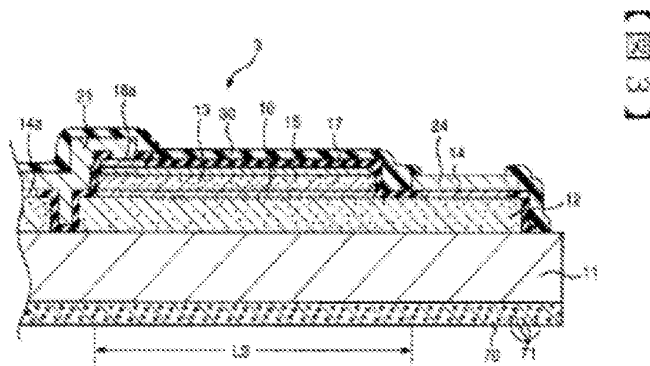


Figure 3 of Seichiro

In addition, Figure 1 shows the top view of the structure having the LED elements 1, 2 and 3 shown in Figures 2 and 3 and does not show two or more contact holes in layers 13 and 10 to expose the layer 12 in any of the LED element 1, 2 or 3.

In other parts of Seichiro, Seichiro describes openings in form of grooves or trenches in the embodiment in Figures 1-3, e.g., an isolation groove or trench 41 in [0021] and through holes 61 and 62 related to the embodiment 2 in Figure 4.

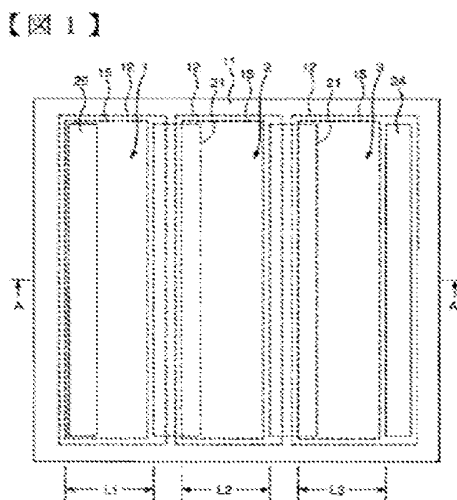


Figure 1 of Seichiro

However, the isolation groove or trench 41 in [0021] is not surrounded by the second conductive type semiconductor layer and the active layer because of their open ended structures. In addition, Seichiro fails to show two or more contact holes in each LED element 1 or 2.

Therefore, nothing in Seichiro teaches the recited contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer in Claim 1 as amended.

Additionally, the First Office Action fails to demonstrate a teaching in Seichiro on the recited first and second bumps arranged on the first side of the semiconductor stack in Claim 1. Specifically, the First Office Action points to the element 26 on top of the top p-layer 13 which is above the active layer 10 and the n-layer 12 in Figure 1 in Seichiro as the recited second bump in Claim 1. Under this mapping, the First Office Action appears to correspond to the space above the top p-layer 12 to the recited “first side of the semiconductor stack” of Claim 1.

In this regard, the First Office Action further points to elements 21, 24 in Figure 1 as the recited first bump arranged on the first side of the semiconductor stack in Claim 1. This contention, however, is based on an incorrect understanding of the technical nature of the element 21 or 24 in Figure 1 in Seichiro.

The element 21 in Seiichiro is a connection electrode that interconnects two adjacent LED elements 1 and 2 and is continuously formed so as to extend over the n-side ohmic electrode 14a of the LED element 1, the insulating film 17 formed in the separation trench 41, and the p-side ohmic electrode 16a of the LED element 2, to electrically connect the n-side ohmic electrode 14a of the LED element 1 to the p-side ohmic electrode 16a of the LED element 2. Therefore, the connection electrode 21 has a portion in the LED element 1 that is either in the same layer as the top p-layer 13 or below the top p-layer 13 as shown by Figure 1 within the LED element 1 and thus cannot be arranged “on the first side” as the element 26 on top of the top p layer 13. The same connection electrode 21 has a portion that is in the LED element 2 and is on top of the p-layer 12 in the LED element 2 rather than in the LED element 1. See Seiichiro at [0027] and [0028]. Therefore, the First Office Action is defective in providing the proper teaching in Seiichiro. The above analysis of the Seiichiro design also demonstrates that Seiichiro teaches a very different LED device structure for interconnecting two adjacent LED elements and thus does not disclose the features as recited in Claim 1 within one light emitting diode.

Specifically, the element 24 in Figure 3 of Seiichiro is an external connection electrode formed over the n-pad electrode 14 of the LED element 3 and, within the LED element 3, is either in the same layer as the top p-layer 13 or below the top p-layer 13 as shown by Figure 3 within the LED element 3 and thus cannot be arranged “on the first side” on top of the top p-layer 13 in the LED element 3.

Claim 1 is amended to explicitly state that the LED package further includes a protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package.

As explained above in the “Overview of the ‘851 Patent” section, this aspect of Claim 1 as amended is supported by the disclosed protective insulation layer designs in the ‘851 Patent as the wafer-level structures to have built-in protection as an individual “protective cage” for surrounding each LED package region on a wafer from external environmental factors. This protective cage for each LED package region is formed as part of the wafer-level fabrication for forming the LED semiconductor stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and will protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent

packaging processes, and during the normal use of the LED package device after the fabrication. Seiichiro fails to disclose this aspect of Claim 1 as amended.

The First Office Action merely points to one sectional view of the layer 17, 30 in Figure 2 or 3 along one direction A-A' as marked in Figure 1 in Seiichiro. This illustration in Seiichiro, however, fails to provide sufficient teaching under 35 U.S.C. §102 to show that “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” of Claim 1 as amended. There is no such teaching in Seiichiro because Seiichiro is completely silent as to the adverse environmental contamination by moisture and others when dividing a wafer into separate LED packages and in subsequent packaging and fabrication processes.

For at least the above defects in the disclosure of Seiichiro, the First Office Action fails to make a showing that Seiichiro discloses each claim limitation in Claim 1 as amended. Therefore, Claim 1 as amended recites multiple features that are missing in Seiichiro and is patentable under 35 U.S.C. §102 over Seiichiro.

Claims 2-4, 7, 9 and 11 are dependent claims of Claim 1 and thus are patentable over Seiichiro based on the above explanations for Claim 1 and based on their own merits.

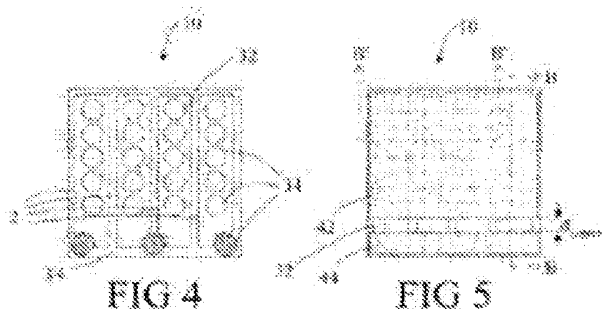
REJECTIONS TO CLAIMS 1-4, 7, 11-12 AND 14-15 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER SHELTON

The rejections to Claims 1-4, 7, 11-12 and 11-14 over Shelton in the First Office Action at Pages 9-11 are traversed because the cited teachings in Shelton fail to support the rejections as contended.

Claim 1 as amended recites a light emitting diode (LED) package that includes, among others, “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer” and “a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” within each single light emitting diode.

The First Office Action at Page 10 contends the vias 34 shown in FIGS. 4 and 5 and described at 6:44-45 correspond to the recited plurality of contact holes in Claim 1:

a plurality of contact holes 34 arranged in the second conductive type semiconductor layer 24 and the active layer, the contact holes exposing the first conductive type semiconductor layer 22 (Figs. 4-5, col. 6, lines 44-45);



The above characterization of the vias 34 of Shelton, however, lacks support in Shelton and misapplies the teachings in Shelton.

First, referring to FIGS. 1-3 in Shelton in connection with FIGS. 4-5 in Shelton, those figures and related text in Shelton do not disclose contact holes that pass through p-layer and active layer within the mesa 24 to expose the n-layer. Further referring to other drawings in FIGS. 1-13, the mesa 24 that contains the p-layer and the active layer in Shelton has no contact holes. The contact to the n-layer is achieved outside the mesa 24 by the n-contact 14 in contact with the n-layer 22.

Second, the vias 34 in FIGS. 4 and 5, which are contended to be the “contact holes” in Claim 1 by the First Office Action, are formed in a dielectric layer 32 to access the p-type electrode 12 and the n-type electrode 14 at 6:7-19:

To address this problem, a bonding pads formation process described with reference to FIGS. 4–11 is employed to adapt the fine features of the electrodes 12, 14 to the larger tolerance of the flip chip bonding process. The bonding pads formation process includes formation of a fanning layer 30 as shown in FIGS. 4–7. Formation of the fanning layer 30 includes depositing a dielectric layer 32 in which vias 34 are formed to provide access to the p-type electrode 12 and the n-type electrode 14, followed by metallization processing that fills the vias 34 with an electrically conductive material 36 and that forms intermediate connecting pads, specifically an intermediate p-type connecting pad 42 and an intermediate n-type connecting pad 44.

Under the teaching by Shelton, the dielectric layer 32 is formed after the formation of the layers or structures 22, 24, 12 and 14 and, specifically, is on top of the layers or structures 22, 24, 12 and 14. Notably, the dielectric layer 32 is located on top of the mesa 24 and, accordingly, the vias 34 formed in the dielectric layer 32 at the position of the mesa 24 are also on top of the mesa 34 and cannot be contact holes arranged in the p-layer and the active layer inside the mesa 24. Therefore, vias 34 in Shelton cannot be “contact holes arranged in ... the second conductive type semiconductor layer and the active layer” as recited in Claim 1 as amended (with added emphasis).

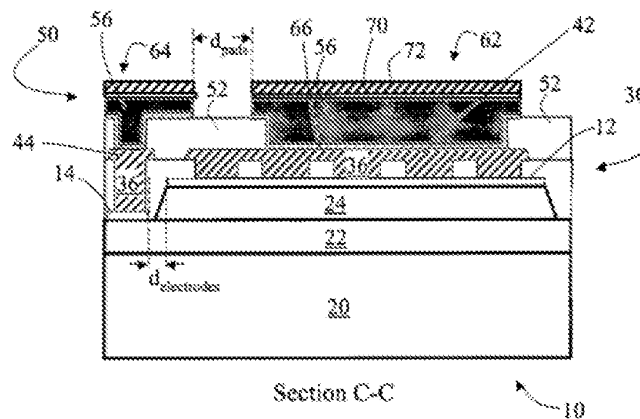
In addition, Shelton teaches that the vias 34 are used to access from the top of the dielectric layer 32 to contact the p-type electrode 12 that is above the mesa 24 and the n-layer 22. Therefore, the vias 34 in the dielectric layer 32 cannot be contact holes inside the mesa 24 underneath the p-type electrode 12. Accordingly, the vias 34 in Shelton cannot be “contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer” as in Claim 1 as amended (with added emphasis).

Therefore, the First Office Action’s reliance on the vias 34 in FIGS. 4 and 5 fails to support a teaching in Shelton of “contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” of Claim 1 as amended.

Accordingly, Claim 1 as amended is distinct from Shelton and is patentable under 35 U.S.C. §102.

The First Office Action also cites the electrically conductive material 56 in the dielectric layer 52 of FIG. 10 in Shelton as a teaching in Shelton for the recited first bump and the recited second bump in Claim 1 (Page 10 of the First Office Action):

a first bump 56 arranged on a first side of the semiconductor stack, extending through the opening in dielectric material 52 and electrically connected to the first conductive type semiconductor layer 22, and a second bump 56 extending through the opening in the dielectric material and electrically connected to the second conductive type semiconductor layer 24 (Fig. 10, col. 8, lines 8-14); and a protective insulation layer 32, 52 covering a sidewall of the semiconductor stack (col. 6, lines 20-22).



This position in the First Office Action is misguided and contradicts the plain language in the relevant portions of Claim 1 on the recited first and second bumps. Claim 1 recites “a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes.” Notably, the contact holes in Claim 1 through which the first bump is electrically connected to the first conductive type semiconductor layer are “arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer.” As discussed above, the First Office Action’s reliance on vias 34 in Shelton as the teaching for the “contact holes” fails to anticipate the recited “contact holes” and,

as such, the above contention on the recited first bump in Claim 1 also fails for lack of support in Shelton.

The First Office Action further relies on the layers 32 and 52 in Shelton (e.g., FIGS. 6 and 10) as the teaching in Shelton for the claimed “protective insulation layer.” In this regard, Claim 1 as amended recites “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” of Claim 1 as amended (with added emphasis). In Shelton, the mesa 24 and the n-layer 22 collectively form a semiconductor stack that applies electrical energy to excite the active layer in the mesa 24 to emit light. The side surfaces of the n layer 22 in the semiconductor stack in Shelton, however, are not covered by either layer 32/30 or layer 52 because the layers 32/30 and 52 are formed above the n-layer 22 and thus cannot cover each side surface of the n-layer 22. Therefore, the teachings in Shelton on layers 32 and 52 fail to disclose and anticipate the above features in Claim 1 as amended.

For at least the above reasons, the First Office Action fails to make a showing that Shelton discloses features recited in Claim 1 as amended. Accordingly, Claim 1 as amended recite multiple features that are missing in Shelton and is patentable under pre-AIA 35 U.S.C. §102 over Shelton.

Claims 2-4, 7, 11-12 and 11-14 are dependent claims of Claim 1 and thus are patentable over Shelton based on the above explanations for Claim 1 and based on their own merits.

REJECTIONS TO CLAIMS 1-3, 5-7 AND 11-15 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER DONOFRIO

The rejections to Claims 1-3, 5-7 and 11-15 over Donofrio at Page 13 of the First Office Action are moot in light of amended Claim 1.

Claim 1 as amended recites “a protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” and this aspect is supported by the original specification, including, Figures 1, 2, 14 and 15 as discussed above in the overview of the ‘851 Patent.

Figure 1

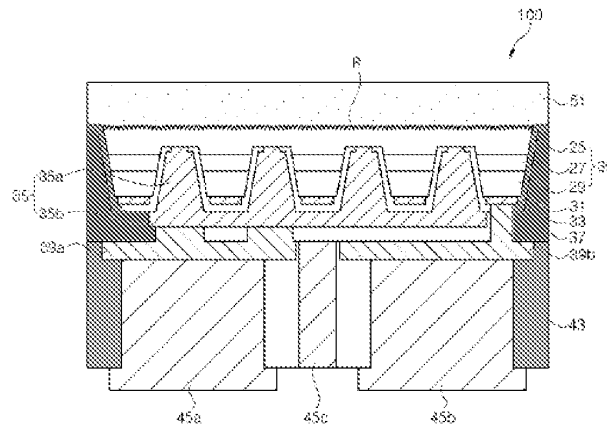


Figure 1 is reproduced to show the protective insulation structure formed by components in blue, red and orange colors to surround the LED package region in the LED package 100. This protective insulation structure is part of the wafer-level structure to surround each individual LED package region from its surroundings and neighboring LED package regions at the wafer level before dividing the wafer into individual LED packages or chips for subsequent packaging processes. This protection can reduce contamination by external environmental factors that may cause the LED layers or structure to deteriorate and adversely affect the device operation, device performance and/or device lifetime, especially considering that LED package device may operate under a high voltage or current and at an elevated temperature. See, e.g., ‘the 851 Patent at 1:33-60; 2:30-55; 6:40-60; 7:13-25; 10:9-23; 14:45-52; 17:26-42. In the example shown in Figure 1, the entire external side surfaces surrounding the LED package 100 are covered by and surrounded by the protective insulation structure. The external side surfaces of the top part of the LED package 100 are slanted external surfaces of the semiconductor stack 30 and are fully covered by the first insulation layer 33 (whose external part is shown in blue) as the first protective insulation layer and is further covered by the top part of the second insulation layer 37 (whose external part is shown in red) over the first insulation layer (whose external part is shown in blue).

Donofrio, however, fails to disclose the claimed “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” and fails to discuss the need for and the benefits of the claimed protective insulation

layer. In fact, Donofrio is completely silent on the technical considerations for having a protective insulation layer covering each external side wall surface of the semiconductor stack.

The First Office Action at Page 13 provides the following explanation to support the rejection:

Donofrio, Figs. 1, 7A, 7B and related text discloses a light emitting diode package 110 having a first conductive type layer 112, a second conductive type layer 114, and an active layer 116 (col. 7, lines 58-64); a plurality of contact holes 118 arranged in the second conductive type semiconductor layer 114 and the active layer 116 which expose the first conductive type semiconductor layer 112 (col. 8, lines 32-35); a first bump 170 on a first side of the semiconductor stack that is connected to the first conductive type semiconductor layer 112 through the holes 118, and a second bump 160 that is electrically connected to the second conductive type semiconductor layer 114 (col. 8, lines 8-17); a protective insulation layer 140 covering a sidewall of the semiconductor stack (col. 8, lines 10-11).

The full paragraph in Donofrio for the above cited section at 8:5-31 is reproduced below:

Continuing with the description of FIG. 1, an anode contact 130, also referred to as a "p-contact", ohmically contacts the p-type layer 114 and extends on the first face 110a of the diode region 110. The anode contact 130 may extend to a greater or less extent on the p-type layer 114 than illustrated in FIG. 1. A transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130. A reflective cathode contact 150, also referred to as an "n-contact" electrically contacts the n-type layer 112 and extends through the transparent insulating layer 140 and onto the transparent insulating layer 140 that is outside the anode contact 130. In some embodiments, the reflective cathode contact 150 may directly and ohmically contact the n-type layer 112. In other embodiments, however, a thin ohmic contact layer, such as a layer of titanium, may provide the actual ohmic contact to the n-type layer 112. The transparent insulating layer 140 and the reflective cathode contact 150 can provide a hybrid reflective structure or "hybrid mirror", wherein the underlying transparent insulating layer 140 provides an index refraction mismatch or index step to enhance the total internal reflection (TIR) from the reflective layer 150 compared to absence of the underlying transparent insulating layer 140. It will also be understood that, in other embodiments, the transparent insulating layer 140 may comprise multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector. Moreover, the reflective cathode contact 150 may also include a plurality of sublayers.

The First Office Action specifically relies on “A transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130” in the above paragraph as the evidence for disclosing the protective insulation layer of Claim 1. Claim 1 as amended explicitly recites the protective insulation layer “covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” (with added emphasis). As discussed above, this feature is advantageous because the protective insulation layer is formed as part of the wafer-level fabrication for forming the LED stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and can protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent packaging processes, and during the normal use of the LED package device after the fabrication.

Donofrio does not disclose this protective insulation layer as recited in Claim 1 and is completely silent on the need for this structure and the advantages provided by this structure. In FIG. 1 of Donofrio, the external side wall surface is not covered by the transparent insulating layer 140.

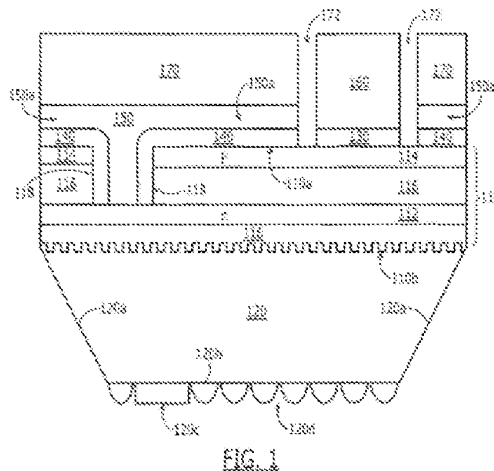


FIG. 1

Donofrio teaches that the transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130 at 8:10-11 and specifically provides examples of extending the layer 140 outside the anode contact 130 by covering top surface of the p-type layer 114 and covering on an inner sidewall of the diode region 110 formed by the via 118.

In Donofrio, the transparent insulating layer 140 is used to provide electrical insulation between the cathode contact 150 in the via 118 for contacting the n-type layer 112 and the p-type layer 114 and the quantum well layers 116. *Id.* at 8:5-15 and 16:7-19. For this function, there is no need for extending the layer 140 to cover external sidewall surfaces. Donofrio also discloses using the layer 104 as an optical reflective layer to direct light downward to improve the optical efficiency of the LED device. *Id.* at 8:20-26 and 9:54-60. Under the teachings of Donofrio, there is no need for the layer 104 to cover each external side wall surface since such a covering layer 104 on the vertical side surface which would reflect light horizontally rather than downward.

Notably, there is not a single statement in Donofrio as to a need for the claimed protective insulation layer in Claim 1. Donofrio is completely silent regarding any technical issues or disadvantages for not covering the external sidewall surfaces by a protective insulation layer. Neither does Donofrio state any benefits for covering each external side wall surface.

Therefore, in light of the teachings in Donofrio and the context of the teachings on the layer 140, the single statement of “A transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130” at 8:10-11 is insufficient as a disclosure of “a protective insulation layer covering each external side wall surface of the semiconductor stack” under pre-AIA 35 U.S.C. §102(b).

Accordingly, the First Office Action fails to show that Donofrio discloses each limitation in Claim 1 as amended. Therefore, Claim 1 as amended is patentable under pre-AIA 35 U.S.C. §102 over Donofrio.

Claims 2-3, 5-7 and 11-15 are dependent claims of Claim 1 and thus are patentable over Donofrio based on the above explanation for Claim 1 and based on their own merits.

REJECTION TO CLAIM 4 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND BEESON

Claim 4, which depends on Claims 1 and 2, is rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Beeson.

Beeson is cited and relied upon for providing a teaching on a wavelength converter in an LED device. However, the disclosure of Beeson does not cure the defects in the disclosure of

Donofrio as discussed above. Therefore, based on the above discussion of Claims 1 and 2, the combined teaching of Donofrio and Beeson fails to disclose each limitation in Claim 4 and fails to render the claimed subject matter in Claim 4 as a whole unpatentable.

REJECTION TO CLAIM 8 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND TAKUMA

Claim 8, which depends on Claims 1 and 7, is rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Takuma.

Takuma is cited and relied upon for providing a teaching related to a dummy bump. However, the disclosure of Takuma does not cure the defects in the disclosure of Donofrio as discussed above. Therefore, based on the above discussion of Claims 1 and 7, the combined teaching of Donofrio and Takuma fails to disclose each limitation in Claim 8 and fails to render the claimed subject matter in Claim 8 as a whole unpatentable.

REJECTION TO CLAIMS 9-10 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND HO

Claim 9, which depends on Claim 1, and its dependent Claim 10 are rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Ho.

Ho is cited and relied upon for providing a teaching related to a heat dissipating structure in LED. However, the disclosure of Ho does not cure the defects in the disclosure of Donofrio as discussed above. Therefore, based on the above discussion of Claim 1, the combined teaching of Donofrio and Ho fails to disclose each limitation in Claims 9-10 and fails to render the claimed subject matter in Claims 9-10 as a whole unpatentable.

CLAIMS 16-35

Claims 16-35 recite features that are missing from the cited prior art based on the discussions of Claims 1-15 as discussed above and based on the additional features in Claims 16-35 that are not in Claims 1-15.

For example, Claims 16-21 recite structures having light emitting diode (LED) packages to include a stack of layers formed over one another and patterned to include an array of LED package regions and each LED package region includes (1) a LED package formed in the stack of layers in a central region of the LED package region and (2) a protective insulation structure formed to surround and protect the LED package from surroundings outside the protective insulation structure and to separate from adjacent LED packages. Claims 16-21 further recite that the protective insulation structure includes a two-layer protective structure having a first protective insulation layer that surrounds and covers each external side wall surface of the semiconductor stack and a second protective insulation layer that forms on the first protective insulation layer to protect the semiconductor stack from an external environment. In light of the disclosure of the cited prior art, the prior art fails to disclose those features in the combination as recited in Claims 16-21.

Next Claims 22-27 recite an electrical contact structure on the first side of the semiconductor stack and electrically coupled to supply the electrical signal to the first and second type semiconductor layers via the contact holes. The recited electrical contact structure includes a first bump, a first electrical contact layer material, a second bump, and a second electrical contact layer material. Claims 22-27 recite an external structure that covers (1) the second side of the semiconductor stack that exports light generated in the active layer outside the LED package, and (2) side wall surfaces of the semiconductor stack. In light of the disclosure of the cited prior art, the prior art fails to disclose those features in the combination as recited in Claims 22-27.

With respect to Claims 28-35, the cited prior art fails to disclose, among others, a LED package as recited in Claims 28-25 with each single light emitting diode including an inclined side wall in the first conductive type semiconductor of its semiconductor stack and a protective insulation layer covering a sidewall of the semiconductor stack of each light emitting diode and having a thickness that varies along the sidewall of the semiconductor stack.

Therefore, Claims 16-35 are patentable over the cited prior art.

CONCLUSION

In light of above explanations and analyses, Patent Owner respectfully submits that the rejections raised in non-final Office Action have been fully addressed and are moot, and that Claims 16-35 as presented in this filing are patentable.

Therefore, Patent Owner respectfully requests the Office to conclude this reexamination proceeding and to issue a reexamination certificate for granting the challenged claims, Claims 1-15, as amended in this filing, and for granting the newly added Claims 16-35.

Please apply the required fees and any charges or credits to Deposit Account No. 50-0665.

REQUEST FOR EXAMINER'S INTERVIEW

In the interest of advancing this proceeding and in compliance with 37 C.F.R. 1.560 governing the interviews in *ex parte* reexamination proceedings, the undersigned respectfully suggests an examiner's interview to be conducted to discuss any outstanding issues that the Office may have in light of the filing of this response.

Respectfully submitted,

Date: March 10, 2017

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Ctrl. No. : 90/013,725
Filed : April 15, 2016
Page : 34 of 34

Ex Parte Reexamination of U.S. Patent No. 9,070,851 B2
Control No.: 90/013,725
Attorney Docket No.: 114898-8904.US00

CERTIFICATE OF SERVICE

I hereby certify that, on March 10, 2017, I caused a true and correct copy of the foregoing
CORRECTION OF INFORMALITY IN PATENT OWNER'S RESPONSE TO OFFICE
ACTION FILED ON SEPTEMBER 19, 2016 in the *ex parte* reexamination of U.S. Patent No.
9,070,851 B2 under Control Number 90/013,725 to be served via First Class U.S. Mail on the
Third Party Requestor via its attorney of record:

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Date: March 10, 2017

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International Application Number:	
Confirmation Number:	7313
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First Named Inventor/Applicant Name:	9070851
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1		SSC_Response.pdf	1135582	yes	34
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	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	33
	Reexam Certificate of Service	34	34
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Ex Parte* reexamination of:
U.S. Patent No. 9,070,851 B2

Inventor: Won Cheol Seo et al.

Confirmation No.: 7313

Control No.: 90/013,725

Examiner: Nguyen, Tuan H.

Filed: April 15, 2016

Art Unit: 3992

For: WAFER-LEVEL LIGHT EMITTING DIODE
PACKAGE AND METHOD OF FABRICATING THE
SAME

Mail Stop *Ex Parte* Reexam

Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

In response to the First Office Action dated September 19, 2016, Patent Owner submits the following amendments and explanations:

Amendments to the Claims are reflected in the listing of claims that begin on page **2** of this paper.

Remarks/Arguments begin on page **10** of this paper.

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A light emitting diode (LED) package, comprising one or more light emitting diodes to emit light, wherein each single light emitting diode includes:

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, ~~the contact holes exposing to~~ penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;

a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; and

a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and

wherein the LED package further includes a protective insulation layer covering each external side wall surface ~~a sidewall~~ of the semiconductor stack facing externally of the LED package so that the protection insulation layer surrounds the LED package.

2. (Original) The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.

3. (Original) The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped single crystal substrate.

4. (Original) The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.

5. (Original) The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.

6. (Original) The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.

7. (Original) The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.

8. (Original) The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.

9. (Original) The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.

10. (Original) The LED package of claim 9, wherein the substrate comprises sapphire or silicon.

11. (Original) The LED package of claim 1, further comprising:
a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and
a second contact layer contacting the second conductive type semiconductor layer,
wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer,
wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.

12. (Original) The LED package of claim 11, further comprising:
a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and
a second electrode pad contacting the second contact layer through a second contact hole

arranged in the second insulation layer and the first insulation layer,

wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.

13. (Original) The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.

14. (Original) A light emitting diode (LED) module, comprising:

a circuit board;

the LED package of claim 1 arranged on the circuit board; and

a lens to adjust an orientation angle of light emitted from the LED package.

15. (Original) The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.

16. (New) A structure having light emitting diode (LED) packages, comprising:

a stack of layers formed over one another and patterned to include an array of LED package regions, each LED package region including (1) a LED package formed in the stack of layers in a central region of the LED package region and (2) a protective insulation structure formed to surround and protect the LED package from surroundings outside the protective insulation structure and to separate from adjacent LED packages,

wherein each LED package formed in the stack of layers includes:

a semiconductor stack including a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack;

contact holes formed as through holes in each semiconductor stack and surrounded by the second conductive type semiconductor layer and the active layer to pass therethrough so as to expose the first conductive type semiconductor layer;

a first electrical contact layer material filling in the contact holes to be electrically coupled to the first conductive type semiconductor layer and connecting the first contact holes;
a first bump on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the first electrical contact layer material; and
a second bump on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor layer, and
wherein the protective insulation structure includes a two-layer protective structure having a first protective insulation layer that surrounds and covers each external side wall surface of the semiconductor stack and a second protective insulation layer that forms on the first protective insulation layer to protect the semiconductor stack from an external environment.

17. (New) The structure as in claim 16, comprising a wafer on which the stack of layers is formed and is patterned to include the array of LED package regions.

18. (New) The structure as in claim 16, wherein each of the contact holes is tapered to have a larger end facing the second side and a smaller end facing the first side.

19. (New) The structure as in claim 16, wherein:
the protective insulation structure further covers an entirety of each external side surface of an electrical contact structure that includes the first and second bumps on the first side of the semiconductor stack to protect the electrical contact structure from an external environment.

20. (New) The structure as in claim 16, wherein:
each contact hole is formed to extend into a portion of the first conductive type semiconductor layer so that a portion of the first electrical contact material reaches into the portion of the first conductive type semiconductor layer to be in contact with the first conductive type semiconductor layer.

21. (New) The structure as in claim 16, wherein each LED package formed in the stack of layers includes:
a dummy bump that is electrically conductive, formed on the first side of the

semiconductor stack between the first and second bumps to be electrically insulated from the first and second bumps to dissipate heat from the LED package.

22. (New) A light emitting diode (LED) package, comprising:

a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, wherein the semiconductor stack is located between a first side and a second side of the semiconductor stack that are on opposite sides of the semiconductor stack, and wherein the first side is closer to the second conductive type semiconductor layer than the first conductive type semiconductor layer and the second side is closer to the first conductive type semiconductor layer than the second conductive type semiconductor layer;

contact holes formed as through holes in the semiconductor stack within an area for a single light emitting diode to be surrounded by the second conductive type semiconductor layer and the active layer to pass therethrough so as to expose the first conductive type semiconductor layer within openings created by the contact holes;

an electrical contact structure on the first side of the semiconductor stack and electrically coupled to supply the electrical signal to the first and second type semiconductor layers via the contact holes, the electrical contact structure including (1) a first bump formed of an electrically conductive material and arranged on the first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer as part of a first electrical contact path to the semiconductor stack via the contact holes, (2) a first electrical contact layer material disposed to fill in the contact holes and to electrically couple the first conductive type semiconductor layer and the first bump via the contact holes, (3) a second bump formed of the electrically conductive material of the first bump and arranged on the first side of the semiconductor stack and electrically insulated from the first bump to be electrically coupled to the second conductive type semiconductor, and (4) a second electrical contact layer material electrically coupled between the second bump and the second conductive type semiconductor layer; and

an external structure that covers (1) the second side of the semiconductor stack that

exports light generated in the active layer outside the LED package, and (2) side wall surfaces of the semiconductor stack.

23. (New) The LED package as in claim 22, wherein the external structure includes:
a first stacked protective insulation structure positioned to cover the entirety of each
external side wall surface of the semiconductor stack to protect the semiconductor stack from an
external environment; and

a second stacked protective insulation structure stacked over the first stacked protective
insulation structure and located on the first side of the semiconductor stack to cover an entirety
of each external side surface of the electrical contact structure to protect the electrical contact
structure from an external environment.

24. (New) The LED package as in claim 22, wherein:
the external structure further covers external side wall surfaces of the electrical contact
structure on the first side of the semiconductor stack.

25. (New) The LED package as in claim 22, wherein the external structure includes:
a first protective insulation layer covering an entirety of each external side wall surface of
the semiconductor stack; and

a second protective insulation layer that surrounds the semiconductor stack and forms on
the first protective insulation layer so that the second protective insulation layer and the first
protective insulation collectively form a two-layer protection structure to cover the entirety of
each external side wall surface of the semiconductor stack and to enclose external sides of the
semiconductor stack.

26. (New) The LED package as in claim 22, wherein the composite insulation structure
includes a phosphor structure that is formed of a phosphor composition that converts light emitted
from the active layer into light at a different wavelength to be exported on the second side out of
the LED package.

27. (New) The LED package as in claim 22, further comprising:
a dummy bump formed of the electrically conductive material and arranged on the first
side of the semiconductor stack near the first bump or second bump to dissipate heat from the

LED package, wherein the dummy bump is not electrically connected to the first bump or the second bump.

28. (New) A light emitting diode (LED) package, comprising one or more light emitting diodes to emit light, wherein each single light emitting diode includes:

a semiconductor stack comprising a first conductive type semiconductor layer, a second conductive type semiconductor layer and an active layer that is interposed between the first and second semiconductor layers to generate light under an electrical signal applied to the first and second type semiconductor layers, the first conductive type semiconductor layer shaped to include an inclined side wall;

a plurality of contact holes arranged in, and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer;

a first bump arranged on a first side of the semiconductor stack and electrically coupled to the first conductive type semiconductor layer via the plurality of contact holes;

a second bump arranged on the first side of the semiconductor stack and electrically coupled to the second conductive type semiconductor layer; and

a protective insulation layer covering a sidewall of the semiconductor stack of each light emitting diode and having a thickness that varies along the sidewall of the semiconductor stack.

29. (New) The LED package of claim 28, wherein the protective insulation layer includes a two-layer protective structure having a first protective insulation layer that includes a uniform thickness along the sidewall of the semiconductor stack and a second protective insulation layer that has a varying thickness along the sidewall of the semiconductor stack.

30. (New) The LED package of claim 28, wherein the second protective insulation layer is formed on the first protective insulation layer.

31. (New) The LED package of claim 28, wherein the protective insulation layer covers side walls of the first conductive type semiconductor layer, the active layer, and the second conductive type semiconductor layer.

32. (New) The LED package of claim 28, wherein each single light emitting diode further includes:

a first contact layer electrically coupling the first conductive type semiconductor layer and the first bump via the contact holes; and

a second contact layer electrically coupled between the second conductive type semiconductor layer and the second bump,

wherein the protective insulation layer extends to cover the second contact layer, the extended portion of the protective insulation layer having a size greater than that of the second contact layer.

33. (New) The LED package of claim 28, wherein the protective insulation layer includes an optically reflective structure to reflect light towards a second side of the semiconductor stack that is opposite to the first side of the semiconductor stack.

34. (New) The LED package of claim 28, wherein the protective insulation layer has an inclined shape along the sidewall of the semiconductor stack.

35. (New) The LED package as in claim 28, wherein each light emitting diode further includes:

a dummy bump formed of an electrically conductive material and arranged on the first side of the semiconductor stack between the first and second bumps to dissipate heat from the LED package, wherein the dummy bump is electrically insulated from the first and second bumps.

REMARKS

Patent Owner acknowledges the helpful written explanations by Examiner Mr. Tuan Nguyen with respect to the rejections to Claims 1-15 of the U. S. Patent No. 9,070,851 B2 (“the ‘851 Patent”) in the First Office Action dated September 19, 2016. Additionally, Patent Owner thanks Mr. Tuan Nguyen, Mr. Minh Nguyen and Mr. Timothy Speer for the telephonic interview with Patent Owner’s counsel on November 17, 2016.

In response, Patent Owner has amended Claims 1-15 by amending Claim 1 and respectfully requests the Office to reconsider and withdraw the outstanding rejections in light of the teachings in the cited prior art and the analyses of such teachings presented in this filing. Specifically, Claims 1-15 as amended and presented in this filing are distinctly different from the prior art teachings relied upon in the First Office Action and are patentable over the cited prior art under the grounds raised.

As part of this response, in addition to amending Claim 1, Patent Owner submits additional Claims 16-35 based on the original specification for consideration by the Office in this proceeding and requests the Office to allow those claims in light of the facts and analyses presented for Claims 1-15 and further in light of the additional features recited in those claims.

The Office sets a shortened statutory period of three months for Applicant’s response by December 19, 2016 (Page 1 of the First Office Action). Accordingly, this response is filed timely.

SUMMARY OF THE EXAMINER’S INTERVIEW INITIATED BY PATENT OWNER

On November 17, 2016, in response to Patent Owner’s request, Mr. Tuan Nguyen, Mr. Minh Nguyen and Mr. Timothy Speer conducted an interview with Patent Owner’s counsel to discuss the cited prior art and rejections in the First Office Action. During the interview, the teachings in cited Seiichiro, Shelton and Donofrio and technical features disclosed and claimed in the ‘851 Patent were discussed. In addition, technical features disclosed in the ‘851 Patent for potential claim amendments to Claim 1 and other claims were discussed. No specific agreements were reached at the interview.

See also “Ex Parte Reexamination Interview Summary” issued by the Office with a mailing date of November 25, 2016.

STATUS OF CLAIMS

Claims 1-15 as originally issued in the '851 Patent are subject to reexamination and are rejected in the First Office Action in response to a third party request.

Patent Owner has amended the claims: Claim 1 has been amended based on the original specification of the '851 Patent; and Claims 16-35 have been newly added based on the original specification of the '851 Patent, including, e.g., Figures 1-27 and associated textual description. No new matter has been added.

Upon entry of the claim amendments, Claims 1-35 are under consideration in this proceeding.

APPLICABLE LAW ON PATENTABILITY

The '851 Patent is based on the U.S. Patent Application No. 13/194,317 filed on July 29, 2011 which was timely filed to claim priorities from Korean Patent Application Nos. 10-2010-0092807 and 10-2010-0092808, both filed on September 24, 2010. Therefore, pre-AIA 35 U.S.C. §102 and 103 are applicable to the patentability of each claim of the '851 Patent in this proceeding.

OVERVIEW OF CERTAIN ASPECTS OF THE '851 PATENT

The '851 Patent, entitled "Wafer-level light emitting diode package and method of fabricating the same," describes wafer-level LED structures with LED package regions to provide protective insulation structure designs as part of the wafer-level structures to protect each individual LED package region from its surroundings and neighboring LED package regions at the wafer level before dividing the wafer into individual LED packages or chips for subsequent packaging processes.

The '851 Patent includes aspects of the disclosed technology regarding dividing the monolithically formed LED package regions grown on a wafer for further processing. When the divided LED package regions are not properly protected, this dividing operation can expose the diced LED packages to the surrounding environment in subsequent processes such as mounting each individual LED package on a circuit board, forming electrical contacts to the mounted circuit board and placing a covering molding member and other steps to form final LED devices. An unprotected diced LED package can be inadvertently contaminated by external

environmental factors and such contamination can cause the LED layers or structure to deteriorate and adversely affect the device operation, device performance and/or device lifetime, especially considering that LED package devices may operate under high voltages or currents and at elevated high temperatures. See, e.g., ‘the 851 Patent at 1:33-60; 2:30-55; 6:40-60; 7:13-25; 10:9-23; 14:45-52; 17:26-42.

In this regard, the ‘851 Patent discloses the recognitions of the above technical issues in fabricating LED devices by the inventors and include Figures 1-27 to illustrate features of its protective insulation layer designs as part of the wafer-level structures. Specifically, the ‘851 Patent show four exemplary embodiments wafer-level protective insulation layer designs in Figures 1, 2, 14 and 15.

For easy reference, Patent Owner reproduces below the annotated versions of Figures 1, 2, 14 and 15 with added colors to illustrate how each LED package region among an array of LED package regions is surrounded by an individual “protective cage” at the wafer level processing and is separated from neighboring LED package regions before being diced into individual LED chips for further packaging.

Figure 1 in the ‘851 Patent shows a cross section view of one LED package region 100 where the protective insulation structure surrounding the LED package region is shown by components in blue, red and orange colors.

Figure 1

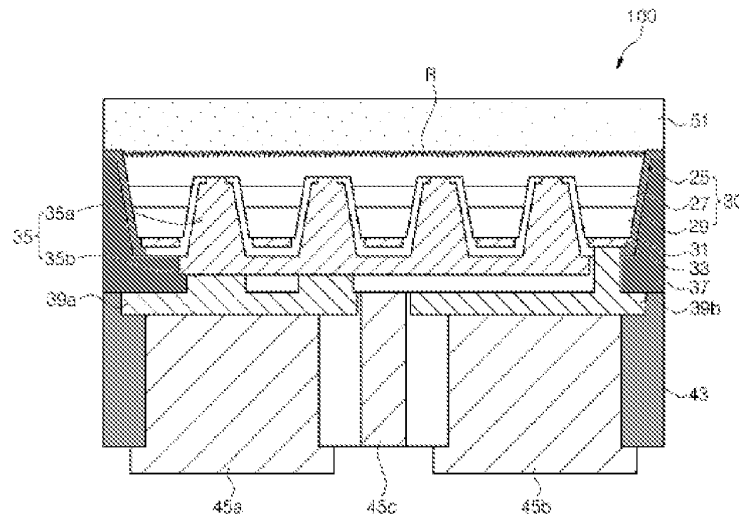


Figure 1 of the ‘851 Patent (Annotated)

In the LED package 100 in Figure 1, the semiconductor stack 30 includes a first conductive type upper semiconductor layer 25, an active layer 27, and a second conductive type lower semiconductor layer 29. The active layer 27 is interposed between the upper and lower semiconductor layers 25, 29. *Id.* at 5:12-23. In this example, four contact holes are formed inside the semiconductor stack 30 and are surrounded by the second conductive type lower semiconductor layer 29 and the active layer 27 to pass through the layers 29 and 27 so as to reach and expose the first conductive type upper semiconductor layer 25. See also, *Id.* at Figures 5(a) and 5(b). Those four contact holes are filled with contact sections 35a contacting the first conductive type upper semiconductor layer 25. *Id.* at 5:24-49. The LED package 100 may include a first contact layer 35, a second contact layer 31, a first insulation layer 33 (in blue), a second insulation layer 37 (in red), a first electrode pad 39a, a second electrode pad 39b, a first bump 45a, and a second bump 45b. The LED package 100 may further include an insulation layer 43 (in orange), a dummy bump 45c, and a wavelength convertor 51. *Id.* at 5: 12-18.

The first contact layer 35 is located under the first insulation layer 33 and contacts the first conductive type upper semiconductor layer 25 through the first insulation layer 33 in the plurality of contact holes 30a. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25, and a connecting section 35b connecting the contact sections 35a to each other. Therefore, the contact sections 35a are electrically connected to each other by the connecting section 35b. The first contact layer 35 is formed under some regions of the first insulation layer 33 and may be composed of a reflective metal layer. *Id.* at 6:5-22.

Notably, Figure 1 shows that, in the specific embodiment as illustrated, the entire external side surfaces surrounding the LED package 100 are covered by and surrounded by the protective insulation structure. The external side surfaces of the top part of the LED package 100 are slanted external surfaces of the semiconductor stack 30 and are fully covered by the first insulation layer 33 (with its external part being shown in blue) as the first protective insulation layer and is further covered by the top part of the second insulation layer 37 (with its external part being shown in red) over the first insulation layer (with its external part being shown in blue). This is an example of a two-layer protective structure outside the semiconductor stack 30.

In addition, in the embodiment in Figure 1, the external side surfaces of the middle part of the LED package 100 are the external side surfaces of the connecting section 35b and the first

electrode pad 39a (on the left-hand side external surface), and the external side surfaces of the second electrode pad 39b (on the right-hand side external surface) that are located in and under the second insulation layer 37. *Id.* at 6:23-39. As illustrated in Figure 1, those middle part external side surfaces are covered, and surrounded by external parts of the first and second insulation layers 33 and 37 as shown in blue and red and the top external part of the insulation layer 43 as shown in orange.

Furthermore, in the specific embodiment in Figure 1, the external side surfaces of the lower part of the LED package 100 shown in Figure 1 are the external side surfaces of the external surfaces of the first bump (on the left-hand side external surface), and the external side surfaces of the second bump 45b (on the right-hand side external surface). The entire exposed external side surfaces of the bumps 45a and 45b are covered and surrounded by external parts of the insulation layer 43 as shown in orange. In Figure 1, the bottom parts of the bumps 45a and 45b have protruded sections that are used to connect to the circuit board for the LED package 100.

Therefore, Figure 1 shows an example of a protective insulation structure formed together with the semiconductor stack 30 during wafer-level fabrication of the semiconductor stack for the LED package 100 to include external parts of the first and second insulation layers 33 (in blue) and 37 (in red) and the external part of the insulation layer 43 (in orange) to surround and cover the entire side wall surfaces of the LED package 100 below the wavelength converter 51 to protect, the semiconductor stack 30 and the underlying electrical contact parts (35b, 39a, 39b, 45a and 45b) from an external environment.

Specifically, the disclosed protective insulation layer designs in the '851 Patent are built into the wafer-level structures to have built-in protection as an individual protective cage or structure for surrounding each LED package region on a wafer from external environmental factors. This protective structure for each LED package region is formed as part of the wafer-level fabrication for forming the LED semiconductor stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and will protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent packaging processes, and during the normal use of the LED package device after the fabrication.

Therefore, the disclosed protective insulation layer designs in the '851 Patent protect the individual LED packages or devices in both fabrication phase and the product use phase.

In light of the above example of a protective insulation structure in Figure 1 in the '851 Patent, the other three examples shown in Figures 2, 14 and 15 are different designs based on the similar basic protection concept illustrated in Figure 1 but provide an additional protective insulation layer 49 or 141 to the protective insulation structure shown in a purple color. The insulation substrate 61 in Figure 2 and the insulation substrate 161 in Figures 14 and 15 correspond to the insulation layer 43 in Figure 1.

Figure 2

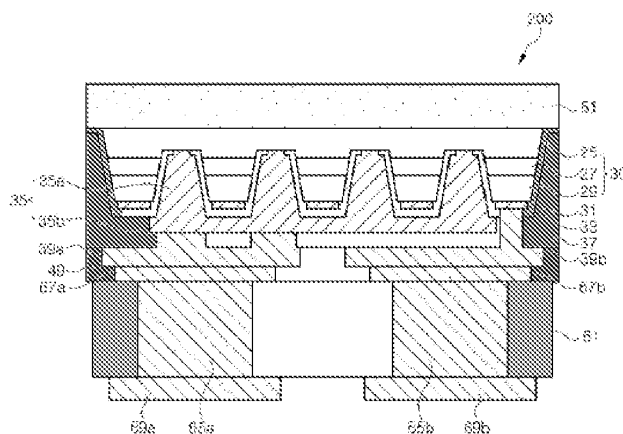


Figure 2 of the '851 Patent (Annotated)

Figure 14

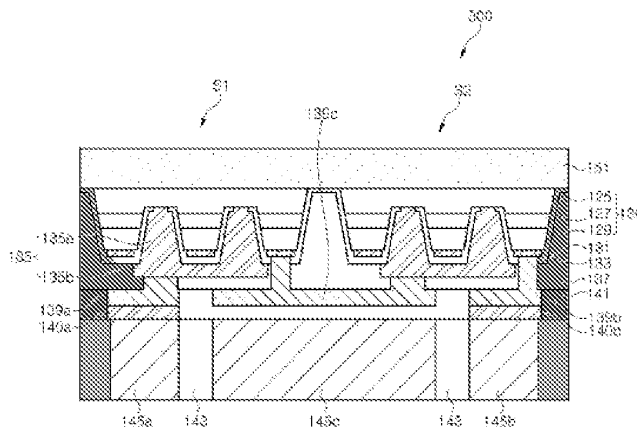


Figure 14 of the '851 Patent (Annotated)

Figure 15

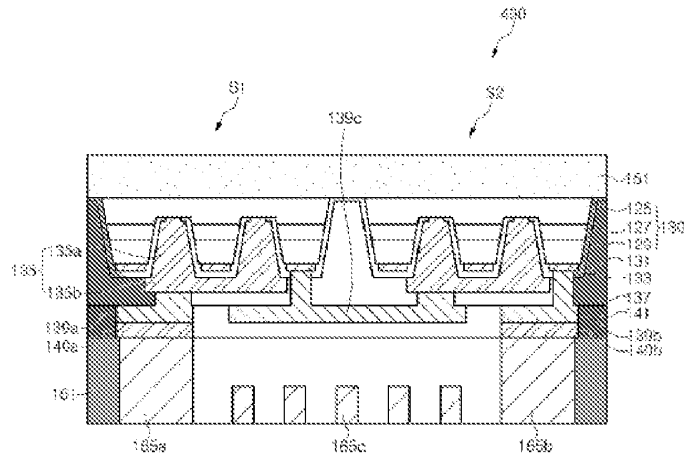


Figure 15 of the '851 Patent (Annotated)

In the exemplary design in Figure 2, to prevent the first and second electrode pads 39a, 39b from being exposed to the outside, the '851 Patent teaches a use of an insulation layer 49 to cover side surfaces and bottom surfaces of the first and second electrode pads 39a, 39b. The insulation layer 49 may have openings, which expose the first and second electrode pads 39a, 39b, and additional metal layers 67a, 67b are then formed in the openings. *Id.* at 7: 46-60. The external parts of the insulation layer 49 is located between the insulation layer 37 and the insulation substrate 61. Therefore, similar to the protective insulation structure shown in colors in Figure 1, the protective insulation structure shown in colored parts of the insulation layers 33, 37, and 49 and the insulation substrate 61 provides built-in protection as an individual protective cage for each LED package region on a wafer from external environmental factors. The designs in Figures 14 and 15 are similar in this regard.

As explained in detail below, the prior art teachings cited in the First Office Action are different in multiple aspects from the protective insulation structure designs in the '851 Patent. For example, none of the cited prior art reference discloses the above wafer level built-in protective insulation structures for individual LED package regions and maintain such structures through the wafer division, subsequent processing and packaging and in the final individual LED devices. The claimed subject matter in Claims 1-15 in the '851 Patent is supported by the

technical disclosures and the LED package designs and the above protective insulation structure designs and is patentable over the prior art teachings cited in the First Office Action.

In another aspect, the '851 Patent discloses built-in heat dissipation bumps that are distinct from the electrical bumps, e.g., the bump 45c between the electrical bumps 45a and 45b in Figure 1, the bump 145c between the electrical bumps 145a and 145b in Figure 14, and bumps 165c between the electrical bumps 165a and 165b in Figure 15. The bumps 45c, 65c and 165c are electrically "dummy" bumps that do not function as electrical paths or connections but are provided to dissipate heat generated in the LED packages. In some LED package designs, such as the examples in Figures 1, 14 and 15, the built-in heat dissipation bumps can be implemented along with the protective insulation structure designs to improve the performance of the LED packages.

The following sections discuss each of the rejections from Page 5 through Page 21 of the First Office Action in the order as appeared therein.

REJECTIONS TO CLAIMS 1-4, 7, 9 AND 11 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER SEIICHIRO

The rejections to Claims 1-4, 7, 9 and 11 over Seiichiro in the First Office Action at Page 5 should be withdrawn because the cited teachings in Seiichiro fail to anticipate those claims as presented in this filing.

The analysis of Claim 1 in the First Office Action at Page 5 is reproduced below:

Regarding to claim 1:

Seiichiro, Figs. 1-3 as shown below, discloses a light emitting diode package including a semiconductor stack comprising a first conductivity type (i.e. n-type) semiconductor layer 12, an active layer 13, and a second conductive type (i.e. p-type) semiconductor layer 14, a plurality of contact holes arranged in the second conductive type semiconductor layer 14 and the active layer 13, the contact holes exposing the first conductive type semiconductor layer 12; a first bump 21, 24 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 12 via the plurality of contact holes; a second bump 26 arranged on the first side of the of the conductor stack, the second bump 26 being electrically connected to the second conductive type semiconductor layer 13; and a protective insulation layer 17, 30 covering a sidewall of the semiconductor stack.

Based on a review of the above cited portions in Seiichiro, Patent Owner respectfully submits that the cited teachings in Seiichiro are different from the subject matter in Claim 1 as

amended and thus do not support the contended mapping between Seiichiro and Claim 1 as amended.

Claim 1 as amended recites a light emitting diode (LED) package that includes, among others, “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer” and “a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” within each single light emitting diode.

The recited “contact holes” are supported by the specification of the ‘851 Patent, including, e.g., the contact holes 35a that are surrounded by the layers 29 and 27 to pass through layers 29 and 27 to reach and expose the layer 28, as illustrated in an example in Figures 5(a) and 5(b) which are reproduced below.

Figure 5

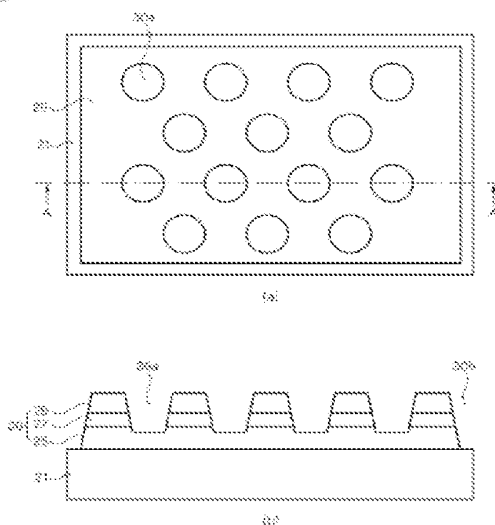


Figure 5 of the ‘851 Patent

The First Office Action generally mentions openings in layers 13 and 10 in Figures 1-3 of Seiichiro to expose the layer 12. However, the First Office Action fails to support this position by a specific illustration or text description in Seiichiro. Figures 2 and 3 in Seiichiro show cross sectional views of the different layers in Seiichiro and thus are reproduced below.

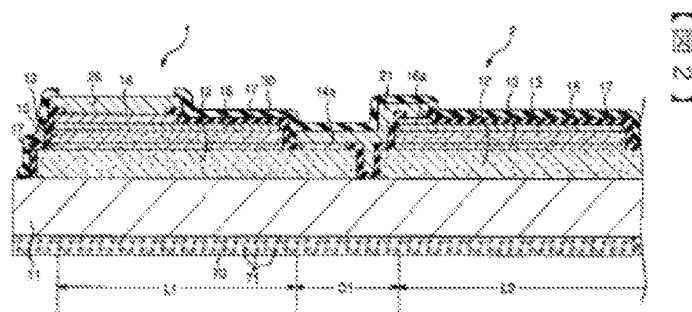


Figure 2 of Seichiro

Figure 2 of Seichiro shows a cross sectional view of two adjacent LED elements 1 and 2. In each LED element 1 or 2, Seichiro does not teach two or more contact holes in layers 13 and 10 to expose the layer 12. Figure 3 shows a cross sectional view of the LED element 3 and does not disclose two or more contact holes in layers 13 and 10 to expose the layer 12.

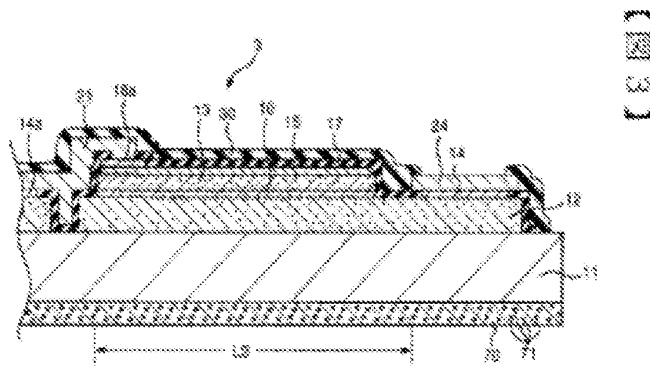


Figure 3 of Seichiro

In addition, Figure 1 shows the top view of the structure having the LED elements 1, 2 and 3 shown in Figures 2 and 3 and does not show two or more contact holes in layers 13 and 10 to expose the layer 12 in any of the LED element 1, 2 or 3.

In other parts of Seichiro, Seichiro describes openings in form of grooves or trenches in the embodiment in Figures 1-3, e.g., an isolation groove or trench 41 in [0021] and through holes 61 and 62 related to the embodiment 2 in Figure 4.

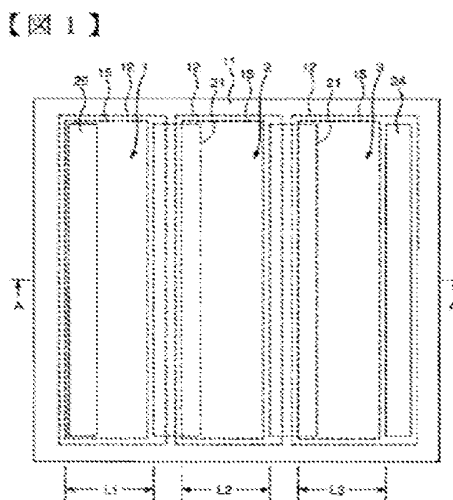


Figure 1 of Seichiro

However, the isolation groove or trench 41 in [0021] is not surrounded by the second conductive type semiconductor layer and the active layer because of their open ended structures. In addition, Seichiro fails to show two or more contact holes in each LED element 1 or 2.

Therefore, nothing in Seichiro teaches the recited contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer in Claim 1 as amended.

Additionally, the First Office Action fails to demonstrate a teaching in Seichiro on the recited first and second bumps arranged on the first side of the semiconductor stack in Claim 1. Specifically, the First Office Action points to the element 26 on top of the top p-layer 13 which is above the active layer 10 and the n-layer 12 in Figure 1 in Seichiro as the recited second bump in Claim 1. Under this mapping, the First Office Action appears to correspond to the space above the top p-layer 12 to the recited “first side of the semiconductor stack” of Claim 1.

In this regard, the First Office Action further points to elements 21, 24 in Figure 1 as the recited first bump arranged on the first side of the semiconductor stack in Claim 1. This contention, however, is based on an incorrect understanding of the technical nature of the element 21 or 24 in Figure 1 in Seichiro.

The element 21 in Seiichiro is a connection electrode that interconnects two adjacent LED elements 1 and 2 and is continuously formed so as to extend over the n-side ohmic electrode 14a of the LED element 1, the insulating film 17 formed in the separation trench 41, and the p-side ohmic electrode 16a of the LED element 2, to electrically connect the n-side ohmic electrode 14a of the LED element 1 to the p-side ohmic electrode 16a of the LED element 2. Therefore, the connection electrode 21 has a portion in the LED element 1 that is either in the same layer as the top p-layer 13 or below the top p-layer 13 as shown by Figure 1 within the LED element 1 and thus cannot be arranged “on the first side” as the element 26 on top of the top p layer 13. The same connection electrode 21 has a portion that is in the LED element 2 and is on top of the p-layer 12 in the LED element 2 rather than in the LED element 1. See Seiichiro at [0027] and [0028]. Therefore, the First Office Action is defective in providing the proper teaching in Seiichiro. The above analysis of the Seiichiro design also demonstrates that Seiichiro teaches a very different LED device structure for interconnecting two adjacent LED elements and thus does not disclose the features as recited in Claim 1 within one light emitting diode.

Specifically, the element 24 in Figure 3 of Seiichiro is an external connection electrode formed over the n-pad electrode 14 of the LED element 3 and, within the LED element 3, is either in the same layer as the top p-layer 13 or below the top p-layer 13 as shown by Figure 3 within the LED element 3 and thus cannot be arranged “on the first side” on top of the top p-layer 13 in the LED element 3.

Claim 1 is amended to explicitly state that the LED package further includes a protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package.

As explained above in the “Overview of the ‘851 Patent” section, this aspect of Claim 1 as amended is supported by the disclosed protective insulation layer designs in the ‘851 Patent as the wafer-level structures to have built-in protection as an individual “protective cage” for surrounding each LED package region on a wafer from external environmental factors. This protective cage for each LED package region is formed as part of the wafer-level fabrication for forming the LED semiconductor stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and will protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent

packaging processes, and during the normal use of the LED package device after the fabrication. Seiichiro fails to disclose this aspect of Claim 1 as amended.

The First Office Action merely points to one sectional view of the layer 17, 30 in Figure 2 or 3 along one direction A-A' as marked in Figure 1 in Seiichiro. This illustration in Seiichiro, however, fails to provide sufficient teaching under 35 U.S.C. §102 to show that “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” of Claim 1 as amended. There is no such teaching in Seiichiro because Seiichiro is completely silent as to the adverse environmental contamination by moisture and others when dividing a wafer into separate LED packages and in subsequent packaging and fabrication processes.

For at least the above defects in the disclosure of Seiichiro, the First Office Action fails to make a showing that Seiichiro discloses each claim limitation in Claim 1 as amended. Therefore, Claim 1 as amended recites multiple features that are missing in Seiichiro and is patentable under 35 U.S.C. §102 over Seiichiro.

Claims 2-4, 7, 9 and 11 are dependent claims of Claim 1 and thus are patentable over Seiichiro based on the above explanations for Claim 1 and based on their own merits.

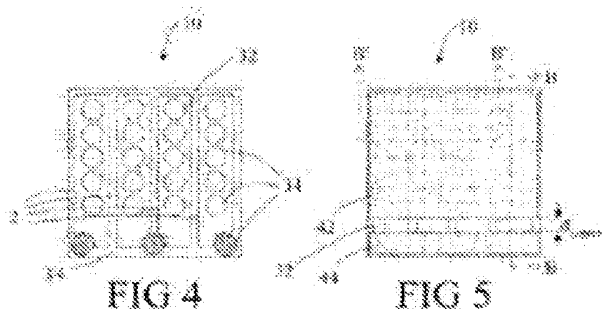
REJECTIONS TO CLAIMS 1-4, 7, 11-12 AND 14-15 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER SHELTON

The rejections to Claims 1-4, 7, 11-12 and 11-14 over Shelton in the First Office Action at Pages 9-11 are traversed because the cited teachings in Shelton fail to support the rejections as contended.

Claim 1 as amended recites a light emitting diode (LED) package that includes, among others, “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer” and “a plurality of contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” within each single light emitting diode.

The First Office Action at Page 10 contends the vias 34 shown in FIGS. 4 and 5 and described at 6:44-45 correspond to the recited plurality of contact holes in Claim 1:

a plurality of contact holes 34 arranged in the second conductive type semiconductor layer 24 and the active layer, the contact holes exposing the first conductive type semiconductor layer 22 (Figs. 4-5, col. 6, lines 44-45);



The above characterization of the vias 34 of Shelton, however, lacks support in Shelton and misapplies the teachings in Shelton.

First, referring to FIGS. 1-3 in Shelton in connection with FIGS. 4-5 in Shelton, those figures and related text in Shelton do not disclose contact holes that pass through p-layer and active layer within the mesa 24 to expose the n-layer. Further referring to other drawings in FIGS. 1-13, the mesa 24 that contains the p-layer and the active layer in Shelton has no contact holes. The contact to the n-layer is achieved outside the mesa 24 by the n-contact 14 in contact with the n-layer 22.

Second, the vias 34 in FIGS. 4 and 5, which are contended to be the “contact holes” in Claim 1 by the First Office Action, are formed in a dielectric layer 32 to access the p-type electrode 12 and the n-type electrode 14 at 6:7-19:

To address this problem, a bonding pads formation process described with reference to FIGS. 4–11 is employed to adapt the fine features of the electrodes 12, 14 to the larger tolerance of the flip chip bonding process. The bonding pads formation process includes formation of a fanning layer 30 as shown in FIGS. 4–7. Formation of the fanning layer 30 includes depositing a dielectric layer 32 in which vias 34 are formed to provide access to the p-type electrode 12 and the n-type electrode 14, followed by metallization processing that fills the vias 34 with an electrically conductive material 36 and that forms intermediate connecting pads, specifically an intermediate p-type connecting pad 42 and an intermediate n-type connecting pad 44.

Under the teaching by Shelton, the dielectric layer 32 is formed after the formation of the layers or structures 22, 24, 12 and 14 and, specifically, is on top of the layers or structures 22, 24, 12 and 14. Notably, the dielectric layer 32 is located on top of the mesa 24 and, accordingly, the vias 34 formed in the dielectric layer 32 at the position of the mesa 24 are also on top of the mesa 34 and cannot be contact holes arranged in the p-layer and the active layer inside the mesa 24. Therefore, vias 34 in Shelton cannot be “contact holes arranged in ... the second conductive type semiconductor layer and the active layer” as recited in Claim 1 as amended (with added emphasis).

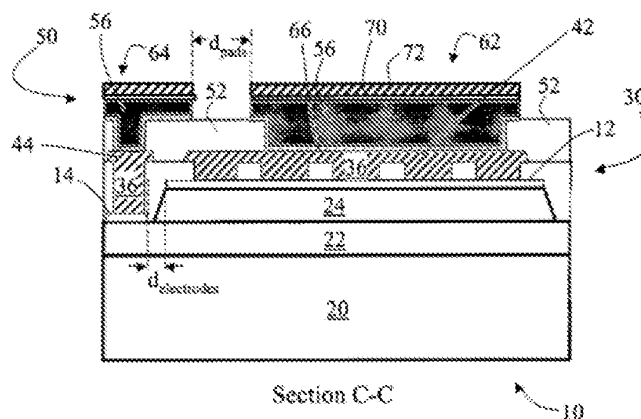
In addition, Shelton teaches that the vias 34 are used to access from the top of the dielectric layer 32 to contact the p-type electrode 12 that is above the mesa 24 and the n-layer 22. Therefore, the vias 34 in the dielectric layer 32 cannot be contact holes inside the mesa 24 underneath the p-type electrode 12. Accordingly, the vias 34 in Shelton cannot be “contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer” as in Claim 1 as amended (with added emphasis).

Therefore, the First Office Action’s reliance on the vias 34 in FIGS. 4 and 5 fails to support a teaching in Shelton of “contact holes arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer” of Claim 1 as amended.

Accordingly, Claim 1 as amended is distinct from Shelton and is patentable under 35 U.S.C. §102.

The First Office Action also cites the electrically conductive material 56 in the dielectric layer 52 of FIG. 10 in Shelton as a teaching in Shelton for the recited first bump and the recited second bump in Claim 1 (Page 10 of the First Office Action):

a first bump 56 arranged on a first side of the semiconductor stack, extending through the opening in dielectric material 52 and electrically connected to the first conductive type semiconductor layer 22, and a second bump 56 extending through the opening in the dielectric material and electrically connected to the second conductive type semiconductor layer 24 (Fig. 10, col. 8, lines 8-14); and a protective insulation layer 32, 52 covering a sidewall of the semiconductor stack (col. 6, lines 20-22).



This position in the First Office Action is misguided and contradicts the plain language in the relevant portions of Claim 1 on the recited first and second bumps. Claim 1 recites “a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes.” Notably, the contact holes in Claim 1 through which the first bump is electrically connected to the first conductive type semiconductor layer are “arranged in and surrounded by the second conductive type semiconductor layer and the active layer, to penetrate through the second conductive type semiconductor layer and the active layer to expose the first conductive type semiconductor layer.” As discussed above, the First Office Action’s reliance on vias 34 in Shelton as the teaching for the “contact holes” fails to anticipate the recited “contact holes” and,

as such, the above contention on the recited first bump in Claim 1 also fails for lack of support in Shelton.

The First Office Action further relies on the layers 32 and 52 in Shelton (e.g., FIGS. 6 and 10) as the teaching in Shelton for the claimed “protective insulation layer.” In this regard, Claim 1 as amended recites “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” of Claim 1 as amended (with added emphasis). In Shelton, the mesa 24 and the n-layer 22 collectively form a semiconductor stack that applies electrical energy to excite the active layer in the mesa 24 to emit light. The side surfaces of the n layer 22 in the semiconductor stack in Shelton, however, are not covered by either layer 32/30 or layer 52 because the layers 32/30 and 52 are formed above the n-layer 22 and thus cannot cover each side surface of the n-layer 22. Therefore, the teachings in Shelton on layers 32 and 52 fail to disclose and anticipate the above features in Claim 1 as amended.

For at least the above reasons, the First Office Action fails to make a showing that Shelton discloses features recited in Claim 1 as amended. Accordingly, Claim 1 as amended recite multiple features that are missing in Shelton and is patentable under pre-AIA 35 U.S.C. §102 over Shelton.

Claims 2-4, 7, 11-12 and 11-14 are dependent claims of Claim 1 and thus are patentable over Shelton based on the above explanations for Claim 1 and based on their own merits.

REJECTIONS TO CLAIMS 1-3, 5-7 AND 11-15 UNDER PRE-AIA 35 U.S.C. § 102(B) OVER DONOFRIO

The rejections to Claims 1-3, 5-7 and 11-15 over Donofrio at Page 13 of the First Office Action are moot in light of amended Claim 1.

Claim 1 as amended recites “a protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” and this aspect is supported by the original specification, including, Figures 1, 2, 14 and 15 as discussed above in the overview of the ‘851 Patent.

Figure 1

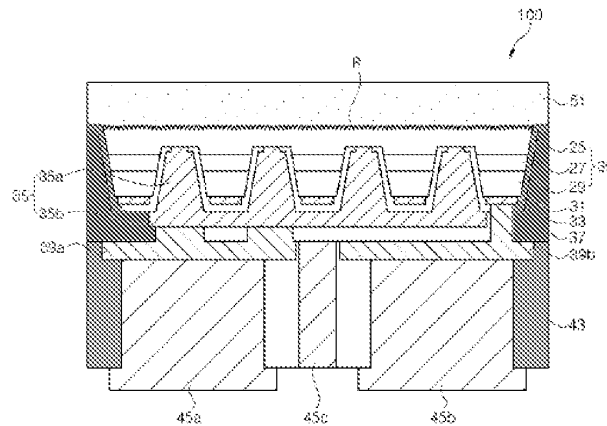


Figure 1 is reproduced to show the protective insulation structure formed by components in blue, red and orange colors to surround the LED package region in the LED package 100. This protective insulation structure is part of the wafer-level structure to surround each individual LED package region from its surroundings and neighboring LED package regions at the wafer level before dividing the wafer into individual LED packages or chips for subsequent packaging processes. This protection can reduce contamination by external environmental factors that may cause the LED layers or structure to deteriorate and adversely affect the device operation, device performance and/or device lifetime, especially considering that LED package device may operate under a high voltage or current and at an elevated temperature. See, e.g., ‘the 851 Patent at 1:33-60; 2:30-55; 6:40-60; 7:13-25; 10:9-23; 14:45-52; 17:26-42. In the example shown in Figure 1, the entire external side surfaces surrounding the LED package 100 are covered by and surrounded by the protective insulation structure. The external side surfaces of the top part of the LED package 100 are slanted external surfaces of the semiconductor stack 30 and are fully covered by the first insulation layer 33 (whose external part is shown in blue) as the first protective insulation layer and is further covered by the top part of the second insulation layer 37 (whose external part is shown in red) over the first insulation layer (whose external part is shown in blue).

Donofrio, however, fails to disclose the claimed “protective insulation layer covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” and fails to discuss the need for and the benefits of the claimed protective insulation

layer. In fact, Donofrio is completely silent on the technical considerations for having a protective insulation layer covering each external side wall surface of the semiconductor stack.

The First Office Action at Page 13 provides the following explanation to support the rejection:

Donofrio, Figs. 1, 7A, 7B and related text discloses a light emitting diode package 110 having a first conductive type layer 112, a second conductive type layer 114, and an active layer 116 (col. 7, lines 58-64); a plurality of contact holes 118 arranged in the second conductive type semiconductor layer 114 and the active layer 116 which expose the first conductive type semiconductor layer 112 (col. 8, lines 32-35); a first bump 170 on a first side of the semiconductor stack that is connected to the first conductive type semiconductor layer 112 through the holes 118, and a second bump 160 that is electrically connected to the second conductive type semiconductor layer 114 (col. 8, lines 8-17); a protective insulation layer 140 covering a sidewall of the semiconductor stack (col. 8, lines 10-11).

The full paragraph in Donofrio for the above cited section at 8:5-31 is reproduced below:

5 Continuing with the description of FIG. 1, an anode contact 130, also referred to as a "p-contact", ohmically contacts the p-type layer 114 and extends on the first face 110a of the diode region 110. The anode contact 130 may extend to a greater or less extent on the p-type layer 114 than illustrated in FIG. 1. A transparent insulating layer 140 also extends on
10 the first face 110a outside the anode contact 130. A reflective cathode contact 150, also referred to as an "n-contact" electrically contacts the n-type layer 112 and extends through the transparent insulating layer 140 and onto the transparent insulating layer 140 that is outside the anode contact 130. In some
15 embodiments, the reflective cathode contact 150 may directly and ohmically contact the n-type layer 112. In other embodiments, however, a thin ohmic contact layer, such as a layer of titanium, may provide the actual ohmic contact to the n-type
20 layer 112. The transparent insulating layer 140 and the reflective cathode contact 150 can provide a hybrid reflective structure or "hybrid mirror", wherein the underlying transparent insulating layer 140 provides an index refraction mismatch or index step to enhance the total internal reflection (TIR) from
25 the reflective layer 150 compared to absence of the underlying transparent insulating layer 140. It will also be understood that, in other embodiments, the transparent insulating layer 140 may comprise multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector. Moreover, the reflective cathode contact 150 may
30 also include a plurality of sublayers.

The First Office Action specifically relies on “A transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130” in the above paragraph as the evidence for disclosing the protective insulation layer of Claim 1. Claim 1 as amended explicitly recites the protective insulation layer “covering each external side wall surface of the semiconductor stack of each light emitting diode facing externally of the LED package so that the protection insulation layer surrounds the LED package” (with added emphasis). As discussed above, this feature is advantageous because the protective insulation layer is formed as part of the wafer-level fabrication for forming the LED stacks and other structures in each LED package region and thus co-exist with each LED package region at all times and can protect the LED package region during dicing the wafer level structure into individual LED packages or chips, in the subsequent packaging processes, and during the normal use of the LED package device after the fabrication.

Donofrio does not disclose this protective insulation layer as recited in Claim 1 and is completely silent on the need for this structure and the advantages provided by this structure. In FIG. 1 of Donofrio, the external side wall surface is not covered by the transparent insulating layer 140.

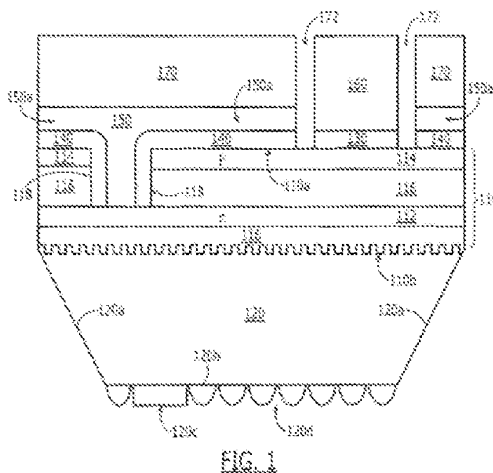


FIG. 1

Donofrio teaches that the transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130 at 8:10-11 and specifically provides examples of extending the layer 140 outside the anode contact 130 by covering top surface of the p-type layer 114 and covering on an inner sidewall of the diode region 110 formed by the via 118.

In Donofrio, the transparent insulating layer 140 is used to provide electrical insulation between the cathode contact 150 in the via 118 for contacting the n-type layer 112 and the p-type layer 114 and the quantum well layers 116. *Id.* at 8:5-15 and 16:7-19. For this function, there is no need for extending the layer 140 to cover external sidewall surfaces. Donofrio also discloses using the layer 104 as an optical reflective layer to direct light downward to improve the optical efficiency of the LED device. *Id.* at 8:20-26 and 9:54-60. Under the teachings of Donofrio, there is no need for the layer 104 to cover each external side wall surface since such a covering layer 104 on the vertical side surface which would reflect light horizontally rather than downward.

Notably, there is not a single statement in Donofrio as to a need for the claimed protective insulation layer in Claim 1. Donofrio is completely silent regarding any technical issues or disadvantages for not covering the external sidewall surfaces by a protective insulation layer. Neither does Donofrio state any benefits for covering each external side wall surface.

Therefore, in light of the teachings in Donofrio and the context of the teachings on the layer 140, the single statement of “A transparent insulating layer 140 also extends on the first face 110a outside the anode contact 130” at 8:10-11 is insufficient as a disclosure of “a protective insulation layer covering each external side wall surface of the semiconductor stack” under pre-AIA 35 U.S.C. §102(b).

Accordingly, the First Office Action fails to show that Donofrio discloses each limitation in Claim 1 as amended. Therefore, Claim 1 as amended is patentable under pre-AIA 35 U.S.C. §102 over Donofrio.

Claims 2-3, 5-7 and 11-15 are dependent claims of Claim 1 and thus are patentable over Donofrio based on the above explanation for Claim 1 and based on their own merits.

REJECTION TO CLAIM 4 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND BEESON

Claim 4, which depends on Claims 1 and 2, is rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Beeson.

Beeson is cited and relied upon for providing a teaching on a wavelength converter in an LED device. However, the disclosure of Beeson does not cure the defects in the disclosure of

Donofrio as discussed above. Therefore, based on the above discussion of Claims 1 and 2, the combined teaching of Donofrio and Beeson fails to disclose each limitation in Claim 4 and fails to render the claimed subject matter in Claim 4 as a whole unpatentable.

REJECTION TO CLAIM 8 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND TAKUMA

Claim 8, which depends on Claims 1 and 7, is rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Takuma.

Takuma is cited and relied upon for providing a teaching related to a dummy bump. However, the disclosure of Takuma does not cure the defects in the disclosure of Donofrio as discussed above. Therefore, based on the above discussion of Claims 1 and 7, the combined teaching of Donofrio and Takuma fails to disclose each limitation in Claim 8 and fails to render the claimed subject matter in Claim 8 as a whole unpatentable.

REJECTION TO CLAIMS 9-10 UNDER PRE-AIA 35 U.S.C. § 103(A) OVER DONOFRIO AND HO

Claim 9, which depends on Claim 1, and its dependent Claim 10 are rejected as being obvious under 35 U.S.C §103(a) over Donofrio and Ho.

Ho is cited and relied upon for providing a teaching related to a heat dissipating structure in LED. However, the disclosure of Ho does not cure the defects in the disclosure of Donofrio as discussed above. Therefore, based on the above discussion of Claim 1, the combined teaching of Donofrio and Ho fails to disclose each limitation in Claims 9-10 and fails to render the claimed subject matter in Claims 9-10 as a whole unpatentable.

CLAIMS 16-35

Claims 16-35 recite features that are missing from the cited prior art based on the discussions of Claims 1-15 as discussed above and based on the additional features in Claims 16-35 that are not in Claims 1-15.

For example, Claims 16-21 recite structures having light emitting diode (LED) packages to include a stack of layers formed over one another and patterned to include an array of LED package regions and each LED package region includes (1) a LED package formed in the stack of layers in a central region of the LED package region and (2) a protective insulation structure formed to surround and protect the LED package from surroundings outside the protective insulation structure and to separate from adjacent LED packages. Claims 16-21 further recite that the protective insulation structure includes a two-layer protective structure having a first protective insulation layer that surrounds and covers each external side wall surface of the semiconductor stack and a second protective insulation layer that forms on the first protective insulation layer to protect the semiconductor stack from an external environment. In light of the disclosure of the cited prior art, the prior art fails to disclose those features in the combination as recited in Claims 16-21.

Next Claims 22-27 recite an electrical contact structure on the first side of the semiconductor stack and electrically coupled to supply the electrical signal to the first and second type semiconductor layers via the contact holes. The recited electrical contact structure includes a first bump, a first electrical contact layer material, a second bump, and a second electrical contact layer material. Claims 22-27 recite an external structure that covers (1) the second side of the semiconductor stack that exports light generated in the active layer outside the LED package, and (2) side wall surfaces of the semiconductor stack. In light of the disclosure of the cited prior art, the prior art fails to disclose those features in the combination as recited in Claims 22-27.

With respect to Claims 28-35, the cited prior art fails to disclose, among others, a LED package as recited in Claims 28-25 with each single light emitting diode including an inclined side wall in the first conductive type semiconductor of its semiconductor stack and a protective insulation layer covering a sidewall of the semiconductor stack of each light emitting diode and having a thickness that varies along the sidewall of the semiconductor stack.

Therefore, Claims 16-35 are patentable over the cited prior art.

CONCLUSION

In light of above explanations and analyses, Patent Owner respectfully submits that the rejections raised in non-final Office Action have been fully addressed and are moot, and that Claims 16-35 as presented in this filing are patentable.

Therefore, Patent Owner respectfully requests the Office to conclude this reexamination proceeding and to issue a reexamination certificate for granting the challenged claims, Claims 1-15, as amended in this filing, and for granting the newly added Claims 16-35.

Please apply the required fees and any charges or credits to Deposit Account No. 50-0665.

REQUEST FOR EXAMINER'S INTERVIEW

In the interest of advancing this proceeding and in compliance with 37 C.F.R. 1.560 governing the interviews in *ex parte* reexamination proceedings, the undersigned respectfully suggests an examiner's interview to be conducted to discuss any outstanding issues that the Office may have in light of the filing of this response.

Respectfully submitted,

Date: Decemer 19, 2016

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Filed : April 15, 2016
Page : 34 of 34

Ex Parte Reexamination of U.S. Patent No. 9,070,851 B2
Control No.: 90/013,725
Attorney Docket No.: 114898-8904.US00

CERTIFICATE OF SERVICE

I hereby certify that, on December 19, 2016, I caused a true and correct copy of the foregoing RESPONSE TO OFFICE ACTION filed in the *ex parte* reexamination of U.S. Patent No. 9,070,851 B2 under Control Number 90/013,725 to be served via First Class U.S. Mail on the Third Party Requestor via its attorney of record:

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Date: December 19, 2016

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Electronic Patent Application Fee Transmittal				
Application Number:		90013725		
Filing Date:		15-Apr-2016		
Title of Invention:		Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same		
First Named Inventor/Applicant Name:		9070851		
Filer:		Bing Ai/Meghan Bright		
Attorney Docket Number:		MT100		
Filed as Large Entity				
Filing Fees for ex parte reexam				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
REEXAMINATION INDEPENDENT CLAIMS	1821	1	420	420
REEXAMINATION CLAIMS IN EXCESS OF 20	1822	15	80	1200
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1620

Electronic Acknowledgement Receipt	
EFS ID:	27829881
Application Number:	90013725
International Application Number:	
Confirmation Number:	7313
Title of Invention:	Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same
First Named Inventor/Applicant Name:	9070851
Customer Number:	97075
Filer:	Bing Ai/Meghan Bright
Filer Authorized By:	Bing Ai
Attorney Docket Number:	MT100
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Deposit Account	500665
Authorized User	Meghan Bright
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Reexam_Response.pdf	1133216	yes	34
			a1df6dea096a60a6aa9a3d4b7e63cd8075fd05a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	9	
	Applicant Arguments/Remarks Made in an Amendment		10	33	
	Reexam Certificate of Service		34	34	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32081	no	2
			75d7b69b55b9b69f0eeb4e3d95351be572e8fac9		
Warnings:					
Information:					
Total Files Size (in bytes):			1165297		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,725	04/15/2016	9070851	MT100	7313
97075 7590 11/25/2016 Perkins Coie LLP - SDO General PO Box 1247 Seattle, WA 98111-1247			EXAMINER NGUYEN, TUAN H	
			ART UNIT 3992	PAPER NUMBER
			MAIL DATE 11/25/2016	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Ex Parte Reexamination Interview Summary	Control No. 90/013,725	Patent Under Reexamination 9070851
	Examiner TUAN H. NGUYEN	Art Unit 3992
All participants (USPTO personnel, patent owner, patent owner's representative):		
(1) <u>TUAN H. NGUYEN</u>	(3) <u>Bing Ai</u>	
(2) <u>Timothy Speer, Minh Nguyen</u>	(4) <u>Seyoung Cheon</u>	
Date of Interview: <u>17 November 2016</u> Type: a) ☒ Telephonic b) ☐ Video Conference c) ☐ Personal (copy given to: 1) ☐ patent owner 2) ☐ patent owner's representative) Exhibit shown or demonstration conducted: d) ☐ Yes e) ☒ No. If Yes, brief description: _____ Agreement with respect to the claims f) ☐ was reached. g) ☒ was not reached. h) ☐ N/A. Any other agreement(s) are set forth below under "Description of the general nature of what was agreed to..." Claim(s) discussed: <u>1.</u> Identification of prior art discussed: <u>Seiichiro et al., Shelton et al., and Donofrio et al..</u> Description of the general nature of what was agreed to if an agreement was reached, or any other comments: <u>Disagreed that contact holes or openings from Seiichiro and Shelton are different from the claimed contact holes as recited in claim 1; claim 1 is not limited to a single LED structure, and the protective insulating layer as recited, is not required to cover the whole structure as discussed. Applicant will amend the claims and the case will be reconsidered.</u> (A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims patentable, if available, must be attached. Also, where no copy of the amendments that would render the claims patentable is available, a summary thereof must be attached.) A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION MUST INCLUDE PATENT OWNER'S STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. (See MPEP § 2281). IF A RESPONSE TO THE LAST OFFICE ACTION HAS ALREADY BEEN FILED, THEN PATENT OWNER IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO PROVIDE THE MANDATORY STATEMENT OF THE SUBSTANCE OF THE INTERVIEW (37 CFR 1.560(b)). THE REQUIREMENT FOR PATENT OWNER'S STATEMENT CAN NOT BE WAIVED. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).		
/Tuan H. Nguyen/ Primary Examiner Art Unit 3992	/Minh Nguyen/ Primary Examiner Art Unit 3992	/Timothy M. Speer/ SPRS Art Unit 3992
cc: Requester (if third party requester)		

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Facsimile Cover Sheet

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If there are any problems with this transmission, please call 858.720.5700**Date:** November 15, 2016COVER SHEET & 2 PAGES

APPLICATION

NUMBER: 90/013,725

ATTORNEY

DOCKET NO.: 114898-8904.US00

Sender:	Telephone:	Facsimile:
Bing Ai, Perkins Coie LLP	(858) 720-5707	(858) 720-5807

Recipient:	Company:	Telephone:	Facsimile:
Examiner Nguyen	United States Patent & Trademark Office	(571) 272-1694	(571) 273-1694

Dear Examiner Nguyen:

Following this cover letter is the Applicant-Initiated Interview Request Form relating to the above-referenced application. Please use the following dial-in information for the interview on Thursday:

Toll Free Dial In Number: (888) 857-7291

Participant Passcode: 858 720 5707

With best regards,

Bing Ai
Reg. No. 43,312

This Fax contains confidential, privileged information intended only for the intended addressee. Do not read, copy or disseminate it unless you are the intended addressee. If you have received this Fax in error, please email it back to the sender at perkinscoie.com and delete it from your system or call us (collect) immediately at 858.720.5700, and mail the original Fax to Perkins Coie LLP, 11988 El Camino Real, Suite 350, San Diego, CA 92130-2594.

Doc Code: M865 or FAI.REQ.INTV

 PTOL-413A (08-10)
 Approved for use through 07/31/2012. OMB 0861-0031
 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form

 Application No.: 90/013,725 First Named Inventor: Won Cheol Seo
 Examiner: Tuan H. Nguyen Art Unit: 3992 Status of Application: Pending
Tentative Participants:

 (1) Examiner Nguyen (2) Bing Ai, Reg. No. 43,312
 (3) Seyoung Cheon -Patent Agent (4) _____

 Proposed Date of Interview: 11/17/16 Proposed Time: 3:00 PM EST

Type of Interview Requested:

 (1) ☒ Telephonic** (2) ☐ Personal (3) ☐ Video Conference

 Exhibit To Be Shown or Demonstrated: ☐ YES ☒ NO

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) <u>35 USC §102(b)</u>	<u>1-4, 7, 9, 11</u>	<u>Seiichiro</u>	☐	☐	☐
(2) <u>35 USC §102(b)</u>	<u>1-4, 7, 11-12, 14-15</u>	<u>Shelton</u>	☐	☐	☐
(3) <u>35 USC §102(b)</u>	<u>1-3, 5-7, 11-15</u>	<u>Donofrio</u>	☐	☐	☐
(4) <u>35 USC §103(a)</u>	<u>4</u>	<u>Donofrio in view of Beeson</u>	☐	☐	☐
☒ Continuation Sheet Attached ☐ Proposed Amendment or Arguments Attached					

Brief Description of Arguments to be Presented:

**Please dial-in using the following information - Dial In Number: (888) 857-7291 / Participant Passcode: 858 720 5707

An interview was conducted on the above-identified application on _____

NOTE: This form should be completed and filed by applicant in advance of the interview (see MPEP § 713.01). If this form is signed by a registered practitioner not of record, the Office will accept this as an indication that he or she is authorized to conduct an interview on behalf of the principal (37 CFR 1.32(a)(3)) pursuant to 37 CFR 1.34. This is not a power of attorney to any above named practitioner. See the Instruction Sheet for this form, which is incorporated by reference. By signing this form, applicant or practitioner is certifying that he or she has read the Instruction Sheet. After the interview is conducted, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible. This application will not be delayed from issue because of applicant's failure to submit a written record of this interview.

 / Bing Ai/
 Applicant/Applicant's Representative Signature

 Examiner/SPE Signature

 Bing Ai
 Typed/Printed Name of Applicant or Representative

 43,312
 Registration Number, if applicable

133591498.1

Doc Code: M865 or FAI.REQ.INTV

PTOL-413A (08-10)
 Approved for use through 07/31/2012. OMB 0851-0031
 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form (continued)

Application No.: 90/013,725 First Named Inventor: Won Cheol Seo
 Examiner: Tuan H. Nguyen Art Unit: 3992 Status of Application: Pending

Additional Issues To Be Discussed

	Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(2)	<u>35 USC §103(a)</u>	<u>8</u>	<u>Donofrio in view of Takuma</u>	☐	☐	☐
(3)	<u>35 USC §103(a)</u>	<u>9-10</u>	<u>Donofrio in view of Ho</u>	☐	☐	☐
(4)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐
(5)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐
(6)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐
(7)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐
(8)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐
(9)	<u> </u>	<u> </u>	<u> </u>	☐	☐	☐

Continuation of Description of Arguments to be Presented:

Toll Free Dial In Number: (888) 857-7291
 Participant Passcode: 858 720 5707

133591498 I



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,725	04/15/2016	9070851	MT100	7313
97075 7590 09/19/2016 Perkins Coie LLP - SDO General PO Box 1247 Seattle, WA 98111-1247			EXAMINER NGUYEN, TUAN H	
			ART UNIT 3992	PAPER NUMBER
			MAIL DATE 09/19/2016	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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ALAN TABOADA - MOSER TABOADA
1030 BROAD STREET, SUITE 203
SHREWSBURY, NJ 07702

***EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM**

REEXAMINATION CONTROL NO. 90/013,725.

PATENT NO. 9070851.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/013,725	Patent Under Reexamination 9070851	
	Examiner TUAN H. NGUYEN	Art Unit 3992	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

- a. ☒ Responsive to the communication(s) filed on 8/8/2016 .
☐ A declaration(s)/affidavit(s) under 37 CFR 1.130(b) was/were filed on _____.

b. ☐ This action is made FINAL.

c. ☒ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 3 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.	3. ☐ Interview Summary, PTO-474.
2. ☒ Information Disclosure Statement, PTO/SB/08.	4. ☐ _____.

Part II SUMMARY OF ACTION

- 1a. ☒ Claims 1-15 are subject to reexamination.
- 1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims 1-15 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.
8. ☒ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of the certified copies have

1 ☐ been received.

2 ☐ not been received.

3 ☒ been filed in Application No. 13/194,317 .

4 ☐ been filed in reexamination Control No. _____.

5 ☐ been received by the International Bureau in PCT application No. _____.

* See the attached detailed Office action for a list of the certified copies not received.

9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Reexamination

Summary of Proceedings

A Request pursuant to 37 CFR 1.510 for ex parte reexamination of the US Patent Number 9,070,851 (the '851 patent) issued to Seo et al. entitled "Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same" was filed on April 15, 2016 by the Third party Requester. An Order granting *ex parte* reexamination of the '851 patent was mailed on May 18, 2016. The Order stated that there was a substantial new question of patentability affecting claims 1-15 of the '851 patent.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 08 August 2016 pursuant to 37 CFR §1.555 have been considered by the examiner.

Note: Where the IDS citations are submitted but not described, the examiner is only responsible for cursorily reviewing the references. The initials of the examiner on the PTO-1449, or equivalent, indicate only that degree of review unless the reference is either applied against the claims, or discussed by the examiner as pertinent art of interest, in a subsequent office action. See Guidelines for Reexamination of Cases in View of *In re Portola Packaging, Inc.*, 110 F.3d 786, 42 USPQ2d 1295 (Fed. Cir. 1997), 64 FR at 15347, 1223 Off. Gaz. Pat. Office at 125 (response to comment 6). Consideration by the examiner of the information submitted in an IDS means that the examiner will consider the documents in the same manner as other documents in Office

search files are considered by the examiner while conducting a search of the prior art in a proper field of search. The initials of the examiner placed adjacent to the citations on the PTO-1449 or PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. MPEP § 609 (Eighth Edition, August 2001).

In this case, it is noted that due to the large number of references cited, and the absence of any description of the relevance of the references, it should be assumed that only the most cursory review of the cited documents consistent with these guidelines has been performed.

Status of claims

The following is the status of the claims with respect to the Request:

Claims 1-15 are reexamined in view of the following prior art submitted by the third party requesters. Of these, claims 1, and 14 are independent claims.

References cited by the Requester

- 1) US 7,179,670 to Shelton et al. (hereinafter "Shelton").
- 2) US 8,368,100 to Donofrio et al. (hereinafter "Donofrio").
- 3) US 7,564,887 to Wang et al. (hereinafter "Wang").
- 4) US 6,657,236 to Thibault et al. (hereinafter "Thibault").
- 5) US 7,335,517 to Hayasaka et al. (hereinafter "Hayasaka").

- 6) US 6,838,702 to Ho (hereinafter "Ho").
- 7) US 2009/0140272 to Beeson et al. (hereinafter "Beeson").
- 8) JP 4,151,284 to Seiichiro e al. (hereinafter "Seiichiro").
- 9) JP 2002-319704 to Takuma et al. (hereinafter "Takuma").
- 10) JP 11008414 to Etsuo (hereinafter "Etsuo").
- 11) KR 610650 to Hwan (hereinafter "Hwan").

Claim Rejections - Relevant statutes

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

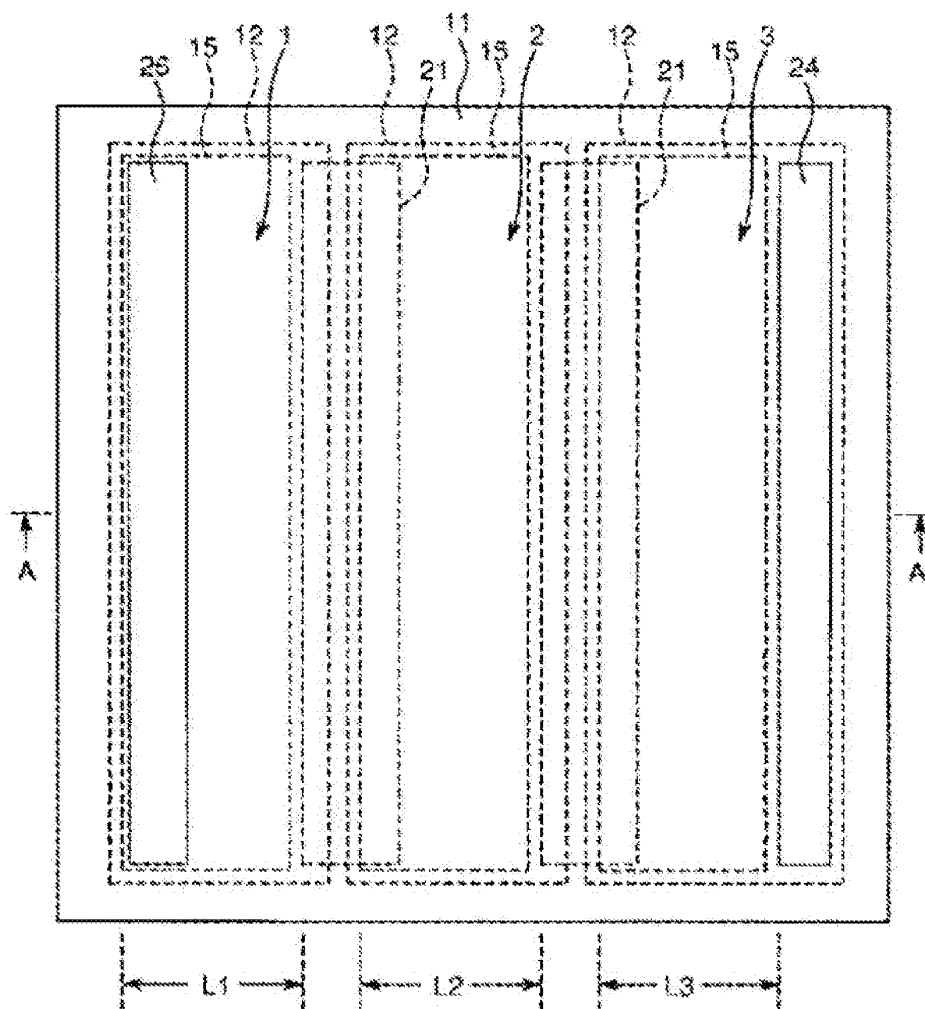
Detailed Analysis

1/. Claims 1-4, 7, 9, 11 are rejected under 35 U.S.C. 102(b) as anticipated by Seiichiro.

Regarding to claim 1:

Seiichiro, Figs. 1-3 as shown below, discloses a light emitting diode package including a semiconductor stack comprising a first conductivity type (i.e. n-type) semiconductor layer 12, an active layer 10, and a second conductive type (i.e. p-type) semiconductor layer 13; a plurality of contact holes arranged in the second conductive type semiconductor layer 13 and the active layer 10, the contact holes exposing the first conductive type semiconductor layer 12; a first bump 21, 24 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 12 via the plurality of contact holes; a second bump 26 arranged on the first side of the of the conductor stack, the second bump 26 being electrically connected to the second conductive type semiconductor layer 13; and a protective insulation layer 17, 30 covering a sidewall of the semiconductor stack.

【 1】



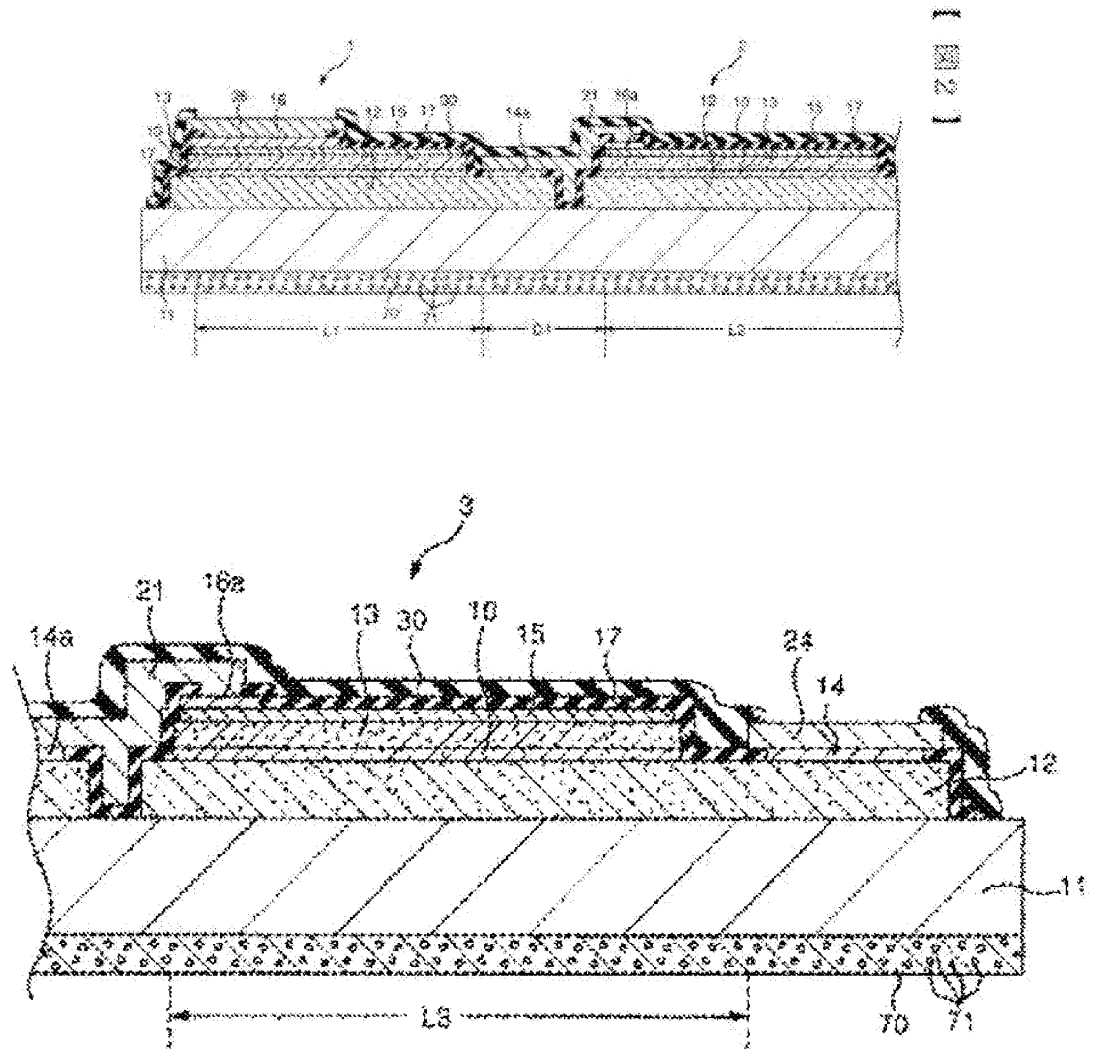


Fig. 3

Regarding to claims 2, 4:

Seiichiro, Fig. 2 shows a wavelength converter 71, arranged on a second side of the semiconductor stack, has a side surface flush with a side surface of the protective insulation layers 17, 30.

Regarding to claim 3:

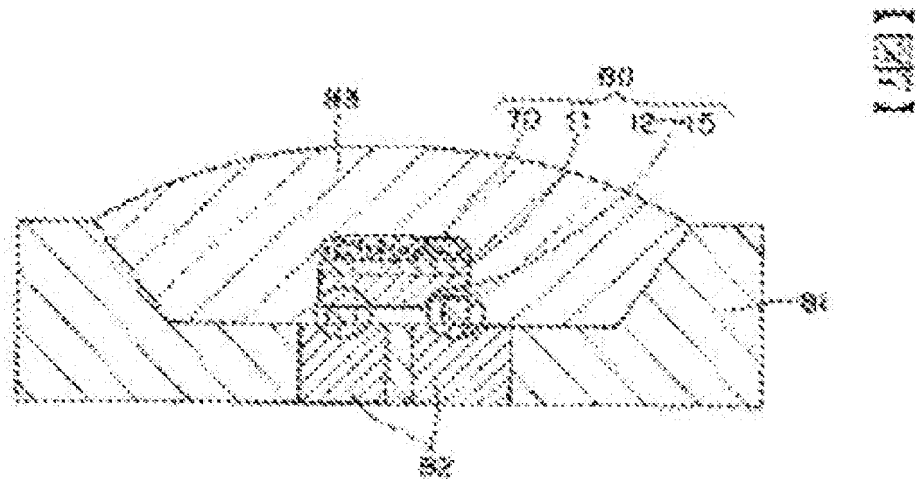
The material disclosed by Seiichiro in paragraph [0014] is considered as phosphors or impurity-doped crystal substrates.

Regarding to claim 7:

Seiichiro, Fig. 2 shows insulation layers 17, 30 arranged on side surfaces of the first and second bumps 21, 26.

Regarding to claim 9:

Seiichiro, Fig. 7 below shows a substrate 81 comprises a first and second through holes 82, and the first and second bumps (shown in circles) are arranged in the holes 82.



Regarding to claim 11:

Seiichiro, Figs. 1-3 show a first contact layer 14 having a first contact sections which contact the first conductive type semiconductor layer 12 in the plurality of contact holes and a connecting section (i.e. top portion) connecting the first contact sections to each other; and a second contact layer 15 which contacts the second conductive type semiconductor layer 13, wherein the protective insulation layer comprises a first insulation layer 17 and a second insulation layer 30, the first insulation layer 17 being arranged between the first contact layer 14 and the second contact layer 15 and covering the second contact layer 15, and the second insulation layer 30 being arranged between the semiconductor stack and the first contact layer 14 and covering the first contact layer 14, wherein the first bump 21, 24 is electrically connected to the first contact layer 14, and the second bump 26 is electrically connected to the second contact layer 15.

2/. Claims 1-4, 7, 11-12, 14-15 are rejected under 35 U.S.C. 102(b) as anticipated by Shelton.

Shelton, Figs. 2, 4, 5 and related text discloses a light emitting diode package 10 having a first conductive type (i.e. n-type base) layer 22, a second conductive type layer 24, and an active layer (i.e. a portion of the layer 24). *Id.* at col. 4, lines 50-56, col. 5, lines 33-36;

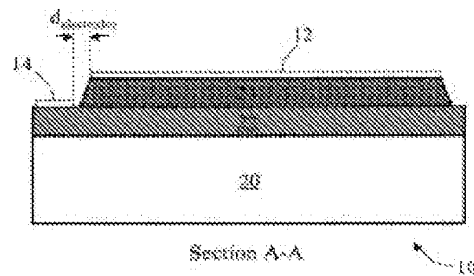


FIG 2

a plurality of contact holes 34 arranged in the second conductive type semiconductor layer 24 and the active layer, the contact holes exposing the first conductive type semiconductor layer 22 (Figs. 4-5, col. 6, lines 44-45);

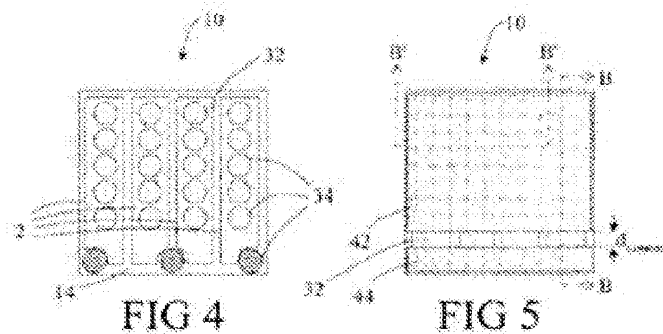
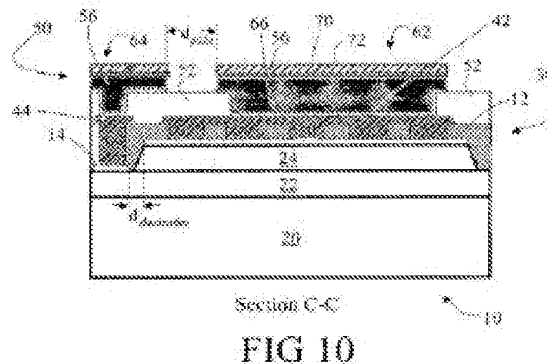


FIG 4

FIG 5

a first bump 56 arranged on a first side of the semiconductor stack, extending through the opening in dielectric material 52 and electrically connected to the first conductive type semiconductor layer 22, and a second bump 56 extending through the opening in the dielectric material and electrically connected to the second conductive type semiconductor layer 24 (Fig. 10, col. 8, lines 8-14); and a protective insulation layer 32, 52 covering a sidewall of the semiconductor stack (col. 6, lines 20-22).



Regarding to claims 2-4:

Shelton, Fig. 16 shows a phosphor sheet wavelength converter 140, arranged on a second side of the semiconductor stack, has a side surface flush with a side surface of the protective insulation layer 32.

Regarding to claim 7:

Shelton, Fig. 10 shows insulation layer 52 arranged on side surfaces of the first and second bumps 56 (col. 8, lines 5-6).

Regarding to claim 11:

Shelton, Fig. 10 shows a first contact layer 14 having a first contact sections which contact the first conductive type semiconductor layer 22 in the plurality of contact holes and a connecting section connecting the first contact sections to each other, and a second contact layer 12 which contacts the second conductive type semiconductor layer 24, wherein the protective insulation layer comprises a first insulation layer 32 and a second insulation layer 52, the first insulation layer 32 arranged between the first

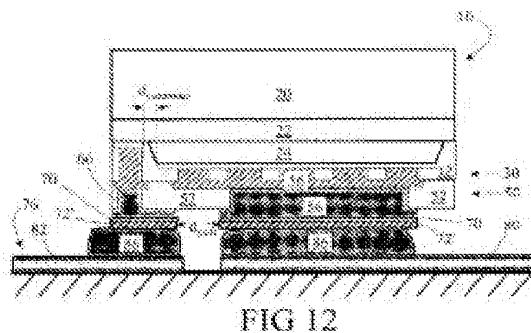
contact layer 14 and the second contact layer 12 and covering the second contact layer 12, a second insulation layer 52 is arranged between the semiconductor stack and the first contact layer 14. The first bump 56 is connected to the first contact layer 14 and the second bump 56 is connected to the second contact layer 12 (col. 6, lines 12-19, col. 8, lines 5-6).

Regarding to claim 12:

Shelton, Fig. 10 shows a first electrode pad 44 which contacts the first contact layer 14, and a second electrode pad 42 which contacts the second contact layer 12. The first bump 56 contacts the first electrode pad 44 and the second bump 56 contacts the second electrode pad 42 (col. 6, lines 12-19).

Regarding to claims 14-15:

Shelton, Fig. 12 shows the light emitting diode 10 bonded to a circuit board 76. The PC board has at least positive and negative metal traces 80, 82 on which bumps 86 are disposed (col. 9, lines 18-22).



3/. Claims 1-3, 5-7 and 11-15 are rejected under 35 U.S.C. 102(e) as anticipated by Donofrio.

Donofrio, Figs. 1, 7A, 7B and related text discloses a light emitting diode package 110 having a first conductive type layer 112, a second conductive type layer 114, and an active layer 116 (col. 7, lines 58-64); a plurality of contact holes 118 arranged in the second conductive type semiconductor layer 114 and the active layer 116 which expose the first conductive type semiconductor layer 112 (col. 8, lines 32-35); a first bump 170 on a first side of the semiconductor stack that is connected to the first conductive type semiconductor layer 112 through the holes 118, and a second bump 160 that is electrically connected to the second conductive type semiconductor layer 114 (col. 8, lines 8-17); a protective insulation layer 140 covering a sidewall of the semiconductor stack (col. 8, lines 10-11).

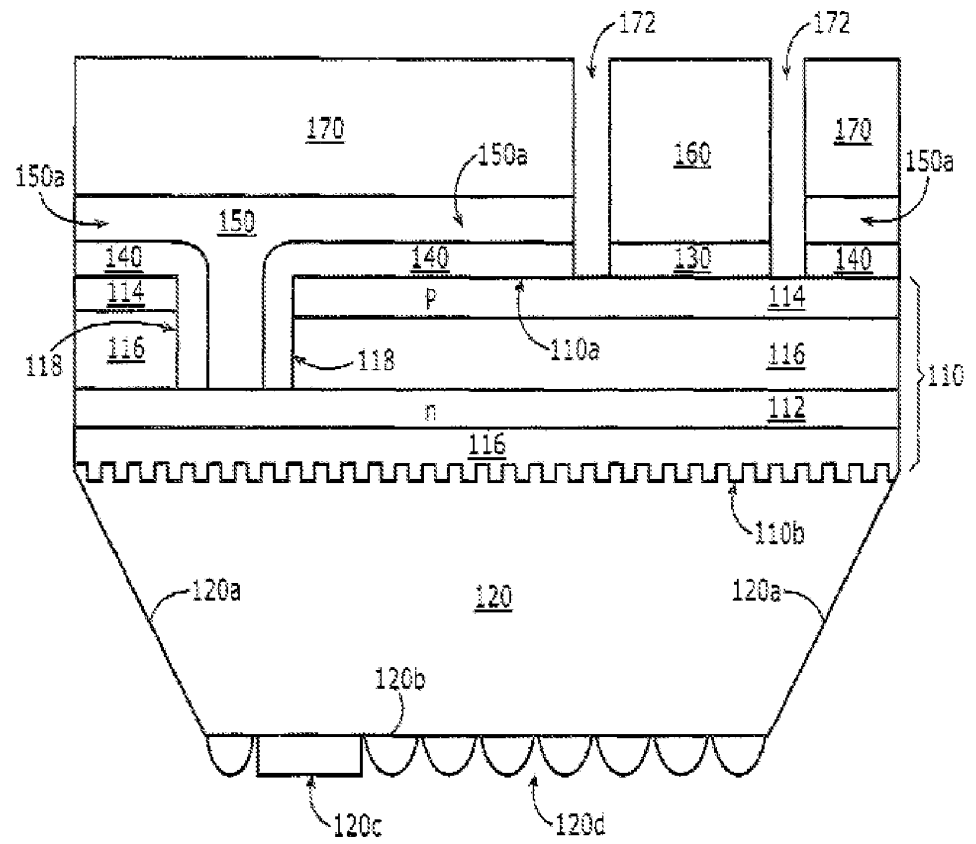


FIG. 1

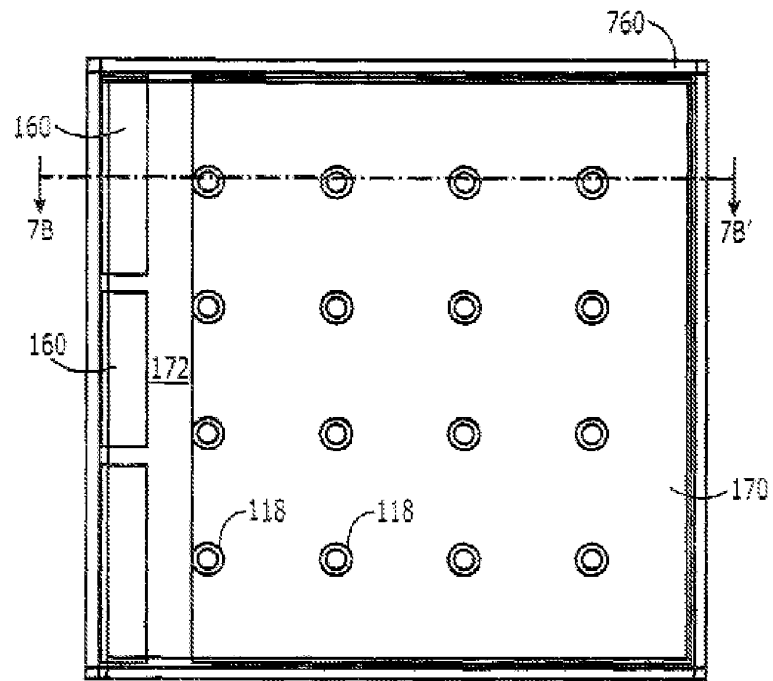


FIG. 7A

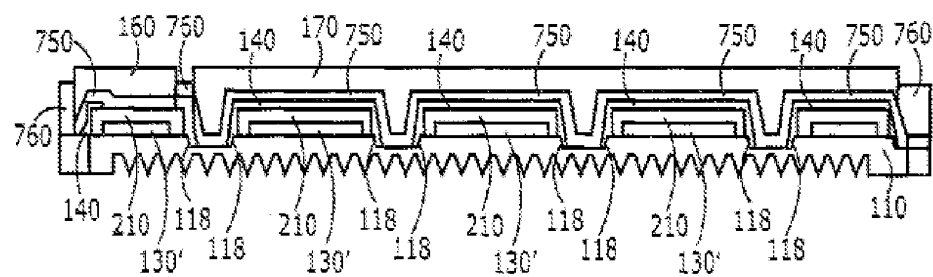


FIG. 7B

Regarding to claims 2-3:

Donofrio, col. 1, lines 46-47 discloses that LED may incorporate a wavelength converter such as phosphor.

Regarding to claims 5, 13:

Donofrio, col. 8, lines 26-30 discloses that the protective insulation layer 140 may comprise a distributed Bragg reflector.

Regarding to claim 6:

Donofrio, col. 9, lines 4-9 discloses that the first conductive type semiconductor layer 112 may have roughened surface. Fig. 1 shows that the interface between the sapphire substrate 120 and the diode region 110 may be textured, as shown by the jagged line.

Regarding to claim 7:

Donofrio, Fig. 3 and text on col. 5, lines 40-41 shows an insulation layer 340 arranged on the side surface of the first bump 170 and the second bump 160 to prevent short circuiting between the bumps.



Donofrio, Fig. 3 shows a first contact layer 150 having a first contact sections which contact the first conductive type semiconductor layer 112 in the plurality of contact holes 118 and a connecting section connecting the first contact sections to each other, and a second contact layer 130 which contacts the second conductive type semiconductor layer 114, wherein the protective insulation layer comprises a first insulation layer 140 and a second insulation layer 340, the first insulation layer 140 arranged between the first contact layer 150 and the second contact layer 130 and

covering the second contact layer 130, a second insulation layer 340 is arranged between the semiconductor stack and the first contact layer 150. The first bump 170 is connected to the first contact layer 150 and the second bump 160 is connected to the second contact layer 130 (col. 4, lines 40-44).

Regarding to claim 12:

Donofrio, Fig. 2 shows a first electrode pad 250 which contacts the first contact layer 150, and a second electrode pad 210 which contacts the second contact layer 130. The first bump 170 contacts the first electrode pad 250 and the second bump 160 contacts the second electrode pad 210 (col. 8, lines 26-30).

Regarding to claims 14-15:

Donofrio, col. 9, lines 15-20, lines 41-43 discloses that the first and second bumps 170, 160 may be mounted on a circuit board or wiring board.

4/. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Donofrio in view of Beeson.

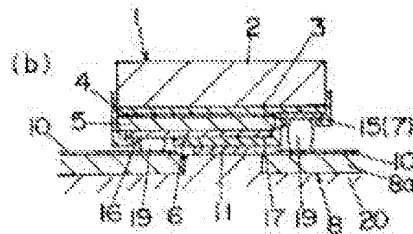
Donofrio discloses substantially the claimed light emitting diode package as noted above except a side of the wavelength converter being flush with a side surface of the protective insulation layer.

[illegible]

FIG. 30

5/. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Trilio* in view of *Takuma*.

Takuma, in a related art, teaches a dummy bump 11 between the first bump and the second bump 19 to improve heat radiation capability of the device (Fig. 23B, paragraph [0054]).



6/. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donofrio in view of Ho.

Donofrio fails to teach a first through hole and a second through hole with the first and second bumps being arranged in the first and second through holes respectively.

Ho, in a related art, discloses a light emitting chip 20 having a heating dissipating substrate 24, the substrate 24 has several opening 241 therethrough. The openings are filled with metals with good heat dissipating properties to allow for faster transfer of heat energy (Fig. 2, col. 3, lines 23-26).

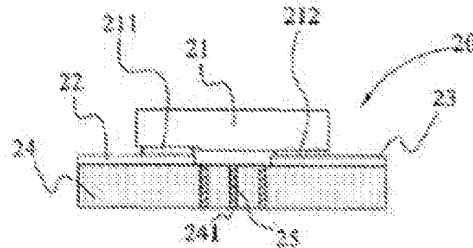


FIG. 2

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed a LED package with the first bump and the second bump being arranged in the first through-hole and the second through-hole as suggested by Ho in Donofrio LED package for faster transfer of heat energy, thus increasing efficiency of heat dissipation.

Other proposed Rejections

The proposed rejection of dependent claims 4-6, 8-10 and 14-15 in SNQP statements No. 4-18, 20, 23-26 are relevant; however, they are cumulative and are not applied to reject the same claims at this time.

CONCLUSION

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that ex parte reexamination proceedings "will be conducted with special dispatch" (37 CFR

1.550(a)). Extensions of time in ex parte reexamination proceedings are provided for in 37 CFR 1.550(c).

Amendment in Reexamination Proceedings

Patent owner is notified that any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37 CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). See MPEP § 2250(IV) for examples to assist in the preparation of proper proposed amendments in reexamination proceedings.

Submissions

In order to insure full consideration of any amendments, affidavits or declarations or other documents as evidence of patentability, such documents must be submitted in response to the first Office action on the merits (which does not result in a close of prosecution). Submissions after the second Office action on the merits, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and by 37 CFR 41.33 after appeal, which will be strictly enforced.

Notice Regarding Certain Reexamination Issue

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 9,070,851 throughout the course of this reexamination

proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Notice Re Patent Owner's Correspondence Address

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated-as the correspondence address of the patent. *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding. and to any reexamination proceeding which is filed after that date. Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone numbers for reexamination inquiries:

Reexamination and Amendment practice

(571) 272-7703

Central Reexam Unit (CRU)

(571) 272-7705

Reexamination Facsimile Transmission No.

(571) 272-9900

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at <https://portal.uspto.gov/authenticate/authenticateuserlocalepf.html>. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are “soft scanned” (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the “soft scanning” process is complete.

Any inquiry concerning this communication should be directed to Central Reexamination Unit at telephone number 571-272-7705

Signed:

/Tuan H. Nguyen/
Primary Examiner
Central Reexamination Unit
Art Unit 3992

Conferees:

/Minh Nguyen/
Primary Examiner
CRU, AU 3992

/Timothy M. Speer/
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		90013725
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	First Named Inventor	Won Cheol Seo	
	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
	Attorney Docket Number	114898-8904.US00	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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163	6852558	B2	2005-02-08	Lee et al.	
164	6858880	B2	2005-02-22	Horiuchi et al.	
165	6861761	B2	2005-03-01	Yang et al.	
166	6867505	B2	2005-03-15	Lee et al.	
167	6869812	B2	2005-03-22	Liu	
168	6870311	B2	2005-03-22	Mueller et al.	
169	6871982	B2	2005-03-29	Holman et al.	
170	6885035	B2	2005-04-26	Bhat et al.	
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174	6906416	B2	2005-06-14	Kamezos
175	6917057	B2	2005-07-12	Stokes et al.
176	6924160	B2	2005-08-02	Wei et al.
177	6924437	B1	2005-08-02	Creekmore et al.
178	6924514	B2	2005-08-02	Suenaga
179	6943433	B2	2005-09-13	Kamada
180	6946309	B2	2005-09-20	Camras et al.
181	6949771	B2	2005-09-27	Yoganandan et al.
182	6953255	B2	2005-10-11	Horiuchi et al.
183	6953952	B2	2005-10-11	Asakawa
184	6956245	B2	2005-10-18	Senda et al.

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185	6957899	B2	2005-10-25	Jiang et al.	
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189	6969626	B2	2005-11-29	Guo et al.	
190	6969946	B2	2005-11-29	Steranka et al.	
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192	6977396	B2	2005-12-20	Shen et al.	
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196	7005324	B2	2006-02-28	Imai	
197	7005679	B2	2006-02-28	Tarsa et al.	
198	7009199	B2	2006-03-07	Hall	
199	7023022	B2	2006-04-04	Eliashevich et al.	
200	7026181	B2	2006-04-11	Guo et al.	
201	7026659	B2	2006-04-11	Slater et al.	
202	7026709	B2	2006-04-11	Tsai et al.	
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204	7045828	B2	2006-05-16	Shimizu et al.	
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207	7054345	B2	2006-05-30	Ryou et al.
208	7067361	B2	2006-06-27	Allen et al.
209	7067849	B2	2006-06-27	Yoo
210	7078252	B2	2006-07-18	Uemura
211	7080932	B2	2006-07-25	Keuper
212	7105860	B2	2006-09-12	Shei et al.
213	7115998	B2	2006-10-03	Hiatt et al.
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218	7138660	B2	2006-11-21	Ota et al.
219	7141825	B2	2006-11-28	Horio et al.
220	7148517	B2	2006-12-12	Tu et al.
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226	7173277	B2	2007-02-06	Tamura et al.
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229	7186580	B2	2007-03-06	Tran et al.
230	7190005	B2	2007-03-13	Gibb et al.
231	7208772	B2	2007-04-24	Lee et al.
232	7210819	B2	2007-05-01	Jiang et al.
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235	7217583	B2	2007-05-15	Negley et al.
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237	7265374	B2	2007-09-04	Lee et al.
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240	7279350	B2	2007-10-09	Wu et al.
241	7279783	B1	2007-10-09	Fjelstad et al.
242	7282743	B2	2007-10-16	Sakai et al.
243	7285801	B2	2007-10-23	Eliashevich et al.
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250	7338169	B2	2008-03-04	Somani

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251	7342357	B2	2008-03-11	Sakano et al.
252	7348212	B2	2008-03-25	Schiaffino et al.
253	7355274	B2	2008-04-08	Lim
254	7361938	B2	2008-04-22	Mueller et al.
255	7361940	B2	2008-04-22	Kim et al.
256	7364982	B2	2008-04-29	Furukawa et al.
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259	7372082	B2	2008-05-13	Kim et al.
260	7375380	B2	2008-05-20	Asahara et al.
261	7391105	B2	2008-06-24	Yeom

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262	7391153	B2	2008-06-24	Suehiro et al.
263	7405433	B2	2008-07-29	Chew
264	7413918	B2	2008-08-19	Tran et al.
265	7419894	B2	2008-09-02	Makiyama et al.
266	7420814	B2	2008-09-02	Kim et al.
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269	7439166	B1	2008-10-21	Milosavljevic et al.
270	7446028	B2	2008-11-04	Hiatt et al.
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272	7456035	B2	2008-11-25	Eliashevich et al.

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273	7456495	B2	2008-11-25	Pohl et al.
274	7470938	B2	2008-12-30	Lee et al.
275	7473934	B2	2009-01-06	Nagai et al.
276	7474681	B2	2009-01-06	Lin et al.
277	7486867	B2	2009-02-03	Wang
278	7488988	B2	2009-02-10	Lin et al.
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281	7491976	B2	2009-02-17	Takeuchi et al.
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284	7524686	B2	2009-04-28	Chu et al.
285	7525248	B1	2009-04-28	Fan
286	7530712	B2	2009-05-12	Lin et al.
287	7531843	B2	2009-05-12	Lin et al.
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289	7544524	B2	2009-06-09	Lin et al.
290	7554126	B2	2009-06-30	Higashi et al.
291	7557443	B2	2009-07-07	Ye et al.
292	7566639	B2	2009-07-28	Kohda
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294	7573074	B2	2009-08-11	Shum et al.

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295	7589355	B2	2009-09-15	Tomoda et al.
296	7589408	B2	2009-09-15	Weng et al.
297	7592194	B2	2009-09-22	Jonda et al.
298	7592633	B2	2009-09-22	Shakuda

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/Bing Ai/	Date (YYYY-MM-DD)	2016-08-08
Name/Print	Bing Ai	Registration Number	43312

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	1	7608921	B2	2009-10-27	Pendse	
	2	7622746	B1	2009-11-24	Lester et al.	
	3	7626210	B2	2009-12-01	Shchekin et al.	
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9	7648849	B2	2010-01-19	Lee et al.	
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11	7652304	B2	2010-01-26	Steigerwald et al.	
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13	7705370	B2	2010-04-27	Fitzgerald	
14	7709282	B2	2010-05-04	Fukshima et al.	
15	7714342	B2	2010-05-11	Lee et al.	
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24	7786498	B2	2010-08-31	Choi et al.	
25	7791103	B2	2010-09-07	Oshima	
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31	7843074	B2	2010-11-30	Gao et al.	
32	7868343	B2	2011-01-11	Negley et al.	
33	7868354	B2	2011-01-11	Garcia et al.	
34	7893547	B2	2011-02-22	Huang et al.	
35	7902572	B2	2011-03-08	Ahn et al.	
36	7906788	B2	2011-03-15	Nagai	
37	7923198	B2	2011-04-12	Sawada	
38	7943286	B2	2011-05-17	Xu et al.	
39	7951625	B2	2011-05-31	Kamei	
40	7968897	B2	2011-06-28	Hata et al.	
41	7998761	B2	2011-08-16	Kim et al.	

Receipt date: 08/08/2016

90013725 - GAU: 3992

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		90013725
Filing Date		2016-04-15
First Named Inventor	Won Cheol Seo	
Art Unit	3992	
Examiner Name	NGUYEN, TUAN H	
Attorney Docket Number	114898-8904.US00	

42	7999271	B2	2011-08-16	Kim et al.	
43	8021904	B2	2011-09-20	Chitnis	
44	8049330	B2	2011-11-01	Tain et al.	
45	8076212	B2	2011-12-13	Takahashi et al.	
46	8076680	B2	2011-12-13	Lee et al.	
47	8097937	B2	2012-01-17	Bogner et al.	
48	8118451	B2	2012-02-21	Householder et al.	
49	8129917	B2	2012-03-06	Kim et al.	
50	8148905	B2	2012-04-03	Miskin et al.	
51	8149509	B2	2012-04-03	Howes	
52	8159000	B2	2012-04-17	Lee et al.	

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53	8163582	B2	2012-04-24	Zimmerman et al.
54	8179938	B2	2012-05-15	Kim
55	8183072	B2	2012-05-22	Seo et al.
56	8183691	B2	2012-05-22	Kanaoka et al.
57	8188488	B2	2012-05-29	Andrews et al.
58	8207543	B2	2012-06-26	Hasnain
59	8211724	B2	2012-07-03	Kim et al.
60	8222672	B2	2012-07-17	Kanamura et al.
61	8227272	B2	2012-07-24	Lee et al.
62	8237173	B2	2012-08-07	Nagai
63	8268715	B2	2012-09-18	Hiatt et al.

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Attorney Docket Number	114898-8904.US00

64	8269228	B2	2012-09-18	Lee et al.
65	8269238	B2	2012-09-18	Kim et al.
66	8288781	B2	2012-10-16	Seo et al.
67	8299476	B2	2012-10-30	Lee et al.
68	8314430	B2	2012-11-20	Illek et al.
69	8334091	B2	2012-12-18	Nozaki et al.
70	8334155	B2	2012-12-18	Krames et al.
71	8337071	B2	2012-12-25	Negley et al.
72	8338844	B2	2012-12-25	Katsuno et al.
73	8350279	B2	2013-01-08	Lee et al.
74	8368100	B2	2013-02-05	Donofrio et al.

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90013725 - GAU: 3992

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Attorney Docket Number	114898-8904.US00	

75	8368190	B2	2013-02-05	Lee et al.	
76	8445933	B2	2013-05-21	Lee et al.	
77	8450751	B2	2013-05-28	Engl et al.	
78	8476648	B2	2013-07-02	Lee et al.	
79	8536612	B2	2013-09-17	Lee et al.	
80	8581291	B2	2013-11-12	Shimokawa et al.	
81	8643029	B2	2014-02-04	Lee et al.	
82	8648369	B2	2014-02-11	Seo et al.	
83	8716727	B2	2014-05-06	Lee et al.	
84	8821961	B2	2014-09-02	Bondoux et al.	
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86	8846521	B2	2014-09-30	Sugizaki
87	8847254	B2	2014-09-30	Roth et al.
88	8847266	B2	2014-09-30	Choi et al.
89	8878245	B2	2014-11-04	Parikh et al.
90	8896011	B2	2014-11-25	Yoon et al.
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92	8937326	B2	2015-01-20	Lee et al.
93	8964020	B2	2015-02-24	Hersee
94	RE36747	E	2000-06-27	Manabe et al.

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U.S.PATENT APPLICATION PUBLICATIONS

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear

Receipt date: 08/08/2016

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1	20020040982	A1	2002-04-11	Uemura
2	20020063258	A1	2002-05-30	Motoki
3	20020068373	A1	2002-06-06	Lo et al.
4	20020070387	A1	2002-06-13	Wang et al.
5	20030010989	A1	2003-01-16	Yukimoto
6	20030067082	A1	2003-04-10	Moshayedi
7	20030222270	A1	2003-12-04	Uemura
8	20030230606	A1	2003-12-18	Devinie
9	20040012958	A1	2004-01-22	Hashimoto et al.
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12	20040211972	A1	2004-10-28	Du et al.
13	20050001225	A1	2005-01-06	Yoshimura et al.
14	20050006659	A1	2005-01-13	Ng et al.
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20	20050248259	A1	2005-11-10	Chang
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22	20060001035	A1	2006-01-05	Suehiro et al.

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23	20060043433	A1	2006-03-02	Matsushita
24	20060081858	A1	2006-04-20	Lin et al.
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29	20060183625	A1	2006-08-17	Miyahara
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34	20070145392	A1	2007-06-28	Haberem et al.
35	20070257901	A1	2007-11-08	Gotou et al.
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37	20080029761	A1	2008-02-07	Peng
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39	20080099890	A1	2008-05-01	Chen et al.
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42	20080182369	A1	2008-07-31	Jeong et al.
43	20080290364	A1	2008-11-27	Kamiya et al.
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Receipt date: 08/08/2016

90013725 - GAU: 3992

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		90013725
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	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
Attorney Docket Number		114898-8904.US00	

45	20090152740	A1	2009-06-18	Park et al.
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48	20100155941	A1	2010-06-24	Matsuki et al.
49	20100176405	A1	2010-07-15	Villard

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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90013725 - GAU: 3992

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		90013725
	Filing Date		2016-04-15
	First Named Inventor	Won Cheol Seo	
	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
Attorney Docket Number		114898-8904.US00	

EXAMINER SIGNATURE			
Examiner Signature	/TUAN H NGUYEN/	Date Considered	09/06/2016
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			
¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.			

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	90013725
Filing Date	2016-04-15
First Named Inventor	Won Cheol Seo
Art Unit	3992
Examiner Name	NGUYEN, TUAN H
Attorney Docket Number	114898-8904.US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Bing Ai/	Date (YYYY-MM-DD)	2016-08-08
Name/Print	Bing Ai	Registration Number	43312

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
90/013,725	04/15/2016	9070851	MT100

97075
Perkins Coie LLP - SDO General
PO Box 1247
Seattle, WA 98111-1247

CONFIRMATION NO. 7313
POA ACCEPTANCE LETTER



Date Mailed: 08/11/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/08/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rswalker/



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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
90/013,725	04/15/2016	9070851	MT100

58027
H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

CONFIRMATION NO. 7313
POWER OF ATTORNEY NOTICE



OC000000085002278

Date Mailed: 08/11/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/08/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rswalker/

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Won Cheol Seo et al.Application No./Patent No.: 90/013,725 - 9,070,851 Filed/Issue Date: April 15, 2016Titled: Wafer-Level Light Emitting Diode Package and Method of Fabricating the SameSeoul Semiconductor Co., Ltd., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 026688, Frame 0805, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

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[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Bing Ai/

2016-08-09

Signature

Date

Bing Ai

43312

Printed or Typed Name

Title or Registration Number

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Under 37 C.F.R. 1.550, I hereby certify that, on August 9, 2016, I caused a true and correct copy of the foregoing STATEMENT UNDER 37 CFR 3.73(c) filed in the Reexam Proceeding Control No. 90/013,725 (U.S. Patent No. 9,070,851) to be served, in compliance with 37 C.F.R. 1.248(a)(4), via First Class U.S. Mail on the third party requestor in the *ex parte* reexamination file under Control Number 90/013,725 via its attorney of record:

Alan Taboada - Moser Taboada
1030 Broad Street, Suite 203
Shrewsbury, NJ 07702

Date: August 9, 2016

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Electronic Acknowledgement Receipt	
EFS ID:	26595205
Application Number:	90013725
International Application Number:	
Confirmation Number:	7313
Title of Invention:	Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same
First Named Inventor/Applicant Name:	9070851
Customer Number:	58027
Filer:	Bing Ai/Meghan Bright
Filer Authorized By:	Bing Ai
Attorney Docket Number:	MT100
Receipt Date:	09-AUG-2016
Filing Date:	15-APR-2016
Time Stamp:	18:43:06
Application Type:	Reexam (Patent Owner)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	373_Statement.pdf	80872	no	3
			f08af6a98d946ac207ca2650329ca2c218604763		

Warnings:

Information:					
2	Reexam Certificate of Service	COS.pdf	90459	no	1
			418cac3c4812648152e2b993609d76a9d4e60d32		
Warnings:					
Information:					
Total Files Size (in bytes):				171331	
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REEXAMINATION – PATENT OWNER POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Control Number(s)</td> <td>90/013,725</td> </tr> <tr> <td>Filing Date(s)</td> <td>April 15, 2016</td> </tr> <tr> <td>First Named Inventor</td> <td>Won Cheol Seo</td> </tr> <tr> <td>Title</td> <td>WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME</td> </tr> <tr> <td>Patent Number</td> <td>9,070,851</td> </tr> <tr> <td>Examiner Name</td> <td>Nguyen, Tuan H.</td> </tr> <tr> <td>Attorney Docket No(s)</td> <td>114898-8904 US00</td> </tr> </table>	Control Number(s)	90/013,725	Filing Date(s)	April 15, 2016	First Named Inventor	Won Cheol Seo	Title	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME	Patent Number	9,070,851	Examiner Name	Nguyen, Tuan H.	Attorney Docket No(s)	114898-8904 US00
Control Number(s)	90/013,725														
Filing Date(s)	April 15, 2016														
First Named Inventor	Won Cheol Seo														
Title	WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME														
Patent Number	9,070,851														
Examiner Name	Nguyen, Tuan H.														
Attorney Docket No(s)	114898-8904 US00														

I hereby revoke all previous patent owner powers of attorney given in the above-identified reexamination proceeding control number(s).

☐ A Power of Attorney is submitted herewith.
 OR
☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the proceedings identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

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I am the:

☐ Inventor, having ownership of the patent being reexamined.
 OR
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 Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on August 2, 2011.

SIGNATURE of Inventor or Patent Owner

Signature	Date
Name	Telephone
Title and Company	

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 1 forms are submitted.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	90013725
	Filing Date	2016-04-15
	First Named Inventor	Won Cheol Seo
	Art Unit	3992
	Examiner Name	NGUYEN, TUAN H
	Attorney Docket Number	114898-8904.US00

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

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Name/Print	Bing Ai	Registration Number	43312

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		90013725
	Filing Date		2016-04-15
	First Named Inventor	Won Cheol Seo	
	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
	Attorney Docket Number	114898-8904.US00	

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	Attorney Docket Number	114898-8904.US00	

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	Attorney Docket Number	114898-8904.US00	

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	Attorney Docket Number	114898-8904.US00	

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	Attorney Docket Number	114898-8904.US00	

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	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
Attorney Docket Number		114898-8904.US00	

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	First Named Inventor	Won Cheol Seo	
	Art Unit	3992	
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	Filing Date		2016-04-15
	First Named Inventor	Won Cheol Seo	
	Art Unit	3992	
	Examiner Name	NGUYEN, TUAN H	
	Attorney Docket Number	114898-8904.US00	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Bing Ai/	Date (YYYY-MM-DD)	2016-08-08
Name/Print	Bing Ai	Registration Number	43312

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Under 37 C.F.R. 1.550, I hereby certify that, on August 8, 2016, I caused a true and correct copy of the foregoing PATENT OWNER POWER OF ATTORNEY and related INFORMATION DISCLOSURE STATEMENTS filed in the Reexam Proceeding Control No. 90/013,725 (U.S. Patent No. 9,070,851) to be served, in compliance with 37 C.F.R. 1.248(a)(4), via First Class U.S. Mail on the third party requestor in the *ex parte* reexamination file under Control Number 90/013,725 via its attorney of record:

Alan Taboada - Moser Taboada
1030 Broad Street, Suite 203
Shrewsbury, NJ 07702

Date: August 8, 2016

/Bing Ai/
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Attorney for Assignee Seoul Semiconductor,
Co. Ltd.

Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
Telephone: (858) 720-5700
Facsimile: (206) 359-7198

Electronic Acknowledgement Receipt	
EFS ID:	26577128
Application Number:	90013725
International Application Number:	
Confirmation Number:	7313
Title of Invention:	Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same
First Named Inventor/Applicant Name:	9070851
Customer Number:	58027
Filer:	Bing Ai/Meghan Bright
Filer Authorized By:	Bing Ai
Attorney Docket Number:	MT100
Receipt Date:	08-AUG-2016
Filing Date:	15-APR-2016
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Application Type:	Reexam (Patent Owner)

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4	Reexam Certificate of Service	COS.pdf	90583	no	1
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CONFIRMATION NO. 7313

SERIAL NUMBER 90/013,725	FILING or 371(c) DATE 04/15/2016 RULE	CLASS 257	GROUP ART UNIT 3992	ATTORNEY DOCKET NO. MT100	
APPLICANTS INVENTORS 9070851, Residence Not Provided; SEOUL SEMICONDUCTOR CO., LTD. (ASSIGNEE), SEOUL, KOREA, REPUBLIC OF; ALAN TABOADA - MOSER TABOADA (3RD PTY REQ.), SHREWSBURY, NJ; ALAN TABOADA - MOSER TABOADA, SHREWSBURY, NJ ** CONTINUING DATA ***** This application is a REX of 13/194,317 07/29/2011 PAT 9070851 ** FOREIGN APPLICATIONS ***** REPUBLIC OF KOREA 10-2010-0092807 09/24/2010 REPUBLIC OF KOREA 10-2010-0092808 09/24/2010 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **					
Foreign Priority claimed ☐ Yes ☐ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged ☐ Yes ☐ No Examiner's Signature _____ Initials _____		☐ Met after Allowance STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS 15	INDEPENDENT CLAIMS 1
ADDRESS Perkins Coie LLP - SDO General PO Box 1247 Seattle, WA 98111-1247 UNITED STATES					
TITLE Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same					
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/013,725	04/15/2016	9070851	MT100	7313

58027 7590 05/18/2016
H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
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EXAMINER
NGUYEN, TUAN H

ART UNIT	PAPER NUMBER
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REEXAMINATION CONTROL NO. 90/013,725.

PATENT NO. 9070851.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

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DECISION ON REQUEST FOR REEXAMINATION

The present application is being examined under the pre-AIA first to invent provisions.

Reexamination has been requested for claims 1-15 of United States Patent number 9,070,851 to Seo et al., entitled: "WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME" (hereinafter "the '851 patent").

A substantial new question of patentability affecting claims 1-15 of the '851 patent is raised by the request for ex parte reexamination.

Substantial New Question of Patentability

In the request for reexamination, the requester alleges that the following prior art references raise a substantial new question of patentability of the issued claims 1-15 of the '851 patent.

Prior Art Relied Upon

Following is a list of the prior art relied upon in the section entitled "Substantial New Question of Patentability".

- 1) US 7,179,670 to Shelton et al. (hereinafter "Shelton").
- 2) US 8,368,100 to Donofrio et al. (hereinafter "Donofrio").
- 3) US 7,564,887 to Wang et al. (hereinafter "Wang").
- 4) US 6,657,236 to Thibault et al. (hereinafter "Thibault").

- 5) US 7,335,517 to Hayasaka et al. (hereinafter "Hayasaka").
- 6) US 6,838,702 to Ho (hereinafter "Ho").
- 7) US 2009/0140272 to Beeson et al. (hereinafter "Beeson").
- 8) JP 4,151,284 to Seiichiro et al. (hereinafter "Seiichiro").
- 9) JP 2002-319704 to Takuma et al. (hereinafter "Takuma").
- 10) JP 11008414 to Etsuo (hereinafter "Etsuo").
- 11) KR 610650 to Hwan (hereinafter "Hwan").

Prosecution History

Following is a brief summary of the most relevant portions regarding the prosecution of application 13/194,317 that matured into U.S. Patent No. 9,070,851:

The base application was filed on 07/29/2011 which claims priority from Foreign applications No. KR 10-2010-0092807 and KR 10-2010-0092808 filed on 09/24/2010.

Review of the prosecution history of the base application reveals that:

On Jan. 15, 2015, the Examiner of record issued an Ex Parte Quale Action allowing claims 1-15, and requiring cancellation of non-elected claims 16-41.

On Feb. 11, 2015, Applicant filed a Reply to Ex Parte Quale Action canceling non-elected claims 16-41.

On Feb. 17, 2015, the Examiner mailed a Notice of Allowance allowing claims 1-15 for the reason as noted previously in the Ex Parte Quale Action under an Examiner's statement of reason for allowance that:

Prior art does not teach or render obvious a LED having an arrangement as claimed such as a “first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.”

Substantial New Question

In view of the prosecution history, it is considered that the evaluation of a prior art reference that teaches or suggests a LED having an arrangement as claimed such as a *“first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.”* would have been considered important in determining the patentability of the claims.

Issues Raised in the Request

In the request filed April 15, 2016, the Requester alleges that the following cited references raise substantial new question of patentability as noted below:

Issue A. Seiichiro either alone or in combination with others.

The Requester asserts that Seiichiro either alone (SNQ #1) or in combination with others (SNQ # 4-11, 25) raises a substantial new question of patentability regarding claims 1-15.

Issue B. Shelton either alone or in combination with others.

The Requester asserts that Shelton either alone (SNQs # 2) or in combination with others (SNQs # 12-18, 26) raises a substantial new question of patentability regarding claims 1-15.

Issue C. Donofrio either alone or in combination with others.

The Requester asserts that Donofrio either alone (SNQs # 3) or in combination with others (SNQs # 19-24) raises a substantial new question of patentability regarding claims 1-15.

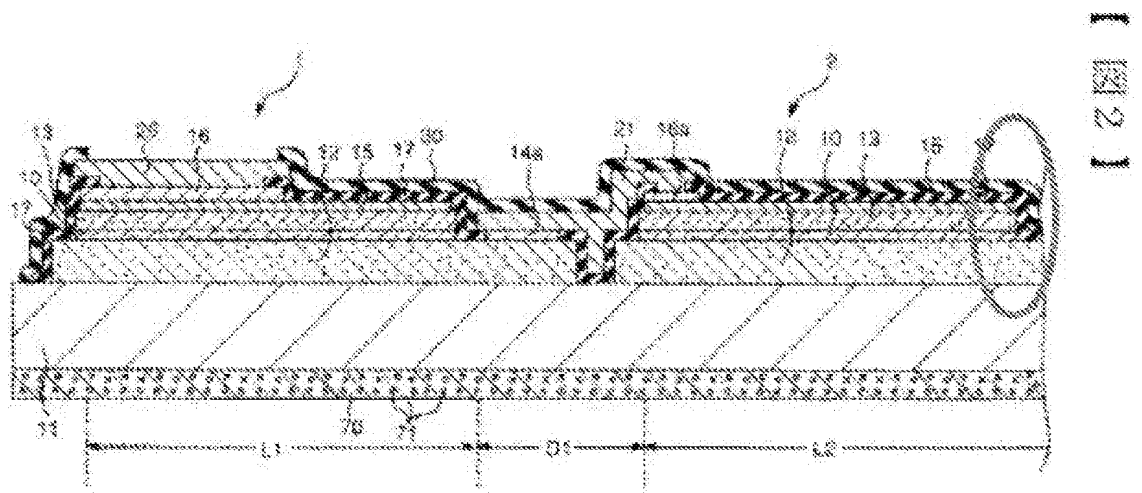
Detailed Explanation

Issue A. Seiichiro either alone or in combination with others.

It is agreed that the consideration of Seiichiro either alone (SNQ #1) or in combination with others (SNQ # 4-11, 25) raises a substantial new question of patentability regarding claims 1-15 of the '851 patent as pointed out in the claim chart of the request.

Regarding SNQ # 1:

Seiichiro, Fig. 2 as shown below appears to disclose a light emitting diode (LED) package, comprising: a semiconductor stack comprising a first conductive type semiconductor layer 12, an active layer 10, and a second conductive type semiconductor layer 13; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump 21 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 12 via the plurality of contact holes; a second bump 26 arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer 13; and a protective insulation layer 17, 30 covering a sidewall of the semiconductor stack.



Since Seiichiro discloses or suggests at least the main components of the '851 invention either alone or in view of others as noted above, Seiichiro teaches or suggests

a LED having an arrangement as claimed such as a *“first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.”* which is directly related to the subject matter considered as the basis for allowability of the patent claims.

Regarding SNQs # 4-11, 25:

The allegations of SNQs # 4-11, 25 over dependent claims based on the alleged SNQ # 1 above, namely the assumption that Seiichiro raises SNQ over independent claim. As such alleged SNQ #1 is agreed to be raised by Seiichiro, the alleged SNQs # 4-11, 25 are raised as well for the same reasons set forth above.

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims 1-15 are patentable. The prosecution history of the base application does not indicate that Seiichiro either alone or in view of others were included for consideration by the examiner in charge of the base application. Accordingly, such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously

considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Thus, Issue A raises a substantial new question regarding claims 1-15 of the '851 patent.

Issue B. Shelton either alone or in combination with others.

It is agreed that the consideration of Shelton either alone (SNQ #2) or in combination with others (SNQs # 12-18, 26) raises a substantial new question of patentability regarding claims 1-15 of the '851 patent as pointed out in the claim chart of the request.

Regarding SNQ # 2:

Shelton, Fig. 10 as shown below appears to disclose a light emitting diode (LED) package, comprising: a semiconductor stack comprising a first conductive type semiconductor layer 22, an active layer (i.e. part of layer 24, col. 4, last paragraph), and a second conductive type semiconductor layer 24; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer 22; a first bump 56 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 22 via the plurality of contact holes; a second bump 56 arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor

layer 24; and a protective insulation layer 32 covering a sidewall of the semiconductor stack.

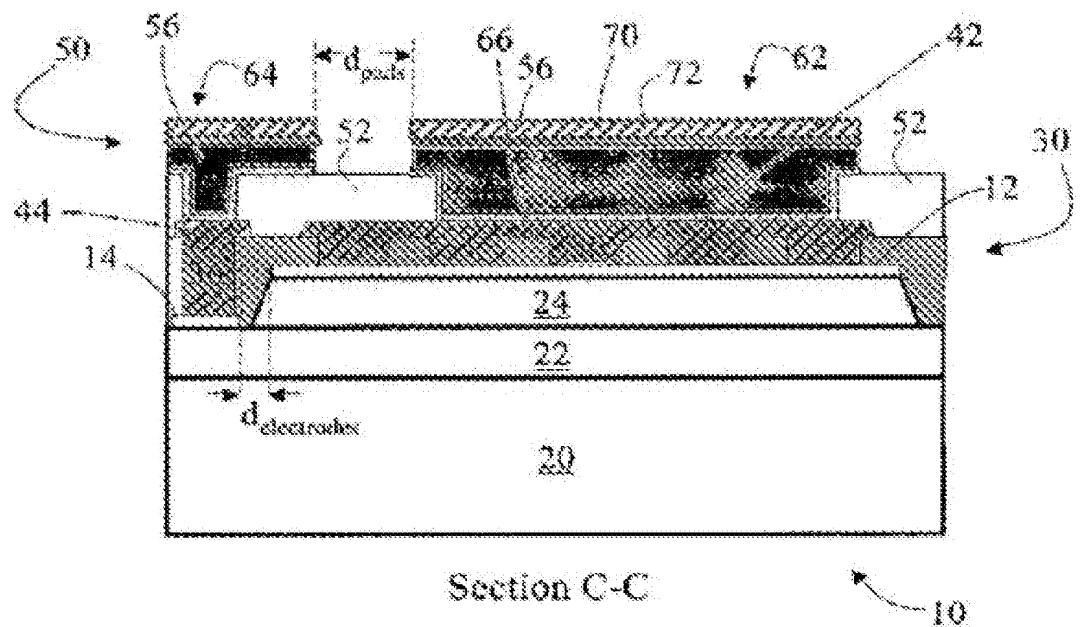


FIG 10

Since Shelton discloses or suggests at least the main components of the '851 invention either alone or in view of others as noted above, Shelton teaches or suggests a LED having an arrangement as claimed such as a *“first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.”* which is

directly related to the subject matter considered as the basis for allowability of the patent claims.

Regarding SNQs # 12-18, 26:

The allegations of SNQs # 12-18, 26 over dependent claims based on the alleged SNQ # 2 above, namely the assumption that Shelton raises SNQ over independent claim. As such alleged SNQ #2 is agreed to be raised by Shelton, the alleged SNQs # 12-18, 26 are raised as well for the same reasons set forth above.

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims 1-15 are patentable. The prosecution history of the base application does not indicate that Shelton either alone or in view of others were included for consideration by the examiner in charge of the base application. Accordingly, such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Thus, Issue B raises a substantial new question regarding claims 1-15 of the '851 patent.

Issue C. Donofrio either alone or in combination with others.

It is agreed that the consideration of Donofrio alone (SNQ # 3) or in combination with others (SNQs # 19-24) raises a substantial new question of patentability regarding claims 1-15 of the '851 patent as pointed out in the claim chart of the request.

Donofrio, fig. 1 as shown below appears to disclose a light emitting diode (LED) package, comprising: a semiconductor stack comprising a first conductive type semiconductor layer 112, an active layer 116 and a second conductive type semiconductor layer 114; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer 112; a first bump 170 arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer 112 via the plurality of contact holes; a second bump 160 arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer 114; and a protective insulation layer 140 covering a sidewall of the semiconductor stack.

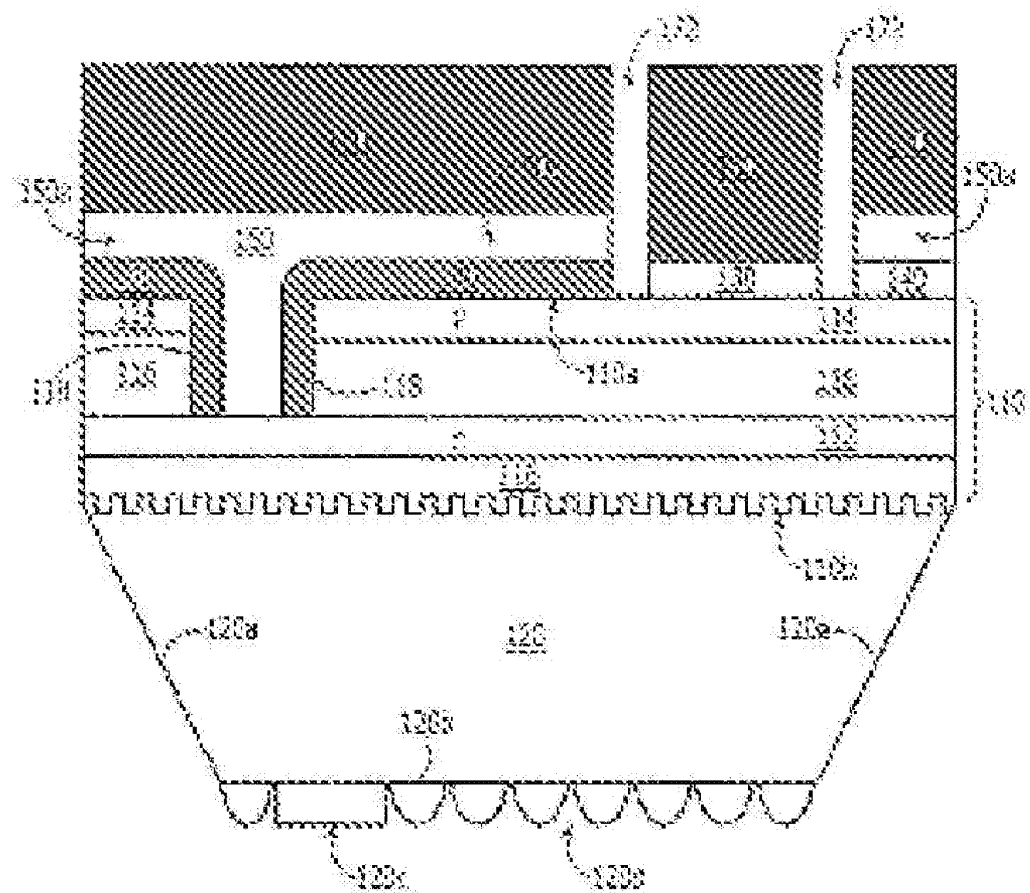


FIG. 1

Since Donofrio discloses or suggests at least the main components of the '851 invention either alone or in view of others as noted above, Donofrio teaches or suggests a LED having an arrangement as claimed such as a *"first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a*

protective insulation layer covering a sidewall of the semiconductor stack.” which is directly related to the subject matter considered as the basis for allowability of the patent claims.

Regarding SNQs # 19-24:

The allegations of SNQs # 19-24 over dependent claims based on the alleged SNQ # 3 above, namely the assumption that Donofrio raises SNQ over independent claim. As such alleged SNQ #3 is agreed to be raised by Donofrio, the alleged SNQs # 19-24 are raised as well for the same reasons set forth above.

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims 1-15 are patentable. The prosecution history of the base application does not indicate that Donofrio either alone or in view of others were included for consideration by the examiner in charge of the base application. Accordingly, such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered nor addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by Federal Courts.

Thus, Issue C raises a substantial new question regarding claims 1-15 of the ‘851 patent.

Accordingly the request for reexamination is GRANT. Claims 1-15 of the '851 patent will be reexamined.

Conclusion

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 9,070,851 throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

All correspondence relating to this Inter Partes reexamination proceeding should be directed as follows:

By U.S. Postal Service Mail to:

Application/Control Number: 90/013,725
Art Unit: 3992

Page 15

Mail Stop Inter Partes Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building
401 Dulany St. Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

/Tuan H. Nguyen/

Tuan H. Nguyen
Primary Examiner
Central Reexamination Unit
Art Unit 3992

Conferees:

/Minh Nguyen/
Primary Examiner
CRU, AU 3992

/Timothy M. Speer/
Supervisory Patent Reexamination Specialist
CRU, AU 3992

Application/Control Number: 90/013,725
Art Unit: 3992

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Order Granting Request For Ex Parte Reexamination	Control No. 90/013,725	Patent Under Reexamination 9070851
	Examiner TUAN H. NGUYEN	Art Unit 3992

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 15 April 2016 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a) ☐ PTO-892, b) ☒ PTO/SB/08, c) ☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

cc:Requester (if third party requester)

U.S. Patent and Trademark Office
PTOL-471G(Rev. 01-13)

Office Action in *Ex Parte* Reexamination

Part of Paper No. 20160503

Search Notes 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Examiner TUAN H NGUYEN	Art Unit 3992

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed of patented file's prosecution history	5/5/2016	TN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Reexamination 	Application/Control No. 90013725	Applicant(s)/Patent Under Reexamination 9070851
	Certificate Date	Certificate Number

Requester Correspondence Address:	☐ Patent Owner	☒ Third Party
ALAN TABOADA - MOSER TABOADA 1030 BROAD STREET, SUITE 203 SHREWSBURY, NJ 07702		

LITIGATION REVIEW ☒	TN (examiner initials)	05/09/2016 (date)
Case Name		Director Initials
None		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
1. No concurrent proceeding	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	13/194,317
		Filing Date	July 29, 2011
		First Named Inventor	Won Cheol Seo
		Art Unit	
		Examiner Name	
		Attorney Docket Number	MT100
Sheet	1	of	1

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			
		JP-4151284-b	2008-07-11	Nichia Chem Ind. Ltd.		
		JP-2002-319704-A	2002-10-31	Matsumita Electric Works		
		KR-610650-B1	2006-08-09	FIONIX Inc.		
		JP-11-008414-A	1999-01-12	Sony Corp.		

Examiner Signature	/TUAN H NGUYEN/	Date Considered	05/05/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Litigation Search Report CRU 3999

Serial No. 90/013,725

To: NGUYEN, Tuan
Location: Central Reexam Unit
Art Unit: 3992
Date: 5/16/16

Case Serial Number: 90/013,725

From: Monica A. Graves
Location: CRU 3999, MDW 4B31
Phone: (571) 272-7253

monica.graves@uspto.gov

Search Notes

Litigation search for U.S. Patent Number – 9,070,851

No Litigation Found

- 1) I performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.
- 2) I performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.
- 3) I performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.
- 4) I performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.
- 5) I performed a search in Lexis in the news databases for any articles about the patent or any articles about litigation on this patent.

Citing References (11)

Treatment	Title	Date	Type	Depth	Headnote(s)
—	1. WAFER-LEVEL LED PACKAGE FOR USE IN DISPLAY DEVICE, HAS BUMP ELECTRICALLY CONNECTED TO CONDUCTIVE TYPE SEMICONDUCTOR LAYER, AND PROTECTIVE INSULATION LAYER COVERING SIDEWALL OF SEMICONDUCTOR STACK Out Of Focus DWPI 2012-D67960 ... type upper portion semiconductor layer, the active layer, and the second conductivity type bottom half conductive layer.First Derwent Appearance:2014.55 Publication No. (Derwent): US 9070851 B2 Original Title (English):WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME Publication Date:2015-06-30 Application No.:US ...	Sep. 24, 2010	DWPI	—	—
—	2. METHOD OF FABRICATING LED IN DISPLAY DEVICES, INVOLVES FORMING PADS THAT ARE ELECTRICALLY CONNECTED TO RESPECTIVE SEMICONDUCTOR LAYERS AND FORMING DUMMY BUMP TO PROVIDE HEAT PASSAGE FOR DISCHARGING HEAT FROM SEMICONDUCTOR STACK Out Of Focus DWPI 2015-49976A+ ... 092807 2010-09-24 Application priority KR 092808 2010-09-24 Application priority Earliest Priority Date:2010-09-24 Related:Continuation of US patent number US 9070851 B Continuation of US patent number US 9070851 B No. of Countries:1 No. of Patents:2 First Derwent Appearance:2015.60 Latest Derwent ...	Sep. 24, 2010	DWPI	—	—
—	3. LED PACKAGE OF LED MODULE USED IN DISPLAY DEVICE, HAS BUMPS THAT ARE ARRANGED ON SIDES OF LIGHT EMITTING CELLS AND ELECTRICALLY CONNECTED TO CONDUCTIVE TYPE SEMICONDUCTOR LAYERS OF LIGHT EMITTING CELLS Out Of Focus DWPI 2015-52815K+ ... s):KR 092807 2010-09-24 Application priority KR 092808 2010-09-24 Application priority Earliest Priority Date:2010-09-24 Related:Division of patent US 9070851 B Division of patent US 9070851 B No. of Countries:1 No. of Patents:2 First Derwent Appearance:2015.62 Latest Derwent Appearance:2015 ...	Sep. 24, 2010	DWPI	—	—

Treatment	Title	Date	Type	Depth	Headnote(s)
---	4. WAFER-LEVEL LED PACKAGE FOR USE IN LIGHT SOURCE MODULE FOR E.G. DISPLAY DEVICES, HAS PROTECTIVE INSULATION LAYER FOR COVERING SIDEWALL OF CONDUCTIVE TYPE SEMICONDUCTOR LAYERS AND INCLUDING INSULATION LAYERS WITH INDICES OF REFRACTION Get Citations DWPI 2015-73646A+ ... 092807 2010-09-24 Application priority KR 092808 2010-09-24 Application priority Earliest Priority Date:2010-09-24 Related:Continuation of US patent number US 9070851 B Continuation of US patent number US 9070851 B No. of Countries:1 No. of Patents:2 First Derwent Appearance:2015.82 Latest Derwent ...	Sep. 24, 2010	DWPI	---	---
---	5. RF 026688/0805 Get Citations ... United States Patent Assignments U.S. Patent & Trademark Office (USPTO)Reel/Frame: 026688/0805 Patents Affected:Patent Number: U.S. Pat. 9070851 Issue Date: June 30, 2015 Patent Number: U.S. Pat. App. 20120074441 Pub. Date: March 29, 2012 Application Number: 13/194317 App. Date Filed ...	Aug. 02, 2011	Assignments	---	---
---	6. WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME Get Citations US PAT 9293664 , U.S. PTO Utility Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a... ... of application No. 14/708,029, filed on 2015/05/08, which is a continuation of application No. 13/194,317, filed on 2011/07/29, now Pat. No. 9,070,851 , 2015/06/30 Previously published as US 2015/0340579 A1, 2015/11/26 Priority Application(s):KR KR 10-2010-0092807 2010/09 ...	Mar. 22, 2016	Patents	---	---
---	7. WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME Get Citations US PAT 9219196 , U.S. PTO Utility Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a... ... s);Perkins Cole LLP Examiner(s):Nguyen, Cuong Q Priority Information Related Information:Continuation of application No. 13/194,317, filed on 2011/07/29, now Pat. No. 9,070,851 Previously published as US 2015/0243844 A1, 2015/08/27 Priority Application(s):KR KR 10-2010-0092807 2010/09/24 Republic of ...	Dec. 22, 2015	Patents	---	---

Treatment	Title	Date	Type	Depth	Headnote(s)
---	8. WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME [Out Of Place] US PAT 9153750 , U.S. PTO Utility A light emitting diode (LED) package includes a plurality of light emitting cells each including a first conductive type semiconductor layer, an active layer, and a second... ... H.C. Park & Associates, PLC Examiner(s):Nguyen, Cuong Q Priority Information Related Information:Division of application No. 13/194,317, filed on 2011/07/29, now Pat. No. 9,070,851 Previously published as US 2015/0255686 A1, 2015/09/10 Priority Application(s):KR KR 10-2010-0092807 2010/09/24 Republic of ...	Oct. 06, 2015	Patents	---	---
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June 30, 2015

Wafer-level light emitting diode package and method of fabricating the same

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CORE TERMS: layer, insulation, semiconductor, bump, conductive, package, pad, emitting, electrode, cell, substrate, stack, holes, exemplary, region, wavelength, chip, convertor, composed, module, fabricating, exposed, silicon, electrically, expose, diode, protective, connector, connecting, sidewall

ENGLISH-ABST:

Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

NO-OF-CLAIMS: 15

EXMPL-CLAIM: 1

NO-OF-FIGURES: 27

NO-DRWG-PP: 19

SUMMARY:

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from and the benefit of Korean Patent Application No. 10-2010-0092807, filed on Sep. 24, 2010, and Korean Patent Application No. 10-2010-0092808, filed on Sep. 24, 2010, which are hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to a light emitting diode package and a method of fabricating the same and, more particularly, to a wafer-level light emitting diode package and a method of fabricating the same.

[0004] 2. Description of the Background

[0005] A light emitting diode (LED) is a semiconductor device that includes an N-type semiconductor and a P-type semiconductor, and emits light through recombination of holes and electrons. Such an LED has been used in a wide range of applications such as display devices, traffic lights, and backlight units. Further, considering the potential merits of lower power consumption and longer lifespan than existing electric bulbs or fluorescent lamps, the application range of LEDs has been expanded to general lighting by replacing existing incandescent lamps and fluorescent lamps.

[0006] The LED may be used in an LED module. The LED module is manufactured through a process of fabricating an LED chip at a wafer level, a packaging process, and a modulation process. Specifically, semiconductor layers are grown on a substrate such as a sapphire substrate, and subjected to a wafer-level patterning process to fabricate LED chips having electrode pads, followed by division into individual chips (chip fabrication process). Then, after mounting the individual chips on a lead frame or a printed circuit board, the electrode pads are electrically connected to lead terminals via bonding wires, and the LED chips are covered by a molding member, thereby providing an LED package (packaging process). Then, the LED package is mounted on a circuit board such as a metal core printed circuit board (MC-PCB), thereby providing an LED module such as a light source module (modulation process).

[0007] In the packaging process, a housing and/or the molding member may be provided to the LED chip to protect the LED chip from the external environment. In addition, a phosphor may be contained in the molding member to convert light emitted by the LED chip so that the LED package may emit a white light, thereby providing a white LED package. Such a white LED package may be mounted on the circuit board such as the MC-PCB and a secondary lens may be provided to the LED package to adjust orientation characteristics of light emitted from the LED package, thereby providing a desired white LED module.

[0008] However, it may be difficult to achieve miniaturization and satisfactory heat dissipation of the conventional LED package including the lead frame or printed circuit board. Furthermore, luminous efficiency of the LED may be deteriorated due to absorption of light by the lead frame or the printed circuit board, electric resistance heating by the lead terminals, and the like.

[0009] In addition, the chip fabrication process, the packaging process, and the modulation process may be separately carried out, thereby increasing time and costs for manufacturing the LED module.

[0010] Meanwhile, alternating current (AC) LEDs have been produced and marketed. The AC LED includes an LED directly connected to an AC power source to permit continuous emission of light. One example of AC LEDs, which can be used by being directly connected to a high voltage AC power source, is disclosed in U.S. Pat. No. 7,417,259, issued to Sakai, et. al.

[0011] According to U.S. Pat. No. 7,417,259, LED elements are arranged in a two-dimensional pattern on an insulating substrate, for example, a sapphire substrate, and are connected in series to form LED arrays. The LED arrays are connected in series to each other, thereby providing a light emitting device that can be operated at high voltage. Further, such LED arrays may be connected in reverse parallel to each other on the sapphire substrate, thereby providing a single-chip light emitting device that can be operated to continuously emit light using an AC power supply.

[0012] Since the AC-LED includes light emitting cells on a growth substrate, for example, on a sapphire substrate, the AC-LED restricts the structure of the light emitting cells and may limit improvement of light extraction efficiency. Thus, investigation has been made into a light emitting diode, for example, an AC-LED that is based on a substrate separation process and includes light emitting cells connected in series to each other.

SUMMARY OF THE INVENTION

[0013] Exemplary embodiments of the invention provide a wafer-level LED package and a method of fabricating the same, which can be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board.

[0014] Exemplary embodiments of the invention also provide a wafer-level LED package and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

[0015] Exemplary embodiments of the invention also provide a method of fabricating an LED package, which may

reduce manufacturing time and cost of an LED module.

[0016] Exemplary embodiments of the invention also provide an LED module and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

[0017] Exemplary embodiments of the invention also provide a wafer-level light emitting diode package and a method of fabricating the same, which includes a plurality of light emitting cells and may be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board.

[0018] Additional features of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention.

[0019] An exemplary embodiment of the present invention discloses an LED package including: a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

[0020] An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package according to the aforementioned exemplary embodiments. The LED module may include a circuit board; the LED package mounted on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

[0021] An exemplary embodiment of the present invention also discloses a method of fabricating an LED package. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of contact holes exposing the first conductive type semiconductor layer; forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region; and forming a first bump and a second bump on the semiconductor stack. The first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes, and the second bump is electrically connected to the second conductive type semiconductor layer.

[0022] An exemplary embodiment of the present invention also discloses a light emitting diode package. The LED package includes a plurality of light emitting cells each including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer of each of the light emitting cells, the contact holes exposing the first conductive type semiconductor layer thereof; a protective insulation layer covering a sidewall of each of the light emitting cells; a connector located arranged on a first side of the light emitting cells and electrically connecting two adjacent light emitting cells to each other; a first bump arranged on the first side of the light emitting cells and electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells; and a second bump arranged in the first side of the light emitting cells and electrically connected to the second conductive type semiconductor layer of a second light emitting cell of the light emitting cells.

[0023] An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package described above. The module includes a circuit board; the LED package arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

[0024] An exemplary embodiment of the present invention also discloses a method of fabricating an LED package including a plurality of light emitting cells. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region and a light emitting cell separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of light emitting cells, each light emitting cell having a plurality of contact holes exposing the first conductive type semiconductor layer; forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region and the light emitting cell separation region; forming a

connector connecting adjacent light emitting cells in series to each other; and forming a first bump and a second bump on the plurality of light emitting cells. Here, the first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells, and the second bump is electrically connected to the second conductive type semiconductor layer of a second light emitting cell of the light emitting cells.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

DRWDESC:

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0027] FIG. 1 is a schematic sectional view of a light emitting diode package according to a first exemplary embodiment of the invention.

[0028] FIG. 2 is a schematic sectional view of a light emitting diode package according to a second exemplary embodiment of the invention.

[0029] FIG. 3 is a sectional view of a light emitting diode module including the light emitting diode package according to the first exemplary embodiment.

[0030] FIG. 4 to FIG. 12 show a method of fabricating the light emitting diode package according to the first exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in FIG. 5 to FIG. 10.

[0031] FIG. 13 is a sectional view showing a method of fabricating the light emitting diode package according to the second exemplary embodiment of the invention.

[0032] FIG. 14 is a schematic sectional view of a light emitting diode package according to a third exemplary embodiment of the invention.

[0033] FIG. 15 is a schematic sectional view of a light emitting diode package according to a fourth exemplary embodiment of the invention.

[0034] FIG. 16 is a sectional view of a light emitting diode module including the light emitting diode package according to the third exemplary embodiment.

[0035] FIG. 17 to FIG. 26 show a method of fabricating the light emitting diode package according to the third exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in FIG. 18 to FIG. 23.

[0036] FIG. 27 is a sectional view showing a method of fabricating the light emitting diode package according to the fourth exemplary embodiment of the invention.

DETDESC:

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0037] The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather,

these exemplary embodiments are provided so that this disclosure is thorough and will fully convey the scope of the invention to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0038] It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0039] FIG. 1 is a schematic sectional view of an LED package **100** according to a first exemplary embodiment of the invention.

[0040] Referring to FIG. 1, the LED package **100** may include a semiconductor stack **30**, a first contact layer **35**, a second contact layer **31**, a first insulation layer **33**, a second insulation layer **37**, a first electrode pad **39a**, a second electrode pad **39b**, a first bump **45a**, and a second bump **45b**. The LED package **100** may further include an insulation layer **43**, a dummy bump **45c**, and a wavelength convertor **51**.

[0041] The semiconductor stack **30** includes a first conductive type upper semiconductor layer **25**, an active layer **27**, and a second conductive type lower semiconductor layer **29**. The active layer **27** is interposed between the upper and lower semiconductor layers **25**, **29**.

[0042] The active layer **27** and the upper and lower semiconductor layers **25**, **29** may be composed of a III-N based compound semiconductor, for example, (Al, Ga, In)N semiconductor. Each of the upper and lower semiconductor layers **25**, **29** may be a single layer or multiple layers. For example, the upper and/or lower semiconductor layers **25**, **29** may include a super lattice layer in addition to a contact layer and a clad layer. The active layer **27** may have a single quantum well structure or a multi-quantum well structure. The first conductive type may be an n-type and the second conductive type may be a p-type. Alternatively, the first conductive type may be a p-type and the second conductive type may be an n-type. Since the upper semiconductor layer **25** can be formed of an n-type semiconductor layer having relatively low specific resistance, the upper semiconductor layer **25** may have a relatively high thickness. Therefore, a roughened surface R may be formed on an upper surface of the upper semiconductor layer **25**, in which the roughened surface R enhances extraction efficiency of light generated in the active layer **27**.

[0043] The semiconductor stack **30** has a plurality of contact holes **30a** (see FIG. 5(b)) formed through the second conductive type lower semiconductor layer **29** and the active layer **27** to expose the first conductive type upper semiconductor layer, and the first contact layer **35** contacts the first conductive type upper semiconductor layer **25** exposed in the plurality of contact holes.

[0044] The second contact layer **31** contacts the second conductive type lower semiconductor layer **29**. The second contact layer **31** includes a reflective metal layer to reflect light generated in the active layer **27**. Further, the second contact layer **31** may form an ohmic contact with the second conductive type lower semiconductor layer **29**.

[0045] The first insulation layer **33** covers the second contact layer **31**. Further, the first insulation layer **33** covers a sidewall of the semiconductor stack **30** exposed in the plurality of contact holes **30a**. In addition, the first insulation layer **33** may cover a side surface of the semiconductor stack **30**. The first insulation layer **33** insulates the first contact layer **35** from the second contact layer **31** while insulating the second conductive type lower semiconductor layer **29** and the active layer **27** exposed in the plurality of contact holes **30a** from the first contact layer **35**. The first insulation layer **33** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation layer **33** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, SiO₂/TiO₂ or SiO₂/Nb₂O₅.

[0046] The first contact layer **35** is located under the first insulation layer **33** and contacts the first conductive type upper semiconductor layer **25** through the first insulation layer **33** in the plurality of contact holes **30a**. The first contact layer **35** includes contact sections **35a** contacting the first conductive type upper semiconductor layer **25**, and a connecting section **35b** connecting the contact sections **35a** to each other. Therefore, the contact sections **35a** are electrically connected to each other by the connecting section **35b**. The first contact layer **35** is formed under some regions of the first insulation layer **33** and may be composed of a reflective metal layer.

[0047]The second insulation layer 37 covers the first contact layer 35 under the first contact layer 35. In addition, the second insulation layer 37 covers the first insulation layer 33 while covering a side surface of the semiconductor stack 30. The second insulation layer 37 may be composed of a single layer or multiple layers. Further, the second insulation layer 37 may be a distributed Bragg reflector.

[0048]The first and second electrode pads 39a, 39b are located under the second insulation layer 37. The first electrode pad 39a may be connected to the first contact layer 35 through the second insulation layer 37. Further, the second electrode pad 39b may be connected to the second contact layer 31 through the second insulation layer 37 and the first insulation layer 33.

[0049]The first bump 45a and the second bump 45b are located under the first and second electrode pads 39a, 39b to be connected thereto, respectively. The first and second bumps 45a, 45b may be formed by plating. The first and second bumps 45a, 45b are terminals electrically connected to a circuit board such as an MC-PCB and have coplanar distal ends. In addition, the first electrode pad 39a may be formed at the same level as that of the second electrode pad 39b, so that the first bump 45a and the second bump 45b may also be formed on the same plane. Therefore, the first and second bumps 45a, 45b may have the same height.

[0050]Meanwhile, the dummy bump 45c may be located between the first bump 45a and the second bump 45b. The dummy bump 45c may be formed together with the first and second bumps 45a and 45b to provide a heat passage for discharging heat from the semiconductor stack 30.

[0051]The insulation layer 43 may cover side surfaces of the first and second bumps 45a, 45b. The insulation layer 43 may also cover a side surface of the dummy bump 45c. In addition, the insulation layer 43 fills spaces between the first bump 45a, the second bump 45b and the dummy bump 45c to prevent moisture from entering the semiconductor stack 30 from outside. The insulation layer 43 also covers side surfaces of the first and second electrode pads 39a, 39b to protect the first and second electrode pads 39a, 39b from external environmental factors such as moisture. Although the insulation layer 43 may be configured to cover the overall side surfaces of the first and second bumps 45a, 45b, the invention is not limited thereto. Alternatively, the insulation layer 43 may cover the side surfaces of the first and second bumps 45a, 45b except for some regions of the side surface near distal ends of the first and second bumps.

[0052]In the present exemplary embodiment, the insulation layer 43 is illustrated as covering the side surfaces of the first and second electrode pads 39a and 39b, but the invention is not limited thereto. Alternatively, another insulation layer may be used to cover the first and second electrode pads 39a, 39b and the insulation layer 43 may be formed under the other insulation layer. In this case, the first and second bumps 45a, 45b may be connected to the first and second electrode pads 39a, 39b through the other insulation layer.

[0053]The wavelength convertor 51 may be located on the first conductive type upper semiconductor layer 25 opposite to the rest of the semiconductor stack 30. The wavelength convertor 51 may contact an upper surface of the first conductive type upper semiconductor layer 25. The wavelength convertor 51 may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength converter 51 may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength conversion.

[0054]In the present exemplary embodiment, the side surface of the semiconductor stack 30 is covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer 33 and/or the second insulation layer 37. In addition, the first contact layer 35 may be covered with the second insulation layer 37 to be protected from an external environment and the second contact layer 31 may be covered with the first insulation layer 33 and the second insulation layer 37 to be protected from an external environment. The first and second electrode pads 39a, 39b are also protected by, for example, the insulation layer 43. Accordingly, it is possible to prevent deterioration of the semiconductor stack 30 due to moisture.

[0055]The wavelength convertor 51 may be attached to the first conductive type upper semiconductor layer 25 at a wafer-level, and then divided together with the protective insulation layer during a chip separation process. Therefore, a side surface of the wavelength convertor 51 may be in a line with the protective insulation layer. That is, the side surface of the wavelength converter 51 may be flush along a straight line with a side surface of the protective insulation layer. Further, the side surface of the wavelength convertor 51 may be in a line with a side surface of the insulation layer 43. Thus, the side surfaces of the wavelength converter 51, the protective insulation layer, and the insulation layer 43 may all be flush along a straight line.

[0056] FIG. 2 is a schematic sectional view of a light emitting diode package **200** according to a second exemplary embodiment of the invention.

[0057] Referring to FIG. 2, the LED package **200** is similar to the LED package **100** according to the above exemplary embodiment. In the present exemplary embodiment, however, first and second bumps **65a**, **65b** are formed in a substrate **61**.

[0058] Specifically, the substrate **61** includes through-holes, which have the first and second bumps **65a**, **65b** formed therein, respectively. The substrate **61** is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto. The substrate **61** having the first and second bumps **65a**, **65b** may be attached to a first electrode pad **39a** and a second electrode pad **39b**. In this case, to prevent the first and second electrode pads **39a**, **39b** from being exposed to the outside, an insulation layer **49** may cover side surfaces and bottom surfaces of the first and second electrode pads **39a**, **39b**. Further, the insulation layer **49** may have openings, which expose the first and second electrode pads **39a**, **39b**, and additional metal layers **67a**, **67b** are then formed in the openings. The additional metal layers **67a**, **67b** may be composed of a bonding metal.

[0059] FIG. 3 is a sectional view of a light emitting diode module including the LED package **100** according to the first exemplary embodiment.

[0060] Referring to FIG. 3, the LED module includes a circuit board **71**, for example, an MC-PCB, the LED package **100**, and a lens **81**. The circuit board **71**, for example, the MC-PCB, has connection pads **73a**, **73b** for mounting the LED packages **100** thereon. The first and second bumps **45a**, **45b** (see FIG. 1) of the LED package **100** are connected to the connection pads **73a**, **73b**, respectively.

[0061] A plurality of LED packages **100** may be mounted on the circuit board **71** and the lens **81** may be disposed on the LED packages **100** to adjust an orientation angle of light emitted from the LED packages **100**.

[0062] In accordance with the second exemplary embodiment, the light emitting diode packages **200** may be mounted on the circuit board instead of the LED packages **100**.

[0063] FIG. 4 to FIG. 12 show a method of fabricating the LED package **100** according to the first exemplary embodiment. In FIG. 5 to FIG. 10, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

[0064] Referring to FIG. 4, a semiconductor stack **30**, which includes a first conductive type semiconductor layer **25**, an active layer **27** and a second conductive type semiconductor layer **29**, is formed on a growth substrate **21**. The growth substrate **21** may be a sapphire substrate but is not limited thereto. Alternatively, the growth substrate **21** may be another kind of heterogeneous substrate, for example, a silicon substrate. Each of the first and second conductive type semiconductor layers **25**, **29** may be composed of a single layer or multiple layers. Further, the active layer **27** may have a single-quantum well structure or multi-quantum well structure.

[0065] The compound semiconductor layers may be formed of III-N based compound semiconductor on the growth substrate **21** by metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE).

[0066] A buffer layer (not shown) may be formed before forming the compound semiconductor layers. The buffer layer is formed to relieve lattice mismatch between the growth substrate **21** and the compound semiconductor layers and may be formed of a GaN-based material layer such as gallium nitride or aluminum nitride.

[0067] Referring to (a) and (b) of FIG. 5, the semiconductor stack **30** is patterned to form a chip (package) separation region **30b** while patterning the second conductive type semiconductor layer **29** and the active layer **27** to form a plurality of contact holes **30a** exposing the first conductive type semiconductor layer **25**. The semiconductor stack **30** may be patterned by photolithography and etching processes.

[0068] The chip separation region **30b** is a region for dividing the LED package structure into individual LED packages and side surfaces of the first conductive type semiconductor layer **25**, the active layer **27** and the second conductive type semiconductor layer **29** are exposed on the chip separation region **30b**. Advantageously, the chip separation region **30b** may be configured to expose the substrate **21** without being limited thereto.

[0069] The plurality of contact holes **30a** may have a circular shape, but is not limited thereto. The contact holes **30** may have a variety of shapes. The second conductive type semiconductor layer **29** and the active layer **27**

are exposed to sidewalls of the plurality of contact holes **30a**. As shown, the contact holes **30a** may have slanted sidewalls.

[0070] Referring to (a) and (b) of FIG. 6, a second contact layer **31** is formed on the second conductive type semiconductor layer **29**. The second contact layer **31** is formed on the semiconductor stack **30** except for regions corresponding to the plurality of contact holes **30a**.

[0071] The second contact layer **31** may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al). The second contact layer **31** may be composed of a single layer or multiple layers. The second contact layer **31** may also be configured to form an ohmic contact with the second conductive type semiconductor layer **29**.

[0072] The second contact layer **31** may be formed before or after formation of the plurality of contact holes **30a**.

[0073] Referring to (a) and (b) of FIG. 7, a first insulation layer **33** is formed to cover the second contact layer **31**. The first insulation layer **33** may cover the side surface of the semiconductor stack **30** exposed to the chip separation region **30b** while covering the sidewalls of the plurality of contact holes **30a**. Here, the first insulation layer **33** may have openings **33a**, which expose the first conductive type semiconductor layer **25** in the plurality of contact holes **30a**.

[0074] The first insulation layer **33** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation layer **33** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction. For example, the first insulation layer **33** may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$. Further, the first insulation layer **33** may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

[0075] Referring to (a) and (b) of FIG. 8, a first contact layer **35** is formed on the first insulation layer **33**. The first contact layer **35** includes contact sections **35a** contacting the first conductive type upper semiconductor layer **25** exposed in the contact holes **30a**, and a connecting section **35b** connecting the contact sections **35a** to each other. The first contact layer **35** may be composed of a reflective metal layer, but is not limited thereto.

[0076] The first contact layer **35** is formed on some regions of the semiconductor stack **30**, so that the first insulation layer **33** is exposed on other regions of the semiconductor stack **30** where the first contact layer **35** is not formed.

[0077] Referring to (a) and (b) of FIG. 9, a second insulation layer **37** is formed on the first contact layer **35**. The second insulation layer **37** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Further, the second insulation layer **37** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

[0078] The second insulation layer **37** may cover the first contact layer **35** while covering the first insulation layer **33**. The second insulation layer **37** may also cover the side surface of the semiconductor stack **30** in the chip separation region **30b**.

[0079] The second insulation layer **37** has an opening **37a** which exposes the first contact layer **35**. Further, the second insulation layer **37** and the first insulation layer **33** are formed with an opening **37b**, which exposes the second contact layer **31**.

[0080] Referring to (a) and (b) of FIG. 10, first and second electrode pads **39a**, **39b** are formed on the second insulation layer **37**. The first electrode pad **39a** is connected to the first contact layer **35** through the opening **37a** and the second electrode pad **39b** is connected to the second contact layer **31** through the opening **37b**.

[0081] The first electrode pad **39a** is separated from the second electrode pad **39b** and each of the first and second electrode pads **39a**, **39b** may have a relatively large area from a top perspective, for example, an area not less than $\frac{1}{3}$ of the area of the LED package.

[0082] Referring to FIG. 11, an insulation layer **43** is formed on the first and second electrode pads **39a**, **39b**.

The insulation layer **43** covers the first and second electrode pads **39a**, **39b** and has grooves which expose upper surfaces of the electrode pads **39a**, **39b**. Further, the insulation layer **43** may have a groove which exposes the second insulation layer **37** between the first and second electrode pads **39a**, **39b**.

[0083] Then, first and second bump **45a**, **45b** are formed in the grooves of the insulation layer **43**, and a dummy bump **45c** may be formed between the first bump and the second bump.

[0084] The bumps may be formed by plating, for example, electroplating, using a metallic material. If necessary, a seed layer for plating may also be formed.

[0085] After the first and second bumps **45a**, **45b** are formed, the insulation layer **43** may be removed. For example, the insulation layer **43** may be formed of a polymer such as photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer **43** may remain to protect the side surfaces of the first and second bumps **45a**, **45b**.

[0086] In the present exemplary embodiment, the insulation layer **43** is illustrated as being directly formed on the first and second electrode pads **39a**, **39b**. In other exemplary embodiments, another insulation layer may be formed to cover the first and second electrode pads **39a**, **39b**. The other insulation layer may be configured to have openings exposing the first and second electrode pads **39a**, **39b**. Then, the processes of forming the insulation layer **43** and the bumps may be carried out.

[0087] Referring to FIG. 12, the growth substrate **21** is removed and a wavelength converter **51** is attached to the first conductive type semiconductor layer **25**. The growth substrate **21** may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

[0088] Then, the exposed surface of the first conductive type semiconductor layer **25** is subjected to anisotropic etching such as photoelectrochemical (PEC) etching to form a roughened surface on the exposed first conductive type semiconductor layer **25**.

[0089] Meanwhile, the wavelength converter such as a phosphor sheet containing phosphors may be attached to the first conductive type semiconductor layer **25**.

[0090] Alternatively, the growth substrate **21** may contain an impurity for converting a wavelength of light generated in the active layer **27**. In this case, the growth substrate **21** may be used as the wavelength converter **51**.

[0091] Then, the LED package structure is divided into individual packages along the chip separation region **30b**, thereby providing finished LED packages **100**. At this time, the second insulation layer **37** is cut together with the wavelength converter **51** so that cut planes thereof can be formed in a line.

[0092] FIG. 13 is a sectional view showing a method of fabricating the LED package **200** according to the second exemplary embodiment of the present invention.

[0093] Referring to FIG. 13, in the method of fabricating the LED package **200** according to the present exemplary embodiment, the processes until the first and second electrode pads **39a**, **39b** are formed are the same as those of the method of fabricating the LED package **100** described above (FIGS. 10 (a) and (b)).

[0094] After the first and second electrode pads **39a**, **39b** are formed, an insulation layer **49** is formed to cover the first and second electrode pads **39a**, **39b**. The insulation layer **49** may cover side surfaces of the first and second electrode pads **39a**, **39b** to protect the first and second electrode pads **39a**, **39b**. The insulation layer **49** has openings which expose the first and second electrode pads **39a**, **39b**. Additional metal layers **67a**, **67b** are then formed in the openings. The additional metal layers **67a**, **67b** may be composed of a bonding metal.

[0095] The substrate **61** is bonded to the first and second electrode pads **39a**, **39b**. The substrate **61** may have through-holes, in which the first and second bumps **65a**, **65b** may be formed. Further, the first and second bumps may be formed at distal ends thereof with pads **69a**, **69b**. The substrate **61** having the first and second bumps **65a**, **65b** and the pads **69a**, **69b** may be separately prepared and bonded to a wafer having the first and second electrode pads **39a**, **39b**.

[0096] Then, as described with reference to FIG. 12, the growth substrate **21** is removed and a wavelength

converter **51** may be attached to the first conductive type semiconductor layer **25**, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages **200** as described in FIG. 2 are provided.

[0097] FIG. 14 is a sectional view of an LED package **300** according to a third exemplary embodiment of the present invention.

[0098] Referring to FIG. 14, the LED package **300** may include a semiconductor stack **130**, which is divided into a plurality of light emitting cells (only two light emitting cells **S1**, **S2** are shown herein), a first contact layer **135**, a second contact layer **131**, a first insulation layer **133**, a second insulation layer **137**, a first electrode pad **139a**, a second electrode pad **139b**, a connector **139c** connecting adjacent light emitting cells to each other in series, a first bump **145a** and a second bump **145b**. Further, the LED package **300** may include a third insulation layer **141**, an insulation layer **143**, a dummy bump **145c**, a wavelength converter **151**, and additional metal layers **140a**, **140b**.

[0099] The semiconductor stack **130** includes a first conductive type upper semiconductor layer **125**, an active layer **127**, and a second conductive type lower semiconductor layer **129**. The semiconductor stack **130** of the present exemplary embodiment is similar to the semiconductor stack **30** described in FIG. 1, and a detailed description thereof will be omitted herein.

[0100] Each of the light emitting cells **S1**, **S2** has a plurality of contact holes **130a** (see FIG. 18(b)) extending through the second conductive type lower semiconductor layer **129** and the active layer **127** to expose the first conductive type upper semiconductor layer, and the first contact layer **135** contacts the first conductive type upper semiconductor layer **125** exposed in the plurality of contact holes. The light emitting cells **S1**, **S2** are separated from each other by a cell separation region **130b** (see FIG. 18(b)).

[0101] The second contact layer **131** contacts the second conductive type lower semiconductor layer **129** of each of the light emitting cells **S1**, **S2**. The second contact layer **131** includes a reflective metal layer to reflect light generated in the active layer **127**. Further, the second contact layer **131** may form an ohmic contact with the second conductive type lower semiconductor layer **129**.

[0102] The first insulation layer **133** covers the second contact layer **131**. Further, the first insulation layer **133** covers a sidewall of the semiconductor stack **130** exposed in the plurality of contact holes **130a**. In addition, the first insulation layer **133** may cover a side surface of each of the light emitting cells **S1**, **S2**. The first insulation layer **133** insulates the first contact layer **135** from the second contact layer **131** while insulating the second conductive type lower semiconductor layer **129** and the active layer **127** exposed in the plurality of contact holes **130a** from the first contact layer **135**. The first insulation layer **133** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Furthermore, the first insulation layer **133** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$.

[0103] The first contact layer **135** is located under the first insulation layer **133** and contacts the first conductive type upper semiconductor layer **125** through the first insulation layer **133** in the plurality of contact holes **130a** in each of the light emitting cells **S1**, **S2**. The first contact layer **135** includes contact sections **135a** contacting the first conductive type upper semiconductor layer **125**, and a connecting section **135b** connecting the contact sections **135a** to each other. Therefore, the contact sections **135a** are electrically connected to each other by the connecting section **135b**. The first contact layers **135** located under the respective light emitting cells **S1**, **S2** are separated from each other and formed under some regions of the first insulation layer **133**. The first contact layer **135** may be composed of a reflective metal layer.

[0104] The second insulation layer **137** covers the first contact layer **135** under the first contact layer **135**. In addition, the second insulation layer **137** may cover the first insulation layer **133** while covering the side surface of each of the light emitting cells **S1**, **S2**. The second insulation layer **137** may be composed of a single layer or multiple layers. Alternatively, the second insulation layer **37** may be composed of a distributed Bragg reflector.

[0105] The first electrode pad **139a** and the second electrode pad **139b** are located under the second insulation layer **137**. The first electrode pad **139a** may be connected to the first contact layer **135** of a first light emitting cell **S1** through the second insulation layer **137**. Further, the second electrode pad **139b** may be connected to the second contact layer **31** of a second light emitting cell **S2** through the second insulation layer **137** and the first insulation layer **133**.

[0106]The connector **139c** is located under the second insulation layer **137** and electrically connects two adjacent light emitting cells **S1**, **S2** to each other through the second insulation layer **137**. The connector **139c** may connect the second contact layer **131** of one light emitting cell **S1** to the first contact layer **135** of another light emitting cell **S2** adjacent thereto, so that the two light emitting cells **S1**, **S2** are connected in series to each other.

[0107]In the present exemplary embodiment, two light emitting cells **S1**, **S2** are illustrated. However, it should be understood that two or more light emitting cells may be connected in series to each other by a plurality of connectors **139c**. Here, the first and second electrode pads **139a**, **139b** may be connected in series to the light emitting cells **S1**, **S2** located at opposite ends of such series array.

[0108]Meanwhile, the third insulation layer **141** may cover the first electrode pad **139a**, the second electrode pad **139b** and the connector **139c** under the first electrode pad **139a**, the second electrode pad **139b** and the connector **139c**. The third insulation layer **141** may have an opening exposing the first electrode pad **139a** and the second electrode pad **139b**. The third insulation layer **141** may be formed of a silicon oxide or silicon nitride film.

[0109]The first bump **145a** and the second bump **145b** are located under the first and second electrode pads **139a**, **139b**, respectively. The first and second bumps **145a**, **145b** may be formed by plating. The first and second bumps **145a**, **145b** are terminals electrically connected to a circuit board such as an MC-PCB and have distal ends coplanar with each other. In addition, the first electrode pad **139a** may be formed at the same level as that of the second electrode pad **139b**, so that the first bump **145a** and the second bump **145b** may also be formed on the same plane. Therefore, the first and second bumps **145a**, **145b** may have the same height.

[0110]The additional metal layers **140a**, **140b** may be interposed between the first bump **145a** and the first electrode pad **139a** and between the second bump **145b** and the second electrode pad **139b**. Here, the additional metal layers **140a**, **140b** are provided to form the first and second electrode pads **139a**, **139b** to be higher than the connector **139c** and may be located inside openings of the third insulation layer **141**. The first and second electrode pads **139a**, **139b** and the additional metal layers **140a**, **140b** may constitute final electrode pads.

[0111]Meanwhile, the dummy bump **145c** may be located between the first bump **145a** and the second bump **145b**. The dummy bump **145c** may be formed together with the first and second bump **145a**, **145b** to provide a heat passage for discharging heat from the light emitting cells **S1**, **S2**. The dummy bump **145c** is separated from the connector **139c** by the third insulation layer **141**.

[0112]The insulation layer **143** may cover side surfaces of the first and second bumps **145a**, **145b**. The insulation layer **143** may also cover a side surface of the dummy bump **145c**. In addition, the insulation layer **143** fills spaces between the first bump **145a**, the second bump **145b** and the dummy bump **145c** to prevent moisture from entering the semiconductor stack **130** from outside. Although the insulation layer **143** may be configured to cover the overall side surfaces of the first and second bumps **145a**, **145b**, the invention is not limited thereto. Alternatively, the insulation layer **143** may cover the side surfaces of the first and second bumps **145a**, **145b** except for some regions of the side surface near distal ends of the first and second bumps.

[0113]The wavelength converter **151** may be located on the light emitting cells **S1**, **S2**. The wavelength converter **151** may contact an upper surface of the first conductive type upper semiconductor layer **125**. The wavelength converter **151** also covers a cell separation region **130b** and a chip separation region. The wavelength converter **151** may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength converter **151** may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength conversion.

[0114]In the present embodiment, the side surfaces of the light emitting cells **S1**, **S2** are covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer **133** and/or the second insulation layer **137**. In addition, the first contact layer **135** may be covered with the second insulation layer **137** to be protected from external environment and the second contact layer **131** may be covered with the first insulation layer **133** and the second insulation layer **137** to be protected from external environment. Further, the first and second electrode pads **139a**, **139b** are also protected by, for example, the third insulation layer **141**. Accordingly, it is possible to prevent deterioration of the light emitting cells **S1**, **S2** due to moisture.

[0115] The wavelength convertor **151** may be attached to the first conductive type upper semiconductor layer **125** at a wafer-level, and then divided together with the protective insulation layer during a chip separation process (or package separation process). Therefore, a side surface of the wavelength convertor **151** may be in a line with the protective insulation layer. Further, the side surface of the wavelength convertor **151** may be in a line with a side surface of the insulation layer **143**.

[0116] FIG. 15 is a schematic sectional view of a light emitting diode package **400** according to a fourth exemplary embodiment of the present invention.

[0117] Referring to FIG. 15, the LED package **400** is similar to the LED package **300** according to the above exemplary embodiment. In present exemplary embodiment, however, first and second bumps **165a**, **165b** are formed in a substrate **161**.

[0118] Specifically, the substrate **161** includes through-holes, which have the first and second bumps **165a**, **165b** formed therein, respectively. The substrate **161** is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto.

[0119] The substrate **161** having the first and second bumps **165a**, **165b** may be attached to a third insulation layer **141**, and the first and second bumps **165a**, **165b** may be connected to first and second electrode pads **139a**, **139b**, respectively. Here, the first and second bumps **165a**, **165b** may be bonded to additional metal layers **140a**, **140b**, respectively.

[0120] FIG. 16 is a sectional view of a light emitting diode module including the LED packages **300** according to the third exemplary embodiment on a circuit board.

[0121] Referring to FIG. 16, the LED module includes a circuit board **171**, for example, an MC-PCB, the LED package **300**, and a lens **181**. The circuit board **171**, for example, the MC-PCB, has connection pads **173a**, **173b** for mounting the LED packages **300** thereon. The first and second bumps **145a**, **145b** (see FIG. 14) of the LED package **300** are connected to the connection pads **73a**, **73b**, respectively.

[0122] A plurality of LED packages **300** may be mounted on the circuit board **171** and the lens **181** may be disposed on the LED packages **300** to adjust an orientation angle of light emitted from the LED packages **300**.

[0123] In other exemplary embodiments, instead of the LED packages **300**, the light emitting diode packages **400** may be mounted on the circuit board.

[0124] FIG. 17 to FIG. 25 show a method of fabricating the LED package **300** according to the third exemplary embodiment. In FIG. 18 to FIG. 23, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

[0125] Referring to FIG. 17, a semiconductor stack **130**, which includes a first conductive type semiconductor layer **125**, an active layer **127** and a second conductive type semiconductor layer **129**, is formed on a growth substrate **121**. The growth substrate **121** and the semiconductor stack **130** are similar to the substrate **21** and the semiconductor stack **30** described with reference to FIG. 4, and a detailed description thereof will thus be omitted herein.

[0126] Referring to (a) and (b) of FIG. 18, the semiconductor stack **130** is patterned to form a chip (package) separation region **130c** and a cell separation region **130b** while patterning the second conductive type semiconductor layer **129** and the active layer **127** to form light emitting cells **S1**, **S2**, each having a plurality of contact holes **130a** exposing the first conductive type semiconductor layer **125**. The semiconductor stack **130** may be patterned by photolithography and etching processes.

[0127] The chip separation region **130c** is a region for dividing the LED package structure into individual LED packages and side surfaces of the first conductive type semiconductor layer **125**, the active layer **127** and the second conductive type semiconductor layer **129** are exposed at the chip separation region **130c**. Advantageously, the chip separation region **130c** and the cell separation region **130b** may be configured to expose the substrate **121** without being limited thereto.

[0128] The plurality of contact holes **130a** may have a circular shape, but is not limited thereto. The contact holes **130** may have a variety of shapes. The second conductive type semiconductor layer **129** and the active layer **127** are exposed to sidewalls of the plurality of contact holes **130a**. The contact holes **130a** may have slanted

sidewalls.

[0129] Referring to (a) and (b) of FIG. 19, a second contact layer **131** is formed on the second conductive type semiconductor layer **129**. The second contact layer **131** is formed on the semiconductor stack **130** in each of the light emitting cells **S1**, **S2** except for regions corresponding to the plurality of contact holes **130a**.

[0130] The second contact layer **131** may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al). The second contact layer **131** may be composed of a single layer or multiple layers. The second contact layer **131** may also be configured to form an ohmic contact with the second conductive type semiconductor layer **129**.

[0131] The second contact layer **131** may be formed before or after the formation of the plurality of contact holes **130a**.

[0132] Referring to (a) and (b) of FIG. 20, a first insulation layer **133** is formed to cover the second contact layer **131**. The first insulation layer **133** may cover the side surface of each of the light emitting cells **S1**, **S2** while covering the sidewalls of the plurality of contact holes **130a**. Here, the first insulation layer **133** may have openings **133a**, which expose the first conductive type semiconductor layer **125** in the plurality of contact holes **130a**.

[0133] The first insulation layer **133** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. In addition, the first insulation layer **133** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction. For example, the first insulation layer **133** may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_{(2)}\text{O}_{(5)}$. Further, the first insulation layer **133** may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

[0134] Referring to (a) and (b) of FIG. 21, a first contact layer **135** is formed on the first insulation layer **133**. The first contact layer **135** is formed on each of the light emitting cells **S1**, **S2**, and includes contact sections **35a** contacting the first conductive type upper semiconductor layer **125** exposed in the contact holes **130a** and a connecting section **135b** connecting the contact sections **135a** to each other. The first contact layer **135** may be composed of a reflective metal layer, but is not limited thereto.

[0135] The first contact layer **135** is formed on some regions of each of the light emitting cells **S1**, **S2**, so that the first insulation layer **133** is exposed at other regions of the semiconductor stack **130** where the first contact layer **135** is not formed.

[0136] Referring to (a) and (b) of FIG. 22, a second insulation layer **137** is formed on the first contact layer **135**. The second insulation layer **137** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the second insulation layer **137** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

[0137] The second insulation layer **137** may cover the first contact layer **135** while covering the first insulation layer **133**. The second insulation layer **137** may also cover the side surface of each of the light emitting cells **S1**, **S2**. In addition, the second insulation layer **137** may fill in the chip separation region **130c** and the cell separation region **130b**.

[0138] The second insulation layer **137** has an opening **137a** which exposes the first contact layer **135** of each of the light emitting cells **S1**, **S2**. Further, the second insulation layer **137** and the first insulation layer **133** are formed with an opening **137b**, which exposes the second contact layer **131**.

[0139] Referring to (a) and (b) of FIG. 23, a connector **139c** and first and second electrode pads **139a**, **139b** are formed on the second insulation layer **137**. The first electrode pad **139a** is connected to the first contact layer **135** of a first light emitting cell **S1** through the opening **137a** and the second electrode pad **139b** is connected to the second contact layer **131** of a second light emitting cell **S2** through the opening **137b**. Further, the connector **139c** connects the first contact layer **135** and the second contact layer **131** of adjacent light emitting cells **S1**, **S2** to each other in series through the openings **137a**, **137b**.

[0140] Referring to FIG. 24, a third insulation layer **141** is formed on the first and second electrode pads **139a**,

139b and the connector **139c**. The third insulation layer **141** covers the first and second electrode pads **139a**, **139b** and the connector **139c**, and has grooves which expose upper surfaces of the electrode pads **139a**, **139b**. Meanwhile, the third insulation layer **141** may have additional metal layers **140a**, **140b** formed in the grooves thereof. The additional metal layers **140a**, **140b** increase the height of the electrode pads **139a**, **139b**, such that final electrode pads may have a greater height than the connector **139c**. The additional metal layers **140a**, **140b** may be formed before the formation of the third insulation layer **141**. Upper surfaces of the additional metal layers **140a**, **140b** may be substantially coplanar with an upper surface of the third insulation layer **141**.

[0141] Referring to FIG. 25, a patterned insulation layer **143** is formed on the third insulation layer **141**. The patterned insulation layer **143** has grooves, which expose the upper side of the first and second electrode pads **139a**, **139b**, for example, the additional metal layers **140a**, **140b**. Further, the patterned insulation layer **143** may have a groove exposing the third insulation layer **141** between the first electrode pad **139a** and the second electrode pad **139b**.

[0142] Then, first and second bumps **145a**, **145b** are formed in the grooves of the insulation layer **143** and a dummy bump **145c** may be formed between the first and second bumps.

[0143] The bumps may be formed by plating, for example, electroplating. As needed, a seed layer for plating may also be formed.

[0144] After the first and second bumps **145a**, **145b** are formed, the insulation layer **143** may be removed. For example, the insulation layer **143** may be formed of a polymer such as photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer **143** may remain to protect the side surfaces of the first and second bumps **145a**, **145b**.

[0145] Referring to FIG. 26, the growth substrate **121** is removed and a wavelength convertor **151** is attached to the light emitting cells **S1**, **S2**. The growth substrate **21** may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

[0146] Then, the exposed surface of the first conductive type semiconductor layer **125** is subjected to anisotropic etching such as PEC etching to form a roughened surface on the exposed first conductive type semiconductor layer **125**.

[0147] Meanwhile, the wavelength convertor **151**, such as a phosphor sheet containing phosphors, may be attached to the first conductive type semiconductor layer **125**.

[0148] Alternatively, the growth substrate **121** may contain an impurity for converting a wavelength of light generated in the active layer **127**. In this case, the growth substrate **121** may be used as the wavelength convertor **151**.

[0149] Then, the LED package structure is divided into individual packages along the chip separation region **130c**, thereby providing finished LED packages **300**. At this time, the second insulation layer **137** is cut together with the wavelength convertor **151** so that cut planes thereof can be formed in a line.

[0150] FIG. 27 is a sectional view explaining a method of fabricating the LED package **400** according to the fourth exemplary embodiment of the invention.

[0151] Referring to FIG. 27, in the method of fabricating the LED package **400** according to this embodiment, the processes until the third insulation layer **141** and the additional metal layers **140a**, **140b** are formed are the same as those of the method of fabricating the LED package **300** described above (FIG. 24).

[0152] In the present exemplary embodiment, the substrate **161** is bonded to the third insulation layer **141**. The substrate **161** may have through-holes, in which the first and second bumps **165a**, **165b** may be formed. Further, the first and second bumps **165a**, **165b** may be formed at distal ends thereof with pads (not shown). In addition, the substrate **161** may have grooves partially formed on a lower surface thereof and filled with a metallic material **165c**. The metallic material **165c** improves substrate heat dissipation.

[0153] Alternatively, the substrate **161** having the first and second bumps **165a**, **165b** may be separately prepared and bonded to a wafer having the first and second electrode pads **139a**, **139b**. The first and second bumps **165a**, **165b** may be electrically connected to first and second electrode pads **139a**, **139b**, respectively.

[0154] Then, as described with reference to FIG. 26, the growth substrate **121** is removed and the wavelength converter **151** may be attached to the light emitting cells **S1**, **S2**, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages **400** as described in FIG. 15 are provided.

[0155] As such, the exemplary embodiments of the invention provide wafer-level LED packages which can be directly formed on a circuit board for a module without using a conventional lead frame or printed circuit board. Accordingly, the LED package may have high efficiency and exhibit improved heat dissipation while reducing time and cost for fabrication of the LED package. In addition, an LED module having the LED package mounted thereon may have high efficiency and exhibit improved heat dissipation.

[0156] Further, the LED package may include a plurality of light emitting cells connected in series to each other and arrays connected in reverse parallel to each other. Further, the plurality of light emitting cells may be connected to a bridge rectifier and may be used to form a bridge rectifier. Therefore, the LED module including the LED package may be operated by AC power without a separate AC/DC converter.

[0157] Although the invention has been illustrated with reference to some exemplary embodiments in conjunction with the drawings, it will be apparent to those skilled in the art that various modifications and changes can be made to the invention without departing from the spirit and scope of the invention. Further, it should be understood that some features of a certain embodiment may also be applied to other embodiment without departing from the spirit and scope of the invention. Therefore, it should be understood that the embodiments are provided by way of illustration only and are given to provide complete disclosure of the invention and to provide thorough understanding of the invention to those skilled in the art. Thus, it is intended that the invention covers the modifications and variations provided they fall within the scope of the appended claims and their equivalents.

ENGLISH-CLAIMS:

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What is claimed is:

1. A light emitting diode (LED) package, comprising:

- -
a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;
- -
a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;
- -
a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes;
- -
a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and
- -
a protective insulation layer covering a sidewall of the semiconductor stack.

2. The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.

3. The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped single crystal substrate.

4. The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.
5. The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.
7. The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.
11. The LED package of claim 1, further comprising:
 - -
a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and
 - -
a second contact layer contacting the second conductive type semiconductor layer,
 - -
wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer,
 - -
wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.
12. The LED package of claim 11, further comprising:
 - -
a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and
 - -
a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer,
 - -
wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.

13. The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.

14. A light emitting diode (LED) module, comprising:

- -
a circuit board;
- -
the LED package of claim 1 arranged on the circuit board; and
- -
a lens to adjust an orientation angle of light emitted from the LED package.

15. The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.

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ALEXANDRIA, Va., July 1 -- United States Patent no. **9,070,851**, issued on June 30, was assigned to Seoul Semiconductor Co. Ltd. (Ansan- ...
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2. US Official News, July 1, 2015 Wednesday, 256 words, US Patent granted to Seoul Semiconductor Co., Ltd. (KR) on June 30, 2015 titled as "Wafer-level light emitting diode package and method of fabricating the same", ALEXANDRIA, Va

United States Patent and Trademark Office has granted patent no. **9,070,851**, on June 30, 2015, to Seoul Semiconductor Co., Ltd. (KR), titled as " ...

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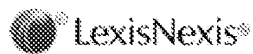
... Patent News Patent Application Number: 13/194,317 Patent Publication Number: **9,070,851**
International Patent Classification Codes: H01L 33/62 (20130101), H01L 27/ ...

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June 30, 2015

Wafer-level light emitting diode package and method of fabricating the same

INVENTOR: Seo, Won Cheol - Ansan-si, Republic of Korea (KR) ; Kal, Dae Sung - Ansan-si, Republic of Korea (KR)**APPL-NO:** 194317 (13)**FILED-DATE:** July 29, 2011**GRANTED-DATE:** June 30, 2015**PRIORITY:** September 24, 2010 - 1020100092807, Republic of Korea (KR) ; September 24, 2010 - 1020100092808, Republic of Korea (KR)**ASSIGNEE-PRE-ISSUE:**

August 2, 2011 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., SEOUL SEMICONDUCTOR CO., LTD., 148-29, GASAN-DONG, GEUMCHEON-GU, SEOUL, KOREA, REPUBLIC OF (), 158-801, Reel and Frame Number: 026688/0805

ASSIGNEE-AT-ISSUE:

Seoul Semiconductor Co., Ltd., Ansan-si, Republic of Korea (KR), Foreign company or corporation (03)

LEGAL-REP: H.C. Park & Associates, PLC**PUB-TYPE:** June 30, 2015 - Patent with a pre-grant publication (B2)**PUB-COUNTRY:** United States of America (US)**LEGAL-STATUS:**

August 2, 2011 - ASSIGNMENT

January 15, 2016 - Payor Number Assigned.

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REL-DATA:

Prior Publication 20120074441, March 29, 2012

US-MAIN-CL: 1#1

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IPC-MAIN-CL: [8] H01L 033#60 (20100101) Advanced Inventive 20150630 (A F I B H US)

IPC-ADDL-CL: [8] H01L 027#15 (20060101) Advanced Inventive 20150630 (A L I B H US)

IPC-ADDL-CL: [8] H01L 033#00 (20100101) Advanced Non-Inventive 20150630 (A L N B H US)

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PRIM-EXMR: Nguyen, Cuong Q

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US Fed News

July 1, 2015 Wednesday 10:32 AM EST

LENGTH: 298 words

HEADLINE: US Patent Issued to Seoul Semiconductor on June 30 for "Wafer-level light emitting diode package and method of fabricating the same" (South Korean Inventors)

DATELINE: ALEXANDRIA, Va.**BODY:**

ALEXANDRIA, Va., July 1 -- United States Patent no. **9,070,851**, issued on June 30, was assigned to Seoul Semiconductor Co. Ltd. ↙(Ansan-si, South Korea).

"Wafer-level light emitting diode package and method of fabricating the same" was invented by Won Cheol Seo (Ansan-si, South Korea) and Dae Sung Kal (Ansan-si, South Korea). According to the abstract* released by the U.S. Patent & Trademark Office: "Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack." The patent was filed on July 29, 2011, under Application No. 13/194,317. *For further information, including images, charts and tables, please visit: <http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=1&u=%2Fnetacgi%2FPTO%2Fsearch-bool.html&r=1&f=G&l=50&co1=AND&d=PTXT&s1=9070851&OS=9070851&RS=9070851> For any query with respect to this article or any other content requirement, please contact Editor at htsyndication@hindustantimes.com

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REEXAM CONTROL NUMBER	FILING OR 371 (c) DATE	PATENT NUMBER
90/013,725	04/15/2016	9070851

58027
H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

**CONFIRMATION NO. 7313
REEXAM ASSIGNMENT NOTICE**



Date Mailed: 04/22/2016

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cc: Third Party Requester(if any)
ALAN TABOADA - MOSER TABOADA
1030 BROAD STREET, SUITE 203
SHREWSBURY, NJ 07702

/rswalker/

Legal Instruments Examiner
Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900



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90/013,725	04/15/2016	9070851

ALAN TABOADA - MOSER TABOADA
1030 BROAD STREET, SUITE 203
SHREWSBURY, NJ 07702

**CONFIRMATION NO. 7313
REEXAMINATION REQUEST
NOTICE**



Date Mailed: 04/22/2016

NOTICE OF REEXAMINATION REQUEST FILING DATE

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Legal Instruments Examiner
Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900

Patent Assignment Abstract of Title

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Filing Dt: 07/29/2011

Patent #: 9070851

Issue Dt: 06/30/2015

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Intl Reg #:

Publication #: US20120074441

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Inventors: Won Cheol SEO, Dae Sung KAL

Title: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

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Assignors: SEO, WON CHEOL

Exec Dt: 08/02/2011

KAL, DAE SUNG

Exec Dt: 08/02/2011

Assignee: SEOUL SEMICONDUCTOR CO., LTD.

148-29, GASAN-DONG, GEUMCHEON-GU

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Correspondent: H.C. PARK & ASSOCIATES, PLC

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STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 1

Complete if Known

Application Number	13/194,317
Filing Date	July 29, 2011
First Named Inventor	Won Cheol Seo
Art Unit	
Examiner Name	
Attorney Docket Number	MT100

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 7,179,670-B2	2007-02-20	GELcore, LLC	
		US- 8,368,100-B2	2013-02-05	Cree, Inc.	
		US- 7,564,887-B2	2009-07-21	Finisar Corporation	
		US- 6,657,236-B1	2003-12-02	Cree Lighting Company	
		US- 7,335,517-B2	2008-02-26	Kabushiki Kaisha Toshiba	
		US- 6,838,702-B1	2005-01-04	Lambda Opto Technology Co., Ltd.	
		US- 2009/0140272-A1	2009-06-04	Goldeneye, Inc.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		JP-4151284-b	2008-07-11	Nichia Chem Ind. Ltd.		
		JP-2002-319704-A	2002-10-31	Matsushita Electric Works		
		KR-610650-B1	2006-08-09	FIONIX Inc.		
		JP-11-008414-A	1999-01-12	Sony Corp.		

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SignatureDate
Considered

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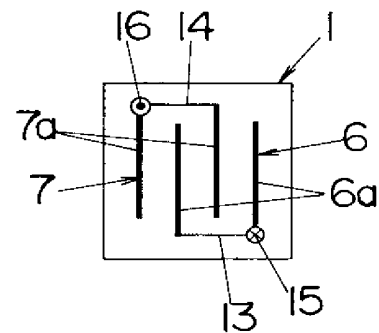
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(54) 【発明の名称】 L E Dチップ

(57) 【要約】

【課題】 発光面内の輝度むらを減少させて輝度の均一性を向上させた L E Dチップを提供する。

【解決手段】 基板上に p 形半導体層および n 形半導体層を形成し、p 形半導体層および n 形半導体層において基板の反対側である L E Dチップ 1 の主チップ面にそれぞれ p 側電極 6 および n 側電極 7 を設ける。主チップ面内において p 側電極 6 および n 側電極 7 はそれぞれ並行する直線部 6 a, 7 a を有し、直線部 6 a, 7 a を横切る方向では p 側電極 6 と n 側電極 7 とが交互に配列される。このような配置により、p 側電極 6 と n 側電極 7 との対向部位が多くなるから、電流密度の分布の偏りが小さくなり、輝度むらの少ない L E Dチップ 1 が得られる。



1 L E Dチップ
6 p 側電極
6 a 直線部
7 n 側電極
7 a 直線部

【特許請求の範囲】

【請求項 1】 基板上に形成された p 形半導体層および n 形半導体層と、p 形半導体層および n 形半導体層において基板の反対側である主チップ面にそれぞれ接続された p 側電極および n 側電極とを備え、前記主チップ面内において p 側電極および n 側電極の少なくとも一部がそれぞれ互いに並行配置され、p 側電極および n 側電極において並行配置された部位を横切る方向では p 側電極と n 側電極とが交互に配列されていることを特徴とする LED チップ。

【請求項 2】 前記 p 側電極および前記 n 側電極において、並行配置された部位が等間隔になるように配列されていることを特徴とする請求項 1 記載の LED チップ。

【請求項 3】 前記 p 側電極と前記 n 側電極との少なくとも一方については、並行配置された部位が主チップ面上では電氣的に接続されていないことを特徴とする請求項 1 記載の LED チップ。

【請求項 4】 前記 p 側電極および前記 n 側電極において、並行配置された部位を横切る方向にそれぞれ分岐しあつ互いに並行する複数の枝部が形成されていることを特徴とする請求項 1 記載の LED チップ。

【請求項 5】 前記主チップ面内において複数の p 側電極および n 側電極の少なくとも一部がそれぞれ互いに並行配置される渦巻き状に延長され、渦巻き状に形成される部位の中心から外側に向かって p 側電極および n 側電極を横切る方向では p 側電極と n 側電極とが交互に配列されていることを特徴とする請求項 1 記載の LED チップ。

【請求項 6】 基板上に形成された p 形半導体層および n 形半導体層と、p 形半導体層および n 形半導体層において基板の反対側である主チップ面にそれぞれ接続された複数個ずつの p 側電極および n 側電極とを備えることを特徴とする LED チップ。

【請求項 7】 前記 p 側電極および前記 n 側電極のうち異種導電形の半導体層に接続された電極間の距離を、同種導電形の半導体層に接続された電極間の距離よりも小さくしたことを特徴とする請求項 6 記載の LED チップ。

【請求項 8】 前記 p 側電極と前記 n 側電極のうち異種導電形の半導体層に接続された電極間が等間隔に配列されていることを特徴とする請求項 7 記載の LED チップ。

【請求項 9】 基板上に形成された p 形半導体層および n 形半導体層と、p 形半導体層および n 形半導体層において基板の反対側である主チップ面にそれぞれ接続された p 側電極および n 側電極とを備え、前記主チップ面が p 側電極および n 側電極との一方により複数の領域に分割され、各領域内にそれぞれ他方が配置されることを特徴とする LED チップ。

【請求項 10】 前記 p 側電極と前記 n 側電極とのうち

の前記一方が前記各領域をそれぞれ全周に亘って囲むように形成されることを特徴とする請求項 9 記載の LED チップ。

【請求項 11】 前記 p 側電極と前記 n 側電極とのうちの前記他方が前記一方に設けた線状部分に並行配置される線状の部分を備えることを特徴とする請求項 9 記載の LED チップ。

【請求項 12】 基板上に形成された p 形半導体層および n 形半導体層と、p 形半導体層および n 形半導体層において基板の反対側である主チップ面にそれぞれ接続された p 側電極および n 側電極とを備え、p 側電極および n 側電極との一方が主チップ面の中心部に配置され、前記一方の周囲を囲む形で他方が配置されていることを特徴とする LED チップ。

【請求項 13】 前記 p 側電極と前記 n 側電極とが交互に入れ子状に配列されていることを特徴とする請求項 12 記載の LED チップ。

【請求項 14】 前記 p 側電極と前記 n 側電極とが等間隔になるように配列されていることを特徴とする請求項 13 記載の LED チップ。

【請求項 15】 前記 p 側電極と前記 n 側電極とが同心円状に配列されていることを特徴とする請求項 13 または請求項 14 記載の LED チップ。

【請求項 16】 前記 p 側電極と前記 n 側電極とが主チップ面の外周形状の相似形状であることを特徴とする請求項 13 または請求項 14 記載の LED チップ。

【請求項 17】 前記 n 側電極と前記 p 側電極との配置パターンが、前記主チップ面内で線対称性を有することを特徴とする請求項 1 または請求項 6 または請求項 9 または請求項 12 記載の LED チップ。

【請求項 18】 前記 n 側電極と前記 p 側電極との配置パターンが、前記主チップ面内で 2 回以上の回転対称性を有することを特徴とする請求項 1 または請求項 6 または請求項 9 または請求項 12 記載の LED チップ。

【請求項 19】 前記 n 側電極と前記 p 側電極との配置パターンが、前記主チップ面内で 2 回以上の回転対称性を有するとともに、2 本以上の対称線に関して線対称性を有することを特徴とする請求項 1 または請求項 6 または請求項 9 または請求項 12 記載の LED チップ。

【請求項 20】 前記 n 側電極と前記 p 側電極とにそれぞれ給電する給電部を設け、n 側電極と p 側電極との少なくとも一方の給電部を複数個設けたことを特徴とする請求項 1 または請求項 6 または請求項 9 記載の LED チップ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、基板上に p 形半導体層と n 形半導体層とが形成され、p 形半導体層および n 形半導体層における基板の反対側である主チップ面において、p 形半導体層および n 形半導体層にそれぞれ p

側電極およびn側電極が接続されたLEDチップに関するものである。

【0002】

【従来の技術】従来から、図25に示すように、サファイアの基板2の上に導電形がn形である窒化ガリウムからなるn形半導体層3を介して、導電形がp形である窒化ガリウムからなるp形半導体層5を積層した構造のLEDチップ1が提供されている。図示するLEDチップ1ではn形半導体層3に接続されるn側電極7とp形半導体層5に接続されるp側電極6とを基板2の両側部に配置してある。

【0003】このように構成されたLEDチップ2はp側電極6およびn側電極7を設けている主チップ面を光取出側とするフェースアップ状態で実装するときには、p側電極6とn側電極7とにそれぞれボンディングワイヤを介して給電する形で使用する。

【0004】また、基板2はサファイアからなり透光性を有するから、図26に示すように基板2を光取出側とするフェースダウン状態での実装も可能であって、この場合にはp側電極6およびn側電極7をバンプ構造として実装基板8に設けた導電体10にp側電極6およびn側電極7を電氣的に接続するようにフリップチップ実装が施される。このような実装形式を採用するときにはLEDチップ1と実装基板8との間に充填材11が充填される。

【0005】

【発明が解決しようとする課題】ところで、上述した従来構成のLEDチップ1ではp側電極6とn側電極7とが点状に1個ずつ設けられたものであり、LEDチップ1の発光面（光取出面）においてp側電極6とn側電極7との間では輝度が高いものの、それ以外の部位では輝度が低いという観察結果が得られている。これは、p側電極6とn側電極7との間では電流密度が十分に大きいのがp側電極6とn側電極7との間から離れると電流密度が急速に小さくなり、電流密度の分布に偏りが生じるからであると考えられる。要するに、LEDチップ1の発光面には輝度むらが生じている。

【0006】一般に提供されているLEDチップ1は発光面が300μm角程度であって、p側電極6とn側電極7との電極面積に対する発光面の面積の比が比較的小さいものであるから、発光面に輝度むらが生じていても通常は実用上で問題になることはない。

【0007】一方、最近では白色LEDを表示器やディスプレイに用いるほか照明用光源として用いることが提案されており、この種の用途に適用するために1チップ当たりの輝度を大きくすることが要求され、結果的にLEDチップの大面積化が要求されている。LEDチップを大面積化すれば、電極面積に対して発光面の面積が従来よりも大きくなるから、発光面内の輝度むらが視覚的に認識されるようになり、照明用光源として使用するに

は問題が生じる。

【0008】本発明は前記事由に鑑みて為されたものであり、その目的は、発光面内の輝度むらを減少させて輝度の均一性を向上させたLEDチップを提供することにある。

【0009】

【課題を解決するための手段】請求項1の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続されたp側電極およびn側電極とを備え、前記主チップ面内においてp側電極およびn側電極の少なくとも一部がそれぞれ互いに並行配置され、p側電極およびn側電極において並行配置された部位を横切る方向ではp側電極とn側電極とが交互に配列されていることを特徴とする。

【0010】請求項2の発明は、請求項1の発明において、前記p側電極および前記n側電極において、並行配置された部位が等間隔になるように配列されていることを特徴とする。

【0011】請求項3の発明は、請求項1の発明において、前記p側電極と前記n側電極との少なくとも一方については、並行配置された部位が主チップ面上では電氣的に接続されていないことを特徴とする。

【0012】請求項4の発明は、請求項1の発明において、前記p側電極および前記n側電極において、並行配置された部位を横切る方向にそれぞれ分岐しかつ互いに並行する複数の枝部が形成されていることを特徴とする。

【0013】請求項5の発明は、請求項1の発明において、前記主チップ面内において複数のp側電極およびn側電極の少なくとも一部がそれぞれ互いに並行配置される渦巻き状に延長され、渦巻き状に形成される部位の中心から外側に向かってp側電極およびn側電極を横切る方向ではp側電極とn側電極とが交互に配列されていることを特徴とする。

【0014】請求項6の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続された複数個ずつのp側電極およびn側電極とを備えることを特徴とする。

【0015】請求項7の発明は、請求項6の発明において、前記p側電極および前記n側電極のうち異種導電形の半導体層に接続された電極間の距離を、同種導電形の半導体層に接続された電極間の距離よりも小さくしたことを特徴とする。

【0016】請求項8の発明は、請求項7の発明において、前記p側電極と前記n側電極のうち異種導電形の半導体層に接続された電極間が等間隔に配列されていることを特徴とする。

【0017】請求項9の発明は、基板上に形成されたp

形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続されたp側電極およびn側電極とを備え、前記主チップ面がp側電極およびn側電極との一方により複数の領域に分割され、各領域内にそれぞれ他方が配置されることを特徴とする。

【0018】請求項10の発明は、請求項9の発明において、前記p側電極と前記n側電極とのうちの前記一方が前記各領域をそれぞれ全周に亘って囲むように形成されることを特徴とする。

【0019】請求項11の発明は、請求項9の発明において、前記p側電極と前記n側電極とのうちの前記他方が前記一方に設けた線状部分に並行配置される線状の部分の備えることを特徴とする。

【0020】請求項12の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続されたp側電極およびn側電極とを備え、p側電極およびn側電極との一方が主チップ面の中心部に配置され、前記一方の周囲を囲む形で他方が配置されていることを特徴とする。

【0021】請求項13の発明は、請求項12の発明において、前記p側電極と前記n側電極とが交互に入れ子状に配列されていることを特徴とする。

【0022】請求項14の発明は、請求項13の発明において、前記p側電極と前記n側電極とが等間隔になるように配列されていることを特徴とする。

【0023】請求項15の発明は、請求項13または請求項14の発明において、前記p側電極と前記n側電極とが同心円状に配列されていることを特徴とする。

【0024】請求項16の発明は、請求項13または請求項14の発明において、前記p側電極と前記n側電極とが主チップ面の外周形状の相似形状であることを特徴とする。

【0025】請求項17の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で線対称性を有することを特徴とする。

【0026】請求項18の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で2回以上の回転対称性を有することを特徴とする。

【0027】請求項19の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で2回以上の回転対称性を有するとともに、2本以上の対称線に関して線対称性を有することを特徴とする。

【0028】請求項20の発明は、請求項1または請求

項6または請求項9の発明において、前記n側電極と前記p側電極とにそれぞれ給電する給電部を設け、n側電極とp側電極との少なくとも一方の給電部を複数個設けたことを特徴とする。

【0029】上述したいずれの構成も、p側電極とn側電極との間で電流の流れる経路が多く形成されるから、発光領域を通過する電流の電流密度の差を従来構成に比較して減少させることができ、発光領域における電流密度の均一化を図ることができる。その結果、従来構成よりも輝度むらを大幅に減少させることができる。なお、LEDチップを実装する態様についてはとくに制限はなく、フェースアップ状態とフェースダウン状態とのいずれの態様においても上述した構成は適用可能である。ただし、p側電極およびn側電極が点状ではない構成を採用する場合に、p側電極およびn側電極が発光面側に存在しないフェースダウン状態で実装するほうが、輝度むらをより低減することが可能である。

【0030】

【発明の実施の形態】以下の各実施形態において説明するLEDチップ1は、図25に示した従来構成と同様に、サファイヤからなる透光性を有する基板2上に、バッファ層（図示せず）、導電形がn形である窒化ガリウム（GaN）層からなるn形半導体層3、クラッド層（図示せず）、発光層4（図23参照）に、クラッド層（図示せず）、導電形がp形である窒化ガリウム（GaN）層からなるp形半導体層5を順に積み重ねた構成を有する。ただし、半導体の種類は上述のような窒化ガリウム系化合物半導体に限定されるものではなく、他の半導体も用いることができる。

【0031】n形半導体層3において基板2とは反対側の面にはn側電極7が形成され、p形半導体層5において基板2とは反対側の面にはp側電極6が形成される。n形半導体層3およびp形半導体層5を含む半導体層において基板1とは反対側の面、すなわちp側電極6およびn側電極7を設けている面を以下では主チップ面と呼ぶ。このLEDチップ1を用いて照明用の光源装置を構成する場合には、図24に示すように、近紫外線により励起されて黄色を発光する蛍光体を分散させた透光性合成樹脂のカバー12内にLEDチップ1を配置すれば、LEDチップ1から発光する青色の光とカバー12内の蛍光体からの黄色の光とを混色させて白色光の光源装置を構成することができる。また、図示例では実装基板8に対してフリップチップ実装を施してフェースダウン状態で実装してある。なお、以下の実施形態においては、LEDチップ1の主チップ面を正方形に形成しているが、主チップ面の形状はこれに限定されるものではない。また、以下に説明する実施形態において、p側電極6とn側電極7とは入れ換え可能である。

【0032】（実施形態1）本実施形態は請求項1、請求項2に対応する。本実施形態では、図1に示すよう

に、p側電極6およびn側電極7がLEDチップ1の主チップ面内において直線部6a、7aを有し、直線部6a、7aが並行配置されるときにも直線部6a、7aにおいてp側電極6およびn側電極7を横切る方向（直交する方向）ではp側電極6とn側電極7とが交互に配列される。また、p側電極6およびn側電極7について図示例では直線部6a、7aを2本ずつ等間隔に設けてあり、同種導電形の半導体層3、5（図23参照）に接続された直線部6a、7a同士は、直線部6a、7aの一端部に設けた導電部13、14によりそれぞれ接続される。つまり、n側電極7の直線部7a間は導電部13により電氣的に接続され、p側電極6の直線部6a間は導電部14により電氣的に接続される。本実施形態ではLEDチップ1の主チップ面の1つの対角線上の角部付近にp側電極6およびn側電極7とそれぞれ電氣的に接続された2つの給電部15、16をアルミニウム蒸着などにより形成してある。つまり、p側電極6とn側電極7とは、それぞれ2本ずつの直線部6a、7aの間の部位に1箇所ずつの給電部15、16を設けてあり、給電部15、16から各直線部6a、7aに分かれて電流が流れるようにしてある。

【0033】しかして、本実施形態のLEDチップ1において給電部15、16に通電して点灯させると、p側電極6およびn側電極7において並行配置された直線部6a、7aの間にそれぞれ発光領域が形成されるから、1個のLEDチップ1内で電流経路を集中させることなく電流を流すことができ、LEDチップ1の発光面の輝度を均一化させることができる。つまり、本実施形態ではp側電極6とn側電極7とが対向する部位が従来構成よりも多く、しかもp側電極6とn側電極7とが等距離になる部位が多いから、電流密度の分布の偏りを低減して輝度の均斉度を高めることができる。

【0034】図1に示した構成ではp側電極6およびn側電極7において並行配置する部位が直線部6a、7aとして形成されていたが、図2に示すように、p側電極6およびn側電極7に蛇行する形状の波形部6b、7bを形成し、波形部6b、7bを並行させるようにしてもよい。あるいはまた、図3に示すように、p側電極6およびn側電極7にL字状に屈曲させた屈曲部6c、7cを形成し、屈曲部6c、7cを並行させるようにしてもよい。図2および図3に示した構成例では、給電部15、16を2本の波形部6b、7bないし屈曲部6c、7cのうちの一方であって導電部13、14から離れた端部に設けてある。いずれの構成においても、給電部15、16の位置はp側電極6とn側電極7との間に流れる電流の電流密度が均一化されるように選択されている。

【0035】（実施形態2）本実施形態は請求項3に対応する。本実施形態では、図4に示すように、p側電極6とn側電極7とがLEDチップ1の主チップ面内にお

いて直線部6a、7aを有し、直線部6a、7aが並行配置されるときにも直線部6a、7aにおいてp側電極6およびn側電極7を横切る方向（直交する方向）ではp側電極6とn側電極7とが交互に配列される。また、p側電極6およびn側電極7について図示例では直線部6a、7aを2本ずつ等間隔に設けてある。ただし、実施形態1とは異なり直線部6a、7aはLEDチップ1内では電氣的に接続されておらず独立している。したがって、給電部15、16は各直線部6a、7aごとに個別に設けてある。また、p側電極6の給電部15を直線部6aの一端側に設けるとすれば、n側電極7の給電部16は直線部7aの他端側に設けるようにしてあり、直線部6a、7aの間で電流が分散して流れるようにしてある。

【0036】本実施形態の構成では、p側電極6およびn側電極7において並行配置されていない部位の割合が実施形態1よりも少なくなる結果、発光領域の電流密度の偏りがより少なくなり、実施形態1の構成よりも輝度の均斉度がさらに高くなる。

【0037】実施形態1と同様に、直線部6a、7aに代えて波形部6a、7aのように曲線状とすることも可能であり、また図5に示すように、L字状に屈曲した屈曲部6c、7cを用いることも可能である。

【0038】（実施形態3）本実施形態は請求項4に対応する。すなわち、図6に示すように、図1に示した実施形態1の構成と同様の構成を有したp側電極6およびn側電極7を設け、さらに直線部6a、7aの直交方向にそれぞれ分岐する複数の枝部6d、7dを設け、枝部6d、7dが互いに並行するように設置してある。本実施形態では、図1に示した実施形態1の構成に比較すると、対向するp側電極6とn側電極7との間の距離が短かく、かつp側電極6およびn側電極7の発光面全体に占める密度が大きいから、LEDチップ1を点灯させたときに発光面全体の輝度が実施形態1の構成よりもさらに均一化される。

【0039】（実施形態4）本実施形態は請求項5に対応する。本実施形態では、図7に示すように、p側電極6とn側電極7とを主チップ面においてそれぞれ渦巻き状に形成してある。図示例ではp側電極6とn側電極7とをともに中心から左回りの渦巻き状として並行配置してあり、中心から外側に向かってp側電極6とn側電極7とを横切る方向ではp側電極6とn側電極7とが交互に配列されるようにしてある。また、給電部15、16は中心側の一端に設けてある。この構成によっても、発光面全体に対してp側電極6とn側電極7とにおける互いに並行していない部分の割合が図1に示した実施形態1よりも少ないから、発光面の輝度をさらに均一化させることが可能になる。ここに、渦巻き状として図7では滑らかな曲線状の渦巻きを例示しているが、図8に示すように直線を連結した形状の渦巻きとしても同様の効果

が得られる。また、図8に示す構成では給電部15、16を渦巻きの外側の端部としてあり、この構成ではチップ面上で給電部15、16が離れて配置されるから電流密度の分布の偏りを低減して発光面の輝度を均斉化しやすくなる。

【0040】（実施形態5）本実施形態は請求項6、請求項7、請求項8に対応する。本実施形態は図9に示すように、主チップ面においてn形半導体層3に複数のn側電極7を設けるとともに、p形半導体層5に複数のp側電極6を設けた構成を有する。図示例ではp側電極6およびn側電極7のうち同種導電形の半導体層に対応する電極間は異種導電形の半導体層に対応する電極間の距離よりも大きくなっている。また、p側電極6およびn側電極7のうち同種導電形の半導体層に対応する電極間は等間隔となるように配列されている。要するに、主チップ面の四隅のうち一方の対角線の両端部にはp側電極6（給電部15と兼用）が配置され、他方の対角線の両端部にはn側電極7（給電部16と兼用）が配置される。この構成により、異種導電形に対応する電極間で等距離になる部分を従来構成よりも増やすことになり、発光面の輝度を均一化することが可能になる。

【0041】図10に示すように、p側電極6とn側電極7とを3個ずつ設ける構成として、主チップ面の四隅に4個の電極を配置するとともに残りの2個の電極を主チップ面の中央部に配置する構成を採用してもよい。つまり、同種導電形の半導体層に対応する各3個の電極を三角形に配置するとともに2個の電極を主チップ面の隣り合う隅部に配置し、残りの1個の電極を主チップ面の中央部に配置しているのであって、異種導電形の半導体層に対応する電極のうちの1つは上述した三角形の中に位置するように配置される。この構成では、異種導電形の半導体層に対応する電極間の電流経路が複数形成されるから、発光面の輝度の均斉度が比較的高くなり、しかも主チップ面の中央付近では異種導電形の半導体層に対応する電極間の距離が他の部位よりも小さいから、発光面の中央付近の輝度が周辺部分よりも高くなる。要するに全体としては発光面の輝度の均一性を保ちながらも、中心付近の輝度を高くすることが可能になる。

【0042】（実施形態6）本実施形態は請求項9に対応する。本実施形態では図11に示すように、n形半導体層3とp形半導体層5にそれぞれ接続されるp側電極6とn側電極7とのうちの一方の電極を直線状に形成し、この電極により主チップ面を2つの領域に分割するとともに、各領域ごとに他方の電極を設けた構成としてある。図示例ではp側電極6を主チップ面の一方の対角線に重なる直線状に形成して主チップ面を2つの領域に分割し、n側電極7を各領域ごとに設けてある。この構成においても従来構成と比較するとp側電極6とn側電極7との間の対向部分が多く形成されるから発光面の輝度が均一化される。

【0043】図11に示す構成ではn側電極7を直線状に形成しているが電極の形状は直線状に限定されるものではなく、たとえばS字状のように曲線状に形成しても同様の効果が得られる。主チップ面を分割する電極はp側電極6とn側電極7とのどちらでもよい。

【0044】また、p側電極6とn側電極7との一方の電極を図12に示すようにH字状などに形成して領域を分割してもよく、また2分割である必要もない。たとえば、p側電極6を十字状に形成することにより主チップ面を4つの領域に分割し、各領域の中央部にそれぞれn側電極7を配置する構成としてもよい。このように分割する領域の個数を増やすと発光面の輝度の均一性をより高めることが可能になる。

【0045】（実施形態7）本実施形態は請求項11に対応する。本実施形態では図13に示すように、図12に示した実施形態6の構成に対して、H字状のp側電極6において主チップ面の中央部に位置する直線部分に並行するようにn側電極7を直線状に延長したものである。この構成を採用すれば、図12に示した実施形態6の構成よりもp側電極6とn側電極7とが等距離になる部分が増えるから、発光面の輝度をより均一化することが可能になる。なお、本実施形態においてもp側電極6とn側電極7との関係を逆にしてもよい。

【0046】（実施形態8）本実施形態は請求項10に対応する。本実施形態では図14に示すように、p側電極6を日字状に形成し、主チップ面に長方形の2つの領域を形成してある。つまり、p側電極6により全周を囲んだ領域を2つ形成してあり、各領域ごとにn側電極7を設けている。この構成では図12に示した実施形態6の構成と比較するとp側電極6とn側電極7との間の電流経路が増加することになり、発光面における輝度の均一性がさらに向上する。

【0047】本実施形態では、p側電極6によって主チップ面に2つの領域を形成しているが、領域の個数数は2個に限定されるものではなく、たとえば図15に示すように、田字状のp側電極6を形成して主チップ面を4領域に分割してp側電極6に全周を囲まれた領域を4個形成し、各領域の中央部にそれぞれn側電極7を配置してもよい。このような構成を採用すれば、図14に示した構成と比較して発光面における輝度の均一性がさらに向上する。本実施形態においても、p側電極6とn側電極7との関係を逆にしてもよい。

【0048】（実施形態9）本実施形態は請求項12に対応する。本実施形態では、図16に示すように、主チップ面の略中央部にp側電極6を配置し、n側電極7によってp側電極6の全周を囲んだ形としているものである。p側電極6は主チップ面の中央から3方向に直線部分を放射状に延長し、一方、n側電極7はp側電極6と中心を一致させた円形部分の内側に中心に向かって3本の直線部分を突設した形状に形成してあり、p側電極6

とn側電極7との直線部分を等角度間隔で配置してある。また、p側電極6の給電部15は主チップ面の中央部とし、n側電極7の給電部16は円形部分の1箇所を設定してある。この構成ではp側電極6とn側電極7とが3回回転対称となる対称性を有した配置になる。本実施形態のLEDチップ1は、図25に示した従来構成と比較して、p側電極6とn側電極7との対向部分が多いから、発光面における輝度の均一性が向上する。なお、本実施形態においてもp側電極6とn側電極7との配置関係を逆にしてもよい。

【0049】（実施形態10）本実施形態は請求項13、請求項14、請求項15に対応する。本実施形態では、図17に示すように、p側電極6とn側電極7とを同心円状に配置し、かつ円の中心から外側に向かってp側電極6とn側電極7とを交互に入れ子状に配置してある。つまり、中心のp側電極6を円環状のn側電極7により囲み、そのn側電極7を円環状のp側電極6で囲み、さらにそのp側電極6をn側電極7で囲んだ形としてある。また、p側電極6とn側電極7との隣接する電極間の距離を等距離になるように構成してある。円環状のp側電極6およびn側電極7には1箇所ずつ給電部15、16が設けられる。本実施形態のLEDチップ1は、p側電極6とn側電極7との間で等距離で対向する部分が図16に示した実施形態9よりも多くなり、発光面の輝度の均一性がさらに向上する。

【0050】また、図16の実施形態では、主チップ面において互いに電氣的に接続されていない複数個の独立したp側電極6とn側電極7とが設けられ、各p側電極6とn側電極7とにそれぞれ給電部15、16を設けているが、図18または図19に示すように、p側電極6とn側電極7とについて同種導電形の半導体層に対応する電極同士をそれぞれ接続する導電部13、14を設けてもよい。この場合には、円環状のp側電極6とn側電極7との一部を切除し、切除した部分を導電部13、14が通るようにすればよい。この構成によっても図17に示した構成と同様の効果が得られる。

【0051】（実施形態11）本実施形態は請求項16に対応する。図17に示した実施形態10の構成では円環状に形成したp側電極6およびn側電極7を用いているが、本実施形態では、図20に示すように、円環状ではなく正方形に形成したp側電極6とn側電極7とを入れ子状に配列してある。つまり、p側電極6とn側電極7とのうち異種導電形の半導体層に対応する電極を囲むほうの電極を、主チップ面の外周形状と相似形となる環状に形成している。

【0052】本実施形態の構成では、p側電極6とn側電極7とを同心円状に配列した構成と比較するとp側電極6とn側電極7との距離が等距離になる部位が少なくなるものの、p側電極6ないしn側電極7を主チップ面の外周縁のごく近傍まで形成することができるから、結

果的に主チップ面の中心部と周縁部との輝度差を小さくすることができる。

【0053】（実施形態12）本実施形態は請求項6、請求項17、請求項18、請求項19に対応する。本実施形態では図21に示すように主チップ面に複数個ずつ設けたものであり（p側電極6を5個、n側電極7を4個設けている）、p側電極6とn側電極7とのうち異種導電形の半導体層に対応する電極間の距離を等しくするように配置してある。また、主チップ面においてp側電極6とn側電極7とが対称性を有するように配列してある。具体的には、正方形の主チップ面の四隅と中心とにそれぞれp側電極6を配置し、各辺の中央にそれぞれn側電極7を配置した形になる。p側電極6とn側電極7との配置パターンを上述のような形とすることにより、縦横斜めの4本の対称線を持つ線対称性と、主チップ面の中心を通る対称軸を有した4回の回転対称性とを有する配置パターンになる。本実施形態の構成では、p側電極6とn側電極7との間で電流経路が従来構成よりも多いから、発光面の輝度の均一性が高くなる。

【0054】なお、p側電極6とn側電極7との形状は点状に限定されるものではなく、請求項9の発明と同様に、主チップ面を複数の領域に分割する形状にp側電極6を形成し分割された各領域にn側電極7を配置する構成を採用してもよい。たとえば、図22に示すように、p側電極6の外周を正六角形とするとともに3本の対角線上にもp側電極6を形成して主チップ面に6個の領域を形成し、正三角形となる各領域の中心にn側電極7を配置する構成としてもよい。この構成では、p側電極6とn側電極7との配置パターンが、6本の対称線を有する線対称性を持ち、かつ6回の回転対称性を有することになる。請求項9に対応する図11ないし図15に示した構成と比較してp側電極6とn側電極7との配置パターンの対称性が高い本実施形態の構成では、これらの構成よりも発光面における輝度の均一性がより高くなる。

（実施形態13）本実施形態は、図23に示すように、図11に示した実施形態6の構成に対してp側電極6を線状ではなく主チップ面のほぼ全面を覆う金属膜により面状に形成し、さらにn側電極7を主チップ面の一方の対角線の両端部に設けた構成としてある。図示例ではp形半導体層5の表面から基板2に跨る部位を絶縁膜17で覆っており、p側電極6およびn側電極7の各給電部15、16はそれぞれ絶縁膜17に形成した窓孔18を通して露出させている。また、実装基板8に設けた導電体10に給電部15、16を電氣的に接続するために、半田または金のような金属のバンプ19を設けている。また、実装基板8における合成樹脂の絶縁層8aに金属のダイ20を挿入し、LEDチップ1とダイ20との間の充填材11として熱伝導性の良好な接着剤を用いている。この構成によって、LEDチップ1からの放熱性を良好にしている。なお、バンプ19を設ける代わりに導

電性接着剤によってp側電極6およびn側電極7を導電体10に接続してもよい。本実施形態の構成によっても上述した他の構成と同様にp側電極6とn側電極7との間の電流経路が従来構成よりも多いため、発光面の輝度の均一性を向上させることができる。

【0055】上述した実施形態のうちp側電極6とn側電極7との少なくとも一方が複数の給電部15、16を備えるもの（つまり、複数のp側電極6あるいは複数のn側電極7が独立して設けられているもの）では、発光面の輝度分布に偏りを少なくするように個々の給電部15、16の間で電流を制御することにより、発光面における輝度の均一性を一層向上させることが可能である。

【0056】

【発明の効果】請求項1の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続されたp側電極およびn側電極とを備え、前記主チップ面内においてp側電極およびn側電極の少なくとも一部がそれぞれ互いに並行配置され、p側電極およびn側電極において並行配置された部位を横切る方向ではp側電極とn側電極とが交互に配列されているものであり、従来構成と比較するとp側電極とn側電極との間で対向する部分が多くなるとともに等距離になる部分が多くなるから、従来構成と比較して主チップ面での電流密度の分布に偏りが少なくなり、結果的に発光面の輝度の均一性が高くなる。

【0057】請求項2の発明は、請求項1の発明において、前記p側電極および前記n側電極において、並行配置された部位が等間隔になるように配列されているので、p側電極とn側電極との間で等距離になる部分が多いことにより、発光面の輝度の均一性をより向上させることができる。

【0058】請求項3の発明は、請求項1の発明において、前記p側電極と前記n側電極との少なくとも一方については、並行配置された部位が主チップ面上では電気的に接続されていないものであり、主チップ面内においてp側電極とn側電極とが並行していない部分の割合が少なく、主チップ面での電流密度の分布の偏りが少なくなり発光面内における輝度の均一性に優れる。

【0059】請求項4の発明は、請求項1の発明において、前記p側電極および前記n側電極において、並行配置された部位を横切る方向にそれぞれ分岐しかつ互いに並行する複数の枝部が形成されているものであり、p側電極とn側電極との距離が枝部によって近距離になり、しかも互に対向する部位が多くなるから、発光面内における輝度の均一性に優れる。

【0060】請求項5の発明は、請求項1の発明において、前記主チップ面内において複数のp側電極およびn側電極の少なくとも一部がそれぞれ互いに並行配置され

る渦巻き状に延長され、渦巻き状に形成される部位の中心から外側に向かってp側電極およびn側電極を横切る方向ではp側電極とn側電極とが交互に配列されているものであり、主チップ面の全体にp側電極とn側電極との対向する部分を形成することができ、発光面の輝度の均一性が高くなる。

【0061】請求項6の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続された複数のp側電極およびn側電極とを備えるものであり、従来構成と比較すると、主チップ面内でp側電極とn側電極との電流経路を分散させることができ、発光面内における輝度の均一性に優れる。

【0062】請求項7の発明は、請求項6の発明において、前記p側電極および前記n側電極のうち異種導電形の半導体層に接続された電極間の距離を、同種導電形の半導体層に接続された電極間の距離よりも小さくしたものであり、同種導電形の半導体層に接続された電極間が近接しないことにより、発光面における輝度の均一性に優れる。

【0063】請求項8の発明は、請求項7の発明において、前記p側電極と前記n側電極のうち異種導電形の半導体層に接続された電極間が等間隔に配列されているものであり、p側電極とn側電極との間に流れる電流の電流密度の偏りが少なくなり、発光面の輝度の均一性を高めることができる。

【0064】請求項9の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面にそれぞれ接続されたp側電極およびn側電極とを備え、前記主チップ面がp側電極およびn側電極との一方により複数の領域に分割され、各領域内にそれぞれ他方が配置されるものであり、主チップ面内においてp側電極とn側電極との対向部分が従来構成よりも多くなるから、発光面の輝度の均一性に優れる。

【0065】請求項10の発明は、請求項9の発明において、前記p側電極と前記n側電極とのうちの前記一方が前記各領域をそれぞれ全周に亘って囲むように形成されるものであり、p側電極とn側電極との間の電流密度の分布の偏りが少なくなり、発光面の輝度の均一性が高くなる。

【0066】請求項11の発明は、請求項9の発明において、前記p側電極と前記n側電極とのうちの前記他方が前記一方に設けた線状部分に並行配置される線状の部分の備えるものであり、p側電極とn側電極との対向部分が多いから、発光面における輝度の均一性に優れる。

【0067】請求項12の発明は、基板上に形成されたp形半導体層およびn形半導体層と、p形半導体層およびn形半導体層において基板の反対側である主チップ面

にそれぞれ接続されたp側電極およびn側電極とを備え、p側電極およびn側電極との一方が主チップ面の中心部に配置され、前記一方を囲む形で他方が配置されているものであり、従来構成と比較すると、主チップ面においてp側電極とn側電極との対向部分が多くなるから、発光面の輝度の均一性に優れる。

【0068】請求項13の発明は、請求項12の発明において、前記p側電極と前記n側電極とが交互に入れ子状に配列されているものであり、主チップ面内においてp側電極とn側電極との対向部分が従来構成よりも多いから、発光面の輝度の均一性が高くなる。

【0069】請求項14の発明は、請求項13の発明において、前記p側電極と前記n側電極とが等間隔になるように配列されているものであり、p側電極とn側電極との間の電極間距離の等しい部分が多くなることによって、電流密度の分布の偏りが少なくなり、発光面の輝度の均一性に優れる。

【0070】請求項15の発明は、請求項13または請求項14の発明において、前記p側電極と前記n側電極とが同心円状に配列されているものであり、p側電極とn側電極との電極間の距離を主チップ面の全体でほぼ等しくすることが可能になり、発光面における輝度の均一性に優れる。

【0071】請求項16の発明は、請求項13または請求項14の発明において、前記p側電極と前記n側電極とを主チップ面の外周形状の相似形状としたものであり、主チップ面の外周縁付近まで電極を形成することができ、主チップ面の外周縁付近と中央付近との輝度差を少なくすることができる。

【0072】請求項17の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で線対称性を有するものであり、電極の配置に対称性が与えられているから、電流密度の分布の偏りを低減することができ、発光面における輝度の均一性に優れる。

【0073】請求項18の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で2回以上の回転対称性を有するものであり、電極の配置に対称性が与えられているから、電流密度の分布の偏りを低減することができ、発光面における輝度の均一性に優れる。

【0074】請求項19の発明は、請求項1または請求項6または請求項9または請求項12の発明において、前記n側電極と前記p側電極との配置パターンが、前記主チップ面内で2回以上の回転対称性を有するとともに、2本以上の対称線に関して線対称性を有するものであり、電極の配置に対称性が与えられているから、電流密度の分布の偏りを低減することができ、発光面におけ

る輝度の均一性に優れる。

【0075】請求項20の発明は、請求項1または請求項6または請求項9の発明において、前記n側電極と前記p側電極とにそれぞれ給電する給電部を設け、n側電極とp側電極との少なくとも一方の給電部を複数個設けたものであり、発光面の輝度分布に偏りを少なくするように個々の給電部の間で電流を制御することにより、発光面における輝度の均一性を向上させることができる。

【図面の簡単な説明】

【図1】本発明の実施形態1を示す概略平面図である。

【図2】同上の他の構成例を示す概略平面図である。

【図3】同上の別の構成例を示す概略平面図である。

【図4】本発明の実施形態2を示す概略平面図である。

【図5】同上の他の構成例を示す概略平面図である。

【図6】本発明の実施形態3を示す概略平面図である。

【図7】本発明の実施形態4を示す概略平面図である。

【図8】同上の他の構成例を示す概略平面図である。

【図9】本発明の実施形態5を示す概略平面図である。

【図10】同上の他の構成例を示す概略平面図である。

【図11】本発明の実施形態6を示す概略平面図である。

【図12】同上の他の構成例を示す概略平面図である。

【図13】本発明の実施形態7を示す概略平面図である。

【図14】本発明の実施形態8を示す概略平面図である。

【図15】同上の他の構成例を示す概略平面図である。

【図16】本発明の実施形態9を示す概略平面図である。

【図17】本発明の実施形態10を示す概略平面図である。

【図18】同上の他の構成例を示す概略平面図である。

【図19】同上の別の構成例を示す概略平面図である。

【図20】本発明の実施形態11を示す概略平面図である。

【図21】本発明の実施形態12を示す概略平面図である。

【図22】同上の他の構成例を示す概略平面図である。

【図23】本発明の実施形態13を示し、(a)は概略平面図、(b)は断面図である。

【図24】本発明に係るLEDチップの使用例を示す断面図である。

【図25】従来構成を示し、(a)は平面図、(b)は断面図である。

【図26】従来構成を示すフェースダウン状態での実装状態を示す断面図である。

【符号の説明】

- 1 LEDチップ
- 2 基板
- 3 n形半導体層

4 発光層
5 p 形半導体層
6 p 側電極

7 n 側電極
13, 14 導電部
15, 16 給電部

【図 1】

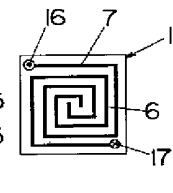
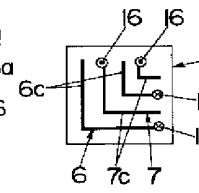
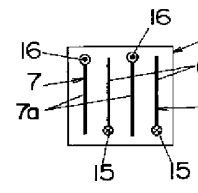
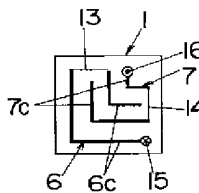
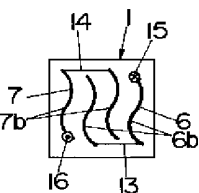
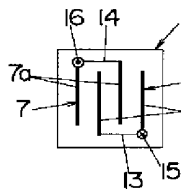
【図 2】

【図 3】

【図 4】

【図 5】

【図 8】



1 LEDチップ
6 p 側電極
6a 直線部
7 n 側電極
7a 直線部

【図 7】

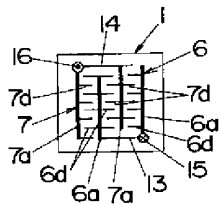
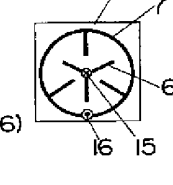
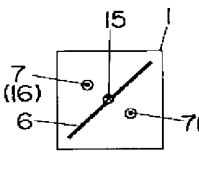
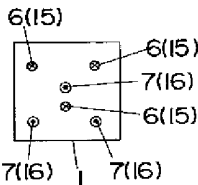
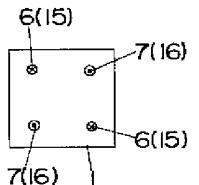
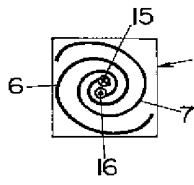
【図 9】

【図 10】

【図 11】

【図 16】

【図 6】



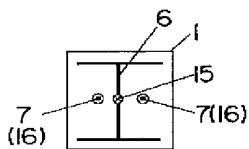
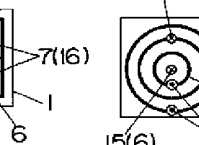
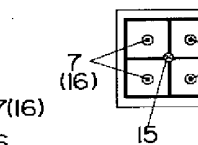
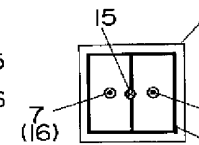
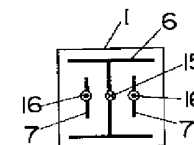
【図 13】

【図 14】

【図 15】

【図 17】

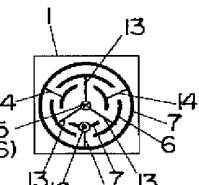
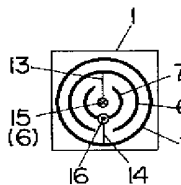
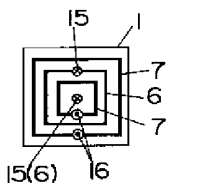
【図 12】



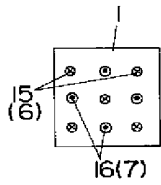
【図 20】

【図 18】

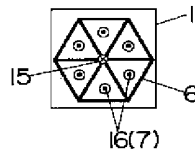
【図 19】



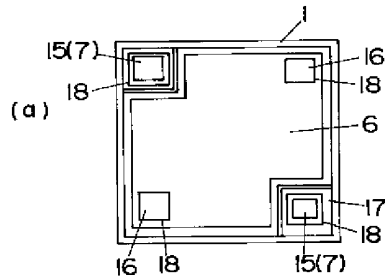
【図 2 1】



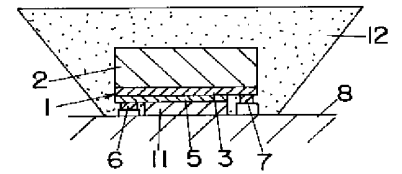
【図 2 2】



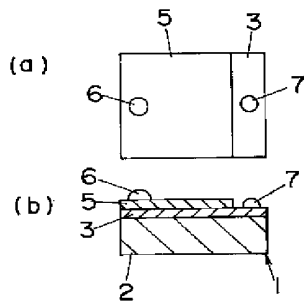
【図 2 3】



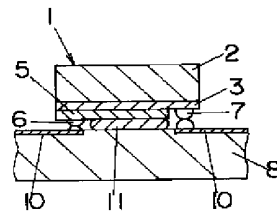
【図 2 4】



【図 2 5】



【図 2 6】



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DESCRIPTION OF DRAWINGS DRAWINGS

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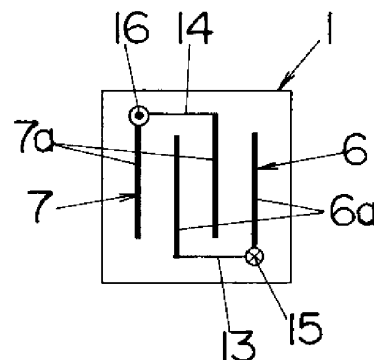
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

- [Drawing 1]It is an outline plan view showing Embodiment 1 of the present invention.
[Drawing 2]It is an outline plan view showing other configuration examples same as the above.
[Drawing 3]It is an outline plan view showing another configuration example same as the above.
[Drawing 4]It is an outline plan view showing Embodiment 2 of the present invention.
[Drawing 5]It is an outline plan view showing other configuration examples same as the above.
[Drawing 6]It is an outline plan view showing Embodiment 3 of the present invention.
[Drawing 7]It is an outline plan view showing Embodiment 4 of the present invention.
[Drawing 8]It is an outline plan view showing other configuration examples same as the above.
[Drawing 9]It is an outline plan view showing Embodiment 5 of the present invention.
[Drawing 10]It is an outline plan view showing other configuration examples same as the above.
[Drawing 11]It is an outline plan view showing Embodiment 6 of the present invention.
[Drawing 12]It is an outline plan view showing other configuration examples same as the above.
[Drawing 13]It is an outline plan view showing Embodiment 7 of the present invention.
[Drawing 14]It is an outline plan view showing Embodiment 8 of the present invention.
[Drawing 15]It is an outline plan view showing other configuration examples same as the above.
[Drawing 16]It is an outline plan view showing Embodiment 9 of the present invention.
[Drawing 17]It is an outline plan view showing Embodiment 10 of the present invention.
[Drawing 18]It is an outline plan view showing other configuration examples same as the above.
[Drawing 19]It is an outline plan view showing another configuration example same as the above.
[Drawing 20]It is an outline plan view showing Embodiment 11 of the present invention.
[Drawing 21]It is an outline plan view showing Embodiment 12 of the present invention.
[Drawing 22]It is an outline plan view showing other configuration examples same as the above.
[Drawing 23]Embodiment 13 of the present invention is shown, (a) is an outline plan view and (b) is a cross sectional view.
[Drawing 24]It is a cross sectional view showing the example of use of the LED chip concerning the present invention.
[Drawing 25]Composition is shown conventionally, (a) is a plan view and (b) is a cross sectional view.
[Drawing 26]It is a cross sectional view showing the mounted state in a facedown state which shows composition conventionally.

[Explanations of letters or numerals]

- 1 LED chip
- Substrate
- N type semiconductor layer
- Luminous layer
- P type semiconductor layer
- p lateral electrode
- n lateral electrode



1 LEDチップ
6 p側電極
6a 直線部
7 n側電極
7a 直線部

Representative drawing

Representative drawing | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| 23 | 24 |

13 and 14 Current carrying part
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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]A p type semiconductor layer and a n type semiconductor layer are formed on a substrate, and the present invention relates to the LED chip by which p lateral electrode and n lateral electrode were connected to the p type semiconductor layer and the n type semiconductor layer, respectively in the main tip surface which is an opposite side of the substrate in a p type semiconductor layer and a n type semiconductor layer.

[0002]

[Description of the Prior Art]From the former, as shown in Fig.25, LED chip 1 of structure in which the conducted type of current laminated the n-type p type semiconductor layer 5 which consists of gallium nitride whose conducted type of current it comes out and is a p form via the n type semiconductor layer 3 which consists of a certain gallium nitride on the substrate 2 of sapphire is provided. In LED chip 1 to illustrate, the p lateral electrode 6 connected to the n lateral electrode 7 connected to the n type semiconductor layer 3 and the p type semiconductor layer 5 is arranged to the side part of the substrate 2.

[0003]LED chip 2 constituted in this way is used in the form where electric power is supplied to the p lateral electrode 6 and the n lateral electrode 7 via a bonding wire, respectively, when mounted in the state of the face up which carries out the main tip surface which is providing the p lateral electrode 6 and the n lateral electrode 7 the optical extraction side.

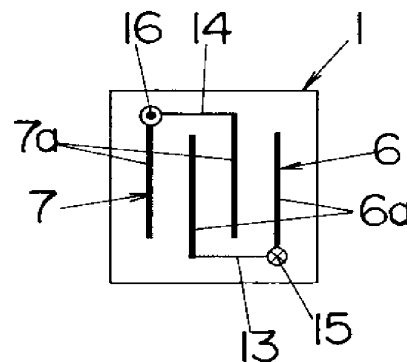
[0004]Since the substrate 2 consists of sapphire and it has translucency, mounting in the facedown state which carries out the substrate 2 the optical extraction side as shown in Fig.26 is also possible. In this case, flip chip mounting is performed so that the p lateral electrode 6 and the n lateral electrode 7 may electrically be connected to the conductor 10 provided to the mounting board 8 by making the p lateral electrode 6 and the n lateral electrode 7 into bump structure. When adopting such a mounting form, it fills up with the filler 11 between LED chip 1 and the mounting board 8.

[0005]

[Problem to be solved by the invention]By the way, with LED chip 1 of composition, the p lateral electrode 6 and the n lateral electrode 7 are provided at a time by punctiform [one] conventionally which was mentioned above, Although luminance is high between the p lateral electrode 6 and the n lateral electrode 7 in the luminescent surface (light extraction surface) of LED chip 1, the audit observation that luminance is low is obtained by the other part. This is considered to be because for current density to become small quickly and for a bias to arise in distribution of current density between the p lateral electrode 6 and the n lateral electrode 7, if it separates from between the p lateral electrode 6 and the n lateral electrodes 7 although current density is sufficiently large. In short, luminance unevenness has arisen in the luminescent surface of LED chip 1.

[0006]A luminescent surface is a 300-micrometer angle degree, and since LED chip 1 provided generally has the comparatively small ratio of the area of a luminescent surface to the electrode area of the p lateral electrode 6 and the n lateral electrode 7, even if luminance unevenness has arisen in the luminescent surface, it is usually on practical use and does not become a problem.

[0007]On the other hand, in order that white LED is used for an indicator or a display, and also using as a light source for lighting may be proposed and it may apply to this kind of use, it is required that the luminance per chip should be enlarged, and these days requires large area-ization of the LED chip as a result. If an LED chip is large-area-ized, since the area of a



1 LEDチップ
6 p側電極
6a 直線部
7 n側電極
7a 直線部

Representative drawing

Representative drawing | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| 23 | 24 |

luminescent surface enlarges conventionally to an electrode area, the luminance unevenness within a luminescent surface will come to be recognized visually, and a problem will arise to use it as a light source for lighting.

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[0008]Succeeding in the present invention in view of the aforementioned reason, the object is to provide the LED chip which decreased the luminance unevenness within a luminescent surface and improved the homogeneity of luminance.

[0009]

[Means for solving problem]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 1 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, Into the aforementioned main tip surface, parallel arrangement of at least one copy of p lateral electrode and n lateral electrode is carried out mutually, respectively, and p lateral electrode and n lateral electrode are alternately arranged towards crossing the part by which parallel arrangement was carried out in p lateral electrode and n lateral electrode.

[0010]In invention of Claim 1, in the aforementioned p lateral electrode and the aforementioned n lateral electrode, invention of Claim 2 is arranged so that the part by which parallel arrangement was carried out may become at equal intervals.

[0011]The part where parallel arrangement of the invention of Claim 3 was carried out in invention of Claim 1 at least about one side of the aforementioned p lateral electrode and the aforementioned n lateral electrode is not electrically connected on the main tip surface.

[0012]A plurality of branches which invention of Claim 4 branches, respectively in the direction which crosses the part by which parallel arrangement was carried out in the aforementioned p lateral electrode and the aforementioned n lateral electrode in invention of Claim 1, and are mutually parallel are formed.

[0013]Invention of Claim 5 is extended in invention of Claim 1 by the curled form by which parallel arrangement of at least one copy of a plurality of p lateral electrodes and n lateral electrode is mutually carried out into the aforementioned main tip surface, respectively, Towards crossing p lateral electrode and n lateral electrode toward the outside from the center of the part formed spirally, p lateral electrode and n lateral electrode are arranged alternately.

[0014]The Claim 6 present invention is characterized by invention comprising the following.

A p type semiconductor layer and a n type semiconductor layer which were formed on a substrate.

p lateral electrode and n lateral electrode of every plurality which were connected to a main tip surface which is an opposite side of a substrate in a p type semiconductor layer and a n type semiconductor layer, respectively.

[0015]Invention of Claim 7 was made smaller than the distance between the electrodes by which the distance between the electrodes connected to the semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode was connected to the semiconductor layer of electric conduction type of the same kind in invention of Claim 6.

[0016]Between the electrodes by which invention of Claim 8 was connected to the semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode in invention of Claim 7 is arranged at equal intervals.

[0017]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 9 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, the aforementioned main tip surface is divided into a plurality of regions by one side with p lateral electrode and n lateral electrode, and another side is arranged in each region, respectively.

[0018]In invention of Claim 9, invention of Claim 10 is formed so that aforementioned one of the aforementioned p lateral electrode and the aforementioned n lateral electrodes may cover the whole circumference, respectively and may surround each aforementioned region.

[0019]Invention of Claim 11 equips the linear part which aforementioned another side of the aforementioned p lateral electrode and the aforementioned n lateral electrodes provided to aforementioned one side with the linear portion by which parallel arrangement is carried out in invention of Claim 9.

[0020]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 12 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, one side with p lateral electrode and n lateral electrode is arranged in the central part of a main tip surface, and another side is arranged in the form surrounding aforementioned one circumference.

[0021]As for invention of Claim 13, in invention of Claim 12, the aforementioned p lateral electrode and the aforementioned n lateral electrode are alternately arranged by nesting form.

[0022]In invention of Claim 13, invention of Claim 14 is arranged so that the aforementioned p lateral electrode and the aforementioned n lateral electrode may become at equal intervals.

[0023]As for invention of Claim 15, in invention of Claim 13 or Claim 14, the aforementioned p lateral electrode and the aforementioned n lateral electrode are arranged concentrically.

[0024]In invention of Claim 13 or Claim 14, the aforementioned p lateral electrode and the aforementioned n lateral electrode of invention of Claim 16 are the similar shape of the peripheral shape of a main tip surface.

[0025]In invention of Claim 17, in invention of Claim 1, Claim 6, Claim 9, or Claim 12, the arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has axial symmetry nature in the aforementioned main tip surface.

[0026]In invention of Claim 18, in invention of Claim 1, Claim 6, Claim 9, or Claim 12, the

arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface.

[0027]In invention of Claim 1, Claim 6, Claim 9, or Claim 12, invention of Claim 19 has axial symmetry nature about two or more symmetrical lines while the arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface.

[0028]In invention of Claim 1, Claim 6, or Claim 9, invention of Claim 20 provided the feed part which supplies electric power to the aforementioned n lateral electrode and the aforementioned p lateral electrode, respectively, and provided multiple feed parts of at least 1 side of n lateral electrode and p lateral electrode.

[0029]Since many courses into which current flows between p lateral electrode and n lateral electrode are formed, the difference of the current density of the current which passes through a luminous region can be conventionally decreased as compared with composition, and any composition mentioned above can attain uniformization of the current density in a luminous region. As a result, luminance unevenness can be conventionally decreased substantially rather than composition. To the modes which mounts an LED chip, there is no restriction in particular and it can apply the composition mentioned above also in which modes of a face-up state and a facedown state. However, when p lateral electrode and n lateral electrode adopt the composition which is not punctiform, the way which p lateral electrode and n lateral electrode mount in the state of facedown one which does not exist in the luminescent surface side is able to reduce luminance unevenness more.

[0030]

[Mode for carrying out the invention]LED chip 1 described in each following embodiment, On the substrate 2 which was shown in Fig.25 and which has the translucency which consists of sapphire conventionally like composition, a buffer layer (not shown) and the conducted type of current -- being n-type -- coming out -- the n type semiconductor layer 3 which consists of a certain gallium nitride (GaN) layer, and a cladding layer (not shown) -- It has the composition which accumulated in order the cladding layer (not shown) and the p type semiconductor layer 5 which consists of the gallium nitride (GaN) layer whose conducted type of current is a p form on the luminous layer 4 (refer to Fig.23). However, the kind of semiconductor is not limited to the above gallium nitride system compound semiconductors, and can use other semiconductors.

[0031]In the n type semiconductor layer 3, the n lateral electrode 7 is formed in the surface of an opposite side, and the p lateral electrode 6 is formed [substrate / 2] in the surface of an opposite side in the substrate 2 in the p type semiconductor layer 5. Below in the semiconductor layer containing the n type semiconductor layer 3 and the p type semiconductor layer 5, the surface which is providing the surface, i.e., the p lateral electrode 6, and the n lateral electrode 7 of the opposite side is called a main tip surface in the substrate 1. In constituting the light equipment for lighting using this LED chip 1, If LED chip 1 is arranged in the covering 12 of the translucency synthetic resin which distributed the fluorescent substance which is excited by the near ultraviolet ray and emits light in yellow as shown in Fig.24, The mixed colors of a blue light which emits light from LED chip 1, and the yellow light of the fluorescent substance in the covering 12 can be carried out, and the light equipment of white light can be constituted. In the illustrated example, flip chip mounting is performed to the mounting board 8, and it has mounted in the state of facedown one. In following embodiments, although the main tip surface of LED chip 1 is formed in the shape of square, the form of a main tip surface is not limited to this. In the embodiment described below, the p lateral electrode 6 and the n lateral electrode 7 can be replaced.

[0032](Embodiment 1) This embodiment corresponds to Claim 1 and Claim 2. In this embodiment, as shown in Fig.1, in the main tip surface of LED chip 1, the p lateral electrode 6 and the n lateral electrode 7 have the straight parts 6a and 7a, While parallel arrangement of the straight parts 6a and 7a is carried out, towards crossing the p lateral electrode 6 and the n lateral electrode 7 in the straight parts 6a and 7a (direction which intersects perpendicularly), the p lateral electrode 6 and the n lateral electrode 7 are arranged alternately. By the illustrated example, it has provided the two straight parts 6a and 7a at a time at equal intervals about the p lateral electrode 6 and the n lateral electrode 7, and the straight part 6a connected to the semiconductor layers 3 and 5 (refer to Fig.23) of electric conduction type of the same kind and 7a are connected by the current carrying parts 13 and 14 provided to the one end part of the straight parts 6a and 7a, respectively. That is, it is electrically connected by the current carrying part 13 between the straight parts 7a of the n lateral electrode 7, and is electrically connected by the current carrying part 14 between the straight parts 6a of the p lateral electrode 6. In this embodiment, the two feed parts 15 and 16 electrically connected with the p lateral electrode 6 and the n lateral electrode 7, respectively are formed near the corner on one diagonal line of the main tip surface of LED chip 1 by the vacuum plating of aluminium etc. That is, the p lateral electrode 6 and the n lateral electrode 7 have provided the feed parts 15 and 16 per place to the part between every two straight parts 6a and 7a, respectively, are divided into each straight part 6a and 7a from the feed parts 15 and 16, and it is made to have flowed through current.

[0033]Then, if it energizes to the feed parts 15 and 16 and they are switched on in LED chip 1 of this embodiment, Since a luminous region is formed, respectively among the straight parts 6a and 7a by which parallel arrangement was carried out in the p lateral electrode 6 and the n lateral electrode 7, current can be sent without centralizing a current route within one LED chip 1, and the luminance of the luminescent surface of LED chip 1 can be made to uniformize. That is, in this embodiment, since there are more parts where the p lateral electrode 6 and the n lateral electrode 7 oppose conventionally than composition and there are many parts where the p lateral electrode 6 and the n lateral electrode 7 moreover become the equal distance, the bias of distribution of current density can be reduced and the regularity of luminance can be raised.

[0034]Although the part which carries out parallel arrangement in the p lateral electrode 6 and the n lateral electrode 7 was formed as the straight parts 6a and 7a with the composition shown in Fig.1, the waveform parts 6b and 7b of form which move in a zigzag direction in the p lateral electrode 6 and the n lateral electrode 7 are formed, and it may be made to make parallel the waveform parts 6b and 7b, as shown in Fig.2. Or the flections 6c and 7c made bent in the shape of an L character are formed in the p lateral electrode 6 and the n lateral electrode 7, and it may be made to make the flections 6c and 7c parallel with them again, as shown in Fig.3. In the configuration example shown in Fig.2 and Fig.3, it has provided at the end which are either the two waveform parts 6b and 7b or the flections 6c and 7c, and is separated from the current carrying parts 13 and 14 in the feed parts 15 and 16. Also in which composition, the position of the feed parts 15 and 16 is chosen so that the current density of the current which flows between the p lateral electrode 6 and the n lateral electrode 7 may be uniformized.

[0035](Embodiment 2) This embodiment corresponds to Claim 3. In this embodiment, as shown in Fig.4, in the main tip surface of LED chip 1, the p lateral electrode 6 and the n lateral electrode 7 have the straight parts 6a and 7a, While parallel arrangement of the straight parts 6a and 7a is carried out, towards crossing the p lateral electrode 6 and the n lateral electrode 7 in the straight parts 6a and 7a (direction which intersects perpendicularly), the p lateral electrode 6 and the n lateral electrode 7 are arranged alternately. By the illustrated example, it has provided the two straight parts 6a and 7a at a time at equal intervals about the p lateral electrode 6 and the n lateral electrode 7. However, it differs in Embodiment 1, and within LED chip 1, it is not electrically connected but the straight parts 6a and 7a are independently. Therefore, the feed parts 15 and 16 are individually provided to each straight part 6a and every 7a. If the feed part 15 of the p lateral electrode 6 is provided to the one end side of the straight part 6a, the feed part 16 of the n lateral electrode 7 is provided to the other end side of the straight part 7a, and current distributes and it makes it have flowed through it among the straight parts 6a and 7a.

[0036]In the composition of this embodiment, as a result of the ratio of the part by which parallel arrangement is not carried out in the p lateral electrode 6 and the n lateral electrode 7 becoming less than Embodiment 1, the bias of the current density of a luminous region decreases more, and the regularity of luminance becomes still higher rather than the composition of Embodiment 1.

[0037]It is also possible to replace with the straight parts 6a and 7a, and to consider it as the shape of a curve like the waveform parts 6a and 7a like Embodiment 1, and as shown in Fig.5, it is also possible to use the flections 6c and 7c bent in the shape of an L character.

[0038](Embodiment 3) This embodiment corresponds to Claim 4. That is, as shown in Fig.6, the p lateral electrode 6 and the n lateral electrode 7 with composition and the same composition of Embodiment 1 shown in Fig.1 are provided, and a plurality of branches 6d and 7d which branch further, respectively in a direction orthogonal to the straight parts 6a and 7a are provided, and it has installed so that the branches 6d and 7d may be mutually parallel. The distance between the p lateral electrode 6 and the n lateral electrode 7 which oppose in this embodiment as compared with the composition of Embodiment 1 shown in Fig.1 is brief, And since the density which accounts for the whole luminescent surface of the p lateral electrode 6 and the n lateral electrode 7 is large, when LED chip 1 is made to turn on, the luminance of the whole luminescent surface is further uniformized rather than the composition of Embodiment 1.

[0039](Embodiment 4) This embodiment corresponds to Claim 5. According to this embodiment, as shown in Fig.7, the p lateral electrode 6 and the n lateral electrode 7 are spirally formed in the main tip surface, respectively. Parallel arrangement is carried out as left-handed rotation being spiral from the center in the p lateral electrode 6 and the n lateral electrode 7, and it is made to be alternately arranged in both illustrated examples from the center in the p lateral electrode 6 and the n lateral electrode 7 towards crossing the p lateral electrode 6 and the n lateral electrode 7 toward the outside. The feed parts 15 and 16 are provided at the end on the center side. Since it is less than Embodiment 1 which the ratio of the portion in the p lateral electrode 6 and the n lateral electrode 7 which is not mutually parallel showed to Fig.1 to the whole luminescent surface also by this composition, it becomes possible to make the luminance of a luminescent surface further uniformize. Although the smooth curve-like whorl is illustrated by Fig.7 as spiral here, the effect same also as a whorl of the form which connected the straight line as shown in Fig.8 is acquired. With the composition shown in Fig.8, the feed parts 15 and 16 are used as the end of the vortical outside, and since the feed parts 15 and 16 separate and are arranged on a chip surface, the bias of distribution of current density is reduced and it becomes easy to make luminance of a luminescent surface regular with this composition.

[0040](Embodiment 5) This embodiment corresponds to Claim 6, Claim 7, and Claim 8. It has the composition which provided two or more p lateral electrodes 6 to the p type semiconductor layer 5 while providing two or more n lateral electrodes 7 to the n type semiconductor layer 3 in a main tip surface, as this embodiment is shown in Fig.9. In the illustrated example, it is enlarging among the p lateral electrode 6 and the n lateral electrode 7 rather than the distance between the electrodes corresponding to the semiconductor layer of different-species electric conduction type between the electrodes corresponding to the semiconductor layer of electric conduction type of the same kind. Among the p lateral electrode 6 and the n lateral electrode 7, between the electrodes corresponding to the semiconductor layer of electric conduction type of the same kind, it is arranged so that it may become regular intervals. In short, in the both ends of one diagonal line, the p lateral electrode 6 (the feed part 15 and combination) is arranged among the four corners of a main tip surface, and the n lateral electrode 7 (the feed part 16 and combination) is arranged in the both ends of the diagonal line of another side. It becomes possible to increase conventionally the portion which becomes the equal distance between the electrodes corresponding to different-species electric conduction type rather than composition, and to uniformize the luminance of a luminescent surface by this composition.

[0041]As shown in Fig.10, while having composition which provides the p lateral electrode 6

and the three n lateral electrodes 7 at a time and arranging four electrodes in the four corners of a main tip surface, the composition which arranges the two remaining electrodes in the central part of the main tip surface may be adopted. That is, while arranging each three electrodes corresponding to the semiconductor layer of electric conduction type of the same kind to triangular shape, two electrodes are arranged to the corner where a main tip surface is adjacent to, The one remaining electrodes are arranged in the central part of the main tip surface, and one of the electrodes corresponding to the semiconductor layer of different-species electric conduction type is arranged so that it may be placed into the triangle mentioned above. In this composition, since multiple current routes between the electrodes corresponding to the semiconductor layer of different-species electric conduction type are formed, The regularity of the luminance of a luminescent surface becomes comparatively high, and moreover, near the center of a main tip surface, since the distance between the electrodes corresponding to the semiconductor layer of different-species electric conduction type is smaller than other parts, the luminance near the center of a luminescent surface becomes higher than a peripheral part. Though the homogeneity of the luminance of a luminescent surface is maintained as the whole in short, it becomes possible to make luminance near a center high.

[0042](Embodiment 6) This embodiment corresponds to Claim 9. In this embodiment, as shown in Fig.11, while one electrode of the p lateral electrodes 6 and the n lateral electrodes 7 which are connected to the n type semiconductor layer 3 and the p type semiconductor layer 5, respectively is formed in linear shape and this electrode divides a main tip surface into two regions, it has composition which provided the electrode of another side for every region. In the illustrated example, the p lateral electrode 6 is formed in the linear shape which laps with one diagonal line of a main tip surface, a main tip surface is divided into two regions, and the n lateral electrode 7 is provided for every region. Since many opposing parts between the p lateral electrode 6 and the n lateral electrode 7 are conventionally formed also in this composition as compared with composition, the luminance of a luminescent surface is uniformized.

[0043]With the composition shown in Fig.11, although the n lateral electrode 7 is formed in linear shape, the form of an electrode is not limited to linear shape, and even if it forms in the shape of a curve, for example like the shape of an S character, the same effect is acquired. Whichever of the p lateral electrode 6 and the n lateral electrode 7 may be sufficient as the electrode which divides a main tip surface.

[0044]As shown in Fig.12, it is necessary to form one electrode of the p lateral electrode 6 and the n lateral electrode 7 in the shape of an H character etc., and a region may be divided, and it is not necessary to be two division. For example, it is good by forming the p lateral electrode 6 in cross shape also as composition which divides a main tip surface into four regions, and arranges the n lateral electrode 7 in the central part of each region, respectively. If the number of the region divided in this way is increased, it will become possible to improve the homogeneity of the luminance of a luminescent surface more.

[0045](Embodiment 7) This embodiment corresponds to Claim 11. In this embodiment, as shown in Fig.13, the n lateral electrode 7 is extended to linear shape so that it may be parallel to the composition of Embodiment 6 shown in Fig.12 with the linear part which is placed at the central part of the main tip surface in the H character-like p lateral electrode 6. Since the portion from which the p lateral electrode 6 and the n lateral electrode 7 become the equal distance rather than the composition of Embodiment 6 shown in Fig.12 will increase if this composition is adopted, it becomes possible to uniformize the luminance of a luminescent surface more. Also in this embodiment, relation between the p lateral electrode 6 and the n lateral electrode 7 may be made reverse.

[0046](Embodiment 8) This embodiment corresponds to Claim 10. In this embodiment, as shown in Fig.14, the p lateral electrode 6 is formed in the shape of a Japanese character, and two regions of rectangular shape are formed in the main tip surface. That is, two regions surrounding [with the p lateral electrode 6] the whole circumference are formed, and the n lateral electrode 7 is provided for every region. As compared with the composition of Embodiment 6 shown in Fig.12, the current route between the p lateral electrode 6 and the n lateral electrode 7 will increase, and this composition further improves the homogeneity of the luminance in a luminescent surface.

[0047]Although two regions are formed in a main tip surface with the p lateral electrode 6 in this embodiment, As it is not limited to two pieces and shown, for example in Fig.15, the number number of regions may form the ****-like p lateral electrode 6, may form four regions which divided the main tip surface into four regions, and had the whole circumference surrounded by the p lateral electrode 6, and may arrange the n lateral electrode 7 in the central part of each region, respectively. If such composition is adopted, as compared with the composition shown in Fig.14, the homogeneity of the luminance in a luminescent surface will further improve. Also in this embodiment, relation between the p lateral electrode 6 and the n lateral electrode 7 may be made reverse.

[0048](Embodiment 9) This embodiment corresponds to Claim 12. According to this embodiment, as shown in Fig.16, the p lateral electrode 6 is arranged in the approximately center part of a main tip surface, and it is considered as the form surrounding [with the n lateral electrode 7] the whole circumference of the p lateral electrode 6. The p lateral electrode 6 extends a linear part radiately in the three directions from the center of a main tip surface, and on the other hand, the n lateral electrode 7 is formed in the form which protruded three linear parts toward the center inside the circular portion which coincided the p lateral electrode 6 and the center, and arranges the linear part of the p lateral electrode 6 and the n lateral electrode 7 by the equiangular distance. The feed part 15 of the p lateral electrode 6 considers it as the central part of the main tip surface, and it has set the feed part 16 of the n lateral electrode 7 as one place of a circular portion. With this composition, the p lateral electrode 6 and the n lateral electrode 7 become arrangement with the symmetry which serves as the symmetry of revolution 3 times. Since LED chip 1 of this embodiment has many opposing parts

of the p lateral electrode 6 and the n lateral electrode 7 conventionally which was shown in Fig.25 as compared with composition, its homogeneity of the luminance in a luminescent surface improves. Also in this embodiment, arrangement relationship of the p lateral electrode 6 and the n lateral electrode 7 may be made reverse.

[0049](Embodiment 10) This embodiment corresponds to Claim 13, Claim 14, and Claim 15. According to this embodiment, as shown in Fig.17, the p lateral electrode 6 and the n lateral electrode 7 are arranged concentrically, and the p lateral electrode 6 and the n lateral electrodes 7 are alternately arranged from the center of the circle to nesting form toward the outside. That is, it is considered as the form which surrounded the central p lateral electrode 6 with the circular n lateral electrode 7, surrounded the n lateral electrode 7 with the circular p lateral electrode 6, and surrounded the p lateral electrode 6 with the n lateral electrode 7 further. It constitutes so that it may become the equal distance about the distance between the adjoining electrodes of the p lateral electrode 6 and the n lateral electrode 7. The one feed part 15 and 16 is provided at a time by the circular p lateral electrode 6 and the n lateral electrode 7. The portion of LED chip 1 of this embodiment which opposes at the equal distance between the p lateral electrode 6 and the n lateral electrode 7 increases more than Embodiment 9 shown in Fig.16, and its homogeneity of the luminance of a luminescent surface further improves.

[0050]Although the independent p lateral electrode 6 and the n lateral electrode 7 of the plurality which is not electrically mutually connected in the main tip surface are provided and the feed parts 15 and 16 are provided to the p lateral electrodes 6 each and the n lateral electrode 7 in the embodiment of Fig.16, respectively, As shown in Fig.18 or Fig.19, the current carrying parts 13 and 14 which connect the electrodes corresponding to the semiconductor layer of electric conduction type of the same kind about the p lateral electrode 6 and the n lateral electrode 7, respectively may be provided. In this case, some of circular p lateral electrodes 6 and n lateral electrodes 7 are excised, and the current carrying parts 13 and 14 should just pass along the excised portion. The same effect as the composition shown in Fig.17 also by this composition is acquired.

[0051](Embodiment 11) This embodiment corresponds to Claim 16. In this embodiment, although the p lateral electrode 6 and the n lateral electrode 7 which were formed in a circle are used with the composition of Embodiment 10 shown in Fig.17, as shown in Fig.20, it is not circular and has arranged the p lateral electrode 6 and the n lateral electrode 7 which were formed in the shape of square to nesting form. That is, the electrode of the way surrounding the electrode corresponding to the semiconductor layer of different-species electric conduction type among the p lateral electrode 6 and the n lateral electrode 7 is formed in annular [used as the peripheral shape of a main tip surface, and similar figures].

[0052]That whose part where the distance of the p lateral electrode 6 and the n lateral electrode 7 turns into the equal distance in the composition of this embodiment as compared with the composition which arranged the p lateral electrode 6 and the n lateral electrode 7 concentrically decreases, Since the p lateral electrode 6 thru/or the n lateral electrode 7 can be formed to very near the outer peripheral edge of a main tip surface, luminance difference of the central part of a main tip surface and a peripheral edge part can be made small as a result.

[0053](Embodiment 12) This embodiment corresponds to Claim 6, Claim 17, Claim 18, and Claim 19. In this embodiment, as shown in Fig.21, more than one are provided every to a main tip surface (five pieces and the four n lateral electrodes 7 are provided for the p lateral electrode 6), and it arranges so that distance between the electrodes corresponding to the semiconductor layer of different-species electric conduction type may be made equal among the p lateral electrode 6 and the n lateral electrode 7. It has arranged so that the p lateral electrode 6 and the n lateral electrode 7 may have symmetry in a main tip surface. It becomes a form which has arranged the p lateral electrode 6 at the four corners and center of a square main tip surface, respectively, and has arranged the n lateral electrode 7 in the center of each side specifically, respectively. By making the arrangement pattern of the p lateral electrode 6 and the n lateral electrode 7 into the above forms, it becomes an arrangement pattern which has axial symmetry nature with four slanting symmetrical lines in every direction, and 4 times of symmetry-of-revolution nature with the axis of symmetry which passes along the center of a main tip surface. In the composition of this embodiment, since there are more current routes conventionally between the p lateral electrode 6 and the n lateral electrode 7 than composition, the homogeneity of the luminance of a luminescent surface becomes high.

[0054]The form of the p lateral electrode 6 and the n lateral electrode 7 is not limited to punctiform, and may adopt the composition which arranges the n lateral electrode 7 as each region which formed the p lateral electrode 6 in the form which divides a main tip surface into a plurality of regions, and was divided into it like invention of Claim 9. For example, it is good for the center of each region which forms the p lateral electrode 6 also on three diagonal lines, forms six regions in a main tip surface while making the periphery of the p lateral electrode 6 into a right hexagon, as shown in Fig.22, and serves as an equilateral triangle also as composition which arranges the n lateral electrode 7. In this composition, the arrangement pattern of the p lateral electrode 6 and the n lateral electrode 7 will have the axial symmetry nature which has six symmetrical lines, and it will have 6 times of symmetry-of-revolution nature. As compared with the composition shown in the Fig.11 thru/or Fig.15 corresponding to Claim 9, the homogeneity of the luminance in a luminescent surface becomes higher rather than these composition with the composition of this embodiment with the high symmetry of the arrangement pattern of the p lateral electrode 6 and the n lateral electrode 7. (Embodiment 13) As shown in Fig.23, this embodiment forms the p lateral electrode 6 in plane-like form to the composition of Embodiment 6 shown in Fig.11 with the metal film which covers substantially the whole surface of the main tip surface instead of a line, and has considered it as the composition which provided the n lateral electrode 7 to the both ends of one diagonal line of a main tip surface further. In the illustrated example, the part over the substrate 2 is covered with the insulator layer 17 from the surface of the p type semiconductor layer 5, and each feed

part 15 and 16 of the p lateral electrode 6 and the n lateral electrode 7 is exposed through the window hole 18 formed in the insulator layer 17, respectively. In order to electrically connect the feed parts 15 and 16 to the conductor 10 provided to the mounting board 8, the bump 19 of metal like solder or gold is provided. The metalized die 20 is inserted in the insulating layer 8a of the synthetic resin in the mounting board 8, and thermally conductive good adhesives are used as the filler 11 between LED chip 1 and the die 20. By this composition, heat dissipation from LED chip 1 is made good. The p lateral electrode 6 and the n lateral electrode 7 may be connected to the conductor 10 with electroconductive glue instead of providing the bump 19. Since there are more current routes between the p lateral electrode 6 and the n lateral electrode 7 conventionally like other composition mentioned above also by composition of this embodiment than composition, the homogeneity of the luminance of a luminescent surface can be improved.

[0055]What at least 1 side of the p lateral electrode 6 and the n lateral electrode 7 equips with a plurality of feed parts 15 and 16 among the embodiments mentioned above () [get blocked and] When two or more p lateral electrode 6 or two or more n lateral electrodes 7 control current by what is provided independently among each feed parts 15 and 16 to the luminance distribution of a luminescent surface to lessen a bias, it is possible to improve the homogeneity of the luminance in a luminescent surface further.

[0056]

[Effect of the Invention]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 1 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, Into the aforementioned main tip surface, parallel arrangement of at least one copy of p lateral electrode and n lateral electrode is carried out mutually, respectively, It is that by which p lateral electrode and n lateral electrode are alternately arranged towards crossing the part by which parallel arrangement was carried out in p lateral electrode and n lateral electrode, Since the portion which becomes the equal distance increases while the portion which opposes between p lateral electrode and n lateral electrode conventionally as compared with composition increases, as compared with composition, a bias decreases in distribution of the current density in a main tip surface conventionally, and the regularity of the luminance of a luminescent surface becomes high as a result.

[0057]Since invention of Claim 2 is arranged so that the part by which parallel arrangement was carried out may become at equal intervals in the aforementioned p lateral electrode and the aforementioned n lateral electrode in invention of Claim 1, According to there being many portions which become the equal distance between p lateral electrode and n lateral electrode, the homogeneity of the luminance of a luminescent surface can be improved more.

[0058]In invention of Claim 1, invention of Claim 3 at least about one side of the aforementioned p lateral electrode and the aforementioned n lateral electrode, On a main tip surface, it is not electrically connected, and there are few ratios of a portion that p lateral electrode and n lateral electrode are not parallel in a main tip surface, the bias of distribution of the current density in a main tip surface decreases, and the part by which parallel arrangement was carried out is excellent in the homogeneity of the luminance within a luminescent surface.

[0059]On invention of Claim 1, and in the aforementioned p lateral electrode and the aforementioned n lateral electrode in invention of Claim 4, It branches in the direction which crosses the part by which parallel arrangement was carried out, respectively, and a plurality of branches which are mutually parallel are formed, and the distance of p lateral electrode and n lateral electrode becomes at a short distance by a branch, and since the part which moreover opposes mutually increases, it excels in the homogeneity of the luminance within a luminescent surface.

[0060]Invention of Claim 5 is extended in invention of Claim 1 by the curled form by which parallel arrangement of at least one copy of a plurality of p lateral electrodes and n lateral electrode is mutually carried out into the aforementioned main tip surface, respectively, Towards crossing p lateral electrode and n lateral electrode toward the outside from the center of the part formed spirally, p lateral electrode and n lateral electrode are arranged alternately, the portion of p lateral electrode and n lateral electrode which opposes can be formed in the whole main tip surface, and the homogeneity of the luminance of a luminescent surface becomes high.

[0061]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 6 was formed on the substrate, Have p lateral electrode and n lateral electrode of every plurality which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, and conventionally as compared with composition. The current route of p lateral electrode and n lateral electrode can be distributed in a main tip surface, and it excels in the homogeneity of the luminance within a luminescent surface.

[0062]Invention of Claim 7 the distance between the electrodes connected to the semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode in invention of Claim 6, When it is made smaller than the distance between the electrodes connected to the semiconductor layer of electric conduction type of the same kind and between the electrodes connected to the semiconductor layer of electric conduction type of the same kind does not approach, it excels in the homogeneity of the luminance in a luminescent surface.

[0063]Invention of Claim 8 is that by which between the electrodes connected to the semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode is arranged at equal intervals in invention of Claim 7, The bias of the current density of the current which flows between p lateral electrode and n lateral electrode decreases, and it can improve the homogeneity of the luminance of a luminescent surface.

[0064]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 9 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, Since the aforementioned main tip surface is divided into a plurality of regions by one side with p lateral electrode and n lateral electrode, another side is arranged in each region, respectively and the opposing part of p lateral electrode and n lateral electrode increases more than composition conventionally in a main tip surface, it excels in the homogeneity of the luminance of a luminescent surface.

[0065]Invention of Claim 10 is formed so that aforementioned one of the aforementioned p lateral electrode and the aforementioned n lateral electrodes may cover the whole circumference, respectively and may surround each aforementioned region in invention of Claim 9, its bias of distribution of the current density between p lateral electrode and n lateral electrode decreases, and the homogeneity of the luminance of a luminescent surface becomes high.

[0066]In invention of Claim 9, invention of Claim 11 equips the linear part which aforementioned another side of the aforementioned p lateral electrode and the aforementioned n lateral electrodes provided to aforementioned one side with the linear portion by which parallel arrangement is carried out, and since there are many opposing parts of p lateral electrode and n lateral electrode, it is excellent in the homogeneity of the luminance in a luminescent surface.

[0067]The p type semiconductor layer and n type semiconductor layer by which invention of Claim 12 was formed on the substrate, It has p lateral electrode and n lateral electrode which were connected to the main tip surface which is an opposite side of a substrate in the p type semiconductor layer and the n type semiconductor layer, respectively, One side with p lateral electrode and n lateral electrode is arranged in the central part of a main tip surface, and since another side is arranged and the opposing part of p lateral electrode and n lateral electrode increases in a main tip surface as compared with composition conventionally in the form surrounding aforementioned one side, it excels in the homogeneity of the luminance of a luminescent surface.

[0068]Since as for invention of Claim 13 the aforementioned p lateral electrode and the aforementioned n lateral electrode are alternately arranged by nesting form and there are more opposing parts of p lateral electrode and n lateral electrode in a main tip surface conventionally in invention of Claim 12 than composition, the homogeneity of the luminance of a luminescent surface becomes high.

[0069]When it is arranged in invention of Claim 13 so that the aforementioned p lateral electrode and the aforementioned n lateral electrode may become at equal intervals, and the equal portion of the inter electrode distance between p lateral electrode and n lateral electrode increases, invention of Claim 14, The bias of distribution of current density decreases and it excels in the homogeneity of the luminance of a luminescent surface.

[0070]In invention of Claim 13 or Claim 14 invention of Claim 15, The aforementioned p lateral electrode and the aforementioned n lateral electrode are arranged concentrically, and it becomes possible to make substantially equal distance between the electrodes of p lateral electrode and n lateral electrode in the whole main tip surface, and excels in the homogeneity of the luminance in a luminescent surface.

[0071]In invention of Claim 13 or Claim 14 invention of Claim 16, The aforementioned p lateral electrode and the aforementioned n lateral electrode can be made into the similar shape of the peripheral shape of a main tip surface, an electrode can be formed to near the outer peripheral edge of a main tip surface, and luminance difference near the outer peripheral edge of a main tip surface and near a center can be lessened.

[0072]In invention of Claim 1, Claim 6, Claim 9, or Claim 12 invention of Claim 17, Since the arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has axial symmetry nature in the aforementioned main tip surface and symmetry is conferred upon arrangement of the electrode, the bias of distribution of current density can be reduced and it excels in the homogeneity of the luminance in a luminescent surface.

[0073]In invention of Claim 1, Claim 6, Claim 9, or Claim 12 invention of Claim 18, Since the arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface and symmetry is conferred upon arrangement of the electrode, the bias of distribution of current density can be reduced and it excels in the homogeneity of the luminance in a luminescent surface.

[0074]In invention of Claim 1, Claim 6, Claim 9, or Claim 12, while having 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface, the arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode invention of Claim 19, Since it has axial symmetry nature about two or more symmetrical lines and symmetry is conferred upon arrangement of the electrode, the bias of distribution of current density can be reduced and it excels in the homogeneity of the luminance in a luminescent surface.

[0075]In invention of Claim 1, Claim 6, or Claim 9 invention of Claim 20, Provide the feed part which supplies electric power to the aforementioned n lateral electrode and the aforementioned p lateral electrode, respectively, and it provides multiple feed parts of at least 1 side of n lateral electrode and p lateral electrode, The homogeneity of the luminance in a luminescent surface can be improved by controlling current between each feed parts to the luminance distribution of a luminescent surface to lessen a bias.

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[CLAIMS](#) [DETAILED DESCRIPTION](#)

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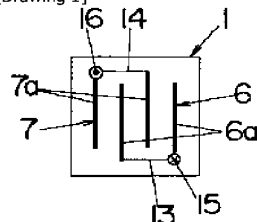
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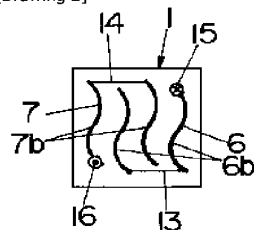
DRAWINGS

[Drawing 1]

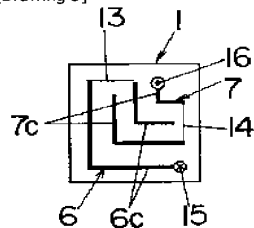


1 LEDチップ
6 p側電極
6a 直線部
7 n側電極
7a 直線部

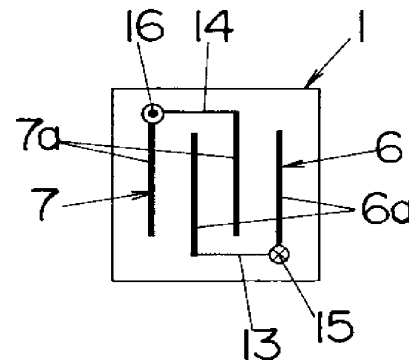
[Drawing 2]



[Drawing 3]



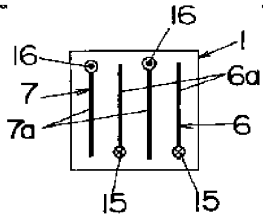
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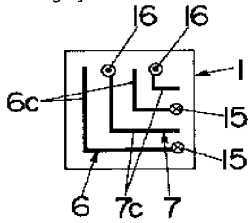
1 LEDチップ
6 p側電極
6a 直線部
7 n側電極
7a 直線部

Representative drawing

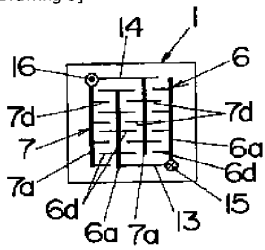
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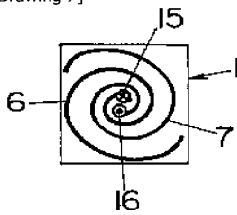
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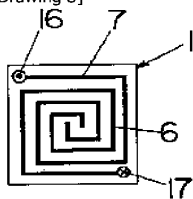
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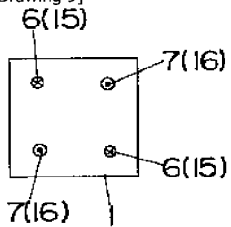
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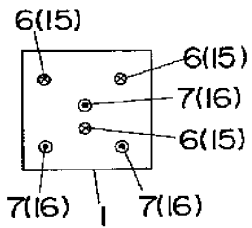
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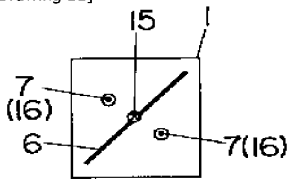
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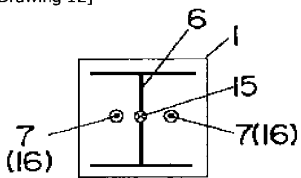
[Drawing 10]



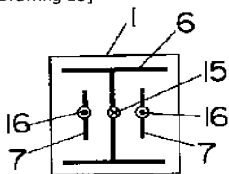
[Drawing 11]



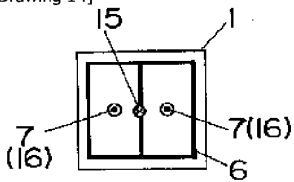
[Drawing 12]



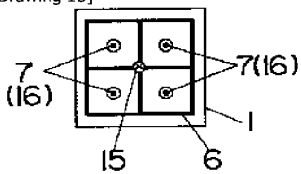
[Drawing 13]



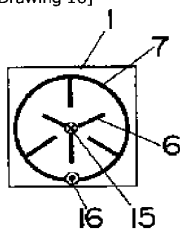
[Drawing 14]



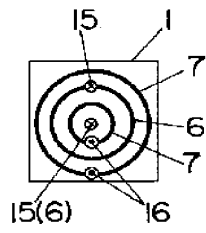
[Drawing 15]



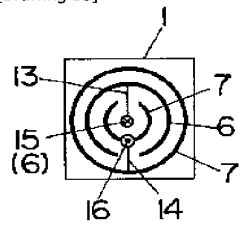
[Drawing 16]



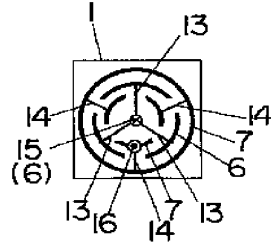
[Drawing 17]



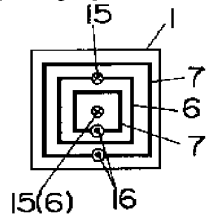
[Drawing 18]



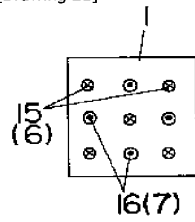
[Drawing 19]



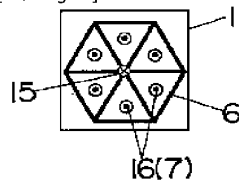
[Drawing 20]



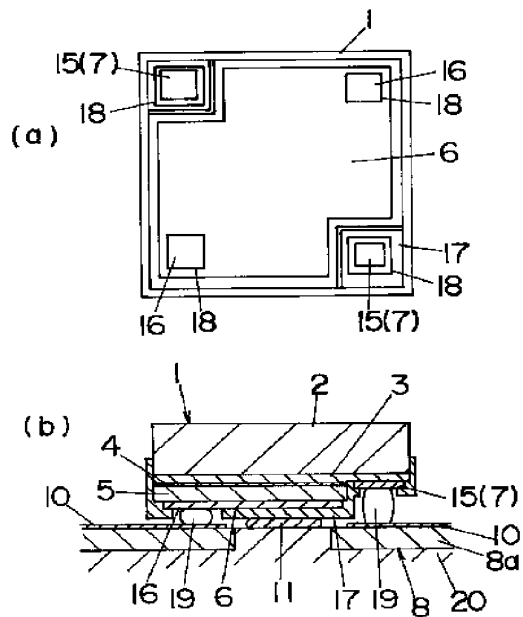
[Drawing 21]



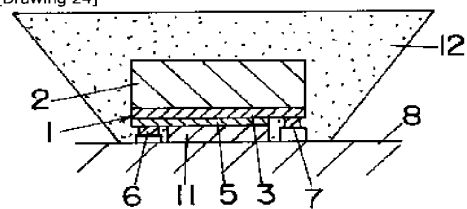
[Drawing 22]



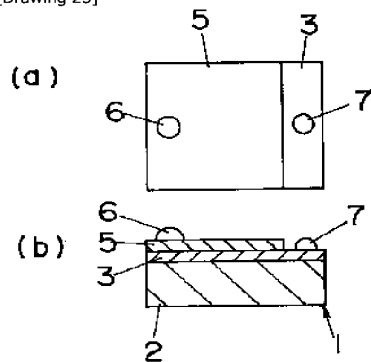
[Drawing 23]



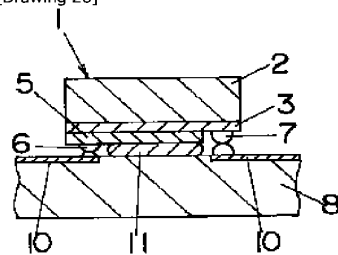
[Drawing 24]



[Drawing 25]



[Drawing 26]



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CLAIMS

[Claim(s)]

[Claim 1] An LED chip which it has the following, and parallel arrangement of at least one copy of p lateral electrode and n lateral electrode is mutually carried out into the aforementioned main tip surface, respectively, and is characterized by arranging p lateral electrode and n lateral electrode alternately towards crossing a part by which parallel arrangement was carried out in p lateral electrode and n lateral electrode.

A p type semiconductor layer and a n type semiconductor layer which were formed on a substrate.

p lateral electrode and n lateral electrode which were connected to a main tip surface which is an opposite side of a substrate in a p type semiconductor layer and a n type semiconductor layer, respectively.

[Claim 2] The LED chip according to claim 1 arranging so that a part by which parallel arrangement was carried out may become at equal intervals in the aforementioned p lateral electrode and the aforementioned n lateral electrode.

[Claim 3] The LED chip according to claim 1, wherein a part by which parallel arrangement was carried out is not electrically connected on a main tip surface at least about one side of the aforementioned p lateral electrode and the aforementioned n lateral electrode.

[Claim 4] The LED chip according to claim 1, wherein a plurality of branches which branch, respectively in the direction which crosses a part by which parallel arrangement was carried out in the aforementioned p lateral electrode and the aforementioned n lateral electrode, and are mutually parallel are formed.

[Claim 5] It is extended by curled form by which parallel arrangement of at least one copy of a plurality of p lateral electrodes and n lateral electrode is mutually carried out into the aforementioned main tip surface, respectively. The LED chip according to claim 1, wherein p lateral electrode and n lateral electrode are alternately arranged towards crossing p lateral electrode and n lateral electrode toward the outside from the center of a part formed spirally.

[Claim 6] An LED chip comprising:

A p type semiconductor layer and a n type semiconductor layer which were formed on a substrate.

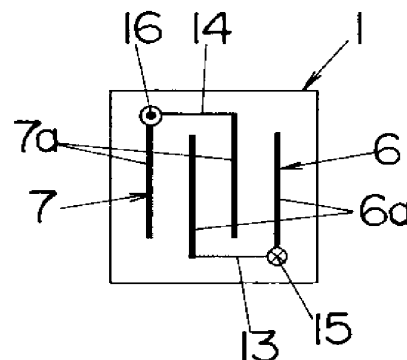
p lateral electrode and n lateral electrode of every plurality which were connected to a main tip surface which is an opposite side of a substrate in a p type semiconductor layer and a n type semiconductor layer, respectively.

[Claim 7] The LED chip according to claim 6 making smaller than distance between electrodes connected to a semiconductor layer of electric conduction type of the same kind distance between electrodes connected to a semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode.

[Claim 8] The LED chip according to claim 7, wherein between electrodes connected to a semiconductor layer of different-species electric conduction type among the aforementioned p lateral electrode and the aforementioned n lateral electrode is arranged at equal intervals.

[Claim 9] An LED chip which it has the following, and the aforementioned main tip surface is divided into a plurality of regions by one side with p lateral electrode and n lateral electrode, and is characterized by arranging another side in each region, respectively.

A p type semiconductor layer and a n type semiconductor layer which were formed on a substrate.



1 LEDチップ
6 p側電極
6a 直線部
7 n側電極
7a 直線部

Representative drawing

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p lateral electrode and n lateral electrode which were connected to a main tip surface which is an opposite side of a substrate in a p type semiconductor layer and a n type semiconductor layer, respectively.

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[Claim 10]The LED chip according to claim 9 forming so that aforementioned one of the aforementioned p lateral electrode and the aforementioned n lateral electrodes may cover the whole circumference, respectively and may surround each aforementioned region.

[Claim 11]The LED chip according to claim 9 equipping a linear part which aforementioned another side of the aforementioned p lateral electrode and the aforementioned n lateral electrodes provided to aforementioned one side with a linear portion by which parallel arrangement is carried out.

[Claim 12]An LED chip, wherein it has the following, one side with p lateral electrode and n lateral electrode is arranged in the central part of a main tip surface and another side is arranged in a form surrounding aforementioned one circumference.

A p type semiconductor layer and a n type semiconductor layer which were formed on a substrate.

p lateral electrode and n lateral electrode which were connected to a main tip surface which is an opposite side of a substrate in a p type semiconductor layer and a n type semiconductor layer, respectively.

[Claim 13]The LED chip according to claim 12, wherein the aforementioned p lateral electrode and the aforementioned n lateral electrode are alternately arranged by nesting form.

[Claim 14]The LED chip according to claim 13 arranging so that the aforementioned p lateral electrode and the aforementioned n lateral electrode may become at equal intervals.

[Claim 15]The LED chip according to claim 13 or 14, wherein the aforementioned p lateral electrode and the aforementioned n lateral electrode are arranged concentrically.

[Claim 16]The LED chip according to claim 13 or 14, wherein the aforementioned p lateral electrode and the aforementioned n lateral electrode are the similar shape of peripheral shape of a main tip surface.

[Claim 17]Claim 1, wherein an arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has axial symmetry nature in the aforementioned main tip surface, or the LED chip according to claim 6, 9, or 12.

[Claim 18]Claim 1, wherein an arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode has 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface, or the LED chip according to claim 6, 9, or 12.

[Claim 19]Claim 1 while an arrangement pattern of the aforementioned n lateral electrode and the aforementioned p lateral electrode having 2 times or more of symmetry-of-revolution nature in the aforementioned main tip surface, wherein it has axial symmetry nature about two or more symmetrical lines, or the LED chip according to claim 6, 9, or 12.

[Claim 20]The LED chip according to claim 1, 6, or 9 having provided a feed part which supplies electric power to the aforementioned n lateral electrode and the aforementioned p lateral electrode, respectively, and providing multiple feed parts of at least 1 side of n lateral electrode and p lateral electrode.

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KR1020060034872 A	US6838702 B1
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심사관 : 이진홍

(54) 엘이디 패키지 및 그 제조방법

요약

본 발명은 자동차를 비롯하여 휴대폰 또는 노트북컴퓨터 등의 소형 전기·전자제품에서 조명으로 사용되는 전구나 램프를 대체할 수 있고, 반도체 제조공정에 의해 저가로 생산이 가능하며, 기존의 램프형 엘이디와 표면실장형 엘이디에 비해 소형화 및 집적화가 가능하고, 방열성능이 우수하여 열적 안정성을 갖도록 함으로써 우수한 내구성을 갖도록 한 것인 바, 상면에 엘이디 소자의 안착을 위한 안착면(11)과 상기 안착면(11) 외곽에 대하여 소정각도로 제1경사면(12) 및 제2경사면(13)이 형성된 캐비티(C)와; 상기 안착면(11)에서 하면으로 관통된 복수의 비아 홀(14)을 갖는 실리콘 기판(10)과; 상기 실리콘 기판(10)의 제1경사면(12)과 제2경사면(13)상에 형성되는 반사층(20)과; 상기 실리콘 기판(10)의 비아 홀(14)에 설치되는 금속 플러그(30)와; 상기 실리콘 기판(10)의 안착면(11)에 안착되며 P 전극과 N 전극이 상기 금속 플러그(30) 상에 본딩되는 엘이디 소자(40)와; 상기 실리콘 기판(10)에 부착되어 엘이디 소자(40)를 보호하고 엘이디 소자(40)에서 방출된 빛을 집속하여 엘이디 소자(40)에서 방출된 빛이 소정의 발산각 이내로 전파되도록 하는 렌즈(60);를 포함하여 이루어지는 엘이디 패키지 및 그 제조방법을 제공한다.

배경도

도 5

색인어

엘이디(LED), 패키지, 반도체, 표면실장, 실리콘

명세서

도면의 간단한 설명

- 도 1은 종래 엘이디 패키지의 일례를 도시한 사시도,
 도 2는 보텀 에미팅형 엘이디 소자의 단면도,
 도 3은 종래 엘이디 패키지의 다른 예를 도시한 사시도,
 도 4는 종래 엘이디 패키지의 또 다른 예를 도시한 단면도,
 도 5는 본 발명의 일 실시 예에 의한 엘이디 패키지의 구조를 도시한 단면도,
 도 6은 본 발명에 의한 엘이디 패키지의 제조공정도,
 도 7은 본 발명에 의한 엘이디 패키지의 제조공정 중 실리콘 기판의 제조과정을 순차적으로 도시한 단면도,
 도 8은 완성된 실리콘 기판 위에 엘이디 소자가 본딩된 상태를 도시한 단면도,
 도 9는 엘이디 소자 위에 형광체가 씌워진 상태를 도시한 단면도,
 도 10은 형광체 위에 렌즈가 캡핑된 상태를 도시한 단면도,
 도 11은 보조 기판의 사시도,
 도 12는 도 11에 도시된 보조 기판의 저면부 사시도,
 도 13은 본 발명의 다른 실시 예에 의한 엘이디 패키지의 단면도이다.

* 도면의 주요부분에 대한 부호의 설명

- 10 : 실리콘 기판 11 : 안착면
 12 : 제1경사면 13 : 제2경사면
 14 : 비아 홀 20 : 반사층
 30 : 금속 플러그 40 : 엘이디 소자
 50 : 형광체 60 : 렌즈
 70 : 보조 기판 72 : 회로패턴(금속단자)
 74 : 뱀프 B : 솔더 뱀프
 C : 캐비티 D : 식각 보호막
 E : 전기 절연막 F : 포토레지스트
 M : UBM 금속층 P : 패드
 P' : 와이어본딩 패드 Q : 와이어

W : 식각창

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 엘이디 패키지에 관한 것으로, 상세히는 자동차를 비롯한 각종 운송수단에서부터 휴대폰 또는 노트북 컴퓨터 등의 소형 전기·전자제품에 이르기까지 조명용으로 사용되는 전구나 램프형 엘이디를 대체할 수 있는 조명용 엘이디 패키지로써, 반도체 제조공정에 의해 저렴한 비용으로 생산이 가능하고, 기존의 램프형 엘이디나 표면실장형 엘이디에 비해 소형화 및 집적화가 가능하며, 방열성능이 우수하여 열적 안정성을 갖도록 함으로써 우수한 내구성을 갖도록 한 것이다.

엘이디(LED; Light Emitting Diode) 즉, 발광다이오드는 주입된 전자와 정공이 재결합할 때 과잉의 에너지를 빛으로 방출하는 다이오드로써, GaAsP등을 이용한 적색 발광다이오드, GaP 등을 이용한 녹색 발광다이오드, InGaN/AlGaIn 다블헤테로 구조를 이용한 청색 발광다이오드 등이 있다.

한편, RGB 엘이디 소자의 조합 또는 형광체를 이용하여 청색 혹은 UV 엘이디로부터 백색광을 생성하는 기술이 개발되면서 단순 발광표시기능 외에 기존의 전구나 형광등 등을 대체할 있는 조명분야와 LCD 디스플레이 장치의 백 라이트 등으로 응용범위가 확장되고 있고, 이를 위한 고휘도 엘이디 개발이 활발히 진행되고 있다.

엘이디 소자의 패키지 형태는 램프형과 표면실장형의 2가지가 있는데, 램프형은 2개의 리드 프레임 중 하나의 리드 프레임 상부에 컵 형상으로 일정한 각을 갖는 금속전극면이 구비되고 그 상부에 엘이디 소자가 실장되며, 그 위에 몰딩된 렌즈가 씌워진 구조로 이루어져 있다. 이러한 램프형 엘이디는 엘이디 소자와 패키지 케이스 간의 열 저항이 크고 패키지의 하부에 히트싱크를 부착하기 어려운 구조로 되어 있기 때문에 고출력용 발광 다이오드에 적용하는데 한계가 있다.

한편, 표면실장형 엘이디는 세라믹 등의 기판 위에 다이 본딩되며 몰딩 에폭시수지로 이루어진 패키지를 가지며, 외형각이 적은 실장영역에 엘이디 소자가 배치되고 와이어로 전극과 연결되는 구조로 이루어져 있다. 표면실장형 엘이디는 열방출이 용이하기 때문에 고출력 엘이디 패키지로써 널리 사용된다.

도 1에 제시된 바와 같은 종래의 표면실장형 엘이디 패키지(대한민국 특허공개 제2003-0053853호)는 엘이디 소자(105)의 실장영역이 형성된 상면을 가지며, 그 실장영역을 중심으로 소정의 도전성 패딩이 형성된 제1세라믹기판(101)과, 이 제1세라믹기판(101) 상면의 실장영역에 배치되어 소정의 도전성 패딩과 연결된 적어도 하나의 엘이디 소자(105)와, 제1세라믹기판(101) 상에 배치되며 엘이디 소자(105)의 실장영역에 상응하는 영역에 캐비티가 형성된 제2세라믹기판(102)과, 엘이디 소자(105)를 둘러싸도록 제2세라믹기판(102)의 캐비티 내에 부착되는 금속반사판(120)을 포함하여 이루어져 있고, 이 금속반사판(120)은 그 상단직경(R)이 하단직경(r)보다 큰 원통형상으로 이루어져 상,하단직경(R,r)의 차이에 의해 형성되는 측면경사각을 변경하는 것에 의해 엘이디 소자(105)의 휘도각 분포를 조절하고, 금속반사판(120)의 면적이나 소재 및 표면코팅을 달리하여 엘이디 소자(105)의 휘도를 조절할 수 있도록 된 것이다.

이와 같은 종래의 표면실장형 엘이디 패키지는 휘도 및 휘도각 조절을 위한 적정 각도를 갖는 경사면(막)을 형성하는 방법 이 세라믹 기판을 기계적인 편칭이나 절단 등에 의해 이루어지고, 그 편칭면이나 절단면에 금속층을 코팅하거나 별도의 금속재 반사판(컵)을 부착하는 구조로 이루어져 있었으므로 기계적인 가공의 한계로 인하여 소형화가 어렵고 수율이 낮아 제조코스트가 높은 문제점을 가지고 있다.

한편, 위에서 언급된 종래의 표면실장형 엘이디 패키지는 내부에 실장된 엘이디 칩과 외측의 기판 사이에 두개의 본딩 와이어를 통해 리드프레임과 전기적인 연결이 이루어지는 구조로 되어 있어 제조공정의 단순화를 도모하는데 지장이 있을 뿐만 아니라 제품의 소형화와 발광효율의 증대에도 한계가 뒤따르게 되었다.

이러한 종래의 엘이디의 단점을 보완하기 위하여 최근에 개발된 것으로 도 2 에 도시된 바와 같이 엘이디 소자의 P극과 N 극의 전극이 모두 소자의 발광면 상에 위치하는 보텀 에미팅(Bottom emitting)형 엘이디 소자가 개발되었다. 보텀 에미팅형 엘이디는 엘이디의 활성층에서 생성된 빛이 투명한 사파이어 기판을 통하여 직접 외부로 방출되기도 하지만, 일부 기판

하부를 향하여 방출된 빛도 소자의 표면에 형성된 P극과 N극용 금속층에서 반사되어 다시 외부로 방출하게 된다. 이와 같은 보텀 에미팅형 엘이디는 발광효율이 톱 에미팅(Top emitting) 소자보다 상대적으로 높기 때문에 고휘도 엘이디 장치에서 많이 사용된다.

상기와 같은 보텀 에미팅 엘이디 소자는 소자의 구조상 소자의 활성층과 소자의 전극이 위치하는 앞면을 뒤집어서 플립칩 본딩하는 것이 필요하다.

미국공개특허 US 2002/0070386 A1에 따르면 엘이디 소자의 발광 효율을 향상시키기 위하여 엘이디 소자의 전면에 P 전극과 N 전극에 대응하는 금속패드 혹은 금속패드와 솔더범프를 구비하고, 실리콘 서브마운트 상에 엘이디 칩의 플립칩 본딩을 위한 솔더 범프를 구비하여, 엘이디 소자를 상기 서브마운트 위에 플립칩 본딩하는 것으로 1차 패키징을 완성한다. 여기서 실리콘 서브마운트는 엘이디 다이와 패키지를 전기적으로 그리고 열적으로 연결시키는 역할과 함께 추가적으로 전압순응제한(voltage-compliance limiting)작용과 같은 전자적(electronic) 기능도 제공한다.

도 3은 미국특허 공보 US6,642,550에서 제시된 또 다른 실리콘 서브마운트의 활용 예를 나타낸 것이다. 상기 발명의 일 실시 예에 따르면 엘이디 배치(200)는 플라스틱 벌브와 같은 투광성 패키지(250)로 밀봉된 엘이디 칩(210)으로 구성되고, 패키지(250)는 두개의 독립된 전기적인 커넥트, 즉 양극(230)과 음극(240)으로 구성된 리드프레임의 일부를 에워싸고 있고, 엘이디 칩(210)은 단수의 와이어 본딩이 가능한 실리콘 서브마운트(280)의 상부에 배치된 솔더 범프들(270) 위에 연결되며, 상기 엘이디 칩(210)은 엘이디 칩의 접촉 패드들(contact pads)이 솔더 범프와 정렬 및 연결되도록 배치된다.

상기 실리콘 서브마운트(280)는 상층부(283)와 하층부(285)로 불리는 두개의 기능적 영역을 가지는데 상층부(283)의 일부는 표면의 반사도를 좋게하기 위해 Al 금속으로 증착된다. 상기 Al 표면의 소정 영역에 솔더범프(270)가 형성되고 ESD (electrostatic discharge) 보호회로(281)가 내장된다. 상기 서브마운트의 하층부(285)에 Au 등의 금속층이 형성되고, 상기 실리콘 서브마운트(280)의 상층부(283)와 하층부(285)를 전기적으로 연결시키기 위한 상기 서브마운트(283)를 관통하는 인터커넥션(260)을 형성한다. 엘이디 칩(210)의 P 및 N 전극 패드를 상기 실리콘 서브마운트 상층부(283) 표면의 솔더범프(270)와 연결하고 리드프레임의 양극(230)과 서브마운트의 상층부(283)를 와이어 본딩(220)하여 전기적으로 연결하고, N극(240)은 실리콘 서브마운트(280)를 관통하는 인터커넥션(260)에 의해 하층부(285)로 연결된다. 이와 같이 실리콘 서브마운트(280)를 관통하는 인터커넥션(260)을 이용함으로써 리드프레임(230, 240)과 엘이디 칩(210) 사이의 와이어 본딩을 한번으로 줄일 수 있는 이점을 가진다.

상기와 같은 실리콘 서브마운트는 엘이디 소자의 부착을 위한 기관으로서의 기능과 동시에 ESD 보호 소자의 내장, 나아가 엘이디 장치의 구동에 필요한 집적회로를 직접 내장할 수 있는 이점을 제공한다.

한편, 실리콘의 MEMS 가공기술을 보다 적극적으로 활용한 실리콘 서브마운트는 상기한 기능 외에 엘이디 소자에서 방출된 빛을 집속하는 캐비티의 기능을 제공할 수 있고 동시에 실리콘 반도체 제조기술이 가진 양산성과 집적화 기능 그리고 웨이퍼 레벨 패키징 기술의 활용 등 부수적인 이점을 얻을 수 있다.

도 4는 이와 같은 취지의 종래의 기술의 일 예를 나타낸 것이다(미국특허번호 US6,531,328 B1). 상기 발명의 일 실시예에 따르면 (100) 혹은 (110) 실리콘 기관의 표면에 54.74°로 기울어진 벽(312)을 가진 홈(311)과, 상기 기관의 배면에 건식 식각을 이용하여 형성된 스루홀(314)과, 상기 기관의 표면에 형성된 SiO₂ 혹은 Si₃N₄의 전기적 절연막(315)과, 상기 기관의 상, 하면과 스루홀(314) 내부에 도금된 금속층(316)을 구비하는 실리콘 기관(308)이 제공된다. 상기 발명의 일 실시예에 따른 엘이디 패키징은 상기 실리콘 기관(308)의 홈(311) 내의 전극 위에 엘이디 칩(303)을 놓는 과정; 전극을 연결하기 위하여 본딩 금속 와이어(304)를 연결하는 과정; 인캡슐레이팅 레진(305)을 충전하는 과정; 그리고 마지막으로 절단선(320)을 따라서 절단하는 과정으로 완성된다.

도 4에 예시한 종래의 발명은 엘이디 소자로부터 방출된 빔을 효과적으로 엘이디 칩 상부의 렌즈로 전달하기 위한 목적으로 사용되는 캐비티를 실리콘 서브마운트에 내장함으로써 별도의 캐비티를 사용하는 것에 비해 패키지의 크기와 부품 수 그리고 조립 공수를 줄일 수 있는 이점을 제공한다.

그러나 도 4에 예시한 종래의 발명에 따르면 캐비티를 구성하는 경사면의 각도가 54.74° 이거나 90°로 제한된다. 엘이디 소자로부터 방출된 빔을 효과적으로 그 상부의 렌즈로 전달하기 위한 목적의 캐비티는 엘이디의 용도, 칩의 크기, 특히 캐비티의 깊이에 상대적인 칩의 두께, 렌즈의 사용 유무 및 사용하는 렌즈의 종류에 따라서 각각 최적의 경사각이 달라져야 한다. 따라서 경사면의 각도가 특정한 각도로 제한된 경우에는 그 활용범위가 매우 제한적일 수 밖에 없는 단점이 있다.

또한, 도 4에 예시한 종래의 발명에 따르면 광학적인 작용을 담당하는 반사층과 전기적인 작용을 담당하는 전극층을 Ag, Au, Pd, Pt 등으로 구성된 금속층으로 동시에 형성한다. 그러나 반사층은 최적의 반사효율을 제공하는 금속 혹은 유전체 막막으로 제조될 필요가 있고 동시에 전극층은 전기적인 전극으로서 요구되는 전기적인 특성과, 특히 엘이디 칩을 플립칩 본딩할 경우에는 솔더범프 하부의 UBM(under bump metallurgy)으로서 요구되는 제반 구성요소, 즉 접착층, 확산방지층, 그리고 산화방지층과 각 구성요소로서 요구되는 제반 특성들을 충분히 제공하는 물질로 구성되어야 할 필요가 있다. 따라서 도 4에 예시한 종래의 발명에 따라서는 반사층과 전극층의 요구조건을 동시에 충분히 만족시키기 어렵다. 또 한편으로 실리콘 기판을 관통하는 스루홀을 채우는 재료는 엘이디 패키지의 전력소모는 낮추는 동시에 열방출을 효과적으로 수행하기 위하여 낮은 전기적 저항과 높은 열전도도를 갖는 물질이 요구됨에도 불구하고 도 4의 종래의 발명은 이에 대한 효과적인 수단을 제공하고 있지 못하고 있다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기한 종래의 제반 문제점을 해소하기 위하여 안출된 것으로, 본 발명의 한 가지 목적은 반도체 제조공정을 통하여 생산이 가능한 표면실장형 엘이디 패키지와 그 제조방법을 제공하는 데 있다.

본 발명의 다른 목적은 엘이디 패키지의 기판으로서 두 가지의 서로 다른 경사각을 가진 캐비티를 구비한 실리콘 기판을 제공하는 데 있다.

본 발명의 다른 목적은 상기 캐비티의 측벽에 엘이디 소자에서 방출된 빛을 효과적으로 반사할 수 있는 금속 혹은 유전체 막막을 제공한다.

본 발명의 다른 목적은 엘이디 소자의 플립칩 본딩에 필요한 효과적인 UBM 금속과 솔더 범프를 제공한다.

본 발명의 다른 목적은 엘이디 소자의 전극을 실리콘 기판의 하부로 연결하기 위하여 실리콘 기판을 관통하는 비아 홀을 형성하고 상기 비아홀을 낮은 전기저항과 높은 열전도도를 가진 Cu 등의 금속으로 채워 낮은 전기적 저항과 높은 열전도도를 가진 연결을 제공한다.

본 발명의 다른 목적은 상기 실리콘 기판을 히트 싱크 혹은 PCB에 실장하는데 필요한 전극패턴과 솔더 범프를 제공한다.

본 발명의 또 다른 목적은 엘이디 소자를 패키징 하는데 있어 엘이디 칩의 다이 본딩 또는 플립칩 본딩, 형광체의 적용, 인캡슐란트의 적용, 렌즈의 몰딩 또는 부착 등 엘이디 소자의 패키징 공정의 대부분이 웨이퍼 레벨에서 패키징이 가능한 웨이퍼 레벨의 엘이디 패키징 기술을 제공하는 것이다.

이와 같은 목적을 달성하기 위하여 본 발명은 상면에 엘이디 소자가 안착되는 안착면과 상기 안착면 외곽에 대하여 소정각도로 제1경사면 및 제2경사면을 갖는 캐비티가 형성되고, 상기 안착면에서 하면으로 관통된 복수의 비아 홀을 갖는 실리콘 기판과; 상기 실리콘 기판의 제1경사면과 제2경사면 상에 형성되는 반사층과; 상기 실리콘 기판의 비아 홀에 설치되는 복수의 금속 플러그와; 상기 실리콘 기판의 안착면에 안착되며 P와 N 전극이 금속 플러그에 본딩되는 엘이디 소자와; 상기 엘이디 소자 위에 도포되는 형광체와; 상기 실리콘 기판 위에 본딩되어 반도체 내부의 형광체를 커버하는 렌즈;를 포함하여 이루어지는 엘이디 패키지를 제공한다.

본 발명은 또, 상기한 엘이디 패키지를 제조하기 위한 방법으로, 실리콘 기판 상에 엘이디 소자의 안착을 위한 안착면과 이 안착면 외곽에 대하여 소정각도로 제1경사면 및 제2경사면을 갖는 캐비티를 형성하는 실리콘 기판 가공공정; 상기 제1경사면 및 제2경사면에 반사층을 코팅(증착)하는 공정; 상기 실리콘 기판의 하면에서 안착면까지 비아 홀을 형성하고, 이 비아 홀에 금속 플러그를 형성하는 공정; 엘이디 소자를 상기 캐비티 내의 안착면에 실장하는 공정; 엘이디 소자가 실장된 실리콘 기판 위에 형광체를 코팅하는 공정; 렌즈를 실리콘 기판 위에 캡핑(본딩)하는 공정;을 포함하는 엘이디 패키지 제조방법을 제공한다.

발명의 구성 및 작용

이하, 본 발명을 한정하지 않는 바람직한 실시 예를 첨부된 도면에 의하여 상세히 설명하기로 한다.

도 5는 본 발명의 일 실시 예에 따른 엘이디 패키지의 구조를 도시한 단면도이고 도 6은 본 발명의 일 실시 예에 따른 패키지의 제조공정도, 그리고 도 7은 본 발명의 일 실시 예에 따른 엘이디 패키지의 제조과정 중 실리콘 기판의 제조과정을 순차적으로 도시한 단면도이다.

도 5 내지 도 7에서와 같이, 본 발명의 엘이디 패키지는 상면에 엘이디 소자 안착을 위한 안착면(11)과; 상기 안착면(11) 외곽에 대하여 소정각도로 제1경사면(12) 및 제2경사면(13)을 갖는 캐비티(C)가 형성되고, 상기 안착면(11)에서 하면으로 관통된 복수의 비아 홀(14)을 갖는 실리콘 기판(10)과; 상기 실리콘 기판(10)의 제1경사면(12)과 제2경사면(13)상에 형성되는 반사층(20)과; 상기 실리콘 기판(10)의 비아 홀(14)에 설치되는 복수의 금속 플러그(30)와; 상기 실리콘 기판(10)의 안착면(11)에 안착되며 P 및 N 전극이 금속 플러그(30)에 본딩되는 엘이디 소자(40)와; 상기 엘이디 소자(40) 위에 도포되는 형광체(50)와; 상기 실리콘 기판(10)에 부착되어 엘이디 소자(40)에서 방출된 빛을 집속하는 렌즈(60);를 포함하여 이루어져 있다.

도 5에 도시된 실시 예에서 본 발명의 엘이디 패키지는 보조 기판(70)상에 부착되는데, 이는 하부로 노출된 금속 플러그(30)가 보조 기판(70)의 상면에 형성된 회로패턴(72)에 솔더링 되어 이루어진다.

본 발명의 바람직한 실시 예에서 상기 반사층(20)은 복수의 금속층으로 이루어지는데, 그 최하층은 실리콘 혹은 실리콘 질화막 또는 실리콘 산화막 등과 접착성이 좋은 Ti, Cr 등으로 이루어지고, 최외곽(상부)층은 엘이디에서 방출된 빛에 대한 반사도가 높은 Ag, Au, Al 등으로 구성된다. 경우에 따라서는 상기 반사층은 금속 대신 복수 층의 유전체로 구성된 박막을 사용하여도 무방하다. 또, 경우에 따라서는 상기 하층과 상층 사이에 제3혹은 제4의 금속 박막을 삽입하여도 무방하다.

본 발명에서 상기 금속 플러그(30)는 엘이디 소자(40)의 P극과 N극을 각각 외부와 전기적으로 연결하기 위한 것으로, Cu, Au 등 전기전도성이 우수한 금속재질을 도금하여 사용한다.

상기 엘이디 소자(40)는 도 4에 도시된 바와 같이 P극과 N극이 소자의 상부, 즉 빛을 생성하는 활성층이 위치한 표면에 위치하는 보텀 에미팅 타입의 엘이디 소자로서 플립칩 방식으로 실리콘 기판상에 부착된다.

상기 형광체(50)는 청색 혹은 UV 빛을 받아서 그 보다 에너지가 낮은 적색과 녹색의 빛을 생성하는 화학재료로서 통상적으로 형광체를 이용하는 백색광 생성장치에 사용되는 것이다.

상기 렌즈(60)는 엘이디 소자(40)에서 방출된 빔을 집속하여 소정의 발산각 이내에서 대부분의 빛이 전파되도록 하는 역할을 한다.

도 5에 도시된 일 실시 예에서 상기 보조 기판(70)은 실리콘 기판(10)을 직접 도시안된 PCB 기판이나 방열판 상에 부착하기 곤란한 경우 혹은 보다 견고한 기계적인 강도가 요구되는 경우에 사용한다.

도 6은 본 발명에 의한 엘이디 패키지의 제조공정도로서, 실리콘 기판(10) 상에 엘이디 소자(40)의 안착을 위한 안착면(11)과 이 안착면(11) 외곽에 대하여 소정각도로 제1경사면(12) 및 제2경사면(13)을 갖는 캐비티(C)를 형성하는 실리콘 기판 가공공정(S1);

상기 제1경사면(12) 및 제2경사면(13)에 반사층(20)을 코팅(증착)하는 공정(S2);

상기 실리콘 기판(10)의 하면에서 안착면(11)까지 비아 홀(14)을 형성하고, 상기 비아 홀(14)에 금속 플러그(30)를 도금하는 공정(S3);

엘이디 소자(40)를 상기 캐비티(C)내의 안착면(11)에 실장하는 공정(S4);

엘이디 소자(40)가 실장된 실리콘 기판(10) 위에 형광체(50)를 코팅하는 공정(S5); 및 렌즈(60)를 실리콘 기판(10) 위에 캡핑(본딩)하는 공정(S6);으로 이루어져 있다.

이하에서는 상기한 제조공정(S1~S6)에 대하여 보다 구체적으로 설명하기로 한다.

도 7은 본 발명에 의한 엘이디 패키지의 제조과정 중 실리콘 기판(10)의 제조공정(S1~S3)을 순차적으로 도시한 단면도이다.

도 7에 도시된 바와 같이 실리콘 기판(10)은 (100) 결정면을 가진 실리콘 웨이퍼로서 LPCVD, Thermal Oxidation 혹은 PECVD법 등으로 각각 실리콘 질화막(Si_3N_4), 실리콘 산화막(SiO_2), 혹은 non-stoichiometric 실리콘 질화막(SiNX) 등으로 식각 보호막(D)을 형성한다(S11).

이어서 상기 실리콘 기판(10)의 상부에 사진전사공정과 건식 식각공정을 통하여 캐비티가 형성될 부위의 식각 보호막(D)을 제거한다(S12). 이때 상기 식각패턴은 (100) 실리콘 웨이퍼의 <110> 결정방향과 나란하게 정렬한다.

다음으로, KOH(potassium hydroxide), TMAH(Tetramethyl ammonium hydroxide), EDP(Ethylenediamine-pyrocatechol) 등의 이방성 실리콘 식각용액으로 실리콘 기판을 식각하여 캐비티(C; cavity)와 안착면(11)을 형성한다(S13).

식각된 캐비티(C; cavity)의 형태는 아래가 잘린 직사각형의 피라미드 모양이 되고, 이때 캐비티(C)의 내측벽(12; 이하에서는 "제1경사면"이라함)이 실리콘 기판(10)의 표면과 이루는 각도는 (100) 실리콘 웨이퍼의 결정구조에 의해 약 54.7° 로 결정된다. 이어서 실리콘 기판(10)의 표면에 형성된 실리콘 질화막 또는 실리콘 산화막의 식각 보호막(D)을 습식 혹은 건식 식각법으로 모두 제거한다(S14).

이어서, 식각 마스크가 없는 상태에서 KOH, TMAH 혹은 EDP 등의 이방성 실리콘 식각용액으로 소정 깊이만큼 식각하면 원래 형성된 캐비티(C)의 제1경사면(12)의 상측 일부에 실리콘 기판(10)의 표면과 이루는 각도가 제1경사면(12)의 경사각과 다른 새로운 제2경사면(13)이 형성된다(S15). 이와 같은 현상은 Drago Resnik 등의 논문에서 제시되어 있다(Drago Resnik et al, J. Micromech. Microeng. 10 (2000) 430-439).

이 제2경사면(13)은 결정확상으로는 (311) 면으로서 기판 표면과 이루는 각도는 약 25° 가 되지만, 실제로는 여러 가지 요인에 의해 약 $20\sim 35^\circ$ 의 완만한 각도를 이루게 된다. 또한, 이때 두 번째 식각 시간을 조절하면 제1경사면(12)과 제2경사면(13)이 차지하는 비를 조절 할 수 있고, 이와 같이 함으로써 두 개의 경사면이 합해진 유효한 경사각을 조절할 수 있다.

다음으로는 단계(S21)에서와 같이 캐비티(C)가 형성된 실리콘 기판(10)의 상부 표면에 전기 절연막(E)으로 실리콘 질화막 또는 실리콘 산화막 등을 소정 두께로 형성한다.(S21)

이어서, 단계(S22)에서와 같이 포토레지스트(F)를 웨이퍼의 전면에 도포한 다음에 캐비티(C) 내부의 소정의 영역에 엘이디 소자의 플립칩을 위한 UBM 금속층 및 솔더 범프를 형성하기 위하여 사진전사공정으로 UBM 금속층과 솔더 범프가 형성될 부위의 상기 포토레지스트(F)를 제거한다. 그 다음, 단계(S23)에서와 같이 UBM 금속층(M)과 솔더 범프(B) 물질을 차례로 증착하고 아세톤 등으로 UBM 금속층(M)과 솔더 범프(B) 하부의 포토레지스트(F)를 제거하여 UBM 금속층(M)과 솔더 범프(B)를 형성한다.

바람직한 UBM 금속층(M)으로는 Ti/Ni/Au, Cr/Ni/Au, Cr/Cr-Cu/Cu/Au 등 통상적으로 전자소자 및 광반도체 소자에 적용되는 UBM 금속층이 바람직하고, 솔더 범프(B) 재료로는 Au, Au/Sn, Sn/Pb, Sn/Ag 등 역시 통상적으로 전자소자 및 광반도체 소자에 적용되는 솔더 범프 재료가 사용된다. 더욱 바람직하게는 후락스(flux)의 사용 없이 리플로우가 가능한 Au 및 Au/Sn 등이 바람직하다.

한편 상기 UBM 패턴과 솔더 범프 패턴이 형태와 면적에 있어서 서로 상이할 필요가 있을 경우에는 상기한 UBM과 솔더범프의 형성공정과 동일한 방법으로 UBM 패턴과 솔더범프 패턴을 각각 형성 하는 것도 가능하다. 또한 상기 솔더범프 재료로서 Au를 사용할 경우에는 (S22) 단계에서 범프를 형성하지 않고 기판 공정이 완료된 후 엘이디 소자를 플립칩 하기 전에 스티드 범핑법으로 범프를 형성하는 것도 무방하다. 또 한편으로, UBM 패턴의 형태는 엘이디 소자의 P극과 N극과 각각 연결될 UBM 패턴이 서로 전기적으로 단락되지 않으면서 가장 넓은 면적을 차지한다는 기본적인 취지에 따른 어떤 형태의 것도 무방하다. 여기에서 가장 넓은 면적을 차지한다는 취지는 엘이디 소자의 하부에 형성된 금속층이 엘이디 소자에서 방출된 빛을 효율적으로 반사시키기 위한 것이고, 또 다른 한편으로는 엘이디 소자에서 발생된 열을 효과적으로 외부로 전달하기 위한 것이다.

마찬가지로 솔더 범프의 수 역시 P극과 N극에 대해 각각 복수로 나누지 않고 P극과 N극에 대해 각각 하나로 하여도 무방하다. 더 나아가서 UBM과 솔더 범프의 형태는 P극과 N극이 전기적으로 단락되지 않는 한도 내에서 어떠한 형태를 가져도 무방하다. 상기 솔더 범프의 높이는 본딩의 용이성과 기계적 강도 등을 고려하여 수 μm 내지 수십 μm 높이로 한다.

다음에 도 7의 단계(S24)에서와 같이 캐비티(C)의 제1,2경사면(12,13)을 거울면으로 만들기 위하여 사진전사공정과 금속의 증착 혹은 도금을 통하여 캐비티(C)의 측벽에 반사층(20)을 형성한다. 상기 반사층(20)의 재료는 Ti/Al, Cr/Al, Cr/Ag, Ti/Ag 등의 금속 다층막이 바람직하며, 이때, 최하층은 상부 금속과 기판 간의 접착을 좋게 하는 물질이 바람직하고, 상부 금속은 엘이디 소자의 발광영역의 파장의 빛에 대한 반사도가 좋은 Ag, Au, Al 등의 금속이 바람직하다. 경우에 따라서는 금속 박막 대신에 복수 층의 유전체를 사용한 반사막을 사용하여도 무방하다.

다음 공정으로, 도 7의 단계(S31)에서와 같이 상기한 공정을 거친 실리콘 기판(10)을 뒤집어서 뒤집어진 실리콘 기판(10)의 표면에 사진전사공정과 건식식각을 통하여 실리콘 기판(10) 자체의 식각을 위한 식각창(W)을 형성하고, 단계(S32)에서와 같이 깊은 실리콘 식각(Deep Si RIE) 혹은 습식식각을 통하여 식각된 바닥면이 하부의 UBM 금속층(M)과 만날 때까지 식각하여 비아 홀(14)을 형성하며, 단계(S33)에서와 같이 이 비아 홀(14)에 Cu, Au, 솔더 등의 금속재료를 도금하여 채워 넣어 금속 플러그(30)를 형성한다.

상기한 도금을 전해 도금방식으로 할 경우에는 도금에 필요한 하지금속(Base metal)막을 실리콘 기판(10)의 전면과 비아 홀(14) 내부에 스프터링을 통하여 형성한다. 상기 금속 플러그(30)가 형성된 상태에서 상기 도금층이 상기 기판(10)의 표면에 지나치게 돌출될 경우에는 연마를 통하여 이 돌출부를 제거하는 것이 바람직하다.

이어서, 단계(S34)에서와 같이 상기 실리콘 기판(10)의 표면에 엘이디 소자의 전극과 연결될 수 있는 전극 패드를 형성하기 위하여, 일 측은 상기 금속 플러그(30)와 연결되고 타 측은 금속 플러그(30)의 외곽으로 전개된 패드(P)를 형성한다.

만약 상기 실리콘 기판(10)이 여타의 또 다른 기판상에 부착되고 그 기판이 상기와 같은 P극과 N극을 위한 금속 패드가 있다면 이 과정에서 상기와 같은 패드 형성은 필요치 않다.

상기한 단계(S11~S34)를 거쳐 실리콘 기판(10)의 제조공정(S1,S2,S3)은 종료된다.

엘이디 소자(40)를 상기 캐비티(C)내의 안착면(11)에 실장하는 공정(S4)은 도 8에 도시되어 있는데, P극과 N극용 전기패드가 형성된 엘이디 소자(40)를 실리콘 기판(10)의 바닥 안착면(11)의 솔더 범프(B) 상에 플립칩 본딩한다.

상기 솔더 범프(B)가 Au 또는 Cu 등의 금속 물질인 경우에는 리플로우 본딩 대신 열압축(thermo compression) 또는 열초음파(thermo sonic) 본딩법이 바람직하다. 또한, 상기 솔더 범프(B)를 Au로 할 경우에는 엘이디 소자를 플립칩 본딩하기 전에 범프를 형성하여도 무방하다. 상기와 같은 엘이디 소자의 플립칩 본딩은 실리콘 웨이퍼로부터 엘이디 패키지용 실리콘 기판을 칩으로 분리한 뒤에 개별적으로 행해져도 무방하지만 더욱 바람직하게는 웨이퍼 상태에서 일괄적으로 수행하여 패키징 시간과 경비를 줄이는 것이 바람직하다.

전술한 실리콘 기판의 제조방법과 패키징 방법은 캐비티 내에 단지 하나의 엘이디 칩이 실장되는 경우를 예시한 것이다. 캐비티 내에 복수의 칩을 실장하기 위해서는 단지 캐비티의 면적을 적절히 확장하는 것으로 가능하며, 또한 엘이디 소자를 정전기로부터 보호하는 용도로 사용되는 제너다이오드나 쇼트키 다이오드 등을 캐비티 내에 추가하는 것도 가능하다.

또한, 상기와 같은 실리콘 기판의 구조와 조립방법은 엘이디 소자의 N극과 P극이 모두 플립칩 본딩으로 연결되는 경우에 바람직한 실리콘 기판의 구조이다. 하지만 본 발명은 엘이디 소자의 N극과 P극이 모두 와이어 본딩에 의해 기판과 연결되거나 혹은 상측과 하측에 각각 존재하여 플립칩 본딩이 N극 혹은 P극 어느 한 전극 패드에 대해서만 이루어지는 경우에도 적용 가능하다. 이에 대한 실시 예는 이후에 다시 구체적으로 설명하기로 한다.

도 9는 엘이디 소자(40) 위에 형광체(50)가 씌워지는 상태(공정 S5)를 도시한 단면도로서, 청색 혹은 UV 엘이디 소자 위에 형광체(50)를 도포하여 백색광원으로 사용하기 위한 것이다. 이 과정 역시 웨이퍼 단위로 수행이 가능하다.

도 10은 엘이디 소자(40)가 안착되고 그 위에 형광체(50)가 도포된 실리콘 기판(10) 위에 렌즈(60)가 장착된 상태(공정 S6)를 도시한 것으로, 이 렌즈(60)는 엘이디 소자(40)와 상기 형광체(50)를 통해 방출된 빛이 소정의 방사각을 갖도록 하는 역할을 하는데, 이 렌즈(60)는 빛의 조준 및 집속을 담당하는 렌즈부(62)와 기판(10)과의 부착을 용이하게 하는 목적의 다리부(64)로 구성되어 있다.

상기 렌즈(60)는 에폭시 수지 혹은 유리 재질이 바람직하며 몰딩이나 기계적인 가공을 통하여 제작한다. 상기 렌즈(60) 재료가 에폭시 수지인 경우에는 사출성형 등의 방법으로 기판상에 직접 형성하는 것이 바람직하고, 유리인 경우에는 실리콘 기판(10)의 렌즈의 다리부(64)가 놓여질 위치에 접착제를 적용하고 상기 렌즈(60)를 기판(10)에 정렬한 다음 가열 및 압착하여 부착한다.

상기 렌즈(60)의 재질이 유리인 경우에는 상기 접착제로서 솔더제를 사용하여도 무방하다. 이 경우에는 실리콘 기판의 접합부와 렌즈의 접합부 하단에 금속막을 형성하여 솔더와의 금속화적인 접합이 가능하도록 한다. 또 다른 방법으로는 상기 실리콘 기판(10)의 제조과정에서 기판의 소정의 위치 즉, 상기 렌즈의 다리부(64)가 접합될 위치에 BCB 등의 폴리머를 미리 형성해두고 상기 에폭시의 접합과 같은 방법으로 부착하는 방법도 가능하다. 상기에서 예시한 에폭시 접합법, 솔더접합법, 그리고 미리 형성된 폴리머 접합법 등 렌즈의 모든 접합법은 실리콘 기판을 날개로 분리한 다음에 개별적으로 수행하는 것도 무방하지만 웨이퍼단위로 진행하는 것이 작업효율 측면에서 바람직하다.

또, 한편으로는 상기 엘이디 소자(40)와 상기 렌즈(60) 혹은 상기 형광물질(50)과 상기 렌즈(60) 사이에 엘이디 소자의 기판물질의 굴절률과 근사한 높은 굴절률을 가진 오일 혹은 젤리 등의 인캡슐란트를 주입하여 상기 엘이디 소자의 표면에서 굴절률 차이에 기인한 빛의 전반사를 줄이는 것이 바람직하다. 이 과정에서 상기 인캡슐란트의 경화를 위해서 필요하다면 상기 실리콘웨이퍼 혹은 실리콘 기판을 가열하는 것도 가능하다.

상기와 같이 엘이디 소자(40) 및 렌즈(60)의 부착이 웨이퍼 상태에서 완료된 경우에는 상기 웨이퍼를 다이아몬드 톱 등으로 절단하여 개별 칩으로 분리함으로써 엘이디의 패키징이 완성된다.

도 11 및 도 12는 엘이디 패키지의 사용을 보다 용이하게 하기 위한 목적의 보조 기판(70)을 도시한 것으로서, 상기 보조 기판(70)은 몸체와 그 상부 및 하부 표면에 형성된 P극 및 N극 회로 패턴(72)과 범프(74)를 구비한다.

보조 기판(70)의 재질로는 열전도성이 우수하고 기계적 강도가 높으며 전기적으로 부도체인 Al_2O_3 , AlN, SiC 등이 바람직하다. 한편 상기 보조 기판(70)이 Cu, CuW, 다이아몬드 등으로 전기적인 도체이거나 전기 저항이 매우 높지 않은 경우에는 상기 보조 기판(70) 상에 형성되는 전극 간의 단락을 방지하기 위하여 표면에 절연물질을 코팅하여 사용하는 것이 바람직하다.

상기 P극 및 N극 회로 패턴(72)은 상기 실리콘 기판(10) 내에 내장된 엘이디 소자(40)를 외부와 전기적으로 연결하기 위한 것으로서, 최상부 표면층은 Au로서 산화를 방지하고, 그 하부에는 솔더와의 젖음성(wettability)이 좋고 솔더재료의 확산을 방지하는 Ni, Pt, Cu 등의 복수의 금속층으로 구성되며, 최하층은 기판과의 접착성이 좋은 Ti, Cr, Al 등이 사용된다.

경우에 따라서는 상기 보조 기판(70)을 관통하는 구멍을 내고 그 구멍을 따라서 하단의 금속막(표시되지 않음)과 전기적인 연결을 하여도 무방하다.

상기 범프(74)는 솔더 페이스트의 스크린 프린팅, 도금, 혹은 진공증착법 등으로 형성가능하고 Au 범프인 경우에는 스퍼터 범프법이 바람직하다. 조립은 상기 실리콘 기판(10) 하부의 본딩 패드(30)를 보조 기판상의 범프(74)와 정렬한 다음에 열과 압력을 적절히 가하여 본딩한다.

도 13은 본 발명의 다른 실시 예를 도시한 엘이디 패키지의 단면도로서, 엘이디 소자의 N극과 P극이 모두 와이어 본딩에 의해 기판과 연결되거나 혹은 N극과 P극이 상부와 하부에 각각 분리되어 존재하여 N극 혹은 P극 어느 한 전극 패드만이 플립칩 본딩으로 연결이 이루어지는 경우에 대응하기 위한 실리콘 기판의 구조를 제공한다. 캐비티(C) 내부 안착면(11)의 면적을 엘이디 소자(40)의 바닥 면적보다 충분히 크게 하고 엘이디 소자(40)가 안착될 바닥의 측면에 와이어 본딩을 위한 별도의 와이어본딩 패드(P')를 구비하고 본딩된 엘이디 소자(40)의 상부에 위치한 전극 패드와 상기 와이어본딩 패드(P')를 와이어(Q)로 연결함으로써 엘이디 소자(40)의 N극과 P극을 각각 실리콘 기판(10)의 하부를 통하여 외부와 연결할 수 있도록 되어 있다.

발명의 효과

이상에서와 같이 본 발명에 의한 표면실장형 엘이디 패키지는 실리콘 기판을 엘이디의 1차 본딩용 기판으로서의 용도와 엘이디에서 방출된 빛을 집속하는 캐비티의 용도 양면으로 활용함으로써 별도의 캐비티를 사용하는 것에 비해 부품수를 줄일 수 있고, 종래의 기판과 캐비티가 별도로 제작되는 구조에 비해 그 크기를 대폭 줄일 수 있으며, 엘이디 패키지의 크

기를 소형화함으로써 복수의 칩을 사용하는 경우에 단위면적당 휘도를 증가시킬 수 있고, 캐비티 측벽의 각도를 2 단계로 형성함으로써 엘이디 소자에서 방출되는 빔의 방사각을 조절 할 수 있으며, 실리콘은 엘이디 소자의 기판재료인 사파이어 혹은 SiC와 활성층인 GaN 등의 반도체 재료와 열팽창계수가 크게 다르지 않으므로 열팽창계수의 차이로 인한 스트레스를 줄일 수 있고, 실리콘 기판과 외부와의 전기적인 연결이 실리콘 기판을 관통하는 비아 홀과 이 비아 홀을 채우는 Cu 플러그를 통해 최단거리로 이루어지므로 전기적인 저항이 적고 열전도도가 높아 방열효율을 향상시킬 수 있으며, 또한 엘이디 소자의 패키징을 웨이퍼 단위로 수행함으로써 개별적으로 패키징 하는 것에 비해 공정수가 크게 줄어 제조 비용을 저감할 수 있는 이점을 가진다.

(57) 청구의 범위

청구항 1.

상면에 엘이디 소자의 안착을 위한 안착면(11)과 상기 안착면(11) 외곽에 대하여 소정각도로 제1경사면(12) 및 제2경사면(13)이 형성된 캐비티(C)와, 상기 안착면(11)에서 하면으로 관통된 복수의 비아 홀(14)을 갖는 실리콘 기판(10)과;

상기 실리콘 기판(10)의 제1경사면(12)과 제2경사면(13)상에 형성되는 반사층(20)과;

상기 실리콘 기판(10)의 비아 홀(14)에 설치되는 금속 플러그(30)와;

상기 실리콘 기판(10)의 안착면(11)에 안착되며 P 전극과 N 전극이 상기 금속 플러그(30) 상에 본딩 되는 엘이디 소자(40)와;

상기 실리콘 기판(10)에 부착되어 엘이디 소자(40)를 보호하고 엘이디 소자(40)에서 방출된 빔을 집속하여 엘이디 소자(40)에서 방출된 빛이 소정의 발산각 이내로 전파되도록 하는 렌즈(60);를 포함하여 이루어지는 엘이디 패키지.

청구항 2.

청구항 1에 있어서,

상기 엘이디 소자(40)는 청색 혹은 UV 엘이디 소자이고, 이 엘이디 소자(40) 위에는 청색광 혹은 UV를 받아 백색광을 내는 형광체(50)가 도포되는 것을 특징으로 하는 엘이디 패키지.

청구항 3.

청구항 1에 있어서,

상기 실리콘 기판(10)은 (100) 실리콘 웨이퍼인 것을 특징으로 하는 엘이디 패키지.

청구항 4.

청구항 1 또는 청구항 2에 있어서,

상기 캐비티(C)와 렌즈(60)사이에는 엘이디 소자(40) 기판물질의 굴절률과 근사한 굴절률을 갖는 오일 이나 젤형의 인캡슐런트가 주입되는 것을 특징으로 하는 엘이디 패키지.

청구항 5.

청구항 1 또는 청구항 2에 있어서,

상기 캐비티(C) 내에 엘이디 소자(40)를 정전기로부터 보호하기 위한 제너다이오드나 쇼트키 다이오드가 내장되는 것을 특징으로 하는 엘이디 패키지.

청구항 6.

청구항 1 또는 청구항 2에 있어서,

상기 캐비티(C) 내에 복수의 엘이디 소자가 내장되는 것을 특징으로 하는 엘이디 패키지.

청구항 7.

청구항 1에 있어서,

상기 엘이디 소자(40)와 렌즈(60)가 부착된 실리콘 기판(10)이 회로 패턴(72)과 범프(74)를 가진 별도의 보조 기판(70)에 부착되고 상기 엘이디 소자(40)의 N극 및 P 전극이 상기 보조 기판(70)을 통하여 외부와 전기적으로 연결되는 것을 특징으로 하는 엘이디 패키지.

청구항 8.

청구항 1에 있어서,

상기 실리콘 기판(10)의 안착면(11)의 면적을 엘이디 소자(40)의 면적보다 크게 하고, 엘이디 소자(40)가 안착될 바닥의 측면에 별도의 와이어본딩 패드(P')를 구비하고, 상기 안착면(11)에 본딩된 엘이디 소자(40)의 상부에 위치한 전극 패드와 상기 와이어본딩 패드(P')를 와이어(Q)로 연결하여 엘이디 소자(40)의 N극과 P극을 각각 실리콘 기판(10)의 비아 홀을 통하여 외부와 연결하도록 된 것을 특징으로 하는 엘이디 패키지.

청구항 9.

실리콘 기판(10) 상에 엘이디 소자(40)의 안착을 위한 안착면(11)과 상기 안착면(11) 외곽에 대하여 소정각도로 제1경사면(12) 및 제2경사면(13)을 갖는 캐비티(C)를 형성하는 실리콘 기판 가공공정(S1);

상기 제1경사면(12) 및 제2경사면(13)에 반사층(20)을 코팅(증착)하는 공정(S2);

상기 실리콘 기판(10)을 뒤집어서 뒤집어진 실리콘 기판(25)의 표면에서 안착면(11)까지 비아 홀(14)을 천공하고, 이 비아 홀(14)에 금속 플러그(30)를 형성하는 공정(S3);

엘이디 소자(40)를 상기 안착면(11)에 실장하는 공정(S4);

렌즈(60)를 실리콘 기판(10) 위에 부착하는 공정(S6);을 포함하여 이루어지는 것을 특징으로 하는 엘이디 패키지의 제조 방법.

청구항 10.

청구항 9에 있어서,

상기 제1경사면(12)은 식각 마스크를 갖는 실리콘의 이방성 식각으로 형성되고, 상기 제2경사면(13)은 식각 마스크를 사용하지 않는 실리콘의 이방성 식각으로 형성되는 것을 특징으로 하는 엘이디 패키지의 제조방법.

청구항 11.

청구항 9에 있어서,

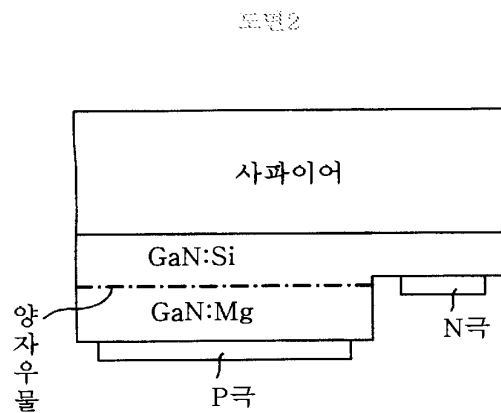
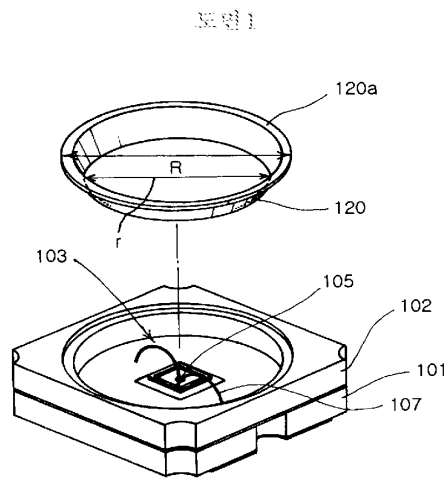
상기 공정(S4와 S6) 사이에 엘이디 소자(40) 위에 형광체(50)를 도포하는 공정(S5)을 더 포함하는 것을 특징으로 하는 엘이디 패키지의 제조방법.

청구항 12.

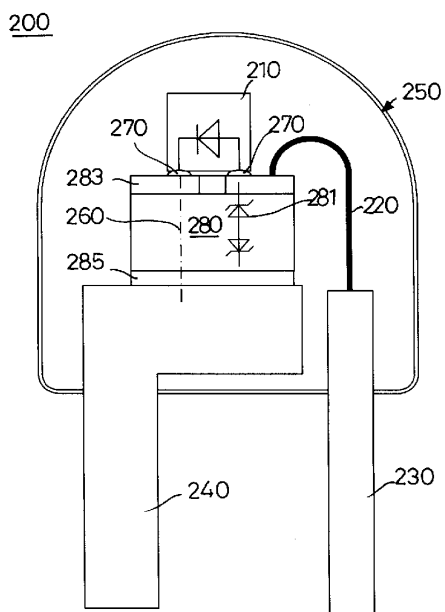
청구항 9 또는 청구항 11에 있어서,

상기 엘이디 소자의 실장, 형광체의 도포, 그리고 렌즈의 부착이 웨이퍼 레벨에서 이루어지는 것을 특징으로 하는 엘이디 패키지의 제조방법.

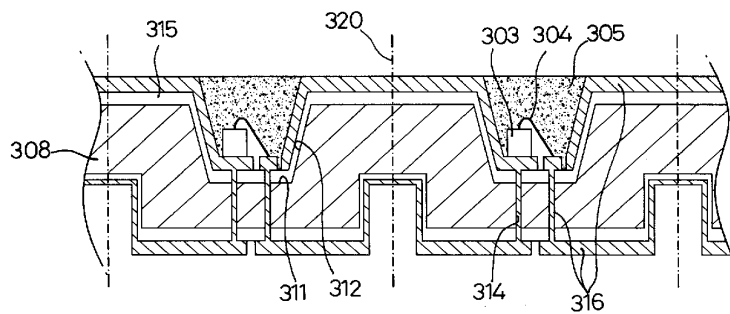
도면



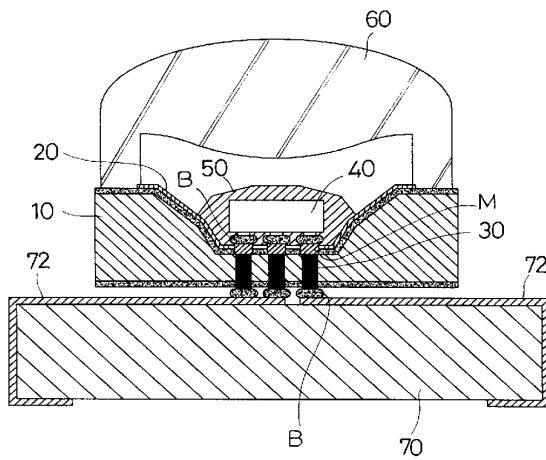
도면3



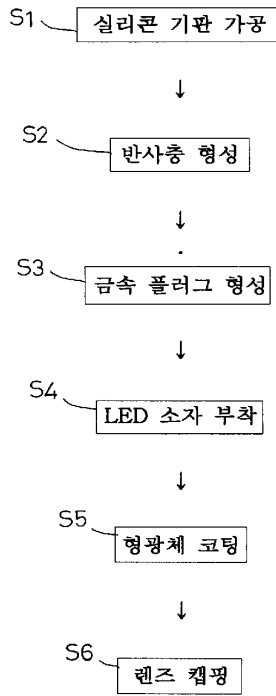
도면4



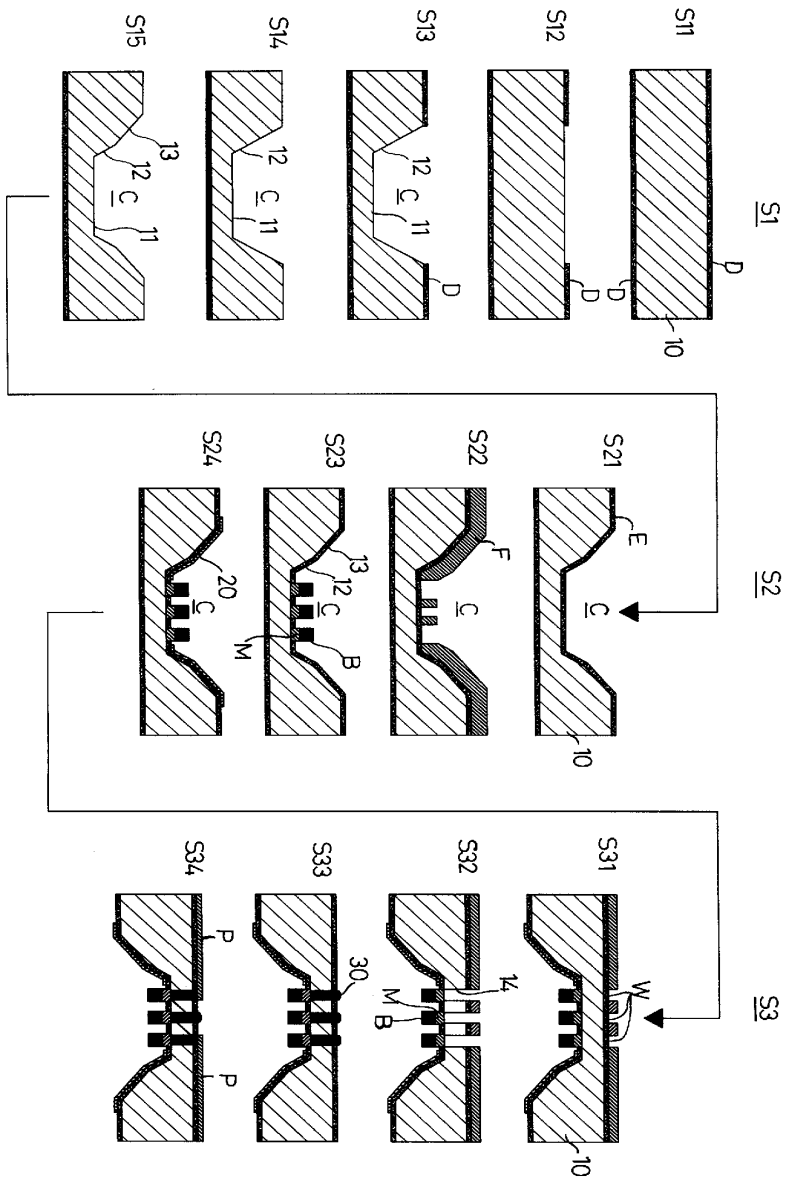
도면5



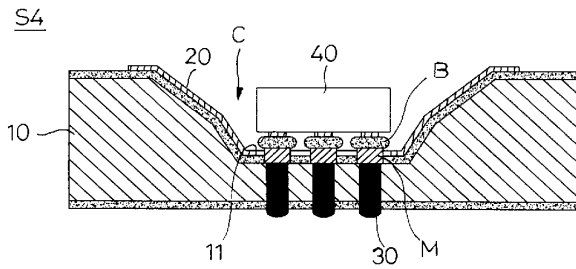
도면6



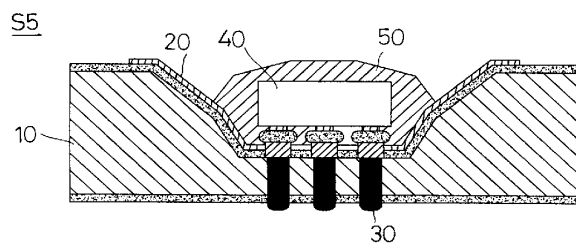
도 87



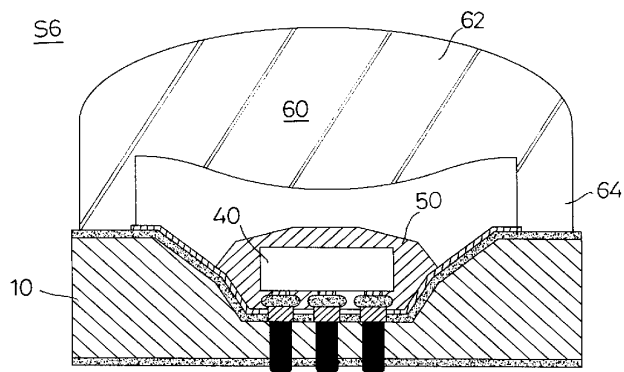
도 88



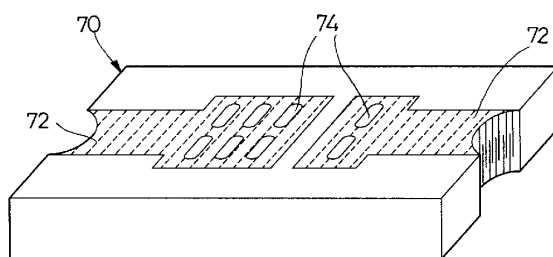
도면9



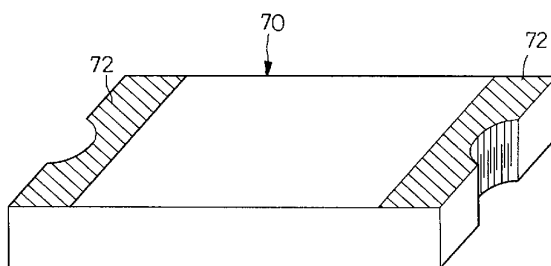
도면10



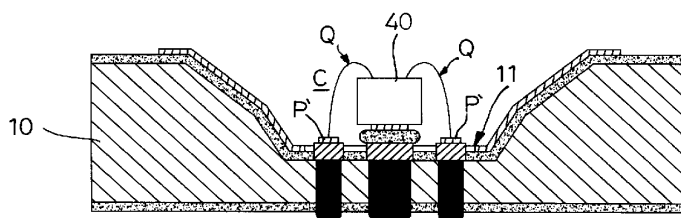
도면11



도면12



도면13



Patent Record Full View

Patent/Publication: KR610650B1

Bibliography

DWPI Title

Led package capable of minimizing size using substrate as dual application and manufacturing method thereof

Original Title

LED PACKAGE CAPABLE OF MINIMIZING SIZE USING SUBSTRATE AS DUAL APPLICATION AND MANUFACTURING METHOD THEREOF

LED package and a manufacturing method thereof. *(Translation from Thomson Reuters)*

English Title

LIGHT EMITTING DIODE PACKAGE AND MANUFACTURING METHOD THEREOF

Assignee/Applicant

Standardized: **FIONIX INC**

Original: FIONIX Inc., KR

Inventor

LEE Sang Hwan, KR

Publication Date (Kind Code)

2006-08-09 (B1)

Application Number / Date

KR200552196A / 2005-06-17

Priority Number / Date / Country

KR200552196A / 2005-06-17 / KR

Abstract

Abstract

PURPOSE: An LED(Light Emitting Diode) package and its manufacturing method are provided to reduce a size of the package by using a substrate as a first bonding substrate and a cavity for receiving emitted light.

CONSTITUTION: A silicon substrate(10) includes a seating surface(11) for an LED. A cavity including a first inclined surface and a second inclined surface is formed on the silicon substrate. A plurality of via holes are formed on the silicon substrate. A reflection layer(20) is formed on the first inclined surface and the second inclined surface of the silicon substrate. A metal plug(30) is formed on the via hole and the silicon substrate. An LED(40) is located at the seating surface of the silicon substrate. A P-electrode, and an N-electrode of LED are bonded to the metal plug. A lens for protecting the LED and receiving the emitted light is mounted on the silicon substrate.

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The low cost by the process of manufacturing semiconductor the production the bulb or the lamp in which the invention is used in the miniature electrical & electronics product including the cellular phone or the notebook computer etc. including the vehicle for the lamp can be replaced is made possible. And the miniaturization and integration are possible in comparison with the existing ramp type LED and surface mount type LED By the protection against heat performance being excellent and having the thermal stability the seating surface (11) for the seating of the LED device in the upper side and the cavity (C), and the multiple via holes (14) penetrated toward the lower-side in the seating surface (11) the LED package which comprises the silicon substrate (10) had, the reflecting layer (20) formed on the first inclined plane (12) and the second inclined surface (13) of the silicon substrate (10), the metal plug (30) installed at the via hole (14) of the silicon substrate (10), P electrode and the LED device (40), and the lens (60) and a manufacturing method thereof are provided. As to P electrode and the LED device

(40), N electrode is bonded on the metal plug (30) it is settled in the seating surface (11) of the silicon substrate (10). As to the lens (60), the light which is adhered to the silicon substrate (10) and protects the LED device (40) and focuses the beam emitted in the LED device (40) and is emitted in the LED device (40) is propagated within the predetermined divergence angle this. As to the, the first inclined plane (12) and the second inclined surface (13) are formed about the seating surface (11) outside into the designated angle it has the excellent durability.

Keywords The LED, package, semiconductor, surface mount device, silicone.

(Translation from Thomson Reuters)

Classes/Indexing

IPC

Current IPC	Invention	Version	Additional	Version
Full	H01L 33/48	20100101	-	-
Main Group	-	-	-	-
Subclass	-	-	-	-

Original IPC	Invention	Version	Additional	Version
Advanced/Full	H01L 33/00	20060101	-	-
Core/Main Group	-	-	-	-
Subclass	-	-	-	-

DWPI Manual Codes



Expand DWPI Manual Codes

Legal Status

INPADOC Legal Status

Gazette Date	Code	Description
2010-08-03	LAPS -	LAPSE DUE TO UNPAID ANNUAL FEE
2009-08-03	FPAY	ANNUAL FEE PAYMENT
2006-08-02	GRNT +	WRITTEN DECISION TO GRANT
2006-06-26	E701 +	DECISION TO GRANT OR REGISTRATION
2005-06-17	A201	REQUEST FOR EXAMINATION

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Expand INPADOC Family (1)

Claims

Claims

All Claims (12)

Claims (English)

1. The LED package which comprises the seating surface (11) for the seating of the LED device in the upper side and the cavity (C), the silicon substrate (10) having multiple via holes (14) penetrated toward the lower-side in the seating surface (11), the reflecting layer (20) formed on the first inclined plane (12) and the second inclined surface (13) of the silicon substrate (10), the metal plug (30) installed at the via hole (14) of the silicon substrate (10), P electrode and the LED device (40), and the lens (60), and as to the, the first inclined plane (12) and the second inclined surface (13) are formed about the seating surface (11) outside into the designated angle; as to P electrode and the LED device (40), N electrode is bonded on the metal plug (30) it is settled in the seating surface (11) of the silicon substrate (10); and as to the lens (60), the light which is adhered to the silicon substrate (10) and protects the LED device (40) and focuses the beam emitted in the LED device (40) and is emitted in the LED device (40) is propagated within the predetermined divergence angle this.

2. As for claim 1, the LED device (40) is blue or the UV LED device. And the LED package in which the fluorescent substance (50) receiving the blue light or UV on this LED device (40) and gives the white light is coated.
3. As for claim 1, the LED package which is the silicon substrate (10) is (100) silicon wafer.
4. As for claim 1 or 2, the LED package in which the encapsulant of oil having the refractive index of the LED device (40) substrate material among the cavity (C) and lens (60) and the fine refractive index or the gel type is injected.
5. As for claim 1 or 2, the Zener diode for protecting the LED device (40) from the static electricity within the cavity (C) or the LED package in which the schottky diode is embedded.
6. As for claim 1 or 2, the LED package in which multiple LED devices are embedded within the cavity (C).
7. As for claim 1, the LED device (40) and lens (60) the attached silicon substrate (10) is LED package which is connected to N pole of the LED device (40) and P electrode is the outside through the daughterboard (70) it is adhered to the separate daughterboard (70) having the circuit pattern (72) and bump (74) electrically.
8. As for claim 1, N pole of the electrode pad which is positioned in the upper portion of the LED device (40) bonded in the seating surface (11) it includes the separate wire bonding pad (P') in the side of the bottom surface in which the LED device (40) is settled it makes the area of the seating surface (11) of the silicon substrate (10) bigger than the area of the LED device (40) and LED device (40) and the LED package connecting P pole through the via hole of the respective silicon substrate (10) to the outside the wire bonding pad (P') is connected to the wire (Q).
9. The manufacturing method of the LED package which comprises cavity (C) having the designated angle about the seating surface (11) for the seating of the LED device (40) on the silicon substrate (10) and seating surface (11) outside the first inclined plane (12) and the second inclined surface (13) including the process (S4): process (S6) adhering the lens (60) on the silicon substrate (10) sets up process (S3) forming the metal plug (30) in this via hole (14) the process (S2): silicon substrate (10) the reflecting layer (20) the coating (deposition) is thrown into confusion in the silicon substrate machining (S1): first inclined plane (12) formed and the second inclined surface (13): LED device (40) in the seating surface (11).
10. The manufacturing method of the LED package which is formed with the anisotropic etching of the silicone; and is formed into the anisotropic etching of the silicone in which the second inclined surface (13) does not use the etching mask of claim 9, wherein the first inclined plane (12) have the etching mask.
11. As for claim 9, the manufacturing method of the LED package further comprising the process (S5) coating with the fluorescent substance (50) between process (the S4 and S6) on the LED device (40).
12. As for claim 9 or 11, the manufacturing method of the LED package in which comprises the mounting of the LED device, and the coating of the fluorescent substance and attaching of the lens in the wafer level.

(Translation from Thomson Reuters)

Description

Background/ Summary

Background/Summary

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Drawing Description

Drawing Description

Figure 1 is a perspective view showing an example of the conventional LED package

Figure 2 is a cross-sectional view of the bottom emitting type LED device

Figure 3 is a perspective view showing the other example of the conventional LED package

Figure 4 is a cross-sectional view showing another example of the conventional LED package

Figure 5 is a cross-sectional view showing the structure of the LED package by the embodiment of the invention

Figure 6 is a fabrication diagram of the LED package according to the invention

Figure 7 is a cross-sectional view which successively shows the manufacturing process of the silicon substrate among the manufacturing process of the LED package according to the invention

Figure 8 is a cross-sectional view showing the state where the LED device is bonded in completed on silicon substrate

Figure 9 is a cross-sectional view showing the state where it is incurred with the fluorescent substance on LED device

Figure 10 is a cross-sectional view showing the state where the lens is capped on the fluorescent substance

Figure 11 is a perspective view of the daughterboard

Figure 12 is a bottom surface perspective view of the daughterboard illustrated in Figure 11

Figure 13 is a cross-sectional view of the LED package by the other embodiment of the invention.

* The description of reference numerals showing the main elements in drawings.

10: silicon substrate 11: seating surface.
12: first inclined plane 13: the second inclined surface.
14: via hole 20: reflecting layer.
30: metal plug 40: LED device.
50: fluorescent substance 60: lens.
70: daughterboard 72: circuit pattern (metal terminal)
74: bump B: solder bump.
C: cavity D: etch barrier layer.
E: electronic insulating film F: photoresist.
M: UBM metallic layer P: pad.
P': wire bonding pad Q: wire.
W: etching window.

(Translation from Thomson Reuters)

Description

Description

The LED package and manufacturing method thereof [Light Emitting Diode Package and manufacturing method thereof]. **Background Art**

The present invention relates to the LED package, and it is the bulb which is specifically used in all kinds of the transportation means including the vehicle for the lamp until it reaches to the miniature electrical & electronics product including the cellular phone or the notebook computer etc. or the LED for illumination package replacing the ramp type LED and the production is possible through the affordable price with the process of manufacturing semiconductor and the miniaturization and integration are possible in comparison with the existing ramp type LED or the surface mount type LED and by the protection against heat performance being excellent and having the thermal stability it has the excellent durability.

Light the electron where the LED (LED: Light Emitting Diode), in other words, the light emitting diode is injected and surplus energy the hole reunites may be the red light-emitting diode using the GaAsP etc. it is the diode releasing, the green light emitting diode using the GaP etc, and the blue light emitting diode etc using the InGaN / AlGaN double hetero structure.

In the meantime, while it develops the technology creating the white light using the combination or the fluorescent substance of the RGB LED device from blue or the UV LED the scope of application is expanded to the back light lamp of the LCD display device and the lighting field replaces the existing bulb or the fluorescent lamp etc. besides the basic light emitting indication function and the high-brightness led development therefor is progressed.

The package type of the LED device includes the ramp type, and the structure in which it has 2 kinds of the surface mount type and the metallic electrode side having the certain angular is equipped at the upper part of one lead frame to the cup shape and the upper portion the LED device has as to the ramp type, among the lead frame of 2 and the molded lens is put on the upper part. There can be the limit it applies to the light emitting diode for the high power because it becomes as the structure difficult that the thermal resistance between the package case and the LED device are big and such ramp type LED adheres to the heat sink to the lower part of the package.

In the meantime, the surface mount type LED includes wire the electrode the LED device is arranged in the built-in region in which the outer shape angular is less it has the package which between is comprised of the molding epoxy resin while becoming on the substrate including the ceramics etc. with die bonding, and the structure of being connected. The surface mount type LED is widely used as the high power LED package because the thermal release is facilitated.

By the result of that the conventional surface mount type LED package (KR2003-0053853 A) like being presented in fig. 1 changes the lateral tilt formed in the first ceramic substrate (101), at least one LED device (105), and the area corresponding to the built-in region of the LED device (105) it is arranged on the first ceramic substrate (101) into cylindrical shape for which the formed second ceramic substrate (102), and this metal plate swash plate (120) is the upper part diameter (R) it is made including the metal reflective sheet (120) adhered within the cavity of the second ceramic substrate (102) the LED device (105) is surrounded are greater than lower end diameter (r) with difference of the phase, and the lower end diameter (R,r) it is made the luminance angle distribution of the LED device (105) is controlled and the area of the metal reflective sheet (120) or the material and surface coating is differentiated and the brightness of the LED device (105) can be controlled. As to the first ceramic substrate (101), it has the upper side in which the built-in region of the LED device (105) is formed and the predetermined conductive pattern is formed around the built-in region. At least one LED device (105) is arranged in the built-in region of this first ceramic substrate (101) upper side and is connected to the predetermined conductive pattern.

This kind of the conventional surface mount type LED package has the method forming the inclined surface (film) is the problem with high manufacturing cost it is the ceramic substrate made with the punching or the cut etc. mechanical the yield is low having the proper angle for the brightness and luminance angle modulation.

In the meantime, the limit followed the lead frame and electrical connection between the substrate of the outside and the LED chip in which the inner portion had the conventional surface mount type LED package mentioned by the upper part through two bonding wires in increase in the miniaturization and luminous efficiency of the product it consists of the structure of being made and the simplification of the manufacturing process is planned but the structure has the impediment.

Recently with it was developed the disadvantage of such conventional LED was complemented as shown in FIG. 2, the bottom emitting type LED device in which P pole of the LED device and electrode of N pole were altogether located on surface the light emitting surface of the device was developed. It is reflected through the sapphire substrate having transparent light in which the bottom emitting type LED is generated in the active layer of LED to the direct outside in the metallic layer for P pole formed on the surface of the light which is emitted and however is emitted towards a part substrate backside. Is the device and N pole and it again releases to the outside. As to this kind of bottom emitting type LED, the luminous efficiency is very much used in the high-brightness led apparatus relatively because it is higher than the saw emitting (Top emitting) device.

What the above-mentioned bottom emitting LED device throws the front side in which the electrode of the active layer of the structure device of the device and device are positioned into confusion and performs flip-chip bonding is necessary.

Metal pad corresponding to P electrode in the front side of the LED device and N electrode the luminous efficiency of the LED device is improved according to US US2002/0070386 A A1 or the metal pad and solder bump are included and the solder bump for the flip chip bonding of the LED chip is included on the silicon sub-mount and with the LED device is performed flip-chip bonding to on the sub mount the first packaging is completed. Here, the silicon sub-mount the electronic (electronic) function like the voltage accommodation limit (voltage-compliance limiting) action additionally provides the LED die and package with the role of electrically thermally connecting.

Figure 3 shows the application example of another silicon sub-mount presented at US6,642,550 A. The invention, according to a preferred embodiment of the present invention, the LED arrangement (200) comprises the LED chip (210) sealed up with the light-transmissive package (250) like the plastic bulb. And it is connected on the solder bump (270) in which the package (250) is arranged in the upper portion of two independent electricals the silicon sub-mount (280) capable of the LED chip (210) is the wire bonding of the singular number a part of the lead frame consisting of the connector, and in other words, the anode (230) and cathode (240) is hemmed round and the LED chip (210) the touch pad (contact pads) of the LED chip is disposed to be connected to the solder bump and queue.

It has two functional domains in which the silicon sub-mount (280) is called as the upper layer (283) and lower layer (285) but in order to make the reflectivity of the surface good a part of the upper layer (283) is deposited to the Al metal. The solder bump (270) is formed and the ESD (electrostatic discharge) protection circuit (281) is embedded in the fixed region of the Al surface. The metallic layer including the Au etc. is formed in the lower layer (285) of the sub mount and the interconnection (260) passing through the sub mount (280) for electrically connecting the upper layer (283) and lower layer (285) of the silicon sub-mount (280) is formed. P and N electrode pad of the LED chip (210) are connected to the solder bump (270) of the silicon sub-mount upper layer (283) surface and the anode (230) of the lead frame and upper layer (283) of the sub mount are carried on with the wire bonding (220) and it connects electrically and it is connected to the lower layer (285) by the interconnection (260) in which N pole (240) passes through the silicon sub-mount (280). In this way, it has the advantage which can reduce the wire bonding between the LED chip (210) and lead frames (230, 240) to single by using the interconnection (260) passing through the silicon sub-mount (280).

The above-mentioned silicon sub-mount provides the direct advantage can have the integrated circuit necessary for the function as the substrate for the attaching of the LED device, simultaneously, the built in of the electrostatic discharge Protection Circuit, furthermore, the driving of the LED device.

In the meantime, the advantage which is of secondary importance with the mass producibility, the integration function and application of the wafer level packaging technology etc. providing the function of the cavity focusing the light in which the silicon sub-mount which more actively utilizes the MEMS texturing technique of the silicone is emitted besides the above-

described function in LED device and which silicone semiconductor fabrication technique has may be obtained.

Figure 4 shows an example of the conventional technology of this kind of the purpose (US6,531,328 A B1). Provided is the electrical insulation film (315), of the SiO₂ formed on the surface of the groove (311), having the wall (312) that according to a preferred embodiment of the present invention, inclines to 54.74° on the surface of (100) or (110) silicon substrate of the invention and the through hole (314), formed in the rear side of the substrate using the dry etch and substrate or the Si₃N₄ and the silicon substrate (308) including the plated metal layer (316) inside top and bottom and through hole (314) of the substrate. It is completed to a process of placing the LED packaging is the LED chip (303) on the electrode within the groove (311) of the silicon substrate (308): a process of connecting the bonding metal wire (304) it connects: a process of charging the encapsulation resin (305): according to the embodiment of the invention and the process finally of cutting according to the cutting line (320).

Advantage of decreasing the size of the package and number of component and number of assembly process by having the cavity used as the purpose of effectively delivering the beam in which the conventional invention exemplified in fig. 4 is emitted from the LED device to the lens of the LED chip upper portion built in the silicon sub-mount the separate cavity is used are provided.

But according to the conventional invention exemplified in fig. 4, the angle comprising the cavity of the inclined surface is with 54.74° or the angle is limited to 90°. The inclination angle of the respective optimal has to be changed according to the kind of the lens which the cavity of the purpose of effectively delivering the beam emitted from LED device to the lens of the upper part uses in the use of LED, and the size of the chip, especially, the depth of the cavity with the thickness of the relative chip, and the use or nonuse of the lens. Therefore, there can be the disadvantage that the application range cannot help being very restrictive in case of being limited as the angle of the inclined surface is the specific angle.

Moreover, at the same time, the reflecting layer managing the optical action and the electrode layer managing the electrical action are formed into the metallic layer consisting of Ag, Au, Pd, Pt etc according to the conventional invention exemplified in fig. 4. But the reflecting layer is comprised of the material which enough provides and need to do all specifications that need to be manufactured with the metal or the dielectric thin film and are required as the electrical property, that the electrode layer is required as the electrical electrode and all composition element, that is required as the UBM (under bump metallurgy) of the solder bump lower part in case of performing flip-chip bonding to especially, the LED chip in other words, the bonding layer, and the diffusion stopper, the oxidation prevention layer and each element, providing the optimised reflection efficiency. Therefore, it is difficult at the same time, to enough satisfy the requirement specification of the electrode layer and reflecting layer according to the conventional invention exemplified in fig. 4. In the mean time, the material filling up the through hole passing through the silicon substrate does not provide the conventional invention of fig. 4 is the effective means about this the material is required having the low electrical resistance and high thermal conductivity the power consumption of the LED package lowers and the thermal release is effectively performed at the same time.

Abstract Problem

The present invention is to provide one purpose of the invention is the surface mount type LED package capable of the production through the process of manufacturing semiconductor and manufacturing method thereof the above-described conventional overall problem is revealed.

Another object of the invention is to provide the silicon substrate including the cavity having the different inclination angle of two kinds of as the substrate of the LED package.

Another object of the invention is to provide the metal or the dielectric thin film which effectively can reflect the light emitted to the sidewall of the cavity in the LED device.

Another object of the invention is to provide the effective UBM metal necessary for the flip chip bonding of the LED device and solder bump.

Another object of the invention is to provide the connection forming the via hole which passes through the silicon substrate in order to connect the electrode of the LED device to the lower part of the silicon substrate and fills in the via hole with the metal including the Cu etc. and having the low electric resistance and high thermal conductivity has the low electrical resistance and high thermal conductivity.

Another object of the invention is to provide the electrode pattern and the necessary solder bump setting up the silicon substrate in the heat sink or PCB but.

Another object of the present invention is to provide the LED packaging technology of the wafer level capable of the majority of the packaging process of the LED device is the packaging in the wafer level including the die bonding or the flip chip bonding of the LED chip, the application of the fluorescent substance, the application of the encapsulant, the molding or the attaching of the lens etc. the LED device is to be packaged.

The this, to accomplish the above objects. And the present invention is to provide the LED package which the seating surface on which the LED device in the upper side is mounted and cavity having the designated angle about the seating surface outside the first inclined plane and the second inclined surface are formed and comprises the first inclined plane of the silicon substrate having multiple via holes penetrated toward the lower-side in the seating surface and silicon substrate and the fluorescent substance which is coated on the LED device in which P and N electrode are bonded in the metal plug and LED device while being settled in the formed reflecting layer, the multiple metal plugs installed in the via hole of the silicon substrate and seating surface of the silicon substrate on the second inclined surface and the lens which is bonded in on silicon substrate and covers the fluorescent substance of the semiconductor inner portion.

The invention provides the method of manufacturing LED package comprising the process routing of the lens in on silicon substrate the capping (bonding) of coating the cavity having the designated angle about the seating surface for the seating of the LED device on the method, for manufacturing the above-described LED package and the silicon substrate and this seating surface outside the first inclined plane and the second inclined surface the fluorescent substance on the process forming the metal plug in this via hole the via hole is formed at the lower-side of the process: silicon substrate of the reflecting layer the coating (deposition) on the silicon substrate machining: first inclined plane formed and the second inclined surface to the seating surface: on silicon substrate in which the process: LED device of setting up the LED device in the seating surface within the cavity is installed.

Invention Configuration

Hereinafter, the preferred embodiment which does not limit the invention decides to be particularly explained with attached drawing.

Figure 5 is a cross-sectional view which is the cross-sectional view and fig. 6 the fabrication diagram of the package according to a preferred embodiment of the present invention and fig. 7 successively shows the manufacturing process of the silicon substrate among the manufacturing process of the LED package according to a preferred embodiment of the present invention showing the structure of the LED package according to a preferred embodiment of the present invention.

As shown in figures 5 through 7, the LED package of the invention comprises the lens (60) which is adhered to the fluorescent substance (50): which is coated on the LED device (40): in which P and N electrode are bonded in the metal plug (30) and LED device (40) while being settled in the reflecting layer (20):, formed on the first inclined plane (12) of the silicon substrate (10): and silicon substrate (10) and the second inclined surface (13) the multiple metal plugs (30) installed at the via hole (14) of the silicon substrate (10) and seating surface (11) of the silicon substrate (10) and silicon substrate (10) and focuses the light emitted in the LED device (40) having the multiple via holes (14) which the cavity (C) is formed and is penetrated toward the lower-side in the seating surface (11) that have the designated angle about the seating surface (11): for the LED device seating and seating surface (11) outside the first inclined plane (12) and the second inclined surface (13) to the upper side.

The metal plug (30) exposed to this is the lower part it is adhered on the daughterboard (70) is soldered in the circuit pattern (72) formed in upper side of daughterboard (70) and the LED package of the invention shown in fig. 5 is made.

The desirable reflecting layer (20) of the invention is composed of the lowermost layer is the silicone or the silicon nitride film or the silicon oxide film, including, the adhesive property is the good Ti, the Cr etc. it is comprised of multiple metallic layers. And the outermost (upper portion) layer comprises the Ag with high reflectivity about the light emitted in LED, the Au, the Al etc. It is acceptable using the thin film consisting of the dielectric of the multi-layer instead of the reflecting layer according to case is the metal. And it may be acceptable that the third or the fourth metallic foil is inserted according to case between the lower layer and upper layer.

In the present invention, the metal material with an excellent electric conductance including the Cu, the Au etc. for connecting electrically is plated with the respective outside and the metal plug (30) uses P pole and N pole of the LED device (40).

As shown in FIG. 4, the LED device (40) is adhered as the LED device positioned at the surface in which P pole and the active layer in which N pole generates the upper portion of the device, in other words, light are positioned of the bottom emitting type to the flip chip type on the silicon substrate.

Energy than that the fluorescent substance (50) receives blue or the UV light may be used in the white light formation apparatus which generally uses the fluorescent substance as the chemical material generating the light of green and low red.

The lens (60) focuses the beam emitted in the LED device (40) and most of lights are propagated within the predetermined divergence angle.

Or in case the hard mechanical intensity is required in case of it being difficult that the daughterboard (70) shown in fig. 5 adheres to the silicon substrate (10) on the direct PCB substrate which is not shown or the radiation plate it uses.

Figure 6 is a fabrication diagram of the LED package according to the invention. The silicon substrate machining (S1) forming the cavity (C) having the designated angle about the seating surface (11) for the seating of the LED device (40) on the silicon substrate (10) and this seating surface (11) outside the first inclined plane (12) and the second inclined surface (13).

The process (S2) the reflecting layer (20) in the first inclined plane (12) and the second inclined surface (13) the coating (deposition).

The process (S3) which forms the via hole (14) at the lower-side of the silicon substrate (10) to the seating surface (11) and plates the metal plug (30) in the via hole (14).

The process (S4) setting up the LED device (40) in the seating surface (11) within the cavity (C).

It comprises the process (S5): coating the fluorescent substance (50) on the silicon substrate (100) in which the LED device (40) is installed and the process (S6) the lens (60) on the silicon substrate (10) the capping (bonding).

Hereinafter, decide to explain more concretely about the above-described manufacturing process (S1~S6).

Figure 7 is a cross-sectional view which successively shows the manufacturing process (S1~S3) of the silicon substrate (10) among the manufacturing process of the LED package according to the invention.

As shown in FIG. 7, the silicon substrate (10) forms the etch barrier layer (D) into LPCVD, the Thermal Oxidation or the plasma enhanced chemical vapor deposition method etc. as the silicon wafer having (100) crystal plane into the respective silicon nitride film (Si_3N_4), the silicon oxide film (SiO_2) or the non-stoichiometric silicon nitride film (SiNX) etc (S11).

Subsequently, the etch barrier layer (D) of the site in which the cavity is formed in the upper portion of the silicon substrate (10) through the photography transcription process and dry etching process is removed (S12). At this time, it is in a line with $\langle 110 \rangle$ crystal ographic direction of (100) silicon wafer the etch pattern arranges.

Next, the silicon substrate is etched to the aqueous anisotropic silicon etchant including the KOH (potassium hydroxide), the TMAH (Tetramethyl ammonium hydroxide), the EDP (Ethylenediamine-pyrocatechol) etc. and the cavity (C: cavity) and seating surface (11) are formed (S13).

The pyramidal shape that lower part are cut of the rectangular becomes the etched form of the cavity (C: cavity) and the angle in which the inner wall (it the hereinafter says to be " first inclined plane " this with 12) of the cavity (C) is comprised of the surface of the silicon substrate (10) is determined with the crystalline structure of (100) silicon wafer as about 54.7° . Subsequently, the etch barrier layer (D) of the silicon nitride film formed on the surface of silicon substrate (10) or the silicon oxide film is altogether removed to the wet or the dry etching (S14).

Subsequently, the new second inclined surface (13) different from the angle comprised in the partial upper side of the first inclined plane (12) of the cavity (C) which is formed if it etches to the aqueous anisotropic silicon etchant including KOH, TMAH or EDP etc. by the predetermined depth in the state where there is no etching mask with the surface of the silicon substrate (10) is the inclination angle of the first inclined plane (12) is formed (S15). This kind of phenomenon is presented in paper including the Drago Resnik etc (Drago Resnik et al, J. Micromech. Microeng. 10 (2000) 430-439).

In the angle in which this second inclined surface (13) is comprised on crystallography as (311) side with the substrate surface, about 25° is. However it is comprised the slow angle of about $20\sim 35^\circ$ with various factors in fact. Moreover, at this time, if the second etch time is adjusted the ratio which the first inclined plane (12) and the second inclined surface (13) occupy can be controlled and by doing in this way the effective inclination angle in which two inclined surfaces are incorporated can be controlled.

Next, the silicon nitride film or the silicon oxide film etc. are formed into the electronic insulating film (E) on the top surface of the silicon substrate (10) in which the cavity (C) is formed the step (S21) into the prescribed thickness. (S21)

Subsequently, in order to form the UBM metallic layer for the flip- chip of the LED device and solder bump on the predetermined area of the cavity (C) inner portion after the photoresist (F) is coated the front side of the wafer with the step (S22) the photoresist (F) of the site in which the UBM metallic layer and solder bump are formed into the photography transcription process is removed. Next, the UBM metallic layer (M) and solder bump (B) material the successively are deposited and the photoresist (F) of the solder bump (B) lower part and UBM metallic layer (M) is removed the step (S23) to acetone etc. and the UBM metallic layer (M) and solder bump (B) are formed.

The UBM metallic layer which generally is applied to the electric component and opto-semiconductor device with the Ti / Ni / Au, the Cr / Ni / Au, the Cr / Cr-Cu / Cu / Au etc. is desirable to the preferred UBM metallic layer (M) and the solder bump material which also generally is applied to the electric component and opto-semiconductor device with au, au / Sn, sn / Pb, the Sn / Ag etc is applied as the solder bump (B) material. More preferably, the au capable of the reflow without the use of the flux and Au / Sn etc. are desirable.

In the meantime, the form are possible that the UBM pattern and solder bump pattern form the UBM pattern and solder bump pattern as to the form and area into the formation process of above-described UBM and solder bump and same method in case of to being different. Moreover, in case of using the Au as the solder bump material (S22) the bump is not formed at the step and after the board processing is completed it is the LED device acceptable to form the bump on the flip- chip below former into the stud bumping method. In the mean time, the form of the UBM pattern of any type according to P pole of the LED device and the primary purpose that the respective connected UBM pattern is not electrically circuit-shortened in each other with N pole and it most occupies the wide side are acceptable. Here, the light in which the metallic layer formed in lower part of the purpose of most occupying the wide side is the LED device is emitted in the LED device is to be efficiently reflected and the heat which and is generated in the LED device on the other hand, is to be effectively delivered to the outside.

Similarly, it may be acceptable that also it does not divide into the respective plurality about P pole and N pole with the number of solder bumps and it is done by the respective one about P pole and N pole. Furthermore, it may be acceptable that the form of the solder bump and UBM has any form in P pole and figure one N pole is not electrically circuit-shortened. The height of the solder bump is done by the number μm to the several tens μm height in consideration of simplicity and

the mechanical strength of the bonding etc.

Next, the reflecting layer (20) is formed on the sidewall of the cavity (C) through the deposition of the photography transcription process and metal or plating in order to make first and second inclined surfaces (12,13) of the cavity (C) the mirror facet the step (S24) of fig. 7. The material of the reflecting layer (20) the metal multilayer of the ti / Al, cr / Al, cr / Ag, the Ti / Ag etc is desirable and at this time, as to the lowermost layer, the good material is the connection between the substrate and the upper metal desirable and the metal including the good ag, the Au, the Al etc. as to the upper metal, of the reflectivity about the light of the wave length of the light emission region of the LED device is desirable. It is acceptable using the reflective film using dielectric of the multi-layer instead of the metallic foil according to case.

The silicon substrate (10) going through the above-described justice the step (S31) of fig. 7 is thrown into confusion to the next process and the etching window (W) for the etching of the silicon substrate (10) itself is formed on the surface of the overturned silicon substrate (10) through the photography transcription process and dry etch and until the etched bottom surface meets with the UBM metallic layer (M) of the lower part it etches through the silicon etch (Deep Si RIE) or the deep wet etching and the via hole (14) is formed the step (S32) and the metal material including the Cu, the Au, the solder etc. is plated and it fills in this via hole (14) and the metal plug (30) is formed the step (S33).

The lower extremity metal (Base metal) film necessary for plating it plates to the electro-plating process is formed inside the front side and via hole (14) of the silicon substrate (10) through the sputtering. In the state where the metal plug (30) is formed, it is desirable to remove this protrusion part through the grinding in case the plating layer is overly protruded on the surface of the substrate (10).

Subsequently, in order that the electrode pad which can be connected to the electrode of the LED device on the surface of the silicon substrate (10) is formed the step (S34) one side is connected to the metal plug (30) and the other side forms the pad (P) developing into the outside of the metal plug (30).

The silicon substrate (10) is adhered on another substrate of the other and if the metal pad for the above-mentioned P pole and N pole has the substrate in this process the above-mentioned pad forming is not necessary.

The manufacturing process (S1,S2,S3) of the silicon substrate (10) is terminated after the above-described step (S11~S34).

The process (S4) setting up the LED device (40) in the seating surface (11) within the cavity (C) is illustrated in 8. P pole and the LED device (40) in which the electric pad for N pole is formed are performed flip-chip bonding to on the solder bump (B) of the bottom surface seating surface (11) of the silicon substrate (10).

The thermocompression (thermo compression) or the thermosonic (thermo sonic) bonding method is instead of desirable with reflow bonding in case the solder bump (B) is the metal material including the Au or the Cu etc. Moreover, it may be acceptable that before performing flip-chip bonding to the LED device in case of the solder bump (B) to the Au the bump is formed. Even if it is individually performed after the flip chip bonding of the above-mentioned LED device separates the silicon substrate for the LED package according to the chip from the silicon wafer it is acceptable but more preferably, it is desirable to summarily perform in the wafer level and decrease the packaging time and expenses.

The above-described method of manufacturing silicon substrate and the packaging method exemplify the case where it only has one LED chip within the cavity. It is possible to add zener diode which is used for is possible that only appropriately expands the area of the cavity in order to set up and protecting moreover, the LED device from the static electricity or the schottky diode etc. to multiple chips within the cavity within the cavity.

Moreover, it is the structure of the preferred silicon substrate in case the structure and assembling method of the above-mentioned silicon substrate N pole and P pole of the LED device are altogether connected to the flip chip bonding. However, even in case N pole and P pole of the LED device are altogether connected with the substrate with the wire bonding or the invention exists in the upper side and lower side and the flip chip bonding is made on N pole or P pole one electrode pad it is applicable. Thereafter specifically the embodiment about this again decides to explain.

Figure 9 is a cross-sectional view showing the state (process S5) in which it is incurred with the fluorescent substance (50) on the LED device (40). The fluorescent substance (50) on blue or the UV LED device can be used as the white light source it coats. The e-process the effectuation is possible by unit of the wafer.

Fig. 10 shows the state (process S6) in which the lens (60) is mounted on the silicon substrate (10) in which the LED device (40) is settled and the fluorescent substance (50) is coated on the upper part. And this lens (60) comprises the leg part (64) of the purpose the beam emitted through the LED device (40) and fluorescent substance (50) having the predetermined radiation angle and of facilitating the attaching between the lens unit (62) and the substrate (10) in which this lens (60) manages the collimation and concentration of light.

The epoxy resin or the vitreous material is desirable and the lens (60) makes through the molding or the mechanical processing. It is desirable that it directly forms into the method including the injection molding etc. on the substrate in case the lens (60) material is the epoxy resin and after in case of being the glass the adhesive is applied to the position in which the leg part (64) of the lens of the silicon substrate (10) is placed and the lens (60) is arranged in the substrate (10) it heats and it compresses and it adheres.

It is acceptable as the adhesive using the soldering materials in case the material of the lens (60) is the glass. In this case,

the metal layer is formed on the junction of the silicon substrate and junction lower part of the lens and the metallic junction with the solder is possible. In the manufacturing process of the silicon substrate (10) as another method, the method for forming the polymer including BCB etc. in advance and adhering to the position in which the predetermined position of the substrate, in other words, the leg part (64) of the lens is welded to the method like the junction of the epoxy is possible. In the above case, it is acceptable to individually perform after the epoxy bonding method, and all bonding method of the polymer bonding method lamp lenses formed with the solder joint method in advance separate the silicon substrate according to the piece but it is desirable in the work efficiency side to progress by unit of the wafer.

And it is desirable to inject the encapsulant including oil or the jelly etc. and having the high refractive index which is closely akin to the refractive index of the substrate material of the LED device to on the other hand between the LED device (40) and lens (60) or the fluorescent material (50) and lens (60) reduce the total reflection of the light caused by the difference of refractive index on the surface of the LED device. In this process, it is possible to heat up the silicon wafer or the silicon substrate if it is needed for the hardening of the encapsulant.

As described above, by case the attaching of the lens (60) and LED device (40) is completed in the wafer level the wafer being cut with the diamond saw etc. and separating into the discrete chip the packaging of LED is completed.

Figures 11 and 12 show the daughterboard (70) of the purpose of more facilitating the use of the LED package. And the daughterboard (70) comprises the body, the upper portion, and P pole formed on the bottom surface, N pole circuit pattern (72) and bump (74).

The thermal conductance is excellent to the material of the daughterboard (70) and the mechanical strength is high and the Al_2O_3 , which is the non-conductor the AlN, the SiC etc. are electrically desirable. In the meantime, in order that daughterboard (70) prevents the short circuit between the electrode which is formed into the Cu, the CuW, the diamond etc. on the daughterboard (70) in case it is the electrical conductor or the electric resistance is not very high, it is desirable to coat the insulating material on the surface and use.

P pole and N pole circuit pattern (72) comprise the outside the LED device (40) embedded within the silicon substrate (10) and the multiple metallic layers including the Ni capable of preventing the diffusion of the solder material the wettability with the solder is good in the lower part it connects electrically and therefore the uppermost point surface layer prevents oxidation as the Au, the Pt, the Cu etc. And the good Ti, the Cr, the Al etc. as to the lowermost layer, of the adhesive property with the substrate is used.

It may be acceptable that the hole passing through the daughterboard (70) is made according to case and it connects.

It enables to form and in case of being the Au bump the stud bumping method the bump (74) is desirable to the screen printing of the solder paste, plating or the vacuum deposition method etc. After the bonding pad (30) of the silicon substrate (10) lower part is arranged with the bump (74) on the daughterboard assembly appropriately adds and bonds heat and pressure.

Figure 13 is a cross-sectional view of the LED package showing the other embodiment of the invention. N pole and P pole of the LED device are altogether connected with the substrate with the wire bonding or in case N pole and P pole are separated in the upper portion and lower part and it exists and the connection is accomplished only N pole or P pole one electrode pad of the flip chip bonding the structure of the silicon substrate for corresponding to is served. By connecting the electrode pad and the wire bonding pad (P') which is the area of the cavity (C) inner portion seating surface (11) positioned in the upper portion of the LED device (40) big and which enough includes the separate wire bonding pad (P') for the wire bonding than the floor space of the LED device (40) in the side of the bottom surface in which the LED device (40) is settled and which is bonded to the wire (Q) N pole and P pole of the LED device (40) can be connected through the lower part of the respective silicon substrate (10) to the outside.

Advantageous Effects

As described above, whereas the separate cavity is used by utilizing it as the use both sides of the cavity focusing the light in which the surface mount type LED package according to the invention is the silicon substrate emitted in the use as the substrate for the first bonding of LED and LED the number of component can be decreased and the size can be drastically reduced in comparison with the structure where the conventional substrate and cavity are separately manufactured and multiple chips the stress due to difference of the coefficient of thermal expansion the semiconductor and coefficient of thermal expansion including the sapphire in which the silicone is the substrate material of the LED device or the GaN etc. are not different the radiation angle can be controlled is the SiC and active layer of the beam emitted from the LED device the angle of the cavity sidewall is formed into 2 step the brightness per the unit area can be increased in case of using can be reduced to by miniaturizing the size of the LED package and since it is made through the via hole in which the electrical connection between the silicon substrate and the outside pass through the silicon substrate and the Cu plug filling this via hole of the minimum distance the electrical resistance can be less and the thermal conductivity is high and the efficiency for heat dissipation can be improved Moreover, it has the advantage which the number of process decreases and can reduce the manufacturing cost whereas it packages the individually by performing the packaging of the LED device by unit of the wafer.

(Translation from Thomson Reuters)

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Citation Record level

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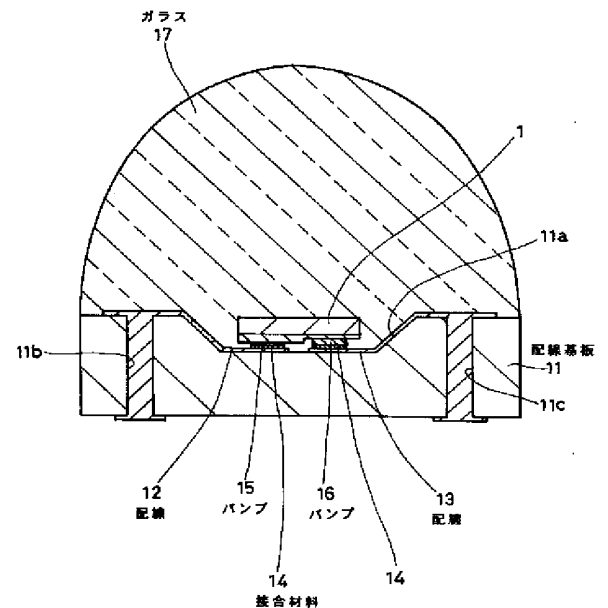
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(22) 出願日	平成 9 年(1997) 6 月18日	(72) 発明者	森田 悦男 東京都品川区北品川 6 丁目 7 番35号 ソニ ー株式会社内
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(54) 【発明の名称】 半導体装置および半導体発光装置

(57) 【要約】

【課題】 発熱環境下や高温環境内で使用可能な耐環境性の半導体装置および封止材料の光学的な変色または着色による輝度劣化を防止することができる半導体発光装置を提供する。

【解決手段】 G a N系半導体層が積層された基板の G a N系半導体層の表面または基板の裏面を配線基板などの基台上に接合する半導体発光装置や電子走行素子などの半導体装置において、接合材料として300℃以上700℃以下の融点を有する金属材料、例えばA u - I n系合金を用いる。また、G a N系半導体層が積層された基板の G a N系半導体層の表面または基板の裏面を配線基板などの基台上に接合し、基板を封止材料で封止する半導体発光装置において、封止材料として350℃より高く700℃以下の融点を有し、かつ、光透過性の無機材料、例えばガラスを用いる。



【特許請求の範囲】

【請求項１】 素子構造を形成する窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層が一方の主面に積層された基板の上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層の表面または上記基板の他方の主面が基台上に接合された半導体装置において、

接合材料として３００℃以上７００℃以下の融点を有する金属材料を用いたことを特徴とする半導体装置。

【請求項２】 接合材料として３５０℃以上７００℃以下の融点を有する金属材料を用いたことを特徴とする請求項１記載の半導体装置。

【請求項３】 上記金属材料がＰｂ－Ｐｄ系、Ａｕ－Ｇａ系、Ａｕ－Ｇｅ系、Ａｕ－Ｓｉ系、Ａｌ－Ｚｎ系、Ａｌ－Ｇｅ系、Ａｌ－Ｍｇ系、Ａｕ－Ｉｎ系、Ａｇ－Ｍｇ系、Ａｌ－Ｃｕ系、Ａｌ－Ｓｉ系、Ａｌ－Ｓｉ－Ｍｇ系、Ａｌ－Ｓｉ－Ｚｎ系、Ａｌ－Ｐｄ系、Ａｌ－Ｉｎ系、Ｃｕ－Ｇｅ系、Ａｇ－Ｇｅ系、Ｃｕ－Ｉｎ系またはＡｕ－Ｚｎ系の合金であることを特徴とする請求項１記載の半導体装置。

【請求項４】 上記半導体装置は上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層が発光素子構造を形成する半導体発光装置であり、上記基板は光透過性を有し、上記基板に関して上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層と同じ側にｐ側電極およびｎ側電極が設けられ、上記ｐ側電極および上記ｎ側電極が上記基台上に設けられた第１の電極部および第２の電極部とそれぞれ電氣的に接続されるように上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層の表面が上記基台上に接合されていることを特徴とする請求項１記載の半導体装置。

【請求項５】 上記基台上に上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層から発生する光を反射させるための反射構造を有する凹部が設けられ、この凹部の底面に上記基板の上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層の表面が接合されていることを特徴とする請求項４記載の半導体装置。

【請求項６】 上記基台は配線基板であり、上記配線基板に設けられた配線により上記凹部の上記反射構造が形成されていることを特徴とする請求項５記載の半導体装置。

【請求項７】 上記半導体装置は電子走行素子であることを特徴とする請求項１記載の半導体装置。

【請求項８】 発光素子構造を形成する窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層が一方の主面に積層された光透過性の基板の上記窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体層の表面または上記基板の他方の主面が基台上に接合され、上記基板が封止材料で封止された半導体発光装置において、上記封止材料として３５０℃より高く７００℃以下の融点を有し、かつ、光透過性を有する無機材料を用いたことを特徴とする半導体発光装置。

【請求項９】 上記無機材料の融点は上記接合の温度より低いことを特徴とする請求項８記載の半導体発光装置。

【請求項１０】 上記無機材料がガラスであることを特徴とする請求項８記載の半導体発光装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】 この発明は、半導体装置および半導体発光装置に関し、特に、窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体を用いた発光ダイオードや半導体レーザあるいは電子走行素子に適用して好適なものである。

【０００２】

【従来の技術】 緑色から青色、さらには紫外線の発光が可能な半導体発光装置として、窒化ガリウム（ＧａＮ）に代表される窒化物系ⅡⅡⅠ－Ⅴ族化合物半導体をサファイア基板やＳｉＣ基板などの上にエピタキシャル成長させて発光ダイオード構造を形成したＧａＮ系発光ダイオードが知られている。

【０００３】 このようなＧａＮ系発光ダイオードは、通常、図７に示すように樹脂でモールド封止が行われた状態で使用される（例えば、特開平８－７８７２７号公報）。すなわち、図７に示すように、このモールド封止型ＧａＮ系発光ダイオードにおいては、発光ダイオード構造を形成するＧａＮ系半導体層１０１が積層されたサファイア基板１０２の裏面が、リードフレーム１０３の上部に設けられた凹部１０３ａの底面に接着剤１０４で接着されている。この凹部１０３ａの底面および内壁面は、動作時にＧａＮ系発光ダイオードの発光層から発生する光を外部に取出すための反射面となっている。接着剤１０４としては、エポキシ樹脂系の接着剤が用いられている。この場合、ＧａＮ系発光ダイオードのｐ側電極およびｎ側電極（図示せず）はＧａＮ系半導体層１０１と同じ側に設けられており、ｐ側電極はワイヤー１０５によりリードフレーム１０３とボンディングされ、ｎ側電極はワイヤー１０６によりリードフレーム１０７とボンディングされている。そして、ＧａＮ系発光ダイオードは、集光機能を持たせることなどを目的として、その近傍の部分のリードフレーム１０３、１０７とともに樹脂１０８でレンズ形状にモールドされている。樹脂１０８としては、一般的には無色透明のエポキシ樹脂が用いられている。

【０００４】

【発明が解決しようとする課題】 しかしながら、上述の従来のモールド封止型ＧａＮ系発光ダイオードにおいては、使用を続けて行くと、ＧａＮ系発光ダイオードが劣化していないにもかかわらず、急激な経時劣化、具体的には、輝度劣化が生じてしまい、信頼性上問題があった。これは、動作時にＧａＮ系発光ダイオードの発光層から発生する光の影響により、樹脂１０８として用いられているエポキシ樹脂が光学的に変色または着色するこ

とにより透過率が低下するためである（例えば、特開平8-148717号公報）。

【0005】一方、発光素子を実装する場合、ワイヤーボンディングなどによる実装方式に比べて小スペースで高密度実装が可能な実装方式としてフリップチップ法がある（例えば、特開平6-104480号公報、特開平6-177429号公報、特開平5-326520号公報）。このフリップチップ法においては、接合材料としては、通常、共晶組成のPb-Sn系合金やAu-Sn系合金が用いられている（例えば、特開平5-90329号公報）。しかしながら、これらの接合材料を用いてGaN系発光ダイオードをフリップチップ法により実装した場合には、それらの接合材料の融点が280℃以下と低い（例えば、Pb-61.9wt%Snの共晶温度は183℃、Au-90wt%Snの共晶温度は217℃、Au-20wt%Snの共晶温度は278℃）、高密度実装による発熱環境下や高温の環境内で使用すると、接合材料が溶融して不良が生じ、信頼性上問題があった。この問題はまた、大電力用半導体素子として注目されているGaN系電子走行素子においても、同様に生じ得るものである。

【0006】したがって、この発明の目的は、封止材料の光学的な変色または着色による輝度劣化を防止することができる半導体発光装置を提供することにある。

【0007】この発明の他の目的は、発熱環境下や高温環境内で使用可能な耐環境性の半導体装置を提供することにある。

【0008】

【課題を解決するための手段】上記目的を達成するために、この発明の第1の発明は、素子構造を形成する窒化

物系III-V族化合物半導体層が一方の主面に積層された基板の窒化物系III-V族化合物半導体層の表面または基板の他方の主面が基台上に接合された半導体装置において、接合材料として300℃以上700℃以下の融点を有する金属材料を用いたことを特徴とするものである。

【0009】ここで、接合材料の融点の上限を700℃としたのは、半導体発光装置などに用いられる窒化物系III-V族化合物半導体層のうちGaN層は通常700～800℃の温度で成長されることから、接合温度はこのGaN層の成長温度の下限である700℃以下に限られるためである。一方、接合材料の融点の下限を300℃としたのは、従来に比べて接合部の耐熱性を向上させるためである。

【0010】この発明の第1の発明において、より高い耐熱性を得る観点からは、接合材料として350℃以上700℃以下の融点を有する金属材料を用いる。

【0011】この発明の第1の発明において、接合材料として用いられる金属材料の具体例を挙げると、Pb-Pd系、Au-Ga系、Au-Ge系、Au-Si系、Al-Zn系、Al-Ge系、Al-Mg系、Au-In系、Ag-Mg系、Al-Cu系、Al-Si系、Al-Si-Mg系、Al-Si-Zn系、Al-Pd系、Al-In系、Cu-Ge系、Ag-Ge系、Cu-In系またはAu-Zn系の合金である。これらの合金の共晶組成および共晶温度を示すと、次の通りである（ASM Handbook, Volume 3, Alloy Phase Diagrams (ASM International, 1992)）。

【0012】

合金	共晶温度 (℃)
Pb-25wt%Pd	474
Au-31wt%Ga	448.6
Au-15.2wt%Ga	339.4
Au-12.5wt%Ge	361
Au-3.2wt%Si	363
Al-94wt%Zn	381
Al-51.6wt%Ge	420
Al-66wt%Mg	437
Au-41.9wt%In	495.4
Ag-51.39wt%Mg	472
Al-32wt%Cu	548.2
Al-12.6wt%Si	577
Al-24wt%Pd	615
Al-17.3wt%In	639
Cu-60.4wt%Ge	644
Ag-82wt%Ge	651
Au-34wt%Zn	667
Au-12wt%Zn	683

なお、共晶組成ではないが、Cu-38.4wt%Inの融点は678℃である。

【0013】この発明の第1の発明において、半導体装置は、典型的には、窒化物系III-V族化合物半導体層が発光素子構造を形成する半導体発光装置である。この場合、基板は光透過性を有し、例えば、この基板に関して窒化物系III-V族化合物半導体層と同じ側にp側電極およびn側電極が設けられる。そして、p側電極およびn側電極が基台に設けられた第1の電極部および第2の電極部とそれぞれ電氣的に接続されるように窒化物系III-V族化合物半導体層の表面が基台上に接合される。また、好適には、基台に窒化物系III-V族化合物半導体層から発生する光を反射させるための反射構造を有する凹部が設けられ、この凹部の底面に基板の窒化物系III-V族化合物半導体層の表面が接合される。基台は例えば配線基板であり、この場合、この配線基板に設けられた配線により凹部の反射構造を形成することができる。この基台は、リードフレームやヘッダーなどであってもよい。

【0014】この発明の第1の発明において、半導体装置は、電子走行素子、具体的には、電界効果トランジスタ(FET)などであってもよい。

【0015】この発明の第2の発明は、発光素子構造を形成する窒化物系III-V族化合物半導体層が一方の主面に積層された光透過性の基板の窒化物系III-V族化合物半導体層の表面または基板の他方の主面が基台上に接合され、基板が封止材料で封止された半導体発光装置において、封止材料として350℃より高く700℃以下の融点を有し、かつ、光透過性を有する無機材料を用いたことを特徴とするものである。

【0016】ここで、封止材料の融点の上限を700℃としたのは、半導体発光装置などに用いられる窒化物系III-V族化合物半導体層のうちGaInN層は通常700～800℃の温度で成長されることから、封止温度はこのGaInN層の成長温度の下限である700℃以下に限られるためである。一方、封止材料の融点の下限を350℃としたのは、十分な耐熱性を得るためである。

【0017】この発明の第2の発明においては、好適には、封止材料として用いられる無機材料の融点は、接合の温度よりも低い。この無機材料は、典型的には、ガラスである。

【0018】この発明において、窒化物系III-V族化合物半導体層は、Ga、Al、InおよびBからなる群より選ばれた少なくとも一種のIII族元素と、少なくともNを含み、場合によってはAsまたはPを含むV族元素とからなる。この窒化物系III-V族化合物半導体層の具体例を挙げると、GaN層、AlGaInN層、GaInN層、AlGaInN層などである。

【0019】上述のように構成されたこの発明の第1の発明においては、接合材料として300℃以上700℃以下の融点を有する金属材料を用いたことにより、従来

のように接合材料としてPb-Sn系合金やAu-Sn系合金を用いた場合に比べて接合部の耐熱性が向上し、発熱環境下や高温環境内での耐久性が向上する。

【0020】上述のように構成されたこの発明の第2の発明においては、封止材料として350℃より高く700℃以下の融点を有し、かつ、光透過性を有する無機材料を用いたことにより、従来のように封止材料としてエポキシ樹脂などの樹脂を用いた場合と異なり、半導体発光装置の使用に伴う、封止材料の光学的な変色または着色を防止することができる。

【0021】

【発明の実施の形態】以下、この発明の実施形態について図面を参照しながら説明する。なお、実施形態の全図において、同一または対応する部分には同一の符号を付す。

【0022】まず、この発明の第1の実施形態によるモールド封止型GaN系発光ダイオードについて説明する。図1はGaN系発光ダイオードを示し、図2は図1に示すGaN系発光ダイオードをガラスで封止したモールド封止型GaN系発光ダイオードを示す。

【0023】図1に示すように、このGaN系発光ダイオードにおいては、例えばc面のサファイア基板1上に、GaNバッファ層2、n型GaN層3、n型AlGaInN層4、GaInNからなる発光層5、p型AlGaInN層6およびp型GaN層7が順次積層されている。ここで、n型GaN層3の上層部、n型AlGaInN層4、発光層5、p型AlGaInN層6およびp型GaN層7はメサ形状にパターニングされている。これらの表面を覆うようにSiO₂膜のような絶縁膜8が設けられている。この絶縁膜8は、電氣的絶縁および表面保護のためのものである。この絶縁膜8には、p型GaN層7の上およびn型GaN層3の上にそれぞれ開口8a、8bが設けられている。そして、開口8aを通じてp型GaN層7にp側電極9がコンタクトしているとともに、開口8bを通じてn型GaN層3にn側電極10がコンタクトしている。p側電極9としては例えばNi/Au膜が用いられ、n側電極10としては例えばTi/Al/Au膜が用いられる。

【0024】図2に示すモールド封止型GaN系発光ダイオードにおいては、配線基板11の上部に設けられた逆台形状の断面形状を有する凹部11の底面に、図1に示すGaN系発光ダイオードがそのGaN系半導体層を下にしてフリップチップ実装されている。

【0025】すなわち、配線基板11の上面には、凹部11aの底面から凹部11aの外側の平坦部にかけて延在するように所定パターンの配線12、13が設けられている。これらの配線12、13はさらに、配線基板11に設けられたスルーホール11b、11cを通じて配線基板11の下面まで延在しており、この下面から突出した部分が電極部を構成している。凹部11aの底面上

の配線12、13の端部は電極部（パッド部）を構成しており、これらの電極部の上に接合材料14が設けられている。そして、図1に示すGa N系発光ダイオードのp側電極9およびn側電極10の上にそれぞれ設けられた例えばAuからなるパンプ15、16が接合材料14により配線12、13の端部の電極部とそれぞれ接合され、互いに機械的および電氣的に接続されている。ここで、これらの配線12、13は、Ga N系発光ダイオードの発光層5から発生する光を反射させて外部に取り出すための反射鏡の役割も果たす。

【0026】この場合、接合材料14としては、先に挙げた300℃以上700℃以下の融点を有する金属材料のうちから必要に応じて選択されたものが用いられ、具体的には、例えば、共晶温度が495.4℃のAu-41.9wt%Inが用いられる。

【0027】配線基板11としては、少なくとも接合材料14による接合温度および後述のモールド封止の温度より高い耐熱温度および電氣的絶縁性を有し、さらに熱伝導が良好なものが用いられ、具体的には例えばアルミナ基板のようなセラミックス基板が用いられる。

【0028】この場合、Ga N系発光ダイオードは、配線基板11の上面とともに、ガラス17でレンズ形状にモールド封止されている。このガラス17としては、融点が350℃より高く700℃以下で光透過性のものが用いられ、具体的には例えばSiO₂にPbO、B₂O₃、Na₂O、ZnOなどを混合したものが用いられる。例えば、SiO₂にPbOおよびB₂O₃を混合したガラスは430～490℃の融点を有する。PbOおよびB₂O₃を主体とし、SiO₂がほとんど入っていないガラスでも350～400℃の融点を得ることができる。

【0029】また、配線基板11の材料とガラス17の材料との組み合わせによっては、配線基板11とガラス17との間に熱膨張係数差があり、これが封止後のガラス17に割れなどを生じさせることもあり得るが、この場合には、ガラス17に熱膨張係数の小さい透明なフィラーを入れるなどして配線基板11とガラス17との間の熱膨張係数差を十分に小さくすることにより、この問題を解決することができる。

【0030】次に、上述のように構成されたモールド封止型Ga N系発光ダイオードの製造方法について説明する。

【0031】まず、配線基板11の凹部11aの底面の配線12、13の端部の電極部上に真空蒸着法、スパッタリング法、めっき法などにより接合材料14を形成する。一方、図1に示すGa N系発光ダイオードのp側電極9およびn側電極10の上には例えばボールボンディング法などによりパンプ15、16を形成する。そして、配線基板11の凹部11aの底面に、Ga N系発光ダイオードを、そのp側電極9およびn側電極10上に

形成されたパンプ15、16が、配線12、13の端部の電極部上に形成された接合材料14の上にくるように位置合わせして置く。この後、この配線基板11を、接合材料14の融点以上の温度に加熱されたリフロー炉（図示せず）内に通し、接合材料14をリフローさせる。これによって、この接合材料14によりGa N系発光ダイオードのパンプ15、16と配線12、13の端部とが接合される。

【0032】次に、このようにして配線基板11上にフリップチップ実装されたGa N系発光ダイオードをガラス17でモールド封止する。このモールド封止は、具体的には例えば次のようにして行うことができる。

【0033】第1の方法では、例えば粉末状のガラス原料をモールドの鋳型に入れ、この鋳型中のガラス原料に、Ga N系発光ダイオードがフリップチップ実装された配線基板11の上面を押し付け、この状態で鋳型をガラス原料の融点よりも高い温度に加熱してガラス原料を溶融させる。この後、鋳型を冷却して配線基板11を取り出す。これによって、ガラス16によりGa N系発光ダイオードがモールド封止される。この方法では、粉末状のガラス原料を用いていることにより、鋳型にガラス原料を入れやすく、また、ガラス原料の表面積の増大によって溶融しやすくなるという利点がある。

【0034】第2の方法では、Ga N系発光ダイオードがフリップチップ実装された配線基板11の上面にこのGa N系発光ダイオードを覆うように例えば粉末状のガラス原料を盛り上げる。この場合、ガラス原料をプレスすることにより、あらかじめ所定の形状に整形してもよい。次に、この配線基板11をガラス原料の融点よりも高い温度に加熱することによりガラス原料を溶融させ、この溶融ガラスを表面張力によりレンズ形状に盛り上がらせた後、冷却する。これによって、ガラス16によりGa N系発光ダイオードがモールド封止される。ここで、ガラス原料を溶融させるための加熱は、加熱炉による加熱、ランプ加熱、集光加熱、熱風の吹き付けなどにより行うことができる。

【0035】第3の方法では、Ga N系発光ダイオードがフリップチップ実装された配線基板11の上面にこのGa N系発光ダイオードを覆うように溶融ガラスをレンズ形状に盛り上げ、その後冷却する。これによって、ガラス16によりGa N系発光ダイオードがモールド封止される。この場合、溶融ガラスの表面張力によりこの溶融ガラスがレンズ形状に自己形成されるようにすることができる。

【0036】以上のように、この第1の実施形態によれば、Ga N系発光ダイオードをフリップチップ実装するための接合材料14として融点が300℃以上700℃以下の金属材料を用い、また、Ga N系発光ダイオードの封止材料として融点が350℃以上700℃以下で光透過性のガラス17を用いていることにより、発熱環境

下や高温環境内でも優れた耐久性を示す耐環境性のモールド封止型GaN系発光ダイオードを実現することができる。さらに、このモールド封止型GaN系発光ダイオードは、封止材料として無機材料であるガラス17を用いていることにより、封止材料としてエポキシ樹脂などの樹脂を用いた場合のように、使用に伴い封止材料の変色や着色が生じることがなく、経時的な輝度劣化が生じるのを防止することができる。また、配線基板11の配線12、13が反射鏡の役割も果たすことにより、別に反射構造を設けなくても、GaN系発光ダイオードから発生する光を効率よく外部に取り出すことができる。

【0037】次に、この発明の第2の実施形態によるモールド封止型GaN系発光ダイオードについて説明する。図3に、このモールド封止型GaN系発光ダイオードを示す。

【0038】図3に示すように、この第2の実施形態によるモールド封止型GaN系発光ダイオードにおいては、配線基板11のスルーホール11b、11cが、パンプ15、16の直下に設けられている。そして、配線12、13は凹部11aの底面および内壁面にのみ設けられており、この凹部11aの外側の平坦部には延在していない。その他のことは、第1の実施形態によるモールド封止型GaN系発光ダイオードと同様であるので、説明を省略する。

【0039】また、この第2の実施形態によるモールド封止型GaN系発光ダイオードの製造方法は第1の実施形態によるモールド封止型GaN系発光ダイオードの製造方法と同様であるので、説明を省略する。

【0040】次に、この発明の第3の実施形態によるフリップチップ実装GaN系半導体レーザについて説明する。図4に、このフリップチップ実装GaN系半導体レーザを示す。

【0041】図4に示すように、この第3の実施形態によるフリップチップ実装GaN系半導体レーザにおいては、配線基板11の上に、図1に示すGaN系発光ダイオードと同様な構造を有するGaN系半導体レーザがそのGaN系半導体層を下にしてフリップチップ実装されている。すなわち、GaN系半導体レーザのp側電極9およびn側電極10の上にそれぞれ設けられたパンプ15、16が接合材料14により配線12、13の端部の電極部と接合され、互いに機械的および電氣的に接続されている。この場合、GaN系半導体レーザのGaN系半導体層の発光領域18が配線12の端部の電極部の直上にくるようにする。これは、このGaN系半導体層の発光領域18はGaN系半導体レーザの動作時に最も温度が上昇するため、この発光領域18で発生した熱を迅速に配線12、さらには配線基板11に伝導させて冷却を行う必要があるからである。配線基板11は、実装面である上面が平坦であることを除いて、第1の実施形態によるモールド封止型GaN系発光ダイオードにおける

配線基板11と同様な構造を有する。

【0042】接合材料14および配線基板11の材料については第1の実施形態と同様であるので、説明を省略する。

【0043】この第3の実施形態によるフリップチップ実装GaN系半導体レーザは、第1の実施形態によるモールド封止型GaN系発光ダイオードの製造方法におけるフリップチップ実装の方法と同様の方法により製造することができる。

【0044】この第3の実施形態によれば、GaN系半導体レーザをフリップチップ実装するための接合材料14として融点が300℃以上700℃以下の金属材料を用いていることにより、発熱環境下や高温環境内でも優れた耐久性を示す耐環境性のフリップチップ実装GaN系半導体レーザを実現することができる。

【0045】次に、この発明の第4の実施形態によるGaN系半導体レーザ装置について説明する。図5に、このGaN系半導体レーザ装置を示す。

【0046】図5に示すように、この第4の実施形態によるGaN系半導体レーザ装置においては、例えばCu製のヒートシンク19上にGaN系半導体レーザ20が実装されている。この場合、このGaN系半導体レーザ20は導電性のSiC基板21の表面に図1に示すGaN系発光ダイオードと同様なGaN系半導体層22が積層されてレーザ構造が形成されたものであり、p側電極9はこのGaN系半導体層22の上に形成されているが、n側電極10はSiC基板21の裏面に形成されている。そして、このGaN系半導体レーザ20のp側電極9が接合材料14によりヒートシンク19に接合され、互いに機械的および電氣的に接続されている。この接合材料14としては、第1の実施形態における接合材料14として用いたものと同様なものを用いることができる。一方、n側電極10の電氣的接続は、例えばAu製のワイヤー23をボンディングすることにより行われる。

【0047】この第4の実施形態によれば、GaN系半導体レーザ20を実装するための接合材料14として融点が300℃以上700℃以下の金属材料を用いていることにより、発熱環境下や高温環境内でも優れた耐久性を示す耐環境性のGaN系半導体レーザ装置を実現することができる。

【0048】次に、この発明の第5の実施形態によるGaN系半導体レーザ装置について説明する。図6に、このGaN系半導体レーザ装置を示す。

【0049】図6に示すように、この第5の実施形態によるGaN系半導体レーザ装置においては、GaN系半導体レーザ20のn側電極10が接合材料14によりヒートシンク19に接合されている。そして、p側電極9にワイヤー23がボンディングされている。その他のことは、第4の実施形態によるGaN系半導体レーザ装置

と同様であるので、説明を省略する。

【0050】この第5の実施形態によれば、第4の実施形態と同様な利点を得ることができる。

【0051】以上、この発明の実施形態について具体的に説明したが、この発明は、上述の実施形態に限定されるものではなく、この発明の技術的思想に基づく各種の変形が可能である。

【0052】例えば、上述の第1、第2および第3の実施形態において、パンプ15、16の表面にも接合材料14を形成しておくことにより、融着による接合をより容易かつ確実に行うことができる。また、接合材料14による融着に超音波ボンディング法や熱圧着ボンディング法を用いることにより、接合温度の低温化を図ることができる。

【0053】また、上述の第1、第2および第3の実施形態におけるパンプ15、16の代わりに、例えばめっき法などにより厚膜のAu膜を形成して接合面積を大きくするようにしてもよい。

【0054】さらに、上述の第1、第2および第3の実施形態においては、GaN系発光ダイオードまたはGaN系半導体レーザの基板としてサファイア基板1を用いているが、必要に応じて、このサファイア基板1の代わりに他の基板、具体的にはSiC基板やGaN基板などを用いてもよい。同様に、第4および第5の実施形態において、SiC基板21の代わりにGaN基板を用いてもよい。

【0055】また、上述の第4および第5の実施形態においては、ダブルヘテロ構造のGaN系半導体レーザにこの発明を適用した場合について説明したが、この発明は、活性層とクラッド層との間に光導波層を設けたいわゆるSCH (Separate Confinement Heterostructure) 構造のGaN系半導体レーザに適用することも可能であり、また、活性層として多重量子井戸構造 (MQW) や単一量子井戸構造 (SQW) のものを用いてもよい。さらに、レーザ構造としては、利得導波や屈折率導波を実現するリッジ導波路型、内部狭窄型、構造基板型、縦モード制御型 (分布帰還 (DFB) 型またはブラッグ反射 (DBR) 型) などの各種のレーザ構造を用いることが可能である。

【0056】さらに、上述の第1、第2、第3、第4および第5の実施形態においては、GaN系発光素子にこの発明を適用した場合について説明したが、例えばGaN系FETを実装する場合にもこの発明を適用することが

ができる。

【0057】

【発明の効果】以上説明したように、この発明による半導体装置によれば、接合材料として300℃以上700℃以下の融点を有する金属材料を用いたことにより、従来のように接合材料としてPb-Sn系合金やAu-Sn系合金を用いた場合に比べて接合部の耐熱性が向上し、これによって発熱環境下や高温環境内で使用可能な耐環境性の半導体装置を提供することができる。

【0058】また、この発明による半導体発光装置によれば、封止材料として350℃より高く700℃以下の融点を有し、かつ、光透過性を有する無機材料を用いたことにより、従来のように封止材料としてエポキシ樹脂などの樹脂を用いた場合と異なり、半導体発光装置の使用に伴う、封止材料の光学的な変色または着色を防止することができ、これによって封止材料の光学的な変色または着色による輝度劣化を防止することができる。

【図面の簡単な説明】

【図1】この発明の第1の実施形態によるモールド封止型GaN系発光ダイオードにおけるGaN系発光ダイオードを示す断面図である。

【図2】この発明の第1の実施形態によるモールド封止型GaN系発光ダイオードを示す断面図である。

【図3】この発明の第2の実施形態によるモールド封止型GaN系発光ダイオードを示す断面図である。

【図4】この発明の第2の実施形態によるフリップチップ実装GaN系半導体レーザを示す断面図である。

【図5】この発明の第3の実施形態によるGaN系半導体レーザ装置を示す断面図である。

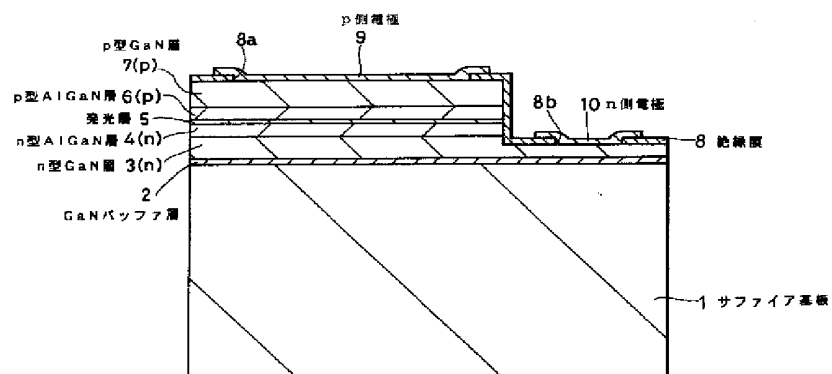
【図6】この発明の第4の実施形態によるGaN系半導体レーザ装置を示す断面図である。

【図7】従来のモールド封止型GaN系発光ダイオードを示す断面図である。

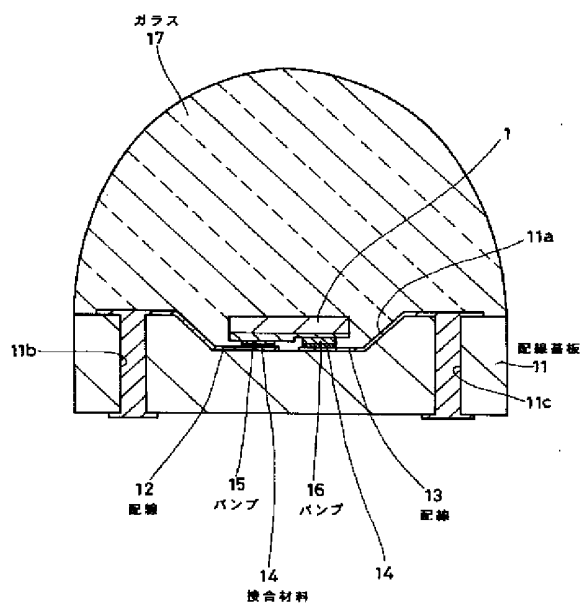
【符号の説明】

1・・・サファイア基板、9・・・p側電極、10・・・n側電極、11・・・配線基板、11a・・・凹部、12、13・・・配線、14・・・接合材料、15、16・・・パンプ、17・・・ガラス、18・・・発光領域、19・・・ヒートシンク、20・・・GaN系半導体レーザ、21・・・SiC基板、22・・・GaN系半導体層

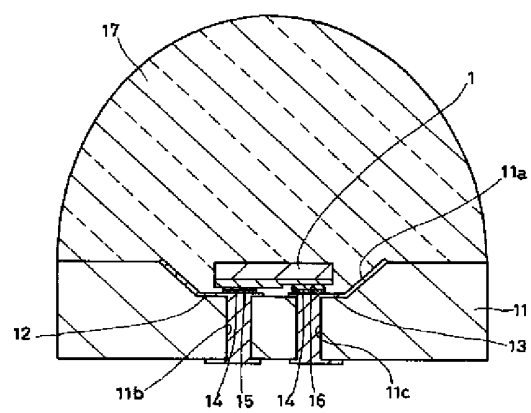
【図 1】



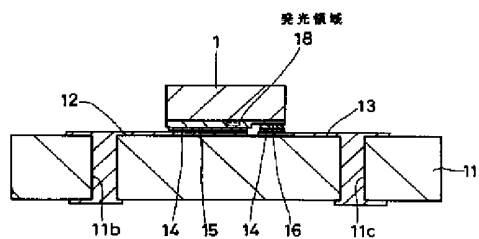
【図 2】



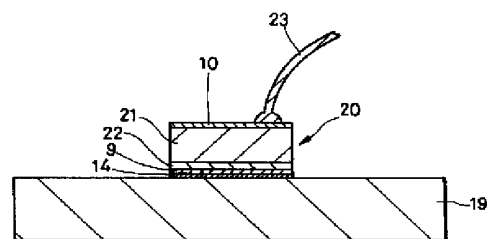
【图 3】



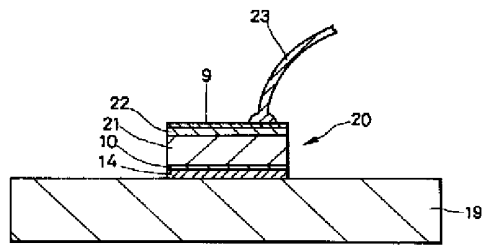
【图 4】



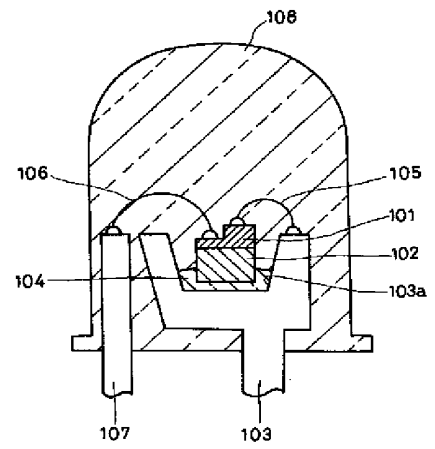
【図 5】



【図 6】



【図 7】



フロントページの続き

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H 0 1 L 29/812

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識別記号

F I

H 0 1 L 29/80

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a cross sectional view showing the GaN system light emitting diode in the mold sealing type GaN system light emitting diode by the first embodiment of this invention.

[Drawing 2]It is a cross sectional view showing the mold sealing type GaN system light emitting diode by the first embodiment of this invention.

[Drawing 3]It is a cross sectional view showing the mold sealing type GaN system light emitting diode by the second embodiment of this invention.

[Drawing 4]It is a cross sectional view showing the flip-chip-mounting GaN system semiconductor laser by the second embodiment of this invention.

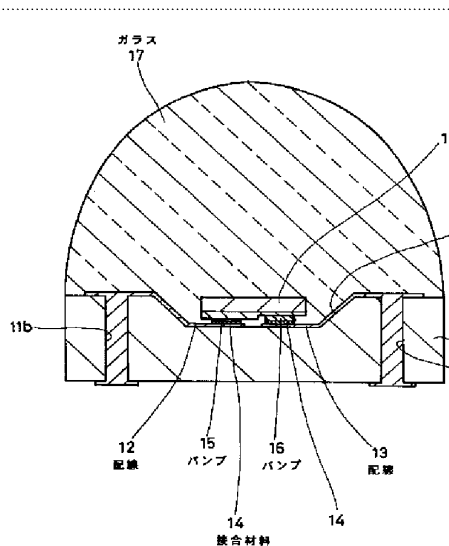
[Drawing 5]It is a cross sectional view showing the GaN system semiconductor laser device by a 3rd embodiment of this invention.

[Drawing 6]It is a cross sectional view showing the GaN system semiconductor laser device by a 4th embodiment of this invention.

[Drawing 7]It is a cross sectional view showing the conventional mold sealing type GaN system light emitting diode.

[Explanations of letters or numerals]

1 ... silicon on sapphire, 9 ... p lateral electrode and 10...n lateral electrode, 11 ... wiring substrate, 11 a ... a concave part and 12, 13 ... wiring, 14 ... a cementing material and 15, 16 ... bump, 17 ... glass, 18 ... luminous region, 19 ... heat sink, 20 ... GaN system semiconductor laser, 21 ... SiC substrate, 22 ... GaN system semiconductor layer



Representative drawing

Representative drawing | 1 | 2 | 3 | 4 | 5 | 6 | 7

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]Especially this invention is applied to the light emitting diode using a nitride system group III-V semiconductor, a semiconductor laser, or an electronic run element about a semiconductor device and a semiconductor emission device, and is suitable.

[0002]

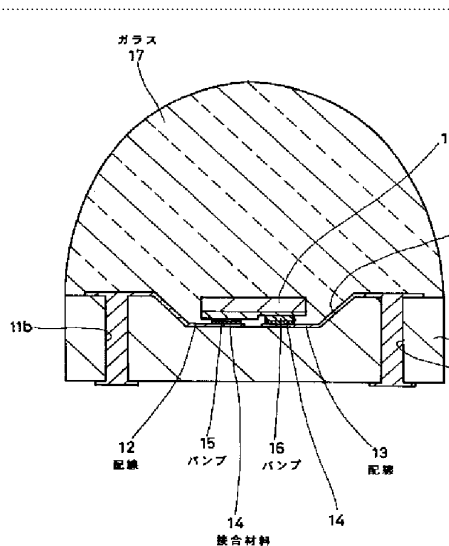
[Description of the Prior Art]From green as blue and a semiconductor emission device which can emit light for ultraviolet rays further, The GaN system light emitting diode which grew epitaxially the nitride system group III-V semiconductor represented by gallium nitride (GaN) on silicon on sapphire, a SiC substrate, etc., and formed light emitting diode structure is known.

[0003]Such a GaN system light emitting diode is used after mold sealing has been performed by resin, as usually shown in Fig.7 (for example, JP,H8-78727,A). Namely, in [as shown in Fig.7] this mold sealing type GaN system light emitting diode, The back surface of the silicon on sapphire 102 in which the GaN system semiconductor layer 101 which forms light emitting diode structure was laminated is adhered to the bottom surface of the concave part 103a provided by the upper part of the leadframe 103 with the adhesives 104. The bottom surface and inner wall surface of this concave part 103a are a reflective surface for taking out outside the light which occurs from the luminous layer of a GaN system light emitting diode at the time of operation. The adhesives of the epoxy resin system are used as the adhesives 104. In this case, p lateral electrode and n lateral electrode (not shown) of the GaN system light emitting diode are provided at the same side as the GaN system semiconductor layer 101, Bonding of the p lateral electrode is carried out to the leadframe 103 by the wire 105, and bonding of the n lateral electrode is carried out to the leadframe 107 by the wire 106. And the mold of the GaN system light emitting diode is carried out to lens shape by the resin 108 with the leadframes 103 and 107 of the portion of the neighborhood for the purpose of giving a condensing function etc. Generally as the resin 108, the water-white epoxy resin is used.

[0004]

[Problem to be solved by the invention]However, in the above-mentioned conventional mold sealing type GaN system light emitting diode, although the GaN system light emitting diode had not deteriorated when use was continued and it went, brightness degradation arose on rapid degradation with the passage of time and a concrete target, and they had a reliability top problem. This is for transmissivity to be deteriorated, when the epoxy resin used as the resin 108 discolors or colors optically under the influence of the light which occurs from the luminous layer of a GaN system light emitting diode at the time of operation (for example, JP,H8-148717,A).

[0005]On the other hand, when it mounts a light emitting device, compared with the packaging system by wire bonding etc., there is the flip chip method by a small space as a packaging system in which high density assembly is possible (for example, JP,H6-104480,A, JP,H6-177429,A, JP,H5-326520,A). In this flip chip method, the Pb-Sn system alloy and Au-Sn system alloy of eutectic composition are usually used as a cementing material (for example, JP,H5-90329,A). However, when a GaN system light emitting diode is mounted by the flip chip method using these cementing materials. Since the melting point of those cementing materials is as low as 280 degrees C or less (for example, the eutectic temperature of Pb-61.9wt%Sn 183 degrees C) When the eutectic temperature of Au-90wt%Sn was used under the heating collar boundary according [the eutectic temperature of 217 degrees C and Au-20wt%Sn] to 278 degrees C and high density assembly, and within high temperature environment, the



Representative drawing

Representative drawing 1 2 3 4 5 6 7

cementing material carried out melting, the defect arose, and it had a reliability top problem. In the GaN system electronic run element which attracts attention as a semiconductor device for big electric power, this problem may arise similarly again.

[0006]Therefore, the object of this invention is to provide the semiconductor emission device which can prevent the brightness degradation by optical discoloration or coloring of a sealing material.

[0007]Other objects of this invention are to provide the semiconductor device of an usable resistance to environment under a heating collar boundary and within hot environments.

[0008]

[Means for solving problem]To achieve the above objects, first invention of this invention, In the semiconductor device with which the surface of the nitride system group III-V semiconductor layer of a substrate or the main surface of another side of a substrate where the nitride system group III-V semiconductor layer which forms element structure was laminated on one main surface was joined on the base, The metallic material which has the melting point above 300 degrees C and below 700 degrees C was used as a cementing material.

[0009]That the maximum of the melting point of a cementing material was 700 degrees C here, Since a GaInN layer usually grows at the temperature of 700-800 degrees C among the nitride system group III-V semiconductor layers used for a semiconductor emission device etc., it is because welding temperature is restricted to 700 degrees C or less which is a minimum of the growing temperature of this GaInN layer. On the other hand, the minimum of the melting point of a cementing material was 300 degrees C in order to improve the heat resistance of a junction compared with the former.

[0010]In first invention of this invention, the metallic material which has the melting point above 350 degrees C and below 700 degrees C is used as a cementing material from a viewpoint of obtaining higher heat resistance.

[0011]If the example of the metallic material used as a cementing material is given in first invention of this invention, A Pb-Pd system, an Au-Ga system, an Au-germanium system, an Au-Si system, an Al-Zn system, It is an alloy of an Al-germanium system, an Al-Mg system, an Au-In system, an Ag-Mg system, an Al-Cu system, an Al-Si system, an Al-Si-Mg system, an Al-Si-Zn system, an Al-Pd system, an Al-In system, a Cu-germanium system, an Ag-germanium system, a Cu-In system, or an Au-Zn system. It is as follows when the eutectic composition and eutectic temperature of these alloys are shown (ASM Handbook, Volume 3, Alloy Phase Diagrams(ASM International, 1992)).).

[0012]

Alloy Eutectic temperature (degree C)

Pb-25wt%Pd 474 Au-31wt%Ga. 448.6 Au-15.2wt%Ga 339.4. Au-12.5wt%germanium 361 Au-3.2wt%Si. 363 Al-94wt%Zn 381 Al-51.6wt%germanium 420 Al-66wt%Mg 437 Au-41.9wt%In 495.4 Ag-51.39wt%Mg 472 Al-32wt%Cu 548.2. Al-12.6wt%Si 577 Al-24wt%Pd 615 Al-17.3wt%In 639 Cu-60.4wt%germanium 644 Ag-82wt%germanium 651 Au-34wt%Zn 667 Au-12wt%Zn 683 -- in addition, Although it is not eutectic composition, the melting point of Cu-38.4wt%In is 678 degrees C.

[0013]Typically in first invention of this invention, a semiconductor device is a semiconductor emission device with which a nitride system group III-V semiconductor layer forms light emitting element structure. In this case, a substrate has a light transmitting property, for example, p lateral electrode and n lateral electrode are provided about this substrate at the same side as a nitride system group III-V semiconductor layer. And the surface of a nitride system group III-V semiconductor layer is joined on a base so that p lateral electrode and n lateral electrode may electrically be connected with the first polar zone provided by the base and the second polar zone, respectively. The concave part which has the reflecting structure for making a base reflect suitably the light which occurs from a nitride system group III-V semiconductor layer is provided, and the surface of the nitride system group III-V semiconductor layer of a substrate is joined to the bottom surface of this concave part. A base is a wiring substrate and can form the reflecting structure of a concave part with the wiring provided by this wiring substrate in this case. This base may be a leadframe, a header, etc.

[0014]In first invention of this invention, a semiconductor device may be a field effect transistor (FET) etc. at an electronic run element and a concrete target.

[0015]The surface of the nitride system group III-V semiconductor layer of the substrate of a light transmitting property or the main surface of another side of a substrate where the nitride system group III-V semiconductor layer in which second invention of this invention forms light emitting element structure was laminated on one main surface is joined on a base, The inorganic material which a substrate has the melting point of 700 degrees C or less in the semiconductor emission device sealed with the sealing material more highly as a sealing material than 350 degrees C, and has a light transmitting property was used.

[0016]That the maximum of the melting point of a sealing material was 700 degrees C here, Since a GaInN layer usually grows at the temperature of 700-800 degrees C among the nitride system group III-V semiconductor layers used for a semiconductor emission device etc., it is because sealing temperature is restricted to 700 degrees C or less which is a minimum of the growing temperature of this GaInN layer. On the other hand, the minimum of the melting point of a sealing material was 350 degrees C in order to obtain sufficient heat resistance.

[0017]In second invention of this invention, the melting point of the inorganic material used as a sealing material is lower than the temperature of junction suitably. Typically, this inorganic material is glass.

[0018]In this invention, a nitride system group III-V semiconductor layer consists of at least one kind of group III elements chosen from Ga, Al, In, and the group which consists of B, and a V group element which contains at least N and contains As or P further by a case. When the example of this nitride system group III-V semiconductor layer is given, they are a GaN layer, an AlGaIn layer, a GaInN layer, an AlGaInN layer, etc.

[0019]In first invention of this invention constituted as mentioned above, By having used the

metallic material which has the melting point above 300 degrees C and below 700 degrees C as a cementing material, the heat resistance of a junction improves compared with the case where a Pb-Sn system alloy and an Au-Sn system alloy are used as a cementing material like before, and the durability the bottom of a heating collar boundary and within hot environments improves.

[0020]In second invention of this invention constituted as mentioned above, By having used the inorganic material which has the melting point of 700 degrees C or less more highly as a sealing material than 350 degrees C, and has a light transmitting property, Unlike the case where resin, such as an epoxy resin, is used as a sealing material like before, the optical discoloration or coloring of a sealing material accompanying use of a semiconductor emission device can be prevented.

[0021]

[Mode for carrying out the invention]Hereinafter, while referring to Drawings for the embodiment of this invention, it describes. In the complete diagram of an embodiment, the same code is given to the portion which is the same or corresponds.

[0022]First, it describes about the mold sealing type GaN system light emitting diode by the first embodiment of this invention. Fig.1 shows a GaN system light emitting diode, and Fig.2 shows the mold sealing type GaN system light emitting diode which sealed with glass the GaN system light emitting diode shown in Fig.1.

[0023]As shown in Fig.1, in this GaN system light emitting diode, GaN buffer layer 2, the n type GaN layer 3, the n type AlGaIn layer 4, the luminous layer 5 which consists of GaInN, the p type AlGaIn layer 6, and the p type GaN layer 7 are successively laminated, for example on the silicon on sapphire 1 of c surface. Here, the upper levels, the n type AlGaIn layer 4, the luminous layer 5, the p type AlGaIn layer 6, and the p type GaN layer 7 of the n type GaN layer 3 are patterned in mesa shape. The insulator layer 8 like a SiO₂ film is provided so that these surfaces may be covered. This insulator layer 8 is a thing for electric insulation and a surface protection. The openings 8a and 8b are provided by this insulator layer 8, respectively on the p type GaN layer 7 and the n type GaN layer 3. And while the p lateral electrode 9 is in contact with the p type GaN layer 7 through the opening 8a, the n lateral electrode 10 is in contact with the n type GaN layer 3 through the opening 8b. As the p lateral electrode 9, for example, nickel/Au membrane are used, and for example, Ti/Al/Au membrane are used as the n lateral electrode 10.

[0024]In the mold sealing type GaN system light emitting diode shown in Fig.2, the GaN system light emitting diode shown in Fig.1 turns the GaN system semiconductor layer down, and flip chip mounting is carried out to the bottom surface of the concave part 11 which has the sectional shape of the shape of an inverted trapezium provided by the upper part of the wiring substrate 11.

[0025]That is, the wiring 12 and 13 of the prescribed pattern is provided by the top surface of the wiring substrate 11 so that it may apply to the flat part of the outside of the concave part 11a and may extend from the bottom surface of the concave part 11a. These wiring 12 and 13 has extended to the lower surface of the wiring substrate 11 further through the through holes 11b and 11c provided by the wiring substrate 11, and the portion projected from this lower surface constitutes the polar zone. The end of the wiring 12 and 13 on the bottom surface of the concave part 11a constitutes the polar zone (pad section), and the cementing material 14 is provided on these polar zone. And for example, it provided, respectively on the p lateral electrode 9 of the GaN system light emitting diode shown in Fig.1, and the n lateral electrode 10, it is joined to the polar zone of the end of the wiring 12 and 13 with the cementing material 14, respectively, and the bumps 15 and 16 which consists of Au are mechanically and electrically connected mutually. Here, the role of the reflector for these wiring 12 and 13 reflecting the light which occurs from the luminous layer 5 of a GaN system light emitting diode, and taking it out outside also performs.

[0026]In this case, what was chosen from among the metallic materials which have the previously quoted melting point above 300 degrees C and below 700 degrees C as the cementing material 14 if needed is used, and, specifically, Au-41.9wt%In whose eutectic temperature is 495.4 degrees C is used, for example.

[0027]It has the heat-resistant temperature and electrical insulation higher than the welding temperature by the cementing material 14, and the temperature of the below-mentioned mold sealing at least as the wiring substrate 11, what has still better heat conduction is used, and a specific for example, ceramic board like an alumina substrate is used.

[0028]In this case, mold sealing of the GaN system light emitting diode is carried out to lens shape with the glass 17 with the top surface of the wiring substrate 11. As this glass 17, the melting point is higher than 350 degrees C, the thing of a light transmitting property is used below 700 degrees C, and what mixed PbO, B₂O₃, Na₂O, ZnO, etc. is specifically used for SiO₂. For example, the glass which mixed PbO and B₂O₃ to SiO₂ has the melting point of 430-490 degrees C. PbO and B₂O₃ can be made into a subject and the melting point of 350-400 degrees C can be obtained also with the glass in which SiO₂ is hardly contained.

[0029]Although thermal expansion coefficient difference is between the wiring substrate 11 and the glass 17 depending on the combination of the material of the wiring substrate 11, and the material of the glass 17 and the glass 17 after this sealing may be made to produce a crack etc., In this case, this problem is solvable by putting a transparent filler with a small coefficient of thermal expansion into the glass 17, and making sufficient small thermal expansion coefficient difference between the wiring substrate 11 and the glass 17.

[0030]Next, it describes about the manufacturing method of the mold sealing type GaN system light emitting diode constituted as mentioned above.

[0031]First, the cementing material 14 is formed by vacuum deposition method, sputtering process, the plating method, etc. on the polar zone of the end of the wiring 12 and 13 of the bottom surface of the concave part 11a of the wiring substrate 11. On the other hand, on the p lateral electrode 9 of the GaN system light emitting diode shown in Fig.1, and the n lateral

electrode 10, the bumps 15 and 16 are formed for example, by the ball bonding method etc. And alignment is carried out and the bumps 15 and 16 formed on the p lateral electrode 9 and the n lateral electrode 10 put a GaN system light emitting diode on the bottom surface of the concave part 11a of the wiring substrate 11 so that it may come on the cementing material 14 formed on the polar zone of the end of the wiring 12 and 13. Then, a reflow of through and the cementing material 14 is carried out into the reflow furnace (not shown) heated in this wiring substrate 11 by the temperature more than the melting point of the cementing material 14. The bumps 15 and 16 of a GaN system light emitting diode and the end of the wiring 12 and 13 are joined with this cementing material 14 by this.

[0032]Next, mold sealing of the GaN system light emitting diode by which did in this way and flip chip mounting was carried out on the wiring substrate 11 is carried out with the glass 17. This mold sealing can be performed specifically, for example, as follows.

[0033]In a first method, powdered raw materials for glass are paid to the mold of a mold, for example, the top surface of the wiring substrate 11 by which flip chip mounting of the GaN system light emitting diode was carried out to the raw materials for glass in this mold is pressed, a mold is heated to a temperature higher than the melting point of raw materials for glass in this state, and melting of the raw materials for glass is carried out. Then, a mold is cooled and the wiring substrate 11 is taken out. Mold sealing of the GaN system light emitting diode is carried out with the glass 16 by this. In this method, by using powdered raw materials for glass, it is easy to pay raw materials for glass to a mold, and there is an advantage of becoming easy to carry out melting according to increase of the surface area of raw materials for glass.

[0034]In a second method, powdered raw materials for glass are heaped up so that a GaN system light emitting diode may cover this GaN system light emitting diode on the top surface of the wiring substrate 11 by which flip chip mounting was carried out. In this case, it may shape in predetermined form beforehand by pressing raw materials for glass. Next, it cools, after carrying out melting of the raw materials for glass and rising this melting glass to lens shape with surface tension by heating this wiring substrate 11 to a temperature higher than the melting point of raw materials for glass. Mold sealing of the GaN system light emitting diode is carried out with the glass 16 by this. Here, heating by a heating furnace, lamp heating, condensing heating, spraying of a hot wind, etc. can perform heating for carrying out melting of the raw materials for glass.

[0035]In the 3rd method, melting glass is heaped up to lens shape so that a GaN system light emitting diode may cover this GaN system light emitting diode on the top surface of the wiring substrate 11 by which flip chip mounting was carried out, and it cools after that. Mold sealing of the GaN system light emitting diode is carried out with the glass 16 by this. In this case, self-formation of this melting glass can be carried out by the surface tension of melting glass at lens shape.

[0036]As mentioned above, according to this first embodiment, the melting point uses the metallic material above 300 degrees C and below 700 degrees C as the cementing material 14 for carrying out flip chip mounting of the GaN system light emitting diode, When the melting point uses the glass 17 of the light transmitting property above 350 degrees C and below 700 degrees C as a sealing material of a GaN system light emitting diode, the mold sealing type GaN system light emitting diode of a resistance to environment in which the durability outstanding also the bottom of a heating collar boundary and within hot environments is shown is realizable. This mold sealing type GaN system light emitting diode, Temporal brightness degradation can be prevented from discoloration or coloring of a sealing material not arising with use, and arising like [at the time of using resin, such as an epoxy resin, as a sealing material], by using the glass 17 which is an inorganic material as a sealing material. When the wiring 12 and 13 of the wiring substrate 11 performs [the role of a reflector], even if it does not independently provide reflecting structure, the light which occurs from a GaN system light emitting diode can be taken out outside efficiently.

[0037]Next, it describes about the mold sealing type GaN system light emitting diode by the second embodiment of this invention. This mold sealing type GaN system light emitting diode is shown in Fig.3.

[0038]As shown in Fig.3, in the mold sealing type GaN system light emitting diode by this second embodiment, the through holes 11b and 11c of the wiring substrate 11 are provided directly under the bumps 15 and 16. And the wiring 12 and 13 is provided by only the bottom surface and inner wall surface of the concave part 11a, and it has not extended in the flat part of the outside of this concave part 11a. Since other is the same as that of the mold sealing type GaN system light emitting diode by a first embodiment, a description is omitted.

[0039]Since the manufacturing method of the mold sealing type GaN system light emitting diode by this second embodiment is the same as the manufacturing method of the mold sealing type GaN system light emitting diode by a first embodiment, a description is omitted.

[0040]Next, it describes about the flip-chip-mounting GaN system semiconductor laser by a 3rd embodiment of this invention. This flip-chip-mounting GaN system semiconductor laser is shown in Fig.4.

[0041]As shown in Fig.4, in the flip-chip-mounting GaN system semiconductor laser by this 3rd embodiment, on the wiring substrate 11, the GaN system semiconductor laser which has the same structure as the GaN system light emitting diode shown in Fig.1 turns that GaN system semiconductor layer down, and flip chip mounting is carried out. That is, on the p lateral electrode 9 of a GaN system semiconductor laser, and the n lateral electrode 10, it is joined to the polar zone of the end of the wiring 12 and 13 with the cementing material 14, and the bumps 15 and 16 provided, respectively are mechanically and electrically connected mutually. In this case, it is made for the luminous region 18 of the GaN system semiconductor layer of a GaN system semiconductor laser to come right above the polar zone of the end of the wiring 12. This is because temperature rises most at the time of operation of a GaN system semiconductor laser, so the luminous region 18 of this GaN system semiconductor layer needs

to cool by making the wiring 12 and also the wiring substrate 11 conduct promptly the heat which occurred in this luminous region 18. The wiring substrate 11 has the same structure as the wiring substrate 11 in the mold sealing type GaN system light emitting diode by a first embodiment except for the top surface which is a component side being flat.

[0042] Since it is the same as that of a first embodiment about the cementing material 14 and the material of the wiring substrate 11, a description is omitted.

[0043] The flip-chip-mounting GaN system semiconductor laser by this 3rd embodiment can be manufactured by the method of the flip chip mounting in the manufacturing method of the mold sealing type GaN system light emitting diode by a first embodiment, and the same method.

[0044] When the melting point uses the metallic material above 300 degrees C and below 700 degrees C as the cementing material 14 for carrying out flip chip mounting of the GaN system semiconductor laser according to this 3rd embodiment, The flip-chip-mounting GaN system semiconductor laser of a resistance to environment in which the durability outstanding also the bottom of a heating collar boundary and within hot environments is shown is realizable.

[0045] Next, it describes about the GaN system semiconductor laser device by a 4th embodiment of this invention. This GaN system semiconductor laser device is shown in Fig.5.

[0046] As shown in Fig.5, in the GaN system semiconductor laser device by this 4th embodiment, the GaN system semiconductor laser 20 is mounted, for example on the heat sink 19 made from Cu. In this case, although the same GaN system semiconductor layer 22 as the GaN system light emitting diode shown in Fig.1 is laminated on the surface of conductive SiC substrate 21, laser structure is formed and the p lateral electrode 9 is formed on this GaN system semiconductor layer 22, this GaN system semiconductor laser 20, The n lateral electrode 10 is formed in the back surface of SiC substrate 21. And it is joined to the heat sink 19 with the cementing material 14, and the p lateral electrode 9 of this GaN system semiconductor laser 20 is mechanically and electrically connected mutually. As this cementing material 14, what was used, and the same thing can be used as the cementing material 14 in a first embodiment. On the other hand, the electrical link of the n lateral electrode 10 is performed by carrying out bonding of the wire 23 made from Au, for example.

[0047] When the melting point uses the metallic material above 300 degrees C and below 700 degrees C as the cementing material 14 for mounting the GaN system semiconductor laser 20 according to this 4th embodiment, The GaN system semiconductor laser device of a resistance to environment in which the durability outstanding also the bottom of a heating collar boundary and within hot environments is shown is realizable.

[0048] Next, it describes about the GaN system semiconductor laser device by the fifth embodiment of this invention. This GaN system semiconductor laser device is shown in Fig.6.

[0049] As shown in Fig.6, in the GaN system semiconductor laser device by this fifth embodiment, the n lateral electrode 10 of the GaN system semiconductor laser 20 is joined to the heat sink 19 with the cementing material 14. And bonding of the wire 23 is carried out to the p lateral electrode 9. Since other is the same as that of the GaN system semiconductor laser device by a 4th embodiment, a description is omitted.

[0050] According to this fifth embodiment, the same advantage as a 4th embodiment can be acquired.

[0051] As mentioned above, although specifically described about the embodiment of this invention, this invention is not limited to an above-mentioned embodiment, and various kinds of deformation based on the technical idea of this invention is possible for it.

[0052] For example, in 1st, 2nd, and 3rd above-mentioned embodiments, junction by weld can be performed more easily and reliably by forming the cementing material 14 also in the surface of the bumps 15 and 16. Low temperature-ization of welding temperature can be attained by using an ultrasonic bonding method and a thermocompression bonding method for weld by the cementing material 14.

[0053] The Au membrane of a thick film is formed, for example by the plating method etc., and it may be made to enlarge a plane-of-composition product instead of the bumps 15 and 16 in 1st, 2nd, and 3rd above-mentioned embodiments.

[0054] In 1st, 2nd, and 3rd above-mentioned embodiments, although the silicon on sapphire 1 is used as a substrate of a GaN system light emitting diode or a GaN system semiconductor laser, Other substrates, specifically SiC substrate, GaN substrates, etc. may be used instead of this silicon on sapphire 1 if needed. Similarly, in the 4th and a fifth embodiment, a GaN substrate may be used instead of SiC substrate 21.

[0055] Although it described in the above-mentioned 4th and fifth embodiment about the case where this invention is applied to the GaN system semiconductor laser of double hetero structure, This invention can also be applied to the so-called GaN system semiconductor laser of the SCH (Separate Confinement Heterostructure) structure which provided the lightguide between the active layer and the cladding layer. The thing of multiple quantum well structure (MQW) or single quantum well structure (SQW) may be used as an active layer. It is possible to use various kinds of laser structures, such as a ridge waveguide type which realizes a gain guided wave and a refractive-index guided wave, an internal strangulation type, a structural substrate type, and a vertical microcavity control type (a distributed feedback (DFB) type or a Bragg reflection (DBR) type), as laser structure.

[0056] In above-mentioned the 1st, the 2nd, the 3rd, the 4th, and fifth embodiment, although described about the case where this invention is applied to a GaN system light emitting device, also when it mounts GaN system FET, for example, this invention can be applied.

[0057]

[Effect of the Invention] By having used the metallic material which has the melting point above 300 degrees C and below 700 degrees C as a cementing material according to the semiconductor device by this invention, as described above, The heat resistance of a junction can improve compared with the case where a Pb-Sn system alloy and an Au-Sn system alloy are used as a cementing material like before, and it can provide the semiconductor device of an

usable resistance to environment under a heating collar boundary and within hot environments by this.

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[0058]By having used the inorganic material which has the melting point of 700 degrees C or less more highly as a sealing material than 350 degrees C, and has a light transmitting property according to the semiconductor emission device by this invention, Unlike the case where resin, such as an epoxy resin, is used as a sealing material like before, the optical discoloration or coloring of a sealing material accompanying use of a semiconductor emission device can be prevented, and the brightness degradation by optical discoloration or coloring of a sealing material can be prevented by this.

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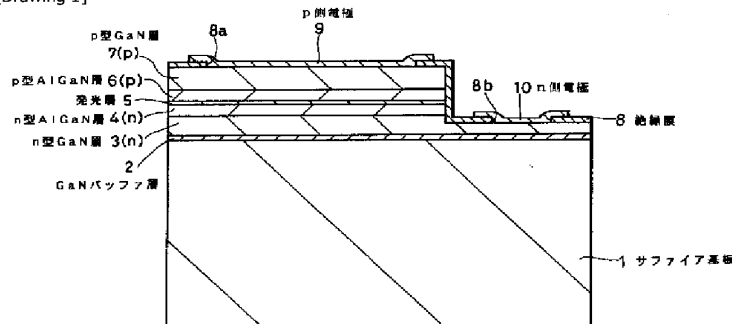
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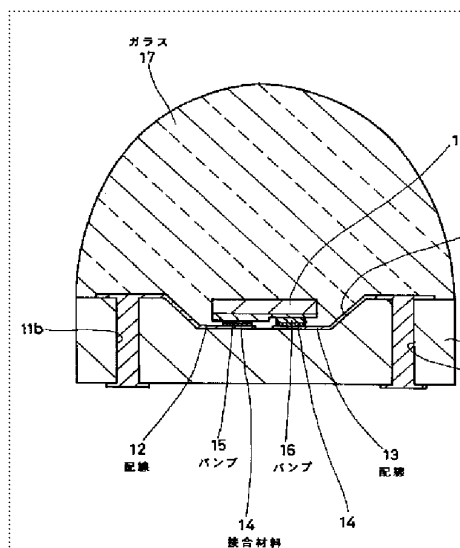
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DRAWINGS

[Drawing 1]

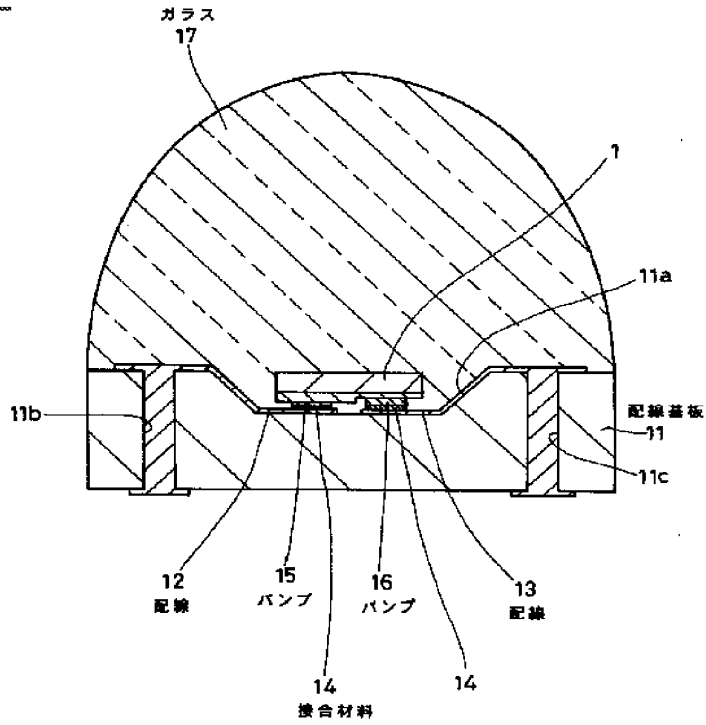


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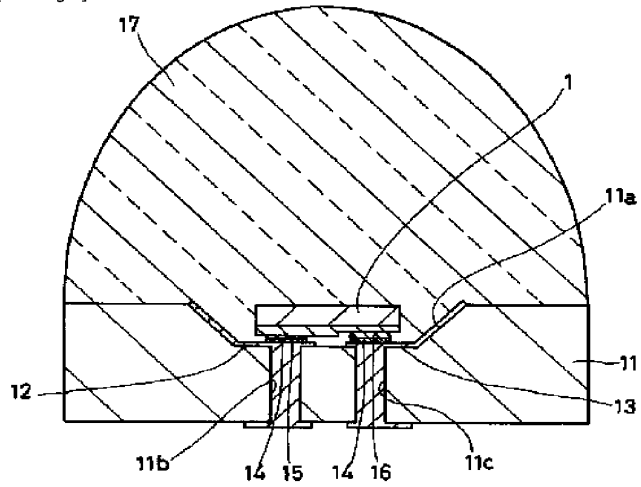


Representative drawing

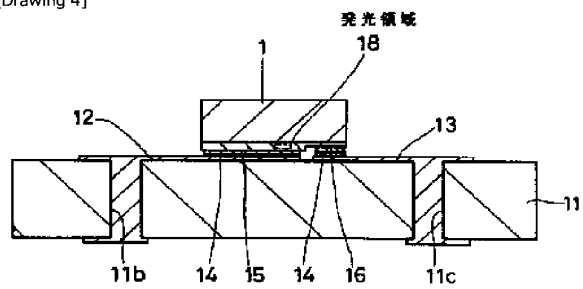
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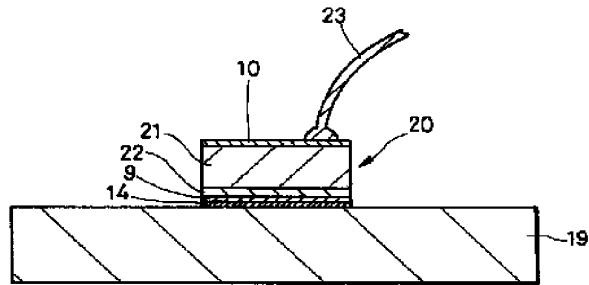
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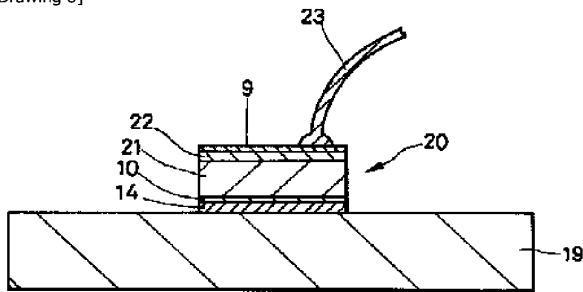
[Drawing 4]



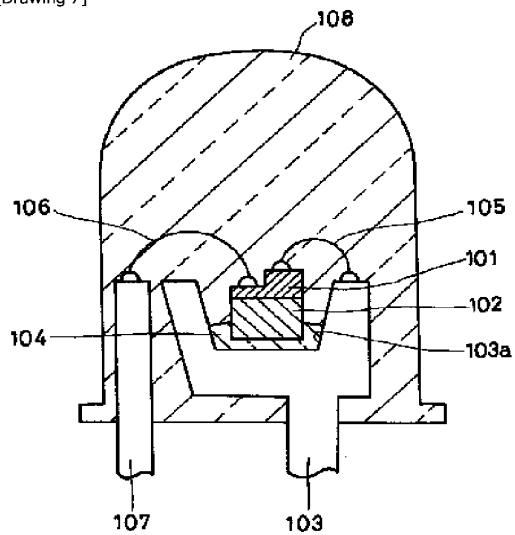
[Drawing 5]



[Drawing 6]



[Drawing 7]



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CLAIMS DETAILED DESCRIPTION

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CLAIMS

[Claim(s)]

[Claim 1]In a semiconductor device with which the surface of the above-mentioned nitride system group III-V semiconductor layer of a substrate or a main surface of another side of the above-mentioned substrate where a nitride system group III-V semiconductor layer which forms element structure was laminated on one main surface was joined on a base, A semiconductor device using a metallic material which has the melting point above 300 degrees C and below 700 degrees C as a cementing material.

[Claim 2]The semiconductor device according to claim 1 using a metallic material which has the melting point above 350 degrees C and below 700 degrees C as a cementing material.

[Claim 3]The above-mentioned metallic material A Pb-Pd system, an Au-Ga system, an Au-germanium system, an Au-Si system, An Al-Zn system, an Al-germanium system, an Al-Mg system, an Au-In system, an Ag-Mg system, The semiconductor device according to claim 1 being an alloy of an Al-Cu system, an Al-Si system, an Al-Si-Mg system, an Al-Si-Zn system, an Al-Pd system, an Al-In system, a Cu-germanium system, an Ag-germanium system, a Cu-In system, or an Au-Zn system.

[Claim 4]The above-mentioned semiconductor device is a semiconductor emission device with which the above-mentioned nitride system group III-V semiconductor layer forms light emitting element structure, The above-mentioned substrate has a light transmitting property, and p lateral electrode and n lateral electrode are provided about the above-mentioned substrate at the same side as the above-mentioned nitride system group III-V semiconductor layer, The semiconductor device according to claim 1, wherein the surface of the above-mentioned nitride system group III-V semiconductor layer is joined on the above-mentioned base so that the above-mentioned p lateral electrode and the above-mentioned n lateral electrode may electrically be connected with first polar zone provided by the above-mentioned base and second polar zone, respectively.

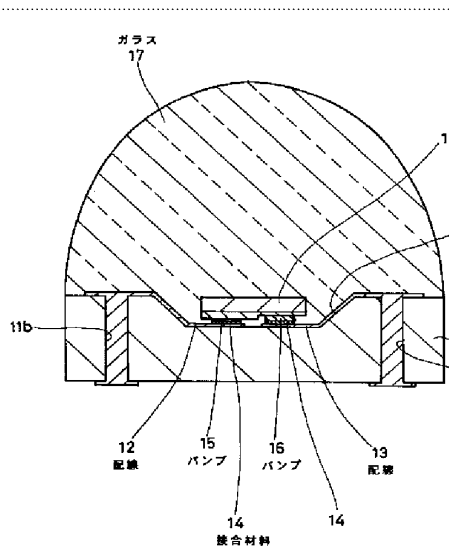
[Claim 5]The semiconductor device according to claim 4, wherein a concave part which has the reflecting structure for making the above-mentioned base reflect light which occurs from the above-mentioned nitride system group III-V semiconductor layer is provided and the surface of the above-mentioned nitride system group III-V semiconductor layer of the above-mentioned substrate is joined to a bottom surface of this concave part.

[Claim 6]The semiconductor device according to claim 5 which the above-mentioned base is a wiring substrate and is characterized by forming the above-mentioned reflecting structure of the above-mentioned concave part with the wiring provided by the above-mentioned wiring substrate.

[Claim 7]The semiconductor device according to claim 1, wherein the above-mentioned semiconductor device is an electronic run element.

[Claim 8]The surface of the above-mentioned nitride system group III-V semiconductor layer of a substrate of a light transmitting property or a main surface of another side of the above-mentioned substrate where a nitride system group III-V semiconductor layer which forms light emitting element structure was laminated on one main surface is joined on a base, A semiconductor emission device using an inorganic material which the above-mentioned substrate has the melting point of 700 degrees C or less in a semiconductor emission device sealed with a sealing material more highly as the above-mentioned sealing material than 350 degrees C, and has a light transmitting property.

[Claim 9]The semiconductor emission device according to claim 8, wherein the melting point of the above-mentioned inorganic material is lower than temperature of the above-mentioned



Representative drawing

Representative drawing 1 2 3 4 5 6 7

junction.

[Claim 10]The semiconductor emission device according to claim 8, wherein the above-mentioned inorganic material is glass.

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最終頁に続く

(54) 【発明の名称】 窒化物半導体発光素子及び発光装置並びにそれらの製造方法

(57) 【特許請求の範囲】

【請求項1】

透光性基板の一方の主面上に、n型窒化ガリウム系化合物半導体層と発光層とp型窒化ガリウム系化合物半導体層とが形成されてなる窒化物半導体発光素子と、該窒化物半導体発光素子がフリップチップ実装されるパッケージと、を有する発光装置において、

上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することによりSiO₂層が上記透光性基板の他方の主面上に形成され、該SiO₂層が形成された透光性基板を個々の素子ごとに分割して前記窒化物半導体発光素子が作製され、

前記SiO₂層を介して光が出力されることを特徴とする発光装置。

【請求項2】

上記発光層は紫外領域の光を発光し、かつ上記蛍光体は、

(1) Re₅(PO₄)₃Q:Eu, Re' (但し、ReはMg、Ca、Ba、Sr、Znから選択される少なくとも1種と、Qはハロゲン元素のF、Cl、Br、Iから選択される少なくとも1種と、Re'はMn、Fe、Cr、Snから選択される少なくとも1種とを有する。)

(2) Re₅(PO₄)₃Q:Eu (但し、ReはSr、Ca、Ba、Mgから選択される少なくとも1種、Qはハロゲン元素のF、Cl、Br、Iから選択される少なくとも1種とを有する。)、

10

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- (3) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$ 、
 (4) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}, \text{Mn}$ 、
 (5) $(\text{SrEu})\text{O} \cdot \text{Al}_2\text{O}_3$ 、
 (6) $3 \cdot 5\text{MgO} \cdot 0.5\text{MgF}_2 \cdot \text{GeO}_2:\text{Mn}$ 、
 (7) $\text{Y}_2\text{O}_3\text{S}:\text{Eu}$ 、
 (8) $\text{Mg}_6\text{As}_2\text{O}_{11}:\text{Mn}$ 、
 (9) $\text{Gd}_2\text{O}_3\text{S}:\text{Eu}$ 及び
 (10) $\text{La}_2\text{O}_3\text{S}:\text{Eu}$ からなる群から選択された少なくとも 1 つの蛍光体を含む請求項 1 記載の発光装置。

【請求項 3】

上記発光層は青色の光を発光し、かつ上記蛍光体は、Ce で付活されたイットリウム・アルミニウム・ガーネット (YAG) 系蛍光体である請求項 1 記載の発光装置。

【請求項 4】

前記窒化物半導体発光素子の上記透光性基板の一方の主面上に複数の発光領域が形成され、その発光領域がそれぞれ、上記 n 型窒化ガリウム系化合物半導体層と上記発光層と上記 p 型窒化ガリウム系化合物半導体層を含んでなる請求項 1 ～ 3 のうちのいずれか 1 つに記載の発光装置。

【請求項 5】

上記複数の発光領域はそれぞれ長方形に形成され、かつその短辺方向に並置された請求項 4 記載の発光装置。

【請求項 6】

上記複数の発光領域が直列に接続された請求項 4 又は 5 記載の発光装置。

【請求項 7】

上記複数の発光領域が並列に接続された請求項 4 又は 5 記載の発光装置。

【請求項 8】

透光性基板の一方の主面上にそれぞれ n 型窒化ガリウム系化合物半導体層と発光層と p 型窒化ガリウム系化合物半導体層を含んでなる複数の発光領域を形成する工程と、

前記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することにより、蛍光体を含む SiO_2 層を前記透光性基板の他方の主面上に形成する工程と、

前記 SiO_2 層が形成された透光性基板を個々の素子ごとに分割して、窒化物半導体発光素子を作製する工程と、

前記窒化物半導体発光素子をパッケージにフリップチップ実装する工程と、
 を有することを特徴とする発光装置の製造方法。

【請求項 9】

透光性基板の一方の主面上に、n 型窒化ガリウム系化合物半導体層と発光層と p 型窒化ガリウム系化合物半導体層とが形成されてなる窒化物半導体発光素子において、

上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することにより SiO_2 層が上記透光性基板の他方の主面上に形成され、
 該 SiO_2 層が形成された透光性基板を個々の素子ごとに分割することにより作製され、
 該 SiO_2 層を介して光が出力されることを特徴とする窒化物半導体発光素子。

【請求項 10】

透光性基板の一方の主面上にそれぞれ n 型窒化ガリウム系化合物半導体層と発光層と p 型窒化ガリウム系化合物半導体層を含んでなる複数の発光領域を形成する工程と、

上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することにより、蛍光体を含む SiO_2 層を上記透光性基板の他方の主面上に形成する工程と、

前記 SiO_2 層が形成された透光性基板を個々の素子ごとに分割する工程と、
を有することを特徴とする窒化物半導体発光素子の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は窒化物半導体素子に関する。

【0002】

【従来の技術】

近年、窒化ガリウム系化合物半導体を用いて構成された発光素子チップと蛍光体とを組み合わせた、白色光の発光が可能な発光ダイオード（白色発光ダイオード）が開発され、使用されるようになってきている。この発光ダイオードは、発光素子チップから出力される青色の光の一部を蛍光体により波長変換して、その波長変換された光と発光素子チップから青色の光との混色により、白色の光を発光させるものであり、従来は、例えば、発光素子チップがマウントされたパッケージ等を蛍光体を含む樹脂でモールドすることにより作製されていた。

【0003】

【発明が解決しようとする課題】

しかしながら、従来の白色の発光ダイオードは、蛍光体を含む樹脂を用いて構成しているので、より波長の短い光を用いると樹脂が劣化するために、青色より波長の短い光の発光素子を用いて十分な信頼性を有する発光ダイオードを構成することが困難であった。

【0004】

そこで、本発明は青色より波長の短い光を発光する発光素子チップと蛍光体とを用いて構成することも可能な発光ダイオードを提供することを目的とする。

【0005】

【課題を解決するための手段】

以上の目的を達成するために、本発明に係る発光装置は、透光性基板の一方の主面上に、 n 型窒化ガリウム系化合物半導体層と発光層と p 型窒化ガリウム系化合物半導体層とが形成されてなる窒化物半導体発光素子と、該窒化物半導体発光素子がフリップチップ実装されるパッケージと、を有する発光装置において、上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することにより SiO_2 層が上記透光性基板の他方の主面上に形成され、該 SiO_2 層が形成された透光性基板を個々の素子ごとに分割して上記窒化物半導体発光素子が作製され、該 SiO_2 層を介して光が出力される。

【0006】

また、本発明に係る発光装置において、上記発光層を紫外領域の光を発光するように構成し、上記蛍光体を、

(1) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$ 、 Re' （但し、 Re は Mg 、 Ca 、 Ba 、 Sr 、 Zn から選択される少なくとも1種と、 Q はハロゲン元素の F 、 Cl 、 Br 、 I から選択される少なくとも1種と、 Re' は Mn 、 Fe 、 Cr 、 Sn から選択される少なくとも1種とを有する。）

(2) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$ （但し、 Re は Sr 、 Ca 、 Ba 、 Mg から選択される少なくとも1種と、 Q はハロゲン元素の F 、 Cl 、 Br 、 I から選択される少なくとも1種とを有する。）

(3) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$ 、

(4) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$ 、 Mn 、

(5) $(\text{SrEu})\text{O}\cdot\text{Al}_2\text{O}_3$ 、

(6) $3.5\text{MgO}\cdot 0.5\text{MgF}_2\cdot\text{GeO}_2:\text{Mn}$ 、

(7) $\text{Y}_2\text{O}_2\text{S}:\text{Eu}$ 、

(8) $\text{Mg}_6\text{As}_2\text{O}_{11}:\text{Mn}$ 、

(9) Gd_2O_3 : Eu 及び

(10) La_2O_3 : Eu からなる群から選択された少なくとも1つの蛍光体とすることができる。

このようにすると、蛍光体の発光のみが観測される発光素子を構成することができる。

【0007】

また、本発明に係る発光装置において、上記発光層を青色の光を発光するように構成し、上記蛍光体として、Ceで付活されたイットリウム・アルミニウム・ガーネット(YAG)系蛍光体を用いて構成してもよい。

【0008】

さらに、本発明に係る発光装置においては、上記窒化物半導体発光素子の上記透光性基板の一方の主面上にそれぞれ上記n型窒化ガリウム系化合物半導体層と上記発光層と上記p型窒化ガリウム系化合物半導体層を含んでなる複数の発光領域を形成するようにしてもよい。

【0009】

また、本発明に係る発光装置においては、上記複数の発光領域をそれぞれ長方形に形成し、各発光領域を短辺方向に並置するようにしてもよい。

【0010】

また、本発明に係る発光装置においては、上記複数の発光領域を直列に接続するようにしてもよいし、上記複数の発光領域を並列に接続するようにしてもよい。

また、本発明に係る発光装置の製造方法は、透光性基板の一方の主面上にそれぞれn型窒化ガリウム系化合物半導体層と発光層とp型窒化ガリウム系化合物半導体層を含んでなる複数の発光領域を形成する工程と、上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板の他方の主面にコートした後、縮合重合することにより、蛍光体を含むSiO₂層を上記透光性基板の他方の主面上に形成する工程と、上記SiO₂層が形成された透光性基板を個々の素子ごとに分割して、窒化物半導体発光素子を作製する工程と、窒化物半導体発光素子をパッケージにフリップチップ実装する工程と、を有する。

また、本発明に係る窒化物半導体発光素子は、透光性基板の一方の主面上に、n型窒化ガリウム系化合物半導体層と発光層とp型窒化ガリウム系化合物半導体層とが形成されてなる窒化物半導体発光素子において、上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板11の他方の主面にコートした後、縮合重合することによりSiO₂層を上記透光性基板の他方の主面上に形成され、該SiO₂層が形成された透光性基板を個々の素子ごとに分割して作製され、該SiO₂層を介して光が出力される。

また、本発明に係る窒化物半導体発光素子の製造方法は、透光性基板の一方の主面上にそれぞれn型窒化ガリウム系化合物半導体層と発光層とp型窒化ガリウム系化合物半導体層を含んでなる複数の発光領域を形成する工程と、上記発光層が発光する光の一部を吸収してその吸収した光の波長より長い波長の光を発光することができる蛍光体が分散されたシリカゾルを透光性基板11の他方の主面にコートした後、縮合重合することにより、蛍光体を含むSiO₂層を上記透光性基板の他方の主面上に形成する工程と、上記SiO₂層が形成された透光性基板を個々の素子ごとに分割する工程と、を有する。

【0011】

【発明の実施の形態】

以下、図面を参照しながら本発明に係る実施の形態の窒化物半導体発光素子について説明する。

実施の形態1.

本実施の形態1の窒化物半導体発光素子は、図1に示すように、例えば、 $1000\mu m \times 1000\mu m$ のサファイア透光性基板11の一方の面に長方形の3つの発光素子1, 2, 3を互いに平行に配置して、透光性基板11を介して光を出力するように構成した発光素子であって、透光性基板11の他方の面(発光観測面)に蛍光体71を含むSiO₂膜7

0を形成したことを特徴とする。

ここで、発光素子1, 2, 3はそれぞれ、紫外領域の波長を有する紫外光を発光する素子であり、蛍光体71は紫外光を吸収して所定の色の光を発生する蛍光体である。

また、本実施の形態1の窒化物半導体発光素子において、 SiO_2 膜70に含まれる蛍光体71の量は、 SiO_2 膜70を介して出力される光が実質的に蛍光体71によって波長変換された光のみになるように設定することが好ましい。

【0012】

以上のように、本実施の形態1の窒化物半導体発光素子では、従来例のように発光素子チップが発生する青色光と蛍光体により波長変換された光との混色により白色光を得るのではなく、紫外線により励起された蛍光体71が発生する所定の色の光のみを利用している

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ので、発光色のばらつきを非常に小さく抑えることができる。
すなわち、従来の混色を利用した白色発光ダイオードは、発光素子チップの発光輝度が変化すると、青色光と黄色光の割合が変化するので、青みを帯びた白色になったり黄色を帯びた白色光になったりするなど、色が変化する。

これに対して、本実施の形態1の窒化物半導体発光素子では、紫外線により励起された蛍光体71が発生する光のみを利用しているので、発光素子チップの発光輝度が変化しても蛍光体の発光色そのものはほとんど変化することではなく、発光色の変化を極めて小さくできる。

【0013】

また、従来の構成では、樹脂に含まれる蛍光体の含有量がばらついた場合においても、青色光と黄色光の割合が変化するので、色が変化するが、本実施の形態1の窒化物半導体発光素子では、蛍光体の含有量が変化しても蛍光体の発光色そのものはほとんど変化することではなく、発光色の変化を極めて小さくできる。

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また、従来の構成では、発光素子チップを基板等を実装した後に、蛍光体を含む樹脂をモールドしているので、例えば、チップの実装位置がばらついた場合に、色むらや色度ばらつきが生じるという問題があったが、本発明の構成では、発光領域と蛍光体の位置関係は常に一定とできるので、かかる問題点を解決することができる。

【0014】

次に、本実施の形態1の窒化物半導体発光素子における蛍光体71、及びその蛍光体71を含む SiO_2 層70について説明する。

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本実施の形態1において、蛍光体71として紫外光により励起されて所定の色の光を発生する蛍光体であれば用いることができ、具体例として、例えば、

(1) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$, Re' (但し、 Re は Mg 、 Ca 、 Ba 、 Sr 、 Zn から選択される少なくとも1種と、 Q はハロゲン元素の F 、 Cl 、 Br 、 I から選択される少なくとも1種と、 Re' は Mn 、 Fe 、 Cr 、 Sn から選択される少なくとも1種とを有する。) (白色)

(2) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$ (但し、 Re は Sr 、 Ca 、 Ba 、 Mg から選択される少なくとも1種、 Q はハロゲン元素の F 、 Cl 、 Br 、 I から選択される少なくとも1種とを有する。) (青色)、

(3) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$ (青色)、

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(4) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$, Mn (緑色)、

(5) $(\text{SrEu})\text{O}\cdot\text{Al}_2\text{O}_3$ (緑色)、

(6) $3\cdot5\text{MgO}\cdot0\cdot5\text{MgF}_2\cdot\text{GeO}_2:\text{Mn}$ (赤色)、

(7) $\text{Y}_2\text{O}_2\text{S}:\text{Eu}$ (赤色)、

(8) $\text{Mg}_6\text{As}_2\text{O}_{11}:\text{Mn}$ (赤色)、

(9) $\text{Gd}_2\text{O}_2\text{S}:\text{Eu}$ (赤色) 及び

(10) $\text{La}_2\text{O}_2\text{S}:\text{Eu}$ (赤色) 等が挙げられる。

また、これらの蛍光体は、単独で用いても良いし、混合して用いてもよい。

【0015】

以下、紫外領域の光を発生する発光素子チップと複数の蛍光体を組み合わせる場合につい

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てより具体的に説明する。

本実施の形態では、1つの SiO_2 層70に異種の蛍光体（例えば、赤、緑、青の蛍光体）を混合して分散させるようにしてもよく、このようにすると、異なる蛍光体からの光の混色による白色光が得られる。この場合、各蛍光物質から発光される光をより良く混色しかつ色ムラを減少させるために、各蛍光体の平均粒径及び形状は類似していることが好ましく、また、各蛍光体は SiO_2 層70に均一に分散されていることが好ましい。

【0016】

また、本発明では、各蛍光物質をそれぞれの別々の SiO_2 層に分散させ、それらを積層することにより多重構造の SiO_2 層70を形成するようにしてもよい。このように SiO_2 層を多重薄膜として構成する場合、それぞれの蛍光物質の紫外光透過率を考慮して、素子上に赤色蛍光物質層、緑色蛍光物質層、及び青色蛍光物質層という順に積層すると、全ての層に均等に紫外光を吸収させることができ好ましい。更に、多重薄膜層である SiO_2 層70において下層から上層にかけて各層中の蛍光物質の粒径が小さくなるように、各蛍光物質の平均粒径の大小関係を青色蛍光物質>緑色蛍光物質>赤色蛍光物質とすると最上層まで良好に紫外光を透過させることができると共に多重薄膜層である SiO_2 層70に紫外光をもれなく吸収させることができる。

【0017】

そのほか、ストライプ状、格子状、またはトライアングル状となるように各蛍光体が含まれる各色変換部を配置するようにして SiO_2 層70を形成するようにしてもよい。また、各色変換部の間に間隔を設けて配置させるようにしてもよく、これにより混色性を良好にできる。またさらに、素子の周囲を全て覆うように SiO_2 層を形成すると、紫外光の漏れを防止できるので好ましい。

【0018】

また、蛍光体71を含む SiO_2 層70は、例えば、シラノール（ $\text{Si}(\text{OEt})_3\text{OH}$ ）とエタノールとを所定の割合で混合してなるシリカゾル中に蛍光体（粉末）71を分散させて、その蛍光体が分散されたシリカゾルを透光性基板11の他方の主面にスピンナーによりコートした後、縮合重合することにより形成することができる。

このようにして形成された SiO_2 層70は、従来の樹脂とは異なり無機物であるため、紫外線による劣化が樹脂に比べて極めて小さく、紫外光を発光する発光ダイオード（紫外域発光ダイオード）と組み合わせて用いることができる。

これに対して、従来例のように樹脂の中に蛍光体を分散させた構成では、ほとんどの樹脂が紫外線により劣化するために長時間の使用に耐え得る素子を構成することができないので、紫外域発光ダイオードを用いた白色発光ダイオードの実用化は困難であった。

【0019】

ここで、本実施の形態1では、 SiO_2 膜70に含まれる蛍光体71の含有量は、 SiO_2 膜70を介して出力される光が実質的に蛍光体71によって波長変換された白色光のみになるように、すなわち、発光素子チップにより発光された紫外光のほとんどが蛍光体71に吸収されて該蛍光体71を励起するように比較的大きく設定することが好ましい。このようにすると発光効率（発光素子に入力された電力に対する出力される光の比）を高くすることができる。

【0020】

また、 SiO_2 膜70に含有させる蛍光体の量は、所望の色調に対応させて種々の値に設定されるものであり、本発明は蛍光体の含有量により限定されるものではないが、本発明者らの検討によると、 SiO_2 膜70に含まれる蛍光体71の含有量が多くなると、透光性基板11に対する SiO_2 膜70の付着強度が強くなることが確認されている。かかる付着強度の面を考慮すると、 SiO_2 膜70における蛍光体の含有量は、30wt%～80wt%に設定することが好ましく、基板11に対する SiO_2 膜70のより高い付着強度を得るためには、40wt%～80wt%に設定することがさらに好ましい。

【0021】

また、本実施の形態1の窒化物半導体発光素子の発光素子1, 2, 3において、各半導体

層及び電極はそれぞれ以下のように形成される。

(1) n型窒化ガリウム系化合物半導体層12 (n層12) は、例えば、サファイアからなる透光性基板11上のほぼ全面に成長されたn型窒化ガリウム系化合物半導体層が分離溝41により分離されて、平面形状が長方形になるように形成される。

【0022】

(2) 活性層10は、n層12とほぼ同一の長さでn層12より狭い幅を有する長方形であって、その1つの長辺がn層12の1つの長辺に実質的に一致するようにn層12上に形成される。このように形成することにより、n層12上に活性層10に沿ってn側オーミック電極を形成するための領域が確保される。

ここで、本実施の形態1では、活性層10の幅は、n側オーミック電極から離れた側に位置する長辺とn側オーミック電極との距離L1、L2、L3が220 μm になるように設定した。

このように、距離L1、L2、L3を220 μm に設定した理由は、n側オーミック電極から220 μm 以上離れた位置にある活性層に注入される電流は減少するからである。

ここで、本実施の形態1において、活性層10はInの含有量を変化させることにより発光波長を変えることができる $\text{In}_x\text{Ga}_{1-x}\text{N}$ 層により構成し、このInの量を紫外光の発光が可能な値に設定する。

【0023】

(3) n側オーミック電極14 (14a) は、活性層10とほぼ同一の長さを有し、n層12上に、活性層10に沿ってかつ活性層10と近接して形成される。

また、n側オーミック電極14 (14a) は、例えば、n層12とのオーミック接触を良好にできるWとAlを含む層により構成する。一例を挙げれば、W層 (200 Å)、Al層 (1000 Å)、W層 (500 Å)、Pt層 (3000 Å)、Ni層 (60 Å) を順次積層することによりn側オーミック電極14 (14a) を形成する。

【0024】

(4) p型窒化ガリウム系半導体層13は、活性層10と同一平面形状を有し活性層10上に重ねて形成される。

実際には、活性層10及びp型窒化ガリウム系半導体層13は、n層12上に活性層10及びp層13を重ねて形成した後、n側オーミック電極14を形成するn層12表面を露出させるために一括してエッチングすることにより形成する。

【0025】

(5) p側オーミック電極15は、p型窒化ガリウム系半導体層13上のほぼ全面に形成され、p層13と良好なオーミック接触を得るために、例えば、Ni層とPt層とを積層することにより構成する。

【0026】

(6) そして、pパッド電極16 (16a) は、例えば、膜厚3000 ÅのPtからなり、p側オーミック電極15上において、n側オーミック電極14とは離れた側に位置するp側オーミック電極15の長辺に沿って形成される。

【0027】

さらに、本実施の形態1の集積型窒化物半導体発光素子において、上述のように構成された発光素子1、2、3は、絶縁保護膜17により素子間が分離され、接続電極21により以下のように接続される。

絶縁保護膜17は、各発光素子のpパッド電極16 (16a) 上及びn側オーミック電極14 (14a) 上を除いて素子全体を覆うように形成される。

接続電極21は、発光素子1のn側オーミック電極14a上、分離溝41に形成された絶縁膜17上及び発光素子2のp側オーミック電極16a上に連続して間の形成され、これにより、発光素子1のn側オーミック電極14aと発光素子2のp側オーミック電極16aが接続される。

また、接続電極21は、発光素子2と発光素子3との間においても同様に形成され、これにより、発光素子2のn側オーミック電極14aと発光素子3のp側オーミック電極16

aが接続される。接続電極21は、Pt又はAu等、種々の金属で構成することができる。

【0028】

尚、本実施の形態1ではさらに、発光素子1のpパッド電極16上に接続電極21と同様の材料からなる外部接続用電極26が形成され、発光素子3のnパッド電極14上に接続電極21と同様の材料からなる外部接続用電極24が形成される。

【0029】

以上のように構成された実施の形態1の窒化物半導体発光素子は、透光性基板11の他方の面に、無機物でありかつ紫外線による劣化がほとんどないSiO₂層70に蛍光体を含

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有させて形成しているため、発光素子チップとして紫外域発光ダイオードを用いることが可能となる。

これにより、発光素子チップの光と蛍光体の光との混色によらず、蛍光体からの光のみを利用して発光ダイオードを構成することができ、色変化の極めて少ない発光ダイオードを実現できる。

また、本実施の形態1の窒化物半導体発光素子は、蛍光体を含む無機物であるSiO₂層70を用いて構成しているため、蛍光体を含む層を従来の樹脂層に比較して耐環境特性を良好にできるので、素子の寿命を長くできる。

【0030】

応用例、

本実施の形態1の窒化物半導体発光素子と同様の構成において、紫外光を発光する発光素子を35個に増やしてそれらの素子を直列に接続し、蛍光体71として、例えば、Ca₁₀(PO₄)₆FCI:Eu, Mnを用いることにより、比較的広い発光面積を有する照明用の窒化物半導体発光素子を構成できる。

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このように構成された照明用の窒化物半導体発光素子は、100Vの一般家庭電源に直接接続して使用したときに、各素子の電流値を、発光効率及び寿命の点でほぼ最適な20mA程度に設定でき、信号機や家庭用の照明等に利用できる。

【0031】

実施の形態2、

次に、本発明に係る実施の形態2の窒化物半導体発光素子について、図4を参照しながら説明する。

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本実施の形態2の集積型窒化物半導体発光素子は、以下の点で実施の形態1の窒化物半導体発光素子と異なる。

相違点1、

実施の形態1の集積型窒化物半導体発光素子において、接続電極21及び外部接続電極24、26を形成することなく、素子全体を覆うように絶縁保護膜30を形成し、発光素子1、2、3のpパッド電極上にそれぞれ絶縁保護膜30を貫通するスルーホール61を形成し、発光素子1、2、3の各n側オーミック電極上にそれぞれ絶縁保護膜30を貫通するスルーホール62を形成する。

【0032】

相違点2、

絶縁保護膜30に形成されたスルーホール61を介して、発光素子1、2、3のpパッド電極間を互いに接続電極51で接続する。

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相違点3、

絶縁保護膜30に形成されたスルーホール62を介して、発光素子1、2、3のn側オーミック電極間を互いに接続電極52で接続する。

以上の相違点1、2、3以外は、実施の形態1の集積型窒化物半導体発光素子と同様に構成する。

すなわち、実施の形態2の集積型窒化物半導体発光素子は、実施の形態1の素子において発光素子1、2、3を並列に接続したものである。

以上のように構成された実施の形態2の窒化物半導体発光素子は、実施の形態1と同様の

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作用効果を有する。

【0033】

以上の実施の形態1, 2では、発光領域が3つの場合について説明したが、本発明はこれに限られるものではなく、4以上の発光領域で構成したものであってもよい。

例えば、図5に示すように、多数(m個)の発光領域1~mを各領域の短辺方向に並置して形成することにより、輝度が高くかつ発光色のばらつきが少なくしかも広い面積の面発光が可能な発光ダイオードを実現できる。

【0034】

以上の実施の形態1, 2では、発光領域が3つの場合について説明したが、本発明はこれに限られるものではなく、1つの発光領域のみを有する例えば、 $300\mu\text{m} \times 300\mu\text{m}$ の一般的に良く用いられる大きさの発光ダイオードに適用することもできることはいうまでもない。

この場合、個々の素子への分離は、例えば、図6に示すように、分割すべき素子と素子との間の SiO_2 層70を除去して、溝72を形成し、その溝72において、スクライビング又はダイシングにより分割するようにすればよい。

【0035】

以上の実施の形態1及び2では、紫外域発光素子チップを用いた本発明に係るより好ましい実施の形態について説明したが、本発明はこれに限られるものではなく、青色の発光素子チップと該チップの青色光により励起され黄色の光を発生する、以下に説明するイットリウム・アルミニウム・ガーネット(YAG)系の蛍光体とを組み合わせる白色発光ダイオードを構成してもよい。

【0036】

本発明に用いられるYAG系蛍光体は、窒化物系半導体を発光層とする半導体発光素子から発光された光を励起させて発光できるセリウムで付活されたイットリウム・アルミニウム酸化物系蛍光物質をベースとしたものである。

具体的なイットリウム・アルミニウム酸化物系蛍光物質としては、 $\text{YAlO}_3:\text{Ce}$ 、 $\text{Y}_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (YAG:Ce)や $\text{Y}_4\text{Al}_2\text{O}_9:\text{Ce}$ 、更にはこれらの混合物などが挙げられる。イットリウム・アルミニウム酸化物系蛍光物質にBa、Sr、Mg、Ca、Znの少なくとも一種が含有されていてもよい。また、Siを含有させることによって、結晶成長の反応を抑制し蛍光物質の粒子を描えることができる。

【0037】

本明細書において、Ceで付活されたイットリウム・アルミニウム酸化物系蛍光物質は特に広義に解釈するものとし、イットリウムの一部あるいは全体を、Lu、Sc、La、Gd及びSmからなる群から選ばれる少なくとも1つの元素に置換したもの、あるいは、アルミニウムの一部あるいは全体をBa、Tl、Ga、Inの何れが又は両方で置換したものなどの蛍光作用を有する蛍光体を含む広い意味に使用する。

【0038】

すなわち、本発明では、一般式 $(\text{Y}_z\text{Gd}_{1-z})_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (但し、 $0 < z \leq 1$)で示されるフォトルミネセンス蛍光体や一般式 $(\text{Re}_{1-a}\text{Sm}_a)_3\text{Re}'_5\text{O}_{12}:\text{Ce}$ (但し、 $0 \leq a < 1$ 、 $0 \leq b \leq 1$ 、Reは、Y、Gd、La、Scから選択される少なくとも一種、Re'は、Al、Ga、Inから選択される少なくとも一種である。)で示されるフォトルミネセンス蛍光体を用いることができる。

【0039】

これらの蛍光物質は、ガーネット構造のため、熱、光及び水分に強く、励起スペクトルのピークを450nm付近に設定することができる。また、発光ピークも、580nm付近にあり700nmまですそを引くブロードな発光スペクトルを持つ。さらに、所望に応じてCeに加えTb、Cu、Ag、Au、Fe、Cr、Nd、Dy、Co、Ni、Ti、Eu、およびPr等を含有させてもよい。

【0040】

またフォトルミネセンス蛍光体は、結晶中にGd(ガドリニウム)を含有することにより

、460nm以上の長波長域の励起発光効率を高くすることができる。Gdの含有量の増加により、発光ピーク波長が長波長に移動し全体の発光波長も長波長側にシフトする。すなわち、赤みの強い発光色が必要な場合、Gdの置換量を多くすることで達成できる。一方、Gdが増加すると共に、青色光によるフォトルミネセンスの発光輝度は低下する傾向にある。

【0041】

しかも、ガーネット構造を持ったイットリウム・アルミニウム・ガーネット系蛍光体の組成のうち、Alの一部をGaで置換することで発光波長が短波長側にシフトする。また、組成のYの一部をGdで置換することで、発光波長が長波長側にシフトする。

【0042】

Yの一部をGdで置換する場合、Gdへの置換を1割未満にし、且つCeの含有（置換）を0.03から1.0に設定することが好ましい。Gdへの置換が2割未満では緑色成分が大きく赤色成分が少なくなるが、Ceの含有量を増やすことで赤色成分を補え、輝度を低下させることなく所望の色調を得ることができる。このような組成にすると温度特性が良好となり発光ダイオードの信頼性を向上させることができる。また、赤色成分を多く有するように調整されたフォトルミネセンス蛍光体を使用すると、ピンク等の中間色を発光することが可能な発光装置を形成することができる。

【0043】

このようなフォトルミネセンス蛍光体は、Y、Gd、Al、及びCeの原料として酸化物、又は高温で容易に酸化物になる化合物を使用し、それらを化学量論比で十分に混合して原料を得る。又は、Y、Gd、Ceの希土類元素を化学量論比で酸に溶解した溶解液を蓆酸で共沈したものを焼成して得られる共沈酸化物と、酸化アルミニウムとを混合して混合原料を得る。これにフラックスとしてフッ化バリウムやフッ化アンモニウム等のフッ化物を適量混合して坩堝に詰め、空气中1350～1450℃の温度範囲で2～5時間焼成して焼成品を得、つぎに焼成品を水中でボールミルして、洗浄、分離、乾燥、最後に篩を通すことで得ることができる。

【0044】

本願発明の発光ダイオードにおいて、このようなフォトルミネセンス蛍光体は、2種類以上のセリウムで付活されたイットリウム・アルミニウム・ガーネット（ざくろ石型）蛍光体や他の蛍光体を混合してもよい。

【0045】

他にも青色、青緑色や緑色を吸収して赤色が発光可能な蛍光体としては、Eu及び／又はCrで付活されたサファイア（酸化アルミニウム）蛍光体やEu及び／又はCrで付活された窒素含有Ca-Al₂O₃-SiO₂蛍光体（オキシナイトライド蛍光硝子）等が挙げられる。これらの蛍光体を利用して発光素子からの光と蛍光体からの光の混色により白色光を得ることもできる。

【0046】

また、発光出力を向上させるためには、本発明で用いられる蛍光物質の平均粒径は10μm～50μmが好ましく、より好ましくは15μm～30μmである。ここで平均粒径とは、空気透過法を基本原理としてサブミクロンサイザーにて測定された平均粒子径を示す。このような粒径を有する蛍光物質は光の吸収率及び変換効率が高く且つ励起波長の幅が広い。このように、光学的に優れた特徴を有する大粒径蛍光物質を含有させることにより、発光素子の主波長周辺の光をも良好に変換し発光することが可能となり、発光装置の量産性が向上される。

【0047】

また、この平均粒径値を有する蛍光物質が頻度高く含有されていることが好ましく、頻度値は20%～50%が好ましい。このように粒径のパラツキが小さい蛍光物質を用いることにより色ムラが抑制され良好な色調を有する発光装置が得られる。

【0048】

同様に、本発明に用いられる他の具体的蛍光体として、Eu及び／又はCrで付活された

窒素含有 $\text{CaO-Al}_2\text{O}_3\text{-SiO}_2$ 蛍光体が挙げられる。この Eu 及び／又は Cr で付活された窒素含有 $\text{CaO-Al}_2\text{O}_3\text{-SiO}_2$ 蛍光体は、酸化アルミニウム、酸化イットリウム、窒化珪素及び酸化カルシウムなどの原料に希土類原料を所定比に混合した粉末を窒素雰囲気下において 1300°C から 1900°C （より好ましくは 1500°C から 1750°C ）において熔融し成形させる。成形品をボールミルして洗浄、分離、乾燥、最後に篩を通して蛍光体を形成させることができる。これにより 450 nm にピークをもった励起スペクトルと約 650 nm にピークがある青色光により赤色発光が発光可能な Eu 及び／又は Cr で付活された Ca-Al-Si-O-N 系オキシナイトライド蛍光硝子とすることができる。

【0049】

なお、Eu 及び／又は Cr で付活された Ca-Al-Si-O-N 系オキシナイトライド蛍光硝子の窒素含有量を増減することによって発光スペクトルのピークを 575 nm から 690 nm に連続的にシフトすることができる。同様に、励起スペクトルも連続的にシフトさせることができる。そのため、Mg、Zn などの不純物がドーピングされた GaN や InGaN を発光層に含む窒化ガリウム系化合物半導体からの光と、約 580 nm の蛍光体の光の合成光により白色系を発光させることができる。特に、約 490 nm の光が高輝度に発光可能な InGaN を発光層に含む窒化ガリウム系化合物半導体からなる発光素子との組合せに理想的に発光を得ることもできる。

【0050】

また、上述の Ce で付活された YAG 系蛍光体と Eu 及び／又は Cr で付活された窒素含有 Ca-Al-Si-O-N 系オキシナイトライド蛍光硝子とを組み合わせることにより青色系が発光可能な発光素子を利用して RGB（赤色、緑色、青色）成分を高輝度を含む極めて演色性の高い発光ダイオードを形成させることもできる。このため、所望の顔料を添加するだけで任意の中間色も極めて簡単に形成させることができる。本発明においては何れの蛍光体も無機蛍光体であり、有機の光散乱剤や SiO_2 などを利用して高コントラストを有しかつ量産性に優れた発光ダイオードを構成することができる。

【0051】

以上のように構成された YAG 系蛍光体を用いた窒化物半導体発光素子は、蛍光体を含む無機物である SiO_2 層 70 を用いて構成しているので、蛍光体を含む層を従来の樹脂層に比較して耐環境特性を良好にでき、素子の寿命を長くできる。

【0052】

【実施例】

以下、本発明に係る実施例を示す。尚、本発明はこれに限定されるものではない。

〔実施例 1〕

（透光性基板 11）

サファイア（C 面）よりなる透光性基板 11 を MOVPE の反応容器内にセットし、水素を流しながら、基板の温度を 1050°C まで上昇させ、基板のクリーニングを行う。この透光性基板 11 としては他に R 面、A 面を主面とするサファイア基板、スピネル（ MgAl_2O_4 ）のような絶縁性基板、GaN 基板などでもよい。

【0053】

（n 型窒化ガリウム系化合物半導体層 12）

基板をクリーニング後、n 型窒化ガリウム系化合物半導体層 12 を次の構成で成長させる。

基板の温度を 510°C まで下げ、透光性基板 11 上に GaN よりなるバッファ層を $100\text{ \AA}$ 成長させる。

次にバッファ層成長後、温度を 1050°C まで上昇させ、アンドープ GaN 層 121 を $1.5\text{ }\mu\text{m}$ の膜厚で成長させる。

続いて 1050°C で、Si を $4.5 \times 10^{18} / \text{cm}^3$ ドープした GaN 層 122 を $2.2\text{ }\mu\text{m}$ の膜厚で成長させる。

【0054】

続いて1050℃で、アンドープGaN層123を3000Åの膜厚で、さらにSiを $4.5 \times 10^{18} / \text{cm}^3$ ドープしたGaN層124を300Å、さらにアンドープGaN層125を50Åの膜厚で成長させる。

【0055】

続いて同様の温度で、アンドープGaNよりなる第1の層を40Å、温度を800℃にして、続いてアンドープIn_{0.13}Ga_{0.87}Nよりなる第2の層を20Åの膜厚で成長させ、これらの操作を繰り返し、第1+第2+の順で交互に10層ずつ積層させ、最後に第1の層を積層させた、n型多層膜層126を成長させる。

【0056】

(活性層13)

次にn型窒化ガリウム系化合物半導体層12を成長後、アンドープGaNよりなる障壁層を200Åの膜厚で成長させ、続いて温度を800℃にして、Siを $5 \times 10^{17} / \text{cm}^3$ ドープしたIn_{0.03}Ga_{0.97}Nよりなる井戸層を30Åの膜厚で成長させる。そして障壁+井戸+障壁+井戸・・・の順で障壁層を6層と、井戸層5層を交互に積層して、総膜厚1350Åの多重量子井戸よりなる活性層13を積層させる。

以上のようにして、370nmの紫外領域の光を発光する活性層を形成する。

【0057】

(p型窒化ガリウム系化合物半導体層14)

活性層13成長後、p型窒化ガリウム系化合物半導体14を次の構成で成長させる。

次に1050℃で、Mgを $5 \times 10^{19} / \text{cm}^3$ ドープしたp型Al_{0.1}Ga_{0.9}Nよりなる第3の層を25Åの膜厚で成長させ、続いてアンドープGaNよりなる第4の層を25Åの膜厚で成長させ、これらの操作を繰り返し、第3+第4の順で交互に4層ずつ積層した超格子よりなるp型多層膜層を200Åの膜厚で成長させる。

続いて1050℃で、Mgを $1 \times 10^{20} / \text{cm}^3$ ドープしたp型GaNよりなる層を2700Åの膜厚で成長させる。

反応終了後、温度を室温まで下げ、窒素雰囲気中で700℃でアニーリングを行い、p型層をさらに低抵抗化する。

【0058】

以上のようにして窒化ガリウム系化合物半導体を成長させたウェハーを反応容器から取り出し、分離溝を形成する部分を除きウェハ全体にSiO₂マスクを形成し、RIEによって、サファイア基板に到達するまでエッチングを行うことにより分離溝を形成する。また、上記のような窒化ガリウム系化合物半導体は、所望に応じてボロンやリンを含有させることも可能である。

さらに分離溝の形成に用いたSiO₂マスクを剥離し、n型窒化ガリウム系化合物半導体層12を露出するために、露出させる部分を除くp型窒化ガリウム系化合物半導体層14の上にSiO₂マスクを形成し、RIEによって、エッチングを行い、n型窒化ガリウム系化合物半導体層12(SiドープGaN層122)の表面を露出させる。

【0059】

次にp型窒化ガリウム系化合物半導体層14のほぼ全面を開口させ、他の部分を覆うようにレジスト塗布し、開口させたp型窒化ガリウム系化合物半導体層上にNiを100Å、Ptを500Å積層後、アニールしてp側オーミック電極15を形成する。さらにp側オーミック電極の一部にPtを3000Å、Niを60Åからなるp側パッド電極16a(16)を形成する。

次にレジストを除去し、今度はn型窒化ガリウム系化合物半導体層上にWを200Å、Alを1000Å、Wを500Å、Ptを3000Å、Niを60Åの順で積層したn側オーミック電極14を形成する。

【0060】

次に全面にSiO₂よりなる絶縁保護膜17を1.5μmの膜厚で形成し、p側パッド電極とn側オーミック電極の一部をRIEにより露出させる。

さらに表面に接続電極を形成する部分を開口させるようにマスク形成して分離溝を挟むp

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側パッド電極とn側オーミック電極とを電氣的に接続する接続電極として、Tiを400 Å、Ptを6000 Å、Auを1000 Å、Niを60 Åの膜厚で形成する。

最後にSiO₂からなる絶縁保護膜30を1.5 μmの膜厚で形成し、外部と電氣的に接続できるように接続電極24、26上の絶縁保護膜30をRIEでエッチングすることにより除去する。

【0061】

(蛍光体71を含むSiO₂層70の形成)

次に、蛍光体{Ca₁₀(PO₄)₆FCI:Eu, Mn}、シラノール(Si(OEt)₃OH)及びエタノールを混合したスラリーを作製する。

ここで、実施例1において、スラリーは、蛍光体：シラノール：エタノールが重量比で4

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：1：2となるように混合した。
すなわち、本実施例1において、スラリーに対する蛍光体の含有量は、57%に設定した。

次に、そのスラリーをノズルからサファイア基板の裏面に滴下して基板を高速で回転させることにより、基板の裏面全体に均一な膜厚を有する、蛍光体、シラノール、エタノールからなるスラリー膜を形成する。

そして、スラリー膜が形成された基板を300℃のオープン内で3時間加熱することにより、スラリー膜内のシラノールを縮合重合して蛍光体が分散含有されたSiO₂膜とする。

このようにして、蛍光体71を含むSiO₂層70が形成される。

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【0062】

このようにして作製された複数の素子領域を有するサファイア基板(ウエハ)を、スクライピング及びダイシングを用いて個々の素子ごとに分割して、350×400 μmの発光素子チップを作製する。

次に、その発光素子チップ80を図7に示すように、パッケージ81に発光素子チップ80の正負の電極それぞれパッケージ81の正負の電極に対向させてフリップチップ実装を行う。

そして、発光素子チップを覆うように透光性のエポキシ樹脂83を形成して、発光素子チップを保護する。

以上のようにして紫外光を発光する発光素子チップを用いた白色発光ダイオードを形成することができる。

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【0063】

[実施例2]

実施例1において、スラリーに対する蛍光体の含有量を30%に変更した以外は実施例1と同様に構成した。

以上の実施例2の発光ダイオードは、製造歩留まりが実施例1に比較して若干低くなったものの、実施例1と同等の性能が得られた。

【0064】

[実施例3]

スラリーに対する蛍光体の含有量を40%に変更した以外は実施例1と同様に構成した。

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以上の実施例3の発光ダイオードは、実施例1と同等の性能が得られ、かつ実施例2に比較して製造歩留まりが向上した。

【0065】

[実施例4]

スラリーに対する蛍光体の含有量を70%に変更した以外は実施例1と同様に構成した。

以上の実施例4の発光ダイオードは、実施例1と同等の性能が得られ、かつ実施例1に比較して製造歩留まりが向上した。

【0066】

[実施例5]

実施例1において、以下の点が異なる以外は実施例1と同様に構成される。

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(1) 実施例 1 において、紫外領域発光素子チップに代えて、青色発光が可能な発光素子チップを用いる。

(2) 蛍光体 71 として、 $(Y_{0.8}Gd_{0.2})_3Al_5O_{12}:Ce$ を用いる。

以下、本実施例 5 の発光ダイオードについて詳細に説明する。

本実施例 5 では、発光素子チップとして、InGa_{0.5}N からなる発光層を有し主発光ピークが 470 nm の LED チップを用いる。この LED チップは、MOCVD 法を利用して形成する。具体的には、反応室内に洗浄したサファイア基板を配置して、反応ガスとして、TMG (トリメチル) ガス、TMI (トリメチルインジウム) ガス、TMA (トリメチルアルミニウム) ガス、アンモニアガス及びキャリアガスとして水素ガス、さらには不純物ガスとしてシランガス及びシクロペンタジエナマグネシウムを利用して成膜する。

【0067】

発光素子チップの層構成として、サファイア基板上に低温バッファ層である AlGa_{0.5}N、結晶性を向上させるノンドープ GaN (厚さ約 1500 Å)、電極が形成され n 型コンタクト層として働く Si ドープの GaN (厚さ約 2165 Å)、結晶性を向上させるノンドープの GaN (厚さ約 300 Å)、n 型クラッド層としてノンドープの GaN (厚さ約 50 Å)、Si をドープした GaN (厚さ約 300 Å) の超格子からなる多層膜、その上に形成される発光層の結晶性を向上させる、ノンドープの GaN (厚さ約 40 Å) と、ノンドープの InGa_{0.5}N (厚さ約 20 Å) の超格子からなる多層膜、多重量子井戸構造からなる発光層として、ノンドープの GaN (厚さ約 250 Å) と、InGa_{0.5}N (厚さ約 30 Å) の多層膜、p 型コンタクト層として働く Mg がドープされた InGa_{0.5}N (厚さ約 25 Å) と Mg がドープされた GaAlN (厚さ約 40 Å) の超格子からなる多層膜及び p 型コンタクト層である Mg がドープされた GaN (厚さ約 1200 Å) を成膜する。

【0068】

こうして成膜した窒化物半導体が成膜された半導体ウエハを部分的にエッチングして、p 型及び n 型コンタクト層を露出させる。スパッタリング法を利用して、各コンタクト層上に n 型及び p 型の電極を形成させた後に、個々の発光素子に分割して青色が発光可能な発光素子チップを作製する。

そして、このようにして作製した発光素子チップと、 $(Y_{0.8}Gd_{0.2})_3Al_5O_{12}:Ce$ 蛍光体とを用いて、実施例 1 と同様にして発光ダイオードを作製する。

【0069】

以上のようにして、作製された発光ダイオードは、混色により白色光が得られ、従来例とは異なり蛍光体を含む層を無機物で構成しているため、従来例に比較して耐環境特性が優れている。

【0070】

【発明の効果】

以上詳細に説明したように、本発明によれば、紫外光を発光する発光ダイオードを用い、蛍光体が発光する光のみにより発光色が白色の発光ダイオードを構成できるので、発光色のバラツキの少ない白色発光ダイオードを提供できる。

また、本発明によれば青色光を発光する発光ダイオードを用い、蛍光体との混色による発光色が白色の発光ダイオードを構成すると、蛍光体を含有する層の劣化を極めて小さくできるので、従来例に比較して寿命の長い白色発光ダイオードを提供できる。

【図面の簡単な説明】

【図 1】 本発明に係る実施の形態 1 の窒化物半導体発光素子の平面図である。

【図 2】 図 1 の A-A' 線についての部分断面図 (発光素子 1, 2 の部分) である。

【図 3】 図 1 の A-A' 線についての部分断面図 (発光素子 3 の部分) である。

【図 4】 本発明に係る実施の形態 2 の窒化物半導体発光素子の平面図である。

【図 5】 本発明に係る変形例の窒化物半導体発光素子の平面図である。

【図 6】 実施の形態の窒化物半導体発光素子において、スクライブ又はダイシングする部分の SiO₂ 層を除去した時の様子を示す図である。

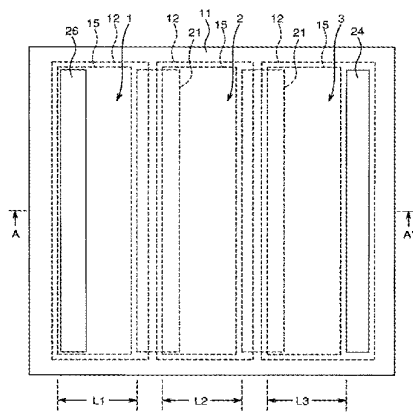
【図 7】 本発明に係る実施例の窒化物半導体発光素子の断面図である。

【符号の説明】

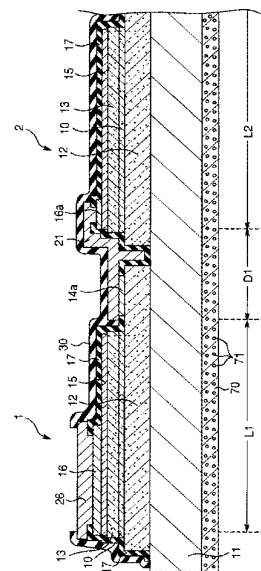
- 1, 2, 3 … 発光素子、
 10 … 活性層、
 11 … サファイア基板、
 12 … n型窒化ガリウム系化合物半導体層、
 13 … p型窒化ガリウム系半導体層、
 14, 14a … n側オーミック電極、
 15 … p側オーミック電極、
 16, 16a … pパッド電極、
 17 … 絶縁保護膜、
 21, 51, 52 … 接続電極、
 24, 26 … 外部接続電極、
 30 … 絶縁保護膜、
 61, 62 … スルーホール、
 41 … 分離溝、
 70 … SiO₂層、
 71 … 蛍光体。

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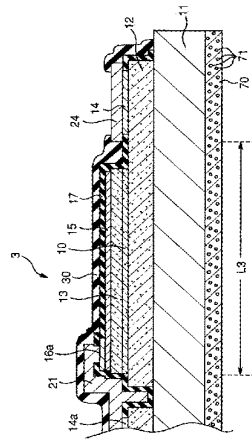
【図1】



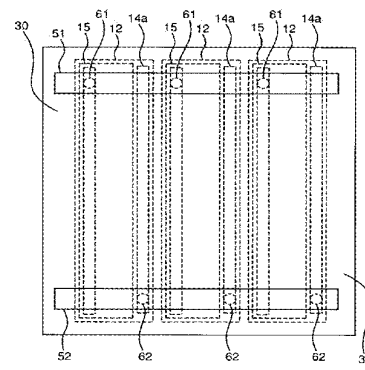
【図2】



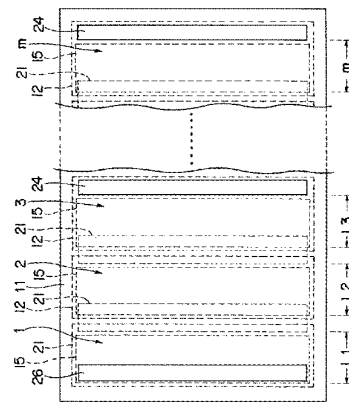
【図 3】



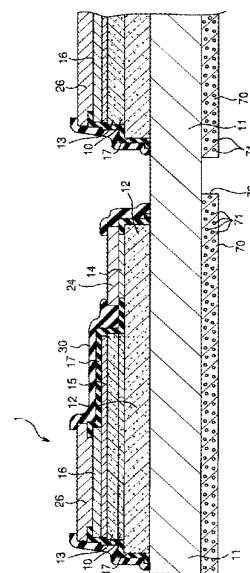
【図 4】



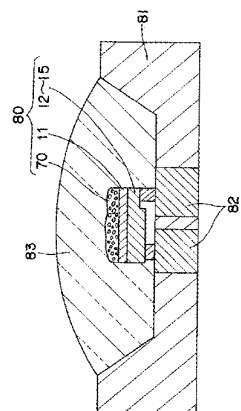
【図 5】



【図 6】



【図 7】



フロントページの続き

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(58)調査した分野(Int.Cl., DB名)

H01L 33/00
H01S 5/00-5/50

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JP,4151284,B

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CLAIMS DETAILED DESCRIPTION

DRAWINGS

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a nitride semiconductor element.

[0002]

[Description of the Prior Art]

In recent years, the light emitting diode (white light emitting diode) in which luminescence of white light which combined the light emitting element chip constituted using the gallium nitride system; compound semiconductor and the fluorescent substance is possible is developed and used increasingly. This light emitting diode carries out wavelength conversion of a part of blue light outputted from a light emitting element chip with a fluorescent substance, and makes a white light emit light with mixed colors with a blue light from that light by which wavelength conversion was carried out and light emitting element chip.

It was produced by conventionally carrying out the mold of the package etc. in which a light emitting element chip was mounted by resin containing a fluorescent substance, for example.

[0003]

[Problem to be solved by the invention]

However, since it constituted using resin containing a fluorescent substance and resin would deteriorate if light with shorter wavelength is used, the conventional white light emitting diode was difficult to constitute the light emitting diode which uses the light emitting device of the light whose wavelength is shorter than blue, and has sufficient reliability.

[0004]

Then, an object of the present invention is also it to provide a possible light emitting diode to constitute light with short wavelength from blue using the light emitting element chip and fluorescent substance which emit light.

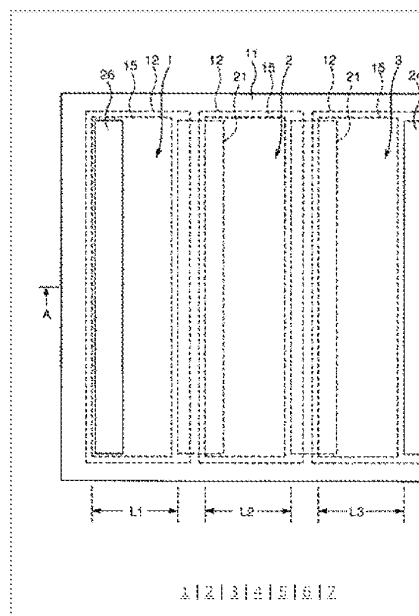
[0005]

[Means for solving problem]

In order to achieve the above object, the luminescent device concerning the present invention, The nitride semiconductor light emitting element which comes to form a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer on one main surface of a translucent substrate, In the luminescent device with which the nitride semiconductor light emitting element has a package by which flip chip mounting is carried out, After carrying out the coat of the silica sol by which the fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in the light of long wave length from the wavelength of the absorbed light was distributed to the main surface of another side of a translucent substrate, By carrying out a condensation polymerization, the translucent substrate in which the SiO₂ layer was formed on the main surface of another side of the above-mentioned translucent substrate, and the SiO₂ layer was formed is divided for each element of every, the above-mentioned nitride semiconductor light emitting element is produced, and light is outputted via the SiO₂ layer.

[0006]

In the luminescent device concerning the present invention, the above-mentioned luminous layer is constituted so that light may be emitted in the light of an ultraviolet region, and it is the above-mentioned fluorescent substance,



(1) $\text{Re}_3(\text{PO}_4)_3\text{Q}:\text{Eu}$, Re^1 (however, Re with at least 1 type chosen from Mg, Ca, Ba, Sr, and Zn)
At least 1 type as which Q is chosen from F of a halogen, Cl, Br, and I, and Re^1 have at least 1 type chosen from Mn, Fe, Cr, and Sn.

(2) $\text{Re}_3(\text{PO}_4)_3\text{Q}:\text{Eu}$ (however, at least 1 type as which Re is chosen from Sr, Ca, Ba, and Mg, and Q have at least 1 type chosen from F of a halogen, Cl, Br, and I.),

(3) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$,

(4) $\text{BaMg}_2\text{Al}_{16}\text{O}_{27}:\text{Eu}$, Mn,

(5) $(\text{SrEu})\text{O}:\text{Al}_2\text{O}_3$,

(6) 3.5MgO and $0.5\text{MgF}_2 \cdot \text{GeO}_2:\text{Mn}$,

(7) $\text{Y}_2\text{O}_3\text{S}:\text{Eu}$,

(8) $\text{Mg}_6\text{As}_2\text{O}_{11}:\text{Mn}$ and (9) $\text{Gd}_2\text{O}_3\text{S}:\text{Eu}$ -- and

(10) It can be considered as at least one fluorescent substance chosen from the group which consists of $\text{La}_2\text{O}_3\text{S}:\text{Eu}$.

If it does in this way, the light emitting device by which only luminescence of a fluorescent substance is observed can be constituted.

[0007]

In the luminescent device concerning the present invention, the above-mentioned luminous layer may be constituted so that light may be emitted in a blue light, and it may constitute as the above-mentioned fluorescent substance using the yttrium aluminum garnet (YAG) system fluorescent substance activated by Ce.

[0008]

It may be made to form a plurality of luminous regions which contain the above-mentioned n type gallium nitride system compound semiconductor layer, the above-mentioned luminous layer, and the above-mentioned p type gallium nitride system compound semiconductor layer, respectively in the luminescent device concerning the present invention on one main surface of the above-mentioned translucent substrate of the above-mentioned nitride semiconductor light emitting element.

[0009]

A plurality of above-mentioned luminous regions are formed in a rectangle, respectively, and it may be made to juxtapose each luminous region to a short side direction in the luminescent device concerning the present invention.

[0010]

It may be made to connect a plurality of above-mentioned luminous regions in series, and may be made to connect a plurality of above-mentioned luminous regions in parallel in the luminescent device concerning the present invention.

The process at which the manufacturing method of the luminescent device concerning the present invention forms a plurality of luminous regions which contain a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer, respectively on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which the fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in the light of long wave length from the wavelength of the absorbed light was distributed to the main surface of another side of a translucent substrate, by carrying out a condensation polymerization, The process of forming the SiO_2 layer containing a fluorescent substance on the main surface of another side of the above-mentioned translucent substrate, The translucent substrate in which the above-mentioned SiO_2 layer was formed is divided for each element of every, and it has the process of producing a nitride semiconductor light emitting element, and the process of carrying out flip chip mounting of the nitride semiconductor light emitting element to a package.

The nitride semiconductor light emitting element concerning the present invention, In the nitride semiconductor light emitting element which comes to form a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which the fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in the light of long wave length from the wavelength of the absorbed light was distributed to the main surface of another side of the translucent substrate 11, By carrying out a condensation polymerization, the translucent substrate in which the SiO_2 layer was formed on the main surface of another side of the above-mentioned translucent substrate, and the SiO_2 layer was formed is divided for each element of every, it is produced, and light is outputted via the SiO_2 layer.

The manufacturing method of the nitride semiconductor light emitting element concerning the present invention, The process of forming a plurality of luminous regions which contain a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer, respectively on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which the fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in the light of long wave length from the wavelength of the absorbed light was distributed to the main surface of another side of the translucent substrate 11, by carrying out a condensation polymerization, It has the process of forming the SiO_2 layer containing a fluorescent substance on the main surface of another side of the above-mentioned translucent substrate, and the process of dividing the translucent substrate in which the above-mentioned SiO_2 layer was formed for each element of every.

[0011]

[Mode for carrying out the invention]

Hereinafter, it describes about the nitride semiconductor light emitting element of the embodiment concerning the present invention, referring to Drawings.

Embodiment 1.

The nitride semiconductor light emitting element of this embodiment 1 arranges mutually the

three rectangular light emitting devices 1, 2, and 3 in parallel to one surface of the sapphire translucent substrate (1000 micrometers x 1000 micrometers) 11, as shown in Fig.1, it is the light emitting device constituted so that light might be outputted via the translucent substrate 11, and formed in the surface (luminescence observation surface) of another side of the translucent substrate 11 the SiO₂ film 70 containing the fluorescent substance 71.

The light emitting devices 1, 2, and 3 are elements which emit light in the ultraviolet radiation which has the wavelength of an ultraviolet region, respectively here, and the fluorescent substance 71 is a fluorescent substance which absorbs ultraviolet radiation and generates the light of a predetermined color.

As for the quantity of the fluorescent substance 71 contained in the SiO₂ film 70, in the nitride semiconductor light emitting element of this embodiment 1, it is preferable to set up so that the light outputted via the SiO₂ film 70 may turn into only light by which wavelength conversion was substantially carried out with the fluorescent substance 71.

[0012]

As mentioned above, in the nitride semiconductor light emitting element of this embodiment 1, white light is not acquired with mixed colors with the light by which wavelength conversion was carried out to the blue glow which a light emitting element chip generates like a conventional case with the fluorescent substance, but since only the light of the predetermined color which the fluorescent substance 71 excited by ultraviolet rays generates is used, dispersion in the luminescent color can be stopped very small.

That is, a color changes -- since the ratio of blue glow and yellow light will change if the light emitting luminance of a light emitting element chip changes, become white tinged with blue or the white light emitting diode using the conventional mixed colors becomes yellowish white light.

On the other hand, in the nitride semiconductor light emitting element of this embodiment 1, since only the light which the fluorescent substance 71 excited by ultraviolet rays generates is used, even if the light emitting luminance of a light emitting element chip changes, the luminescent color of a fluorescent substance itself hardly changes, and it can make change of the luminescent color very small.

[0013]

When the content of the fluorescent substance contained in resin differs in the conventional composition, since the ratio of blue glow and yellow light changes, a color changes, but, in the nitride semiconductor light emitting element of this embodiment 1, even if the content of a fluorescent substance changes, the luminescent color of a fluorescent substance itself hardly changes, and it can make change of the luminescent color very small.

In the conventional composition, since the mold of the resin containing a fluorescent substance was carried out after mounting a light emitting element chip in a substrate etc., when the mounting position of a chip varied, there was a problem that an irregular color and chromaticity dispersion arose, for example, but, in the composition of the present invention, since it can do that the positional relationship of a luminous region and a fluorescent substance is always constant, this problem is solvable.

[0014]

Next, it describes about the fluorescent substance 71 in the nitride semiconductor light emitting element of this embodiment 1, and the SiO₂ layer 70 containing the fluorescent substance 71. it can use, if it is a fluorescent substance which is excited by ultraviolet radiation as the fluorescent substance 71, and generates the light of a predetermined color in this embodiment 1 -- as an example -- for example

(1) Re₃(PO₄)₃Q:Eu, Re' (however, Re with at least 1 type chosen from Mg, Ca, Ba, Sr, and Zn) At least 1 type as which Q is chosen from F of a halogen, Cl, Br, and I, and Re' have at least 1 type chosen from Mn, Fe, Cr, and Sn (white).

(2) Re₃(PO₄)₃Q:Eu (however, at least 1 type as which Re is chosen from Sr, Ca, Ba, and Mg, and Q have at least 1 type chosen from F of a halogen, Cl, Br, and I.) (blue),

(3) BaMg₂Al₁₆O₂₇:Eu (blue),

(4) BaMg₂Al₁₆O₂₇:Eu, Mn (green),

(5) (SrEu) O-Al₂O₃ (green),

(6) 3.5MgO and 0.5MgF₂*GeO₂:Mn (red),

(7) Y₂O₃:Eu (red),

(8) Mg₆As₂O₁₁:Mn (red),

(9) Gd₂O₃:Eu (red) -- and

(10) La₂O₃:Eu (red) etc. are mentioned.

These fluorescent substances may be used solely, and it may mix and may use them.

[0015]

Hereinafter, it describes more specifically about the case where the light emitting element chip which generates the light of an ultraviolet region, and a plurality of fluorescent substances are combined.

According to this embodiment, if a fluorescent substance (for example, red, a green and blue fluorescent substance) of a different kind is mixed in the one SiO₂ layer 70, it may be made to distribute it and it does in this way, the white light by the mixed colors of the light from a different fluorescent substance will be acquired. In this case, in order to improve more light which emits light from each fluorescent substance mixed colors and to decrease color unevenness, it is preferable to distribute in the SiO₂ layer 70 uniformly [as for the mean particle diameter and form of each fluorescent substance, it is preferable that it is similar, and / each fluorescent substance].

[0016]

Each separate SiO₂ layer is made to distribute each fluorescent substance, and it may be made to form the SiO₂ layer 70 of the multiplet structure by laminating them in the present invention. Thus, when it constitutes a SiO₂ layer as a multiplex thin film and laminates on an element in consideration of the ultraviolet radiation transmissivity of each fluorescent substance at order

called a red fluorescent material layer, a green fluorescence material layer, and a blue phosphor layer, all the layers can be made to absorb ultraviolet radiation uniformly, and it is preferable. In the SiO₂ layer 70 which is a multiplex thin layer, from a lower layer, so that the particle diameter of the fluorescent substance in each layer may become small [the upper layer]. If size relation of the mean particle diameter of each fluorescent substance is used as a blue phosphor > green fluorescence substance > red fluorescent substance, fitness can be made to transmit ultraviolet radiation to the top layer, and it cannot leak to the SiO₂ layer 70 which is a multiplex thin film layer, and can make it absorb ultraviolet radiation.

[0017]

In addition, as each convert-colors part in which each fluorescent substance is contained so that it may become stripe shape, lattice shape, or the shape of a triangle is arranged, it may be made to form SiO two-layer 70. An interval is provided, it may be made to make it arrange between each convert-colors part, and, thereby, mixed-colors nature can be made good. Since leakage of ultraviolet radiation can be prevented if it forms SiO two-layer so that all the circumferences of an element may be covered, it is preferable.

[0018]

The SiO₂ layer 70 containing the fluorescent substance 71, For example, the fluorescent substance (powder) 71 is distributed in the silica sol which mixes a silanol (Si(OEt)₃OH) and ethanol at a predetermined ratio. After carrying out the coat of the silica sol by which the fluorescent substance was distributed to the main surface of another side of the translucent substrate 11 with a spinner, it can form by carrying out a condensation polymerization.

Thus, unlike conventional resin, since the formed SiO₂ layer 70 is an inorganic substance, its degradation by ultraviolet rays is very small compared with resin, and ultraviolet radiation can be used for it in combination with the light emitting diode (ultraviolet area light emitting diode) which emits light.

On the other hand, since almost all resin deteriorated by ultraviolet rays and the element which can be equal to prolonged use could not be constituted in the composition which distributed the fluorescent substance in resin like a conventional case, utilization of the white light emitting diode using an ultraviolet area light emitting diode was difficult.

[0019]

By this embodiment 1, the content of the fluorescent substance 71 contained in the SiO₂ film 70 here, so that the light outputted via the SiO₂ film 70 may turn into only white light by which wavelength conversion was substantially carried out with the fluorescent substance 71. That is, it is preferable to set up comparatively largely so that most ultraviolet radiation which emitted light with the light emitting element chip may be absorbed into the fluorescent substance 71 and it may excite the fluorescent substance 71. If it does in this way, luminous efficiency (ratio of the light to the electric power input into the light emitting device outputted) can be made high.

[0020]

The quantity of the fluorescent substance made to contain in the SiO₂ film 70, Although it is made to correspond to a desired color tone, and is set to various values and the present invention is not limited by the content of a fluorescent substance, according to examination of the inventors. If the content of the fluorescent substance 71 contained in the SiO₂ film 70 increases, it is checked that the bond strength of the SiO₂ film 70 to the translucent substrate 11 becomes strong. If the surface of this bond strength is taken into consideration, the content of the fluorescent substance in the SiO₂ film 70, It is preferable to set up to 30wt% - 80wt%, and in order to obtain the higher bond strength of the SiO₂ film 70 to the substrate 11, it is still more preferable to set up to 40wt% - 80wt%.

[0021]

In the light emitting devices 1, 2, and 3 of the nitride semiconductor light emitting element of this embodiment 1, each semiconductor layer and an electrode are formed as follows, respectively.

(1) For example, the n type gallium nitride system compound semiconductor layer grown-up all over substantially on the translucent substrate 11 which consists of sapphire is separated by the isolation groove 41, and the n type gallium nitride system compound semiconductor layer 12 (n layer 12) is formed so that plane shape may become a rectangle.

[0022]

(2) The active layer 10 is a rectangle which has width narrower than substantially same length and n layer 12 as the n layer 12, and it is formed on the n layer 12 so that the one long side may correspond to one long side of the n layer 12 substantially. By forming in this way, the region for forming n side ohmic electrode along with the active layer 10 on the n layer 12 is secured.

Here, in this embodiment 1, the width of the active layer 10 was set up so that the distance L1, L2, and L3 of the long side and n side ohmic electrode which are placed at the side which is separated from n side ohmic electrode might be set to 220 micrometers.

Thus, the Reason for having set the distance L1, L2, and L3 as 220 micrometers is that the current injected into the active layer in the position which separated 220 micrometers or more from n side ohmic electrode decreases.

Here, in this embodiment 1, the In_xGa_{1-x}N layer which can change a luminous wavelength by changing the content of In constitutes the active layer 10, and luminescence of ultraviolet radiation sets the quantity of this In as a possible value.

[0023]

(3) The n side ohmic electrode 14 (14a) has the substantially same length as the active layer 10, on the n layer 12, along with the active layer 10, approaches with the active layer 10 and is formed.

The layer which contains W and Al which can make good ohmic contact with the n layer 12, for example constitutes the n side ohmic electrode 14 (14a). If an example is given, the n side ohmic electrode 14 (14a) will be formed by laminating successively W layer (200A), an Al layer

(1000Å), W layer (500Å), a Pt layer (3000Å), and an Ni layer (60Å).

[0024]

(4) The p type gallium nitride system semiconductor layer 13 has the same plane shape as the active layer 10, and is formed in piles on the active layer 10.

Actually, after forming the active layer 10 and the p layer 13 in piles on the n layer 12, the active layer 10 and the p type gallium nitride system semiconductor layer 13 are formed by etching collectively, in order to expose the n layer 12 surface which forms the n side ohmic electrode 14.

[0025]

(5) In order to be formed all over substantially on the p type gallium nitride system semiconductor layer 13 and to obtain the p layer 13 and good ohmic contact, constitute the p side ohmic electrode 15 by laminating an Ni layer and a Pt layer, for example.

[0026]

(6) And the p pad electrode 16 (16a) consists of Pt of 3000 Å of film thickness, and is formed on the p side ohmic electrode 15 along the long side of the p side ohmic electrode 15 which is placed at the side left in the n side ohmic electrode 14, for example.

[0027]

In the accumulated type nitride semiconductor light emitting element of this embodiment 1, between elements is separated by the insulation protection film 17, and the light emitting devices 1, 2, and 3 constituted as mentioned above are connected as follows by the bonding electrode 21.

The insulation protection film 17 is formed so that the whole element may be covered except for the p pad electrode 16 of each light emitting device 1 (16a), and n side ohmic electrode 14 (14a) top.

Continuously, between is formed by the bonding electrode 21 on the insulator layer 17 formed in the isolation groove 41, and the p side ohmic electrode 16a of the light emitting device 2 on the n side ohmic electrode 14a of the light emitting device 1, and by this, The n side ohmic electrode 14a of the light emitting device 1 and the p side ohmic electrode 16a of the light emitting device 2 are connected.

Between the light emitting device 2 and the light emitting device 3, the bonding electrode 21 is formed similarly, and, thereby, the n side ohmic electrode 14a of the light emitting device 2 and the p side ohmic electrode 16a of the light emitting device 3 are connected. The bonding electrode 21 can consist of various metal, such as Pt or Au.

[0028]

In this embodiment 1, the bonding electrode 21 and the electrode 26 for external connection which consists of the same material are further formed on the p pad electrode 16 of the light emitting device 1, and the bonding electrode 21 and the electrode 24 for external connection which consists of the same material are formed on the n pad electrode 14 of the light emitting device 3.

[0029]

The nitride semiconductor light emitting element of the embodiment 1 constituted as mentioned above, Since the surface of another side of the translucent substrate 11 is made to contain a fluorescent substance in the SiO₂ layer 70 which is an inorganic substance and does not almost have degradation by ultraviolet rays and it forms in it, it becomes possible to use an ultraviolet area light emitting diode as a light emitting element chip.

By this, it cannot be based on the mixed colors of the light of a light emitting element chip, and the light of a fluorescent substance, but a light emitting diode can be constituted only using the light from a fluorescent substance, and very few light emitting diodes of a color change can be realized.

Since the layer which contains a fluorescent substance since it constitutes using the SiO₂ layer 70 which is an inorganic substance containing a fluorescent substance can make an environmental capability-proof good as compared with the conventional resin layer as for the nitride semiconductor light emitting element of this embodiment 1, it can lengthen the life of an element.

[0030]

Application.

In the same composition as the nitride semiconductor light emitting element of this embodiment 1, increase the light emitting device which emits light in ultraviolet radiation to 35 pieces, connect in series, and those elements as the fluorescent substance 71. For example, the nitride semiconductor light emitting element for lighting which has a comparatively wide emission area can be constituted by using Ca₁₀(PO₄)₆FCl:Eu and Mn.

When it is used for it, having carried out direct continuation of the nitride semiconductor light emitting element for lighting constituted in this way to the ordinary home power supply of 100V, the electric current value of each element can be set as substantially optimal about 20 mA in respect of luminous efficiency and a life, and it can use it for a signal, lighting for home use, etc.

[0031]

Embodiment 2.

Next, about the nitride semiconductor light emitting element of the embodiment 2 concerning the present invention, while referring to Fig.4, it describes.

The accumulated type nitride semiconductor light emitting element of this embodiment 2 differs from the nitride semiconductor light emitting element of embodiment 1 in respect of the following.

The different features 1.

In the accumulated type nitride semiconductor light emitting element of embodiment 1, without forming the bonding electrode 21 and the external connection electrodes 24 and 26, The insulation protection film 30 is formed so that the whole element may be covered, the through hole 61 which penetrates the insulation protection film 30, respectively is formed on p pad

electrode of the light emitting devices 1, 2, and 3, and the through hole 62 which penetrates the insulation protection film 30, respectively is formed on n side ohmic electrodes each of the light emitting devices 1, 2, and 3.

[0032]

The different features 2.

Between p pad electrode of the light emitting devices 1, 2, and 3 is mutually connected with the bonding electrode 51 via the through hole 61 formed in the insulation protection film 30.

The different features 3.

Between n side ohmic electrode of the light emitting devices 1, 2, and 3 is mutually connected with the bonding electrode 52 via the through hole 62 formed in the insulation protection film 30.

It constitutes like the accumulated type nitride semiconductor light emitting element of embodiment 1 except the above the different features 1 and 2 and 3.

That is, the accumulated type nitride semiconductor light emitting element of embodiment 2 is a thing connected to parallel about the light emitting devices 1, 2, and 3 in the element of embodiment 1.

The nitride semiconductor light emitting element of the embodiment 2 constituted as mentioned above has the same operation effect as embodiment 1.

[0033]

Although described about the case where the number of luminous regions is three, in the above embodiment 1 and 2, the present invention is not limited to this and may consist of four or more luminous regions.

For example, as shown in Fig.5, the light emitting diode in which the surface light of the area with dispersion wide few moreover in the luminescent color whose luminance is high is possible is realizable by juxtaposing and forming the luminous region { a large number (m pieces) } 1 - m in the short side direction of each region.

[0034]

Although described about the case where the number of luminous regions is three, in the above embodiment 1 and 2, For example, the present invention is not limited to this and it has only one luminous region; it cannot be overemphasized that it is also applicable to the light emitting diode (300 micrometers x 300 micrometers) of a size generally used well.

In this case, as shown in Fig.6, separation for each element removes the SiO₂ layer 70 between the element and element which should be divided, forms the slot 72, and should just divide it by scribing or dicing in that slot 72, for example.

[0035]

In the above embodiment 1 and 2, described about the preferable embodiment rather than having started the present invention which used the ultraviolet area light emitting element chip, but. The present invention may constitute a white light emitting diode combining the fluorescent substance of an yttrium aluminum garnet (YAG) system which is not restricted to this, is excited by the blue glow of a blue light emitting element chip and the chip, and generates a yellow light and which is described below.

[0036]

The YAG system fluorescent substance used for the present invention is based on the yttrium aluminum oxide system fluorescent substance activated with the cerium which excites the light which emitted light from the semiconductor light emitting element which makes a nitride system semiconductor a luminous layer, and can emit light.

As a specific yttrium aluminum oxide system fluorescent substance, YAlO₃:Ce, Y₃Al₅O₁₂:Ce(s) (YAG:Ce) and Y₃Al₂O₅:Ce(s), these mixtures, etc. are mentioned. At least 1 type of Ba, Sr, Mg, Ca, and Zn may be contained in the yttrium aluminum oxide system fluorescent substance. By making Si contain, the reaction of crystal growth can be inhibited and the particles of a fluorescent substance can be arranged.

[0037]

In this Description, especially the yttrium aluminum oxide system fluorescent substance activated by Ce shall be interpreted in a broad sense. What replaced some or the whole of yttrium by at least one element chosen from the group which consists of Lu, Sc, La, Gd, and Sm, Or it is used for the wide meaning containing the fluorescent substance which has scintillation effects, such as what replaced a part or the whole of aluminum by any of Ba, Ti, Ga, and In, or both.

[0038]

That is, at the present invention, it is a general formula (Y_zGd_{1-z})₃Al₅O₁₂:Ce). The photoluminescence fluorescent substance and general formula (Re_{1-a}Sm_a)₃Re'₂O₁₂:Ce) which are shown by {0< z<=1 [however,]} (however, at least 1 type as which 0<=a<1, 0<=b<=1, and Re are chosen from Y, Gd, La, and Sc, and Re' are at least 1 type chosen from Al, Ga, and In.) -- the photoluminescence fluorescent substance shown can be used.

[0039]

For garnet structure, these fluorescent substances are strong for heat, light, and moisture, and can set up the peak of an excitation spectrum near 450 nm. It has a broadcloth emission spectrum in which a light emission peak is also near 580 nm, and it pulls the skirt to 700 nm. Tb, Cu, Ag, Au, Fe, Cr, Nd, Dy, Co, nickel, Ti, Eu, Pr, etc. may be made to contain according to a request in addition to Ce.

[0040]

The photo luminescence fluorescent substance can make high excited light efficiency of a long wavelength region of 460 nm or more by containing Gd (gadolinium) during a crystal. By the increase in the content of Gd, an emission peak wavelength moves to long wavelength, and also shifts the whole luminous wavelength to the long wavelength side. That is, when the strong luminescent color of redness is required, the substitution volume of Gd can be attained by making [many] it. On the other hand, Gd increases and the light emitting luminance of the photoluminescence by blue glow tends to be deteriorated.

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[Translation done.]

[0041]

And a luminous wavelength shifts a part of Al to the short wavelength side in replacing by Ga among composition of an yttrium aluminum garnet system fluorescent substance with garnet structure. A luminous wavelength shifts a part of Y of composition to the long wavelength side in replacing by Gd.

[0042]

When replacing a part of Y by Gd, it is preferable to carry out substitution to Gd to less than ten percent, and to set content (substitution) of Ce as 1.0 from 0.03. A red component is suppliable with the substitution to Gd increasing the content of Ce, although the red component of a green component decreases largely at the less than twenty percent, and a desired color tone can be acquired, without making luminance be deteriorated. If such composition is used, temperature characteristics become good and it can improve the reliability of a light emitting diode. If the photo luminescence fluorescent substance adjusted so that it might have many red components is used, the luminescent device which can emit light in neutral colors, such as pink, can be formed.

[0043]

An oxide or the compound which turns into an oxide easily at an elevated temperature is used for such a photo luminescence fluorescent substance as a raw material of Y, Gd, Al, and Ce, it mixes them sufficiently by a stoichiometric ratio, and obtains a raw material. Or the coprecipitated oxide produced by calcinating what carried out the coprecipitation of the solution which dissolved the rare earth element of Y, Gd, and Ce in acid by the stoichiometric ratio with oxalic acid, and an aluminum oxide are mixed, and a mixed raw material is obtained. Mix a proper quantity of fluorides, such as barium fluoride and ammonium fluoride, as flux to this, stuff crucible, calcinate in the temperature requirement of 1350-1450 degree in the air C for 2 to 5 hours, obtain a burned product, and then it carries out the ball mill of the burned product underwater, It can obtain by letting a screen pass at washing, separation, drying, and the last.

[0044]

In the light emitting diode of the invention in this application, such a photo luminescence fluorescent substance may mix the yttrium aluminum garnet (garnet type) fluorescent substance and other fluorescent substances which were activated with two or more kinds of cerium.

[0045]

Otherwise absorb blue, and blue-green and green and as a fluorescent substance in which red can emit light, The nitrogen content $\text{Ca-Al}_2\text{O}_3\text{-SiO}_2$ fluorescent substance (oxy nitride fluorescence glass) etc. which were activated by the sapphire (aluminum oxide) fluorescent substance, Eu, and/or Cr which were activated by Eu and/or Cr are mentioned. White light can also be acquired using these fluorescent substances with the mixed colors of the light from a light emitting device, and the light from a fluorescent substance.

[0046]

In order to improve a radiant power output, as for the mean particle diameter of the fluorescent substance used by the present invention, 10 micrometers - 50 micrometers are preferable, and it is 15 micrometers - 30 micrometers more preferably. Mean particle diameter shows here the mean particle diameter measured in the subsieve sizer by making an air permeability method into a basic principle. The rate of the absorption of light and conversion efficiency are high, and the fluorescent substance which has such particle diameter has the wide width of excited wavelengths. Thus, by making the large diameter fluorescent substance which has the characteristics excellent in the optical target contain, it becomes possible to also convert satisfactorily the light of a dominant wavelength periphery of a light emitting device, and to emit light, and the mass production nature of a luminescent device improves.

[0047]

the fluorescent substance which has this mean-particle-diameter value -- frequency -- containing highly is preferable and 20% - 50% of a frequency value is preferable. Thus, the luminescent device which color unevenness is inhibited and has a good color tone is obtained by using a fluorescent substance with small variation in particle diameter.

[0048]

Similarly, the nitrogen content $\text{CaO-Al}_2\text{O}_3\text{-SiO}_2$ fluorescent substance activated by Eu and/or Cr is mentioned as other specific fluorescent substances used for the present invention. The nitrogen content $\text{CaO-Al}_2\text{O}_3\text{-SiO}_2$ fluorescent substance activated by this Eu and/or Cr, Melting of the powder which mixed the rare earth raw material to the predetermined ratio is carried out to raw materials, such as an aluminum oxide, yttrium oxide, silicon nitride, and a calcium oxide, and it is made to mold into them in 1300 degrees C to 1900 degrees C (from 1500 degrees C to 1750 degrees C [Preferably]) in the bottom of a nitrogen atmosphere. The ball mill of the molded article can be carried out, and a fluorescent substance can be made to form in washing, separation, drying, and the last through a screen. It can be considered as the excitation spectrum which had a peak in 450 nm by this, and the Ca-Al-Si-O-N system oxy nitride fluorescence glass activated by Eu and/or Cr in which red light can emit light by the blue glow which has a peak in about 650 nm.

[0049]

The peak of an emission spectrum can be continuously shifted from 575 nm to 690 nm by fluctuating the nitrogen content of the Ca-Al-Si-O-N system oxy nitride fluorescence glass activated by Eu and/or Cr. Similarly, an excitation spectrum can also be shifted continuously. Therefore, a white system can be made to emit light by the synthetic light of the light from the gallium nitride system compound semiconductor which contains in a luminous layer GaN by which impurities, such as Mg and Zn, were doped, and InGaN, and the light of about 580-nm fluorescent substance. In particular, about 490-nm light can also obtain luminescence ideal for combination with the light emitting device which consists of the gallium nitride system compound semiconductor which contains in a luminous layer InGaN which can emit light to high-intensity.

[0050]

moreover -- using the light emitting device in which a blue system can emit light by combining the nitrogen content Ca-Al-Si-O-N system oxy nitride fluorescence glass activated by the YAG system fluorescent substance, Eu, and/or Cr which were activated by above-mentioned Ce -- RGB (red and green --) The light emitting diode with very high color rendering properties which contains a blue component in high-intensity can also be made to form. For this reason, any neutral colors can also be made to form very simply only by adding desired paints. In the present invention, any fluorescent substance is an inorganic fluorescent substance, and it can constitute the light emitting diode which has high contrast using an organic light scattering agent, SiO₂, etc., and was excellent in mass production nature.

[0051]

Since the nitride semiconductor light emitting element using the YAG system fluorescent substance constituted as mentioned above is constituted using the SiO₂ layer 70 which is an inorganic substance containing a fluorescent substance, the layer containing a fluorescent substance can make an environmental capability-proof good as compared with the conventional resin layer, and it can lengthen the life of an element.

[0052]

[Working example]

Hereinafter, the working example concerning the present invention is shown. The present invention is not limited to this.

[Working example 1]

(Translucent substrate 11)

Setting the translucent substrate 11 consisting of sapphire (C surface) in the reaction container of MOVPE, and passing hydrogen, the temperature of a substrate is raised to 1050 degrees C, and a substrate is cleaned. The silicon on sapphire which otherwise makes R surface and A surface a main surface as this translucent substrate 11, an insulating substrate like a spinel (MgAl₂O₄), a GaN substrate, etc. may be sufficient.

[0053]

(N type gallium nitride system compound semiconductor layer 12)

The n type gallium nitride system compound semiconductor layer 12 is grown up with the next composition after cleaning a substrate.

The temperature of a substrate is lowered to 510 degrees C, and 100A of buffer layers which come from GaN on the translucent substrate 11 are grown up.

Next, temperature is raised to 1050 degrees C after buffer layer growth, and undoping GaN layer 121 is grown up by 1.5-micrometer film thickness.

Then, GaN layer 122 which cm⁻³[4.5x10¹⁸]-doped Si at 1050 degrees C is grown up by 2.2-micrometer film thickness.

[0054]

Then, GaN layer 124 which is 3000-A film thickness about undoping GaN layer 123, and cm⁻³[4.5x10¹⁸]-doped Si further at 1050 degrees C grows up 300 A of undoping GaN layers 125 by 50-A film thickness further.

[0055]

Then, at the same temperature, the first layer that consists of the undoping GaN shall be 40 A, and temperature shall be 800 degrees C, then -- growing up the second layer which consists of undoping In_{0.11}Ga_{0.89}N by 20-A film thickness, and repeating these operations -- the -- the n type multilayer film layer 126 on which you made it laminate ten layers at a time alternately in order of 1+the 2nd+, and it made the first layer laminate finally is grown up.

[0056]

(Active layer 13)

Next, the barrier layer which consists of the undoping GaN shall be grown up by 200-A film thickness after growing up the n type gallium nitride system compound semiconductor layer 12, and temperature shall be 800 degrees C continuously, The well layer which consists of In_{0.03}Ga_{0.97}N which cm⁻³[5x10¹⁷]-doped Si is grown up by 30-A film thickness. And barrier + well + barrier + well Six layers and five layers of well layers are alternately laminated for a barrier layer in order, and the active layer 13 which consists of a multiplex quantum well of 1350 A of the total film thickness is made to laminate.

The active layer which emits light in the light of a 370-nm ultraviolet region as mentioned above is formed.

[0057]

(P type gallium nitride system compound semiconductor layer 14)

The p type gallium nitride system compound semiconductor 14 is grown up with the next composition after active-layer 13 growth.

Next, the 3rd layer that consists of p type Al_{0.1}Ga_{0.9}N which cm⁻³[5x10¹⁹]-doped Mg at 1050 degrees C is grown up by 25-A film thickness, then -- growing up the 4th layer that consists of the undoping GaN by 25-A film thickness, and repeating these operations -- the -- the p type multilayer film layer which consists of superlattice which it laminated four layers at a time alternately 4th in order of 3+ is grown up by 200-A film thickness.

Then, the layer which consists of p type GaN which cm⁻³[1x10²⁰]-doped Mg at 1050 degrees C is grown up by 2700-A film thickness.

Temperature is lowered to a room temperature after ending reaction, annealing is performed at 700 degrees C in a nitrogen atmosphere, and a p type layer is low-resistance-ized further.

[0058]

The wafer into which the gallium nitride system compound semiconductor was grown up as mentioned above is picked out from a reaction container, a SiO₂ mask is formed in the whole wafer except for the portion which forms an isolation groove, and an isolation groove is formed by etching until it reaches silicon on sapphire by RIE. As for the above gallium nitride system compound semiconductors, it is possible to also make boron and a phosphorus contain according to a request.

In order to exfoliate the SiO₂ mask furthermore used for formation of an isolation groove and to expose the n type gallium nitride system compound semiconductor layer 12, A SiO₂ mask is formed on the p type gallium nitride system compound semiconductor layer 14 except the portion to expose, and by RIE, it etches and exposes the surface of the n type gallium nitride system compound semiconductor layer 12 (Si dope GaN layer 122).

[0059]

Next, the opening substantially of the whole surface of the p type gallium nitride system compound semiconductor layer 14 is carried out, a resist application is carried out, on the p type gallium nitride system compound semiconductor layer which carried out the opening, the annealing of 100 A and the Pt is carried out for nickel after 500A lamination, and the p side ohmic electrode 15 is formed so that other portions may be covered. Furthermore, 3000 A is formed for Pt and the p side pad electrode 16a which consists of 60A (16) is formed in some p side ohmic electrodes for nickel.

Next, a resist is removed and the n side ohmic electrode 14 which laminated 500 A and Pt at 3000 A, and laminated [W / 200 A and Al] nickel for 1000 A and W in 60-A order is shortly formed on a n type gallium nitride system compound semiconductor layer.

[0060]

Next, the insulation protection film 17 which consists of SiO₂ is formed in the whole surface by 1.5-micrometer film thickness, and some of p side pad electrodes and n side ohmic electrodes are exposed by RIE.

As a bonding electrode which electrically connects p side pad electrode which carries out mask formation and faces across an isolation groove so that the opening of the portion which furthermore forms a bonding electrode in the surface may be carried out, and n side ohmic electrode, 6000 A and Au are formed at 1000 A, and nickel is formed [Ti] for 400 A and Pt by 60-A film thickness.

Finally the insulation protection film 30 which consists of SiO₂ is formed by 1.5-micrometer film thickness, and it removes by etching the insulation protection film 30 on the bonding electrode 24 and 26 by RIE so that it can electrically connect with outside.

[0061]

(Formation of the SiO₂ layer 70 containing the fluorescent substance 71)

Next, the slurry which mixed a fluorescent substance {Ca₁₀(PO₄)₆Cl:Eu, Mn}, a silanol (Si(OEt)₃ OH), and ethanol is produced.

Here, in the working example 1, the slurry was mixed so that fluorescent substance:silanol:ethanol might be set to 4:1:2 by a weight ratio.

That is, in this example 1, the content of the fluorescent substance to a slurry was set up to 57%.

Next, the slurry film which consists of the fluorescent substance, the silanol, and ethanol which have uniform film thickness is formed in the whole back surface of a substrate by dropping the slurry at the back surface of silicon on sapphire from a nozzle, and rotating a substrate at high speed.

And it is considered as the SiO₂ film which carried out the condensation polymerization of the silanol in a slurry film and in which distributed content of the fluorescent substance was carried out by heating the substrate in which the slurry film was formed within 300 degrees C oven for 3 hours.

Thus, the SiO₂ layer 70 containing the fluorescent substance 71 is formed.

[0062]

Thus, the silicon on sapphire (wafer) which has a plurality of produced element regions is divided for each element of every using scribing and dicing, and a 350x400-micrometer light emitting element chip is produced.

next, the light emitting element chip 80 is shown in Fig.7 -- as -- the package 81 -- each electrode of the positive/negative of the light emitting element chip 80 -- it is made to oppose to the electrode of the positive/negative of the package 81, and flip chip mounting is performed.

And the epoxy resin 83 of translucency is formed so that a light emitting element chip may be covered, and a light emitting element chip is protected.

The white light emitting diode using the light emitting element chip which emits light in ultraviolet radiation as mentioned above can be formed.

[0063]

[Working example 2]

In the working example 1, it constituted like the working example 1 except having changed the content of the fluorescent substance to a slurry to 30%.

As for the light emitting diode of the above working example 2, although the manufacturing yield became low slightly as compared with the working example 1, the performance equivalent to the working example 1 was obtained.

[0064]

[Working example 3]

It constituted like the working example 1 except having changed the content of the fluorescent substance to a slurry to 40%.

The performance equivalent to the working example 1 was obtained, and the manufacturing yield of the light emitting diode of the above working example 3 improved as compared with the working example 2.

[0065]

[Working example 4]

It constituted like the working example 1 except having changed the content of the fluorescent substance to a slurry to 70%.

The performance equivalent to the working example 1 was obtained, and the manufacturing yield of the light emitting diode of the above working example 4 improved as compared with the working example 1.

[0066]

[Working example 5]

In the working example 1, except that the following points differ, it is constituted like the working example 1.

(1) In the working example 1, replace with an ultraviolet region light emitting element chip, and use the light emitting element chip in which blue light is possible.

(2) Use $(Y_{0.8}Gd_{0.2})_3Al_5O_{12}:Ce$ as the fluorescent substance 71.

Hereinafter, it describes in detail about the light emitting diode of this example 5.

In this example 5, as a light emitting element chip, it has a luminous layer which consists of InGa_N, and a main-light-emission peak uses the LED chip which is 470 nm. This LED chip is formed using the MOCVD method. Arrange specifically the silicon on sapphire washed in the reaction chamber, and as reactant gas, Hydrogen gas is used as TMG (trimethyl) gas, TMI (trimethylindium) gas, TMA (trimethylaluminum) gas, ammonia gas, and carrier gas, silane gas and cyclo pen TAJIA magnesium are used as impurity gas, and membranes are formed.

[0067]

AlGa_N which is a low temperature buffer layer on silicon on sapphire as lamination of a light emitting element chip, Ga_N of the Si dope which non-doped Ga_N (about 1500Å in thickness) and the electrode which improve crystallinity are formed, and works as a n type contact layer (about 21650Å in thickness), Non-doped Ga_N (about 3000Å in thickness) which improves crystallinity, Ga_N non-doped as a n type clad layer (about 50Å in thickness), Non-doped Ga_N (about 40Å in thickness) which improves the crystallinity of the multilayer film which consists of the superlattice of Ga_N (about 300Å in thickness) which doped Si, and the luminous layer formed on it. As a luminous layer which consists of the non-doped multilayer film which consists of the superlattice of InGa_N (about 20Å in thickness), and multiple quantum well structure, The multilayer film of non-doped Ga_N (about 250Å in thickness), and InGa_N (about 30Å in thickness), Mg which works as a p type contact layer forms Ga_N (about 1200Å in thickness) by which Mg which is the multilayer film and p type contact layer which consists of superlattice of doped InGa_N (about 25Å in thickness) and GaAlN (about 40Å in thickness) by which Mg was doped was doped.

[0068]

In this way, the semiconductor wafer in which the nitride semiconductor which formed membranes was formed is etched partially, and a p type and a n type contact layer are exposed. After making the electrode of a n type and a p type form on each contact layer using sputtering process, it divides into each light emitting device, and produces the light emitting element chip in which blue can emit light.

And a light emitting diode is produced like the working example 1 using the light emitting element chip which was carried out in this way and produced, and a $(Y_{0.8}Gd_{0.2})_3Al_5O_{12}:Ce$ fluorescent substance.

[0069]

White light is acquired with mixed colors, and since the light emitting diode produced as mentioned above constitutes the layer which contains a fluorescent substance unlike a conventional case from an inorganic substance, as compared with the conventional case, the environmental capability-proof is excellent.

[0070]

[Effect of the Invention]

As described in details above, at the present invention, only light in which a fluorescent substance emits light can constitute a light emitting diode with the white luminescent color using a light emitting diode which emits light in ultraviolet radiation.

Therefore, a white light emitting diode with little variation in the luminescent color can be provided.

Since degradation of the layer which contains a fluorescent substance can be made very small if a light emitting diode with the white luminescent color by mixed colors with a fluorescent substance is constituted using the light emitting diode which emits light in blue glow according to the present invention, as compared with a conventional case, a long-life white light emitting diode can be provided.

[Brief Description of the Drawings]

[Drawing 1] It is a plan view of the nitride semiconductor light emitting element of the embodiment 1 concerning the present invention.

[Drawing 2] It is a fragmentary sectional view (portion of the light emitting devices 1 and 2) about the A-A' line of Fig. 1.

[Drawing 3] It is a fragmentary sectional view (portion of the light emitting device 3) about the A-A' line of Fig. 1.

[Drawing 4] It is a plan view of the nitride semiconductor light emitting element of the embodiment 2 concerning the present invention.

[Drawing 5] It is a plan view of the nitride semiconductor light emitting element of the modification concerning the present invention.

[Drawing 6] In the nitride semiconductor light emitting element of an embodiment, it is the figure showing a situation when a scribe or the SiO₂ layer of a portion which carries out dicing is removed.

[Drawing 7] It is a cross sectional view of the nitride semiconductor light emitting element of the working example concerning the present invention.

[Explanations of letters or numerals]

1, 2, 3 -- Light emitting device,

10 -- Active layer,

11 -- Silicon on sapphire

12 -- N type gallium nitride system compound semiconductor layer

13 -- P type gallium nitride system semiconductor layer,

14, 14 a--n side ohmic electrode,
15 -- P side ohmic electrode
16, 16 a--p pad electrode,
17 -- Insulation protection film,
21, 51, 52 -- Bonding electrode,
24, 26 -- External connection electrode,
30 -- Insulation protection film,
61, 62 -- Through hole,
41 -- Isolation groove,
70 -- SiO two-layer,
71 -- Fluorescent substance.

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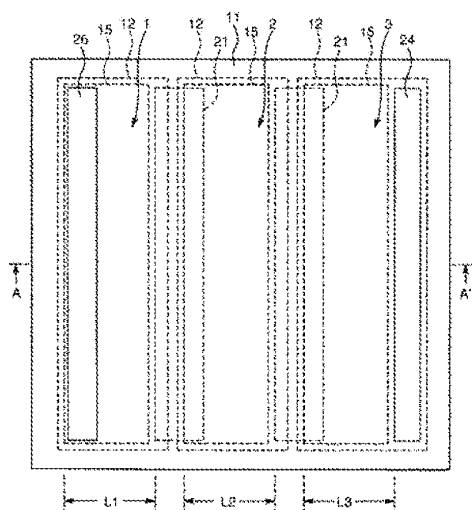
DRAWINGS

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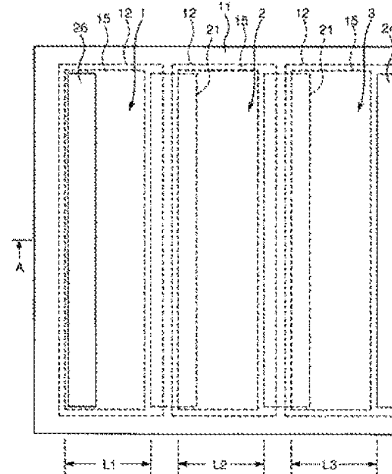
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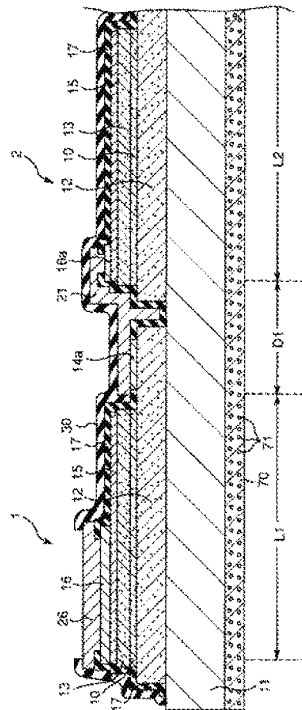
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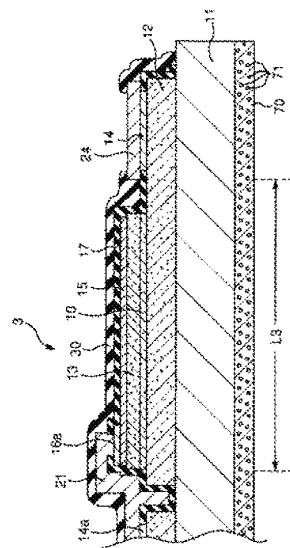
[Drawing 1]



1 | 2 | 3 | 4 | 5 | 6 | 7

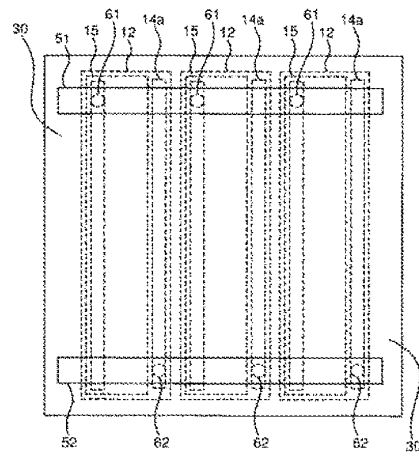


[Drawing 2]

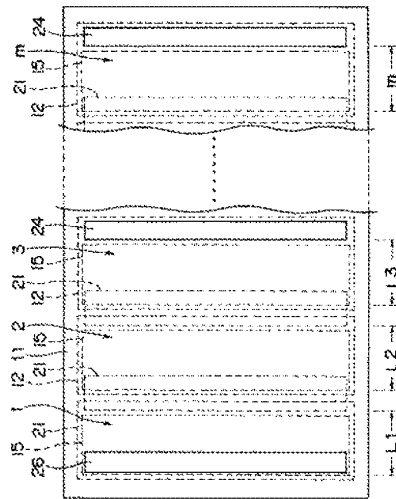


[Drawing 3]

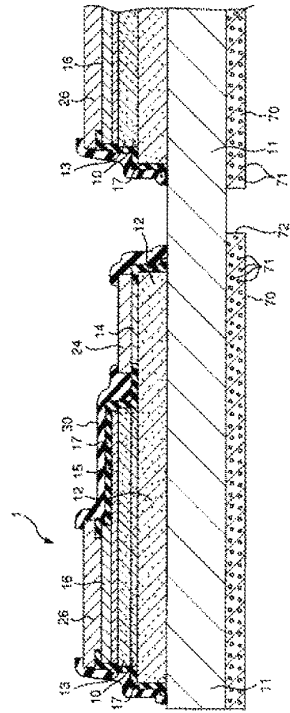
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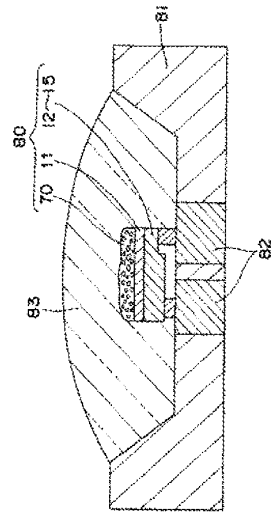
[Drawing 4]



[Drawing 5]



[Drawing 6]



[Drawing 7]

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CLAIMS

(57) [Claim(s)]

[Claim 1]

In a luminescent device which has a nitride semiconductor light emitting element which comes to form a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer on one main surface of a translucent substrate, and a package in which flip chip mounting of the nitride semiconductor light emitting element is carried out.

After carrying out the coat of the silica sol by which a fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in light of long wave length from wavelength of the absorbed light was distributed to a main surface of another side of a translucent substrate. By carrying out a condensation polymerization, a translucent substrate in which a SiO_2 layer was formed on a main surface of another side of the above-mentioned translucent substrate, and the SiO_2 layer was formed is divided for each element of every, and the aforementioned nitride semiconductor light emitting element is produced.

A luminescent device, wherein light is outputted via the aforementioned SiO₂ layer.

[Claim 2]

The above-mentioned luminous layer emits light in light of an ultraviolet region, and is the above-mentioned fluorescent substance,

- (1) $\text{Re}_3(\text{PO}_4)_3\text{Q}:\text{Eu}$, Re' (however, Re with at least 1 type chosen from Mg , Ca , Ba , Sr , and Zn). At least 1 type as which Q is chosen from F of a halogen, Cl , Br , and I , and Re' have at least 1 type chosen from Mn , Fe , Cr , and Sn .
- (2) $\text{Re}_3(\text{PO}_4)_3\text{Q}:\text{Eu}$ (however, at least 1 type as which Re is chosen from Sr , Ca , Ba , and Mg , and Q have at least 1 type chosen from F of a halogen, Cl , Br , and I .), (3) $\text{BaMg}_2\text{Al}_{18}\text{O}_{27}:\text{Eu}$,
- (4) $\text{BaMg}_2\text{Al}_{18}\text{O}_{27}:\text{Eu}$, Mn ,
- (5) $(\text{SrEu})\text{O-Al}_2\text{O}_3$,
- (6) 3.5MgO and $0.5\text{MgF}_2:\text{GeO}_2:\text{Mn}$,
- (7) $\text{Y}_2\text{O}_3:\text{Eu}$,
- (8) $\text{Mg}_6\text{As}_3\text{O}_{11}:\text{Mn}$,
- (9) $\text{Gd}_2\text{O}_3:\text{Eu}$ -- and
- (10) The luminescent device according to claim 1 containing at least one fluorescent substance chosen from a group which consists of $\text{La}_2\text{O}_3:\text{Eu}$.

[Claim 3]

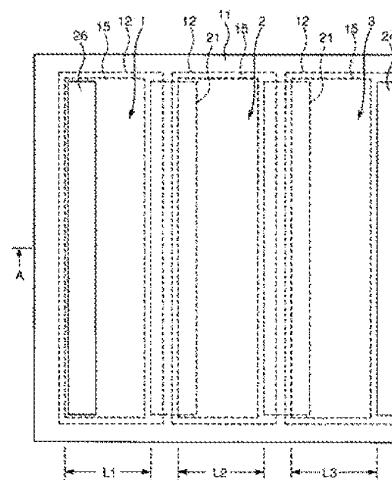
The luminescent device according to claim 1 which is the yttrium aluminum garnet (YAG) system fluorescent substance in which the above-mentioned luminous layer emitted light in a blue light, and the above-mentioned fluorescent substance was activated by Ce.

[Claim 4]

A plurality of luminous regions are formed on one main surface of the above-mentioned translucent substrate of the aforementioned nitride semiconductor light emitting element. A luminescent device of any one description in Claims 1-3 in which the luminous region contains the above-mentioned n type gallium nitride system compound semiconductor layer, the above-mentioned luminous layer, and the above-mentioned p type gallium nitride system compound semiconductor layer, respectively.

[Claim 5]

The luminescent device according to claim 4 which a plurality of above-mentioned luminous regions were formed in a rectangle, respectively, and was juxtaposed in the short side



212 | 3 | 4 | 5 | 6 | 7

direction.

[Claim 6]

The luminescent device according to claim 4 or 5 to which a plurality of above-mentioned luminous regions were connected in series.

[Claim 7]

The luminescent device according to claim 4 or 5 to which a plurality of above-mentioned luminous regions were connected in parallel.

[Claim 8]

A process of forming a plurality of luminous regions which contain a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer, respectively on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which a fluorescent substance which can absorb a part of light where the aforementioned luminous layer emits light, and can emit light in light of long wave length from wavelength of the absorbed light was distributed to a main surface of another side of a translucent substrate, by carrying out a condensation polymerization, A process of forming a SiO₂ layer containing a fluorescent substance on a main surface of another side of the aforementioned translucent substrate,

A process of dividing a translucent substrate in which the aforementioned SiO₂ layer was formed for each element of every, and producing a nitride semiconductor light emitting element,

A process of carrying out flip chip mounting of the aforementioned nitride semiconductor light emitting element to a package,

A manufacturing method of a ****(ing) luminescent device.

[Claim 9]

In a nitride semiconductor light emitting element which comes to form a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which a fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in light of long wave length from wavelength of the absorbed light was distributed to a main surface of another side of the above-mentioned translucent substrate by carrying out a condensation polymerization, A nitride semiconductor light emitting element, wherein it is produced by dividing a translucent substrate in which the SiO₂ layer was formed for each element of every and light is outputted via the SiO₂ layer.

[Claim 10]

A process of forming a plurality of luminous regions which contain a n type gallium nitride system compound semiconductor layer, a luminous layer, and a p type gallium nitride system compound semiconductor layer, respectively on one main surface of a translucent substrate, After carrying out the coat of the silica sol by which a fluorescent substance which can absorb a part of light where the above-mentioned luminous layer emits light, and can emit light in light of long wave length from wavelength of the absorbed light was distributed to a main surface of another side of a translucent substrate, by carrying out a condensation polymerization, A process of forming a SiO₂ layer containing a fluorescent substance on a main surface of another side of the above-mentioned translucent substrate, and a process of dividing a translucent substrate in which the aforementioned SiO₂ layer was formed for each element of every, A manufacturing method of a ****(ing) nitride semiconductor light emitting element.

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same		
First Named Inventor/Applicant Name:		Seo Won Cheol		
Filer:		Alan Michael Taboada		
Attorney Docket Number:		MT100		
Filed as Large Entity				
Filing Fees for ex parte reexam				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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REQUEST FOR EX PARTE REEXAMINATION	1812	1	12000	12000
Pages:				
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Total in USD (\$)				12000

Electronic Acknowledgement Receipt	
EFS ID:	25509423
Application Number:	90013725
International Application Number:	
Confirmation Number:	7313
Title of Invention:	Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same
First Named Inventor/Applicant Name:	Seo Won Cheol
Correspondence Address:	Alan Taboada Moser Taboada 1030 Broad Street Suite 203 Shrewsbury NJ 07702 US 7329357100 docketing@mtiplaw.com
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Attorney Docket Number:	MT100
Receipt Date:	15-APR-2016
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Application Type:	Reexam (Third Party)

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Attorney Docket No.: MT100

Date: 04/15/16

1. ☒ This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 9,070,851 issued June 30, 2015. The request is made by:
 - ☐ patent owner.
 - ☒ third party requester.
2. ☒ The name and address of the person requesting reexamination is:

Alan Taboada - Moser Taboada

1030 Broad Street, Suite 203

Shrewsbury, NJ 07702
3. ☐ a. A check in the amount of \$_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);
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4. ☒ Any refund should be made by ☐ check or ☐ credit to Deposit Account No. _____ 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.
5. ☒ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)
6. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
 - ☐ Landscape Table on CD
7. ☐ Nucleotide and/or Amino Acid Sequence Submission
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 - b. Specification Sequence Listing on:
 - i. ☐ CD-ROM (2 copies) or CD-R (2 copies); or
 - ii. ☐ paper
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8. ☐ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.
9. ☒ Reexamination of claim(s) 1-15 is requested.
10. ☒ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.
11. ☒ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

[Page 1 of 2]

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b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2).

13. ☐ A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. ☒ a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:
H.C. Park & Associates, PLC
1894 Preston White Drive
Reston, VA 20191
Date of Service: 04/15/16; or

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OR

☒ Firm or Individual Name Alan Taboada - Moser Taboada

Address
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City Shrewsbury State NJ Zip 07702

Country USA

Telephone (732) 935-7100 Email ataboada@mtiplaw.com

16. ☐ The patent is currently the subject of the following concurrent proceeding(s):

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☐ c. Copending Interference No. _____

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re <i>Ex Parte</i> Reexamination of:	§	
U.S. Patent No. 9,070,851	§	Control No.: Not Yet Assigned
	§	
	§	Group Art Unit: Not Yet Assigned
Issue Date: June 30, 2015	§	
	§	Examiner: Not Yet Assigned
	§	
For: WAFER-LEVEL LIGHT EMITTING	§	
DIODE PACKAGE AND METHOD OF	§	
FABRICATING THE SAME	§	
	§	
Inventors: Seo et al.	§	

Mail Stop *Ex Parte* Reexamination
Commissioner for Patents
P.O. Box. 1450
Alexandria, VA 22313-1450

**REQUEST FOR *EX PARTE* REEXAMINATION OF U.S. PATENT NO. 9,070,851
UNDER 35 U.S.C. §§ 301-307 AND § 37 C.F.R. 1.510**

Reexamination of U.S. Patent No. 9,070,851

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LIST OF EXHIBITS CITED IN REEXAMINATION

<i>EXHIBIT #</i>	<i>DESCRIPTION</i>
<i>1</i>	<i>United States Patent No. 9,070,851 to Seo et al. entitled “Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same” (hereinafter “the ‘851 patent”)</i>
<i>2</i>	<i>Japan Patent No. 4,151,284 to Seiichiro et al. entitled “Nitride Semiconductor Light Emitting Element”</i>
<i>3</i>	<i>United States Patent No. 7,179,670 to Shelton et al. entitled “Flip-Chip Light Emitting Diode Device Without Sub-Mount”</i>
<i>4</i>	<i>United States Patent No. 8,368,100 to Donofrio et al. entitled “Semiconductor Light Emitting Diodes Having Reflective Structures and Methods of Fabricating Same”</i>
<i>5</i>	<i>United States Patent No. 7,564,887 to Wang et al. entitled “Long Wavelength Vertical Cavity Surface Emitting Lasers”</i>
<i>6</i>	<i>United States Patent No. 6,657,236 to Thibeault et al. entitled “Enhanced Light Extraction in LEDs Through the Use of Internal and External Optical Elements”</i>
<i>7</i>	<i>United States Patent No. 7,335,517 to Hayasaka et al. entitled “Multichip Semiconductor Device, Chip Therefor and Method of Formation Thereof”</i>
<i>8</i>	<i>Japanese Laid Open Patent Publication No. 2002319704 to Takuma et al. entitled “LED Chip”</i>
<i>9</i>	<i>United States Patent No. 6,838,702 to Ho entitled “Light Emitting Diode”</i>
<i>10</i>	<i>Korea Patent No. 610650 to Hwan entitled “Light Emitting Diode Package and Manufacturing Method Thereof”</i>
<i>11</i>	<i>Japanese Laid Open Patent Publication No. 11008414 to Etsuo entitled “Semiconductor Device and Semiconductor Light-Emitting Device”</i>
<i>12</i>	<i>United States Patent Application Publication No. 2009/0140272 to Beeson et al. entitled “Solid-State Light Source”</i>

Reexamination of U.S. Patent No. 9,070,851

I. IDENTIFICATION OF CLAIMS FOR WHICH REEXAMINATION IS SOUGHT

Requester requests ex parte reexamination of claims 1-15 of U.S. Patent No. 9,070,851 (hereinafter “the ‘851 patent”) (Exhibit 1) under the provisions of 35 U.S.C. §§ 301-307 and § 37 C.F.R. 1.510. The ‘851 patent, entitled “Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same,” issued to Seo et al on June 30, 2015 from United States Application Serial No. 13/194,317, filed on July 29, 2011, which claims priority to Korean Application Nos. 10-2010-0092807 and 10-2010-0092808, filed on September 24, 2010. As detailed in this Request, there is nothing new or non-obvious in the claimed subject matter in claims 1-15 of the ‘851 patent. Thus, claims 1-15 of the ‘851 patent should be rejected and canceled in reexamination.

II. PARTICULAR STATEMENTS REGARDING EACH SUBSTANTIAL NEW QUESTION OF PATENTABILITY

Pursuant to 35 U.S.C. § 301 and 37 C.F.R. § 1.510, the following prior art references raise substantial new questions of patentability regarding the claims of the ‘851 patent:

<i>IDENTIFICATION OF REFERENCES</i>	<i>§102 DATE</i>	<i>EXHIBIT #</i>
<i>Japan Patent No. 4,151,284 to Seiichiro et al.</i>	November 22, 2002	2
<i>United States Patent No. 7,179,670 to Shelton et al.</i>	March 5, 2004	3
<i>United States Patent No. 8,368,100 to Donofrio et al.</i>	November 14, 2007	4
<i>United States Patent No. 7,564,887 to Wang et al.</i>	June 30, 2004	5
<i>United States Patent No. 6,657,236 to Thibeault et al.</i>	December 3, 1999	6
<i>United States Patent No. 7,335,517 to Hayasaka et al.</i>	December 1, 1997	7
<i>Japanese Laid Open Patent Publication No.</i>	October 31, 2002	8

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<i>2002319704 to Takuma et al.</i>		
<i>United States Patent No. 6,838,702 to Ho</i>	October 10, 2003	9
<i>Korea Patent No. 610650 to Hwan</i>	August 9, 2006	10
<i>Japanese Laid Open Patent Publication No. 11008414 to Etsuo</i>	January 12, 1999	11
<i>United States Patent Application Publication No. 2009/0140272 to Beeson et al.</i>	December 3, 2007	12

In particular, pursuant to 37 C.F.R. § 1.510(b)(1), Requester submits the following statements pointing out each substantial new question of patentability (“SNQP”):

SNQP Statement No. 1:

Whether Seiichiro et al. anticipates claims 1-4, 7, 9 and 11-12 of the ‘851 patent.

SNQP Statement No. 2:

Whether Shelton et al. anticipates claims 1-4, 7, 11-12 and 14-15 of the ‘851 patent.

SNQP Statement No. 3:

Whether Donofrio et al. anticipates claims 1-3, 5-7 and 11-15 of the ‘851 patent.

SNQP Statement No. 4:

Whether claims 5 and 13 of the ‘851 patent are obvious in light of Seiichiro et al. in view of Wang et al.

SNQP Statement No. 5:

Whether claim 6 of the ‘851 patent is obvious in light of Seiichiro et al. in view of Thibeault et al.

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SNOP Statement No. 6:

Whether claim 8 of the '851 patent is obvious in light of Seiichiro et al. in view of Hayasaka et al.

SNOP Statement No. 7:

Whether claim 8 of the '851 patent is obvious in light of Seiichiro et al. in view of Takuma et al.

SNOP Statement No. 8:

Whether claim 10 of the '851 patent is obvious in light of Seiichiro et al. in view of Ho.

SNOP Statement No. 9:

Whether claim 10 of the '851 patent is obvious in light of Seiichiro et al. in view of Hwan.

SNOP Statement No. 10:

Whether claim 10 of the '851 patent is obvious in light of Seiichiro et al. in view of Etsuo.

SNOP Statement No. 11:

Whether claims 14 and 15 of the '851 patent are obvious in light of Seiichiro et al. et al in view of Donofrio et al.

Reexamination of U.S. Patent No. 9,070,851

SNOP Statement No. 12:

Whether claims 5 and 13 of the '851 patent are obvious in light of Shelton et al. in view of Wang et al.

SNOP Statement No. 13:

Whether claim 6 of the '851 patent is obvious in light of Shelton et al. in view of Thibeault et al.

SNOP Statement No. 14:

Whether claim 8 of the '851 patent is obvious in light of Shelton et al. in view of Hayasaka et al.

SNOP Statement No. 15:

Whether claim 8 of the '851 patent is obvious in light of Shelton et al. in view of Takuma et al.

SNOP Statement No. 16:

Whether claims 9 and 10 of the '851 patent are obvious in light of Shelton et al. in view of Ho.

SNOP Statement No. 17:

Whether claims 9 and 10 of the '851 patent are obvious in light of Shelton et al. in view of Hwan.

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SNOP Statement No. 18:

Whether claims 9 and 10 of the '851 patent are obvious in light of Shelton et al. in view of Etsuo.

SNOP Statement No. 19:

Whether claim 4 of the '851 patent is obvious in light of Donofrio et al. in view of Beeson et al.

SNOP Statement No. 20:

Whether claim 8 of the '851 patent is obvious in light of Donofrio et al. in view of Hayasaka et al.

SNOP Statement No. 21:

Whether claim 8 of the '851 patent is obvious in light of Donofrio et al. in view of Takuma et al.

SNOP Statement No. 22:

Whether claims 9 and 10 of the '851 patent are obvious in light of Donofrio et al. in view of Ho.

SNOP Statement No. 23:

Whether claims 9 and 10 of the '851 patent are obvious in light of Donofrio et al. in view of Hwan.

Reexamination of U.S. Patent No. 9,070,851

SNOP Statement No. 24:

Whether claims 9 and 10 of the '851 patent are obvious in light of Donofrio et al. in view of Etsuo.

SNOP Statement No. 25:

Whether claim 6 of the '851 patent is obvious in light of Seiichiro et al. in view of Donofrio et al.

SNOP Statement No. 26:

Whether claim 6 of the '851 patent is obvious in light of Shelton et al. in view of Donofrio et al.

Under 35 U.S.C. § 304, the Office must determine whether "a substantial new question of patentability" affecting any claim of the patent has been raised. Additionally, 37 CFR § 1.510(b)(1) requires that a request for ex parte reexamination include "a statement pointing out each substantial new question of patentability based on prior patents and printed publications." If such a new question is found, an order for *ex parte* reexamination of the patent is issued. It is therefore important to identify, and this Request clearly sets forth in detail, the "substantial new questions of patentability" in view of prior patents and printed publications.

Reexamination of U.S. Patent No. 9,070,851

As set out below, all of the claims of the '851 patent are anticipated or rendered obvious by the prior art set forth above and discussed below. In the sections that follow, Requester provides proposed rejections of the claims of the '851 patent, a summary of the scope and content of the '851 patent, and a summary of the prosecution history of the '851 patent. Additionally, Requester provides a discussion of the scope and content of the prior art and a detailed explanation of the relevance and manner of applying the prior art to claims 1-15 of the '851 patent.

III. PROPOSED REJECTIONS OF THE CLAIMS OF THE '851 PATENT

Claims 1-4, 7, 9, and 11-12 are rejected under pre-AIA 35 U.S.C. § 102 (b) as anticipated by Japan Patent No. 4,151,284, issued to Seichiro et al.

Claims 1-4, 7, 11-12, and 14-15 are rejected under pre-AIA 35 U.S.C. § 102 (b) as anticipated by United States Patent No. 7,179,670, issued to Shelton et al.

Claims 1-3, 5-7 and 11-15 are rejected under pre-AIA 35 U.S.C. § 102 (e) as anticipated by United States Patent No. 8,368,100, issued to Donofrio et al.

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Claims 5 and 13 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of United States Patent No. 7,564,887, issued to Wang et al.

Claim 6 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of United States Patent No. 6,657,236, issued to Thibeault et al.

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of United States Patent No. 7,335,517, issued to Hayasaka et al.

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of Japanese Laid Open Patent Publication No. 2002319704, issued to Takuma et al.

Claim 10 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of United States Patent No. 6,838,702, issued to Ho.

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Claim 10 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of Korea Patent No. 610650, issued to Hwan.

Claim 10 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al., in view of Japanese Laid Open Patent Publication No. 11008414, issued to Etsuo.

Claims 14 and 15 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seiichiro et al, in view of United States Patent No. 8,368,100, issued to Donofrio et al.

Claims 5 and 13 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of United States Patent No. 7,564,887, issued to Wang et al.

Claim 6 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of United States Patent No. 6,657,236, issued to Thibeault et al.

Reexamination of U.S. Patent No. 9,070,851

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of United States Patent No. 7,335,517, issued to Hayasaka et al.

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of Japanese Laid Open Patent Publication No. 2002319704, issued to Takuma et al.

Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of United States Patent No. 6,838,702, issued to Ho.

Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of Korea Patent No. 610650, issued to Hwan.

Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of Japanese Laid Open Patent Publication No. 11008414, issued to Etsuo.

Reexamination of U.S. Patent No. 9,070,851

Claim 4 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,100, issued to Donofrio et al., in view of United States Patent Application No. 2009/0140272, issued to Beeson et al.

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,100, issued to Donofrio et al., in view of United States Patent No. 7,335,517, issued to Hayasaka et al.

Claim 8 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,100, issued to Donofrio et al., in view of Japanese Laid Open Patent Publication No. 2002319704, issued to Takuma et al.

Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,702, issued to Donofrio et al., in view of United States Patent No. 6,838,702, issued to Ho.

Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,702, issued to Donofrio et al., in view of Korea Patent No. 610650, issued to Hwan.

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Claims 9 and 10 are rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 8,368,702, issued to Donofrio et al., in view of Japanese Laid Open Patent Publication No. 11008414, issued to Etsuo.

Claim 6 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of Japan Patent No. 4,151,284, issued to Seichiro et al., in view of United States Patent No. 8,368,100, issued to Donofrio et al.

Claim 6 is rejected as obvious under pre-AIA 35 U.S.C. § 103 in light of United States Patent No. 7,179,670, issued to Shelton et al., in view of United States Patent No. 8,368,100, issued to Donofrio et al.

IV. THE SCOPE AND CONTENT OF THE '851 PATENT

A. Scope and Content of the Disclosure of the '851 Patent

The '851 patent relates to a wafer-level light emitting diode (LED) package and a method of fabricating the same. Exhibit 1, Col. 2, ll. 31-32. According to the '851 patent, the LED package can be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board. *Id.*, Col. 2, ll. 33-34. Moreover, the LED package may have high efficiency and exhibit improved heat dissipation. *Id.*, Col. 2, ll. 36-39.

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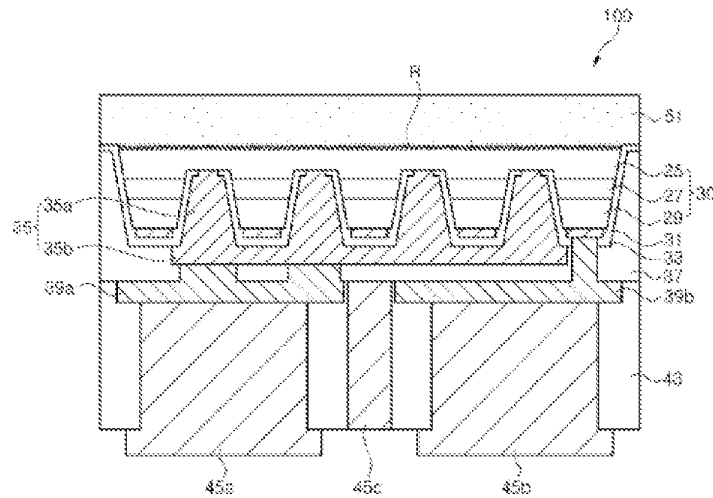
The '851 patent describes what it claims are the shortcomings of prior art LED packages. According to the '851 patent, conventional LED packages, including the lead frame or the circuit board, may not have satisfactory miniaturization or heat dissipation. *Id.*, Col. 1, ll. 61-63. Furthermore, the '851 patent explains that prior art LED packages may have deteriorated luminous efficiency due to absorption of light by the lead frame or the printed circuit board. *Id.*, Col. 1, ll. 63-67.

The '851 patent further describes how alternating current (AC) LEDs, or LEDs directly connected to an AC source, have been produced. As described, the AC-LED elements are arranged in a two-dimensional pattern on a substrate and are connected in series to form LED arrays. *Id.*, Col. 2, ll. 11-14. According to the '851 patent, the AC-LED restricts the structure of the light emitting cells and may limit improvement of the light extraction efficiency since the AC-LED includes light emitting cells on a growth substrate. *Id.*, Col. 2, ll. 21-24.

The '851 patent purports to solve these problems by providing an LED package, and a method of fabrication thereof, which may be formed without using a conventional lead frame or printed circuit board.

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Figure 1



Specifically, as shown in Figure 1 of the '851 patent, shown above, the disclosure describes an LED package 100, which includes a semiconductor stack 30, a first contact layer 35, a second contact layer 31, a first insulation layer 33, a second insulation layer 37, a first electrode pad 39a, a second electrode pad 39b, a first bump 45a, and a second bump 45b. *Id.*, Col. 5, ll. 12-16. The semiconductor stack 30 includes a first conductive type semiconductor layer 25, a second conductive type semiconductor layer 29, and an active layer 27 disposed between the first conductive type and second conductive type semiconductor layers 25, 29. *Id.*, Col. 5, ll. 19-23. The semiconductor stack 30 contains a plurality of contact holes formed through the second conductive type semiconductor layer 29 and the active layer 27 to expose the first conductive type semiconductor layer 25. *Id.*, Col. 5, ll. 43-46. The LED package 100 may further include an insulation layer 43, a dummy bump 45c, and a wavelength converter 51. *Id.*, Col. 5, ll. 16-18.

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B. Scope of the Claims of the '851 Patent

The '851 patent includes two independent device claim and thirteen dependent device claims. Claims 1 and 14 are independent claims. Claims 2-13 depend on Claim 1. Claim 15 depends on Claim 14. Claim 1 of the '851 patent reads as follows:

1. A light emitting diode (LED) package, comprising:

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;

a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes;

a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer;

and

a protective insulation layer covering a sidewall of the semiconductor stack.

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Claim 2 provides that the package includes “a wavelength converter arranged on a second side of the semiconductor stack.” The second side is opposite to the first side of the semiconductor stack. Claim 3 provides that the wavelength converter includes a phosphor sheet or an impurity-doped single crystal substrate. Claim 4 provides the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer. Claim 5 provides the protective insulation layer includes a distributed Bragg reflector. Claim 6 provides the first conductive type semiconductor layer includes a roughened surface. Claim 7 provides that the package includes an insulation layer on the sides of the first and second bumps. Claim 8 provides that the package includes a dummy bump between the first and second bumps. Claim 9 provides that the package includes a substrate, which includes a first through-hole and a second through-hole with the first bump and the second bump being arranged in the first and second through-hole, respectively. Claim 10 provides the substrate is sapphire or silicon.

Claim 11 provides that the package further includes a first contact layer, which includes first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other, and a second contact layer, which contacts the second conductive type semiconductor layer. The protective insulation layer includes a first insulation layer

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arranged between the first contact layer and the second contact layer and covering the second contact layer, and a second insulation layer arranged between the semiconductor stack and the first contact layer and covering the first contact layer. The first bump is electrically connected to the first contact layer and the second bump is electrically connected to the second contact layer. Claim 12 provides that the device further includes a first electrode pad, which contacts the first contact layer through a first contact hole arranged in the second insulation layer, and a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer. The first bump and the second bump contact the first electrode pad and the second electrode pad, respectively. Claim 13 provides that at least one of the first and second insulation layers includes a distributed Bragg reflector.

Claim 14 of the '851 patent reads as follows:

14. A light emitting diode (LED) module, comprising:

a circuit board;

the LED package of claim 1 arranged on the circuit board; and

a lens to adjust an orientation angle of light emitted from the LED package.

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Claim 15 provides that the circuit board includes a metal core printed circuit board (MC-PCB), and a plurality of LED packages is arranged on the MC-PCB.

V. THE PROSECUTION HISTORY OF THE '851 PATENT

United States Patent Application No. 13/194,317 was filed on July 29, 2011, claiming priority to Korean Patent Application Nos. 10-2010-0092807 and 10-2010-009280, filed September 24, 2010. The application listed claims 1-51, which included four independent claims and forty-seven dependent claims.

On May 22, 2014, the Examiner mailed a Restriction and/or Election Requirement, which required restriction of the claims between Group I, claims 1-15 and 25-41, and Group II, claims 16-24 and 42-51, under 35 U.S.C. §§ 121 and 372. The Examiner further required election between Embodiment 1 – Figures 1 and 4-12; Embodiment 2, Figures 2 and 13; Embodiment 3 – Figures 2, 14 and 16-26; and Embodiment 4 – Figures 15 and 17.

On July 15, 2014, Applicants filed a Response to Restriction Requirement and elected Group I, claims 1-15 and 25-41, with traverse.

On October 22, 2014, the Examiner mailed a Notice of Non-Compliant or Non-Responsive Amendment, which stated that Applicants failed to respond to the species restriction

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requirement between Embodiments 1-4. The Examiner stated that the difference between the species is that “the connection structure between the semiconductor stack and the bump are different between the species and these different [*sic*] are not obvious from each other.”

On November 13, 2014, Applicants filed a Response to Notice of Non-Compliant Response and elected Group I and Species 1/Embodiment 1 described in Figures 1 and 4-12 and included in claims 1-15 and 25-41¹, with traverse.

On January 15, 2015, the Examiner mailed an Ex Parte Quayle Action, which stated that claims 1 and 4-15 were allowed, and that non-elected claims 2 and 3 were rejoined and allowed because they depend on claim 1. The Examiner required cancellation of claims 16-41, which were drawn to non-elected species.

On February 11, 2015, Applicants filed a Reply to Ex Parte Quayle Action and canceled claims 16-41.

The Examiner mailed a Notice of Allowance on January 15, 2015. Applicants submitted thirteen information disclosure statements, which included more than forty five references, all of which now appear on the front of the ‘851 patent. The Examiner cited four references and

¹ Applicants stated that they elected claims 1-15 and 25-41, however, they elected Species 1/Embodiment 1, which Examiner asserted to be drawn to claims 1-15. *See* Response dated November 13, 2014 at p. 1.

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asserted that the prior art did not teach or render obvious a LED having an arrangement as claimed such as a “first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.” *See* Notice of Allowance dated January 15, 2015, pp. 2-3.

VI. THE SCOPE AND CONTENT OF THE PRIOR ART

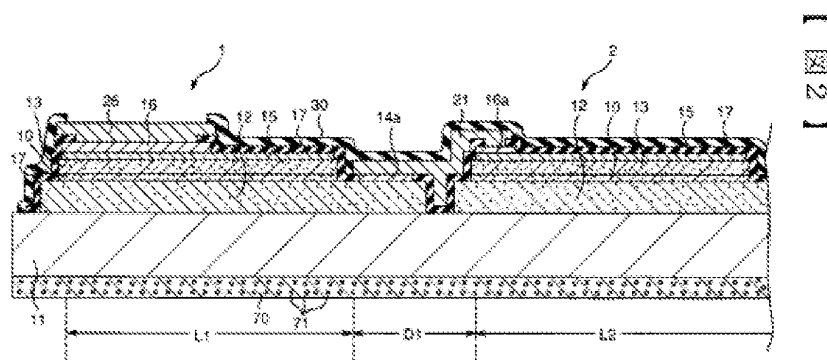
A. Japan Patent No. 4,151,284 to Seiichiro et al. (Exhibit 2)

Seiichiro et al. was published on November 22, 2002. Seiichiro et al. qualifies as prior art to the ‘851 patent under pre-AIA 35 U.S.C. § 102 (a). Seiichiro et al. was not cited or considered by the Examiner during prosecution of the ‘851 patent. Seiichiro et al. is highly relevant prior art that raises a substantial new question of patentability because it teaches all of the elements of claims 1-4, 7, 9 and 11-12 and renders claims 5, 6, 8, 10 and 13-15 obvious, including a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump

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being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack, and considered in conjunction with the other prior art described herein, it renders claims 1-15 of '851 patent anticipated or obvious.

Seiichiro et al. is entitled "Nitride Semiconductor Light Emitting Element," and teaches a nitride semiconductor light emitting element wherein an N-type gallium nitride based compound semiconductor layer and a light emitting layer and a P-type gallium nitride based compound semiconductor layer are formed on one main surface of a translucent substrate and an SiO₂ layer containing phosphor which absorbs a part of the light generated from the light emitting layer and can generate a light whose wavelength is longer than that of the absorbed light formed on the other main surface of the translucent substrate. *See Exhibit 2, Abstract.*



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Figure 2 shows a light emitting device with a p type gallium nitride system semiconductor layer 13, an active layer 10, and a p layer 13. *See* Exhibit 2, Paragraph [0024]. The p side pad electrodes and n side ohmic electrodes may be exposed by RIE. *Id.* at Paragraph [0060]. The LED includes a bonding electrode 21 and an electrode 26 for external connection, which consists of the same material, which are further formed on the p pad electrode 16 of the light emitting device 1, and a bonding electrode 21 and an electrode 24 for external connection which consists of the same material are formed on the n pad electrode 14 of the light emitting device 3. *Id.* at Paragraph [0028]. The LED also includes an insulation protection film 17. *Id.* at Paragraph [0027].

Seiichiro et al. alone anticipates at least claims 1-4, 7, 9, and 11-12 of the '851 patent, and renders claims 5, 6, 8, 10 and 14-15 obvious when combined with other prior art or common knowledge.

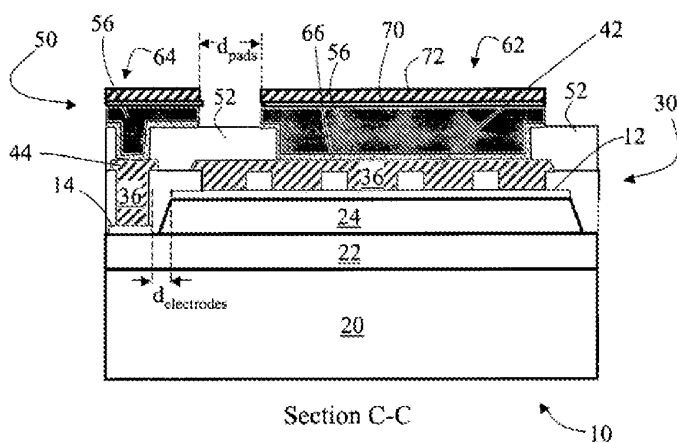
B. United States Patent No. 7,179,670 issued to Shelton et al. (Exhibit 3)

Shelton et al. was filed on March 5, 2004, published on September 8, 2005 and issued on February 20, 2007. Shelton et al. qualifies as prior art to the '851 patent under pre-AIA 35 U.S.C. § 102 (b). Shelton et al. was not cited or considered by the Examiner during prosecution of the '851 patent. Shelton et al. is highly relevant prior art that raises a substantial new question of patentability because it teaches all of the elements of claims 1-4, 7, 11, 12, 14 and 15,

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including a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack, and considered in conjunction with the other prior art described herein, it renders claims 1-15 of '851 patent anticipated or obvious.

Shelton et al. is entitled "Flip-Chip Light Emitting Diode Device Without Sub-mount," and teaches a light emitting diode having a backside and a front-side with at least one n-type electrode and at least one p-type electrode disposed thereon. *See Exhibit 3, Abstract.*



Section C-C

FIG 10

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Figure 10 shows a light emitting device 10, which includes an n-type base layer 22 and second layer, or mesa, 24. *Id.* at Col. 4, ll. 50-53. Shelton et al. states that there is “an active region adjacent the n-type cladding layer” and that there is a p-type cladding layer “adjacent a side of the active region distal from the substrate 20.” *Id.* at Col. 4-5, ll. 65-2. Therefore, it is inherent that the active region is an active layer. The light emitting device 10 further includes vias 34, shown in Figure 4, which provide access to the p-type and n-type electrodes 12, 14. *Id.* at Col. 6, ll. 44-45. A first bump and a second bump of a metallization material 56 are arranged on the first side of the device to form a p-type bonding pad 62 and an n-type bonding pad 64. *Id.* at Col. 8, ll. 5-14. The device 10 further includes a dielectric layer 32. *Id.* at Col. 6, ll. 12-15. The light emitting device 10 may be bonded to a printed circuit board 76, as shown in Figure 12. *Id.* at Col. 9, ll. 18-20.

Shelton et al. alone anticipates at least claims 1-4, 7, 11, 12, 14 and 15 of the ‘851 patent, and renders claims 5, 8-10 and 13 obvious when combined with other prior art or common knowledge.

C. United States Patent No. 8,368,100 issued to Donofrio et al. (Exhibit 4)

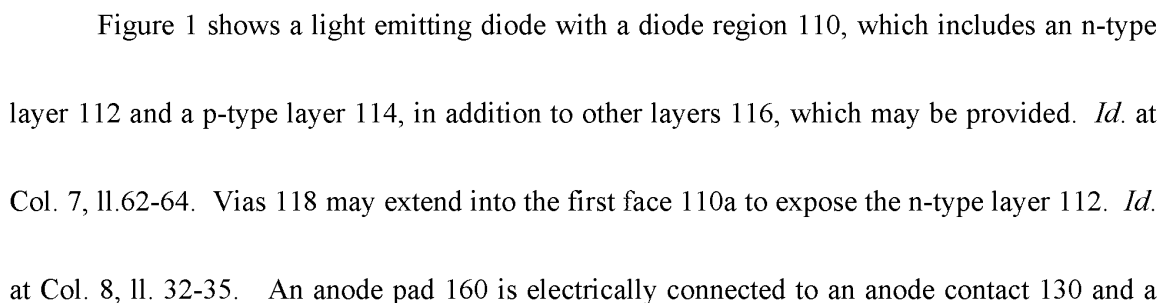
Donofrio et al. was filed on May 11, 2009, published on November 19, 2009 and issued on February 5, 2013. Donofrio et al. claims a priority date of November 14, 2007 based on United States Application No. 11/985,410. Donofrio et al. qualifies as prior art under pre-AIA

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35 U.S.C. § 102 (e). Although the publication of Donofrio et al. was cited by the Applicant in an information disclosure statement during prosecution of the '851 patent, no evidence exists that the Examiner considered any of the technical teachings of Donofrio et al. to a greater degree than documents are generally considered during a search of Office file records. 35 U.S.C. § 303 provides, "[t]he existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office." Donofrio et al. is highly relevant prior art that raises a substantial new question of patentability because it teaches all of the elements of claims 1-3, 5-7 and 11-15, including a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack, and considered in conjunction with the other prior art described herein, it renders claims 1-15 of '851 patent anticipated or obvious.

Donofrio et al. is entitled "Semiconductor Light Emitting Diodes Having Reflective Structures and Methods of Fabricating the Same," and teaches light emitting diodes, which include a diode region having first and second opposing faces that include therein an n-type layer and a p-type layer, an anode contact that ohmically contacts the p-type layer and extends on the

first face, and a cathode contact that ohmically contacts the n-type layer and also extends on the first face. *See* Exhibit 4, Abstract. The anode contact and/or the cathode contact may further provide a hybrid reflective structure on the first face that is configured to reflect substantially all light that emerges from the first face back into the first face. Related fabrication methods are also described. *Id.*



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cathode pad 170 is electrically connected to a reflective cathode contact 150. *Id.* at Col. 8, ll. 39-42. The light emitting diode further includes a protective insulation layer 140. *Id.* at Col. 8, ll. 10-11. The anode pad 160 and the cathode pad 170 may be mounted onto a supporting substrate, such as a printed circuit board. *Id.* at Col. 9, ll. 15-19.

Donofrio et al. alone anticipates at least claims 1-3, 5-7 and 11-15 of the '851 patent, and renders claims 4 and 8-10 obvious when combined with other prior art or common knowledge.

D. United States Patent No. 7,564,887 issued to Wang et al. (Exhibit 5)

Wang et al. was filed on February 25, 2005, published on January 5, 2006 and issued on July 21, 2009. It claims a priority date of June 30, 2004 based on United States Provisional Application No. 60/583,980. Wang et al. qualifies as prior art to the '851 patent under pre-AIA 35 U.S.C. § 102(b). Wang et al. was not cited or considered by the Examiner during prosecution of the '851 patent. Wang et al. is highly relevant prior art that raises a substantial new question of patentability because together with Seichiro et al., Shelton et al., or Donofrio et al., it teaches all of the limitations of claims 5 and 13, including an insulation layer that includes a distributed Bragg reflector.

Wang et al. is entitled "Long Wavelength Vertical Cavity Surface Emitting Lasers," and teaches a vertical cavity surface emitting laser, the optical guide for which may be formed from an upper distributed Bragg reflector. *See* Exhibit 5, Abstract and Col. 9, ll. 51-55. When

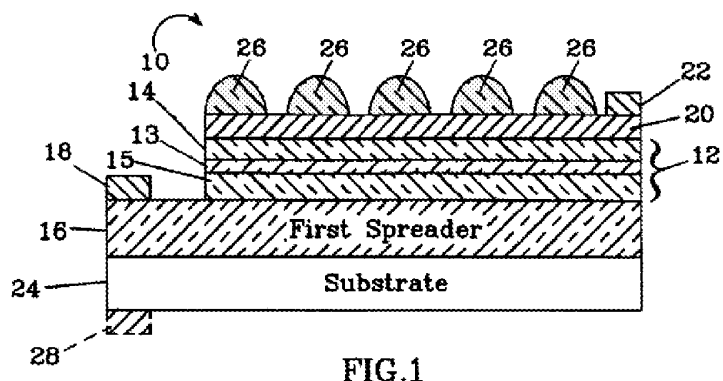
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considered with the other prior art discussed herein, Wang et al. renders claims 5 and 13 of the ‘851 patent obvious.

E. United States Patent No. 6,657,236 issued to Thibeault et al. (Exhibit 6)

Thibeault et al. was filed on November 28, 2000, published on December 2, 2003 and issued on July 21, 2009. It claims a priority date of December 3, 1999 based on United States Provisional Application No. 60/168,817. Thibeault et al. qualifies as prior art to the ‘851 patent under pre-AIA 35 U.S.C. § 102(b). Thibeault et al. was not cited or considered by the Examiner during prosecution of the ‘851 patent. Thibeault et al. is highly relevant prior art that raises a substantial new question of patentability because together with Seichiro et al., Shelton et al., or Donofrio et al., it teaches all of the limitations of claim 6, including that the first conductive type semiconductor layer may have a roughened surface.

Thibeault et al. is entitled, “Enhanced Light Extraction in LEDs through the Use of Internal and External Optical Elements,” and teaches LED structures which provide surface for reflecting, refracting or scattering light. *See* Exhibit 6, Abstract. The LED structures may have a first and second spreader layer, which are semiconducting or conducting layers that are spread across the device to effectively inject current into the active layer. *Id.* at Col. 3, ll. 59-64.



As shown in Figure 1, the second spreader layer 20 may have an array of light extracting elements 26 formed on the surface thereof so as to roughen the surface and allow otherwise trapped TIR light to pass through. *Id.* at Col. 5, ll. 57-61. When considered with the other prior art discussed herein, Thibeault et al. renders claim 6 of the '851 patent obvious.

F. United States Patent No. 7,335,517 issued to Hayasaka et al. (Exhibit 7)

Hayasaka et al. was filed on July 30, 2004, published on January 20, 2005 and issued on February 26, 2008. It claims a priority date of December 1, 1997 based on United States Application No. 08/980,873. Hayasaka et al. qualifies as prior art to the '851 patent under pre-AIA 35 U.S.C. § 102(b). Hayasaka et al. was not cited or considered by the Examiner during prosecution of the '851 patent. Hayasaka et al. is highly relevant prior art that raises a substantial new question of patentability because together with Seiichiro et al., Shelton et al., or

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Donofrio et al., it teaches all of the limitations of claim 8, including a dummy bump between the first bump and the second bump.

Hayasaka et al. is entitled “Multichip Semiconductor Device, Chip Therefor and Method of Fabrication Thereof,” and teaches a multichip semiconductor device in which chips are stacked, each chip having a semiconductor substrate formed on top with circuit components and an interlayer insulating film formed on the top of the semiconductor substrate. *See* Exhibit 7, Abstract. One chip has a connect plug of a metal formed in a through hole that passes through the substrate and interlayer film and electrically connects with another chip. *Id.* An embodiment of the semiconductor device can include a heat radiation dummy bump 8d between chips 1a and 1b, which may be formed of metal. *Id.* at Col. 18, ll. 41-47. When considered with the other prior art discussed herein, Hayasaka et al. renders claim 8 of the ‘851 patent obvious.

G. Japanese Laid Open Patent Publication No. 2002319704 to Takuma et al. (Exhibit 8)

Takuma et al. was published on October 31, 2002. Takuma et al. qualifies as prior art to the ‘851 patent under pre-AIA 35 U.S.C. § 102(b). Takuma et al. was not cited or considered by the Examiner during prosecution of the ‘851 patent. Takuma et al. is highly relevant prior art that raises a substantial new question of patentability because together with Seiichiro et al.,

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Shelton et al., or Donofrio et al., it teaches all of the limitations of claim 8, including a dummy bump between the first bump and the second bump.

Takuma et al. is entitled “LED Chip,” and teaches an LED chip with p- and n-type semiconductor layers formed on a substrate and p- and n-side electrodes respectively provided in the p- and n-type semiconductor layers on the main surface of the chip opposite to the substrate. *See* Exhibit 8, Abstract. The electrodes on the main surface of the chip have straight line sections, which are parallel to each other, and are alternately arranged in the direction traversing the straight line sections. *Id.* Because of this configuration, offset of current density distribution becomes smaller and the luminance unevenness of the chip is reduced. *Id.* A filler 11 is disposed between the p lateral electrode and the n-lateral electrode. *Id.* at Paragraph [0054]. When considered with the other prior art discussed herein, Takuma et al. renders claim 8 of the ‘851 patent obvious.

H. United States Patent No. 6,838,702 issued to Ho. (Exhibit 9)

Ho was filed on October 10, 2003 and issued on January 4, 2005. Ho qualifies as prior art to the ‘851 patent under pre-AIA 35 U.S.C. § 102(b). Ho was not cited or considered by the Examiner during prosecution of the ‘851 patent. Ho is highly relevant prior art that raises a substantial new question of patentability because together with Seichiro et al., Shelton et al., or

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Donofrio et al., it teaches all of the limitations of claims 9 and 10, including an LED package with a substrate having first and second through holes, the first bump being arranged in the first through-hole and the second bump being arranged in the second through-hole, and a ceramic substrate.

Ho is entitled “Light Emitting Diode,” and teaches a light emitting chip with heat dissipating structure, which includes an epitaxy chip and electrodes and uses insulation material with good heat-dissipation to form the substrate of the emission layer. *See* Exhibit 9, Abstract. The substrate has a plurality of openings filled with conducting metals, which results in better heat conductivity and dissipation rates. *Id.*

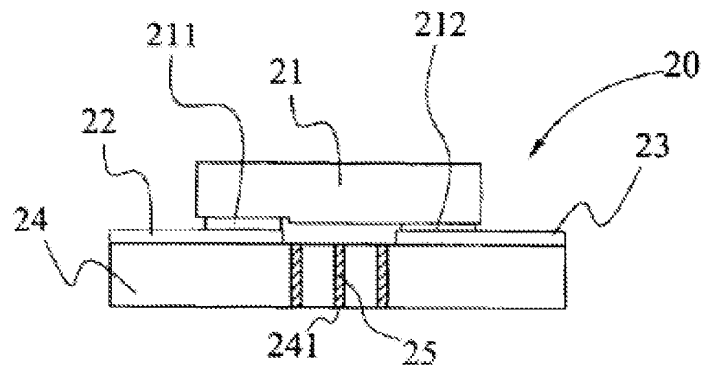


FIG.2

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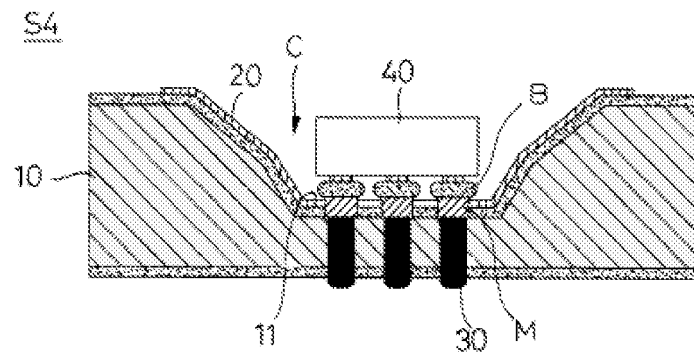
As shown in Figure 2, the heat dissipating substrate 24 has several openings 241, which are filled with metals. *Id.* at Col. 3, ll. 23-26. The heat dissipating substrate 24 may be a ceramic substrate. *Id.* at Col. 2, ll. 11-15. Silicon and sapphire are examples of ceramics, which may be used to form a heat dissipating substrate. When considered with the other prior art discussed herein, Ho renders claims 9 and 10 of the '851 patent obvious.

I. Korea Patent No. 610650 to Hwan. (Exhibit 10)

Hwan was published on August 9, 2006. Hwan qualifies as prior art to the '851 patent under pre-AIA 35 U.S.C. § 102(b). Hwan was not cited or considered by the Examiner during prosecution of the '851 patent. Hwan is highly relevant prior art that raises a substantial new question of patentability because together with Seiichiro et al., Shelton et al., or Donofrio et al., it teaches all of the limitations of claims 9 and 10, including an LED package with a substrate having first and second through holes, the first bump being arranged in the first through-hole and the second bump being arranged in the second through-hole, and a silicon substrate.

Hwan is entitled "LED Package Capable of Minimizing Size Using Substrate as Dual Application and Manufacturing Method Thereof," and teaches a silicon substrate which includes a silicon substrate for an LED. *See* Exhibit 10, Abstract. A plurality of holes is formed through the silicon substrate. *Id.*

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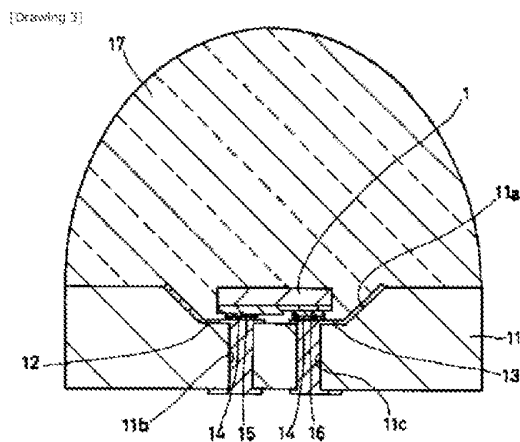
As shown in the representative figure of Ho, which is shown above, the silicon substrate 10 has a plurality of holes therethrough. The holes are filled with metal plugs 30. *Id.* When considered with the other prior art discussed herein, Ho renders claims 9 and 10 of the '851 patent obvious.

J. Japanese Laid Open Patent Publication No. 11008414 to Etsuo. (Exhibit 11)

Etsuo was published on January 12, 1999. Etsuo qualifies as prior art to the '851 patent under pre-AIA 35 U.S.C. § 102(b). Etsuo was not cited or considered by the Examiner during prosecution of the '851 patent. Etsuo is highly relevant prior art that raises a substantial new question of patentability because together with Seiichiro et al., Shelton et al., or Donofrio et al., it teaches all of the limitations of claims 9 and 10, including an LED package with a substrate having first and second through holes, the first bump being arranged in the first through-hole and the second bump being arranged in the second through-hole.

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Etsuo is entitled “Semiconductor Device and Semiconductor Light-Emitting Device.” As shown in Figure 3, below, Etsuo teaches a light emitting diode with through holes 11b and 11c through the substrate 11. *Id.* at Paragraph [0038]. The through holes are directly under bumps 15 and 16. The substrate 11 may be a ceramic board such as an alumina substrate. *Id.* at Paragraph [0027].



When considered with the other prior art discussed herein, Etsuo renders claims 9 and 10 of the ‘851 patent obvious.

K. United States Patent Application Publication No. 2009/0140272 to Beeson et al. (Exhibit 12)

Beeson et al. was filed on December 3, 2008 and published on June 4, 2009. It claims a priority date of December 3, 2007 based on United States Provisional Application No. 61/005,258. Beeson et al. qualifies as prior art to the ‘851 patent under pre-AIA 35 U.S.C. §

102(b). Beeson et al. was not cited or considered by the Examiner during prosecution of the '851 patent. Beeson et al. is highly relevant prior art that raises a substantial new question of patentability because together with Seichiro et al., Shelton et al., or Donofrio et al., it teaches all of the limitations of claim 4, including a wavelength converter having a side surface flush with a side surface of the protective insulation layer.

As shown in Figure 30, the wavelength conversion layer 1302 has a surface in contact with a surface of the dichroic layer 1502. Claim 4 of the '851 patent simply request “a side surface” of a wavelength converter to be flush with “a side surface” of a protective insulating

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layer. As clearly shown in Figure 30, a surface of the wavelength conversion layer 1302 (*i.e.*, wavelength converter) is in contact with a surface of the dichroic layer 1502 (*i.e.*, protective insulating layer). Hence, when considered with the other prior art discussed herein, Beeson et al. renders claim 4 of the '851 patent obvious.

VII. CLAIMS 1-7 AND 11-15 OF THE '851 PATENT ARE ANTICIPATED BY THE PRIOR ART

Invalidity based on a lack of novelty ("anticipation") requires that the same invention, including each element and limitation of the claims, was known or used by others before it was invented by the patentee. *See Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 299; 36 USPQ2d 1101 (Fed. Cir. 1995). Novelty of a claim is judged by a simple comparison of the literal language of the scrutinized claim with a single piece of prior art. *See Lindemann Maschinenfabrik v. American Hoist & Derrick*, 730 F.2d 1452, 1458; 221 USPQ 481 (Fed. Cir. 1984). Anticipation requires just a single, complete disclosure of the invention in the reference. A reference anticipates a claim if it discloses the claimed invention "such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention." *See In re Graves*, 69 F.3d 1147, 1152; 36 USPQ2d 1697 (Fed. Cir. 1995) (citing *In re LeGrice*, 301 F.2d 929, 936, 133 USPQ 365, 372 (CCPA 1962)); *In re Donohue*, 766 F.2d 531, 533; 226 USPQ 619, 621 (Fed. Cir. 1985). A claim lacks novelty, and

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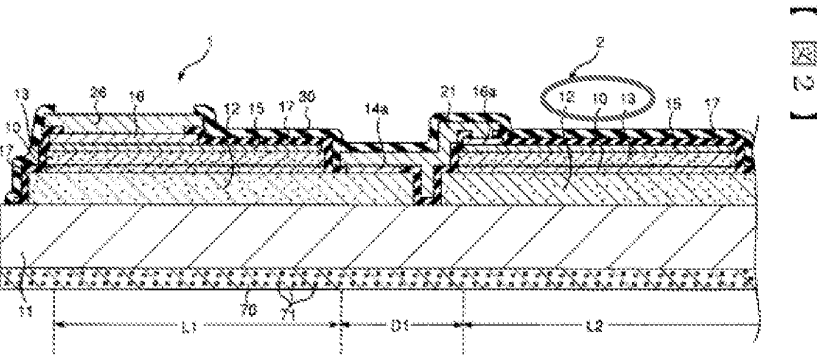
is thus not valid under 35 U.S.C. § 102, if every feature of that claim is found, either expressly or under principles of inherency, in a single prior art reference or document. *See Elmer v. ICC Fabricating, Inc.*, 67 F.3d 1571; 36 USPQ2d 1417 (Fed. Cir. 1995).

VIII. SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY UNDER § 102

SNQP Statement No. 1: Whether Seiichiro et al. anticipates claims 1-4, 7, 9 and 11-12 of the ‘851 patent.

As detailed in Claim Chart 1, Japan Patent No. 4,151,284 to Seiichiro et al. (Exhibit 2) anticipates claims 1-4, 7, 9 and 11-12 of the ‘851 patent.

Claim Chart 1

U.S. PATENT NO. 9,070,851 CLAIM	JAPAN PATENT NO. 4,151,284 SEIICHIRO ET AL.
1. A light emitting diode (LED) package, comprising: a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;	Seiichiro et al. states that the present invention provides “a possible light emitting diode” at Exhibit 2, Paragraph [0004].  Figure 2 of Seiichiro et al. shows a semiconductor stack comprising a first conductive type (i.e., an n type) semiconductor layer 12, an active layer 10, and a second conductive type (i.e., p type) semiconductor

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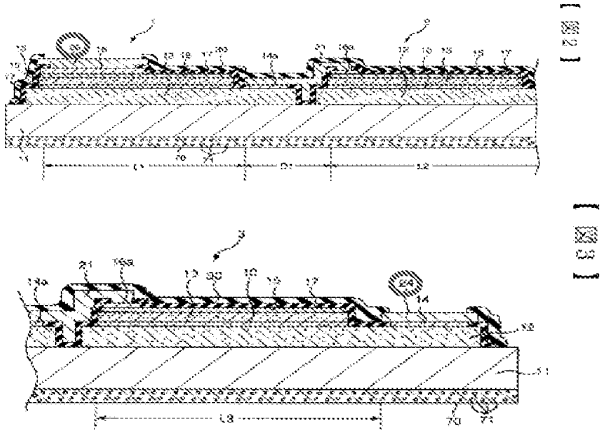
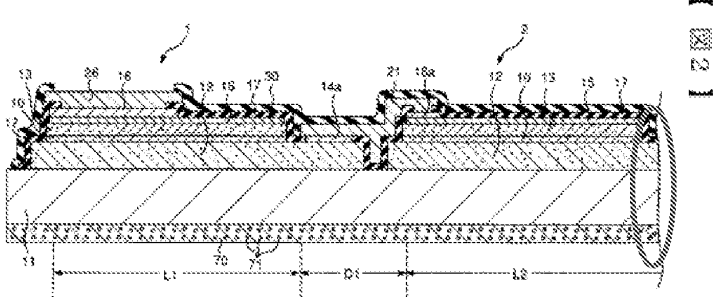
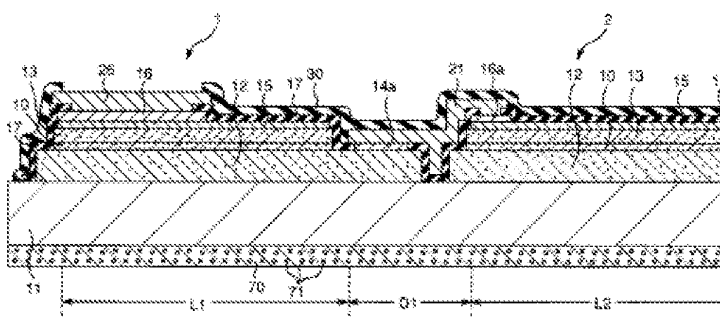
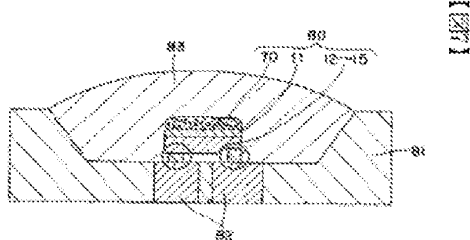
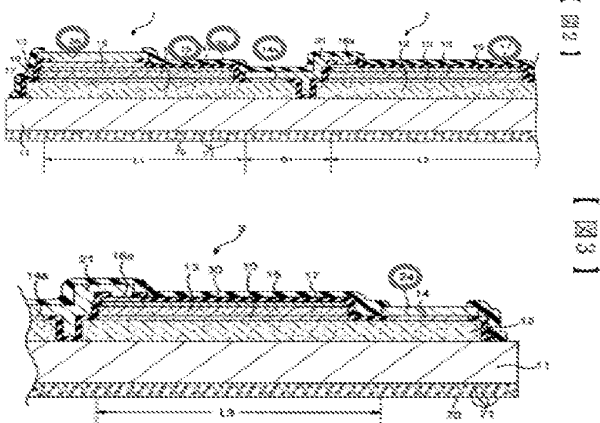
	layer 13. <i>Id.</i> at Paragraphs [0021]-[0024].
a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;	Seiichiro et al. discloses a plurality of contact holes arranged in the second conductive type semiconductor layer 13 and the active layer 10 that expose the first conductive type semiconductor layer 12 because some of the p side pad electrodes and n side ohmic electrodes are exposed by reactive ion etching (RIE) at Paragraph [0060].
a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and	 Figures 2 and 3 of Seiichiro et al. show a first bump (i.e., electrode) 26 arranged on a first side of the semiconductor stack, which is electrically connected to the first conductive type semiconductor layer 12 through the plurality of contact holes and a second bump (i.e., electrode) 24 arranged on the first side of the semiconductor stack, which is electrically connected to the second conductive type semiconductor layer 13. <i>Id.</i> at Paragraph [0028].
a protective insulation layer covering a sidewall of the semiconductor stack.	

	Figure 2 of Seichiro et al. shows a protective insulation layer (i.e., insulation protection film) 17 and a protective insulation layer (i.e., insulation protection film) 30, each of which is formed to cover the whole element, including a sidewall of the semiconductor stack. <i>Id.</i> at Paragraphs [0027] and [0030].
2. The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.	Figure 2 of Seichiro shows a wavelength converter (i.e., fluorescent substance) 71. The wavelength converter is disposed on a second side of the semiconductor stack. The second side is opposite to the first side. <i>Id.</i> at Paragraphs [0011] and [0014].
3. The LED package of claim 2, wherein the wavelength converter comprises a phosphor	The wavelength converter may (1) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$, Re' (however, Re with at least 1 type chosen from Mg, Ca, Ba, Sr, and Zn) At least 1 type as which Q is chosen from F of a halogen, Cl, Br, and I, and Re' have at least 1 type chosen from Mn, Fe, Cr, and Sn (white).

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sheet or an impurity-doped crystal substrate.	(2) $\text{Re}_5(\text{PO}_4)_3\text{Q}:\text{Eu}$ (however, at least 1 type as which Re is chosen from Sr, Ca, Ba, and Mg, and Q have at least 1 type chosen from F of a halogen, Cl, Br, and I.) (blue), (3) $\text{BaMg}_2\text{Al}_6\text{O}_{27}:\text{Eu}$ (blue), (4) $\text{BaMg}_2\text{Al}_6\text{O}_{27}:\text{Eu, Mn}$ (green), (5) $(\text{SrEu})\text{O} \cdot \text{Al}_2\text{O}_3$ (green), (6) 3.5MgO and $0.5\text{MgF}_2^{**}\text{GeO}_2:\text{Mn}$ (red), (7) $\text{Y}_2\text{O}_2\text{S}:\text{Eu}$ (red), (8) $\text{Mg}_6\text{As}_2\text{O}_{11}:\text{Mn}$ (red), (9) $\text{Gd}_2\text{O}_2\text{S}:\text{Eu}$ (red) -- and (10) $\text{La}_2\text{O}_2\text{S}:\text{Eu}$ (red), which are phosphors, or impurity-doped crystal substrates, as shown by the notations such as ".Eu." <i>Id.</i> at Paragraph [0014].
4. The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.	 Figure 2 shows the wavelength converter has a side surface flush with a side surface of the protective insulation layer 17 or the protective insulation layer 30.
7. The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.	 Figure 2 of Seiichiro et al. shows an insulation layer (i.e., insulation protection film) 17 and an insulation layer (i.e., insulation protection film) 30, each of which is formed to cover the whole element, including side surfaces of the first and second bumps 24, 26. <i>Id.</i> at Paragraphs [0027] and [0030].

9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 Figure 7 of Seiichiro et al. shows a substrate 81 comprises a first through-hole and a second through-hole 82, the first bump and the second bump (red circles enclosed above) are arranged in the first through-hole and the second through-hole 82, respectively.
11. The LED package of claim 1, further comprising: a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and a second contact layer contacting the second conductive type semiconductor layer, wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the	 Figures 2 and 3 of Seiichiro et al. show a first contact layer (i.e., p side electrode) 15 having first contact sections which contact the first conductive type semiconductor layer 12 in the plurality of contact holes, and a second contact layer (i.e., n side electrode) 14, which contacts the second conductive type semiconductor layer 12. The device also includes a first insulation layer 17 and a second insulation layer 30. The first insulation layer 17 is between the first contact layer 15 and the second contact layer 14, and the second insulation layer 30 is between the semiconductor stack and the first contact layer 15 and covers the first contact layer 15. The first bump 26 is electrically connected to the first contact layer 15 and the second bump 24 is electrically connected to the second contact layer 14. <i>Id.</i> at Paragraphs [0026], [0027] and [0060].

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first contact layer, wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.	
12. The LED package of claim 11, further comprising: a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer, wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.	Figures 2 and 3 of Seichiro et al. show a first electrode pad (i.e., p pad electrode) 16, which contacts the first contact layer through a first contact hole in the second insulation layer and a second electrode pad (i.e., p pad electrode) 14a, which contacts the second contact layer through a second hole in the second insulation layer. The first bump 26 and the second bump 24 contact the first electrode pad 16 and the second electrode pad 14a, respectively. <i>Id.</i> at Paragraphs [0027], [0028] and [0060].

For the foregoing reasons, Seichiro et al. anticipates claims 1-4, 7, 9, and 11-12 of the ‘851 patent.

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SNQP Statement No. 2: Whether Shelton et al. anticipates claims 1-4, 7, 11-12, and 14-15 of the '851 patent.

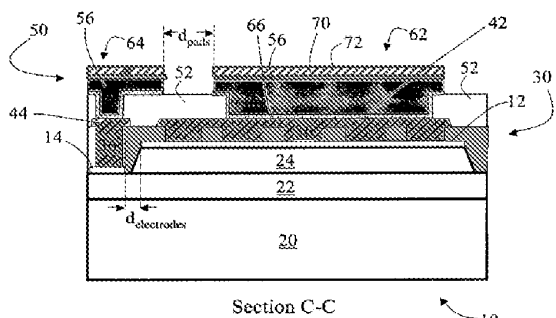
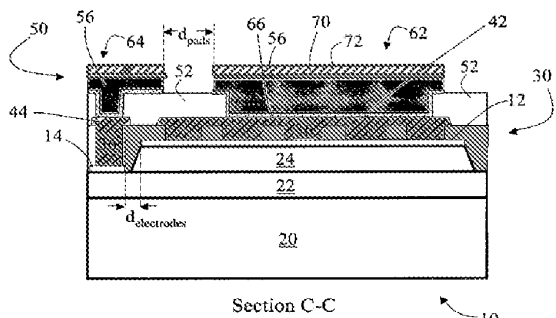
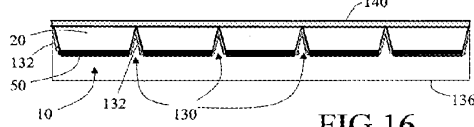
As detailed in Claim Chart 2, United States Patent No. to Shelton et al. (Exhibit 3)

anticipates claims 1-4, 7, 11-12, and 14-15 of the '851 patent.

Claim Chart 2

U.S. PATENT NO. 9,070,851 CLAIM	U.S. PATENT NO. 7,179,670 SHELTON ET AL.
1. A light emitting diode (LED) package, comprising: a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;	Shelton et al. discloses a light emitting diode. <i>See</i> Exhibit 3, Abstract. Section A-A FIG 2 Figure 2 of Shelton et al. shows a light emitting diode 10 with a first conductive type (i.e., n-type base) layer 22, a second conductive type semiconductor layer (i.e., mesa) 24, and an active region (i.e., a portion of the mesa 24). <i>Id.</i> at Col. 4, ll. 50-67, Col. 5, ll. 33-36.
a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;	FIG 4 FIG 5 Figures 4 and 5 of Shelton et al. show a plurality of contact holes (i.e., vias) 34 arranged in the second conductive type semiconductor layer 24 and the active layer, which expose the first conductive type semiconductor layer 22 and provide access to the p-type and n-type electrodes 12, 14. <i>Id.</i> at Col.

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a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and	6, ll. 44-45.  Section C-C FIG 10 Figure 10 of Shelton et al. shows a first bump (i.e., metallization material) 56 extending through the opening in dielectric material 52 and electrically connected to the first conductive type semiconductor material 22, and a second bump (i.e., metallization material) 56, which extends through the opening in the dielectric material and electrically connected to the second conductive type semiconductor material 24. <i>Id.</i> at Col. 8, ll. 8-14.
a protective insulation layer covering a sidewall of the semiconductor stack.	 Section C-C FIG 10 Figure 10 of Shelton et al. shows a protective insulation layer (i.e., dielectric material) 32 covering a sidewall of the semiconductor stack. <i>Id.</i> at Col. 6, ll. 20-22.
2. The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.	 FIG 16 Figure 16 of Shelton et al. shows a wavelength converter (i.e., phosphor coating) 140, which is arranged on a second side of the semiconductor stack opposite to the first side of the semiconductor stack. The wavelength converter 140 provides a selected light conversion. <i>Id.</i> at Col. 11, ll. 63-67.

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3. The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped crystal substrate.	The wavelength converter 140, which provides selected light conversion, is a phosphor sheet. <i>Id.</i>
4. The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.	FIG 16 As would be shown if Figures 10 and 16 of Shelton et al. were combined, the wavelength converter 140 has a side surface that is flush with a side surface of the protective insulation layer 32.
7. The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.	Section C-C FIG 10 Figure 10 of Shelton et al. shows an insulation layer 52, which is arranged on the side surfaces of the first bump 56 and the second bump 56. <i>Id.</i> at Col. 8, ll. 5-6.
11. The LED package of claim 1, further comprising: a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and a second contact layer contacting the second conductive type semiconductor layer, wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer	Section C-C FIG 10 Figure 10 of Shelton et al. shows a first contact layer (i.e., n-

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being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer, wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.	type electrode) 14, which contacts the first conductive type semiconductor layer 22 through the holes 34 formed through the second conductive type semiconductor layer 24, and a second contact layer (i.e., p-type electrode) 12, which contacts the second conductive type semiconductor layer 24. A first insulation layer 32 is arranged between the first contact layer 14 and the second contact layer 12 and covering the second contact layer 12. A second insulation layer 52 is arranged between the semiconductor stack and the first contact layer 14. The first bump 56 is connected to the first contact layer 14 and the second bump 56 is connected to the second contact layer 12. <i>Id.</i> at Col. 6, ll. 12-19, Col. 8, ll. 5-6.
12. The LED package of claim 11, further comprising: a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer, wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.	Section C-C FIG 10 Figure 10 of Shelton et al. shows a first electrode pad (i.e., n-type connecting pad) 44, which contacts the first contact layer 14, and a second electrode pad (i.e., p-type connecting pad) 42, which contacts the second contact layer 12. The first bump 56 contacts the first electrode pad 44 and the second bump 56 contacts the second electrode pad 42. <i>Id.</i> at Col. 6, ll. 12-19.
14. A light emitting diode (LED) module, comprising: a circuit board; the LED package of claim 1 arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.	FIG 12

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	Figure 12 of Shelton et al. shows the light emitting diode 10 bonded to a circuit board 76. <i>Id.</i> at Col. 9, ll. 18-22.
15. The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.	The printed circuit board has at least positive and negative power traces 80, 82, on which bonding bumps 86 are disposed. The bonding bumps 86 may be metal such as copper, gold, silver, or the like.

For the foregoing reasons, Shelton et al. anticipates claims 1-4, 7, 11-12 and 14-15 of the ‘851 patent.

SNQP Statement No. 3: Whether Donofrio et al. anticipates claims 1-3, 5-7 and 11-15 of the ‘851 patent.

As detailed in Claim Chart 3, United States Patent No. 8,368,100 to Donofrio et al. (Exhibit 4) anticipates claims 1-3, 5-7 and 11-15 of the '851 patent.

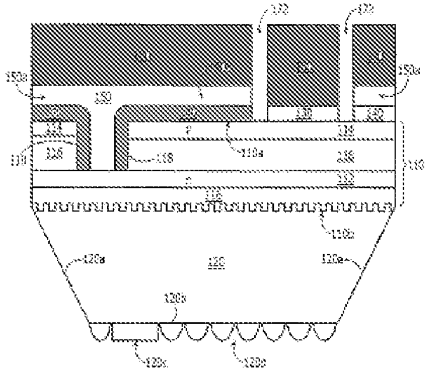
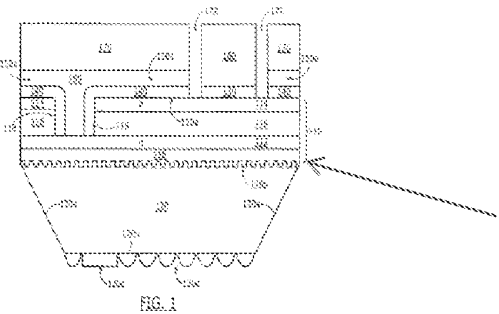
Claim Chart 3

[illegible]

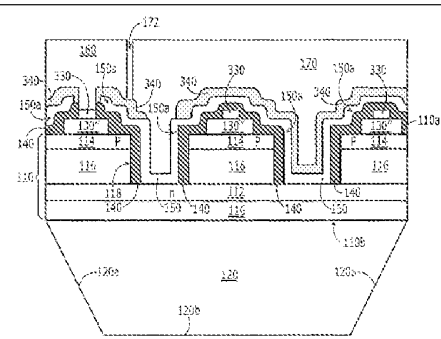
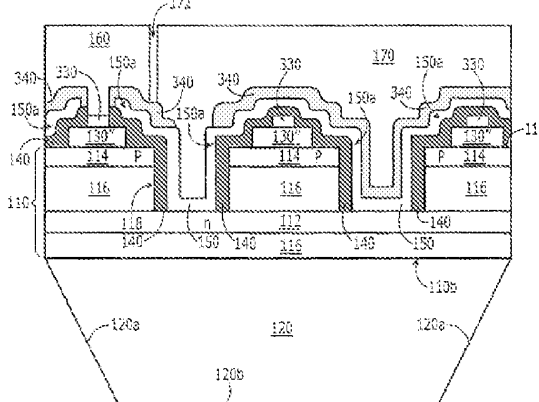
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	includes a first conductive type semiconductor layer (i.e., n-type layer) 112 and a second conductive type semiconductor layer (i.e., p-type layer) 114. The diode region 110 may have an active layer (i.e., additional layer) 116, which may include quantum wells, buffer layers, etc. <i>Id.</i> Col. 7, ll. 58-64.
a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;	FIG. 1 Figure 1 of Donofrio et al. shows a plurality of contact holes (i.e., vias) 118, arranged in the second conductive type semiconductor layer and the active layer 116, which expose the first conductive type semiconductor layer 112. <i>Id.</i> Col. 8, ll. 32-35.
a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and	FIG. 1 Figure 1 of Donofrio et al. shows a first bump (i.e., anode pad) 170 on a first side of the semiconductor stack that is electrically connected to the first type semiconductor layer 112 through the holes 118, and a second bump (i.e., cathode pad) 160 that is electrically connected to the second conductive type semiconductor layer 114. <i>Id.</i> Col. 8, ll. 8-17.

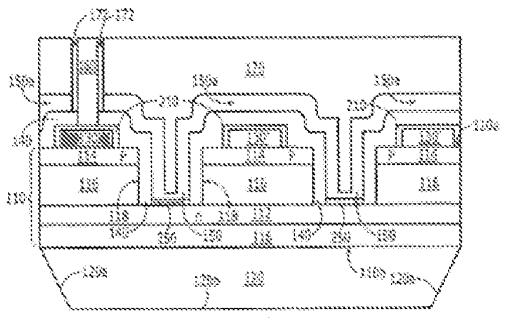
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a protective insulation layer covering a sidewall of the semiconductor stack.	 FIG. 1 Figure 1 of Donofrio et al. shows a protective insulation layer (i.e., transparent insulating layer) 140 covering a sidewall of the semiconductor stack. <i>Id.</i> Col. 8, ll. 10-11.
2. The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.	Donofrio et al. discloses that the LED may incorporate a wavelength converter (i.e., wavelength conversion material). <i>Id.</i> Col. 1, ll. 46-47.
3. The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped crystal substrate.	Donofrio et al. discloses that the wavelength converter may be a phosphor sheet. <i>Id.</i> Col. 1, ll. 46-47.
5. The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.	Donofrio et al. discloses that the protective insulation layer 140 may comprise a distributed Bragg reflector. <i>Id.</i> Col. 8, ll. 26-30.
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.	 FIG. 1 Donofrio et al. discloses that the first conductive type semiconductor layer 112 may have a roughened surface. Figure 1 shows that the interface between the sapphire substrate 120 and the diode region 110 may

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	be textured, as shown by the jagged line. <i>Id.</i> Col. 9, ll. 4-9.
7. The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.	 FIG. 3 Figure 3 of Donofrio et al. shows an insulation layer (i.e., insulating layer) 340 arranged on the side surface of the first bump 170 and the second bump 160 to prevent the first and second bumps 170, 160 from short circuiting one another. <i>Id.</i> Col. 15, ll. 40-41.
11. The LED package of claim 1, further comprising: a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and a second contact layer contacting the second conductive type semiconductor layer, wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer, wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.	 FIG. 3 Figure 3 of Donofrio et al. shows a first contact layer (i.e., reflective cathode contact) 150, which contacts the first conductive type semiconductor layer 112 through the holes 118 and a second contact layer (i.e., anode contact) 130, which contacts the second conductive type semiconductor layer. The first insulation layer 140 is between the first contact layer 150 and the second contact layer 130 and covers the second contact layer 130. The second insulation layer 340 is between the semiconductor stack and the first contact layer 150 and covers the first contact layer 150. The first bump 170 contacts the first contact layer 150 and the second bump 160 contacts the second contact layer 130. <i>Id.</i> Col. 14, ll. 40-44,

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	Col. 16, ll. 30-31, Col. 15, ll. 40-41.
12. The LED package of claim 11, further comprising: a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer, wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.	 Figure 2 of Donofrio et al. shows a first electrode pad (i.e., ohmic contact layer) 250, contacting the first contact layer 150, and a second electrode pad (i.e., barrier layer) 210 contacting the second contact layer 130. The first bump 170 and the second bump 160 contact the first electrode pad 250 and second electrode pad 210, respectively. <i>Id.</i> Col. 8, ll. 26-30.
13. The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.	Donofrio discloses that the first insulation layer 140 may comprise a distributed Bragg reflector. <i>Id.</i> Col. 12, ll. 54-57, Col. 13, ll. 27-29.
14. A light emitting diode (LED) module, comprising: a circuit board; the LED package of claim 1 arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.	Donofrio et al. discloses that the first bump 170 and the second bump 160 may be mounted on a circuit board or wiring board, and microlenses may be provided. <i>Id.</i> at Col. 9, ll. 15-20, ll. 41-43.
15. The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.	Donofrio et al. discloses that the circuit board may be a wiring board. <i>Id.</i> at Col. 9, ll. 15-20.

For the foregoing reasons, Donofrio et al. anticipates claims 1-3, 5-7 and 11-15 of the

‘851 patent.

IX. CLAIMS 4-6, 8-10 AND 14-15 OF THE '851 PATENT ARE OBVIOUS

A claimed invention is unpatentable if the differences between the claimed invention and the prior art “are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *See* 35 U.S.C. § 103(a) (1994); *Graham v. John Deere Co.*, 383 U.S. 1, 13-14 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of secondary considerations of nonobviousness. *See Graham*, 383 U.S. at 17-18; *Miles Labs., Inc. v. Shandon Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993). Even if a single prior art reference does not disclose each and every limitation of the claimed invention, the claim may still be invalid as obvious under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *SIBIA Neurosciences, Inc. v. Cadus Pharmaceutical Corp.*, 225 F.3d 1349, 1355 (Fed. Cir. 2000). In some situations, obviousness can be predicated on a single reference. *See Cornell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983) (“anticipation is the epitome of obviousness”).

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A determination of obviousness requires an “expansive and flexible approach.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit’s rigid application of the “teaching/suggestion/motivation test” as the test for obviousness, making it clear that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.*

According to the Supreme Court:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 417. Thus, the question is “whether the improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 418. Obviousness is based on underlying factual inquiries regarding “the scope and content of the prior art, the level of ordinary skill in the field of the invention, the differences between the claimed invention and the prior art, and any objective evidence of non-obviousness such as long-felt need, and commercial success.” *Id.* (referring to the “*Graham* factors” as recited in *Graham v. John Deere*, 383 U.S. 1, 17 (1966)).

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MPEP § 2141 provides:

Exemplary rationales that may support a conclusion of obviousness include: (A) Combining prior art elements according to known methods to yield predictable results; (B) Simple substitution of one known element for another to obtain predictable results; (C) Use of known technique to improve similar devices (methods, or products) in the same way; (D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (E) “Obvious to try”- choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; (G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

See also MPEP § 2143.

X. SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY UNDER § 103

SNQP Statement No. 4: Whether claims 5 and 13 of the ‘851 patent are obvious in light of Seiichiro et al. in view of Wang et al.

As detailed in Claim Chart 4, Seiichiro et al. in view of Wang et al. renders claims 5 and 13 of the ‘851 patent obvious. As described above, Seiichiro et al. teaches a light emitting diode package, which includes a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer, a plurality contact holes formed in the second conductive type semiconductor layer and the active layer, a first bump on a first side of the semiconductor stack, a second bump on the first side of the semiconductor stack, and a

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protective insulation layer covering a sidewall of the semiconductor stack. The plurality of contact holes expose the first conductive type semiconductor layer. The first bump is electrically connected to the first conductive type semiconductor layer through the contact holes. The second bump is electrically connected to the second conductive type semiconductor layer. Seiichiro et al. fails to explicitly teach the protective insulation layer comprising a distributed Bragg reflector. Wang et al. teaches a protective insulation layer comprising a distributed Bragg reflector to achieve desired luminescence and reflection wavelengths in luminescent devices. *See* Exhibit 5, Col. 3, ll. 51-55. Because both Seiichiro et al. (Exhibit 2) and Wang et al. (Exhibit 5) relate to improved luminescent devices, and because Wang applies a known technique with a predictable result to improve a similar device, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 4

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF WANG ET AL.
5. The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.	Wang et al. discloses that the protective insulation layer (i.e., dielectric materials) may be layered with amorphous Si, and therefore, combinations for mirror stacks (e.g. distributed Bragg reflectors) can include pairings of materials into high and low reflective index pairs to create suitable distributed Bragg reflectors. <i>See</i> Exhibit 5, Col. 4, ll-4-8.
13. The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.	Wang et al. discloses that the first or second insulation layer (i.e., dielectric materials) may be layered with amorphous Si, and therefore, combinations for mirror stacks (e.g. distributed Bragg reflectors) can include pairings of materials into high and low reflective index pairs to create suitable distributed Bragg reflectors. <i>Id.</i>

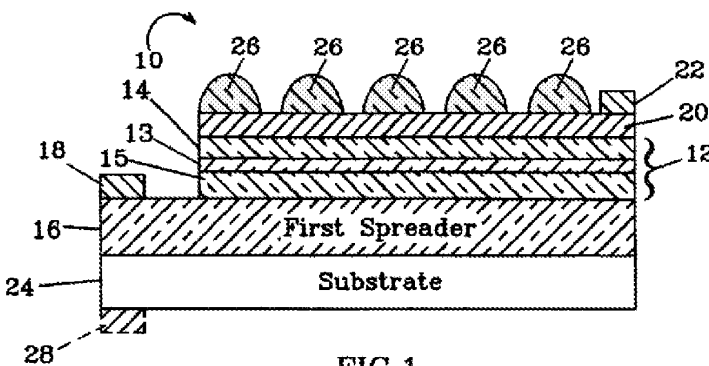
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For the foregoing reasons, Seiichiro et al. in view of Wang et al. renders claims 5 and 13 of the '851 patent obvious.

SNQP Statement No. 5: Whether claim 6 of the '851 patent is obvious in light of Seiichiro et al. in view of Thibeault et al.

As detailed in Claim Chart 5, Seiichiro et al. in view of Thibeault et al. renders claim 6 of the '851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. fails to explicitly teach a roughened surface of the first conductive type semiconductor layer. However, Thibeault et al. teaches a roughened surface of a first semiconductor material to allow for normally trapped TIR light to pass through or refract and escape, which ultimately results in enhanced light extraction. *See* Exhibit 6, Col. 6, ll. 57-61. Because both Seiichiro et al. (Exhibit 2) and Thibeault et al. (Exhibit 6) relate to enhanced light emitting diodes, and because Thibeault et al. applies a known roughening technique with a predictable result to improve a known light emitting diode, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 5

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF THIBEAULT ET AL.
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.	 The diagram shows a cross-section of an LED structure. At the bottom is a substrate 24. Above it is a first spreader 16. Above the first spreader is a second spreading layer 20, which is part of a larger layer 12. The second spreading layer 20 has a roughened surface with light extraction elements 26. Above the second spreading layer 20 is a first conductive type semiconductor layer 14, which is part of a larger layer 10. The first conductive type semiconductor layer 14 has a roughened surface. Above the first conductive type semiconductor layer 14 is a second conductive type semiconductor layer 18. A light source 10 is indicated by a curved arrow. Other labels include 13, 15, 22, and 28. FIG.1 Figure 1 of Thibeault et al. shows that the first conductive type semiconductor layer (i.e., the second spreading layer) 20 may be roughed by an array of light extraction elements (LEEs) formed on the second spreading layer 20 of conductive material. The LEEs 26 provide surfaces for normally trapped TIR light to pass through or refract and escape, thereby increasing the efficiency of the LED 10. <i>See Exhibit 6, Col. 6, ll. 57-61.</i>

For the foregoing reasons, Seiichiro et al. in view of Thibeault et al. renders claim 6 of the '851 patent obvious.

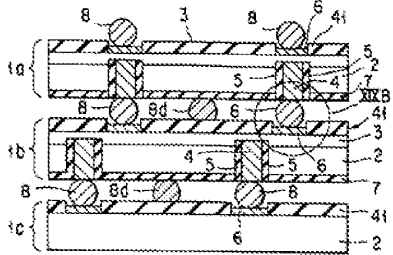
SNQP Statement No. 6: Whether claim 8 of the ‘851 patent is obvious in light of Seiichiro et al. in view of Hayasaka et al.

As detailed in Claim Chart 6, Seiichiro et al. in view of Hayasaka et al. renders claim 8 of the '851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. fails to explicitly teach a dummy bump between the first bump and the

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second bump. Hayasaka et al. teaches a dummy bump between the first bump and the second bump to improve the heat radiation capability of the semiconductor device. Because both Seiichiro et al. (Exhibit 2) and Hayasaka et al. (Exhibit 7) relate to semiconductor devices, and Hayasaka et al. teaches that using a dummy bump element in a semiconductor device produces a predictable result of improving the heat radiation capability of the device, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 6

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF HAYASAKA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	 Figure 19A of Hayasaka et al. shows an embodiment of a device having a heat radiation dummy bump 8d between the first and second bumps (i.e., chips) 1a and 1b. The dummy bump 8d may be made of a metal such as gold. See Exhibit 7, Col. 18, ll. 41-42, 47.

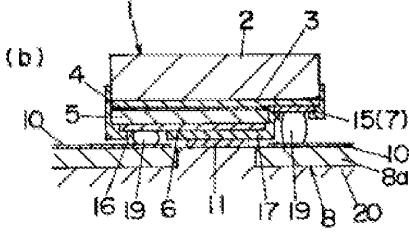
For the foregoing reasons, Seiichiro et al. in view of Hayasaka et al. renders claim 8 of the '851 patent obvious.

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SNQP Statement No. 7: Whether claim 8 of the '851 patent is obvious in light of Seiichiro et al. in view of Takuma et al.

As detailed in Claim Chart 7, Seiichiro et al. in view of Takuma et al. renders claim 8 of the '851 patent obvious. As described above Seiichiro et al. teaches all of the limitations of claim 1. Additionally, Seiichiro et al. teaches that the insulation layer is arranged on the side surfaces of the first bump and the second bump, as recited in claim 7. Seiichiro et al. fails to explicitly teach a dummy bump between the first bump and the second bump. However, Takuma teaches a dummy bump between the first bump and the second bump in order to improve heat dissipation from the LED package. *See* Exhibit 8, Paragraph [0054]. Because both Seiichiro et al. (Exhibit 2) and Takuma et al. (Exhibit 8) relate to light emitting diodes and because Takuma teaches that using a dummy bump in an LED package produces the predictable result of improving the heat dissipation from the LED package, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 7

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF TAKUMA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	 Figure 23B of Takuma et al. shows a dummy bump (i.e., filler 11) between the first bump 19 and the second bump 19.

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	The dummy bump 11 acts to improve the heat dissipation from LED chip 1. <i>See</i> Exhibit 8, Paragraph [0054].

For the foregoing reasons, Seiichiro et al. in view of Takuma et al. renders claim 8 of the ‘851 patent obvious.

SNQP Statement No. 8: Whether claim 10 of the ‘851 patent is obvious in light of Seiichiro et al. in view of Ho.

As detailed in Claim Chart 8, Seiichiro et al. in view of Ho renders claim 10 of the ‘851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. further teaches the substrate may comprise silicon. *See* Exhibit 2, Paragraph [0005]. Seiichiro et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Ho teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to allow for faster transfer of heat energy, thus increasing efficiency of heat dissipation. *See* Exhibit 9, Col.3, ll. 23-30. Because both Seiichiro et al. (Exhibit 2) and Ho (Exhibit 9) relate to light emitting diodes, and because using the technique of Ho would predictably result in increased efficiency of heat dissipation in the device of Seiichiro et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 8

U.S. PATENT NO. 9,070,851	CLAIM	SEIICHIRO ET AL. IN VIEW OF HO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 FIG.2 Figure 2 of Ho shows a light emitting chip 20 having a heating dissipating substrate 24. The heat dissipating substrate 24 has several through-holes (i.e., openings) 241 there through. The through-holes 241 are filled with the first bump and the second bump (i.e., metals with good heat dissipating properties). <i>See Exhibit 9, Col. 3, ll. 23-26.</i>	10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Seiichiro et al. discloses the substrate comprises silicon. <i>See Exhibit 2, Paragraph [0005].</i>	

For the foregoing reasons, Seichiro et al. in view of Ho renders claim 10 of the ‘851 patent obvious.

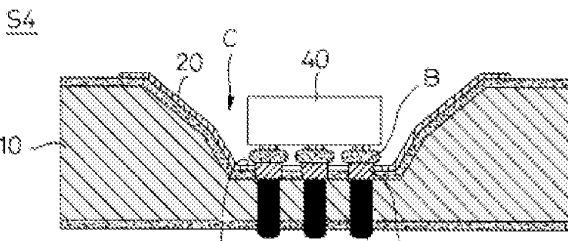
SNQP Statement No. 9: Whether claim 10 of the '851 patent is obvious in light of Seiichiro et al. in view of Hwan.

As detailed in Claim Chart 9, Seiichiro et al. in view of Hwan renders claim 10 of the ‘851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. fails to explicitly teach a first through-hole and a second through-hole with the

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first and second bumps being arranged in the first and second through-holes, respectively. Hwan teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to allow for improved heat dissipation and decreased thermal conductivity. Because both Seiichiro et al. (Exhibit 2) and Hwan (Exhibit 10) relate to light emitting diodes, and because using the technique of Hwan would predictably result in increased heat dissipation and decreased thermal conductivity in the device of Seiichiro et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 9

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF HWAN
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 Figure 8 of Hwan shows a substrate 10 with a plurality of through-holes formed there through. The first hole is filled with a first bump (i.e., metal plug) 30 and the second hole is filled with a second bump (i.e., metal plug) 30. See Exhibit 10, Abstract.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Hwan discloses that the substrate 10 is a silicon substrate. <i>Id.</i>

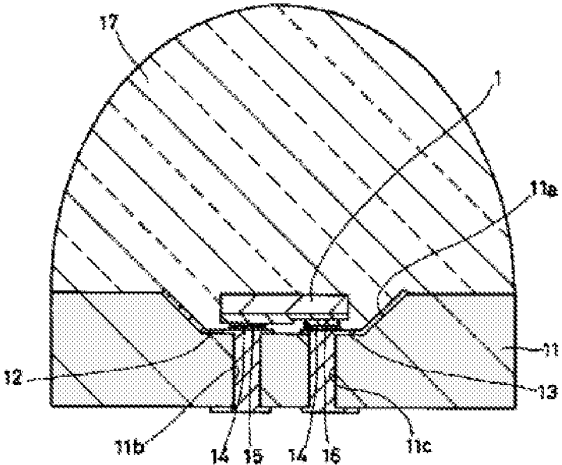
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For the foregoing reasons, Seiichiro et al. in view of Hwan renders claim 10 of the '851 patent obvious.

SNQP Statement No. 10: Whether claim 10 of the '851 patent is obvious in light of Seiichiro et al. in view of Etsuo.

As detailed in Claim Chart 10, Seiichiro et al. in view of Etsuo renders claim 10 of the '851 patent obvious. As described above, Seiichiro teaches all of the limitations of claim 1. Seiichiro et al. also discloses the substrate comprises silicon. *See* Exhibit 2, Paragraph [0005]. Seiichiro et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Etsuo teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to increase heat dissipation *See* Exhibit 11, Paragraph [0027]. Because both Seiichiro et al. (Exhibit 2) and Etsuo (Exhibit 11) relate to light emitting diodes, and because using the technique of Etsuo would predictably result in increased heat dissipation in the device of Seiichiro et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 10

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF ETSUO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	【図 3】  Figure 3 of Etsuo shows a light emitting diode with a substrate 11 having through holes 11b and 11c formed therethrough. The bumps 15 and 16 are positioned in the top of the through holes 11b and 11c, respectively. <i>See</i> Exhibit 11, Paragraph [0038].
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Seiichiro et al. discloses the substrate comprises silicon. <i>See</i> Exhibit 2, Paragraph [0005].

For the foregoing reasons, Seiichiro et al. in view of Etsuo renders claim 10 of the '851 patent obvious.

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SNQP Statement No. 11: Whether claims 14 and 15 of the '851 patent are obvious in light of Seiichiro et al. in view of Donofrio et al.

As detailed in Claim Chart 11, Seiichiro et al. in view of Donofrio et al. renders claims 14 and 15 of the '851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. fails to explicitly teach a module with the LED package, a circuit board and a lens to adjust the angle of light emitted from the package. Donofrio et al. teaches that the LED package is mounted on a circuit board and that microlenses are provided for the module. Because both Seiichiro et al. (Exhibit 2) and Donofrio et al. (Exhibit 4) relate to light emitting diodes, and it would be obvious to combine the LED package of Seiichiro et al. with a circuit board and lens with a reasonable expectation of success, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 11

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF DONOFRIO ET AL.
14. A light emitting diode (LED) module, comprising: a circuit board; the LED package of claim 1 arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.	Donofrio et al. discloses that the LED package may be mounted on a circuit board or wiring board, and microlenses may be provided. <i>Id.</i> at Col. 9, ll. 15-20, ll. 41-43.
15. The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a	Donofrio et al. discloses that the circuit board may be a wiring board. <i>Id.</i> at Col. 9, ll. 15-20.

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plurality of the LED packages is arranged on the MC-PCB.	

For the foregoing reasons, Seichiro et al. in view of Donofrio et al. renders claims 14 and 15 of the '851 patent obvious.

SNQP Statement No. 12: Whether claims 5 and 13 of the '851 patent are obvious in light of Shelton et al. et al. in view of Wang et al.

As detailed in Claim Chart 12, Shelton et al. in view of Wang et al. renders claims 5 and 13 of the '851 patent obvious. As described above, Shelton et al. teaches a light emitting diode package, which includes a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer, a plurality contact holes formed in the second conductive type semiconductor layer and the active layer, a first bump on a first side of the semiconductor stack, a second bump on the first side of the semiconductor stack, and a protective insulation layer covering a sidewall of the semiconductor stack. The plurality of contact holes expose the first conductive type semiconductor layer. The first bump is electrically connected to the first conductive type semiconductor layer through the contact holes. The second bump is electrically connected to the second conductive type semiconductor layer. Shelton et al. fails to explicitly teach the protective insulation layer comprising a distributed Bragg reflector. Wang et al. teaches a protective insulation layer comprising a distributed Bragg reflector to achieve desired luminescence and reflection wavelengths in luminescent devices. *See Exhibit 5,*

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Col. 3, ll. 51-55. Because both Shelton et al. (Exhibit 3) and Wang et al. (Exhibit 5) relate to improved luminescent devices, and apply a known technique with predictable results to improve similar devices, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 12

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF WANG ET AL.
5. The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.	Wang et al. discloses that the protective insulation layer (i.e., dielectric materials) may be layered with amorphous Si, and therefore, combinations for mirror stacks (e.g. distributed Bragg reflectors) can include pairings of materials into high and low reflective index pairs to create suitable distributed Bragg reflectors. <i>See</i> Exhibit 5, Col. 4, ll-4-8.
13. The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.	Wang et al. discloses that the insulation layers (i.e., dielectric materials) may be layered with amorphous Si, and therefore, combinations for mirror stacks (e.g. distributed Bragg reflectors) can include pairings of materials into high and low reflective index pairs to create suitable distributed Bragg reflectors. <i>Id.</i>

For the foregoing reasons, Shelton et al. in view of Wang et al. renders claims 5 and 13 of the '851 patent obvious.

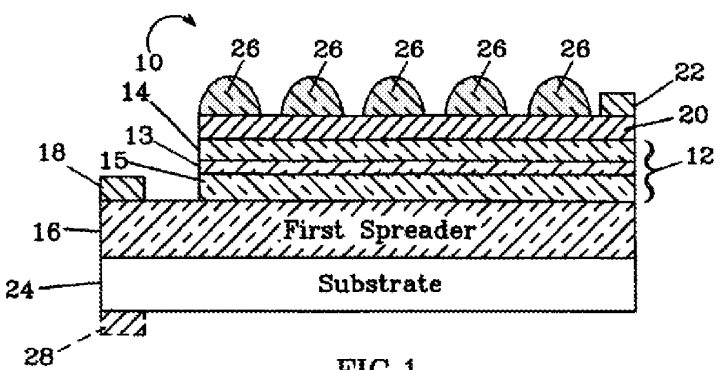
SNQP Statement No. 13: Whether claim 6 of the '851 patent is obvious in light of Shelton et al. in view of Thibeault et al.

As detailed in Claim Chart 13, Shelton et al. in view of Thibeault et al. renders claim 6 of the '851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim

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1. Shelton et al. fails to explicitly teach a roughened surface of the first conductive type semiconductor layer. However, Thibeault et al. teaches a roughened surface of a first semiconductor material to allow for normally trapped TIR light to pass through or refract and escape, which ultimately results in enhanced light extraction. *See* Exhibit 6, Col. 6, ll. 57-61. Because both Shelton et al. (Exhibit 3) and Thibeault et al. (Exhibit 6) relate to enhanced light emitting diodes, and because Thibeault et al. applies a known roughening technique with predictable results to a known light emitting diode, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 13

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON IN VIEW OF THIBEAULT ET AL.
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.	 FIG.1 Figure 1 of Thibeault et al. shows that the first conductive type semiconductor layer (i.e., the second spreading layer) 20 may be roughened by an array of light extraction elements (LEEs) formed on the second spreading layer 20 of conductive material. The LEEs 26 provide surfaces for normally trapped TIR light to pass through or refract and escape, thereby increasing the efficiency of the LED 10. <i>See</i> Exhibit 6, Col. 6, ll. 57-61.

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For the foregoing reasons, Shelton et al. in view of Thibeault et al. renders claim 6 of the ‘851 patent obvious.

SNQP Statement No. 14: Whether claim 8 of the ‘851 patent is obvious in light of Shelton et al. in view of Hayasaka et al.

As detailed in Claim Chart 14, Shelton et al. in view of Hayasaka et al. renders claim 8 of the ‘851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim 1. Shelton et al. fails to explicitly teach a dummy bump between the first bump and the second bump. Hayasaka et al. teaches a dummy bump between the first bump and the second bump to improve the heat radiation capability of the semiconductor device. Because both Shelton et al. (Exhibit 3) and Hayasaka et al. (Exhibit 7) relate to semiconductor devices, and Hayasaka et al. teaches that using a dummy bump element in a semiconductor device produces the predictable result of improving the heat radiation capability of the device, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 14

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF HAYASAKA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	FIG. 19A Figure 19A of Hayasaka et al. shows an embodiment of a device having a heat radiation dummy bump 8d between the first and second bumps (i.e., chips) 1a and 1b. The dummy bump 8d may be made of a metal such as gold. <i>See Exhibit 7, Col. 18, ll. 41-42, 47.</i>

For the foregoing reasons, Shelton et al. in view of Hayasaka et al. renders claim 8 of the ‘851 patent obvious.

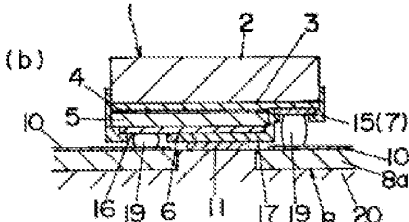
SNQP Statement No. 15: Whether claim 8 of the ‘851 patent is obvious in light of Shelton et al. in view of Takuma et al.

As detailed in Claim Chart 15, Shelton et al. in view of Takuma et al. renders claim 8 of the ‘851 patent obvious. As described above Shelton et al. teaches all of the limitations of claim 1. Additionally, Shelton et al. teaches that the insulation layer is arranged on the side surfaces of the first bump and the second bump, as recited in claim 7. Shelton et al. fails to explicitly teach a dummy bump between the first bump and the second bump. However, Takuma et al. teaches a dummy bump between the first bump and the second bump in order to improve heat dissipation

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from the LED package. *See* Exhibit 8, Paragraph [0054]. Because both Shelton et al. (Exhibit 3) and Takuma et al. (Exhibit 8) relate to light emitting diodes and because Takuma et al. teaches that using a dummy bump in an LED package produces the predictable result of improving the heat dissipation from the LED package, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 15

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF TAKUMA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	 Figure 23B of Takuma et al. shows a dummy bump (i.e., filler 11) between the first bump 19 and the second bump 19. The dummy bump 11 acts to improve the heat dissipation from LED chip 1. <i>See</i> Exhibit 8, Paragraph [0054].

For the foregoing reasons, Shelton et al. in view of Takuma et al. renders claim 8 of the ‘851 patent obvious.

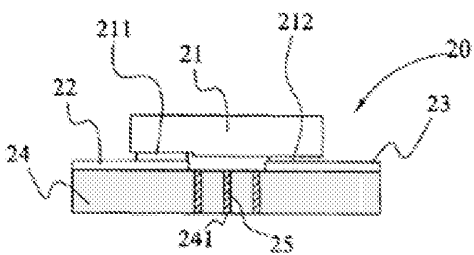
SNQP Statement No. 16: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Shelton et al. in view of Ho.

As detailed in Claim Chart 16, Shelton et al. in view of Ho renders claims 9 and 10 of the ‘851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim 1.

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Shelton et al. further discloses that the substrate may be sapphire or silicon carbide. *See* Exhibit 3, Col. 4, ll. 58-60. *See* Exhibit 2, Paragraph [0005]. Shelton et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Ho teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second bump in the second through-hole to allow for faster transfer of heat energy, thus increasing efficiency of heat dissipation. *See* Exhibit 9, Col.3, ll. 23-30. Because both Shelton et al. (Exhibit 3) and Ho (Exhibit 9) relate to light emitting diodes, and because using the technique of Ho would predictably result in increased efficiency of heat dissipation in the device of Shelton et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 16

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF HO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 FIG.2 Figure 2 of Ho shows a light emitting chip 20 having a heating dissipating substrate 24. The heat dissipating substrate 24 has several through-holes (i.e., openings) 241 there through. The through-holes 241 are filled with the first

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	bump and the second bump (i.e., metals with good heat dissipating properties). <i>See</i> Exhibit 9, Col. 3, ll. 23-26.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Shelton et al. discloses that the substrate may be sapphire or silicon carbide. <i>See</i> Exhibit 3, Col. 4, ll. 58-60.

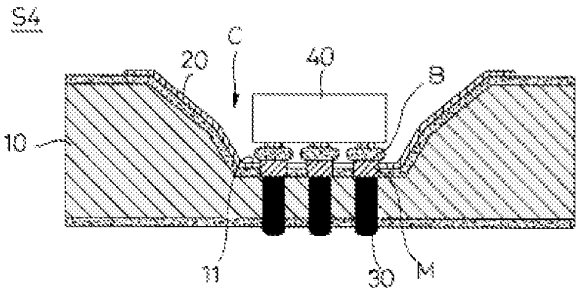
For the foregoing reasons, Shelton et al. in view of Ho renders claims 9 and 10 of the ‘851 patent obvious.

SNQP Statement No. 17: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Shelton et al. in view of Hwan.

As detailed in Claim Chart 17, Shelton et al. in view of Hwan renders claims 9 and 10 of the ‘851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim 1. Shelton et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Hwan teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to allow for improved heat dissipation and decreased thermal conductivity. Because both Shelton et al. (Exhibit 3) and Hwan (Exhibit 10) relate to light emitting diodes, and because using the technique of Hwan would predictably result in increased heat dissipation and decreased thermal conductivity in the device of Shelton et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

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Claim Chart 17

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF HWAN
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 Figure 8 of Hwan shows a substrate 10 with a plurality of through-holes formed there through. The first hole is filled with a first bump (i.e., metal plug) 30 and the second hole is filled with a second bump (i.e., metal plug) 30. See Exhibit 10, Abstract.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Shelton et al. discloses that the substrate may be sapphire or silicon carbide. See Exhibit 3, Col. 4, ll. 58-60.

For the foregoing reasons, Shelton et al. in view of Hwan renders claims 9 and 10 of the ‘851 patent obvious.

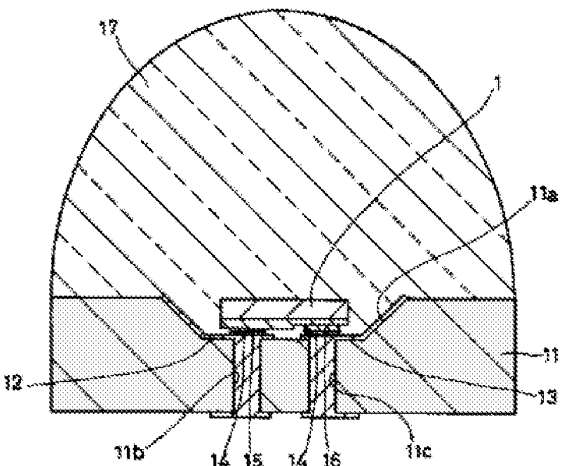
SNQP Statement No. 18: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Shelton et al. in view of Etsuo.

As detailed in Claim Chart 18, Shelton et al. in view of Etsuo renders claims 9 and 10 of the ‘851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim 1. Shelton et al. discloses that the substrate may be sapphire or silicon carbide. See Exhibit 3, Col. 4, ll. 58-60. Shelton et al. fails to explicitly teach a first through-hole and a second through-

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hole with the first and second bumps being arranged in the first and second through-holes, respectively. Etsuo teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to increase heat dissipation *See* Exhibit 11, Paragraph [0027]. Because both Shelton et al. (Exhibit 3) and Etsuo (Exhibit 11) relate to light emitting diodes, and because using the technique of Etsuo would predictably result in increased heat dissipation in the device of Shelton et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 18

U.S. PATENT NO. 9,070,851 CLAIM	SHELTON ET AL. IN VIEW OF ETSUO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	【図 3】  Figure 3 of Etsuo shows a light emitting diode with a substrate 11 having through holes 11b and 11c formed there through. The bumps 15 and 16 are positioned in the top of the through holes 11b and 11c, respectively. <i>See</i> Exhibit 11, Paragraph [0038].
10. The LED package of claim 9,	Shelton et al. discloses that the substrate may be sapphire or

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wherein the substrate comprises sapphire or silicon.	silicon carbide. <i>See</i> Exhibit 3, Col. 4, ll. 58-60.

For the foregoing reasons, Shelton et al. in view of Etsuo renders claims 9 and 10 of the ‘851 patent obvious.

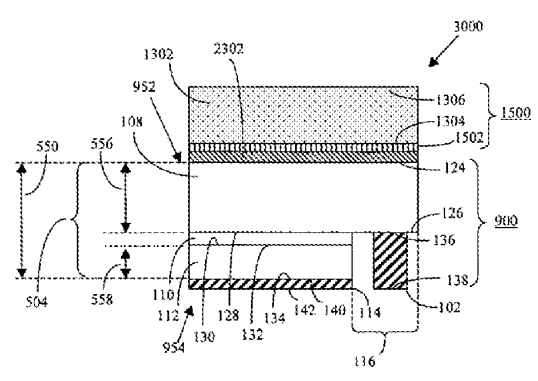
SNQP Statement No. 19: Whether claim 4 of the ‘851 patent is obvious in light of Donofrio et al. in view of Beeson et al.

As detailed in Claim Chart 19, Donofrio et al. in view of Beeson et al. renders claims 9 and 10 of the ‘851 patent obvious. As described above, Donofrio et al. teaches a light emitting diode package, which includes a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer, a plurality contact holes formed in the second conductive type semiconductor layer and the active layer, a first bump on a first side of the semiconductor stack, a second bump on the first side of the semiconductor stack, and a protective insulation layer covering a sidewall of the semiconductor stack. The plurality of contact holes expose the first conductive type semiconductor layer. The first bump is electrically connected to the first conductive type semiconductor layer through the contact holes. The second bump is electrically connected to the second conductive type semiconductor layer. Donofrio et al. also teaches a wavelength converter arranged on a second side of the semiconductor stack. *See* Exhibit 4, Col. 1, ll. 46-47. Donofrio et al. fails to explicitly teach a side of the wavelength

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converter being flush with a side surface of the protective insulation layer. Beeson et al, however, discloses that a side surface of the protective insulation layer is flush with a side surface of the wavelength converter resulting in a more uniform light emitting stack. Because both Donofrio et al. (Exhibit 4) and Beeson et al. (Exhibit 12) relate to light emitting diodes and the simple substitution of the wavelength with a side surface flush with the side surface of the protective insulation layer would yield the same predictable results for the diode of Donofrio et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 19

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF BEESON ET AL.
4. The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.	 FIG. 30 Beeson et al. discloses a wavelength converter (i.e., wavelength conversion layer) 1302, which has a side surface that is flush with a side surface of the protective insulation layer (i.e., dichoric layer) 1502.

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For the foregoing reasons, Donofrio et al. in view of Beeson et al. renders claim 4 of the ‘851 patent obvious.

SNQP Statement No. 20: Whether claim 8 of the ‘851 patent is obvious in light of Donofrio et al. in view of Hayasaka et al.

As detailed in Claim Chart 20, Donofrio et al. in view of Hayasaka et al. renders claim 8 of the ‘851 patent obvious. As described above, Donofrio et al. teaches all of the limitations of claim 1. Donofrio et al. fails to teach a dummy bump between the first bump and the second bump. Hayasaka et al. teaches a dummy bump between the first bump and the second bump to improve the heat radiation capability of the semiconductor device. Because both Donofrio et al. (Exhibit 4) and Hayasaka et al. (Exhibit 7) relate to semiconductor devices, and Hayasaka et al. teaches that using a dummy bump element in a semiconductor device produces the predictable result of improving the heat radiation capability of the device, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

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Claim Chart 20

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF HAYASAKA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	FIG. 19A Figure 19A of Hayasaka et al. shows an embodiment of a device having a heat radiation dummy bump 8d between the first and second bumps (i.e., chips) 1a and 1b. The dummy bump 8d may be made of a metal such as gold. <i>See Exhibit 7, Col. 18, ll. 41-42, 47.</i>

For the foregoing reasons, Donofrio et al. in view of Hayasaka et al. renders claim 8 of the '851 patent obvious.

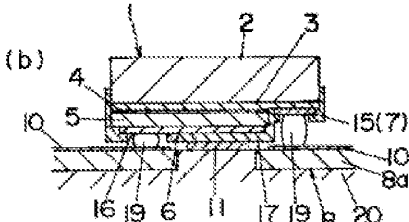
SNQP Statement No. 21: Whether claim 8 of the '851 patent is obvious in light of Donofrio et al. in view of Takuma et al.

As detailed in Claim Chart 21, Donofrio et al. in view of Takuma et al. renders claim 8 of the '851 patent obvious. As described above Donofrio et al. teaches all of the limitations of claim 1. Additionally, Donofrio et al. teaches that the insulation layer is arranged on the side surfaces of the first bump and the second bump, as recited in claim 7. Donofrio et al. fails to explicitly teach a dummy bump between the first bump and the second bump. However, Takuma et al. teaches a dummy bump between the first bump and the second bump in order to

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improve heat dissipation from the LED package. *See* Exhibit 8, Paragraph [0054]. Because both Donofrio et al. (Exhibit 4) and Takuma et al. (Exhibit 8) relate to light emitting diodes and because Takuma et al. teaches that using a dummy bump in an LED package produces the predictable result of improving the heat dissipation from the LED package, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 21

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF TAKUMA ET AL.
8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.	 Figure 23B of Takuma et al. shows a dummy bump (i.e., filler 11) between the first bump 19 and the second bump 19. The dummy bump 11 acts to improve the heat dissipation from LED chip 1. <i>See</i> Exhibit 8, Paragraph [0054].

For the foregoing reasons, Donofrio et al. in view of Takuma et al. renders claim 8 of the ‘851 patent obvious.

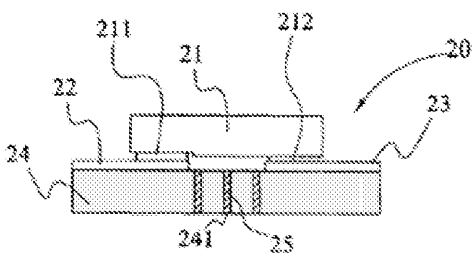
SNQP Statement No. 22: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Donofrio et al. in view of Ho.

As detailed in Claim Chart 22, Donofrio et al. in view of Ho renders claims 9 and 10 of the ‘851 patent obvious. As described above, Donofrio et al. teaches all of the limitations of

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claim 1. Donofrio et al. further discloses that the substrate may be a sapphire or silicon substrate. *See* Exhibit 4, Col. 1, ll. 37-40. Donofrio et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Ho teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to allow for faster transfer of heat energy, thus increasing efficiency of heat dissipation. *See* Exhibit 9, Col.3, ll. 23-30. Because both Donofrio et al. (Exhibit 4) and Ho (Exhibit 9) relate to light emitting diodes, and because using the technique of Ho would predictably result in increased efficiency of heat dissipation in the device of Donofrio et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 22

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF HO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 FIG.2 Figure 2 of Ho shows a light emitting chip 20 having a heating dissipating substrate 24. The heat dissipating substrate 24 has several openings 241 therethrough. The openings 241 are filled with metals with good heat

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	dissipating properties. <i>See</i> Exhibit 9, Col. 3, ll. 23-26.
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Donofrio et al. discloses that the substrate may be a sapphire or silicon substrate. <i>See</i> Exhibit 4, Col. 1, ll. 37-40.

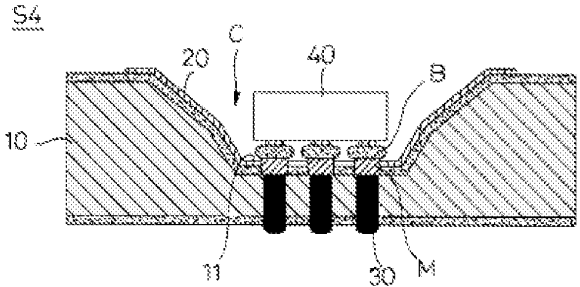
For the foregoing reasons, Donofrio et al. in view of Ho renders claims 9 and 10 of the ‘851 patent obvious.

SNQP Statement No. 23: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Donofrio et al. in view of Hwan.

As detailed in Claim Chart 23, Donofrio et al. in view of Hwan renders claims 9 and 10 of the ‘851 patent obvious. As described above, Donofrio et al. teaches all of the limitations of claim 1. Donofrio et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Hwan teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second-bump in the second through-hole to allow for improved heat dissipation and decreased thermal conductivity. Because both Donofrio et al. (Exhibit 4) and Hwan (Exhibit 10) relate to light emitting diodes, and because using the technique of Hwan would predictably result in increased heat dissipation and decreased thermal conductivity in the device of Donofrio et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

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Claim Chart 23

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF HWAN
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	 Figure 2 of Ho shows a light emitting chip 20 having a heating dissipating substrate 24. The heat dissipating substrate 24 has several through-holes (i.e., openings) 241 there through. The through-holes 241 are filled with the first bump and the second bump (i.e., metals with good heat dissipating properties). <i>See Exhibit 9, Col. 3, ll. 23-26.</i>
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Donofrio et al. discloses that the substrate may be a sapphire or silicon substrate. <i>See Exhibit 4, Col. 1, ll. 37-40.</i>

For the foregoing reasons, Donofrio et al. in view of Hwan renders claims 9 and 10 of the ‘851 patent obvious.

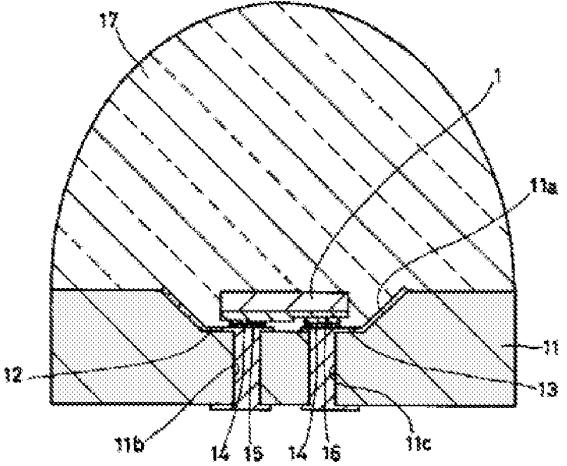
SNQP Statement No. 24: Whether claims 9 and 10 of the ‘851 patent are obvious in light of Donofrio et al. in view of Etsuo.

As detailed in Claim Chart 24, Donofrio et al. in view of Etsuo renders claims 9 and 10 of the ‘851 patent obvious. As described above, Donofrio et al. teaches all of the limitations of claim 1. Donofrio et al. further discloses that the substrate may be a sapphire or silicon substrate.

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See Exhibit 4, Col. 1, ll. 37-40. Donofrio et al. fails to explicitly teach a first through-hole and a second through-hole with the first and second bumps being arranged in the first and second through-holes, respectively. Etsuo teaches a first through-hole and a second through-hole, with the first bump in the first through-hole and the second bump in the second through-hole to increase heat dissipation See Exhibit 11, Paragraph [0027]. Because both Donofrio et al. (Exhibit 4) and Etsuo (Exhibit 11) relate to light emitting diodes, and because using the technique of Etsuo would predictably result in increased heat dissipation in the device of Donofrio et al., one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 24

U.S. PATENT NO. 9,070,851 CLAIM	DONOFRIO ET AL. IN VIEW OF ETSUO
9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.	【圖 3】  Figure 3 of Etsuo shows a light emitting diode with a

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	substrate 11 having through holes 11b and 11c formed there through. The bumps 15 and 16 are positioned in the top of the through holes 11b and 11c, respectively. <i>See</i> Exhibit 11, Paragraph [0038].
10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.	Donofrio et al. discloses that the substrate may be a sapphire or silicon substrate. <i>See</i> Exhibit 4, Col. 1, ll. 37-40.

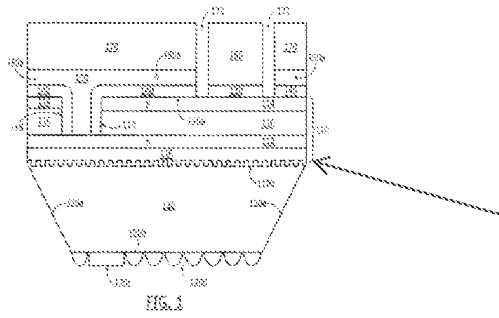
For the foregoing reasons, Donofrio et al. in view of Etsuo renders claims 9 and 10 of the ‘851 patent obvious.

SNQP Statement No. 25: Whether claim 6 of the ‘851 patent is obvious in light of Seiichiro et al. in view of Donofrio et al.

As detailed in Claim Chart 25, Seiichiro et al. in view of Donofrio et al. renders claim 6 of the ‘851 patent obvious. As described above, Seiichiro et al. teaches all of the limitations of claim 1. Seiichiro et al. fails to explicitly teach a roughened surface of the first conductive type semiconductor layer. However, Donofrio et al. teaches a roughened surface of a first semiconductor material which ultimately results in enhanced light extraction. *See* Exhibit 4, Col. 9, ll. 4-9. Because both Seiichiro et al. (Exhibit 2) and Donofrio et al. (Exhibit 4) relate to enhanced light emitting diodes, and because Donofrio et al. applies a known roughening technique with a predictable result to improve a known light emitting diode, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

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Claim Chart 25

U.S. PATENT NO. 9,070,851 CLAIM	SEIICHIRO ET AL. IN VIEW OF DONOFRIO ET AL.
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.	 Donofrio et al. discloses that the first conductive type semiconductor layer 112 may have a roughened surface. Figure 1 shows that the interface between the sapphire substrate 120 and the diode region 110 may be textured, as shown by the jagged line. <i>Id.</i> Col. 9, ll. 4-9.

For the foregoing reasons, Seiichiro et al. in view of Donofrio et al. renders claim 6 of the ‘851 patent obvious.

SNQP Statement No. 26: Whether claim 6 of the ‘851 patent is obvious in light of Shelton et al. in view of Donofrio et al.

As detailed in Claim Chart 26, Shelton et al. in view of Donofrio et al. renders claim 6 of the ‘851 patent obvious. As described above, Shelton et al. teaches all of the limitations of claim 1. Shelton et al. fails to explicitly teach a roughened surface of the first conductive type semiconductor layer. However, Donofrio et al. teaches a roughened surface of a first semiconductor material which ultimately results in enhanced light extraction. *See* Exhibit 4, Col.

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9, ll. 4-9. Because both Shelton et al. (Exhibit 3) and Donofrio et al. (Exhibit 4) relate to enhanced light emitting diodes, and because Donofrio et al. applies a known roughening technique with a predictable result to improve a known light emitting diode, one of ordinary skill in the art would have a motivation to combine the teachings of the two references.

Claim Chart 26

U.S. PATENT NO. 9,070,851	SHELTON ET AL. IN VIEW OF DONOFRIO ET AL.
CLAIM	
6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.	Donofrio et al. discloses that the first conductive type semiconductor layer 112 may have a roughened surface. Figure 1 shows that the interface between the sapphire substrate 120 and the diode region 110 may be textured, as shown by the jagged line. <i>Id.</i> Col. 9, ll. 4-9.

For the foregoing reasons, Shelton et al. in view of Donofrio et al. renders claim 6 of the ‘851 patent obvious.

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XI. CONCLUSION

A number of substantial new questions of patentability regarding claims 1-15 of the '851 patent are raised under 35 U.S.C. §§ 102 and 103. The foregoing illustrates that the above-cited references disclose teachings not previously considered or discussed on the record during the original prosecution of the '851 patent. In sum, the art cited herein provides new, non-cumulative technological teachings not previously considered and discussed on the record, which raise new SNQPs as to claims 1-15 of the '851 patent.

Requester respectfully requests that the '851 patent be reexamined in view of the compelling showing made in this Request that claims 1-15 of the '851 patent are invalid.

Dated: April 15, 2016

Respectfully submitted,

/ Alan Taboada /

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XII. CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 1.510(b)(5) and 37 C.F.R. § 1.33(c), I hereby certify that on April 15, 2016, a complete copy of this *ex parte* reexamination request, including the accompanying transmittal, Form PTO/SB/08, and all attachments and exhibits, are being served via Express Mail Label No. EF 022912675 US upon the current attorneys of record for the Patent Owner:

H.C. Park & Associates, PLC
1894 Preston White Drive
Reston, VA 20191
Customer Number: 58027

XIII. CERTIFICATION OF NO ESTOPPEL

Pursuant to 37 C.F.R. § 1.510(b)(6), Requester certifies that the statutory estoppel provisions of 35 U.S.C. §315(e)(1) and 35 U.S.C. §325(e)(1) do not prohibit Requester from filing the present *ex parte* reexamination request.

Respectfully submitted,

Electronic Signature: / Alan Taboada /

Alan Taboada

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US009070851B2

(12) **United States Patent**
Seo et al.

(10) **Patent No.:** **US 9,070,851 B2**
(45) **Date of Patent:** **Jun. 30, 2015**

(54) **WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME**

(75) Inventors: **Won Cheol Seo**, Ansan-si (KR); **Dae Sung Kal**, Ansan-si (KR)

(73) Assignee: **Seoul Semiconductor Co., Ltd.**, Ansan-si (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 816 days.

(21) Appl. No.: **13/194,317**

(22) Filed: **Jul. 29, 2011**

(65) **Prior Publication Data**

US 2012/0074441 A1 Mar. 29, 2012

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
H01L 33/60 (2010.01)
H01L 33/62 (2010.01)
(Continued)

(52) **U.S. Cl.**
CPC **H01L 33/62** (2013.01); **H01L 27/153** (2013.01); **H01L 33/0079** (2013.01); **H01L 33/20** (2013.01); **H01L 33/38** (2013.01); **H01L 33/382** (2013.01); **H01L 33/46** (2013.01); **H01L 2933/0016** (2013.01); **H01L 2924/0002** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC ... H01L 33/382; H01L 33/0079; H01L 33/22; H01L 33/0041; H01L 2224/8592
USPC 257/88-103, E33.062, E33.064
See application file for complete search history.

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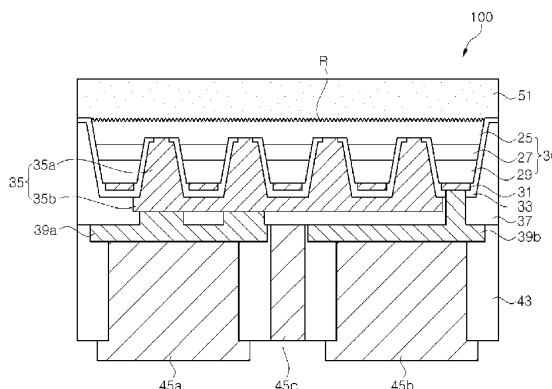
Primary Examiner — Cuong Q Nguyen

(74) *Attorney, Agent, or Firm* — H.C. Park & Associates, PLC

(57) **ABSTRACT**

Exemplary embodiments of the present invention provide a wafer-level light emitting diode (LED) package and a method of fabricating the same. The LED package includes a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

15 Claims, 19 Drawing Sheets



(51) **Int. Cl.**

H01L 27/15 (2006.01)
H01L 33/10 (2010.01)
H01L 33/50 (2010.01)
H01L 33/00 (2010.01)
H01L 33/20 (2010.01)
H01L 33/38 (2010.01)
H01L 33/46 (2010.01)
H01L 33/48 (2010.01)

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(52) **U.S. Cl.**

CPC **H01L33/486** (2013.01); **H01L 33/10**
(2013.01); **H01L 33/50** (2013.01)

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Figure 1

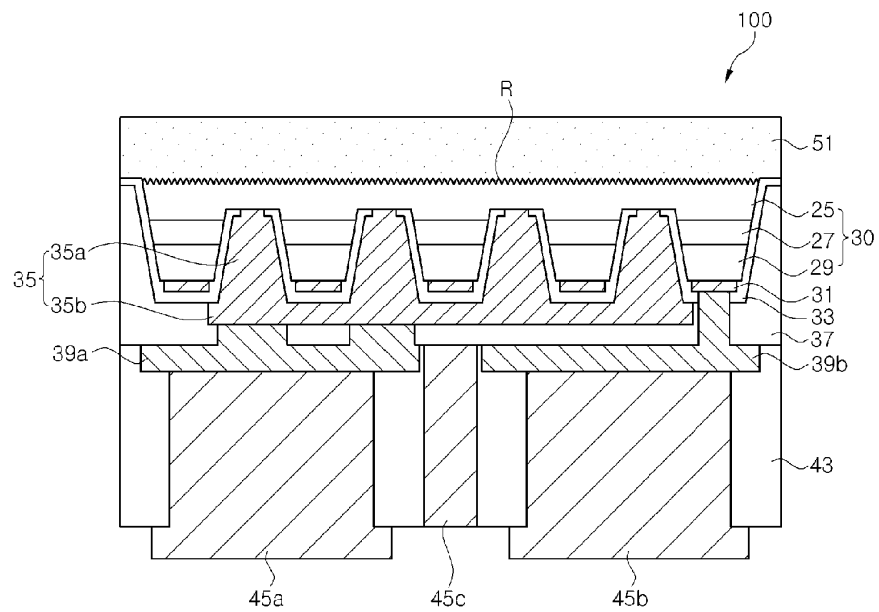


Figure 2

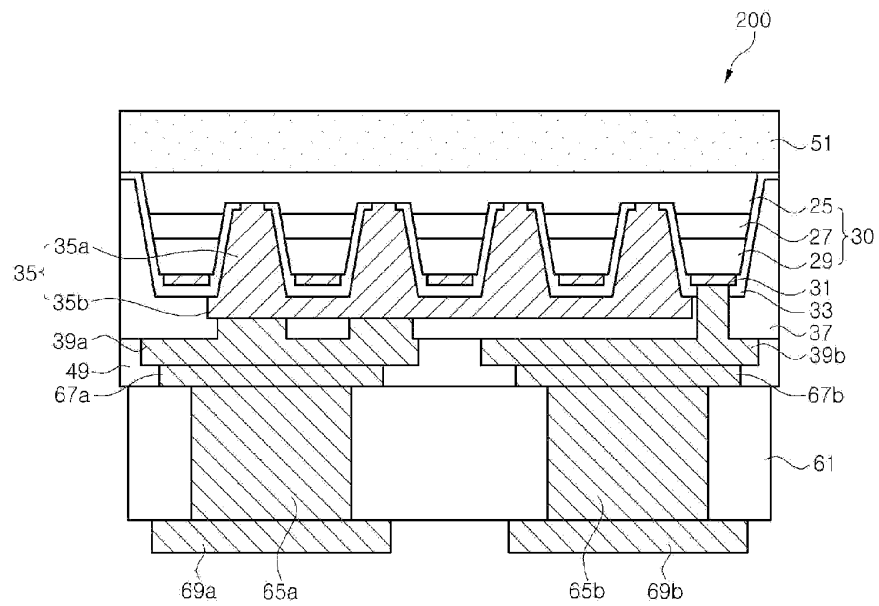


Figure 3

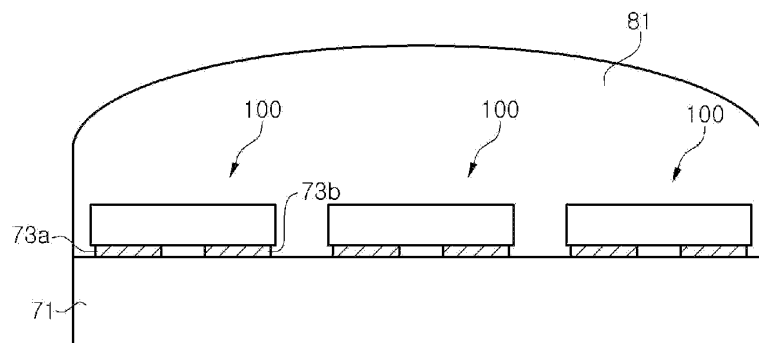


Figure 4

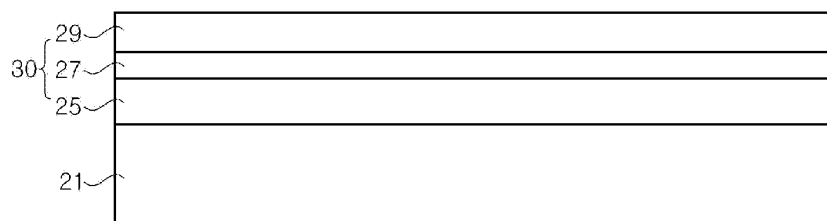


Figure 5

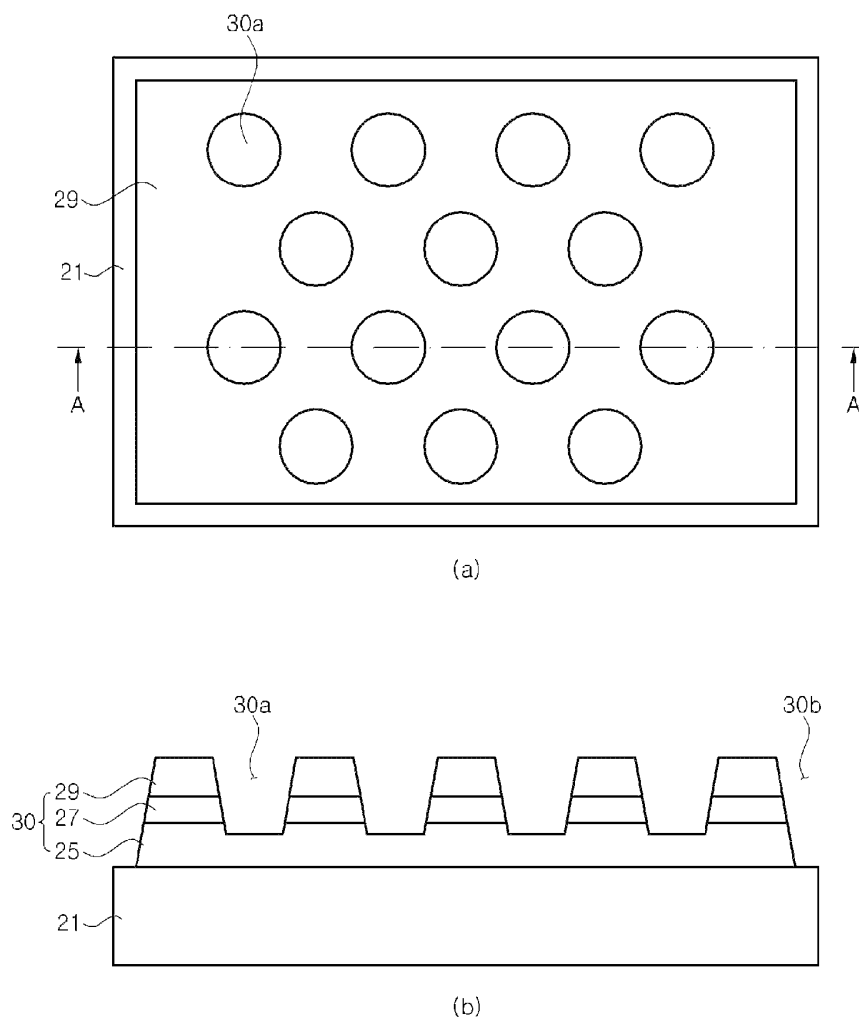


Figure 6

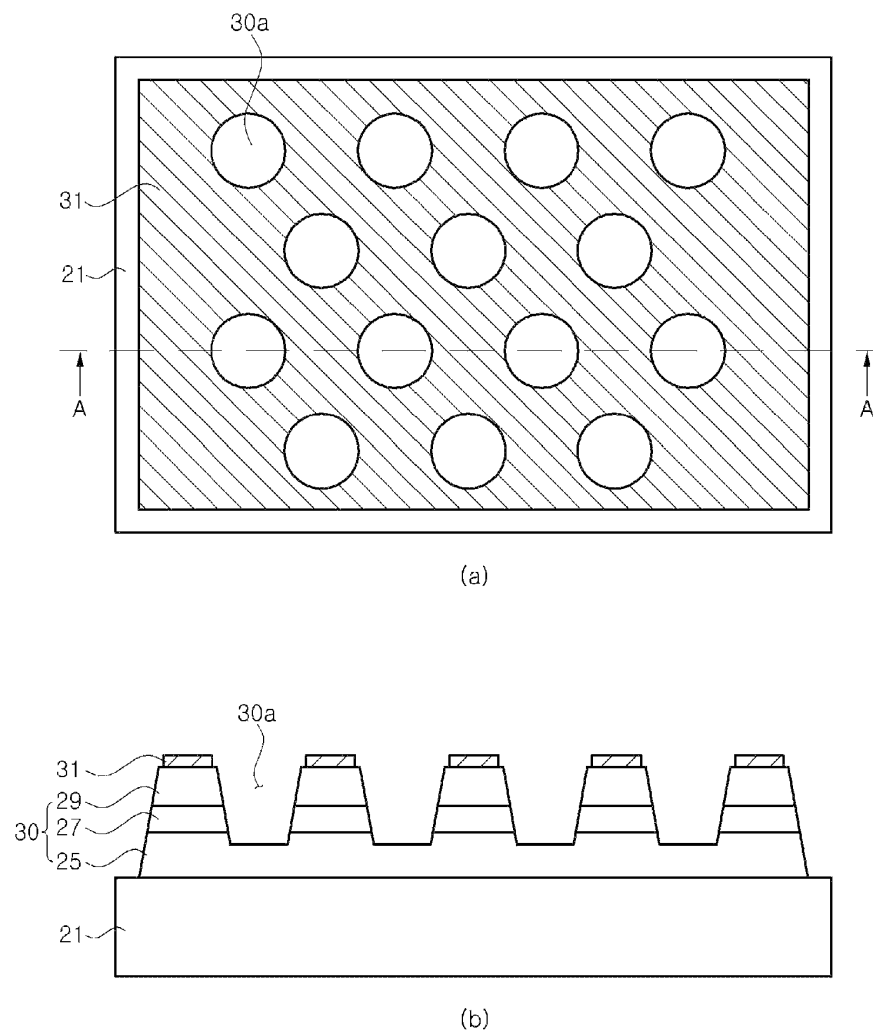


Figure 7

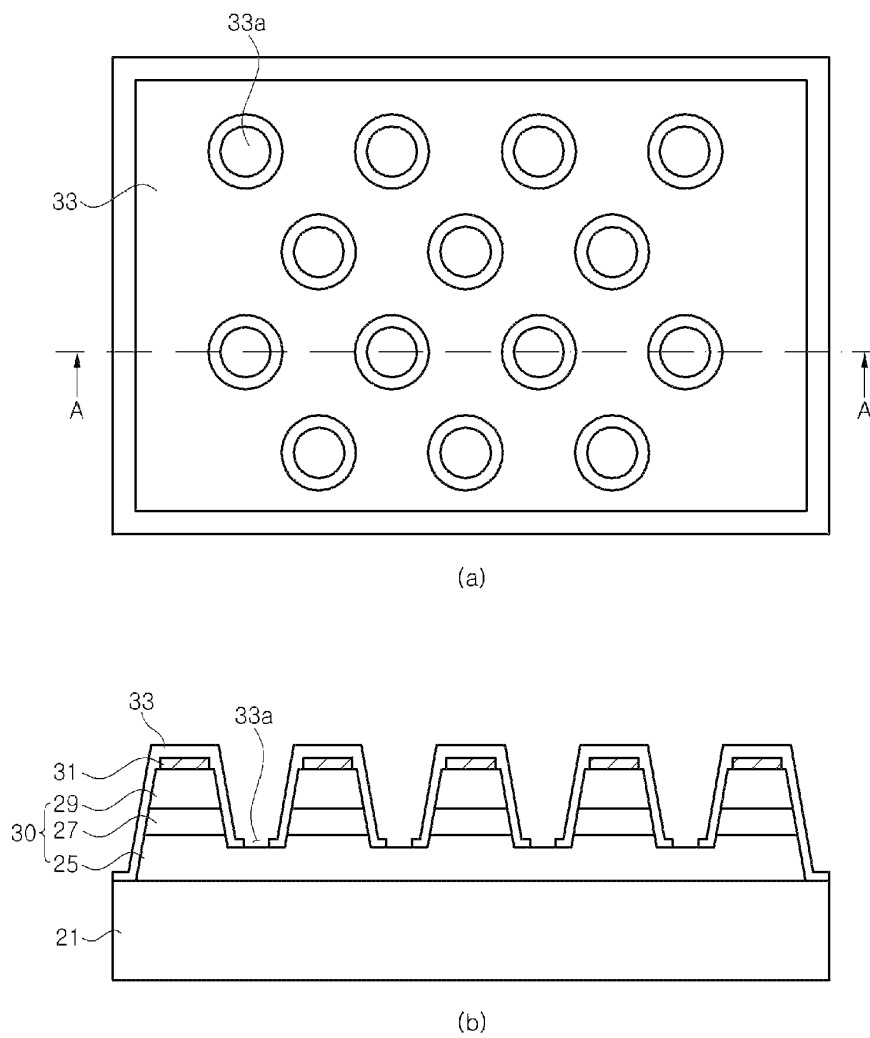


Figure 8

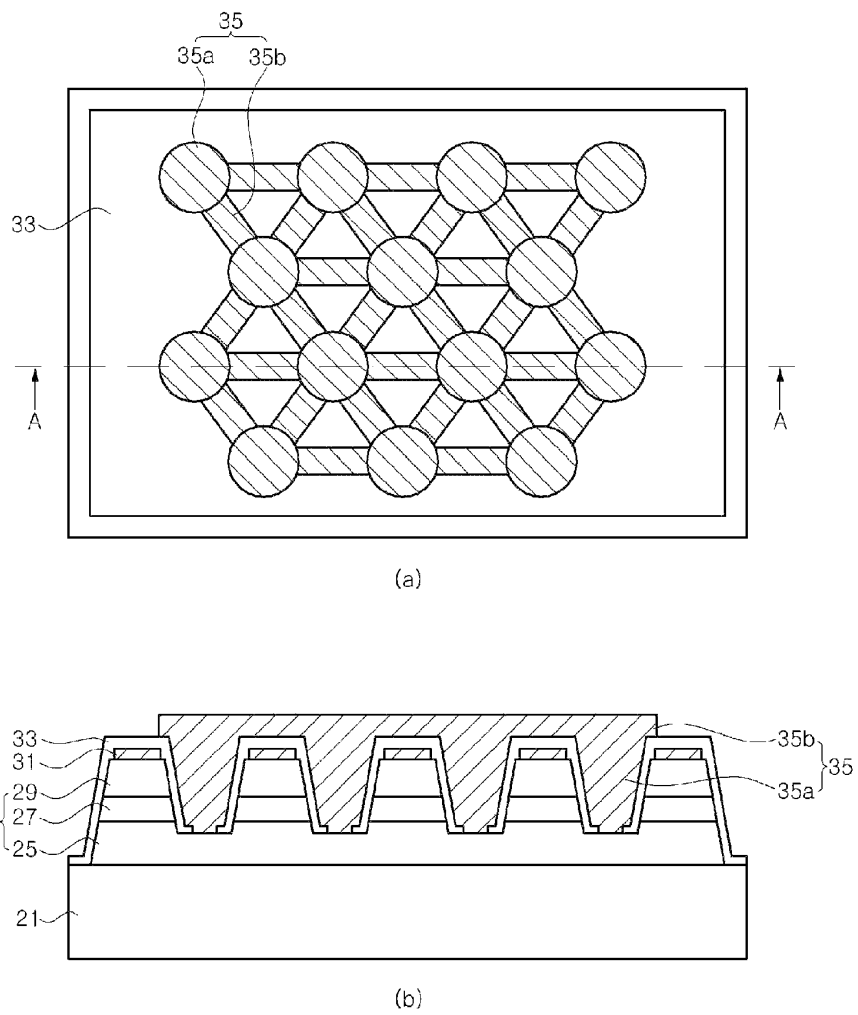


Figure 9

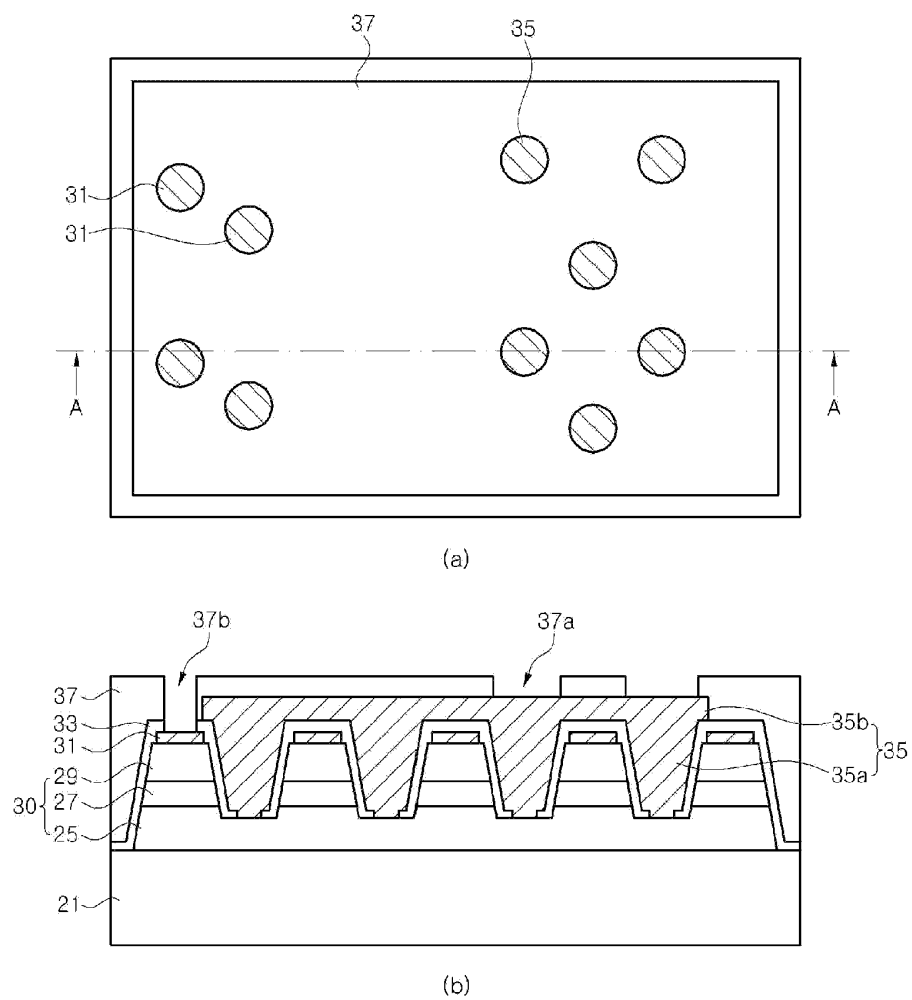


Figure 10

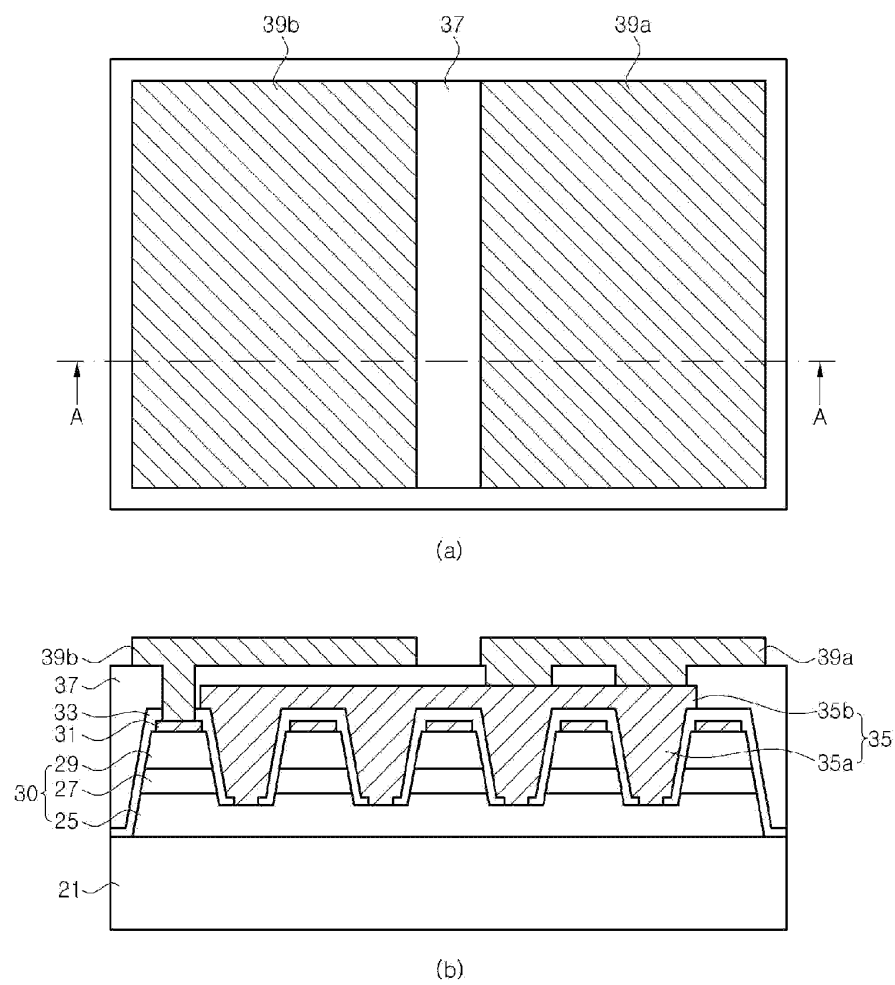


Figure 11

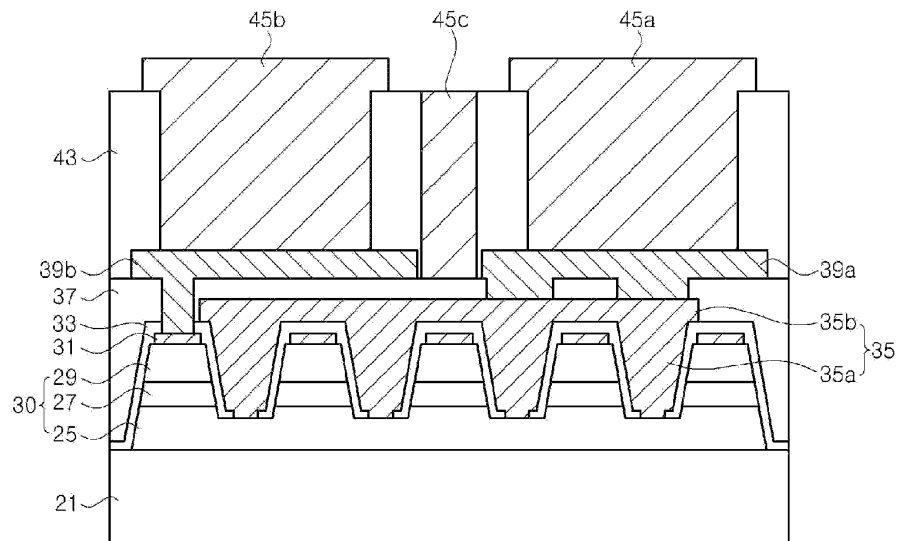


Figure 12

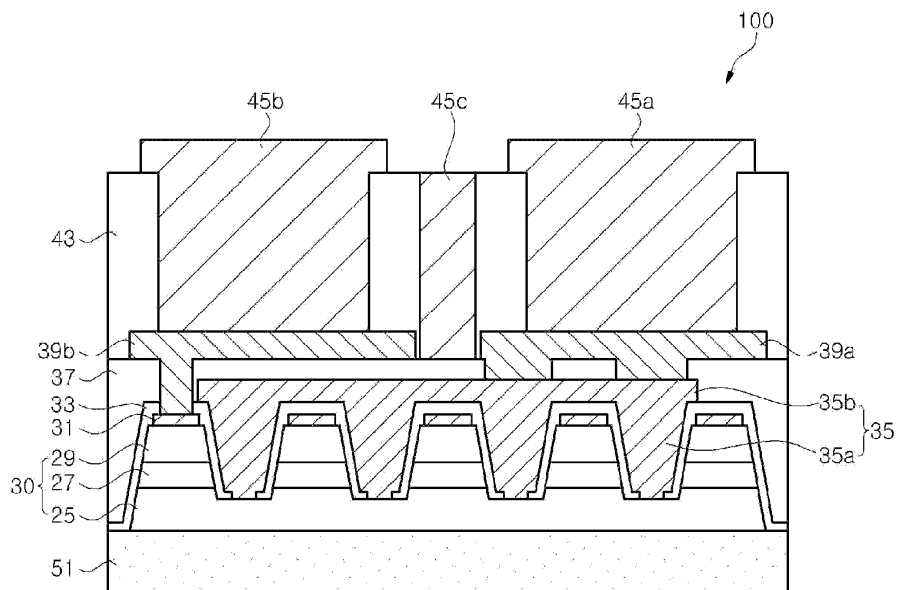


Figure 13

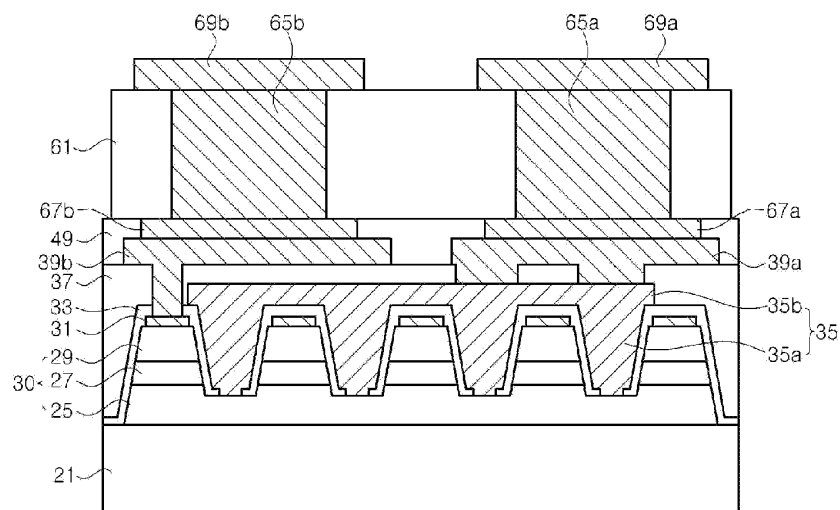


Figure 14

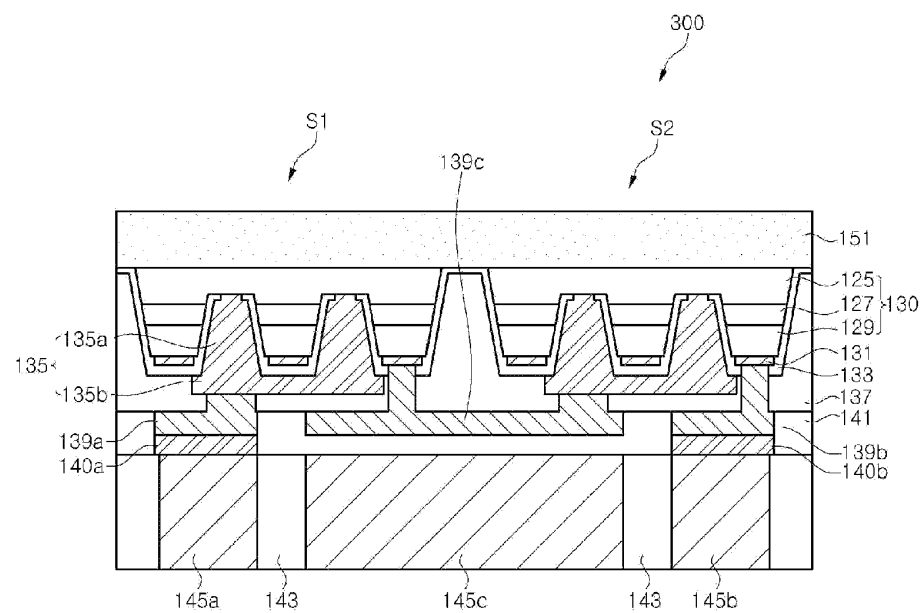


Figure 15

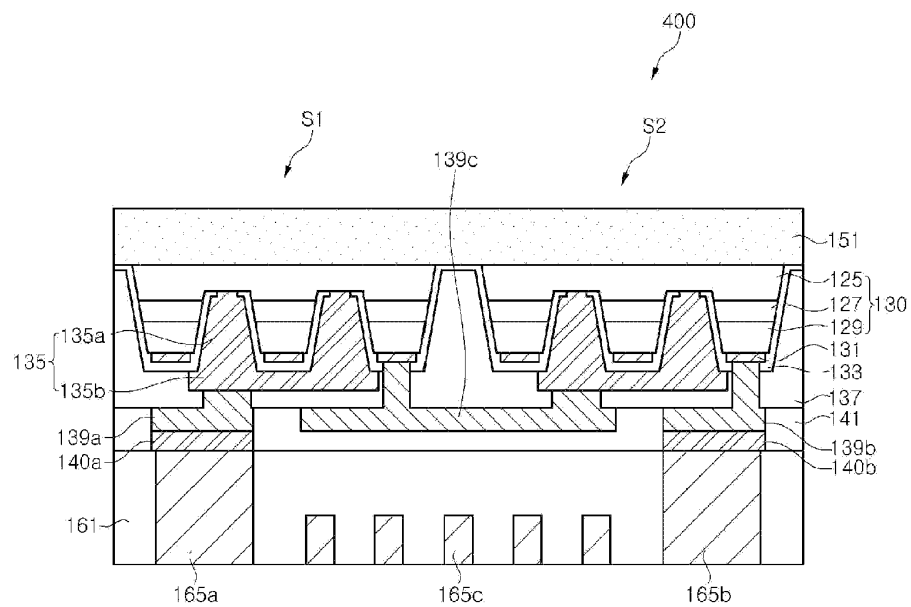


Figure 16

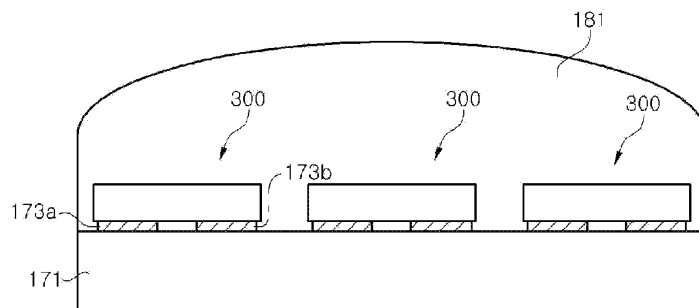


Figure 17

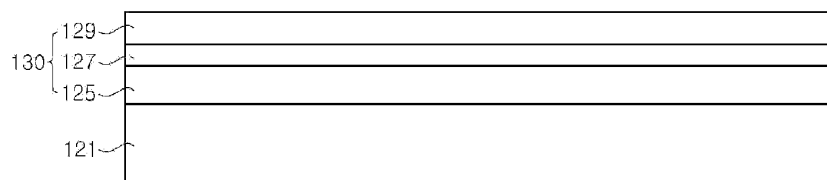


Figure 18

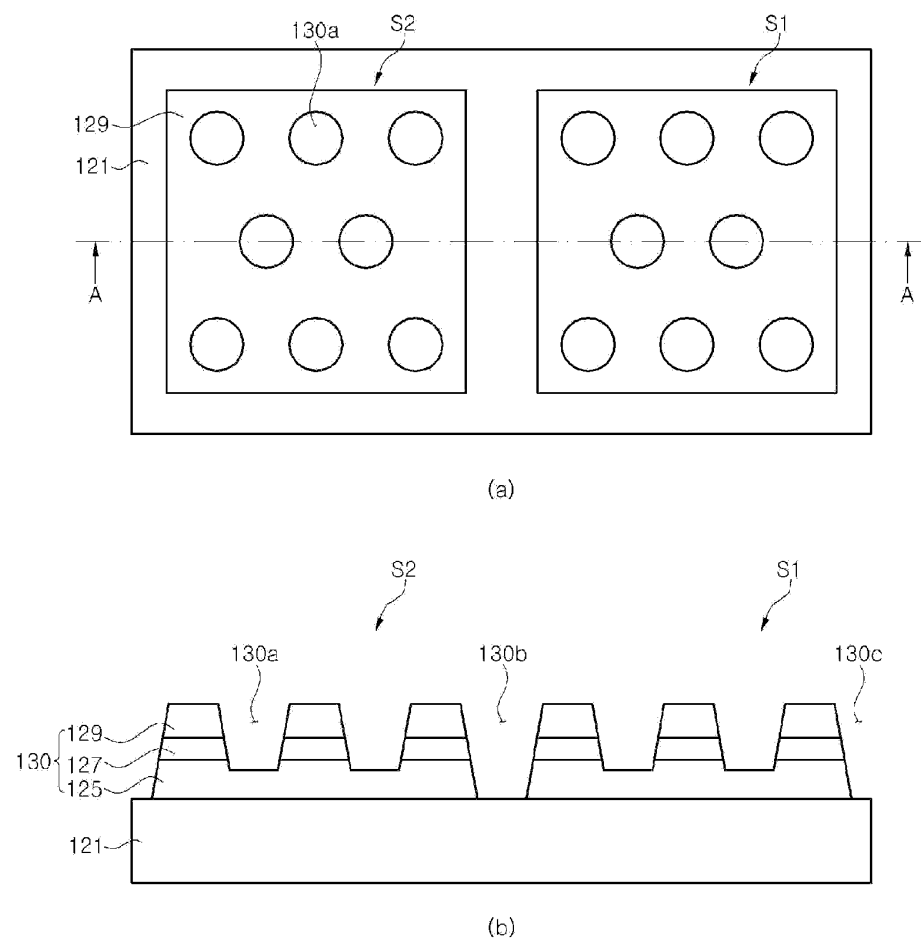


Figure 19

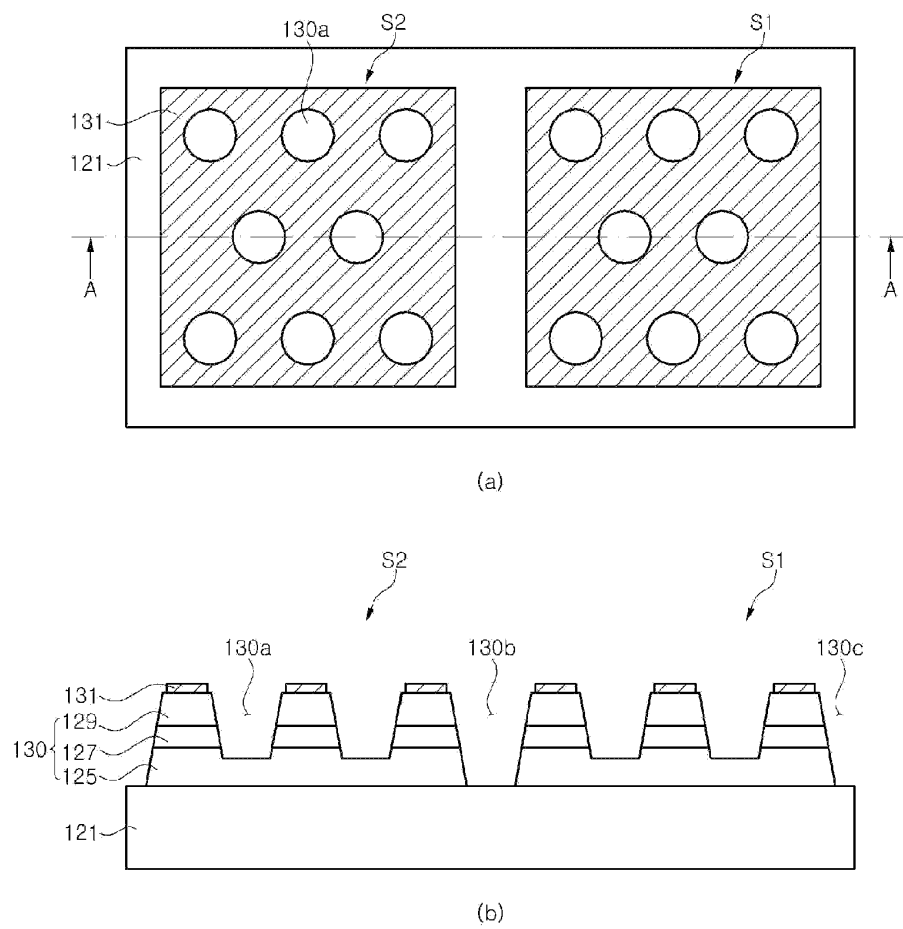


Figure 20

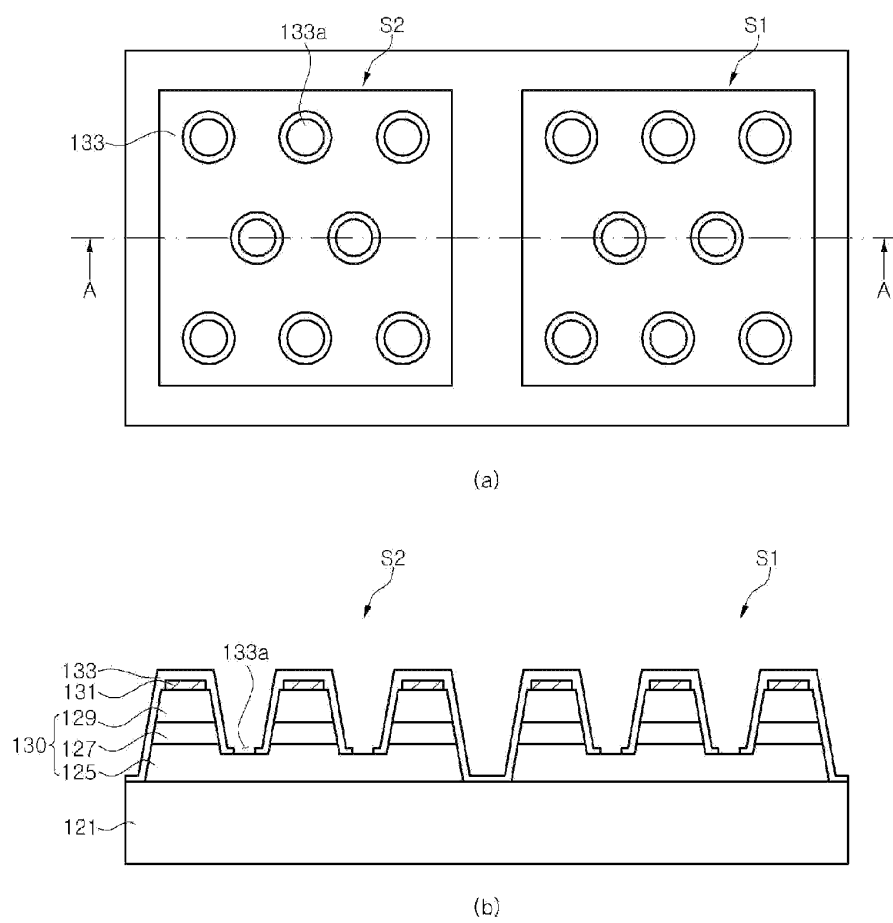


Figure 21

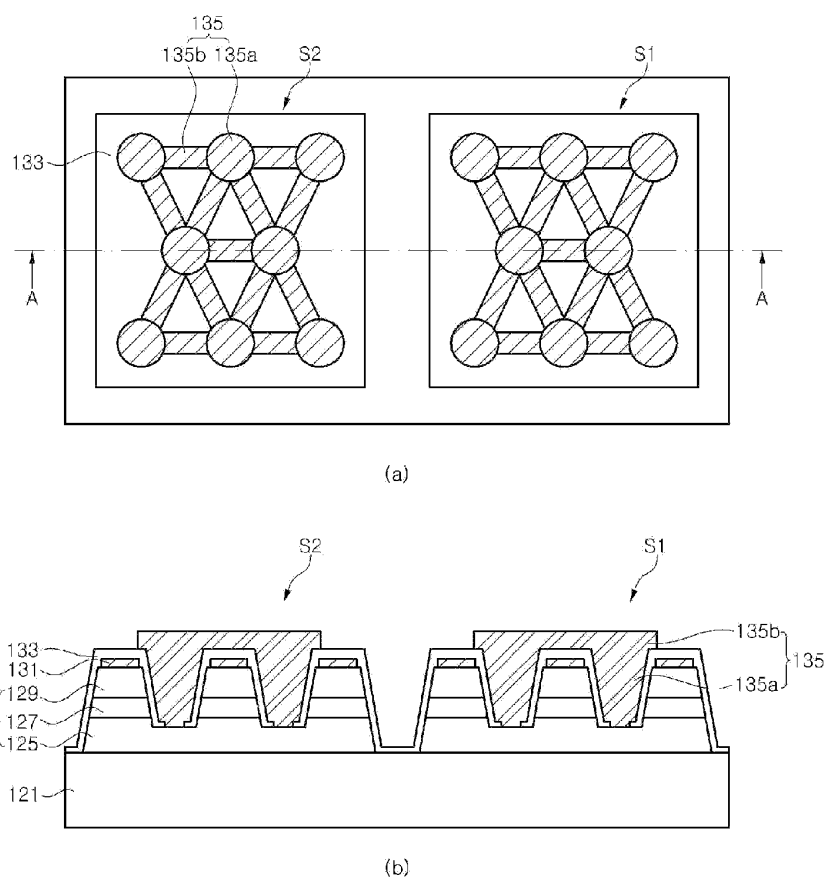


Figure 22

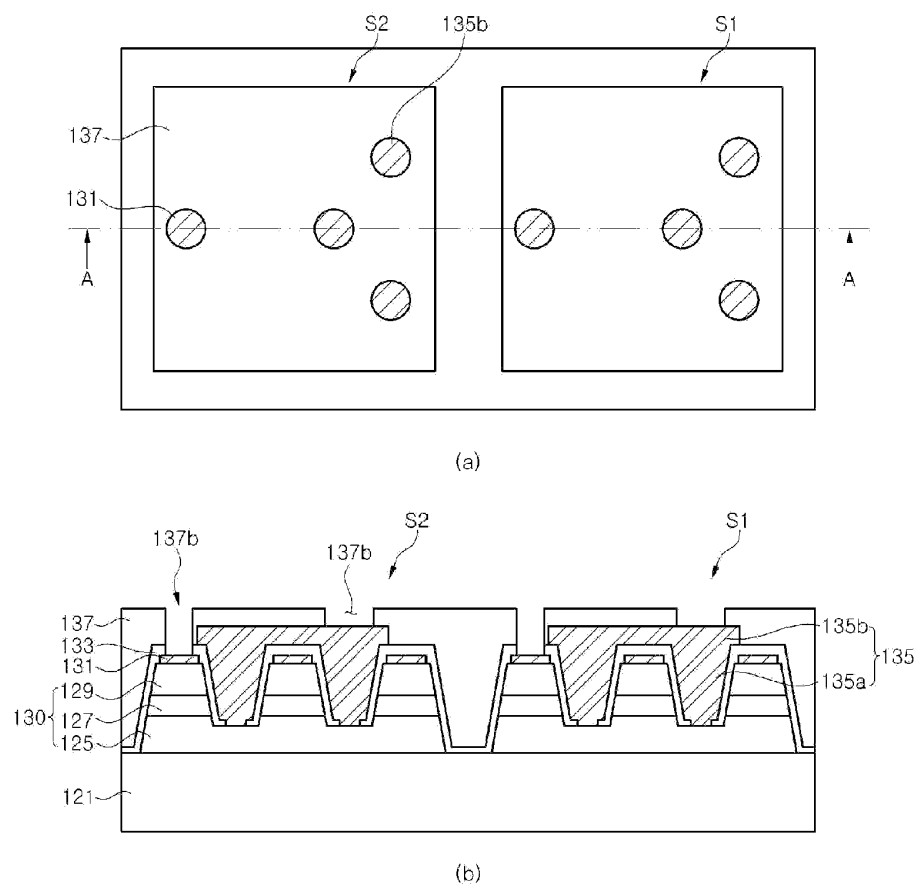


Figure 23

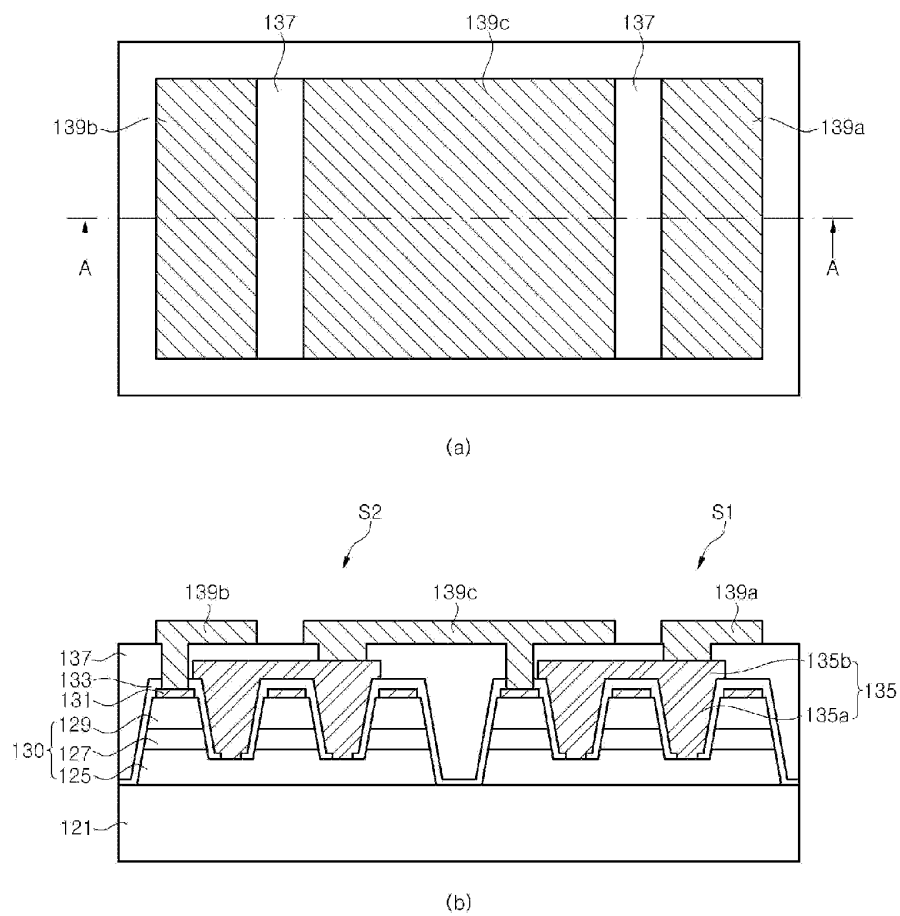


Figure 26

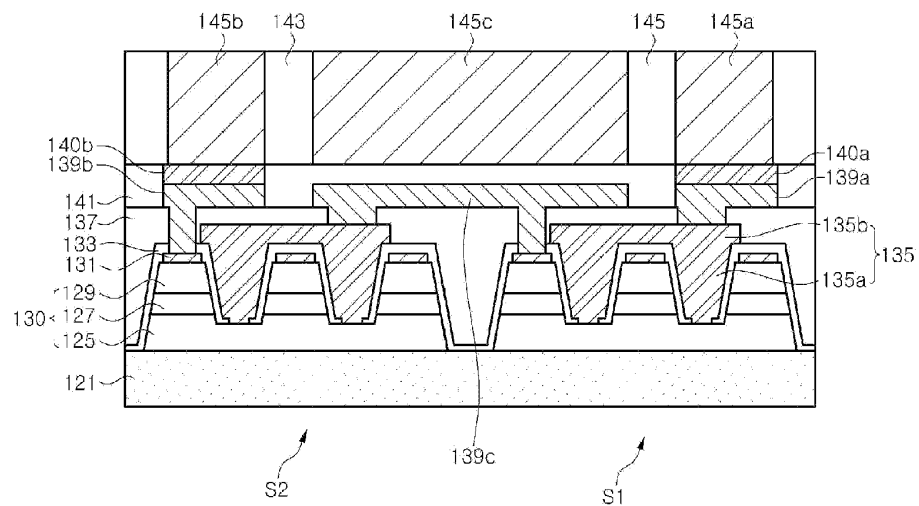
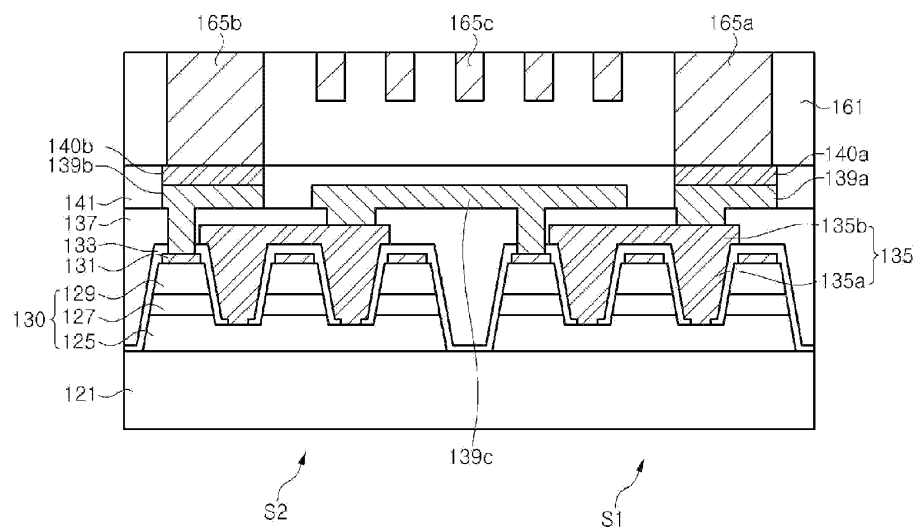


Figure 27



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WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from and the benefit of Korean Patent Application No. 10-2010-0092807, filed on Sep. 24, 2010, and Korean Patent Application No. 10-2010-0092808, filed on Sep. 24, 2010, which are hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a light emitting diode package and a method of fabricating the same and, more particularly, to a wafer-level light emitting diode package and a method of fabricating the same.

2. Description of the Background

A light emitting diode (LED) is a semiconductor device that includes an N-type semiconductor and a P-type semiconductor, and emits light through recombination of holes and electrons. Such an LED has been used in a wide range of applications such as display devices, traffic lights, and back-light units. Further, considering the potential merits of lower power consumption and longer lifespan than existing electric bulbs or fluorescent lamps, the application range of LEDs has been expanded to general lighting by replacing existing incandescent lamps and fluorescent lamps.

The LED may be used in an LED module. The LED module is manufactured through a process of fabricating an LED chip at a wafer level, a packaging process, and a modulation process. Specifically, semiconductor layers are grown on a substrate such as a sapphire substrate, and subjected to a wafer-level patterning process to fabricate LED chips having electrode pads, followed by division into individual chips (chip fabrication process). Then, after mounting the individual chips on a lead frame or a printed circuit board, the electrode pads are electrically connected to lead terminals via bonding wires, and the LED chips are covered by a molding member, thereby providing an LED package (packaging process). Then, the LED package is mounted on a circuit board such as a metal core printed circuit board (MC-PCB), thereby providing an LED module such as a light source module (modulation process).

In the packaging process, a housing and/or the molding member may be provided to the LED chip to protect the LED chip from the external environment. In addition, a phosphor may be contained in the molding member to convert light emitted by the LED chip so that the LED package may emit a white light, thereby providing a white LED package. Such a white LED package may be mounted on the circuit board such as the MC-PCB and a secondary lens may be provided to the LED package to adjust orientation characteristics of light emitted from the LED package, thereby providing a desired white LED module.

However, it may be difficult to achieve miniaturization and satisfactory heat dissipation of the conventional LED package including the lead frame or printed circuit board. Furthermore, luminous efficiency of the LED may be deteriorated due to absorption of light by the lead frame or the printed circuit board, electric resistance heating by the lead terminals, and the like.

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In addition, the chip fabrication process, the packaging process, and the modulation process may be separately carried out, thereby increasing time and costs for manufacturing the LED module.

Meanwhile, alternating current (AC) LEDs have been produced and marketed. The AC LED includes an LED directly connected to an AC power source to permit continuous emission of light. One example of AC LEDs, which can be used by being directly connected to a high voltage AC power source, is disclosed in U.S. Pat. No. 7,417,259, issued to Sakai, et. al.

According to U.S. Pat. No. 7,417,259, LED elements are arranged in a two-dimensional pattern on an insulating substrate, for example, a sapphire substrate, and are connected in series to form LED arrays. The LED arrays are connected in series to each other, thereby providing a light emitting device that can be operated at high voltage. Further, such LED arrays may be connected in reverse parallel to each other on the sapphire substrate, thereby providing a single-chip light emitting device that can be operated to continuously emit light using an AC power supply.

Since the AC-LED includes light emitting cells on a growth substrate, for example, on a sapphire substrate, the AC-LED restricts the structure of the light emitting cells and may limit improvement of light extraction efficiency. Thus, investigation has been made into a light emitting diode, for example, an AC-LED that is based on a substrate separation process and includes light emitting cells connected in series to each other.

SUMMARY OF THE INVENTION

Exemplary embodiments of the invention provide a wafer-level LED package and a method of fabricating the same, which can be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board.

Exemplary embodiments of the invention also provide a wafer-level LED package and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

Exemplary embodiments of the invention also provide a method of fabricating an LED package, which may reduce manufacturing time and cost of an LED module.

Exemplary embodiments of the invention also provide an LED module and a method of fabricating the same, which has high efficiency and exhibits improved heat dissipation.

Exemplary embodiments of the invention also provide a wafer-level light emitting diode package and a method of fabricating the same, which includes a plurality of light emitting cells and may be directly formed in a module on a circuit board without using a conventional lead frame or printed circuit board.

Additional features of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention.

An exemplary embodiment of the present invention discloses an LED package including: a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer; a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes; a second bump arranged on the first side of the semiconductor stack, the second bump being electrically con-

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nected to the second conductive type semiconductor layer; and a protective insulation layer covering a sidewall of the semiconductor stack.

An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package according to the aforementioned exemplary embodiments. The LED module may include a circuit board; the LED package mounted on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

An exemplary embodiment of the present invention also discloses a method of fabricating an LED package. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of contact holes exposing the first conductive type semiconductor layer; forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region; and forming a first bump and a second bump on the semiconductor stack. The first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes, and the second bump is electrically connected to the second conductive type semiconductor layer.

An exemplary embodiment of the present invention also discloses a light emitting diode package. The LED package includes a plurality of light emitting cells each including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer; a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer of each of the light emitting cells, the contact holes exposing the first conductive type semiconductor layer thereof; a protective insulation layer covering a sidewall of each of the light emitting cells; a connector located arranged on a first side of the light emitting cells and electrically connecting two adjacent light emitting cells to each other; a first bump arranged on the first side of the light emitting cells and electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells; and a second bump arranged in the first side of the light emitting cells and electrically connected to the second conductive type semiconductor layer of a second light emitting cell of the light emitting cells.

An exemplary embodiment of the present invention also discloses a light emitting diode module including the LED package described above. The module includes a circuit board; the LED package arranged on the circuit board; and a lens to adjust an orientation angle of light emitted from the LED package.

An exemplary embodiment of the present invention also discloses a method of fabricating an LED package including a plurality of light emitting cells. The method includes forming a semiconductor stack including a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer on a first substrate; patterning the semiconductor stack to form a chip separation region and a light emitting cell separation region; patterning the second conductive type semiconductor layer and the active layer to form a plurality of light emitting cells, each light emitting cell having a plurality of contact holes exposing the first conductive type semiconductor layer; forming a protective insulation layer covering a sidewall of the semiconductor stack in the chip separation region and the light emitting cell separation region; forming a connector connecting adjacent light emit-

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ting cells in series to each other; and forming a first bump and a second bump on the plurality of light emitting cells. Here, the first bump is electrically connected to the first conductive type semiconductor layer via the plurality of contact holes of a first light emitting cell of the light emitting cells, and the second bump is electrically connected to the second conductive type semiconductor layer of a second light emitting cell of the light emitting cells.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the principles of the invention.

FIG. 1 is a schematic sectional view of a light emitting diode package according to a first exemplary embodiment of the invention.

FIG. 2 is a schematic sectional view of a light emitting diode package according to a second exemplary embodiment of the invention.

FIG. 3 is a sectional view of a light emitting diode module including the light emitting diode package according to the first exemplary embodiment.

FIG. 4 to FIG. 12 show a method of fabricating the light emitting diode package according to the first exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in FIG. 5 to FIG. 10.

FIG. 13 is a sectional view showing a method of fabricating the light emitting diode package according to the second exemplary embodiment of the invention.

FIG. 14 is a schematic sectional view of a light emitting diode package according to a third exemplary embodiment of the invention.

FIG. 15 is a schematic sectional view of a light emitting diode package according to a fourth exemplary embodiment of the invention.

FIG. 16 is a sectional view of a light emitting diode module including the light emitting diode package according to the third exemplary embodiment.

FIG. 17 to FIG. 26 show a method of fabricating the light emitting diode package according to the third exemplary embodiment, in which (a) is a plan view and (b) is a sectional view taken along line A-A of (a) in FIG. 18 to FIG. 23.

FIG. 27 is a sectional view showing a method of fabricating the light emitting diode package according to the fourth exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough and will fully convey the scope of the invention to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions

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may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

FIG. 1 is a schematic sectional view of an LED package 100 according to a first exemplary embodiment of the invention.

Referring to FIG. 1, the LED package 100 may include a semiconductor stack 30, a first contact layer 35, a second contact layer 31, a first insulation layer 33, a second insulation layer 37, a first electrode pad 39a, a second electrode pad 39b, a first bump 45a, and a second bump 45b. The LED package 100 may further include an insulation layer 43, a dummy bump 45c, and a wavelength convertor 51.

The semiconductor stack 30 includes a first conductive type upper semiconductor layer 25, an active layer 27, and a second conductive type lower semiconductor layer 29. The active layer 27 is interposed between the upper and lower semiconductor layers 25, 29.

The active layer 27 and the upper and lower semiconductor layers 25, 29 may be composed of a III-N based compound semiconductor, for example, (Al, Ga, In)N semiconductor. Each of the upper and lower semiconductor layers 25, 29 may be a single layer or multiple layers. For example, the upper and/or lower semiconductor layers 25, 29 may include a super lattice layer in addition to a contact layer and a clad layer. The active layer 27 may have a single quantum well structure or a multi-quantum well structure. The first conductive type may be an n-type and the second conductive type may be a p-type. Alternatively, the first conductive type may be a p-type and the second conductive type may be an n-type. Since the upper semiconductor layer 25 can be formed of an n-type semiconductor layer having relatively low specific resistance, the upper semiconductor layer 25 may have a relatively high thickness. Therefore, a roughened surface R may be formed on an upper surface of the upper semiconductor layer 25, in which the roughened surface R enhances extraction efficiency of light generated in the active layer 27.

The semiconductor stack 30 has a plurality of contact holes 30a (see FIG. 5(b)) formed through the second conductive type lower semiconductor layer 29 and the active layer 27 to expose the first conductive type upper semiconductor layer, and the first contact layer 35 contacts the first conductive type upper semiconductor layer 25 exposed in the plurality of contact holes.

The second contact layer 31 contacts the second conductive type lower semiconductor layer 29. The second contact layer 31 includes a reflective metal layer to reflect light generated in the active layer 27. Further, the second contact layer 31 may form an ohmic contact with the second conductive type lower semiconductor layer 29.

The first insulation layer 33 covers the second contact layer 31. Further, the first insulation layer 33 covers a sidewall of the semiconductor stack 30 exposed in the plurality of contact holes 30a. In addition, the first insulation layer 33 may cover a side surface of the semiconductor stack 30. The first insulation layer 33 insulates the first contact layer 35 from the second contact layer 31 while insulating the second conductive type lower semiconductor layer 29 and the active layer 27 exposed in the plurality of contact holes 30a from the first contact layer 35. The first insulation layer 33 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation

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layer 33 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$.

The first contact layer 35 is located under the first insulation layer 33 and contacts the first conductive type upper semiconductor layer 25 through the first insulation layer 33 in the plurality of contact holes 30a. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25, and a connecting section 35b connecting the contact sections 35a to each other. Therefore, the contact sections 35a are electrically connected to each other by the connecting section 35b. The first contact layer 35 is formed under some regions of the first insulation layer 33 and may be composed of a reflective metal layer.

The second insulation layer 37 covers the first contact layer 35 under the first contact layer 35. In addition, the second insulation layer 37 covers the first insulation layer 33 while covering a side surface of the semiconductor stack 30. The second insulation layer 37 may be composed of a single layer or multiple layers. Further, the second insulation layer 37 may be a distributed Bragg reflector.

The first and second electrode pads 39a, 39b are located under the second insulation layer 37. The first electrode pad 39a may be connected to the first contact layer 35 through the second insulation layer 37. Further, the second electrode pad 39b may be connected to the second contact layer 31 through the second insulation layer 37 and the first insulation layer 33.

The first bump 45a and the second bump 45b are located under the first and second electrode pads 39a, 39b to be connected thereto, respectively. The first and second bumps 45a, 45b may be formed by plating. The first and second bumps 45a, 45b are terminals electrically connected to a circuit board such as an MC-PCB and have coplanar distal ends. In addition, the first electrode pad 39a may be formed at the same level as that of the second electrode pad 39b, so that the first bump 45a and the second bump 45b may also be formed on the same plane. Therefore, the first and second bumps 45a, 45b may have the same height.

Meanwhile, the dummy bump 45c may be located between the first bump 45a and the second bump 45b. The dummy bump 45c may be formed together with the first and second bumps 45a and 45b to provide a heat passage for discharging heat from the semiconductor stack 30.

The insulation layer 43 may cover side surfaces of the first and second bumps 45a, 45b. The insulation layer 43 may also cover a side surface of the dummy bump 45c. In addition, the insulation layer 43 fills spaces between the first bump 45a, the second bump 45b and the dummy bump 45c to prevent moisture from entering the semiconductor stack 30 from outside. The insulation layer 43 also covers side surfaces of the first and second electrode pads 39a, 39b to protect the first and second electrode pads 39a, 39b from external environmental factors such as moisture. Although the insulation layer 43 may be configured to cover the overall side surfaces of the first and second bumps 45a, 45b, the invention is not limited thereto. Alternatively, the insulation layer 43 may cover the side surfaces of the first and second bumps 45a, 45b except for some regions of the side surface near distal ends of the first and second bumps.

In the present exemplary embodiment, the insulation layer 43 is illustrated as covering the side surfaces of the first and second electrode pads 39a and 39b, but the invention is not limited thereto. Alternatively, another insulation layer may be used to cover the first and second electrode pads 39a, 39b and the insulation layer 43 may be formed under the other insulation layer. In this case, the first and second bumps 45a, 45b

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may be connected to the first and second electrode pads **39a**, **39b** through the other insulation layer.

The wavelength converter **51** may be located on the first conductive type upper semiconductor layer **25** opposite to the rest of the semiconductor stack **30**. The wavelength converter **51** may contact an upper surface of the first conductive type upper semiconductor layer **25**. The wavelength converter **51** may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength converter **51** may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength conversion.

In the present exemplary embodiment, the side surface of the semiconductor stack **30** is covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer **33** and/or the second insulation layer **37**. In addition, the first contact layer **35** may be covered with the second insulation layer **37** to be protected from an external environment and the second contact layer **31** may be covered with the first insulation layer **33** and the second insulation layer **37** to be protected from an external environment. The first and second electrode pads **39a**, **39b** are also protected by, for example, the insulation layer **43**. Accordingly, it is possible to prevent deterioration of the semiconductor stack **30** due to moisture.

The wavelength converter **51** may be attached to the first conductive type upper semiconductor layer **25** at a wafer-level, and then divided together with the protective insulation layer during a chip separation process. Therefore, a side surface of the wavelength converter **51** may be in a line with the protective insulation layer. That is, the side surface of the wavelength converter **51** may be flush along a straight line with a side surface of the protective insulation layer. Further, the side surface of the wavelength converter **51** may be in a line with a side surface of the insulation layer **43**. Thus, the side surfaces of the wavelength converter **51**, the protective insulation layer, and the insulation layer **43** may all be flush along a straight line.

FIG. 2 is a schematic sectional view of a light emitting diode package **200** according to a second exemplary embodiment of the invention.

Referring to FIG. 2, the LED package **200** is similar to the LED package **100** according to the above exemplary embodiment. In the present exemplary embodiment, however, first and second bumps **65a**, **65b** are formed in a substrate **61**.

Specifically, the substrate **61** includes through-holes, which have the first and second bumps **65a**, **65b** formed therein, respectively. The substrate **61** is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto. The substrate **61** having the first and second bumps **65a**, **65b** may be attached to a first electrode pad **39a** and a second electrode pad **39b**. In this case, to prevent the first and second electrode pads **39a**, **39b** from being exposed to the outside, an insulation layer **49** may cover side surfaces and bottom surfaces of the first and second electrode pads **39a**, **39b**. Further, the insulation layer **49** may have openings, which expose the first and second electrode pads **39a**, **39b**, and additional metal layers **67a**, **67b** are then formed in the openings. The additional metal layers **67a**, **67b** may be composed of a bonding metal.

FIG. 3 is a sectional view of a light emitting diode module including the LED package **100** according to the first exemplary embodiment.

Referring to FIG. 3, the LED module includes a circuit board **71**, for example, an MC-PCB, the LED package **100**, and a lens **81**. The circuit board **71**, for example, the MC-PCB, has connection pads **73a**, **73b** for mounting the LED

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packages **100** thereon. The first and second bumps **45a**, **45b** (see FIG. 1) of the LED package **100** are connected to the connection pads **73a**, **73b**, respectively.

A plurality of LED packages **100** may be mounted on the circuit board **71** and the lens **81** may be disposed on the LED packages **100** to adjust an orientation angle of light emitted from the LED packages **100**.

In accordance with the second exemplary embodiment, the light emitting diode packages **200** may be mounted on the circuit board instead of the LED packages **100**.

FIG. 4 to FIG. 12 show a method of fabricating the LED package **100** according to the first exemplary embodiment. In FIG. 5 to FIG. 10, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

Referring to FIG. 4, a semiconductor stack **30**, which includes a first conductive type semiconductor layer **25**, an active layer **27** and a second conductive type semiconductor layer **29**, is formed on a growth substrate **21**. The growth substrate **21** may be a sapphire substrate but is not limited thereto. Alternatively, the growth substrate **21** may be another kind of heterogeneous substrate, for example, a silicon substrate. Each of the first and second conductive type semiconductor layers **25**, **29** may be composed of a single layer or multiple layers. Further, the active layer **27** may have a single-quantum well structure or multi-quantum well structure.

The compound semiconductor layers may be formed of III-N based compound semiconductor on the growth substrate **21** by metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE).

A buffer layer (not shown) may be formed before forming the compound semiconductor layers. The buffer layer is formed to relieve lattice mismatch between the growth substrate **21** and the compound semiconductor layers and may be formed of a GaN-based material layer such as gallium nitride or aluminum nitride.

Referring to (a) and (b) of FIG. 5, the semiconductor stack **30** is patterned to form a chip (package) separation region **30b** while patterning the second conductive type semiconductor layer **29** and the active layer **27** to form a plurality of contact holes **30a** exposing the first conductive type semiconductor layer **25**. The semiconductor stack **30** may be patterned by photolithography and etching processes.

The chip separation region **30b** is a region for dividing the LED package structure into individual LED packages and side surfaces of the first conductive type semiconductor layer **25**, the active layer **27** and the second conductive type semiconductor layer **29** are exposed on the chip separation region **30b**. Advantageously, the chip separation region **30b** may be configured to expose the substrate **21** without being limited thereto.

The plurality of contact holes **30a** may have a circular shape, but is not limited thereto. The contact holes **30a** may have a variety of shapes. The second conductive type semiconductor layer **29** and the active layer **27** are exposed to sidewalls of the plurality of contact holes **30a**. As shown, the contact holes **30a** may have slanted sidewalls.

Referring to (a) and (b) of FIG. 6, a second contact layer **31** is formed on the second conductive type semiconductor layer **29**. The second contact layer **31** is formed on the semiconductor stack **30** except for regions corresponding to the plurality of contact holes **30a**.

The second contact layer **31** may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al). The second contact layer **31** may be composed of a single layer or multiple layers. The second contact layer **31** may also

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be configured to form an ohmic contact with the second conductive type semiconductor layer 29.

The second contact layer 31 may be formed before or after formation of the plurality of contact holes 30a.

Referring to (a) and (b) of FIG. 7, a first insulation layer 33 is formed to cover the second contact layer 31. The first insulation layer 33 may cover the side surface of the semiconductor stack 30 exposed to the chip separation region 30b while covering the sidewalls of the plurality of contact holes 30a. Here, the first insulation layer 33 may have openings 33a, which expose the first conductive type semiconductor layer 25 in the plurality of contact holes 30a.

The first insulation layer 33 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the first insulation layer 33 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction. For example, the first insulation layer 33 may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$. Further, the first insulation layer 33 may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

Referring to (a) and (b) of FIG. 8, a first contact layer 35 is formed on the first insulation layer 33. The first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25 exposed in the contact holes 30a, and a connecting section 35b connecting the contact sections 35a to each other. The first contact layer 35 may be composed of a reflective metal layer, but is not limited thereto.

The first contact layer 35 is formed on some regions of the semiconductor stack 30, so that the first insulation layer 33 is exposed on other regions of the semiconductor stack 30 where the first contact layer 35 is not formed.

Referring to (a) and (b) of FIG. 9, a second insulation layer 37 is formed on the first contact layer 35. The second insulation layer 37 may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Further, the second insulation layer 37 may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

The second insulation layer 37 may cover the first contact layer 35 while covering the first insulation layer 33. The second insulation layer 37 may also cover the side surface of the semiconductor stack 30 in the chip separation region 30b.

The second insulation layer 37 has an opening 37a which exposes the first contact layer 35. Further, the second insulation layer 37 and the first insulation layer 33 are formed with an opening 37b, which exposes the second contact layer 31.

Referring to (a) and (b) of FIG. 10, first and second electrode pads 39a, 39b are formed on the second insulation layer 37. The first electrode pad 39a is connected to the first contact layer 35 through the opening 37a and the second electrode pad 39b is connected to the second contact layer 31 through the opening 37b.

The first electrode pad 39a is separated from the second electrode pad 39b and each of the first and second electrode pads 39a, 39b may have a relatively large area from a top perspective, for example, an area not less than $\frac{1}{3}$ of the area of the LED package.

Referring to FIG. 11, an insulation layer 43 is formed on the first and second electrode pads 39a, 39b. The insulation layer 43 covers the first and second electrode pads 39a, 39b and has grooves which expose upper surfaces of the electrode pads 39a, 39b. Further, the insulation layer 43 may have a

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groove which exposes the second insulation layer 37 between the first and second electrode pads 39a, 39b.

Then, first and second bump 45a, 45b are formed in the grooves of the insulation layer 43, and a dummy bump 45c may be formed between the first bump and the second bump.

The bumps may be formed by plating, for example, electroplating, using a metallic material. If necessary, a seed layer for plating may also be formed.

After the first and second bumps 45a, 45b are formed, the insulation layer 43 may be removed. For example, the insulation layer 43 may be formed of a polymer such as photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer 43 may remain to protect the side surfaces of the first and second bumps 45a, 45b.

In the present exemplary embodiment, the insulation layer 43 is illustrated as being directly formed on the first and second electrode pads 39a, 39b. In other exemplary embodiments, another insulation layer may be formed to cover the first and second electrode pads 39a, 39b. The other insulation layer may be configured to have openings exposing the first and second electrode pads 39a, 39b. Then, the processes of forming the insulation layer 43 and the bumps may be carried out.

Referring to FIG. 12, the growth substrate 21 is removed and a wavelength converter 51 is attached to the first conductive type semiconductor layer 25. The growth substrate 21 may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

Then, the exposed surface of the first conductive type semiconductor layer 25 is subjected to anisotropic etching such as photoelectrochemical (PEC) etching to form a roughened surface on the exposed first conductive type semiconductor layer 25.

Meanwhile, the wavelength converter such as a phosphor sheet containing phosphors may be attached to the first conductive type semiconductor layer 25.

Alternatively, the growth substrate 21 may contain an impurity for converting a wavelength of light generated in the active layer 27. In this case, the growth substrate 21 may be used as the wavelength converter 51.

Then, the LED package structure is divided into individual packages along the chip separation region 30b, thereby providing finished LED packages 100. At this time, the second insulation layer 37 is cut together with the wavelength converter 51 so that cut planes thereof can be formed in a line.

FIG. 13 is a sectional view showing a method of fabricating the LED package 200 according to the second exemplary embodiment of the present invention.

Referring to FIG. 13, in the method of fabricating the LED package 200 according to the present exemplary embodiment, the processes until the first and second electrode pads 39a, 39b are formed are the same as those of the method of fabricating the LED package 100 described above (FIGS. 10 (a) and (b)).

After the first and second electrode pads 39a, 39b are formed, an insulation layer 49 is formed to cover the first and second electrode pads 39a, 39b. The insulation layer 49 may cover side surfaces of the first and second electrode pads 39a, 39b to protect the first and second electrode pads 39a, 39b. The insulation layer 49 has openings which expose the first and second electrode pads 39a, 39b. Additional metal layers 67a, 67b are then formed in the openings. The additional metal layers 67a, 67b may be composed of a bonding metal.

The substrate 61 is bonded to the first and second electrode pads 39a, 39b. The substrate 61 may have through-holes, in which the first and second bumps 65a, 65b may be formed. Further, the first and second bumps may be formed at distal

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ends thereof with pads **69a**, **69b**. The substrate **61** having the first and second bumps **65a**, **65b** and the pads **69a**, **69b** may be separately prepared and bonded to a wafer having the first and second electrode pads **39a**, **39b**.

Then, as described with reference to FIG. **12**, the growth substrate **21** is removed and a wavelength convertor **51** may be attached to the first conductive type semiconductor layer **25**, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages **200** as described in FIG. **2** are provided.

FIG. **14** is a sectional view of an LED package **300** according to a third exemplary embodiment of the present invention.

Referring to FIG. **14**, the LED package **300** may include a semiconductor stack **130**, which is divided into a plurality of light emitting cells (only two light emitting cells **S1**, **S2** are shown herein), a first contact layer **135**, a second contact layer **131**, a first insulation layer **133**, a second insulation layer **137**, a first electrode pad **139a**, a second electrode pad **139b**, a connector **139c** connecting adjacent light emitting cells to each other in series, a first bump **145a** and a second bump **145b**. Further, the LED package **300** may include a third insulation layer **141**, an insulation layer **143**, a dummy bump **145c**, a wavelength convertor **151**, and additional metal layers **140a**, **140b**.

The semiconductor stack **130** includes a first conductive type upper semiconductor layer **125**, an active layer **127**, and a second conductive type lower semiconductor layer **129**. The semiconductor stack **130** of the present exemplary embodiment is similar to the semiconductor stack **30** described in FIG. **1**, and a detailed description thereof will be omitted herein.

Each of the light emitting cells **S1**, **S2** has a plurality of contact holes **130a** (see FIG. **18(b)**) extending through the second conductive type lower semiconductor layer **129** and the active layer **127** to expose the first conductive type upper semiconductor layer, and the first contact layer **135** contacts the first conductive type upper semiconductor layer **125** exposed in the plurality of contact holes. The light emitting cells **S1**, **S2** are separated from each other by a cell separation region **130b** (see FIG. **18(b)**).

The second contact layer **131** contacts the second conductive type lower semiconductor layer **129** of each of the light emitting cells **S1**, **S2**. The second contact layer **131** includes a reflective metal layer to reflect light generated in the active layer **127**. Further, the second contact layer **131** may form an ohmic contact with the second conductive type lower semiconductor layer **129**.

The first insulation layer **133** covers the second contact layer **131**. Further, the first insulation layer **133** covers a sidewall of the semiconductor stack **130** exposed in the plurality of contact holes **130a**. In addition, the first insulation layer **133** may cover a side surface of each of the light emitting cells **S1**, **S2**. The first insulation layer **133** insulates the first contact layer **135** from the second contact layer **131** while insulating the second conductive type lower semiconductor layer **129** and the active layer **127** exposed in the plurality of contact holes **130a** from the first contact layer **135**. The first insulation layer **133** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Furthermore, the first insulation layer **133** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction, for example, $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$.

The first contact layer **135** is located under the first insulation layer **133** and contacts the first conductive type upper semiconductor layer **125** through the first insulation layer **133** in the plurality of contact holes **130a** in each of the light

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emitting cells **S1**, **S2**. The first contact layer **135** includes contact sections **135a** contacting the first conductive type upper semiconductor layer **125**, and a connecting section **135b** connecting the contact sections **135a** to each other. Therefore, the contact sections **135a** are electrically connected to each other by the connecting section **135b**. The first contact layers **135** located under the respective light emitting cells **S1**, **S2** are separated from each other and formed under some regions of the first insulation layer **133**. The first contact layer **135** may be composed of a reflective metal layer.

The second insulation layer **137** covers the first contact layer **135** under the first contact layer **135**. In addition, the second insulation layer **137** may cover the first insulation layer **133** while covering the side surface of each of the light emitting cells **S1**, **S2**. The second insulation layer **137** may be composed of a single layer or multiple layers. Alternatively, the second insulation layer **137** may be composed of a distributed Bragg reflector.

The first electrode pad **139a** and the second electrode pad **139b** are located under the second insulation layer **137**. The first electrode pad **139a** may be connected to the first contact layer **135** of a first light emitting cell **S1** through the second insulation layer **137**. Further, the second electrode pad **139b** may be connected to the second contact layer **131** of a second light emitting cell **S2** through the second insulation layer **137** and the first insulation layer **133**.

The connector **139c** is located under the second insulation layer **137** and electrically connects two adjacent light emitting cells **S1**, **S2** to each other through the second insulation layer **137**. The connector **139c** may connect the second contact layer **131** of one light emitting cell **S1** to the first contact layer **135** of another light emitting cell **S2** adjacent thereto, so that the two light emitting cells **S1**, **S2** are connected in series to each other.

In the present exemplary embodiment, two light emitting cells **S1**, **S2** are illustrated. However, it should be understood that two or more light emitting cells may be connected in series to each other by a plurality of connectors **139c**. Here, the first and second electrode pads **139a**, **139b** may be connected in series to the light emitting cells **S1**, **S2** located at opposite ends of such series array.

Meanwhile, the third insulation layer **141** may cover the first electrode pad **139a**, the second electrode pad **139b** and the connector **139c** under the first electrode pad **139a**, the second electrode pad **139b** and the connector **139c**. The third insulation layer **141** may have an opening exposing the first electrode pad **139a** and the second electrode pad **139b**. The third insulation layer **141** may be formed of a silicon oxide or silicon nitride film.

The first bump **145a** and the second bump **145b** are located under the first and second electrode pads **139a**, **139b**, respectively. The first and second bumps **145a**, **145b** may be formed by plating. The first and second bumps **145a**, **145b** are terminals electrically connected to a circuit board such as an MC-PCB and have distal ends coplanar with each other. In addition, the first electrode pad **139a** may be formed at the same level as that of the second electrode pad **139b**, so that the first bump **145a** and the second bump **145b** may also be formed on the same plane. Therefore, the first and second bumps **145a**, **145b** may have the same height.

The additional metal layers **140a**, **140b** may be interposed between the first bump **145a** and the first electrode pad **139a** and between the second bump **145b** and the second electrode pad **139b**. Here, the additional metal layers **140a**, **140b** are provided to form the first and second electrode pads **139a**, **139b** to be higher than the connector **139c** and may be located inside openings of the third insulation layer **141**. The first and

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second electrode pads **139a**, **139b** and the additional metal layers **140a**, **140b** may constitute final electrode pads.

Meanwhile, the dummy bump **145c** may be located between the first bump **145a** and the second bump **145b**. The dummy bump **145c** may be formed together with the first and second bump **145a**, **145b** to provide a heat passage for discharging heat from the light emitting cells **S1**, **S2**. The dummy bump **145c** is separated from the connector **139c** by the third insulation layer **141**.

The insulation layer **143** may cover side surfaces of the first and second bumps **145a**, **145b**. The insulation layer **143** may also cover a side surface of the dummy bump **145c**. In addition, the insulation layer **143** fills spaces between the first bump **145a**, the second bump **145b** and the dummy bump **145c** to prevent moisture from entering the semiconductor stack **130** from outside. Although the insulation layer **143** may be configured to cover the overall side surfaces of the first and second bumps **145a**, **145b**, the invention is not limited thereto. Alternatively, the insulation layer **143** may cover the side surfaces of the first and second bumps **145a**, **145b** except for some regions of the side surface near distal ends of the first and second bumps.

The wavelength convertor **151** may be located on the light emitting cells **S1**, **S2**. The wavelength convertor **151** may contact an upper surface of the first conductive type upper semiconductor layer **125**. The wavelength convertor **151** also covers a cell separation region **130b** and a chip separation region. The wavelength convertor **151** may be a phosphor sheet having a uniform thickness without being limited thereto. Alternatively, the wavelength convertor **151** may be a substrate, for example, a sapphire substrate or a silicon substrate, which is doped with an impurity for wavelength conversion.

In the present embodiment, the side surfaces of the light emitting cells **S1**, **S2** are covered with a protective insulation layer. The protective insulation layer may include, for example, the first insulation layer **133** and/or the second insulation layer **137**. In addition, the first contact layer **135** may be covered with the second insulation layer **137** to be protected from external environment and the second contact layer **131** may be covered with the first insulation layer **133** and the second insulation layer **137** to be protected from external environment. Further, the first and second electrode pads **139a**, **139b** are also protected by, for example, the third insulation layer **141**. Accordingly, it is possible to prevent deterioration of the light emitting cells **S1**, **S2** due to moisture.

The wavelength convertor **151** may be attached to the first conductive type upper semiconductor layer **125** at a wafer-level, and then divided together with the protective insulation layer during a chip separation process (or package separation process). Therefore, a side surface of the wavelength convertor **151** may be in a line with the protective insulation layer. Further, the side surface of the wavelength convertor **151** may be in a line with a side surface of the insulation layer **143**.

FIG. 15 is a schematic sectional view of a light emitting diode package **400** according to a fourth exemplary embodiment of the present invention.

Referring to FIG. 15, the LED package **400** is similar to the LED package **300** according to the above exemplary embodiment. In present exemplary embodiment, however, first and second bumps **165a**, **165b** are formed in a substrate **161**.

Specifically, the substrate **161** includes through-holes, which have the first and second bumps **165a**, **165b** formed therein, respectively. The substrate **161** is an insulation substrate, for example, a sapphire substrate or a silicon substrate, but is not limited thereto.

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The substrate **161** having the first and second bumps **165a**, **165b** may be attached to a third insulation layer **141**, and the first and second bumps **165a**, **165b** may be connected to first and second electrode pads **139a**, **139b**, respectively. Here, the first and second bumps **165a**, **165b** may be bonded to additional metal layers **140a**, **140b**, respectively.

FIG. 16 is a sectional view of a light emitting diode module including the LED packages **300** according to the third exemplary embodiment on a circuit board.

Referring to FIG. 16, the LED module includes a circuit board **171**, for example, an MC-PCB, the LED package **300**, and a lens **181**. The circuit board **171**, for example, the MC-PCB, has connection pads **173a**, **173b** for mounting the LED packages **300** thereon. The first and second bumps **145a**, **145b** (see FIG. 14) of the LED package **300** are connected to the connection pads **173a**, **173b**, respectively.

A plurality of LED packages **300** may be mounted on the circuit board **171** and the lens **181** may be disposed on the LED packages **300** to adjust an orientation angle of light emitted from the LED packages **300**.

In other exemplary embodiments, instead of the LED packages **300**, the light emitting diode packages **400** may be mounted on the circuit board.

FIG. 17 to FIG. 25 show a method of fabricating the LED package **300** according to the third exemplary embodiment. In FIG. 18 to FIG. 23, (a) is a plan view and (b) is a sectional view taken along line A-A of (a).

Referring to FIG. 17, a semiconductor stack **130**, which includes a first conductive type semiconductor layer **125**, an active layer **127** and a second conductive type semiconductor layer **129**, is formed on a growth substrate **121**. The growth substrate **121** and the semiconductor stack **130** are similar to the substrate **21** and the semiconductor stack **30** described with reference to FIG. 4, and a detailed description thereof will thus be omitted herein.

Referring to (a) and (b) of FIG. 18, the semiconductor stack **130** is patterned to form a chip (package) separation region **130c** and a cell separation region **130b** while patterning the second conductive type semiconductor layer **129** and the active layer **127** to form light emitting cells **S1**, **S2**, each having a plurality of contact holes **130a** exposing the first conductive type semiconductor layer **125**. The semiconductor stack **130** may be patterned by photolithography and etching processes.

The chip separation region **130c** is a region for dividing the LED package structure into individual LED packages and side surfaces of the first conductive type semiconductor layer **125**, the active layer **127** and the second conductive type semiconductor layer **129** are exposed at the chip separation region **130c**. Advantageously, the chip separation region **130c** and the cell separation region **130b** may be configured to expose the substrate **121** without being limited thereto.

The plurality of contact holes **130a** may have a circular shape, but is not limited thereto. The contact holes **130a** may have a variety of shapes. The second conductive type semiconductor layer **129** and the active layer **127** are exposed to sidewalls of the plurality of contact holes **130a**. The contact holes **130a** may have slanted sidewalls.

Referring to (a) and (b) of FIG. 19, a second contact layer **131** is formed on the second conductive type semiconductor layer **129**. The second contact layer **131** is formed on the semiconductor stack **130** in each of the light emitting cells **S1**, **S2** except for regions corresponding to the plurality of contact holes **130a**.

The second contact layer **131** may include a transparent conductive oxide film such as indium tin oxide (ITO) or a reflective metal layer such as silver (Ag) or aluminum (Al).

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The second contact layer **131** may be composed of a single layer or multiple layers. The second contact layer **131** may also be configured to form an ohmic contact with the second conductive type semiconductor layer **129**.

The second contact layer **131** may be formed before or after the formation of the plurality of contact holes **130a**

Referring to (a) and (b) of FIG. **20**, a first insulation layer **133** is formed to cover the second contact layer **131**. The first insulation layer **133** may cover the side surface of each of the light emitting cells **S1**, **S2** while covering the sidewalls of the plurality of contact holes **130a**. Here, the first insulation layer **133** may have openings **133a**, which expose the first conductive type semiconductor layer **125** in the plurality of contact holes **130a**.

The first insulation layer **133** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. In addition, the first insulation layer **133** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction. For example, the first insulation layer **133** may be formed by alternately stacking $\text{SiO}_2/\text{TiO}_2$ or $\text{SiO}_2/\text{Nb}_2\text{O}_5$. Further, the first insulation layer **133** may be formed to provide a distributed Bragg reflector having high reflectivity over a wide wavelength range of blue, green, and red light by adjusting the thickness of each of the insulation layers.

Referring to (a) and (b) of FIG. **21**, a first contact layer **135** is formed on the first insulation layer **133**. The first contact layer **135** is formed on each of the light emitting cells **S1**, **S2**, and includes contact sections **35a** contacting the first conductive type upper semiconductor layer **125** exposed in the contact holes **130a** and a connecting section **135b** connecting the contact sections **135a** to each other. The first contact layer **135** may be composed of a reflective metal layer, but is not limited thereto.

The first contact layer **135** is formed on some regions of each of the light emitting cells **S1**, **S2**, so that the first insulation layer **133** is exposed at other regions of the semiconductor stack **130** where the first contact layer **135** is not formed.

Referring to (a) and (b) of FIG. **22**, a second insulation layer **137** is formed on the first contact layer **135**. The second insulation layer **137** may be composed of a single layer or multiple layers, such as a silicon oxide or silicon nitride film. Alternatively, the second insulation layer **137** may be composed of a distributed Bragg reflector, which is formed by alternately stacking insulation layers having different indices of refraction.

The second insulation layer **137** may cover the first contact layer **135** while covering the first insulation layer **133**. The second insulation layer **137** may also cover the side surface of each of the light emitting cells **S1**, **S2**. In addition, the second insulation layer **137** may fill in the chip separation region **130c** and the cell separation region **130b**.

The second insulation layer **137** has an opening **137a** which exposes the first contact layer **135** of each of the light emitting cells **S1**, **S2**. Further, the second insulation layer **137** and the first insulation layer **133** are formed with an opening **137b**, which exposes the second contact layer **131**.

Referring to (a) and (b) of FIG. **23**, a connector **139c** and first and second electrode pads **139a**, **139b** are formed on the second insulation layer **137**. The first electrode pad **139a** is connected to the first contact layer **135** of a first light emitting cell **S1** through the opening **137a** and the second electrode pad **139b** is connected to the second contact layer **131** of a second light emitting cell **S2** through the opening **137b**. Further, the connector **139c** connects the first contact layer **135**

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and the second contact layer **131** of adjacent light emitting cells **S1**, **S2** to each other in series through the openings **137a**, **137b**.

Referring to FIG. **24**, a third insulation layer **141** is formed on the first and second electrode pads **139a**, **139b** and the connector **139c**. The third insulation layer **141** covers the first and second electrode pads **139a**, **139b** and the connector **139c**, and has grooves which expose upper surfaces of the electrode pads **139a**, **139b**. Meanwhile, the third insulation layer **141** may have additional metal layers **140a**, **140b** formed in the grooves thereof. The additional metal layers **140a**, **140b** increase the height of the electrode pads **139a**, **139b**, such that final electrode pads may have a greater height than the connector **139c**. The additional metal layers **140a**, **140b** may be formed before the formation of the third insulation layer **141**. Upper surfaces of the additional metal layers **140a**, **140b** may be substantially coplanar with an upper surface of the third insulation layer **141**.

Referring to FIG. **25**, a patterned insulation layer **143** is formed on the third insulation layer **141**. The patterned insulation layer **143** has grooves, which expose the upper side of the first and second electrode pads **139a**, **139b**, for example, the additional metal layers **140a**, **140b**. Further, the patterned insulation layer **143** may have a groove exposing the third insulation layer **141** between the first electrode pad **139a** and the second electrode pad **139b**.

Then, first and second bumps **145a**, **145b** are formed in the grooves of the insulation layer **143** and a dummy bump **145c** may be formed between the first and second bumps.

The bumps may be formed by plating, for example, electroplating. As needed, a seed layer for plating may also be formed.

After the first and second bumps **145a**, **145b** are formed, the insulation layer **143** may be removed. For example, the insulation layer **143** may be formed of a polymer such as photoresist and may be removed after the bumps are formed. Alternatively, the insulation layer **143** may remain to protect the side surfaces of the first and second bumps **145a**, **145b**.

Referring to FIG. **26**, the growth substrate **121** is removed and a wavelength converter **151** is attached to the light emitting cells **S1**, **S2**. The growth substrate **21** may be removed by an optical technique such as laser lift-off (LLO), mechanical polishing or chemical etching.

Then, the exposed surface of the first conductive type semiconductor layer **125** is subjected to anisotropic etching such as PEC etching to form a roughened surface on the exposed first conductive type semiconductor layer **125**.

Meanwhile, the wavelength converter **151**, such as a phosphor sheet containing phosphors, may be attached to the first conductive type semiconductor layer **125**.

Alternatively, the growth substrate **121** may contain an impurity for converting a wavelength of light generated in the active layer **127**. In this case, the growth substrate **121** may be used as the wavelength converter **151**.

Then, the LED package structure is divided into individual packages along the chip separation region **130c**, thereby providing finished LED packages **300**. At this time, the second insulation layer **137** is cut together with the wavelength converter **151** so that cut planes thereof can be formed in a line.

FIG. **27** is a sectional view explaining a method of fabricating the LED package **400** according to the fourth exemplary embodiment of the invention.

Referring to FIG. **27**, in the method of fabricating the LED package **400** according to this embodiment, the processes until the third insulation layer **141** and the additional metal

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layers **140a**, **1140b** are formed are the same as those of the method of fabricating the LED package **300** described above (FIG. **24**).

In the present exemplary embodiment, the substrate **161** is bonded to the third insulation layer **141**. The substrate **161** may have through-holes, in which the first and second bumps **165a**, **165b** may be formed. Further, the first and second bumps **165a**, **165b** may be formed at distal ends thereof with pads (not shown). In addition, the substrate **161** may have grooves partially formed on a lower surface thereof and filled with a metallic material **165c**. The metallic material **165c** improves substrate heat dissipation.

Alternatively, the substrate **161** having the first and second bumps **165a**, **165b** may be separately prepared and bonded to a wafer having the first and second electrode pads **139a**, **139b**. The first and second bumps **165a**, **165b** may be electrically connected to first and second electrode pads **139a**, **139b**, respectively.

Then, as described with reference to FIG. **26**, the growth substrate **121** is removed and the wavelength converter **151** may be attached to the light emitting cells **S1**, **S2**, followed by division of the LED package structure into individual LED packages. As a result, the finished LED packages **400** as described in FIG. **15** are provided.

As such, the exemplary embodiments of the invention provide wafer-level LED packages which can be directly formed on a circuit board for a module without using a conventional lead frame or printed circuit board. Accordingly, the LED package may have high efficiency and exhibit improved heat dissipation while reducing time and cost for fabrication of the LED package. In addition, an LED module having the LED package mounted thereon may have high efficiency and exhibit improved heat dissipation.

Further, the LED package may include a plurality of light emitting cells connected in series to each other and arrays connected in reverse parallel to each other. Further, the plurality of light emitting cells may be connected to a bridge rectifier and may be used to form a bridge rectifier. Therefore, the LED module including the LED package may be operated by AC power without a separate AC/DC converter.

Although the invention has been illustrated with reference to some exemplary embodiments in conjunction with the drawings, it will be apparent to those skilled in the art that various modifications and changes can be made to the invention without departing from the spirit and scope of the invention. Further, it should be understood that some features of a certain embodiment may also be applied to other embodiment without departing from the spirit and scope of the invention. Therefore, it should be understood that the embodiments are provided by way of illustration only and are given to provide complete disclosure of the invention and to provide thorough understanding of the invention to those skilled in the art. Thus, it is intended that the invention covers the modifications and variations provided they fall within the scope of the appended claims and their equivalents.

What is claimed is:

1. A light emitting diode (LED) package, comprising:
 - a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;
 - a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;

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a first bump arranged on a first side of the semiconductor stack, the first bump being electrically connected to the first conductive type semiconductor layer via the plurality of contact holes;

a second bump arranged on the first side of the semiconductor stack, the second bump being electrically connected to the second conductive type semiconductor layer; and

a protective insulation layer covering a sidewall of the semiconductor stack.

2. The LED package of claim 1, further comprising a wavelength converter arranged on a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack.

3. The LED package of claim 2, wherein the wavelength converter comprises a phosphor sheet or an impurity-doped single crystal substrate.

4. The LED package of claim 2, wherein the wavelength converter comprises a side surface flush with a side surface of the protective insulation layer.

5. The LED package of claim 1, wherein the protective insulation layer comprises a distributed Bragg reflector.

6. The LED package of claim 1, wherein the first conductive type semiconductor layer comprises a roughened surface.

7. The LED package of claim 1, further comprising an insulation layer arranged on side surfaces of the first bump and the second bump.

8. The LED package of claim 7, further comprising a dummy bump arranged between the first bump and the second bump.

9. The LED package of claim 1, further comprising a substrate comprising a first through-hole and a second through-hole, the first bump and the second bump being arranged in the first through-hole and the second through-hole, respectively.

10. The LED package of claim 9, wherein the substrate comprises sapphire or silicon.

11. The LED package of claim 1, further comprising:

a first contact layer comprising first contact sections contacting the first conductive type semiconductor layer in the plurality of contact holes and a connecting section connecting the first contact sections to each other; and a second contact layer contacting the second conductive type semiconductor layer,

wherein the protective insulation layer comprises a first insulation layer and a second insulation layer, the first insulation layer being arranged between the first contact layer and the second contact layer and covering the second contact layer, and the second insulation layer being arranged between the semiconductor stack and the first contact layer and covering the first contact layer, wherein the first bump is electrically connected to the first contact layer, and the second bump is electrically connected to the second contact layer.

12. The LED package of claim 11, further comprising: a first electrode pad contacting the first contact layer through a first contact hole arranged in the second insulation layer; and

a second electrode pad contacting the second contact layer through a second contact hole arranged in the second insulation layer and the first insulation layer, wherein the first bump and the second bump contact the first electrode pad and the second electrode pad, respectively.

13. The LED package of claim 11, wherein at least one of the first insulation layer and the second insulation layer comprises a distributed Bragg reflector.

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14. A light emitting diode (LED) module, comprising:
a circuit board;
the LED package of claim 1 arranged on the circuit board;
and
a lens to adjust an orientation angle of light emitted from the LED package.

15. The LED module of claim 14, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and a plurality of the LED packages is arranged on the MC-PCB.

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90/013,725	04/15/2016	257	3992	MT100		
RULE						
APPLICANTS INVENTORS 9070851, Residence Not Provided; SEOUL SEMICONDUCTOR CO., LTD. (ASSIGNEE), SEOUL, KOREA, REPUBLIC OF; ALAN TABOADA - MOSER TABOADA (3RD PTY REQ.), SHREWSBURY, NJ; ALAN TABOADA - MOSER TABOADA, SHREWSBURY, NJ ** CONTINUING DATA ***** This application is a REX of 13/194,317 07/29/2011 PAT 9070851 ** FOREIGN APPLICATIONS ***** REPUBLIC OF KOREA 10-2010-0092807 09/24/2010 REPUBLIC OF KOREA 10-2010-0092808 09/24/2010 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **						
Foreign Priority claimed ☐ Yes ☐ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged <u>Examiner's Signature</u>		☐ Met after Allowance <u>Initials</u>	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
					15	1
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TITLE Wafer-Level Light Emitting Diode Package and Method of Fabricating the Same						
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