

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Seo, et al.
U.S. Patent No.: 9,293,664 Attorney Docket No.: 38191-0005IP1
Issue Date: Mar. 22, 2016
Appl. Serial No.: 14/815,433
Filing Date: Jul. 31, 2015
Title: WAFER-LEVEL LIGHT EMITTING DIODE PACKAGE AND
METHOD OF FABRICATING THE SAME

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 9,293,664 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

LGI1001	U.S. Patent No. 9,293,664 to Seo, et al. (“the ’664 Patent”)
LGI1002	Declaration of Dr. Eric Bretschneider
LGI1003	Prosecution History of the ’664 Patent
LGI1004	Reexamination History of U.S. Patent No. 9,070,851
LGI1005	U.S. Patent Pub. No. 2010/0117111 to Illek et al. (“Illek”)
LGI1006	U.S. Patent No. 6,066,861 to Hohn et al. (“Hohn”)
LGI1007	U.S. Patent Pub. No. 2005/0194605 to Shelton et al. (“Shelton”)
LGI1008	U.S. Patent Pub. No. 2003/0021113 to Begemann (“Begemann”)
LGI1009	U.S. Patent Pub. No. 2009/0283787 to Donofrio et al. (“Donofrio”)
LGI1010	JP Publication JP 2009-88299 to Sano et al. (“Sano”)
LGI1011	Certified English Translation of Sano and Translator’s Declaration
LGI1012	U.S. Patent No. 6,693,352 to Huang et al. (“Huang”)
LGI1013	U.S. Patent No. 7,554,126 to Higashi et al. (“Higashi”)
LGI1014	Excerpt from ANSI/IES RP-16-10: Nomenclature and Definitions for Illuminating Engineering
LGI1015	U.S. Patent No. 6,448,657 to Dorleans (“Dorleans”)

LG Innotek Co. Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-19 (“the Challenged Claims”) of U.S. Patent No. 9,293,664 (“the ’664 Patent”).

I. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’664 Patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds in the table below, as explained in this Petition and the Declaration of Eric Bretschneider, Ph.D. *See, e.g.*, LGI1002, ¶¶ 1-227.

Ground	’664 Patent Claims	Basis for Rejection
Ground 1A	1-6, 8, 9, 11, 12	§102 over Illek
Ground 1B	1-6, 8-18	§103 over Illek
Ground 1C	7, 19	§103 over Illek and Begemann
Ground 2A	1-19	§103 over Donofrio and Sano
Ground 2B	19	§103 over Donofrio, Sano, and Begemann

Illek (LGI1005) published on May 13, 2010; Begemann (LGI1008) published on January 30, 2003; Donofrio (LGI1009) published on November 19,

2009, and Sano (LGI1010)¹ published on April 23, 2009. Thus, each qualify as prior art under at least 35 U.S.C. §102(b) because they were published over a year before the earliest actual filing date of the '664 Patent in the United States (Jul. 29, 2011).

Sano and Begemann do not appear on the face of the '664 Patent and were not considered during original examination of the '664 Patent.

Donofrio and Illek were among a large number of references that were cited by the Applicant during prosecution of the '664 Patent and that appear on the face of the '664 Patent; however, they were not applied or discussed by the Patent Office during prosecution. LGI1003. In fact, no rejections—involving these references or any others—were ever presented by the Office during prosecution. Moreover, as laid out in detail in this Petition, features of the '664 Patent that led to allowance are plainly taught by both Illek and Donofrio.

For at least these reasons, there is no basis for a determination under 35 U.S.C. § 325(d) that substantially similar prior art and/or arguments have already been presented to the Office. To be sure, the factors identified in the PTAB's *Becton, Dickinson and Company* decision (designated informative)

¹ Sano (LGI1010) was published in Japanese. Thus, all citations to Sano below will be to the certified English translation (LGI1011).

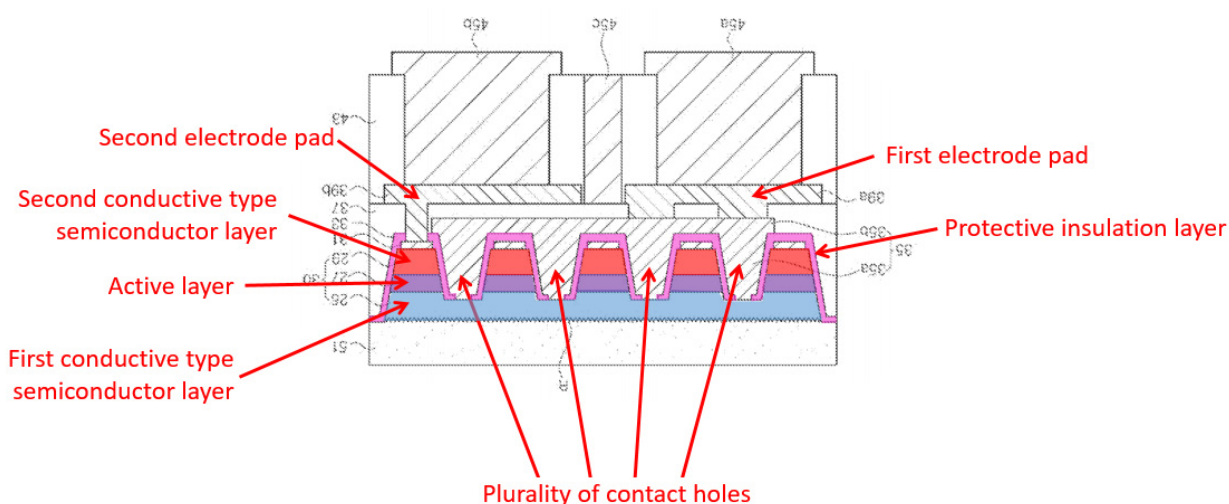
overwhelmingly weigh against such a finding. *See Dickinson and Company v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-28 (PTAB Dec. 15, 2017).

Further weighing against such a finding, the PTAB articulated several instances where § 325(d) consideration over previously-presented prior art are not appropriate, including—as is the case here—“where there are clear errors in the original prosecution,” “where the prior art at issue was only cursorily considered,” and where there are “changed claim constructions.” *Kayak Software Corp. v. IBM Corp.*, CBM2016-00075, Paper 16 at 11 (PTAB Dec. 15, 2016) (designated informative); *see also Digital Check Corp. d/b/a ST Imaging v. E-ImageData Corp.*, IPR2017-00178, Paper 6 at 12-13 (PTAB April 25, 2017) (declining to exercise discretion to deny institution under § 325(d) where prior art was cited in an IDS but there was no indication that the claims were rejected based on those references); *Pure Storage, Inc. v. Realtime Data LLC*, IPR2018-00549, Paper 7 at 11 (PTAB July 23, 2018) (declining to exercise discretion to deny institution under § 325(d) where “there is no evidence of record that [the prior art references] were substantively considered by the Examiner.”); *Synaptic Medical Inc. v. Karl Storz-Endoscopy-America, Inc.*, IPR2018-00462, Paper 6 at 10 (PTAB July 16, 2018) (declining to exercise discretion to deny institution under § 325(d) where references were listed on an information disclosure statement but otherwise “not applied to reject the claims.”).

II. BACKGROUND

A. Overview of the '664 Patent

The '664 Patent generally relates to a light emitting diode (LED) package/module that includes a semiconductor stack (a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer) and a plurality of contact holes in the semiconductor stack that expose the first conductive type semiconductor layer. *See* LGI1001 at Abstract. The '664 Patent further mentions that a protective insulation layer covers a sidewall of the semiconductor stack. *Id.* In order to make electrical connections to the first and second semiconductor layers, first and second electrode pads, respectively, are arranged over the semiconductor stack. *See id.*, Claim 1. An example of this configuration is illustrated below in FIG. 1 of the '664 Patent:



LGI1001, FIG. 1 (rotated, annotated); LGI1002, ¶¶38-41. Through this configuration, the '664 Patent alleges that LEDs “can be directly formed in a

module on a circuit board without using a conventional lead frame or printed circuit board.” LGI1001, 2:35-39.

The Challenged Claims of the '664 Patent further specify that the protective insulation layer, which covers the sidewall of the semiconductor stack, includes layers having different indices of refraction from each other. *See, e.g.*, LGI1001, Claims 1, 6, 12. However, as demonstrated by the art cited herein, LEDs having protective insulation layers with layers having different indices of refraction from each other were well-known in the prior art, including Illek and Donofrio. LGI1002, ¶¶42-43.

B. Prosecution History

1. Original Prosecution

The '664 Patent issued from U.S. Application No. 14/815,433 (“the '433 Application”), which was filed on July 31, 2015. The '433 Application was allowed on November 12, 2015, without having received any rejections from the examiner, and subsequently issued. *See generally* LGI1003. In the Notice of Allowance, the examiner stated that the prior art did not disclose, among other things, a “***protective insulation layer*** covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer, wherein the protective insulation layer includes insulation layers having different

indices of refraction from each other.” *Id.*, 14-20.² However, as will be detailed in this Petition, such insulation layers were well-known at the time of the ’664 Patent.

2. Reexamination of Related Application

U.S. Patent No. 9,070,851 (“the ’851 Patent”) issued from U.S. Application No. 13/194,317, which is a parent application to the ’664 Patent. The ’851 Patent was subject to an *ex parte* reexamination request filed on April 15, 2016, and subsequently granted on May 18, 2016. *See* LGI1004, 247-264, 428-556. In the Non-Final Office Action dated September 19, 2016, the Office rejected all claims under reexamination over various combinations involving the cited references. *See id.*, 111-137. Incidentally, among the numerous rejections, the Office indicated that the U.S. application corresponding to Donofrio anticipated most of the claims under reexamination. *See id.*, 125-130. In order to overcome Donofrio, the Patent Owner significantly narrowed the claims to recite “a protective insulation layer covering *each external side wall surface* of the semiconductor stack of each light emitting diode *facing externally* of the LED package *so that the protection insulation layer surrounds the LED package.*” *Id.*, 92. While these narrowing amendments formed the basis for patentability in the reexamination proceedings of the ’851 Patent, similar language is absent from the claims in the ’664 Patent, as illustrated in the table below. *See id.*, 5-12; LGI1002, ¶46.

² All emphasis added unless otherwise noted.

From Claim 1 of the '851 Patent	From Claim 1 of the '664 Patent
a protective insulation layer covering <i>each external side wall surface</i> of the semiconductor stack of each light emitting diode <i>facing externally</i> of the LED package <i>so that the protection insulation layer surrounds the LED package</i>	a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer

C. Claim Construction

Petitioner submits that all claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100; LGI1002, ¶¶32-33. Petitioner further submits that all claim terms should be given their plain meaning under the *Phillips* standard as detailed in the relevant sections below.

D. Level of Ordinary Skill

For purposes of this IPR, a person of ordinary skill in the art (POSITA) would have had at least a Bachelor of Science degree (or equivalent) in electrical engineering, physics, or a comparable field. LGI1002, ¶34. Additionally, a

POSITA would have had two or more (e.g. 2-5) years of experience in design and/or manufacturing of LED devices. *Id.*

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

As detailed below, Petitioner will prevail on the Challenged Claims. *See* LGI1002, ¶¶38-225.

A. [GROUND 1A]: Claims 1-6, 8, 9, 11, and 12 are anticipated by Illek

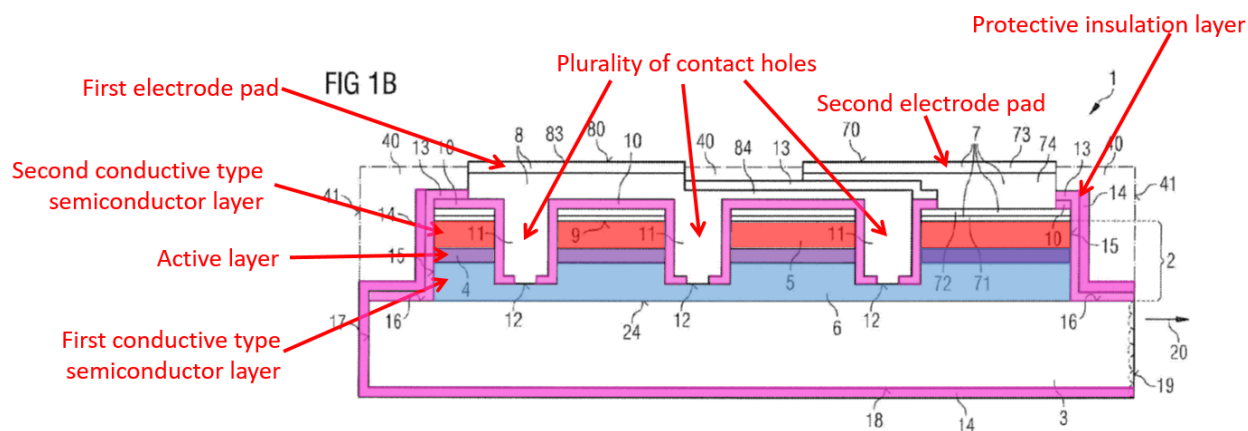
Overview of Illek

Illek is entitled “Optoelectronic Component and Method for Producing a Plurality of Optoelectronic Components” and is directed to “an LED component to emit incoherent radiation.” LGI1005 at Title, [0095]. In particular, Illek teaches “a light-emitting diode semiconductor body ... compris[ing] two regions 5, 6 having different types of conductivity (n-type or p-type)” and an “active region 4 ... formed between these regions 5 and 6.” *Id.*, [0085].

Illek’s LED further includes “a plurality of openings through the active region, through which the contact can extend from one side of the active region to the other side of the active region.” *Id.*, [0046]. Illek also teaches “two insulation layers 10 and 13” as well as a “mirror layer 14” that covers various surfaces of its LED component. *Id.*, [0120], [0128].

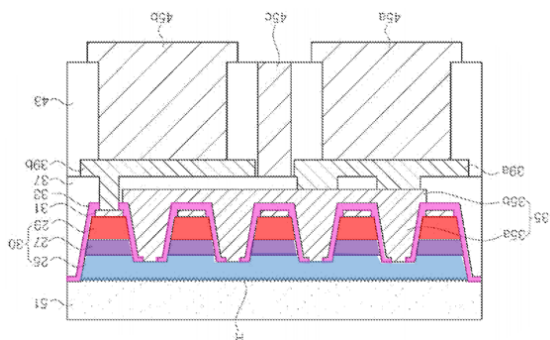
As for its mirror layer 14, Illek teaches that it can be a “multilayer structure comprising exclusively dielectric layers, in particular, a sequence of a large number of dielectric layer pairs having layers with different refractive indices arranged alternately in the multilayer structure....” *Id.*, [0131].

Thus, similar to the structure as claimed in the '664 Patent and as annotated below, Illek's LED component includes first and second conductive type semiconductor layers (*i.e.*, regions 6 and 5; shown in blue and red, respectively), an active layer (*i.e.*, active region 4, shown in purple), and a protective insulation layer (*i.e.*, layers 10, 13, and 14, shown in pink). LGI1002, ¶¶49-52. Illek also teaches, as shown below, a plurality of contact holes (*i.e.*, recesses 11) as well as first and second electrode pads (*i.e.*, contacts 8 and 7). *Id.*

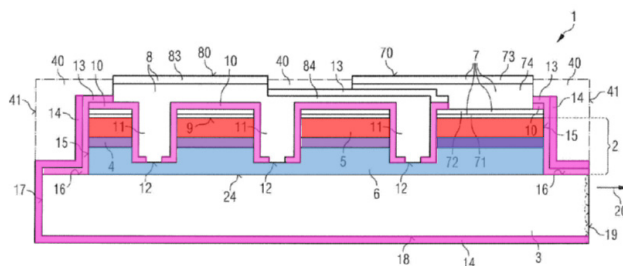


LGI1005, FIG. 1B (annotated).

Structural similarities between the LED components of the '664 Patent and Illek are highlighted through the side-by-side comparison below. LGI1002, ¶53.



Annotated FIG. 1 of '664 Patent



Anntoated FIG. 1B of Illek

Claim 1

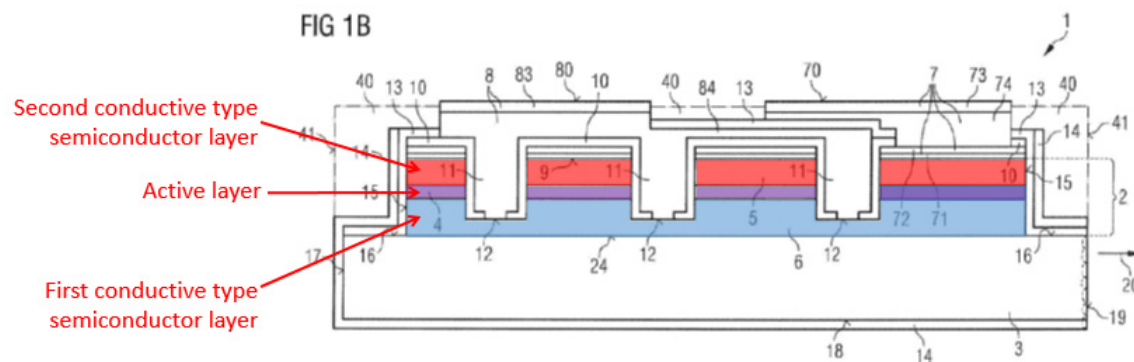
[1pre]: “A light emitting diode (LED) package, comprising:”

To the extent the preamble is limiting, which Petitioner does not concede, Illek discloses element [1pre]. LGI1002, ¶55. Specifically, Illek teaches that its “component 1...is designed to generate visible radiation” and further that this component is “designed as an **LED component** to emit incoherent radiation.” LGI1005, [0095]; *see also id.*, FIG. 1B, [0015] (“...the component is implemented as a light-emitting diode....”). LED **component** is simply another name for LED **package**, and the two terms may be used interchangeably. LGI1002, ¶55 (citing LGI1014).

[1a]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Illek discloses element [1a]. LGI1002, ¶¶56-57. Specifically, as shown in FIG. 1B, Illek’s LED includes a semiconductor body 2 that is made up of a first

conductive type semiconductor region 6 (blue), an active region 4 (purple), and a second conductive type semiconductor region 5 (red):



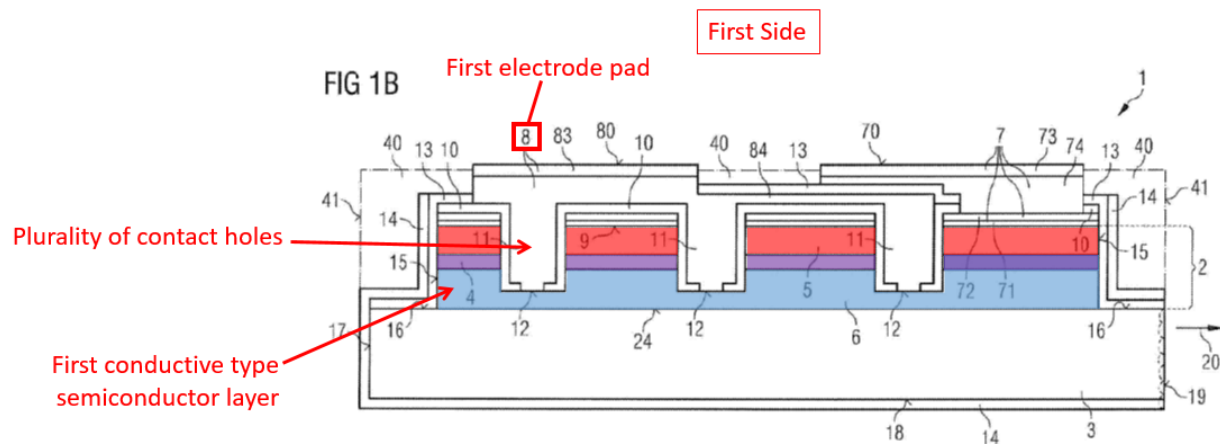
LGI1005, FIG. 1B (annotated); [0084]; [0089]; LGI1002, ¶¶56-57. Illek also teaches that the semiconductor regions 5 and 6 can be either n-type or p-type. LGI1005, [0085]; [0115].

[1b]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Illek discloses element [1b]. LGI1002, ¶¶58-60. In particular, Illek teaches that “[a]n ***opening may be formed through the active region in the semiconductor body***, through which opening the contact extends from one side of the active region to the other side of the active region....In particular, ***a plurality of openings through the active region*** can be provided, through which the contact can extend from one side of the active region to the other side of the active region.” LGI1005, [0046]. The “number of recesses 11” of Illek, which correspond to the claimed

[1c]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Illek discloses element [1c]. LGI1002, ¶¶61-63. For example, Illek teaches “contacts 7 and 8 [that] are electrically conductively connected to the semiconductor body 2,” with both contacts being “arranged on the side of the semiconductor body that faces away from the carrier 3.” LGI1005, [0096]-[0097]. More specifically, the “**second contact 8** is electrically conductively connected...**to the region 6** of the semiconductor body.” *Id.*, [0102]. And as illustrated below, the second contact 8 “extends through one or, preferably, through a number of [recesses 11] through the active region 4.”



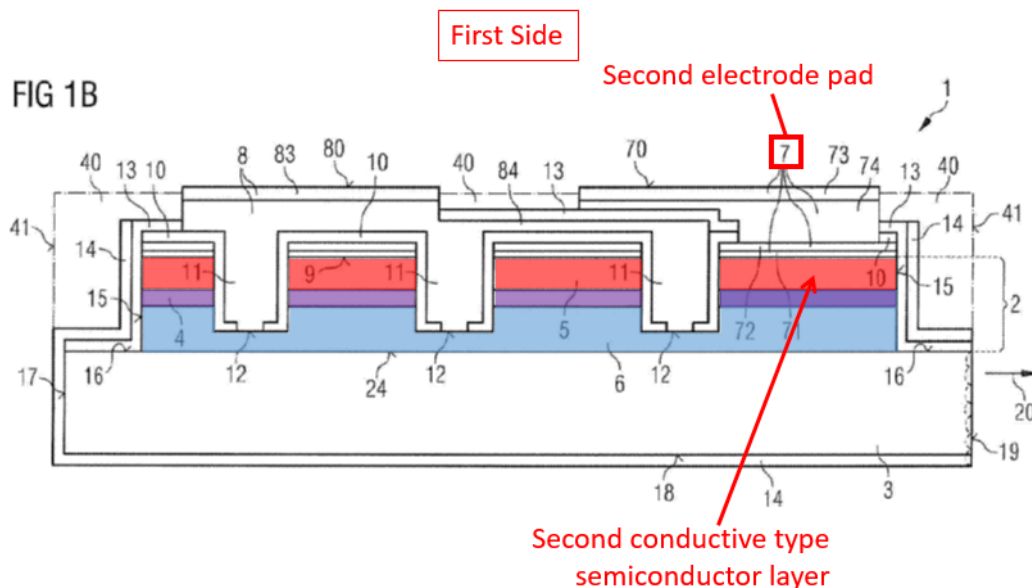
LGI1005, FIG. 1B (annotated); [0110]; LGI1002, ¶¶61-62.

Thus, the first electrode pad of Illek (*i.e.*, contact 8) is arranged over a first side of the semiconductor stack (*i.e.*, side that faces away from the carrier 3) and is further electrically connected to the first conductive type semiconductor layer (*i.e.*,

region 6) via some of the plurality of contact holes (*i.e.*, recesses 11). LGI1002, ¶¶61-63.

[1d]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

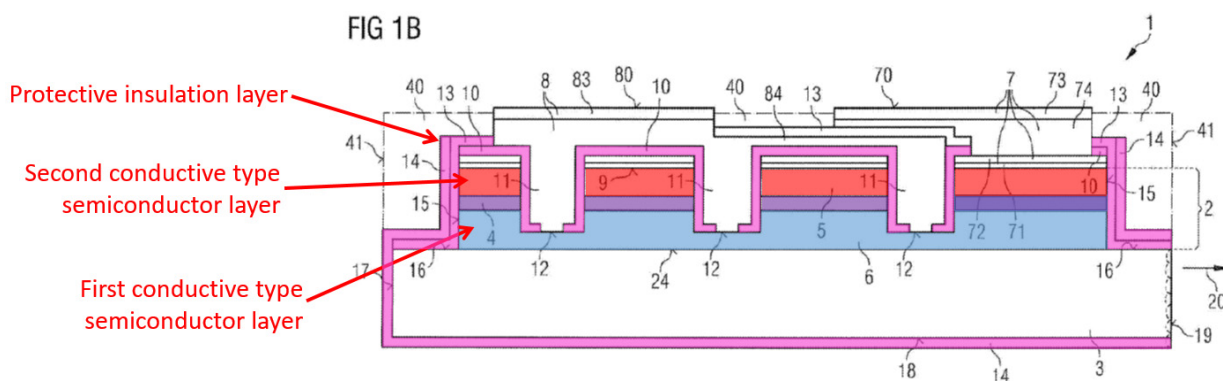
Illek discloses element [1d]. LGI1002, ¶¶64-65. For example, Illek teaches “contacts 7 and 8 [that] are electrically conductively connected to the semiconductor body 2,” with both contacts being “arranged on the side of the semiconductor body that faces away from the carrier 3.” LGI1005, [0096]-[0097]. More specifically, the “***first contact 7*** is electrically ***conductively connected...to the region 5*** of the semiconductor body.” *Id.*, [0102]; LGI1002, ¶64. Thus, as illustrated below, the second electrode pad of Illek (*i.e.*, contact 7) is arranged over a first side of the semiconductor stack (*i.e.*, side that faces away from the carrier 3) and is further electrically connected to the second conductive type semiconductor layer (*i.e.*, region 5):



LGI1005, FIG. 1B (annotated); LGI1002, ¶¶64-65.

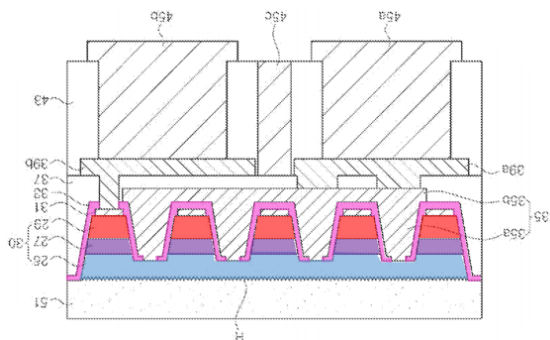
[1e]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”

Illek discloses element [1e]. LGI1002, ¶¶66-74. For example, as illustrated below, Illek teaches applying various insulation layers (shown in pink) on the sidewalls of the first and second semiconductor layers:

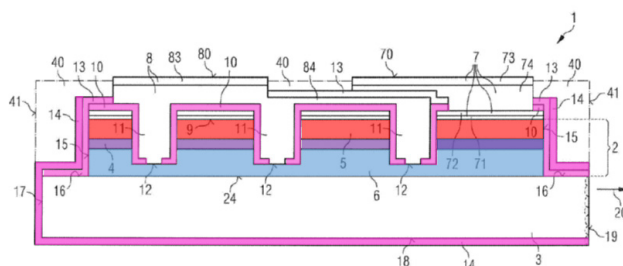


LGI1005, FIG. 1B (annotated); LGI1002, ¶¶66-69. Specifically, Illek teaches a *first insulation layer 10* and a *second insulation layer 13* that are applied on multiple faces and sidewalls of the LED as shown above. *See* LGI1005, [0109]-[0112]; [0120]. Insulation layers 10 and 13, which can be made from insulating materials such as “a silicon nitride such as SiN, a silicon oxide such as SiO₂, or a silicon oxynitride such as SiON,” are added to provide electrical insulation. *Id.*, [0112]; [0120]; LGI1002, ¶68. In addition to insulation layers 10 and 13, Illek further provides a *mirror layer 14* that is applied on various faces and sidewalls. *See* LGI1005, [0128]. The mirror layer 14 “can be implemented as a dielectric mirror” and also provides protective insulation. *Id.*, [0130]; LGI1002, ¶68. Thus, Illek teaches three insulation layers—first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14—that together provide the claimed protective insulation layer. LGI1002, ¶¶67-69. Indeed, the ’664 Patent explicitly mentions that the protective insulation layer can be made up of multiple layers as in Illek. *See* LGI1001, 7:16-29 (“The protective insulation layer may include, for example, the first insulation layer 33 and/or the second insulation layer 37.”), 6:1-7 (“The first insulation layer 33 may be composed of a single layer or *multiple layers*....”), 6:22-24 (“The second insulation layer 37 may be composed of a single layer or multiple layers.”); LGI1002, ¶67.

To wit, as demonstrated by the side-by-side comparison of the '664 Patent and Illek below, the protective insulation layer 33 of the '664 Patent (shown in pink) is structurally and functionally analogous to the layers 10/13/14 of Illek (also shown in pink). LGI1002, ¶¶69.



Annotated FIG. 1 of '664 Patent

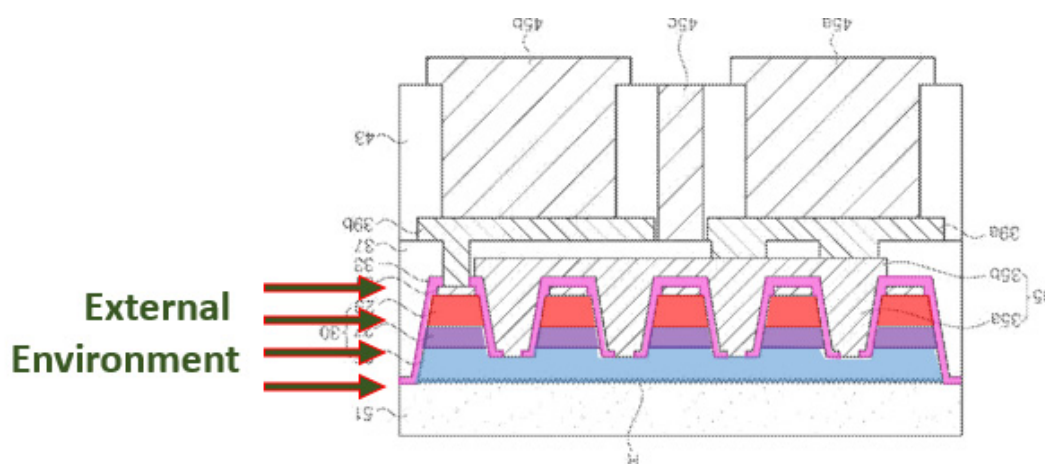


Anntoated FIG. 1B of Illek

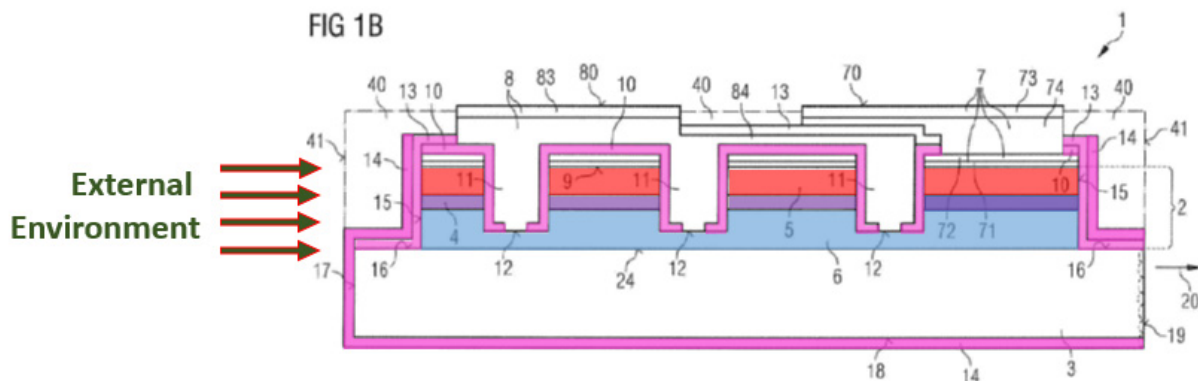
Additionally, because the layers 10/13/14 of Illek are materials that exhibit insulating characteristics and are deposited directly onto the semiconductor stack, they act as a protective outer layer that serves to passivate the underlying semiconductor material, thereby providing protection against undesirable effects such as metal diffusion into the semiconductor region. LGI1002, ¶¶70-71. The insulating layers 10/13/14 of Illek further serve to protect the contacts 7 and 8 from short-circuiting. LGI1005, [0109] (“In order to *avoid a short-circuit* between the contacts 7 and 8 on the connection side, the contacts are *electrically insulated* from one another on the connection side. A *first insulation layer 10*...insulates the second contact 8 on the connection side from the first contact 7 and, in particular,

insulates the second contact 8 from the surface 9 of the semiconductor body 2.”); LGI1002, ¶¶70-71.

Furthermore, to the extent that the “protective insulation layer” as claimed in the ’664 Patent requires some sort of protection from the external environment—a notion with which Petitioner does not agree—Illek’s insulating layers 10/13/14 nevertheless provide this aspect. LGI1002, ¶¶72-74. For example, as illustrated below, the ’664 Patent suggests that its protective insulation layer (pink) may be able to provide protection from “an external environment”:



LGI1001, FIG. 1 (annotated); 7:16-29; LGI1002, ¶72. Even under such narrow treatment of what it means for a layer to be “protective,” as shown below, the identified protective insulation layers 10/13/14 of Illek (pink) provide similar protection from the external environment by virtue of facing externally relative to, and surrounding, the LED package:



LGI1005, FIG. 1B (annotated); [0147]; LGI1002, ¶¶73-74. Thus, either alone or together with the optional encapsulation 40 (shown in ghost lines), the layers 10/13/14 of Illek provide protection from “external influences.” LGI1005, [0147]-[0148]; LGI1002, ¶¶72-74.

[1f]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”

Illek discloses element [1f]. LGI1002, ¶¶76-77. As discussed above for element [1e], the protective insulation layer of Illek includes a mirror layer 14. Moreover, Illek teaches that its mirror layer 14 “can be implemented as a multi-layer structure, *incorporating dielectric layers with different refractive indices*. The cold-light reflector may, in particular, be implemented as a *dielectric multi-layer structure*.” LGI1005, [0013]. Illek further teaches the mirror layer 14 can be “[a] multilayer structure comprising exclusively dielectric layers, in particular, *a sequence of a large number of dielectric layer pairs having layers with different refractive indices* arranged alternately in the multilayer structure.” *Id.*, [0131]. Accordingly, the mirror layer 14 of Illek is “a protective insulation layer [that]

includes insulation layers having different indices of refraction from each other.”

LGI1002, ¶¶76-77.

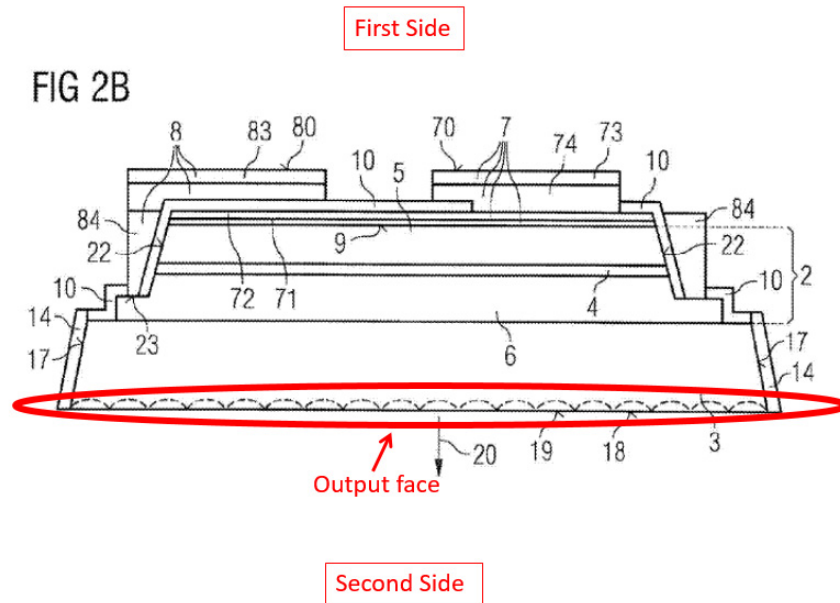
Claim 2

[2a]: “The LED package of claim 1, further comprising a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack,”

Illek discloses element [2a]. LGI1002, ¶¶78-80. For example, Illek teaches a wavelength convertor that can be located at its output face: “A further element can be applied to the output face 19 (not illustrated explicitly). ***A luminescence conversion layer, for instance, containing a conversion material, can be applied to the output face.*** This layer can absorb radiation that is generated in the active region and ***convert it into radiation with a greater wavelength.*** The two types of radiation can be mixed, so that radiation having a mixed color, e.g., white light, can be radiated from the side of the component that faces away from the luminescent conversion layer.” LGI1005, [0143]; LGI1002, ¶78.

Illek teaches that the output face can be positioned at any desired surface of the carrier 3 by “simply by not applying a mirror layer to the desired face.” LGI1005, [0142]; [0161]; LGI1002, ¶79. For example, Illek teaches that the output

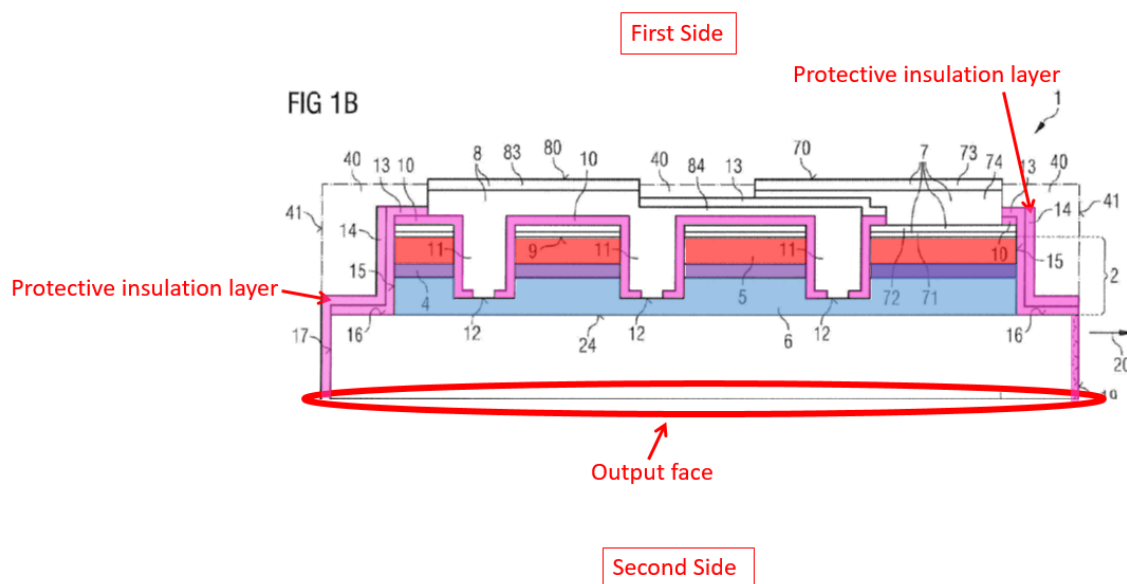
face—which includes luminescence conversion layer—can be located at a second side that is opposite the first side:³



LGI1005, FIG. 2B (annotated); [0161]; LGI1002, ¶79.

Annotated FIG. 1B of Illek below illustrates how the FIG. 1B implementation would look if reconfigured from a side-looker arrangement to a top-looker arrangement as in FIG. 2B:

³ As discussed for element [1d], the side that faces away from the carrier 3 in Illek corresponds to the “first side of the semiconductor stack.”



LGI1005, FIG. 1B (modified, annotated); [0161]; LGI1002, ¶80. In this case, Illek’s luminescence conversion layer (*i.e.*, wavelength convertor) that is applied to the output face is arranged over a second side of the semiconductor stack.
LGI1002, ¶80.

[2b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”

Illek discloses element [2b]. LGI1002, ¶¶82-83. Specifically, Illek explicitly teaches that any of the conversion materials mentioned in U.S. Pat. No. 6,066,861 (“Hohn”; LGI1006) can be used. *See* LGI1005, [0143] (“Suitable conversion materials are described, for instance, in document WO 98/12757 (U.S. Pat. No. 6,066,861), the entire disclosure content of which is explicitly incorporated into the present application.”). Hohn teaches that the wavelength convertor can include a “transparent epoxy casting resin” that contains “a

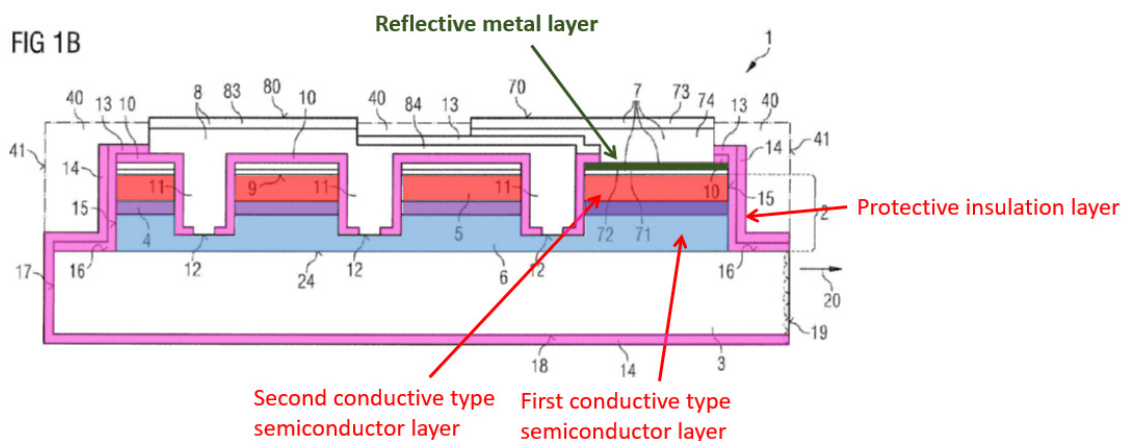
phosphorous group of the general formula $A_3B_5X_{12}:M$.” LGI1006, Abstract. Such a layer of phosphor-containing resin corresponds to the claimed phosphor sheet.

LGI1002, ¶82. Further, Hohn teaches that the conversion material can include “Ce-doped garnets,” which is an impurity-doped material. LGI1006, Claim 6; 7:4-8; LGI1002, ¶83.

Claim 3

[3a]: “The LED package of claim 1, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer”

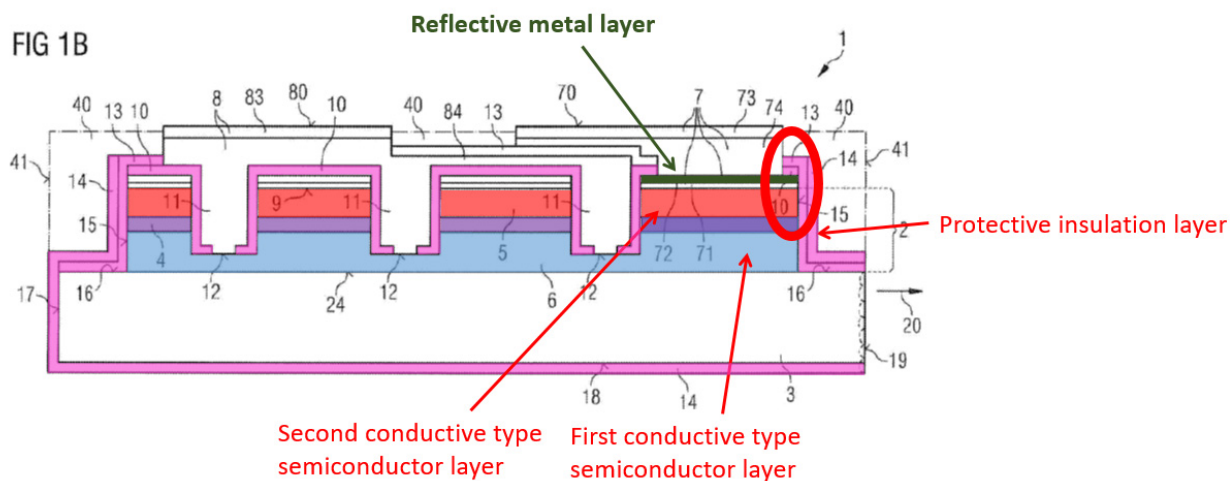
Illek discloses element [3a]. LGI1002, ¶85. As illustrated below, Illek teaches a reflector layer 72 (green) that is positioned over the second conductive type semiconductor layer (red):



LGI1005, FIG. 1B (annotated); [0103]; LGI1002, ¶85. Illek further teaches that a highly reflective material, such as Al, may be used for the reflector layer 72. *Id.*, [0107].

[3b]: “a part of the transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer.”

Illek discloses element [3b]. LGI1002, ¶89. As illustrated below, a part of the reflective metal layer (*i.e.*, reflector layer 72, shown in green) of Illek is positioned between the second conductive type semiconductor layer (*i.e.*, region 5, shown in red) and the protective insulation layer (*i.e.*, layers 10, 13, 14, shown in pink):



LGI1005, FIG. 1B (annotated); [0103]; LGI1002, ¶89.

Claim 4

[4a]: “The LED package of claim 3, wherein the transparent conductive oxide film contact layer includes an ITO (Indium Tin Oxide).”

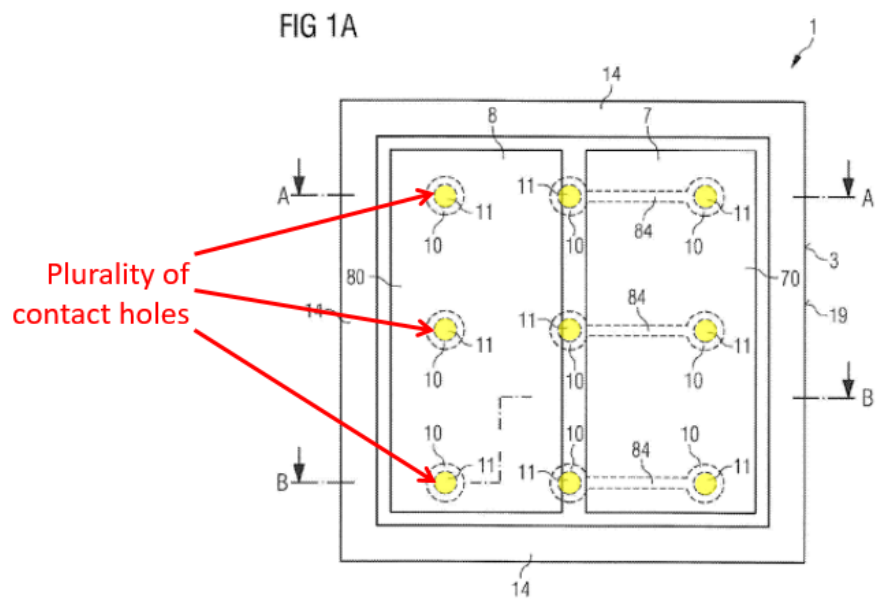
Illek satisfies this claim limitation. LGI1002, ¶91. In particular, Petitioner notes that claim 4 is directed to a narrower limitation concerning the “transparent conductive oxide film contact layer” feature, which itself was recited as *one of two*

options in claim 3, namely a transparent conductive oxide film contact layer *or* a reflective metal layer. However, claim 4 does not narrow the type of reflective metal layer that is recited in claim 3, nor does it narrow claim 3 to necessarily include the transparent conductive oxide film contact layer. That is, while claim 4 narrows the type of “transparent conductive oxide film contact layer,” claim 4 does not require that the LED package of claim 3 actually possess the transparent conductive oxide film contact layer. LGI1002, ¶91. Accordingly, claim 4, which depends from claim 3, is satisfied by an LED package that discloses a reflective metal layer. *Id.* As explained above for claim 3, Illek teaches a reflective metal layer and, therefore, also satisfies claim 4. *Id.*

Claim 5

[5a]: “The LED package of claim 4, wherein at least one of the contact holes has a circular shape, and”

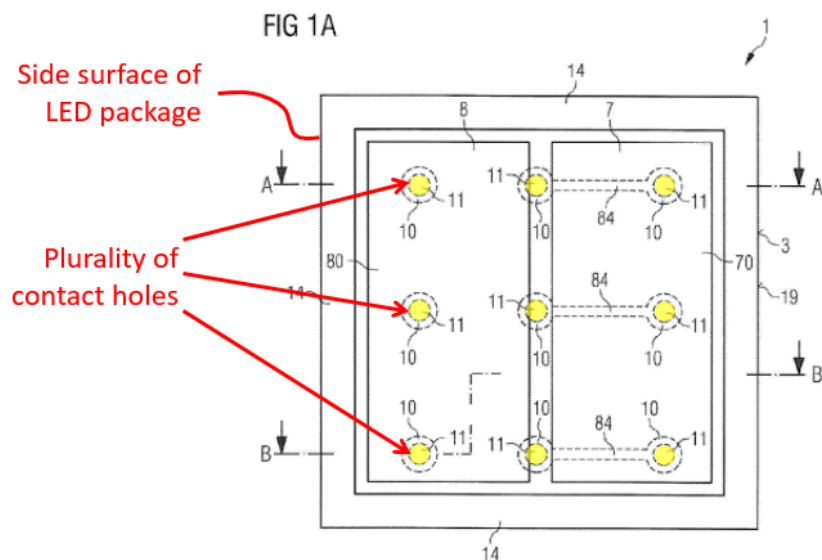
Illek discloses element [5a]. LGI1002, ¶93. For example, as seen in FIG. 1A below, the recesses 11 (*i.e.*, contact holes) of Illek have a circular shape:



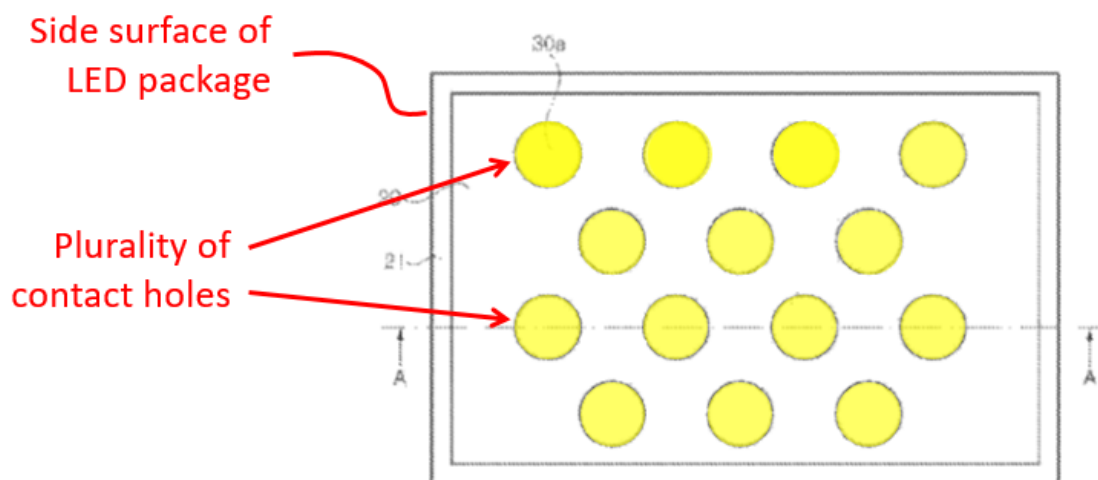
LGI1005, FIG. 1A (annotated); LGI1002, ¶93.

[5b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”

Illek discloses element [5b]. LGI1002, ¶¶94-95. For example, as seen in FIG. 1A below, the recesses 11 (*i.e.*, contact holes) of Illek are arranged along at least one side surface of the LED package:



LGI1005, FIG. 1A (annotated); LGI1002, ¶94. Indeed, Illek's arrangement of its contact holes along the side surface of the LED package corresponds to that shown in the '664 Patent:



LGI1001, FIG. 5(a) (annotated); LGI1002, ¶95.

Claim 6

[6pre]: “A light emitting diode (LED) module, comprising:”

To the extent the preamble is limiting, which Petitioner does not concede, Illek discloses element [6pre]. LGI1002, ¶96. Initially, as noted above for element [1pre], Illek teaches an LED component/package. *See* LGI1005, [0095]; FIG. 1B, [0015]. Additionally, Illek teaches that its LED component/package is mounted on an external carrier such as a circuit board. *Id.*, [0019]; [0099]; [0122]. An LED component/package that is mounted on a circuit board is a LED module. LGI1002, ¶96 (citing LGI1014).

[6a]: “a circuit board;”

Illek discloses element [6a]. LGI1002, ¶97. For example, Illek teaches that its LED component can be “mounted on the external connection carrier, preferably a connection carrier of large area such as *a circuit board*.” LGI1005, [0019]; *see also id.*, [0099]; [0122].

[6b]: “a LED package arranged over the circuit board without bonding wires, wherein the LED package includes:”

Illek discloses element [6b]. LGI1002, ¶99. Specifically, Illek teaches an LED package that is “in the manner of a flip-chip, to be electrically conductively connected to external connection conductors, preferably directly, for instance by means of electrically conductive adhesive or solder.” LGI1005, [0127]. A flip-chip architecture, as utilized in Illek as well as the ’664 Patent, allows the LED chip to be mounted directly without the use of bonding wires. LGI1002, ¶¶38-39,

99. Indeed, Illek expressly teaches that “using bonding wires can be omitted.”

LGI1005, [0127].

[6c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Illek discloses element [6c]. See Ground 1A [1a]; LGI1002, ¶¶56-57, 100.

[6d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Illek discloses element [6d]. See Ground 1A [1b]; LGI1002, ¶¶58-60, 101.

[6e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Illek discloses element [6e]. See Ground 1A [1c]; LGI1002, ¶¶61-63, 102.

[6f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

Illek discloses element [6f]. See Ground 1A [1d]; LGI1002, ¶¶64-65, 103.

[6g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”

Illek discloses element [6g]. See Ground 1A [1e]; LGI1002, ¶¶66-74, 104.

[6h]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and”

Illek discloses element [6h]. See Ground 1A [1f]; LGI1002, ¶¶76-77, 105.

[6i]: “a lens to adjust an orientation angle of light emitted from the LED package.”

Illek discloses element [6i]. LGI1002, ¶106. For example, Illek teaches that “an optical element such as *a refractive element for the beam shaping, in particular, a lens*, or a diffractive element can be located on the output face and, in particular, applied to the component.” LGI1005, [0143]. The lens of Illek that is located at the output face of the LED, by shaping the output beam through optical refraction, serves to adjust an orientation angle of light emitted from the LED package. LGI1002, ¶106.

Claim 8

[8pre]: “A light emitting diode (LED) module, comprising:”

To the extent the preamble is limiting, which Petitioner does not concede, Illek discloses element [8pre]. *See* Ground 1A [6pre]; LGI1002, ¶¶96, 107.

[8a]: “a circuit board;”

Illek discloses element [8a]. *See* Ground 1A [6a]; LGI1002, ¶108.

[8b]: “a LED package bonded on the circuit board without bonding wires; wherein the LED package comprising”

Illek discloses element [8b]. *See* Ground 1A [6b]; LGI1002, ¶¶38-39, 110. Specifically, a flip-chip architecture, as utilized in Illek as well as the ’664 Patent, allows the LED chip to be bonded directly on the circuit board without the use of bonding wires. *Id.*

[8c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Illek discloses element [8c]. See Ground 1A [6c]; LGI1002, ¶¶56-57, 111.

[8d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Illek discloses element [8d]. See Ground 1A [6d]; LGI1002, ¶¶58-60, 112.

[8e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Illek discloses element [8e]. See Ground 1A [6e]; LGI1002, ¶¶61-63, 113.

[8f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

Illek discloses element [8f]. See Ground 1A [6f]; LGI1002, ¶¶64-65, 114.

[8g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer.”

Illek discloses element [8g]. See Ground 1A [6g]; LGI1002, ¶115.

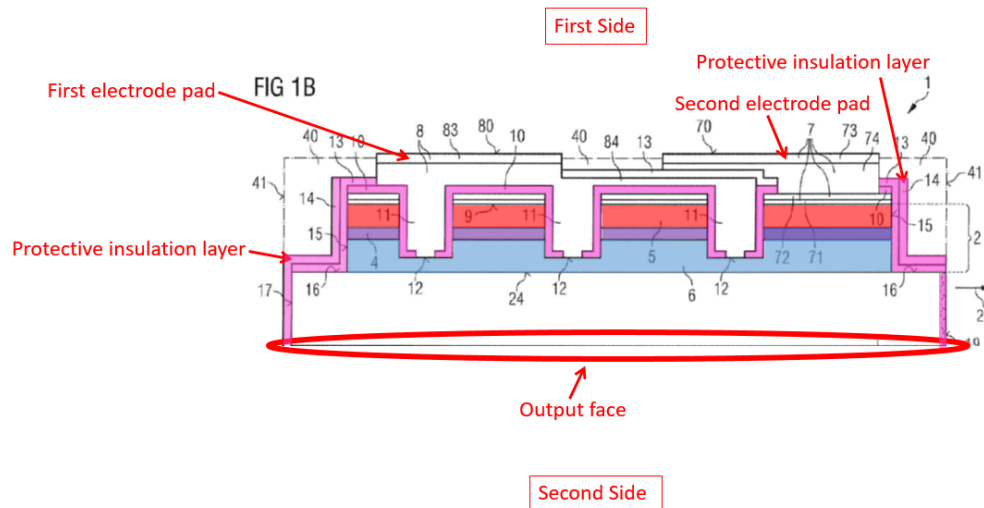
Incidentally, because the protective insulation layer of Illek covers the sidewall of both the first and second conductive type semiconductor layers, it covers the sidewall of the first conductive type semiconductor layer as recited in element [8g]. See Ground 1A [1e]; LGI1002, ¶¶66-74.

Claim 9

[9a]: “The LED module of claim 8, further comprising a wavelength converter over the opposite side of the LED package to the first and second electrode pads,”

Illek discloses element [9a]. See Ground 1A [2a]; LGI1002, ¶¶78-80, 116.

Moreover, the second side of the semiconductor stack, as discussed above for Ground 1A [2a] and illustrated in the annotated drawing below, is on the opposite side of the LED package to the first and second electrode pads:



LGI1005, FIG. 1B (modified, annotated); Analysis for Ground 1A [1c] and [1d], *supra*; LGI1002, ¶¶61-65, 116.

[9b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”

Illek discloses element [9b]. See Ground 1A [2b]; LGI1002, ¶¶82-83, 117.

Claim 11

[11a]: “The LED module of claim 8, further comprises a lens to adjust an orientation angle of light emitted from the LED package.”

Illek discloses element [11a]. *See* Ground 1A [6i]; LGI1002, ¶¶106, 121.

Claim 12

[12a]: “The LED module of claim 8, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”

Illek discloses element [12a]. *See* Ground 1A [1f]; LGI1002, ¶¶76-77, 122.

B. [GROUND 1B]: Claims 1-6 and 8-18 are rendered obvious by Illek

Although, as described above in Ground 1A, Illek anticipates claim 1-6, 8, 9, 11, and 12, the same claims, along with claims 10, and 13-18, are further rendered obvious by Illek in view of the knowledge of a POSITA under 35 U.S.C. § 103. *See* LGI1002, ¶¶54-132. To clarify, in addition to the application of Illek found in Ground 1A, below, with respect to identified elements, it is revealed how a POSITA would have additionally found the element obvious in view of Illek’s teachings.

For example, with respect to elements [1e] and [1f], to the extent the Board determines that Illek does not explicitly disclose these features, a POSITA would have understood that Illek’s insulations layers 10 and 13 along with its mirror layer 14 collectively make up the “protective insulation layer” as claimed in the ’664 Patent. LGI1002, ¶¶66-75. Indeed, Illek’s layers 10/13/14 are each described as being insulators, and a POSITA would understand that their application to the

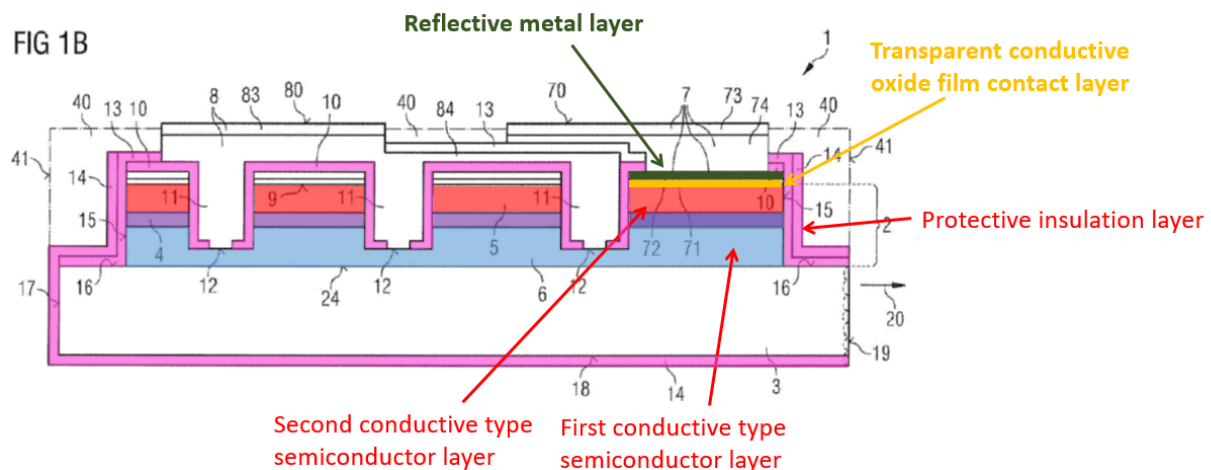
various faces—including sidewalls—of the semiconductor stack would serve to passivate and protect the semiconductor stack to thereby, for instance, prevent shorting of the junction. LGI1005, [0112]; [0120]; [0130]; LGI1002, ¶¶70-74.

With respect to element [2a], to the extent the Board determines that Illek does not explicitly disclose these features, a POSITA would have recognized that Illek's LED package shown in FIG. 1B can be easily modified to move the output face from a side surface of the carrier 3 (*i.e.*, side-looker) to its bottom surface (*i.e.* top-looker), thereby allowing the wavelength convertor to be arranged over a second side of the semiconductor stack. LGI1002, ¶¶78-81. In fact, Illek expressly teaches that the output face can be positioned at any desired surface of the carrier 3 and further shows, in FIG. 2B, an implementation in which the output face is positioned at the second/bottom side. LGI1005, [0142]; [0161]; FIG. 2B; LGI1002, ¶79. Thus, moving the location of the output face shown in FIG. 1B from the side to the bottom merely entails a simple substitution of a side-looker configuration with a top-looker configuration to obtain predictable results. LGI1002, ¶¶80-81.

With respect to element [2b], to the extent the Board determines that Illek does not explicitly disclose these features, a POSITA would have readily recognized that Illek's luminescence conversion layer (*i.e.*, wavelength convertor) can be made from various well-known wavelength conversion materials, including

a phosphor sheet or an impurity-doped material as claimed. LGI1002, ¶84. For example, Hohn, the entire disclosure of which was incorporated into Illek, explicitly teaches the use of a phosphor-containing epoxy (*i.e.*, phosphor sheet) or a Ce-doped garnet (*i.e.*, impurity-doped material) in such wavelength converting applications. LGI1006, Abstract; Claim 6; LGI1002, ¶¶81-83.

With respect to the “transparent conductive oxide film contact layer” as recited in claims 3 and 4, to the extent the Board determines that Illek does not explicitly disclose these features, a POSITA would have recognized that the “semitransparent” “contact layer 71” of Illek, which as illustrated below is positioned between the reflective metal layer and the second conductive type semiconductor layer, is a “transparent conductive oxide film contact layer.”



LGI1005, FIG. 1B (annotated); [0106]; LGI1002, ¶¶86-88, 90. In particular, a POSITA would have known that a semitransparent contact layer that is “optimized

for electrical contact formation” as in Illek is a conductive oxide film. LGI1005, [0106]; LGI1002, ¶87. Moreover, a POSITA would have known that Indium Tin Oxide (ITO) was a commonly-used material for making transparent conductive oxide film contact layers at the time of Illek as well as the ’664 Patent and would have been well-suited for use as the semitransparent contact layer 71. LGI1002, ¶87 (citing to LGI1012, Abstract, 2:44-64; 7:26-35). Therefore, Illek renders obvious the “transparent conductive oxide film contact layer” limitation of claim 3 as well as the ITO limitation of claim 4. LGI1002, ¶¶87-88, 92.

With respect to the “circuit board” as recited in claims 6 and 8, although Illek does not explicitly show an LED package that is bonded to or otherwise arranged over a circuit board, a POSITA would have found Illek sufficient to teach the recited circuit board, and, regardless, would have found the recited circuit board obvious in view of Illek’s disclosure of an LED package that is designed to be mounted on a circuit board. LGI1005, [0019]; [0099]; [0122]; LGI1002, ¶¶98, 109 (citing LGI1007).

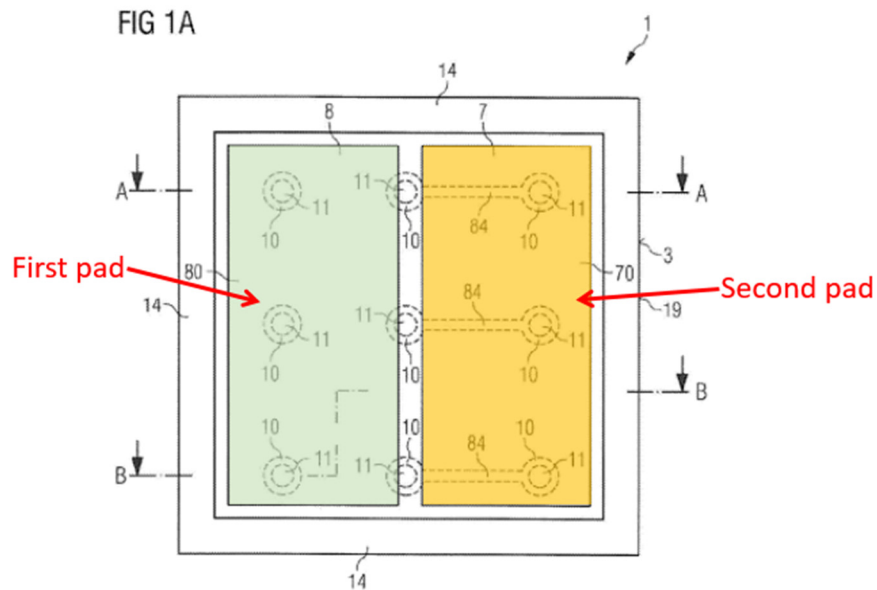
The remaining claim elements of claims 1-6, 8, 9, 11, 12 are disclosed by Illek as discussed above for Ground 1A. *See* LGI1002, ¶¶55-117, 121, 122.

Petitioner now turns to the additional recitations of claims 10 and 13-18 and how those claims are rendered obvious in view of Illek.

Claim 10

[10a]: “The LED module of claim 9, wherein each area of the first and second pads has an area not less than $\frac{1}{3}$ of the LE package.”

Illek discloses element [10a]. LGI1002, ¶¶118-120. For example, as seen in FIG. 1A below, the first and second pads of Illek, shown in green and yellow respectively, each appear to have areas that take up roughly half (*i.e.*, not less than $\frac{1}{3}$) of the LED package:



LGI1005, FIG. 1A (annotated); LGI1002, ¶118. Indeed, it was well-known to a POSITA at the time of Illek, as well as the '664 Patent, to maximize the areas of electrode pads in flip-chip applications. LGI1002, ¶118. Maximizing the areas of electrode pads, for instance, helped reduce the need for high precision when mounting the LED chips onto circuit boards and further helped better dissipate heat generated during the mounting process. *Id.* (citing to LGI1013, 10:47-54).

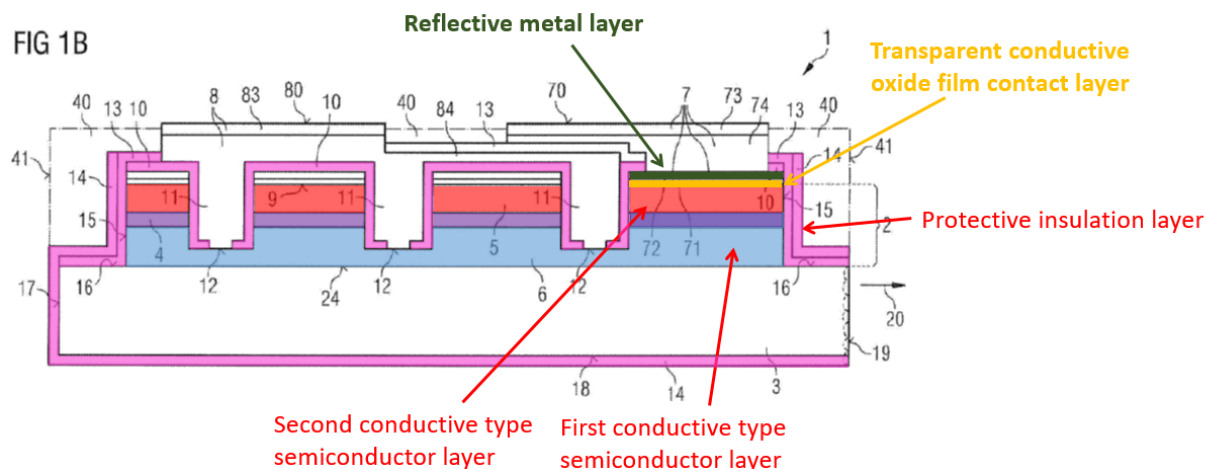
Thus, to the extent Illek does not explicitly disclose that each area of the first and second pads has an area not less than 1/3 of the LED package, a POSITA would have found such a feature obvious and would have recognized further that it is simply a matter of design choice to make the electrode pads as large as possible without them shorting. LGI1002, ¶¶119-120. Indeed, a plethora of prior art during this time period expressly teach maximizing the areas of electrode pad pairs to each cover about half the total area of the LED chip. LGI1002, ¶120 (citing to LGI1013, 10:47-54). That is, a POSITA would have recognized that maximizing the areas of the electrode pads such that each covers approximately half the area of the LED chip—*i.e.*, each pad covering an area not less than 1/3 of the LED package—is a simple and routine design choice that would allow the flip-chip type component of Illek to be more easily mounted during manufacturing. LGI1002, ¶¶119-120.

Claim 13

[13a]: “The LED module of claim 12, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer; and”

As discussed above for Ground 1A [3a], Illek teaches providing a reflective metal layer over the second conductive type semiconductor layer. LGI1002, ¶¶85-86, 123.

Additionally, as discussed above for Ground 1B with respect to claims 3 and 4, and as illustrated below, Illek further renders obvious providing a transparent conductive oxide film contact layer over the second conductive type semiconductor layer:

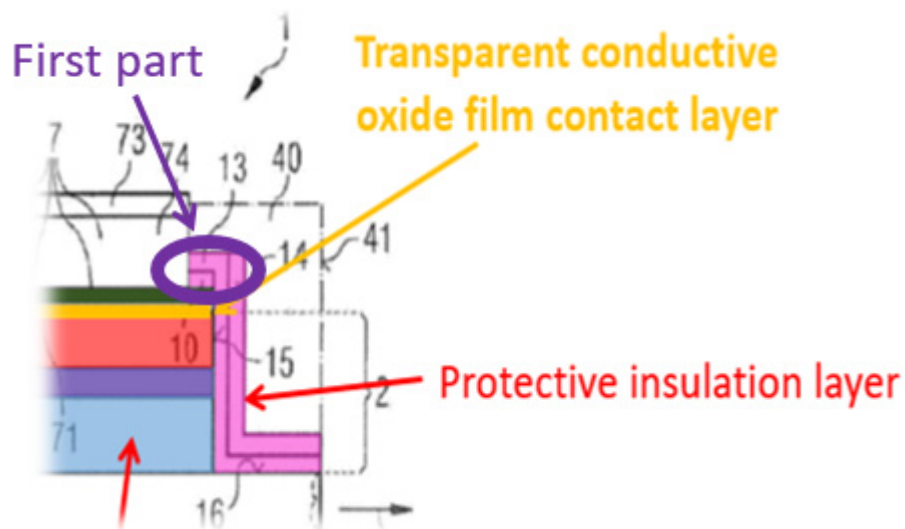


LGI1005, FIG. 1B (annotated); [0106]; LGI1002, ¶¶86-88, 123.

Thus, Illek discloses an LED module comprising a transparent conductive oxide film contact layer *as well as* a reflective metal layer over the second conductive type semiconductor layer, thus doubly satisfying element [13a].
LGI1002, ¶123.

[13b]: “a first part of the protective insulation layer covering the contact layer.”

Illek discloses element [13b]. LGI1002, ¶124. For example, as seen in FIG. 1B below, the protective insulation layer (*i.e.*, layers 10/13/14, shown in pink) includes a horizontal portion, labeled as “first part,” that covers an upper side of the contact layer (yellow):

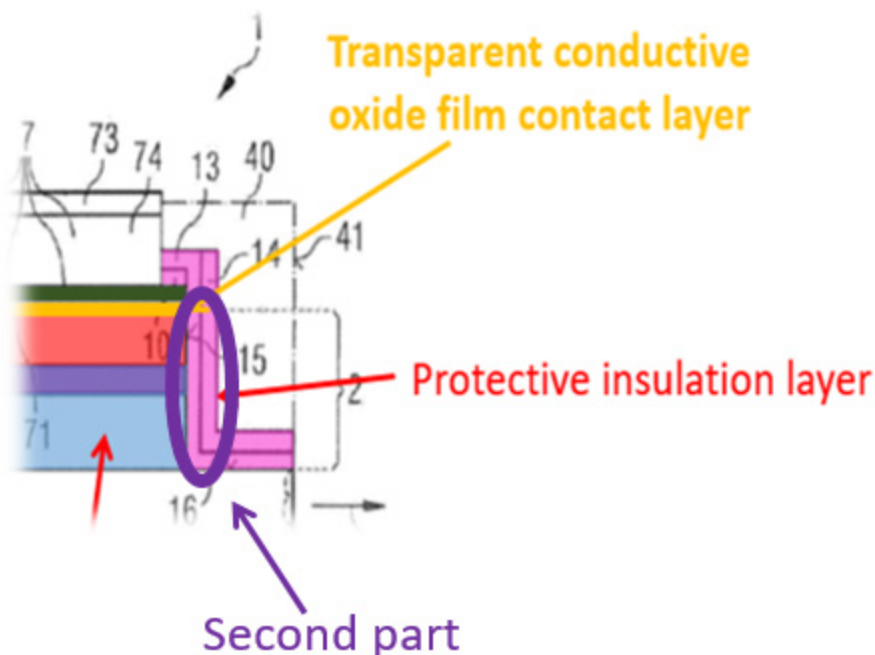


LGI1005, FIG. 1B (cropped, annotated); [0109]; LGI1002, ¶124.

Claim 14

[14a]: “The LED module of claim 13, wherein a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer,”

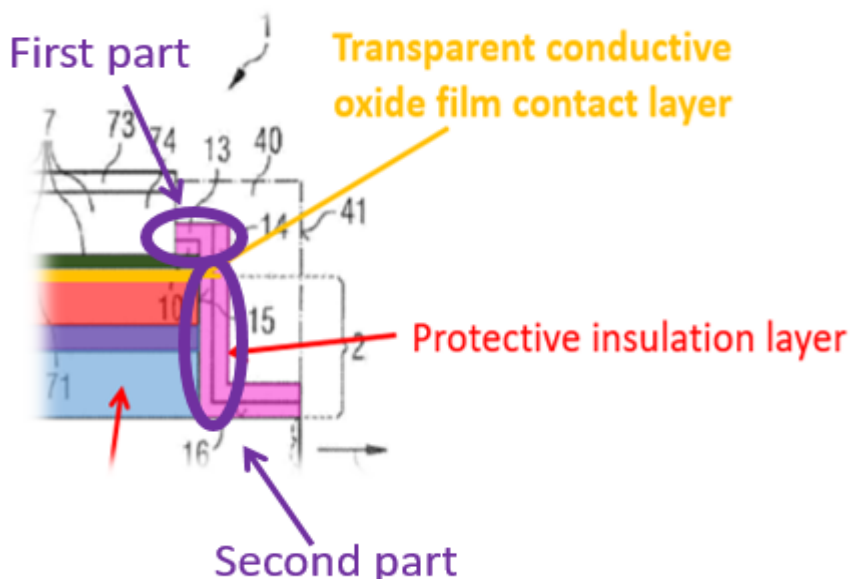
Illek discloses element [14a]. LGI1002, ¶125. For example, as seen in FIG. 1B below, the protective insulation layer (*i.e.*, layers 10/13/14, shown in pink) includes a vertical portion, labeled as “second part,” that covers the sidewall of the first conductive type semiconductor layer (blue):



LGI1005, FIG. 1B (cropped, annotated); [0109]-[0112]; [0120]; [0128]; LGI1002, ¶125.

[14b]: “the second part of the protective insulation layer contacts the first part of the protective insulation layer.”

Illek discloses element [14b]. LGI1002, ¶126. For example, as seen in FIG. 1B below, the protective insulation layer (*i.e.*, layers 10/13/14, shown in pink) includes a horizontal portion (labeled “first part”) and a vertical portion (labeled “second part”) that contact each other:



LGI1005, FIG. 1B (cropped, annotated); LGI1002, ¶126.

Claim 15

[15a]: “The LED module of claim 14, wherein each area of the first and second pads is not less than $\frac{1}{3}$ of area of the LED package.”

Illek discloses element [15a]. See Ground 1B [10a]; LGI1002, ¶¶118-120, 127.

Claim 16

[16a]: “The LED module of claim 15, further comprising a wavelength convertor the opposite side of the LED package to the first and second electrode pads,”

Illek discloses element [16a]. See Ground 1A [9a]; LGI1002, ¶¶116, 128.

[16b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”

Illek discloses element [16b]. See Ground 1A [9b]; LGI1002, ¶¶82-84, 117, 129.

Claim 17

[17a]: “The LED module of claim 16, at least one of the contact holes has a circular shape, and”

Illek discloses element [17a]. See Ground 1A [5a]; LGI1002, ¶¶93, 130.

[17b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”

Illek discloses element [17b]. See Ground 1A [5b]; LGI1002, ¶¶94-95, 131.

Claim 18

[18a]: “The LED module of claim 17, further comprising a lens to adjust an orientation angle of light emitted from the LED package.”

Illek discloses element [18a]. See Ground 1A [6i]; LGI1002, ¶¶106, 132.

C. [GROUND 1C]: Claims 7 and 19 are rendered obvious by Illek in view of Begemann

Claim 7

[7a]: “The LED module of claim 6, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and the LED packages is arranged over the MC-PCB.”

Illek in view of Begemann renders obvious element [7a]. LGI1002, ¶¶133-140. Specifically, as discussed above respect to Ground 1A [6a], Illek teaches mounting its LED component on a circuit board. LGI1005, [0019]; [0099]; [0122]. Illek does not, however, disclose a specific type of circuit board to be used, as it leaves that implementation detail to the POSITA. LGI1002, ¶136.

Begemann, which is directed to an LED lamp, teaches a similar configuration as Illek in which LED chips are mounted on a printed circuit board (PCB). LGI1008, [0012]; LGI1002, ¶137. Begemann additionally discloses that a specific type of PCB—namely a “metal-core PCB” or “MC-PCB”—can be used in LED applications. LGI1008, [0012]; [0028]; LGI1002, ¶137.

Multiple reasons would have prompted a POSITA to incorporate Begemann’s MC-PCB to Illek’s LED device. LGI1002, ¶¶138-140.

First, given the structural and functional similarities between Illek and Begemann—*e.g.*, both references disclose an LED chip that is mounted on a circuit board—a POSITA would have recognized that the advantages achieved by Begemann’s use of an MC-PCB would likewise improve Illek. LGI1002, ¶¶138-139; MPEP §2144(II); MPEP § 2143 I(C)-(D); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 405, 417 (2007). For instance, Begemann explains that MC-PCB is “customarily used” in LED applications and that “[s]uch PCBs have a relatively high heat conduction,” thereby resulting in “a very good heat dissipation from the LED arrays....” LGI1008, [0012]; *see also id.*, [0028] (“[MC-PCB] is responsible for a good heat transfer.”). Because LED chips tend to generate excess heat, thermal management is critical. LGI1002, ¶139. Indeed, Illek recognizes the need to reduce “excessive internal temperatures within the [LED] component” to thereby minimize “thermally induced damage to the [LED] component.”

LGI1005, [0012]. Thus, a POSITA would have been motivated to mount Illek's LED components on an MC-PCB, as opposed to a less thermally conductive type of PCB, to achieve improved heat dissipation. LGI1002, ¶139.

Second, a POSITA would have considered the use of an MC-PCB, as disclosed by Begemann, to be a routine and conventional design choice given the popularity of this technique at the time of Illek as well as the '664 Patent. LGI1002, ¶140; *see also In re Magna Elecs., Inc.*, 611 Fed. Appx. 969, 974 (Fed. Cir. 2015) (citing *In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975) (finding a generic feature that “provides no novel or unexpected result” as “an obvious matter of design choice”). Indeed, many other references before and during this time period teach the use of an MC-PCB to improve heat dissipation in LED devices. LGI1002, ¶140. (citing LGI1008, [0012]; LGI1009, [0093]). There was nothing new or inventive about using an MC-PCB at the time of the '664 Patent. LGI1002, ¶140. Indeed, incorporating the MC-PCB of Begemann into the LED device of Illek amounts to merely combining prior art elements from the same field, according to known methods to yield predictable results. *See KSR*, 550 U.S. at 417; LGI1002, ¶140.

Thus, the Illek-Begemann combination renders obvious element [7a]. LGI1002, ¶¶136-140.

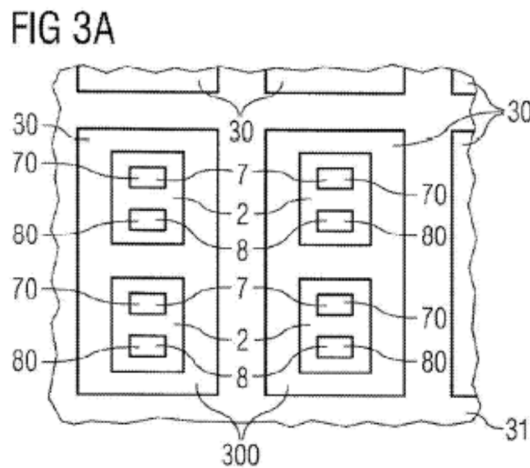
Claim 19

[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”

Illek in view of Begemann renders obvious element [19a]. See Ground 1C [7a]; LGI1002, ¶¶136-140, 141.

[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”

Illek in view of Begemann renders obvious element [19b]. LGI1002, ¶¶142-143. For example, as seen in FIG. 3A below, Illek teaches mounting a plurality of LED packages on an auxiliary carrier:



LGI1005, FIG. 3A; [0169]; LGI1002, ¶142. To the extent Illek doesn’t expressly disclose arranging the plurality of LED packages on the MC-PCB, Begemann provides this feature.

Specifically, as discussed above for element [7a], Begemann teaches mounting LED packages on an MC-PCB, and a POSITA would have found it

obvious to incorporate Begemann's MC-PCB to Illek's LED device. LGI1002,

¶¶136-140. Additionally, as shown below, Begemann explicitly teaches mounting multiple LED chips onto an MC-PCB:

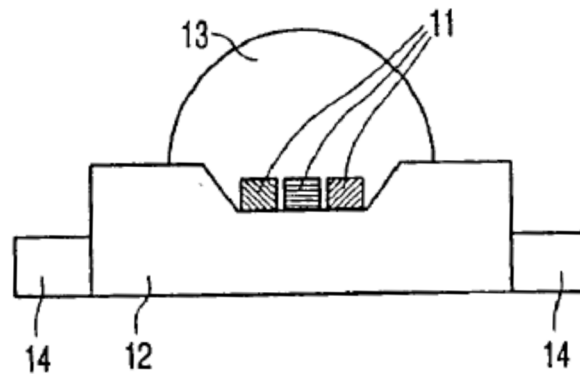


FIG. 3B

LGI1008, FIG. 3B; [0029]. A POSITA would have considered the mounting of multiple LED packages on an MC-PCB to be a routine and conventional design choice. LGI1002, ¶143; *see also In re Magna Elecs., Inc.*, 611 Fed. Appx. 969, 974 (Fed. Cir. 2015) (citing *In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975) (finding a generic feature that “provides no novel or unexpected result” as “an obvious matter of design choice”). Indeed, the arrangement of a plurality of LED packages on an MC-PCB, as evidenced by Begemann, was common practice in the field of LED design and manufacturing, and there was nothing new or inventive about changing the number of LED packages being mounted or even the type of circuit board being utilized at the time of the '664 Patent. LGI1002, ¶143. Thus,

incorporating the multiple-chip configuration of Begemann into the LED device of Illek amounts to merely combining prior art elements from the same field, according to known methods to yield predictable results. *See KSR*, 550 U.S. at 417; LGI1002, ¶143.

Thus, the Illek-Begemann combination renders obvious element [19b]. LGI1002, ¶¶142-143.

A. [GROUND 2A]: Claims 1-19 are rendered obvious by Donofrio in view of Sano

Overview of Donofrio

Donofrio is entitled “Semiconductor Light Emitting Diodes Having Reflective Structures and Methods of Fabricating Same” and is directed to “[l]ight emitting diodes includ[ing] a diode region having first and second opposing faces that include therein an n-type layer and a p-type layer, an anode contact that ohmically contacts the p-type layer and extends on the first face, and a cathode contact that ohmically contacts the n-type layer and also extends on the first face.” LGI1009, Abstract.

In particular, Donofrio teaches “an n-type layer 112 and a p-type layer 114,” an active region 116 between these layers, and “a via 118 [that exposes] the n-type layer 112.” *Id.*, [0040]-[0042]. Donofrio also teaches an anode pad 160, a cathode pad 170, and an insulating layer 140 that extends into the via 118. *Id.*, [0042]-[0043].

FIG. 1

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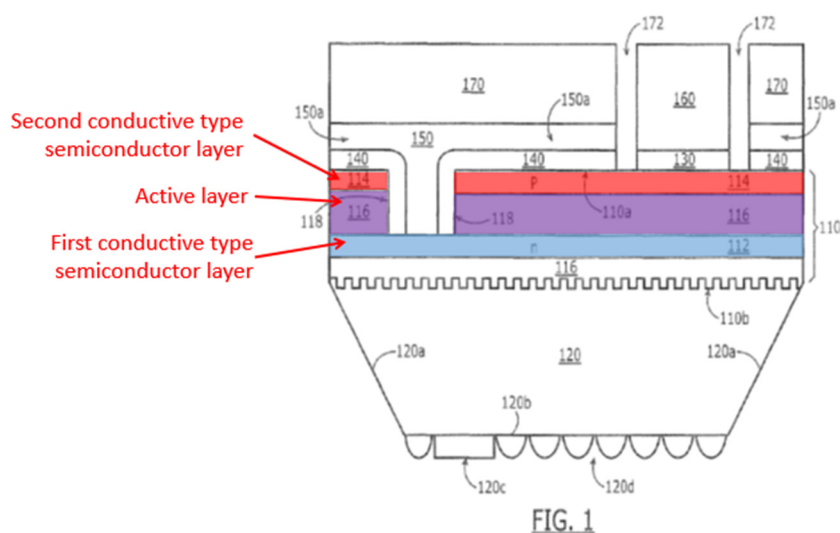
Claim 1

[1pre]: “A light emitting diode (LED) package, comprising:”

To the extent the preamble is limiting, which Petitioner does not concede, Donofrio discloses element [1pre]. LGI1002, ¶151. Specifically, Donofrio teaches “an LED that is suitable for flip-chip mounting” and is generally directed to “LED chips.” LGI1009, [0046], [0050].

[1a]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Donofrio discloses element [1a]. LGI1002, ¶¶152-153. Specifically, as shown in FIG. 1, Donofrio’s LED includes a semiconductor stack that is made up of an n-type semiconductor layer 112 (blue), an active region 116 (purple), and a p-type semiconductor layer 114 (red):



LGI1009, FIG. 1 (annotated); [0040]; [0052]; LGI1002, ¶152.

Regarding its layer 116, Donofrio describes an “active region” that emits light such that the LED emits “visible light from the diode region 110.” LGI1009, [0052]; [0102] (“the active layer”); [0059]; [0062]; [0055]; [0064]. Further, FIG. 2 shows a layer 116 that is described as “[o]ther layers or regions 116” of the “diode region 110” that “need not be described herein.” *Id.*, [0040]. A POSITA would have understood from the disclosure of the LED including an “active layer” that emits light and the description of the “diode region 110” as emitting light, as well as from a basic understanding of how LEDs have functioned for decades, that the layer 116 (purple) positioned between the n-type semiconductor layer 112 and the p-type semiconductor layer 114 constitutes the light emitting active layer described elsewhere in Donofrio. LGI1002, ¶153; LGI1009, FIG. 2; [0052]; [0102]; [0059]; [0062]; [0040].

[1b]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Donofrio discloses element [1b]. LGI1002, ¶154. In particular, Donofrio teaches “a *via 118* [that] extends into the first face 110a *to expose the n-type layer 112.*” LGI1009, [0042]. The vias 118, which correspond to the claimed plurality of contact holes, are shown in yellow in the top-down view of Donofrio’s LED below:

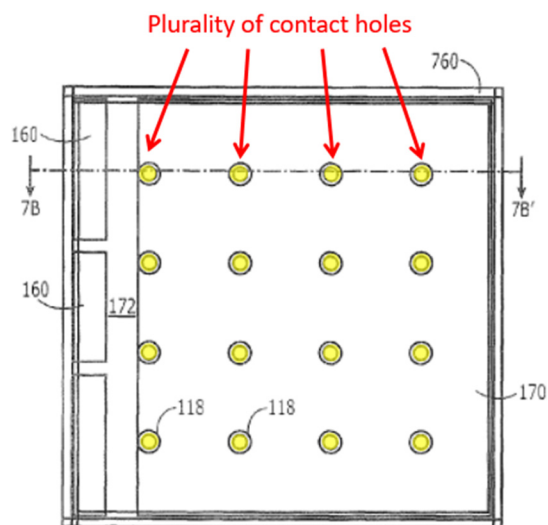


FIG. 7A

LGI1009, FIG. 7A (annotated); [0077]; LGI1002, ¶154.

As seen in the cross-sectional view of FIG. 1 below, the plurality of contact holes (yellow) in Donofrio are arranged in the second conductive type semiconductor layer (red) and the active layer (purple) to expose the first conductive type semiconductor layer (blue):

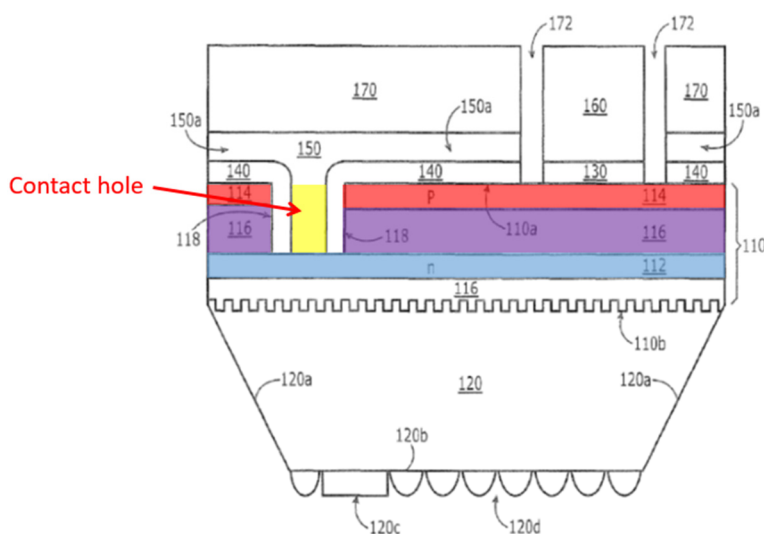


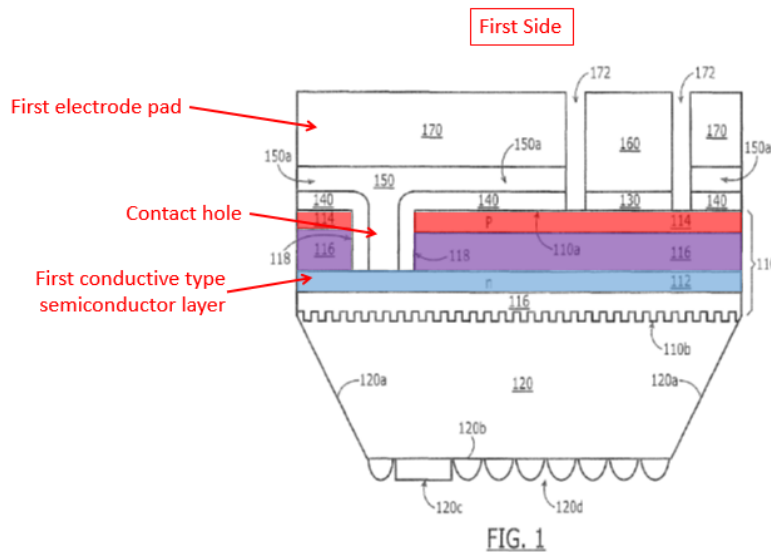
FIG. 1

LGI1009, FIG. 1 (annotated); [0042]; LGI1002, ¶154.

[1c]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Donofrio discloses element [1c]. LGI1002, ¶¶155-156. For example, Donofrio teaches a “**cathode pad 170**...that is electrically connected to the reflective cathode contact 150,” which in turn “electrically contacts the n-type layer 112.” *Id.*, [0043], [0041]. Additionally, the cathode contact 150 extends “into the via 118, to electrically, and in some embodiments ohmically, contact the n-type layer 112 that is exposed in the via 118.” *Id.*, [0042].

Thus, as illustrated below, the first electrode pad of Donofrio (*i.e.*, cathode pad 170) is arranged over a first side of the semiconductor stack and is further electrically connected to the first conductive type semiconductor layer (*i.e.*, n-type layer 112) via some of the plurality of contact holes (*i.e.*, via 118):

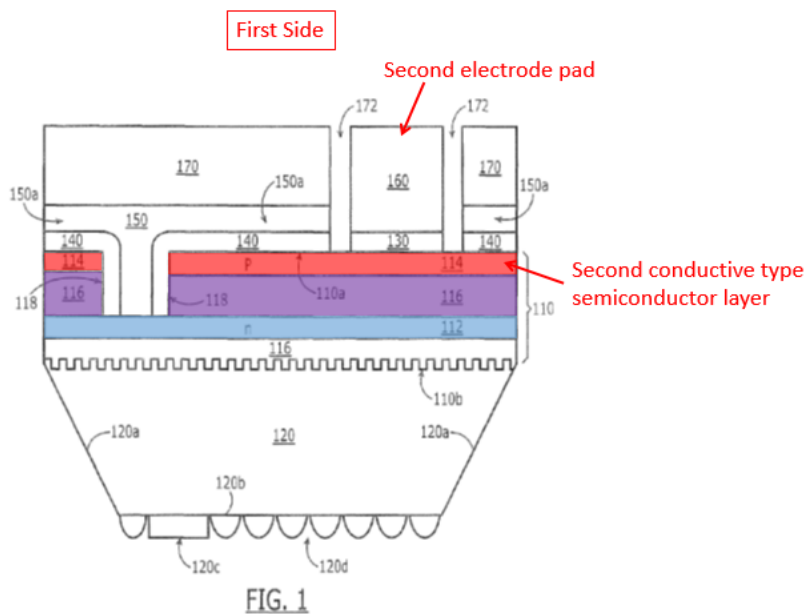


LGI1009, FIG. 1 (annotated); LGI1002, ¶156.

[1d]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

Donofrio discloses element [1d]. LGI1002, ¶¶157-158. For example, Donofrio teaches an “*anode pad 160*... that is electrically connected to the anode contact 130,” which in turn “contacts the p-type layer 114.” *Id.*, [0043], [0041]. LGI1002, ¶157.

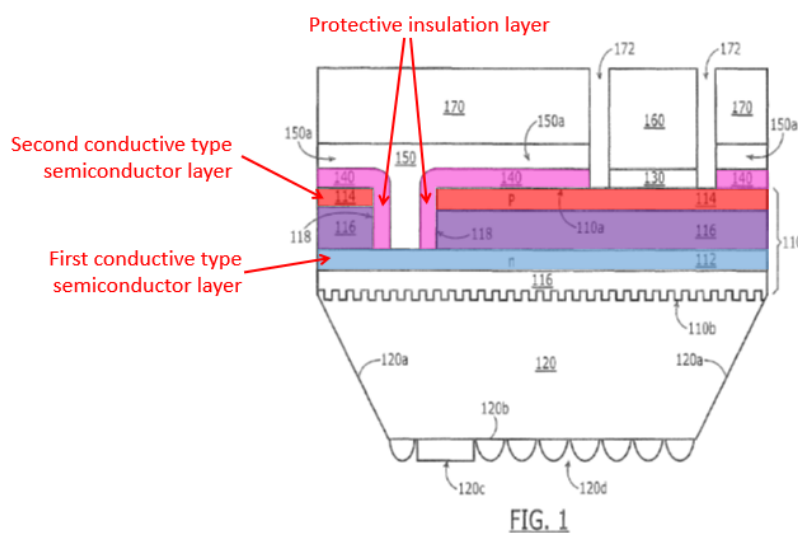
Thus, as illustrated below, the second electrode pad of Donofrio (*i.e.*, anode pad 160) is arranged over a first side of the semiconductor stack and is further electrically connected to the second conductive type semiconductor layer (*i.e.*, p-type layer 114):



LGI1009, FIG. 1 (annotated); LGI1002, ¶¶157-158.

[1e]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”

Donofrio discloses element [1e]. LGI1002, ¶¶159-170. For example, as shown in FIG. 1 below, Donofrio teaches an “**insulating layer 140** [that] extends into the via 118” where the via 118 has been etched through the semiconductor layers to expose the first conductive type semiconductor layer (*i.e.*, n-type layer 112):



LGI1009, FIG. 1 (annotated); [0042]; [0073]; LGI1002, ¶¶159-160. As shown above, the “insulating layer 140 is provided **on the sidewalls** of the via 118,” and therefore covers a sidewall of the semiconductor stack. LGI1009, [0061].

LGI1002, ¶¶159-160. In this way, the insulating layer 140 of Donofrio (shown in pink above) serves to passivate and protect the semiconductor stack to, for instance, prevent shorting of the junction. LGI1002, ¶160.

While Donofrio discloses a protective insulation layer that covers the semiconductor sidewall, Donofrio does not explicitly mention that sidewalls of ***both*** the first ***and*** second conductive type semiconductor layers are covered. LGI1002, ¶161. Rather, annotated FIG. 1 above appears to show that the sidewalls of only the second semiconductor layer 114 (shown in red above) is covered. *Id.* This is because the via 118 (*i.e.*, contact hole) of Donofrio, which is etched through the semiconductor stack to expose the n-type layer 112 (*i.e.*, first conductive type semiconductor layer), is shown in FIG. 1 as stopping perfectly at the boundary between the active region 116 (purple) and the n-type layer 112 (blue). LGI1009, [0073]; LGI1002, ¶161. That is, because the via 118 does not extend further ***into*** the n-type layer 112, the protective insulation layer stops short of covering the sidewall of the n-type layer as well.

However, a POSITA would have recognized that such perfect stopping of a multi-layer etching process precisely at the boundary between two semiconductor layers is highly unlikely—especially without the use of any additional etch-stop layers, which is not shown as used in Donofrio. LGI1002, ¶162.

Rather, a POSITA would have recognized that, as illustrated in modified FIG. 1 of Donofrio shown below, the via 118 would have at least partially etched into the n-type layer 112 (blue) to thereby cause the protective insulation layer (pink) to extend into that region (circled in red):

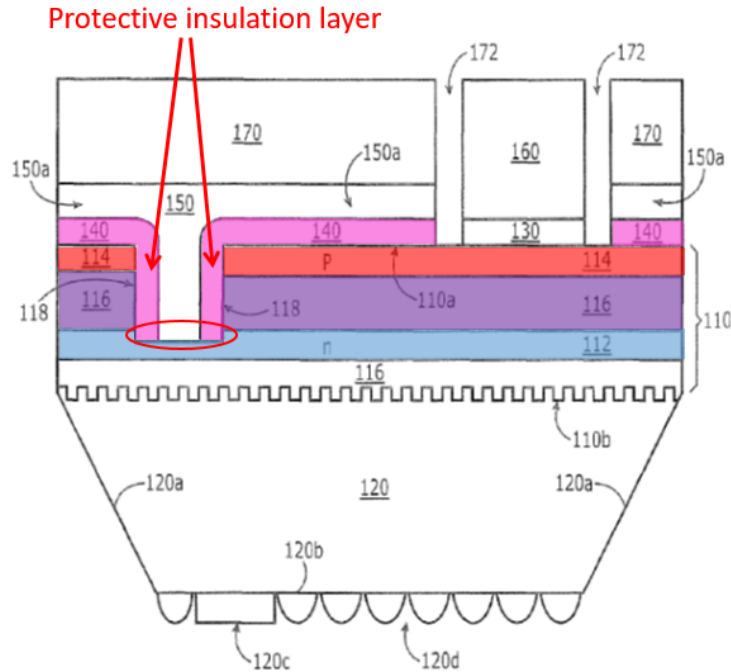
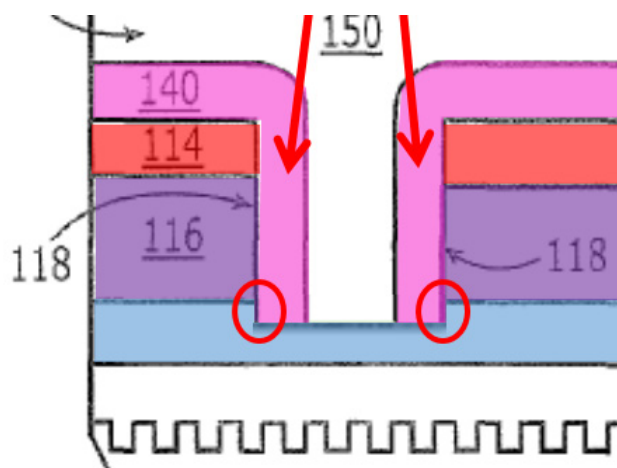


FIG. 1

LGI1009, FIG. 1 (modified, annotated); LGI1002, ¶¶162-165. Otherwise, any unetched material remaining on top of the n-type layer would prevent contact 150 from making ohmic contact with the n-type layer. LGI1002, ¶¶164-165. A slight overetch into the n-type layer, on the other hand, would ensure good electrical contact and is indeed commonly practiced in semiconductor manufacturing. LGI1002, ¶163 (citing LGI1015, 3:44-51 (“During etching of contact vias, some degree of overetch into the underlying silicon substrate 12 is necessary to ensure that the contacts are completely open.”)).

Thus, as shown in the close-up of the same modified drawing below, the resulting sidewall (circled in red) of the n-type layer 112 (first conductive type

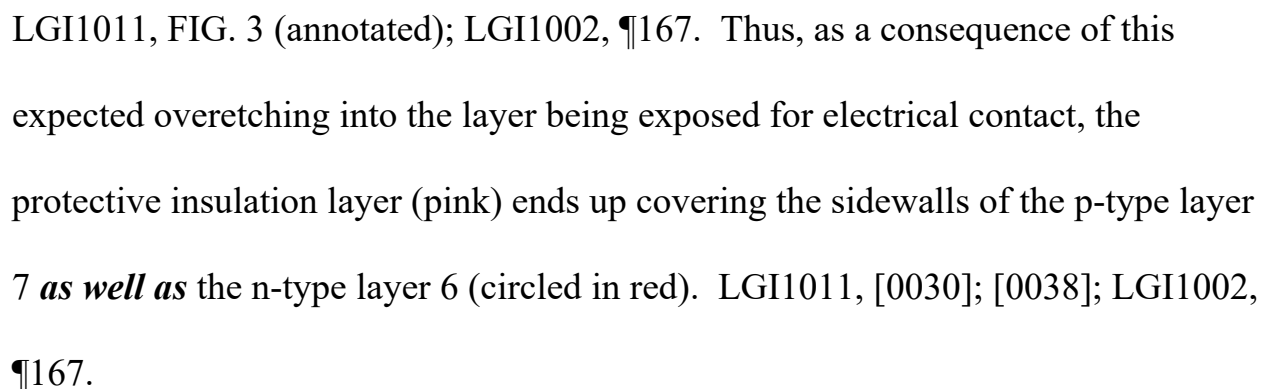
semiconductor layer) would also become covered by the protective insulation layer:



LGI1009, FIG. 1 (modified, cropped, annotated); LGI1002, ¶165.

To the extent the overetching of the via 118 into the n-type layer—and the subsequent coating of the resulting sidewall with the protective insulation layer—is not rendered obvious by Donofrio, a plethora of prior art during this time period further demonstrate the obviousness of element [1e]. LGI1002, ¶¶166-170.

For example, similar to Donofrio which teaches that “a via, such as via 118, is etched through a p-type layer, such as a p-type layer 114...to expose an n-type layer, such as an n-type layer 11” (LGI1009, [0073]), Sano (LGI1011) teaches a LED semiconductor stack where the “p-type semiconductor layer 7 [is] selectively etched and removed to expose a part of the n-type semiconductor layer 6.”



A POSITA would have been motivated to incorporate Sano's partial etching of the n-type layer into Donofrio's etching process for several reasons. LGI1002, ¶¶168-170.

First, given the vast structural and functional similarities between Donofrio and Sano—*e.g.*, both are LED references that teach etching through the claimed semiconductor stack in order to expose and make electrical contact with the n-type

layer—a POSITA would have recognized that any advantages achieved by Sano’s fabrication process would likewise improve Donofrio. LGI1002, ¶168. Indeed, by overetching into the first semiconductor layer (*i.e.*, n-type layer 112) of Donofrio, a POSITA would have been able to more reliably establish electrical connection between the first electrode pad and the first semiconductor layer. *Id.* Without such overetching, for example, slight variations in processing conditions may lead to insufficient exposure of the n-type layer, which in turn would lead to poor electrical contact to the electrode. *Id.*

Second, a POSITA would have considered the partial etching of the layer being exposed for electrical contact, as disclosed by Sano, to be a routine and conventional design choice given the popularity of this technique around the time period of the ’664 Patent. LGI1002, ¶¶169-170; *see also In re Magna Elecs., Inc.*, 611 Fed. Appx. 969, 974 (Fed. Cir. 2015) (citing *In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975) (finding a generic feature that “provides no novel or unexpected result” as “an obvious matter of design choice”). Indeed, many other references during this time period teach similar overetching for the purpose of ensuring reliable electrical contact. LGI1002, ¶170 (citing LGI1005, FIG. 1B; LGI1013, FIG. 1). Thus, there is nothing new or inventive, at the time of the ’664 Patent, about forming the claimed contact hole that extends into the first semiconductor layer (and subsequently covering the resulting sidewall of the first semiconductor

layer with the protective insulation layer). LGI1002, ¶170. Thus, incorporating the overetching of Sano into the etching process of Donofrio amounts to merely combining prior art elements from the same field, according to known methods to yield predictable results. *See KSR*, 550 U.S. at 417; LGI1002, ¶170.

Thus, Donofrio, either alone or in combination with Sano, renders obvious element [1e]. LGI1002, ¶¶159-170.

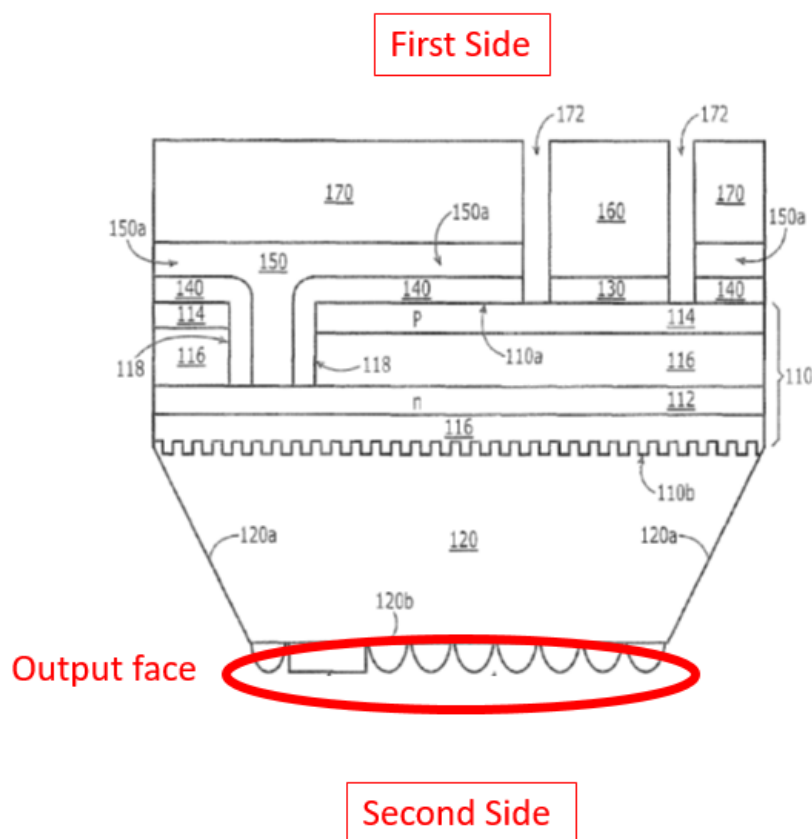
[1f]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”

Donofrio discloses element [1f]. LGI1002, ¶171. For example, Donofrio teaches that its insulating layer 140, which corresponds to the claimed protective insulation layer, “may comprise multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector.” LGI1009, [0041]. Sublayers of oxide and nitride would have different indices of refraction from each other. LGI1002, ¶171. Moreover, a “distributed Bragg reflector” is, as noted in the ’664 Patent, a structure that is “formed by alternately stacking insulation layers having different indices of refraction.” LGI1001, 6:3-7. Thus, the Donofrio-Sano combination renders obvious claim 1. LGI1002, ¶171.

Claim 2

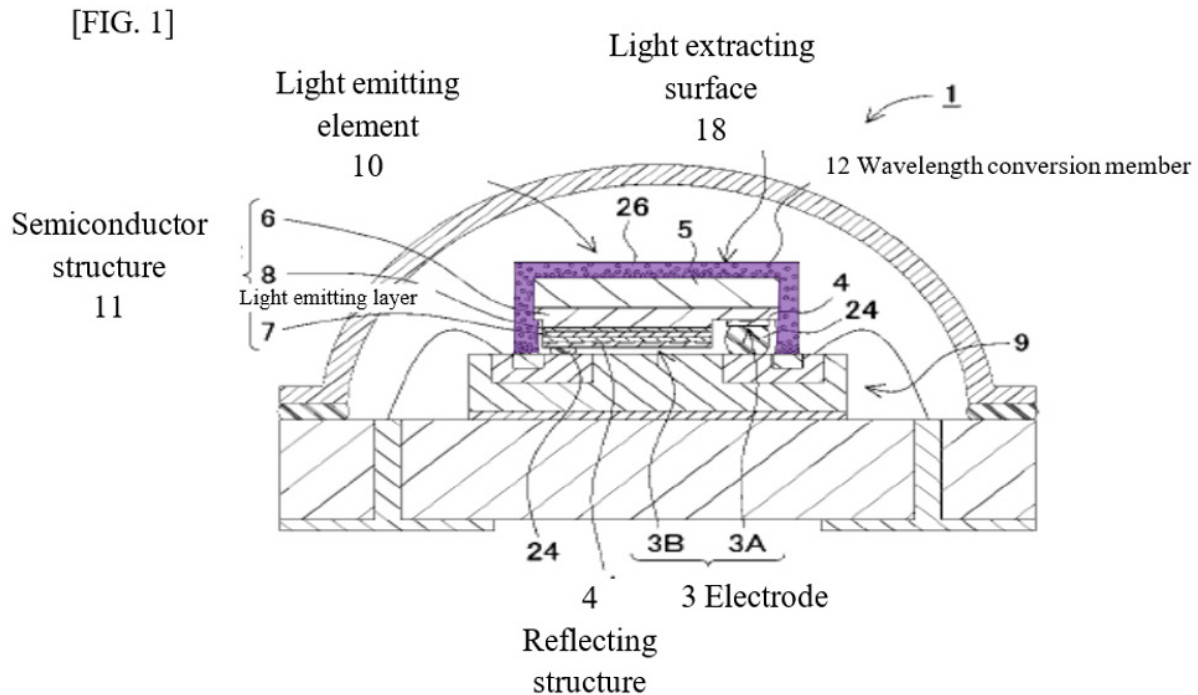
[2a]: “The LED package of claim 1, further comprising a wavelength convertor arranged over a second side of the semiconductor stack, the second side being opposite to the first side of the semiconductor stack,”

Donofrio discloses element [2a]. LGI1002, ¶¶172-174. For example, Donofrio teaches “incorporat[ing] wavelength conversion material such as phosphor.” LGI1009, [0004]. Although Donofrio doesn’t specify the location of the wavelength conversion material, a POSITA would have recognized that such material should be arranged over the output face (*i.e.*, second side) of the LED package, as illustrated below, to be able to convert the wavelength of the light being output by the LED:



LGI1009, FIG. 1 (annotated); LGI1002, ¶172 (citing to LGI1005, [0143]).

Furthermore, as illustrated below, Sano teaches arranging a wavelength conversion member 12 over a light extracting surface 18 of a flip-chip mounted LED package:



LGI1011, FIG. 1 (annotated); [0020]-[0022], [0028]; LGI1002, ¶173. By providing the wavelength conversion member 12 in this manner, Sano teaches that “desired light” can be emitted from the LED device. LGI1011, [0028].

A POSITA would have found it obvious to implement Donofrio’s LED device using Sano’s wavelength conversion member, LGI1002, ¶¶173-174. Indeed, Sano explicitly teaches that its wavelength conversion member can be applied to flip-chip mounted LED devices—like Donofrio—to emit the desired wavelength of light. LGI1011, [0028]; LGI1002, ¶173. A POSITA would have

been able to readily add Sano's wavelength conversion member to the output face of Donofrio's flip-chip mounted LED chip without substantially changing the resulting structure or function. LGI1002, ¶174. Because Donofrio expressly teaches the use of a wavelength conversion material, a POSITA would simply be relying on the compatible structure of Sano for implementation details.

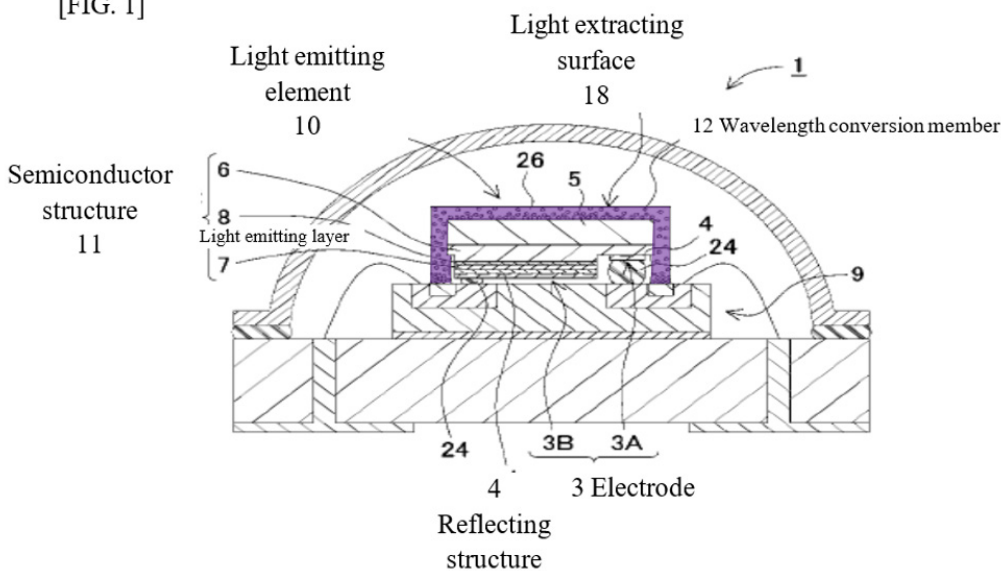
Thus, Donofrio, either alone or in combination with Sano, renders obvious element [2a]. LGI1002, ¶¶172-174.

[2b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”

Donofrio discloses element [2b]. LGI1002, ¶¶175-176. Specifically, Donofrio teaches that “wavelength conversion material ***such as phosphor***” may be used. LGI1009, [0004].

Moreover, Sano teaches the use of a phosphor-based wavelength conversion member (purple) that is the form of a sheet:

[FIG. 1]



LGI1011, FIG. 1 (annotated); [0020]-[0022], [0028]; LGI1002, ¶175. Sano further teaches the use of impurity-doped materials in its wavelength conversion member, including for example BAM:Mn, CaAlSiN₃:Eu, (Re_{1-x}Sm_x)₃(AlGa)₅O₁₂:Ce (0 ≤ x < 1, 0 ≤ y ≤ 1), (Sr_xMg_{1-x})₂SiO₄:Eu, Sr-Ca-Si-N:Eu, Ca-Si-N:Eu, Sr-Si-N:Eu, Sr-Ca-Si-O-N:Eu, Ca-Si-O-N:Eu, Sr-Si-O-N:Eu, LSi₂O₂N₂:Eu, L_xSi_yN_(2/3x+4/3y):Eu. LGI1011, [0022], [0075], [0077]; LGI1002, ¶176. For reasons discussed above for element [2a], a POSITA would have been able to readily apply Sano's wavelength conversion member to Donofrio's LED device. LGI1002, ¶174

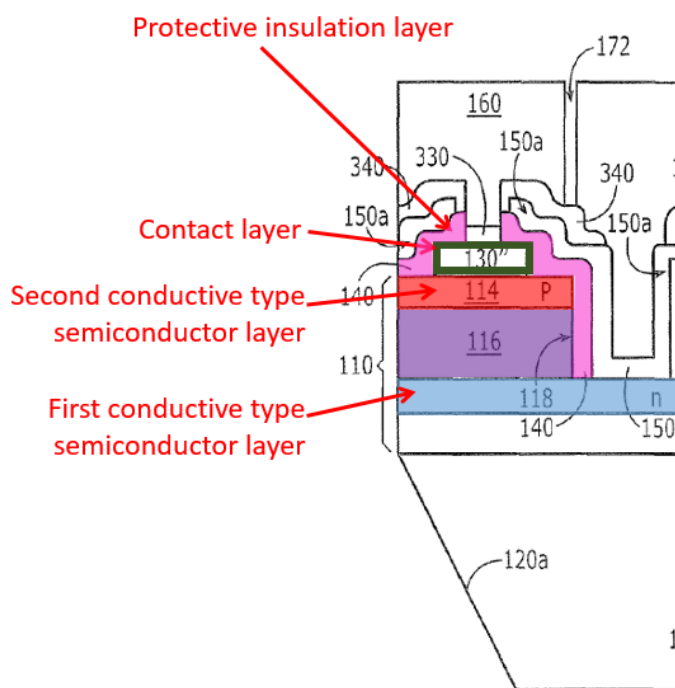
Thus, the Donofrio-Sano combination renders obvious element [2b].

LGI1002, ¶¶175-176.

Claim 3

[3a]: “The LED package of claim 1, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer”

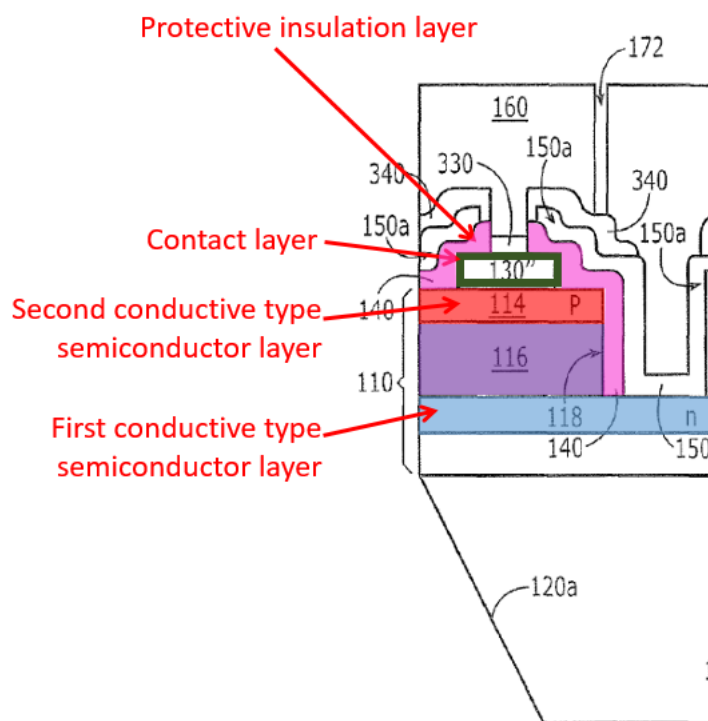
Donofrio discloses element [3a]. LGI1002, ¶177. As illustrated below, Donofrio teaches a “transparent anode contact 130” (green) that is positioned over the second conductive type semiconductor layer (red):



LGI1009, FIG. 3 (cropped, annotated); [0065]; LGI1002, ¶177. Donofrio further teaches that its transparent anode contact layer “may be a transparent conductive oxide, such as indium tin oxide (ITO).” LGI1009, [0065].

[3b]: “a part of the transparent conductive oxide film contact layer or the reflective metal layer is formed between the second conductive type semiconductor layer and the protective insulation layer.”

Donofrio discloses element [3b]. LGI1002, ¶178. As illustrated below, a part of the transparent conductive oxide film contact layer (green) of Donofrio is positioned between the second conductive type semiconductor layer (red) and the protective insulation layer (pink):



LGI1009, FIG. 3 (cropped, annotated); LGI1002, ¶178. Thus, the Donofrio-Sano combination renders obvious claim 3.

Claim 4

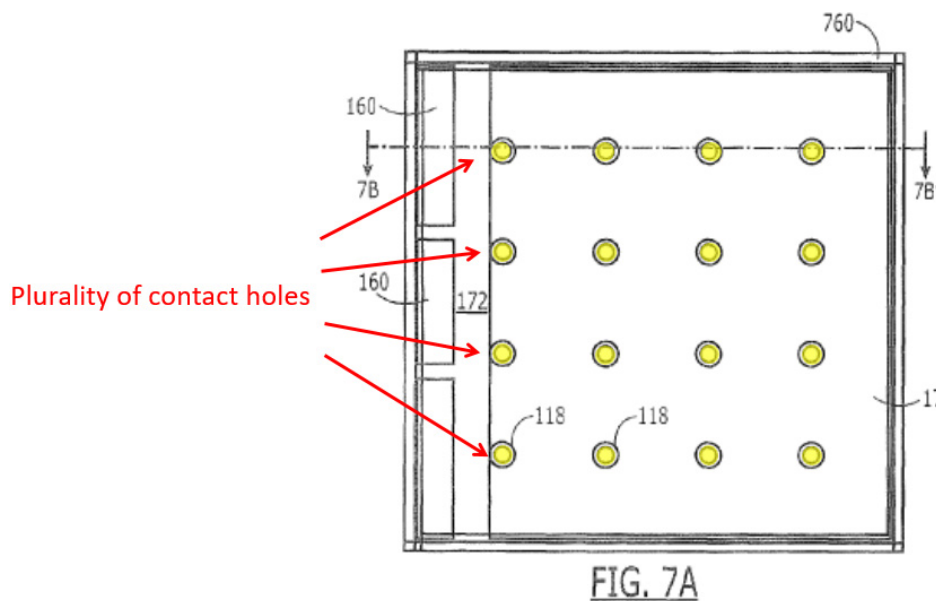
[4a]: “The LED package of claim 3, wherein the transparent conductive oxide film contact layer includes an ITO (Indium Tin Oxide).”

Donofrio discloses element [4a]. LGI1002, ¶179. In particular, as discussed above for element [3b], Donofrio teaches that its transparent anode contact layer “may be a transparent conductive oxide, such as indium tin oxide (ITO).” LGI1009, [0065]. Thus, the Donofrio-Sano combination renders obvious claim 4. LGI1002, ¶179.

Claim 5

[5a]: “The LED package of claim 4, wherein at least one of the contact holes has a circular shape, and”

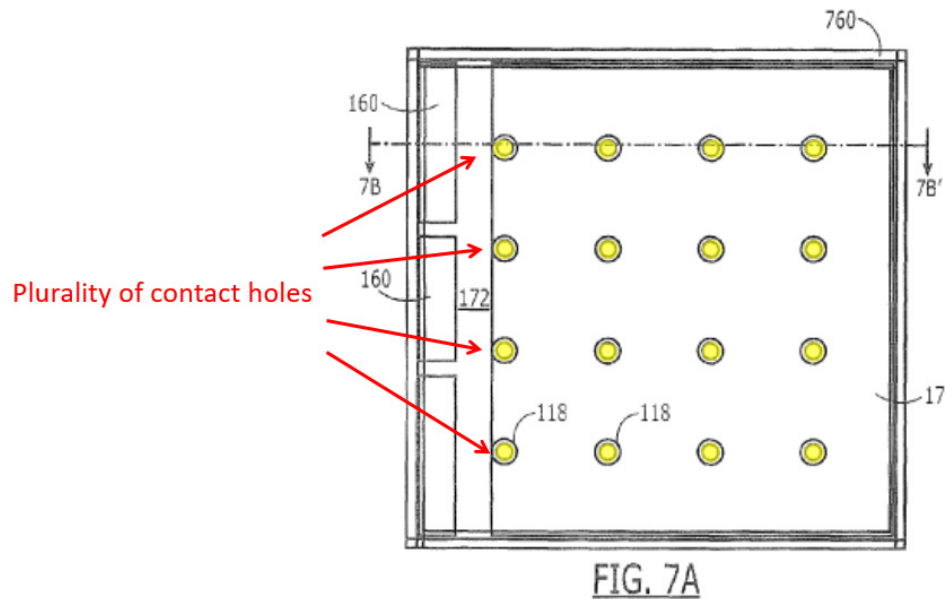
Donofrio discloses element [5a]. LGI1002, ¶180. For example, as seen in FIG. 7A below, the vias 118 (*i.e.*, contact holes) of Donofrio have a circular shape:



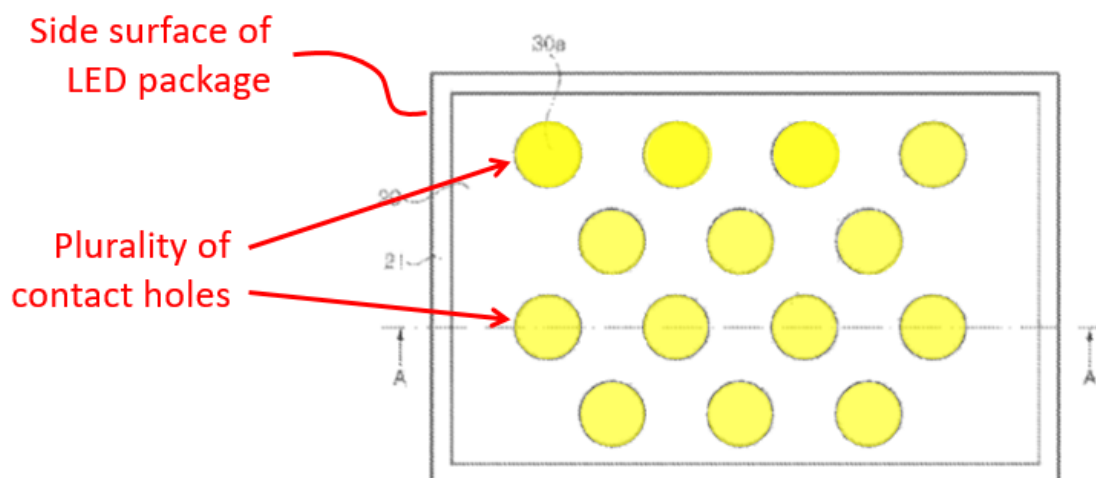
LGI1009, FIG. 7A (annotated); LGI1002, ¶180.

[5b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”

Donofrio discloses element [5b]. LGI1002, ¶¶181-182. For example, as seen in FIG. 7A below, the vias 118 (*i.e.*, contact holes) of Donofrio are arranged along at least one side surface of the LED package:



LGI1005, FIG. 7A (annotated); LGI1002, ¶181. Indeed, Donofrio's arrangement of its contact holes along the side surface of the LED package corresponds to that shown in the '664 Patent:



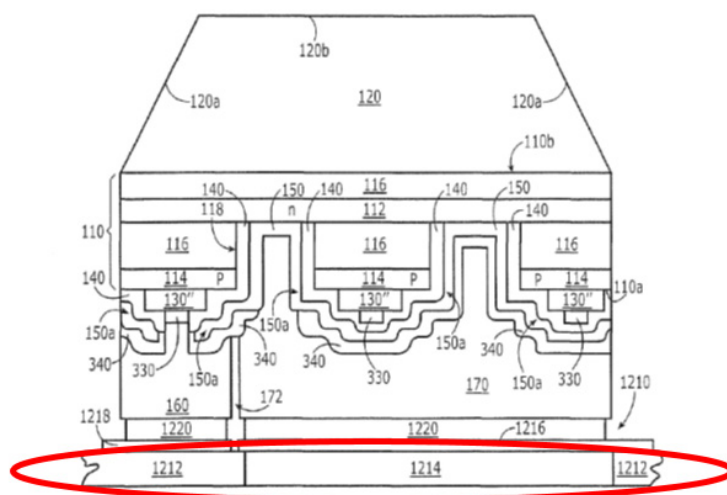
LGI1001, FIG. 5(a) (annotated); LGI1002, ¶182.

Thus, the Donofrio-Sano combination renders obvious claim 5. LGI1002, ¶¶181-182.

Claim 6

[6pre]: “A light emitting diode (LED) module, comprising:”

To the extent the preamble is limiting, which Petitioner does not concede, Donofrio discloses element [6pre]. LGI1002, ¶183. Initially, as noted above for element [1pre], Donofrio teaches an LED component. LGI1009, [0046], [0050]. Additionally, Donofrio teaches that its LED component is “suitable for flip-chip mounting” and can be “mounted on a supporting substrate, such as a printed circuit board or other wiring board.” LGI1009, [0046]. The LED component of Donofrio, as mounted on a mounting substrate 1210, is shown below:



LGI1009, FIG. 12 (annotated); [0091]. An LED component package that is mounted on a circuit board, as shown above, is a LED module. LGI1002, ¶183 (citing LGI1014).

[6a]: “a circuit board;”

Donofrio discloses element [6a]. LGI1002, ¶¶183-184. For example, Donofrio teaches that its LED component can be “mounted on a supporting substrate, such as a printed circuit board or other wiring board.” LGI1009, [0046]; FIG. 12; LGI1002, ¶¶183-184.

[6b]: “a LED package arranged over the circuit board without bonding wires, wherein the LED package includes:”

Donofrio discloses element [6a]. LGI1002, ¶185. Specifically, Donofrio teaches an LED package that is “suitable for flip-chip mounting.” LGI1009, [0046]. A flip-chip architecture, as utilized in Donofrio as well as the ’664 Patent, allows the LED chip to be mounted directly without the use of bonding wires.

LGI1002, ¶185. Indeed, the parent application to Donofrio, which is incorporated by reference, is entitled “Wire Bond Free Wafer Level LED,” thus further confirming Donofrio’s objective of eliminating the need for bonding wires through its flip-chip configuration. LGI1009, [0001]; LGI1002, ¶185.

[6c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Donofrio discloses element [6c]. See Ground 2A [1a]; LGI1002, ¶¶152-153, 186.

[6d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Donofrio discloses element [6d]. See Ground 2A [1b]; LGI1002, ¶¶154, 187.

[6e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Donofrio discloses element [6e]. See Ground 2A [1c]; LGI1002, ¶¶155-156, 188.

[6f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

Donofrio discloses element [6f]. See Ground 2A [1d]; LGI1002, ¶¶157-158, 189.

[6g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,”

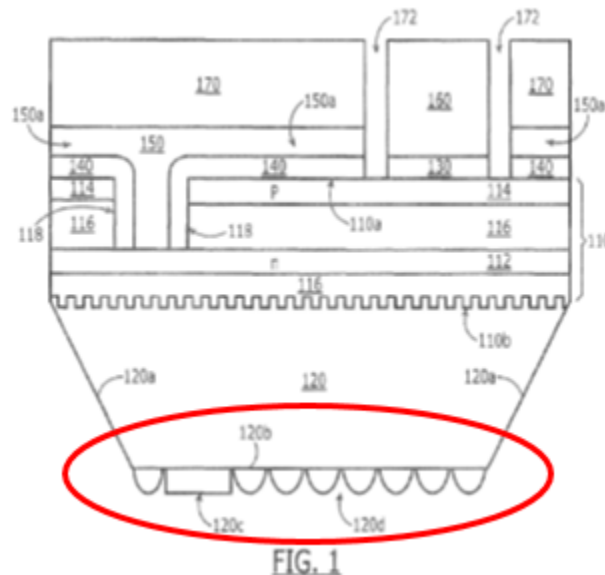
Donofrio discloses element [6g]. See Ground 2A [1e]; LGI1002, ¶¶159-170, 190.

[6h]: “wherein the protective insulation layer includes insulation layers having different indices of refraction from each other; and”

Donofrio discloses element [6h]. See Ground 2A [1f]; LGI1002, ¶¶171, 191.

[6i]: “a lens to adjust an orientation angle of light emitted from the LED package.”

Donofrio discloses element [6i]. LGI1002, ¶192. For example, as shown below, Donofrio teaches that its light output face can include microlenses, lenticular lenses, and other enhancement features to enhance light extraction:



LGI1009, FIG. 1 (annotated); [0047]; [0094]; LGI1002, ¶192. The lenses of Donofrio located at the output face of the LED, by shaping the output beam

through optical refraction, serve to adjust an orientation angle of light emitted from the LED package. LGI1002, ¶192.

For these reasons, the combination of Donofrio and Sano renders obvious claim 6.

Claim 7

[7a]: “The LED module of claim 6, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and the LED packages is arranged over the MC-PCB.”

Donofrio discloses element [7a]. LGI1002, ¶193. Specifically, Donofrio discloses that various “mounting substrates, such as ***metal core substrates***, printed circuit boards, lead frames and/or other conventional mounting substrates, may be used to mount many of the embodiments described herein in a flip-chip configuration.” LGI1009; [0093]. For these reasons, the combination of Donofrio and Sano renders obvious claim 7.

Claim 8

[8pre]: “A light emitting diode (LED) module, comprising:”

Donofrio discloses element [8pre]. See Ground 2A [6pre]; LGI1002, ¶¶183, 194.

[8a]: “a circuit board;”

Donofrio discloses element [8a]. See Ground 2A [6a]; LGI1002, ¶¶184, 195.

[8b]: “a LED package bonded on the circuit board without bonding wires; wherein the LED package comprising”

Donofrio discloses element [8b]. See Ground 2A [6b]; LGI1002, ¶¶185, 196. Specifically, a flip-chip architecture, as utilized in Donofrio as well as the '664 Patent, allows the LED chip to be bonded directly on the circuit board without the use of bonding wires. LGI1002, ¶196.

[8c]: “a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;”

Donofrio discloses element [8c]. See Ground 2A [6c]; LGI1002, ¶¶152-153, 186, 197.

[8d]: “a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;”

Donofrio discloses element [8d]. See Ground 2A [6d]; LGI1002, ¶¶154, 187, 198.

[8e]: “a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;”

Donofrio discloses element [8e]. See Ground 2A [6e]; LGI1002, ¶¶155-156, 188, 199.

[8f]: “a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and”

Donofrio discloses element [8f]. See Ground 2A [6f]; LGI1002, ¶¶157-158, 189, 200.

[8g]: “a protective insulation layer covering a sidewall of the first conductive type semiconductor layer.”

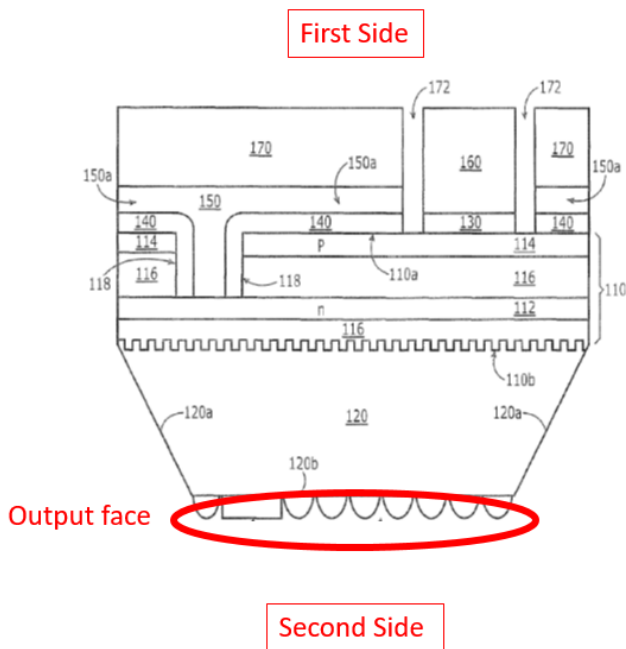
Donofrio discloses element [8g]. See Ground 2A [1e] and [6g]; LGI1002, ¶¶159-170, 190, 201.

For these reasons, the combination of Donofrio and Sano renders obvious claim 8.

Claim 9

[9a]: “The LED module of claim 8, further comprising a wavelength converter over the opposite side of the LED package to the first and second electrode pads,”

Donofrio discloses element [9a]. See Ground 2A [2a]; LGI1002, ¶202. Moreover, the second side of the semiconductor stack, as discussed above for Ground 2A [2a] and illustrated in the annotated drawing below, is on the opposite side of the LED package to the first and second electrode pads 170, 160:



LGI1009, FIG. 1 (annotated); LGI1002, ¶202.

[9b]: “wherein the wavelength convertor comprises a phosphor sheet or an impurity-doped material.”

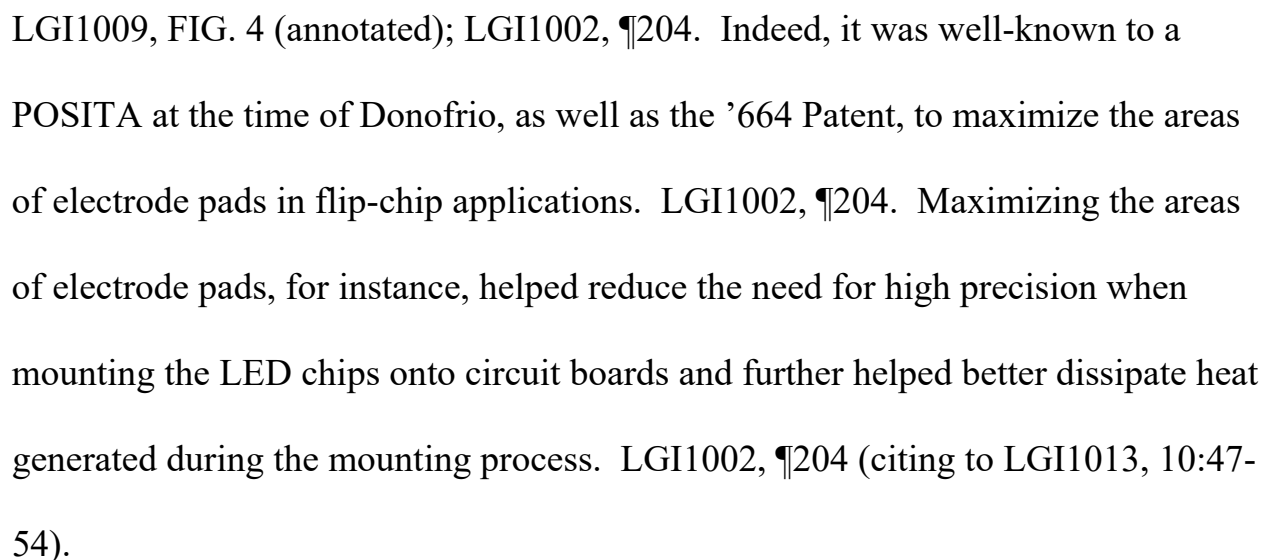
Donofrio discloses element [9b]. *See* Ground 2A [2b]; LGI1002, ¶¶175-176, 203.

For these reasons, the combination of Donofrio and Sano renders obvious claim 9.

Claim 10

[10a]: “The LED module of claim 9, wherein each area of the first and second pads has an area not less than $\frac{1}{3}$ of the LE package.”

Donofrio discloses element [10a]. LGI1002, ¶¶204-206. For example, as seen in FIG. 4 below, the first and second pads of Donofrio, shown in green and



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Further, a plethora of prior art during this time period expressly teach maximizing the areas of electrode pad pairs to each cover about half the total area of the LED chip. LGI1002, ¶206 (citing to LGI1013, 10:47-54). That is, a POSITA would have recognized that maximizing the areas of the electrode pads such that each covers approximately half the area of the LED chip—*i.e.*, each pad covering an area not less than 1/3 of the LED package—is a simple and routine design choice that would allow the flip-chip type component of Donofrio to be more easily mounted during manufacturing. LGI1002, ¶¶205-206. For these reasons, the combination of Donofrio and Sano renders obvious claim 10.

Claim 11

[11a]: “The LED module of claim 8, further comprises a lens to adjust an orientation angle of light emitted from the LED package.”

Donofrio discloses element [11a]. *See* Ground 2A [6i]; LGI1002, ¶¶192, 207.

For these reasons, the combination of Donofrio and Sano renders obvious claim 11.

Claim 12

[12a]: “The LED module of claim 8, wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.”

Donofrio discloses element [12a]. *See* Ground 2A [1f]; LGI1002, ¶¶171, 208.

For these reasons, the combination of Donofrio and Sano renders obvious claim 12.

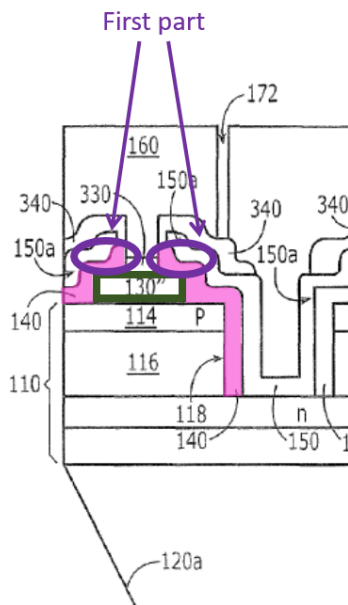
Claim 13

[13a]: “The LED module of claim 12, further comprising a transparent conductive oxide film contact layer or a reflective metal layer over the second conductive type semiconductor layer; and”

209.

[13b]: “a first part of the protective insulation layer covering the contact layer.”

FIG. 3 below, the protective insulation layer (pink) includes a horizontal portion, labeled as “first part,” that covers an upper side of the contact layer (green):

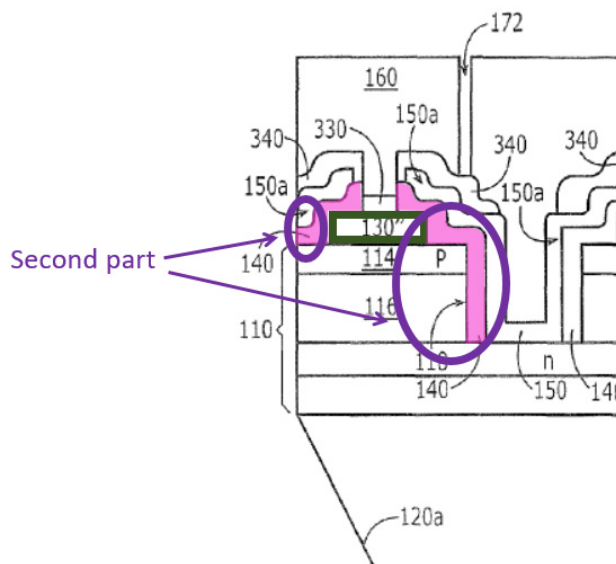


LGI1009, FIG. 3 (cropped, annotated); LGI1002, ¶210. For these reasons, the combination of Donofrio and Sano renders obvious claim 13.

Claim 14

[14a]: “The LED module of claim 13, wherein a second part of the protective insulation layer covers the sidewall of the first conductive type semiconductor layer,”

Donofrio discloses element [14a]. LGI1002, ¶211. For example, as seen in FIG. 3 below, the protective insulation layer (pink) includes vertical portions, labeled as “second part,” that covers the sidewall of the first conductive type semiconductor layer:

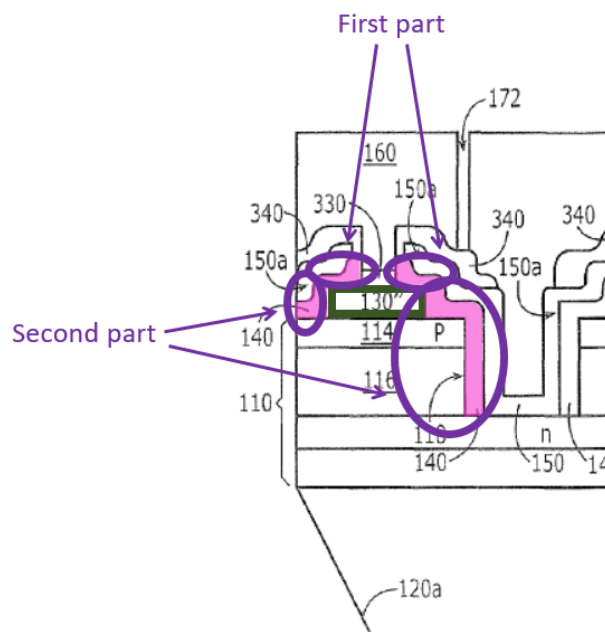


LGI1009, FIG. 3 (cropped, annotated); *see analysis for Ground 2A [1e]*; LGI1002, ¶211.

[14b]: “the second part of the protective insulation layer contacts the first part of the protective insulation layer.”

Donofrio discloses element [14b]. LGI1002, ¶212. For example, as seen in FIG. 3 below, the protective insulation layer (pink) includes horizontal portions

(labeled “first part”) and vertical portions (labeled “second part”) that contact each other:



LGI1009, FIG. 3 (cropped, annotated); LGI1002, ¶212. For these reasons, the combination of Donofrio and Sano renders obvious claim 14.

Claim 15

[15a]: “The LED module of claim 14, wherein each area of the first and second pads is not less than $\frac{1}{3}$ of area of the LED package.”

Donofrio discloses element [15a]. See Ground 2A [10a]; LGI1002, ¶¶204-206, 213. For these reasons, the combination of Donofrio and Sano renders obvious claim 15.

Claim 16

[16a]: “The LED module of claim 15, further comprising a wavelength convertor the opposite side of the LED package to the first and second electrode pads,”

Donofrio discloses element [16a]. See Ground 2A [9a]; LGI1002, ¶¶202, 214.

[16b]: “wherein the wavelength converter comprises a phosphor sheet or an impurity-doped material.”

Donofrio discloses element [16b]. See Ground 2A [9b]; LGI1002, ¶¶175-176, 203, 215. For these reasons, the combination of Donofrio and Sano renders obvious claim 16.

Claim 17

[17a]: “The LED module of claim 16, at least one of the contact holes has a circular shape, and”

Donofrio discloses element [17a]. See Ground 2A [5a]; LGI1002, ¶¶180, 216.

[17b]: “wherein the plurality of the contact holes are arranged along at least one side surface of the LED package.”

Donofrio discloses element [6c]. See Ground 2A [5b]; LGI1002, ¶¶181-182, 217. For these reasons, the combination of Donofrio and Sano renders obvious claim 17.

Claim 18

[18a]: “The LED module of claim 17, further comprising a lens to adjust an orientation angle of light emitted from the LED package.”

Donofrio discloses element [18a]. *See* Ground 2A [6i]; LGI1002, ¶¶192, 218.

For these reasons, the combination of Donofrio and Sano renders obvious claim 18.

Claim 19

[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”

Donofrio discloses element [19a]. *See* Ground 2A [7a]; LGI1002, ¶¶193, 219.

[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”

Donofrio discloses element [19b]. LGI1002, ¶220. For example, Donofrio teaches mounting LED chips on various types of mounting substrates, including MC-PCB. LGI1009, [0093]; LGI1002, ¶220. To the extent Donofrio does not expressly show mounting multiple LED chips on a single circuit board, a POSITA would have found it obvious to mount multiple chips on an MC-PCB to, for example, mix different types of LEDs and/or to maximize light output. LGI1002, ¶220 (citing LGI1008). For these reasons, the combination of Donofrio and Sano renders obvious claim 19.

B. [GROUND 2B]: Claim 19 is rendered obvious by Donofrio in view of Sano and Begemann

Claim 19

[19a]: “The LED module of claim 17, wherein the circuit board comprises a metal core printed circuit board (MC-PCB), and”

Donofrio in view of Sano renders obvious element [19a]. *See* Ground 2A [7a]; LGI1002, ¶¶193, 223.

[19b]: “a plurality of the LED packages is arranged on the MC-PCB.”

Donofrio and Sano further in view of Begemann discloses element [19b]. LGI1002, ¶¶224-225. Specifically, Donofrio teaches mounting LED chips on various types of mounting substrates, including MC-PCB. LGI1009, [0093]; LGI1002, ¶224. To the extent Donofrio doesn’t expressly disclose arranging a ***plurality of LED packages*** on the MC-PCB, Begemann provides this feature. *Id.*

For example, as shown below, Begemann explicitly teaches mounting multiple LED chips onto an MC-PCB:

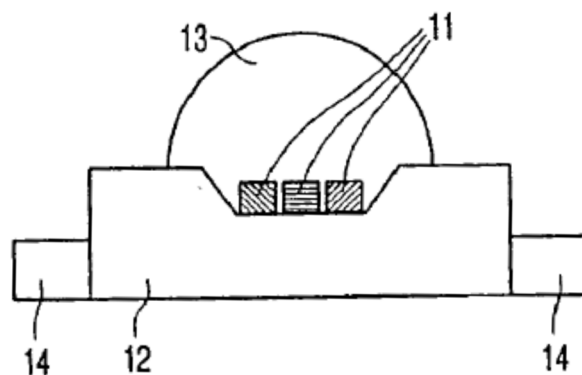


FIG. 3B

LGI1008, FIG. 3B; [0029]. A POSITA would have considered the mounting of multiple LED packages on an MC-PCB to be obvious and a routine and conventional design choice. LGI1002, ¶225; *see also In re Magna Elecs., Inc.*, 611 Fed. Appx. 969, 974 (Fed. Cir. 2015) (citing *In re Kuhle*, 526 F.2d 553, 555

(CCPA 1975) (finding a generic feature that “provides no novel or unexpected result” as “an obvious matter of design choice”). Indeed, the arrangement of a plurality of LED packages on an MC-PCB, as evidenced by Begemann, was common practice in the field of LED design and manufacturing, and there was nothing new or inventive about changing the number of LED packages being mounted or even the type of circuit board being utilized at the time of the ’664 Patent. LGI1002, ¶225. Thus, incorporating the multiple-chip configuration of Begemann into the LED device of Donofrio in view of Sano amounts to merely combining prior art elements from the same field, according to known methods to yield predictable results. *See KSR*, 550 U.S. at 417; LGI1002, ¶225.

Thus, the Donofrio-Sano-Begemann combination renders obvious element [19b]. LGI1002, ¶¶224-225. For these reasons, the combination of Donofrio, Sano, and Begemann renders obvious claim 19.

IV. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 06-1050 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

V. CONCLUSION

Petitioner requests *inter partes* review of the Challenged Claims pursuant to

Grounds 1A-1C and 2A-2B.

VI. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

LG Innotek Co. Ltd. is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for *inter partes* review for the '664 Patent. The '664 Patent is the subject of a civil action styled *Seoul Semiconductor Co. et al v. Fry's Electronics, Inc*, No. 2:18-cv-00386-JRG (E.D. Tex.).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR38191-0005IP1@fr.com

(referencing Docket No. 38191-0005IP1 and cc'ing PTABInbound@fr.com,
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Respectfully submitted,

Dated June 11, 2019

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *inter partes* review totals 13,785 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated June 11, 2019

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on June 11, 2019, a complete and entire copy of this Petition for *inter partes* review and all supporting exhibits were provided via Priority Mail Express, to the Patent Owner by serving the correspondence address of record as follows:

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