

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG INNOTEK CO. LTD.,

Petitioner,

v.

SEOUL SEMICONDUCTOR CO., LTD.,

Patent Owner.

Case IPR2019-01154

Patent 9,293,664

**PATENT OWNER PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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EXHIBIT LIST

Ex. 2001 Declaration of Dr. William Alan Doolittle (with appendices A-S)

I. Introduction

LG Innotek Co. Ltd. (“Petitioner”) filed its petition (the “Petition”) for *inter partes* review (“IPR”) against U.S. Pat. No. 9,293,664 (the “’664 Patent”) alleging 5 different grounds as listed at Page 1 of the Petition:

Ground	’664 Patent Claims	Basis for Rejection
Ground 1A	1-6, 8, 9, 11, 12	§102 over Illek
Ground 1B	1-6, 8-18	§103 over Illek
Ground 1C	7, 19	§103 over Illek and Begemann
Ground 2A	1-19	§103 over Donofrio and Sano
Ground 2B	19	§103 over Donofrio, Sano, and Begemann

As shown by the evidence and analyses in this filing, Petitioner has failed to establish a reasonable likelihood of success, and the Petition should be denied under 35 U.S.C. § 314(a).

Every challenged claim in the ’664 Patent requires a “protective insulation layer.” The ’664 Patent describes this layer as being important to protect the semiconductor device from the external environment, thus preventing deterioration of the device’s semiconductor layers due to the influence of external environmental factors such as moisture. None of Petitioner’s primary references—Illek and Donofrio—teach the “protective insulation layer.”

Petitioner’s allegation ignores the protective aspect of the limitation, and only establishes that its references teach a layer that electrically isolates and

performs other functions, but not one that provides protection. Demonstrating the lack of a protective layer, Petitioner's Ground 1A–B reference (Illek) teaches adding a protective encapsulation on top of what Petitioner alleges is the protective insulation layer. But Petitioner's contention lacks logic and makes no sense—why
5 would a protective encapsulant be added to protect protective layers? Illek's encapsulation demonstrates that the layers it covers do not provide protection. Petitioner's Ground 2A–B reference (Donofrio) does not teach any protection at all. Further, its semiconductor is completely exposed to the environment and would be subject to deterioration.

10 Petitioner's only allegation that the layers themselves protect is that they are made of certain materials. But Petitioner—and its expert without analysis—merely declared that these materials protect but they provided no fact or evidence in the cited prior art or any other evidence to support their contention. These materials in the cited prior art by Petitioner are not inherently protective, and this is
15 demonstrated by the teachings in the prior art and by the evidence provided in the declaration of Dr. William Alan Doolittle of Georgia Tech. Dr. Doolittle provides various examples regarding how these materials would be designed to lack protection. And designing a layer to lack protection is designed to—it makes the structure less rigid and prone to cracking. The materials identified by Petitioner
20 simply do not inherently provide protective functions. The Petition lacks the

evidence to support Petitioner's invalidity grounds and there is no basis in the Petition and in the declaration of Petitioner's expert for a finding of a reasonable likelihood for any of claims 1–19.

In addition, Petitioner has not established that there is any motivation to
5 combine its references in Grounds 2A–B (a combination of Illek and Sano and another of Illek, Sano and Begemann). Petitioner seized on a technical concept—over-etching—and applied it as a justification to combine the entirety of Donofrio and Sano in a contrived way that has no technical basis in Illek, Sano or/and Begemann. Petitioner provided no reasons or motivation in the cited references or
10 any other suitable source that would justify the combination.

Furthermore, Petitioner has failed to demonstrate a reasonable likelihood that it will prevail with respect to any of claims 1–19 under 35 U.S.C. § 314(a).

Patent Owner respectfully requests that the Petition be denied.

II. The '664 Patent

15 The '664 Patent is directed to a more efficient LED. '664 Patent at 1:23–26; 2:47–49; *see also* EX2001 at ¶ 28.¹ Higher efficiency is obtained by protecting the semiconductor stack from moisture—to reduce deterioration—during the wafer-level fabrication process. *See, e.g.*, '664 Patent at 7:28–29; 13:49–50.

¹ Patent Owner has submitted as evidence the declaration of Dr. William Alan Doolittle.

A. The Improved Device Of The '664 Patent

Shown below in Fig. 12 is an illustration of the improved LED, with a few relevant features annotated. *See* '664 Patent at 4:26–28. The LED package includes a semiconductor stack 30 (green) that comprises two conductive semiconductor layers and an active layer. *Id.* at 5:22–26. Surrounding the semiconductor stack 30 is a protective insulation layer that includes a first protective insulation layer 33 and/or a second protective insulation layer 37. *Id.* at 5:59-6:31; 7:19–21; FIG. 12. This protective insulation layer is insulating and provides electrical insulation. *Id.* Importantly, the protective insulation layer provides protection from the external environment and thus prevents deterioration of the light-emitting semiconductor stack 30 (green) due to influences of the external environment such as moisture. *See id.* at 7:17–42; 13:38–58; FIG. 14; *see also id.* at 10:43–44 (stating that the packages are separated). As can be seen from the example in FIG. 12 of the '664 Patent reproduced below, the sidewalls of the LED are fully covered by the protective insulation layer, with at least one protective insulation layer 33 (in red) or 37 (in blue), or both layers 33 and 37. *See also* EX2001 at ¶¶ 28–37, 43.

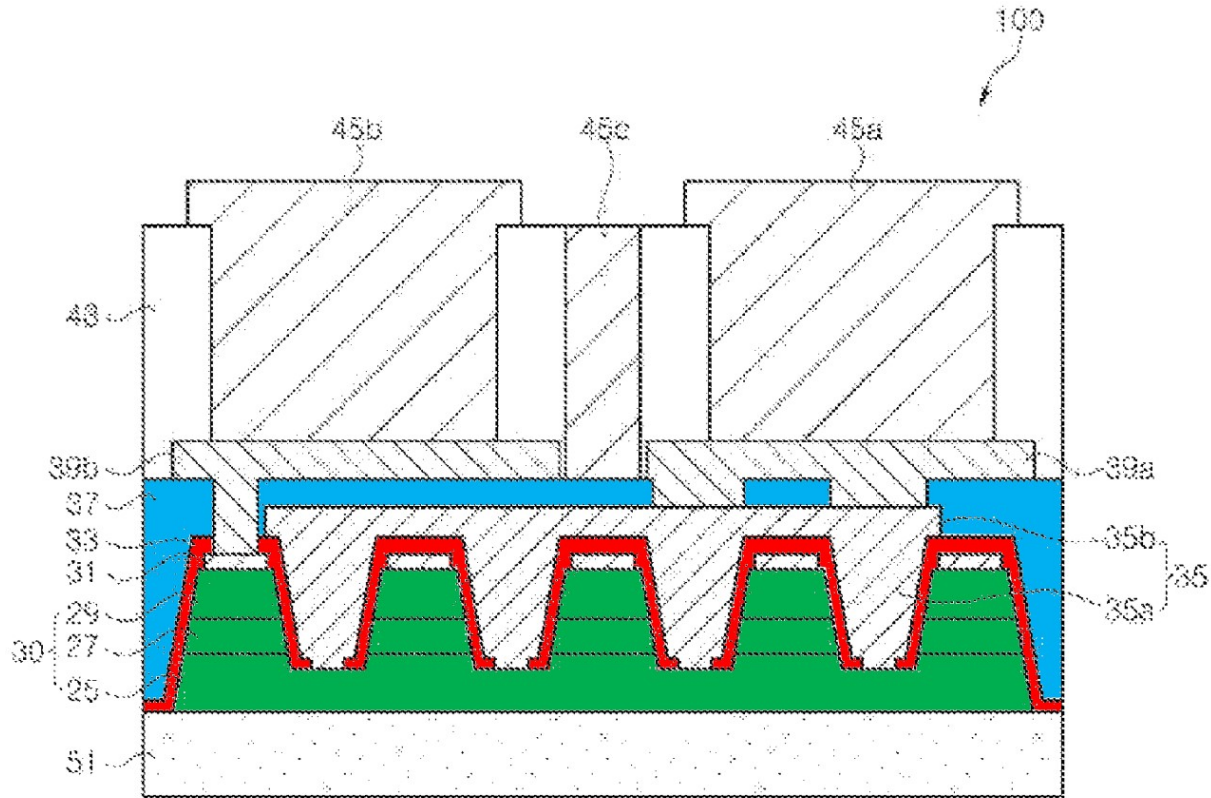


FIG. 12 of the '664 Patent (Annotated)

Furthermore, the protective insulation layer, in addition to being protective and insulating, can be implemented with different indices of refraction surrounding the semiconductor stack 30 to perform as an optical reflector to improve the optical output efficiency of final LED device. *See* '664 Patent at 5:59-6:31; FIG. 1; 9:8-53; FIG. 9; 11:50-12:20; FIG. 14; 15:18-28; 15:43-50; FIG. 22.

B. The Steps To Arrive At The Improved Device

The '664 Patent discloses the protective insulation layer that prevents deterioration of the semiconductor during wafer-level fabrication, before any

single LED device is separated. *See* '664 Patent at 1:23–26; 2:50–55; *see also id.* at 7:30–42; *see also* EX2001 at ¶¶ 30–35. Provided below is a discussion of the steps demonstrating how the claimed LED is created. *See, e.g., id.* at 4:26–38; 8:15-18; and FIGS. 4 through 12.

5 First, the semiconductor structure 30 (green) is formed on a growth substrate 21 (aqua). *See* '664 Patent at 8:15–18; Fig. 4.

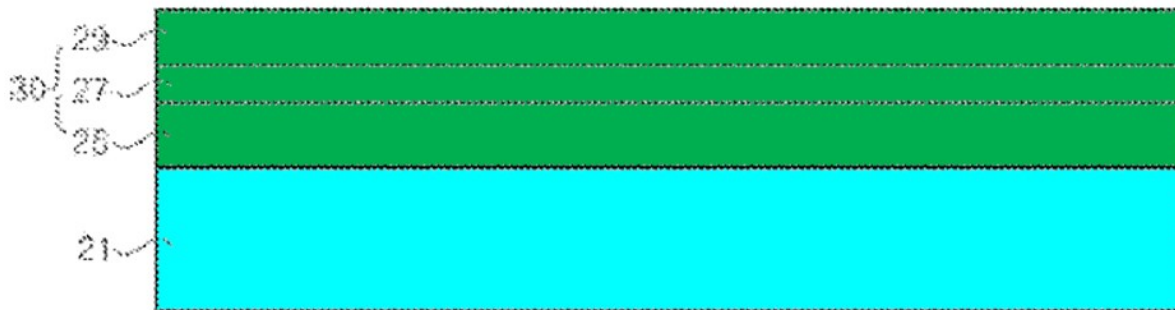


FIG. 4 of the '664 Patent (Annotated)

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The semiconductor substrate 30 (green) is structured to include an active layer 29 and two semiconductor layers 25 and 29 of different conductivity types and is etched to form holes 30a (circled) to allow access to the semiconductor layer 25 from the side having the other semiconductor layer 29. *See, e.g.,* '664 Patent at 8:40–46. A second contact layer 31 (orange) is then formed to provide an electrical contact to the semiconductor layer 29. *See id.* at 8:61–65.

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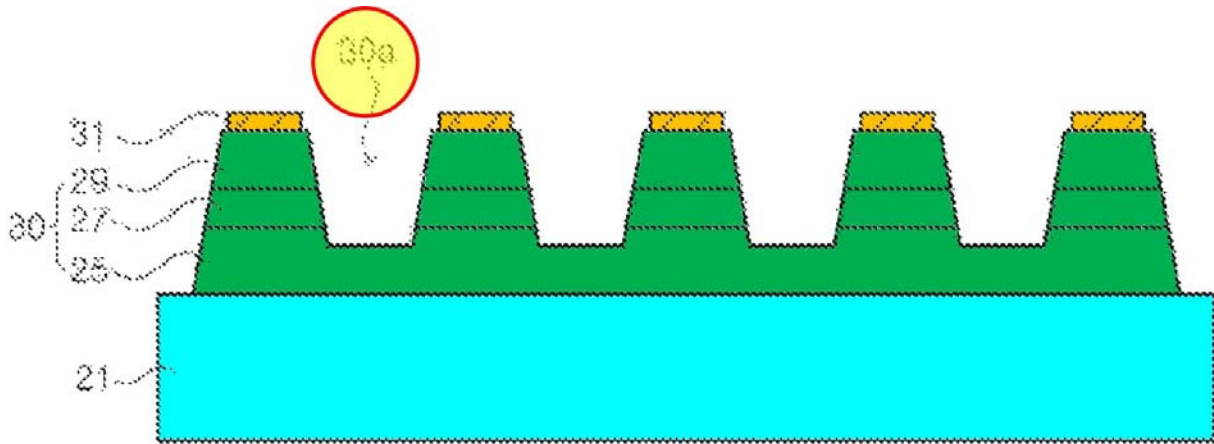


FIG. 6(b) of the '664 Patent (Annotated)

At this point in the process, the first protective insulation layer 33 (red) is
5 formed to cover the second contact layer 31 (orange). '664 Patent at 9:8–15.

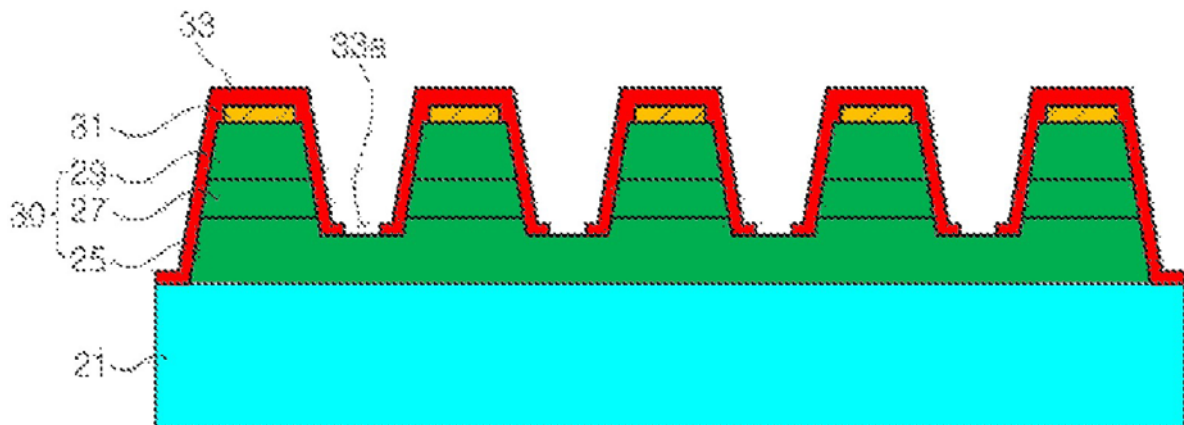


FIG. 7(b) of the '664 Patent (Annotated)

Following the above, a first contact layer 35 (also annotated orange) is formed in the holes 30a to provide an electrical contact to the semiconductor layer 25.

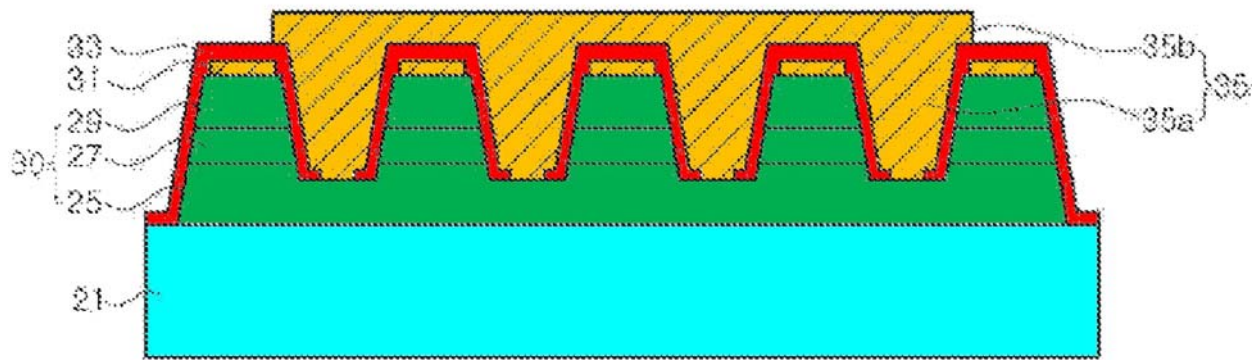
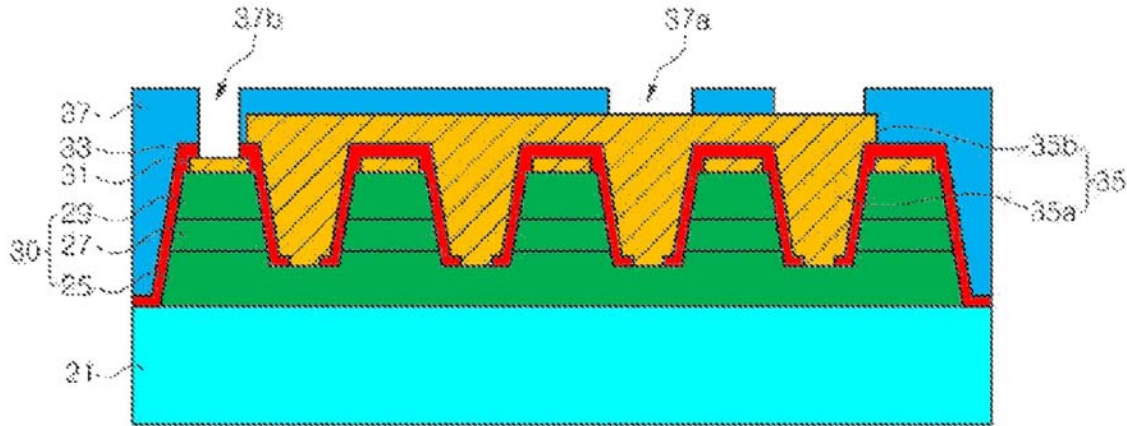


FIG. 8(b) of the '664 Patent (Annotated)

Specifically, the first contact layer 35 includes contact sections 35a contacting the first conductive type upper semiconductor layer 25, and a connecting section 35b connecting the contact sections 35a to each other. Therefore, the contact sections 35a are electrically connected to each other by the connecting section 35b. *Id.* at 9:27-34 and 6:8-18.

Thereafter, a second protective insulation layer 37 (blue) is formed onto the first contact layer 35 (orange). '664 Patent at 9:39-59. The second insulation layer is formed with holes 37a and b to expose the contact layers. *See id.* The first

and second protective insulation layers 33 and 37 protect the semiconductor structure (green) from deterioration due to moisture. *See id.* at 7:17–29.



5

FIG. 9(b) of the '664 Patent (Annotated)

Other elements (*e.g.*, the insulation layer 43 and bumps 45, not annotated) are thereafter formed. *See, e.g.*, '664 Patent at Figs. 10–12; 9:54–59; 9:65–67. The “LED package structure [is then] divided into individual packages along the chip separating region.” *Id.* at 10:43–44. The chip separating regions (annotated in
10 purple dashes, below) are locations in the wafer where the individual LEDs would be cut. *See, e.g.*, EX2001 at ¶ 35; *see also* '664 Patent at Fig. 5. Although each figure shown above was of a single chip region, a POSITA would understand that the representation was merely of a section of the entire wafer. *See* EX2001 at ¶ 35;
15 *see also* '664 Patent at 1:23–26; 2:35–55.

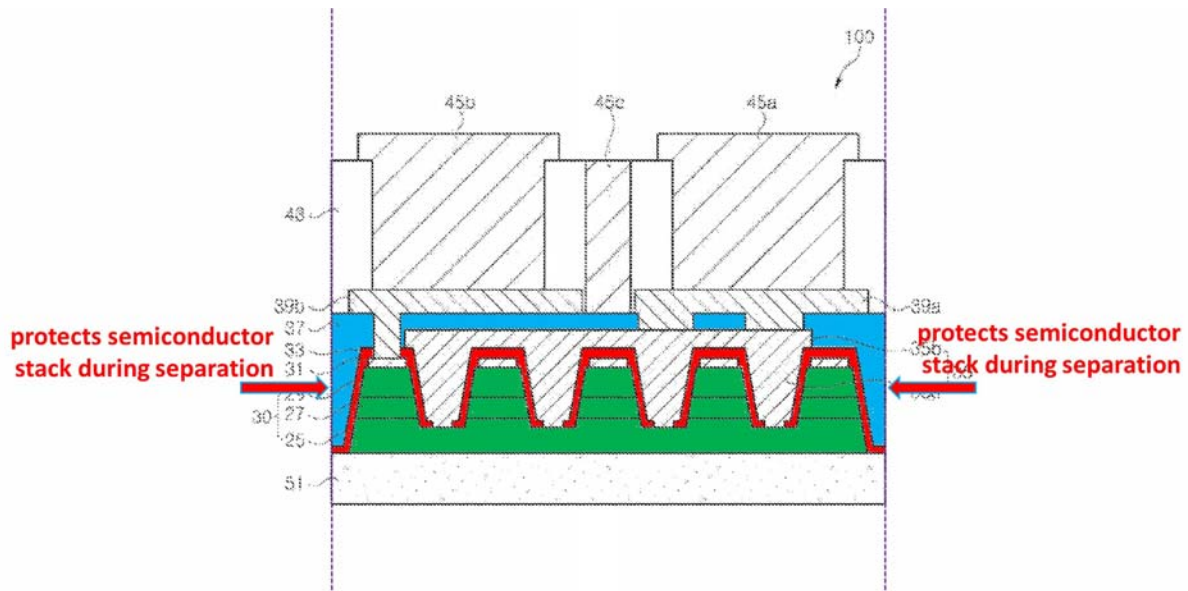


FIG. 12 of the '664 Patent (Annotated)

5 The protective insulation layer (annotated red and blue, above) protects the semiconductor stack 30 (green) during the chip separation process and subsequently throughout the life of the chip. *See, e.g., '664 Patent at 7:30–42 and 13:38–58.* The protective insulation layer prevents against influences from the external environment such as moisture from entering the semiconductor stack and
10 causing deterioration. *See, e.g., id. at 7:27–28 and 13:49–50.* By reducing semiconductor stack deterioration during wafer level fabrication, the final LEDs perform at a higher efficiency. EX2001 at ¶ 37.

 If the LED chips fabricated on a wafer are separated without protective insulation, the semiconductor stack in each LED chip will be exposed to

environmental conditions such as moisture during the separation process and subsequent packaging. In that case, the LED would suffer from deterioration. Even if protection were later added, *e.g.*, through a package and encapsulation, there would still be deterioration between the wafer-level separation and encapsulation steps. Dr. Doolittle explains how deterioration during separation occurs in detail at ¶ 37 of his declaration.

C. Exemplary Claim Of The '664 Patent²

For illustrative purposes, shown below is claim 1 of the '664 Patent, and some corresponding support in Fig. 12.

1. A light emitting diode (LED) package, comprising:

² The Petition refers to the reexamination history at pages 6–7 of the Petition, and makes the conclusory inference—without analysis—that the '448 Patent claims should match the claims of U.S. Pat. No. 9,070,851. Petitioner, however, has pointed to no evidence or legal support stating that family members must have the same claims. These are two different patents with different claims as illustrated by the comparison of the claims on the two patents at pages 6-7 of the Petition. Therefore, what occurred in U.S. Pat. No. 9,070,851 is not relevant to Petitioner's failure to demonstrate the claimed “protective insulation layer” of the '664 Patent in this Petition.

a semiconductor stack comprising a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer;

5 a plurality of contact holes arranged in the second conductive type semiconductor layer and the active layer, the contact holes exposing the first conductive type semiconductor layer;

10 a first electrode pad arranged over a first side of the semiconductor stack, the first electrode pad being electrically connected to the first conductive type semiconductor layer via some of the plurality of contact holes;

15 a second electrode pad arranged over the first side of the semiconductor stack, the second electrode pad being electrically connected to the second conductive type semiconductor layer; and

a protective insulation layer covering a sidewall of the first conductive type semiconductor layer and the second conductive type semiconductor layer,

20 wherein the protective insulation layer includes insulation layers having different indices of refraction from each other.

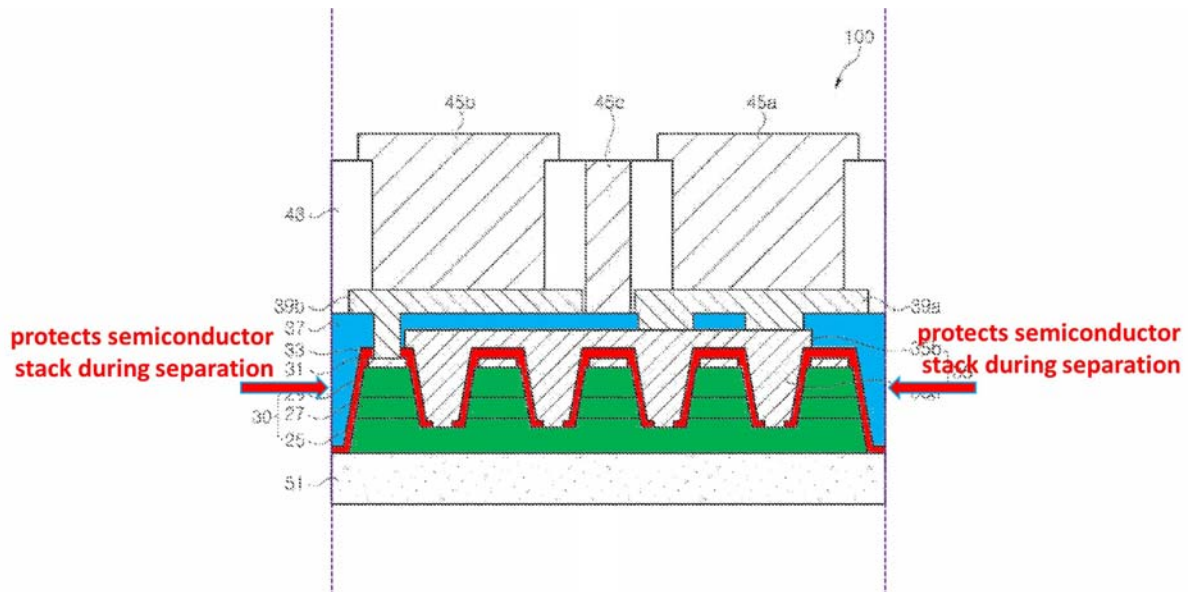


FIG. 12 of the '664 Patent (Annotated)

III. Claim Construction

5 The Board construes claims in accordance with their ordinary and customary meaning as understood by one of ordinary skill in the art. *See* 37 C.F.R. § 42.100; *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Patent Owner presents one term for construction because the Petition uses it in the Petition inconsistent with the *Phillips* standard.

10 A. “protective insulation layer” (all challenged claims)

 The Petition applies the “protective insulation layer” in a manner where it refers to electrical insulation only. *See, e.g.*, Petition at 17. Petitioner’s application takes away all meaning from “protective” in light of express use of insulation as a

separate word for the claimed layer. A POSITA, however, would have understood the ordinary and customary meaning of “protective insulation layer” to be “a layer that is structured to be both protective by substantially preventing the deterioration of the semiconductor stack and insulating by substantially preventing the flow of an electrical current.” *See, e.g.*, EX2001 at ¶ 39.

This construction is supported in the language of the claims. The challenged phrase recites both “protective” and “insulation,” and a POSITA would have given meaning to both terms. *See, e.g.*, EX2001 at ¶ 43. Protective and insulation describe two separate properties that the layer must have—the layer must protect, and the layer must insulate.

The specification of the ’664 Patent makes-clear that “insulation” refers to electrical isolation—to substantially prevent the flow of an electrical current. One of the main functions of the insulator is to electrically insulate two conductive layers, so that the flow of an electrical current can be controlled. EX2001 at ¶ 41.

As shown below, the protective insulator 33 (red) electrically isolates the first contact layer 35 (brown) from the second contact layer 31 (orange). *See, e.g.*, ’664 Patent at 9:8–15; 5:63-6:1. The electrical current runs through the semiconductor stack 30 (green) to power the active layer 27 and emit light. *See id.* at 5:27–45. Electrically insulating the first contact layer 35 (brown) from the second contact layer 31 (orange) is necessary in order to control current and have it directed

through the holes (red arrows). EX2001 at ¶ 43. If the protective insulation layer 33 did not electrically insulate and substantially prevent the flow of current, the LED would not work. *Id.*

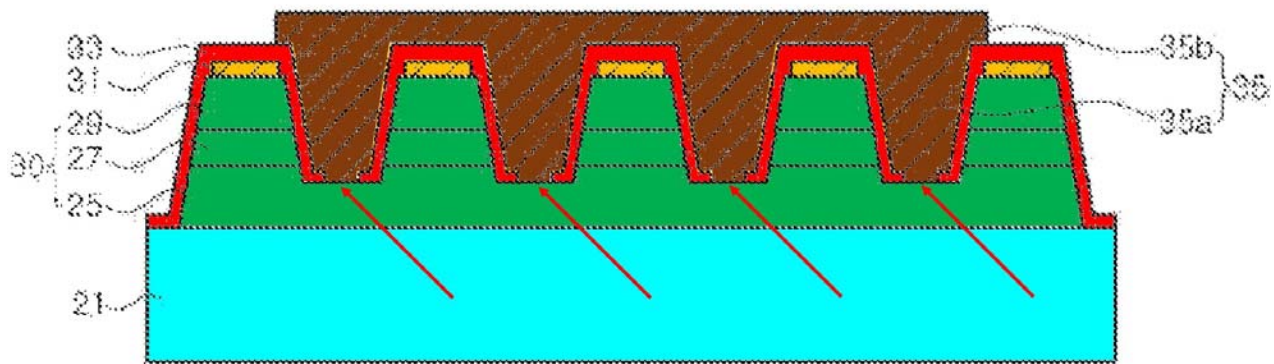


FIG. 8(b) of the '664 Patent (Annotated)

Furthermore, an “insulation layer” is commonly understood in the semiconductor art to refer to a layer that performs electrical isolation. *See, e.g.,* EX2001 at ¶ 41. This is demonstrated in all figures of the '664 Patent. *Id.* This is also demonstrated in Petitioner’s cited references, where the insulator is used to electrically isolate two conductive layers. *See, e.g.,* EX1005 at Fig. 1B, element 10; EX1007 at ¶ 5; EX1008 at ¶ 10; EX1009 at ¶ 41; EX1011 at ¶ 6; EX1012 at 4:65; EX1013 at 7:49–64. A POSITA would understand that, in the context of semiconductor devices, that certain materials need to be electrically isolated from other materials. EX2001 at ¶ 41. A POSITA would have recognized that an

“insulation layer” to be one that performs electrical isolation—it substantially prevents the flow of an electrical current. *Id.*

5 The ’664 Patent demonstrates that the “protective insulation layer” must do more than electrically isolate—it must protect and substantially prevent the deterioration of the semiconductor stack. EX2001 at ¶ 42. The “protective insulation layer” is described in two sections of the specification (*see* ’664 Patent at 7:17–43 and 13:38–58) and, in both of those sections, the protective insulation layer “prevent[s] deterioration of the light emitting cells ... due to moisture.” *Id.* at 7:7:28–29 and 13:49–50. When the LED is separated at the wafer-level, the
10 protective insulation layer (annotated red and blue below) protects the semiconductor stack in each LED. *See id.* at 3:23–25, 7:17–42, and 13:38–58; *see also id.* at 10:43–44. A POSITA would understand that the “protective insulation layer” substantially prevents the deterioration of the semiconductor stack. EX2001 at ¶ 42.

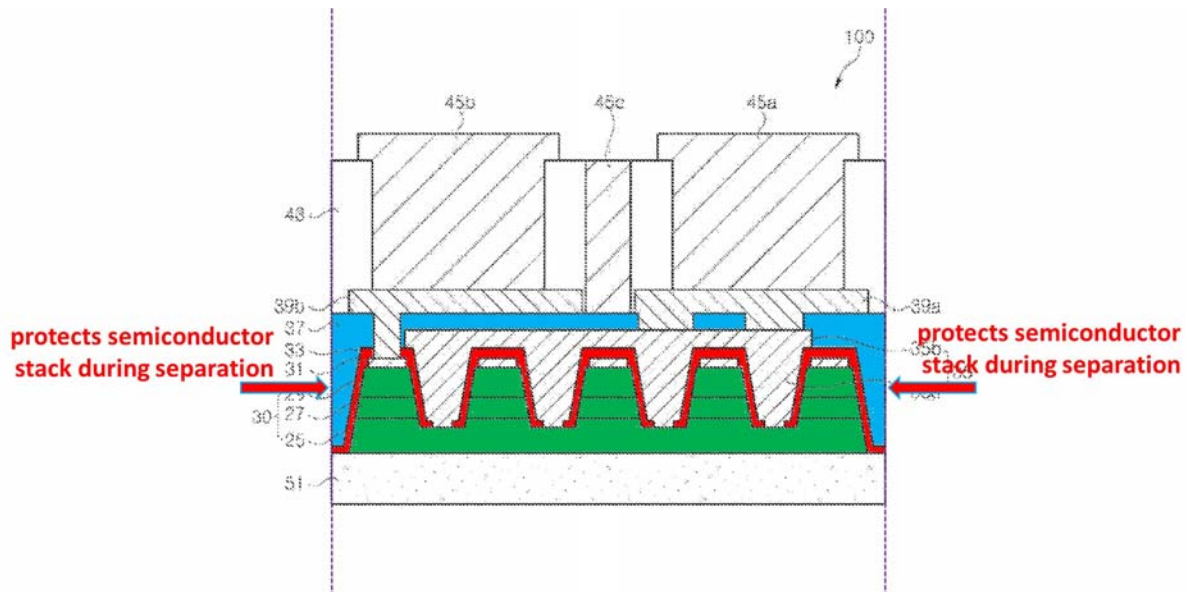


FIG. 12 of the '664 Patent (Annotated)

A POSITA would give meaning to the term “protective,” because an
5 insulator that electrically isolates does not also necessarily protect. Certain
materials will electrically isolate, but will not protect. Dr. Doolittle explains this in
depth at ¶¶ 43–45 of his declaration, providing many supported examples. For a
material like SiO₂, for example, preventing moisture migration depends on how
porous the material is. *See id.* (demonstrating numerous examples where SiO₂ is
10 porous and provides poor moisture protection). Insulators are commonly made in
the semiconductor art to be porous because porous materials provide benefits, such
as having less stress. *Id.* at ¶ 44. A porous SiO₂ layer will electrically isolate—and
will have the benefit of reducing stress and lessen the probability of cracking—but

will not prevent the migration of moisture. *Id.* Protective means more than electrical isolation. *Id.* at ¶ 43.

Accordingly, a POSITA would understand that the ordinary and customary meaning of “protective insulation layer” would be “a layer that is structured to be both protective by substantially preventing deterioration of the semiconductor stack and insulating by substantially preventing the flow of an electrical current.”

IV. Petitioner Fails To Demonstrate A Reasonable Likelihood Of Success For Any Claim

Petitioner’s 5 grounds are reproduced below.

- **Ground 1A:** 1-6, 8, 9, 11, 12 §102 over Illek
- **Ground 1B:** 1-6, 8-18 §103 over Illek
- **Ground 1C:** 7, 19 §103 over Illek and Begemann
- **Ground 2A:** 1-19 §103 over Donofrio and Sano
- **Ground 2B:** 19 §103 over Donofrio, Sano, and Begemann

Petitioner relied on Illek and Donofrio as primary references to teach the “protective insulation layer” for all claims of its 5 grounds: three grounds under Grounds 1A-B based on Illek and two grounds under Grounds 2A–B based on Donofrio, respectively.

Illek and Donofrio do not teach the “protective insulation layer.” Instead, they only teach an insulating layer—a layer that electrically isolates. In fact, Illek,

beyond not teaching a protective insulation layer, provides teachings that its insulating layers are not protective—its device requires an additional and separate encapsulation structure to provide protection. Both Illek and Donofrio’s semiconductor stacks would suffer from deterioration due to moisture during the wafer level fabrication steps because they lack the “protective insulation layer.”

Petitioner’s 5 grounds lack a basis in the teachings of the references and, in fact, are directly contradict the teachings of the references. The anticipation contention under Ground 1A fails to show that Illek discloses an identical invention as claimed. In the four obviousness grounds under Grounds 1B, 1C, 2A and 2B, Petitioner turned a blind eye to the disclosures and objectives of the very references it relied upon and failed to provide the required “articulated reasoning” with “rational underpinning” to support its arguments. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Instead, Petitioner relied on hindsight, using the claims of the ’664 Patent as a roadmap to force together prior art disclosures based on baseless and conclusory rationales. The law bars that approach. *Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341, 1352-53 (Fed. Cir. 2013).

Patent Owner requests that the Board to deny the institution.

A. Grounds 1A–C Should Be Denied

1. Ground 1A: Illek Does Not Anticipate Claims 1–6, 8, 9, 11, or 12

Petitioner relied on Illek to anticipate claims 1–6, 8, 9, 11, and 12 in Ground

5 1A. *See* Petition at 1. It is well established law for anticipation under 35 U.S.C. §
102 that that the prior art reference must describe the identical invention. *See*
Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed.Cir.1989) (“[t]he
identical invention must be shown in as complete detail as is contained in the ...
claim”). Contrary to Petitioner’s contention, Illek does not disclose an identical
10 invention as claimed in claims 1–6, 8, 9, 11, or 12.

Specifically, Petitioner relied on Illek’s “first insulation layer 10, second
insulation layer 13, and dielectric mirror layer 14 [to] together provide the claimed
protective insulation layer.” *See* Petition at 16 and 33. None of Illek’s first
insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 provide
15 protective functions. Illek’s semiconductor stack would suffer from deterioration
due to moisture—a situation that the ’664 Patent’s protective insulation layer
solves. *See* ’664 Patent at 7:17–29.

a. The First Insulation Layer 10, Second Insulation Layer 13, And Dielectric Mirror Layer 14 Do Not Protect

Illek's disclosure demonstrates that none of the first insulation layer 10,
5 second insulation layer 13, and dielectric mirror layer 14 (annotated below in
bright green, yellow, aqua, and yellow, respectively) provide protective functions.
In addition, Illek teaches that these layers need protection by a separate
encapsulation structure 40 formed during later packaging steps in order to protect
the semiconductor stack (green) from moisture. *See* EX2001 at ¶¶ 49–51. Illek
10 specifically teaches that “[s]ubsequent encapsulation of the components in order to
protect them” is done after the components have been cut from the wafer. *See*
EX1005 at ¶ 147. “The encapsulation 40 [(red)] ... protects the active region 4
from destruction [of] external influences such as moisture.” *See id.* at ¶ 148.

A POSITA would understand that Illek teaches that—prior to the
15 encapsulation being added—there would be no moisture protection for the
semiconductor stack.³ EX2001 at ¶¶ 50–51. Moisture protection for the
semiconductor stack is the stated reason for the encapsulation. EX2001 at ¶¶ 50–

³ Furthermore, Illek's mirror layer 14 “advantageously” uses Al (EX1005 at ¶
132), a material that Illek warns is susceptible to water damage and a reason why
the encapsulation should be added (*id.* at ¶ 151).

51; *see also* EX1005 at ¶ 151. Consequently, a POSITA would understand that the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 lack protective functions against moisture, and are not the claimed “protective insulation layer.”⁴

⁴ Even with the addition of the encapsulation (red), the semiconductor stack (green) would suffer from deterioration due to moisture. *See, e.g.*, EX2001 at ¶¶ 49 and 51. Packaging and encapsulation are added after LEDs are removed from a wafer. Illek’s LED would only receive water protection after the LED was removed from the wafer. Illek’s semiconductor stack would suffer from moisture and deterioration after the LED is cut from the wafer and exposed to the environment. *See* EX2001 at ¶ 37.

FIG 1B

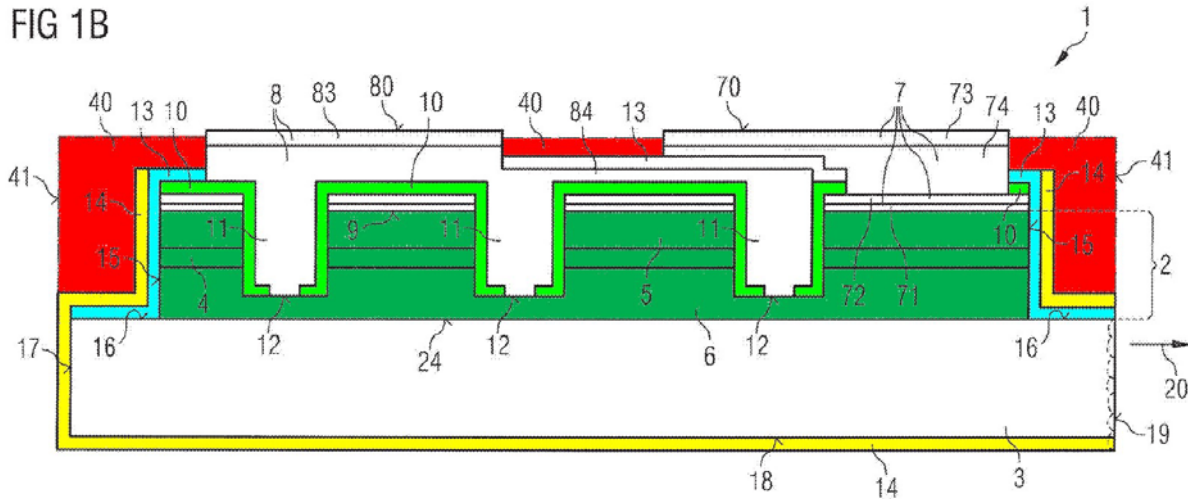


FIG. 1B of Illek (Annotated)

Furthermore, in light of Illek’s teaching of the protective encapsulation 40, a

POSITA looking at Illek would have understood that none of the first insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 teach protection.

EX2001 at ¶ 51. Illek teaches creating a moisture-protective encapsulation 40 (EX1005 at ¶¶ 147–148), and a POSITA would have found multiple layers of protection redundant if a moisture-protective encapsulation 40 were used. EX2001

at ¶ 51. Illek does not teach multiple layers of protection in addition to the encapsulation 40. *Id.* The first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 lack protection to environmental conditions such as moisture. *Id.* These layers would be subject to deterioration. *Id.*

A POSITA would not have read the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 to protect—in addition to the

encapsulation 40—because this would add redundant layers, provide minimal benefit,⁵ and would have many negatives. EX2001 at ¶ 51.

Making a layer protective presents many negatives. *Id.* (stating that designing for protection is a “trade-off”). Designing a layer to protect against moisture requires that the layer be less porous. *See id.* at ¶¶ 51 and 44–46. A less porous layer is more prone to stress, and this increases the probability that the layer cracks and breaks. *Id.* at ¶ 44. A POSITA would not have unnecessarily designed an LED to be more prone to cracks and breakage. EX2001 at ¶ 51.

Furthermore, beyond providing an encapsulant, Illek instructs that its layers 10/13/14 should lack protection—Ilek instructs a POSITA that it is “advantageous[]” to use Al in the mirror layer 14. *See* EX1005 at ¶ 132. Illek recognizes that Al is susceptible to water damage (*i.e.*, its semiconductor stack would be susceptible to deterioration). *Id.* at ¶ 151.⁶ A POSITA would not have unnecessarily introduced stress to a device that does not need protection because it uses encapsulant 40 for protection. *Id.*

⁵ The minimal benefit would be adding water protection between wafer cutting and encapsulation.

⁶ In addition, silver, another commonly used reflective metal for mirrors, is also sensitive to moisture. EX2001 at ¶ 52.

In light of Illek, a POSITA would have understood that the first insulation layer 10, second insulation layer 13, or the dielectric mirror layer 14 **do not** teach protection. *See also* EX2001 at ¶¶ 49–62. Accordingly, none of claims 1–6, 8, 9, 11, and 12 are anticipated.

5 **b. Petitioner Has Presented No Evidence Supporting Anticipation**

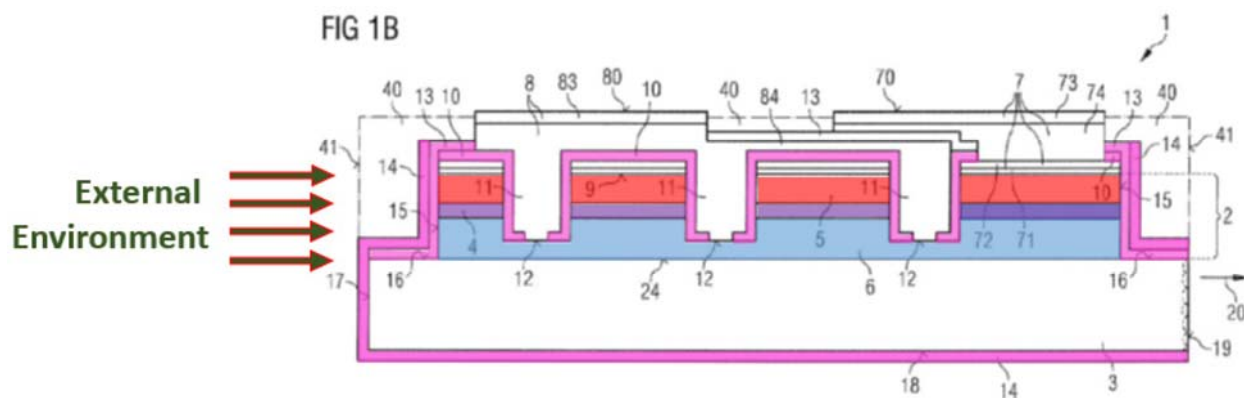
Beyond the above, Petitioner has presented no evidence that supports a finding of anticipation. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (“[i]n an [*inter partes* review], the petitioner has the burden from the onset to
10 show with particularity why the patent it challenges is unpatentable”) (citing 35 U.S.C. § 312(a)(3)); *see also* 37 C.F.R. § 42.104(b).

Petitioner’s argument that Illek teaches protection does not demonstrate that Petitioner’s alleged “protective insulation layer” (first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) provides protection. Petitioner
15 only establishes that the **encapsulation 40** is disclosed by Illek as a protective mechanism that protects the semiconductor stack from an external environment. *See* Petition at 19. But, the encapsulation 40 is not the first insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 based on Illek’s disclosure.

Without justification, Petitioner extends the protective qualities of the
20 encapsulation 40 to the first insulation layer 10, second insulation layer 13, and

dielectric mirror layer 14. *See id.* But, Petitioner's position is in contrary to Illek's explicit disclosure that encapsulation 40 is a separate structure from the layers 10/13/14, is formed in a subsequent process after singularization of the components, and that the encapsulation is made of special materials that are protective and are different from those for the layers 10/13/14. EX1005 at ¶¶ 147–151. The very explicit teaching in Illek for providing the protective encapsulation 40 as a designated protective structure separate from the layers 10/13/14 demonstrates that the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 as disclosed in Illek lack protection.

In light of the Petition and the declaration of its expert, Petitioner failed to provide any evidence that its identified “protective insulation layer” (*i.e.*, the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) provides any protection for the semiconductor stack in the disclosure of Illek.



Excerpt from Page 19 of the Petition

Petitioner's only Illek citations (EX1005 at ¶¶ 147–148) do not discuss the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 having protective qualities—they only describe the encapsulation 40, and how it provides moisture protection. *See* Petition at 19.

5 Further, Petitioner's expert's declaration demonstrates that Petitioner lacks any evidence to support that its alleged "protective insulation layer" (*i.e.*, the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) provides any protection. Petitioner's expert testified that "the three insulating layers 10, 13, and 14 of Illek together correspond to the protective insulation layer
10 as recited in the '664 Patent." EX1002 at ¶ 69. Petitioner's expert, however, acknowledged that the encapsulation 40 is a separate structure from the three insulating layers 10, 13, and 14. *Id.* at ¶ 75. Without any support, Petitioner's expert made a conclusory statement that "the configuration of Illek's layers 10/13/14 necessarily provide such protection by surrounding and facing
15 externally." *Id.* at ¶ 73. Petitioner's expert's analysis, however, requires the properties of the encapsulation 40 to demonstrate any protective qualities. *Id.* at ¶¶ 73–75. Petitioner's expert fails to explain why Illek's protective teachings of a separate structure—encapsulation 40—would lead to the conclusion that layers 10,

13, and 14 would also necessarily provide protection.⁷ Petitioner’s expert’s analysis demonstrates that the Petition lacks any evidence that its alleged “protective insulation layer” (*i.e.*, the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) provide protection.

5 Patent Owner’s expert, in contrast, cited technical literature and testified how it is improper to impart structural qualities of the encapsulant to layers 10/13/14 because they are entirely different structures. *See* EX2001 at ¶ 53 (stating in part that imparting qualities of one structure to an entirely different structure “is a mistake in analysis in my opinion”).

10 The Petition provides no evidence that could support a finding that the alleged “protective insulation layer” (*i.e.*, the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) performs any protection. Therefore, Petitioner has failed to present any evidence that supports a finding of anticipation of claims 1–6, 8, 9, 11, and 12.

⁷ Nonetheless, the Board should not give Petitioner’s expert’s testimony any weight. It parrots attorney arguments and conclusory statements that the properties of the encapsulation 40 can be extended to the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14. *Compare* Petition at 18–19 with EX1002 at ¶¶ 72–74.

**c. None Of The Materials Cited For Layers 10/13/14
Provides Protection**

Beyond the above, the materials of the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 do not demonstrate that they provide any protection. Illek only describes the first insulation layer 10 and second insulation layer 13 as potentially being “a silicon nitride such as SiN, a silicon oxide such as SiO₂, or a silicon oxynitride such as SiON.” EX1005 at ¶¶ 112 and 120. And the dielectric mirror layer 14 can be a silicon dioxide, dielectric materials, or various metalizations with Au, Ag, or Al. *See id.* at ¶¶ 130–132. But this does not describe their protective qualities. As Dr. Doolittle explains in depth, while citing nearly 20 references in the appendix to his declaration, that these materials are known and used in the art in non-protective ways. *See* EX2001 at ¶¶ 54–59 and 43–45. Petitioner’s bare allegation that these materials provide protection is insufficient for anticipation. Illek does not teach the first insulation layer 10, the second insulation layer 13, and the dielectric mirror layer 14 as a “protective insulation layer.”

The protective qualities—or lack thereof—of the first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14 depend on several factors, including how porous they are. *See, e.g.,* EX2001 at ¶¶ 43–45. A material like SiO₂, would provide no protection if it were designed to be porous. *Id.* A porous

SiO₂ layer would, however, provide less stress. *Id.* Simply because Illek teaches some materials, does not necessarily mean that they are protective. *Id.* ¶¶ 54–58 and 43–45. This is especially the case when non-protective layers provide benefits over protective layers, such as reducing cracking or delamination. *Id.* at ¶¶ 44–46.

5 Illek does not describe that any of the materials used for the first insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 are designed for protection. Petitioner has failed to show that Illek teaches the “protective insulation layer.”

Tellingly, Illek specifically describes moisture protection—and the materials
10 used—when a component is supposed to have protection. *See* EX1005 at ¶¶ 149–151; *see also* EX2001 at ¶ 52. As an example of a suitable protective material, Illek teaches that the encapsulation 40 is made of a molding compound BCB (benzo-cyclo-butene). *Id.* at ¶ 149. Further, Illek warns that any materials having phosphide, arsenide, or Al are susceptible to moisture damage (*see id.* at ¶ 151),
15 and describes having Al in its mirror layer 14 as “advantageous.” *Id.* at ¶ 132. Illek teaches providing the encapsulation 40, in part, to protect the mirror layer 14 and other components. *See* EX2001 at ¶ 52. And, Illek teaches that moisture protection may be unnecessary if nitrides are used, because there would be little risk in damaging nitrides with moisture. EX1005 at ¶ 150.

If a device needs protection, Illek instructs a POSITA to use a moisture protective encapsulant and, if the risk of damage is low, Illek instructs a POSITA not to use any protection at all. EX2001 at ¶ 52. Notably, Illek does not provide any teaching that any protective materials would be used for layers 10, 13, or 14, and it would be inappropriate for the board to infer any for a finding of anticipation.⁸ Petitioner has offered no evidence that its alleged “protective insulation layer,” *i.e.*, layers 10, 13, and 14, provides any protection.

Petitioner’s expert has not provided any evidence that Illek’s the first insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 provide protection. Petitioner’s expert merely described the first insulation layer 10 and second insulation layer 13 as providing electrical isolation. EX1002 at ¶ 68 (excerpted below). Petitioner’s expert did not state that the mirror layer 14

⁸ See *Metabolite Labs., Inc. v. Lab.Corp. of Am. Holdings*, 370 F.3d 1354, 1367, 71 USPQ2d 1081, 1091 (Fed. Cir. 2004) (explaining that “[a] prior art reference that discloses a genus still does not inherently disclose all species within that broad category” but must be examined to see if a disclosure of the claimed species has been made); *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (inherency requires that an inherent characteristic “necessarily flows from the teachings”).

provides any protection, beyond stating that it can be made of a dielectric or silicon dioxide. *See id.* (excerpted below). As described above, these materials do not demonstrate protective qualities (*see also* EX2001 at ¶¶ 43–46), and the “protective insulation layer” requires more than electrical isolation.

5 “As for layers 10 and 13, Illek teaches that its first insulation layer 10 and second insulation layer 13 are made of insulating materials such as silicon nitride, silicon oxide, or silicon oxynitride and that they are selectively applied over the semiconductor stack to
10 provide electrical isolation.” EX1002 at ¶ 68 (emphasis added)

Petitioner’s expert’s only support for protection is that Illek teaches protection via its encapsulation 40. *See* EX1002 at ¶¶ 72–74. But, as noted above, Illek’s disclosure of encapsulation 40 as a designated protective structure
15 demonstrates that none of the first insulation layer 10, second insulation layer 13, or dielectric mirror layer 14 provide protection.

In light of the disclosure in Illek on the protection and lack of evidence by the Petitioner’s expert, the Board should give Petitioner’s expert declaration on this issue little weight if any, because the cited-to paragraphs (¶¶ 72–74) parrot attorney
20 arguments in the Petition without providing any evidence in Illek or any other source. *Compare* Petition at 18–19 with EX1002 at ¶¶ 72–74.

None of Petitioner's identified layers (*i.e.*, first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14) are made from materials that necessarily provide protection. None of these materials teach protection. *See Metabolite Labs.*, 370 F.3d at 1367; *Ex parte Levy*, 17 USPQ2d at 1464.

5 Nonetheless, Petitioner has not argued any protective qualities, and it is not the Board's responsibility to recreate an argument for Petitioner. *See Shopkick Inc., v. Novitaz, Inc.*, IPR2015-00279, at 29 (PTAB May 29, 2015) (Paper 7) (“[i]t is Petitioner's responsibility ‘to explain specific evidence that supports its arguments, not the Board's responsibility to search the record and piece together
10 what may support Petitioner's arguments’”) (*citing Dominion Dealer Solutions, LLC v. Autoalert, Inc.*, Case IPR2013-00225, at 4 (PTAB Oct. 10, 2013) (Paper 15)). For at least this reason, Petitioner has failed to demonstrate that claims 1–6, 8, 9, 11, and 12 are anticipated.

 Furthermore, Illek's alleged “protective insulation layer” (layers 10/13/14)
15 are completely different in their structure and material composition of encapsulation 40 and, thusly, do not protect. *See* Petition at 16 (stating that the “first insulation layer 10, second insulation layer 13, and dielectric mirror layer 14—that together provide the claimed protective insulation layer”). Based on the teachings in Illek on the locations and functions of the layers 10, 13 and 14, it is
20 not feasible to include the molding compound BCB of the encapsulation 40 in the

layers 10, 13 and 14 in order to provide protection. Since Illek's encapsulation 40 is added during the LED's packaging step, after the LED had been cut from its wafer (EX2001 at ¶ 53; *see also* EX1005 at ¶ 14), a POSITA would not view the encapsulation 40 as a layer and much less the encapsulation 40 being part of the

5 "protective insulation layer." EX2001 at ¶ 53.

d. Illek Does Not Anticipate Claims 1–6, 8, 9, 11, or 12

As demonstrated by any one of the reasons in the preceding sections, Petitioner has failed to establish that Illek teaches the "protective insulation layer." Petitioner has not demonstrated that Illek anticipates claims 1–6, 8, 9, 11, or 12.⁹

10 *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) ("A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference"); *see also In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950–51 (Fed. Cir. 1999) ("[i]nherency, however, may not be

15 established by probabilities or possibilities").

In fact, Petitioner's relied upon sections of Illek (EX1005 at ¶¶ 147–148) demonstrate that none of the first insulation layer 10, second insulation layer 13, or

⁹ Petitioner relied on the same arguments for independent claim 6 and 8. *See* Petition at 29 and 31.

dielectric mirror layer 14 provide moisture protection. Therefore, the reliance on the layers 10/13/14 in Illek by Petitioner and its expert as its contended “proactive insulating layer” renders that the Petition fails to show that Illek discloses an identical invention as claimed in claims 1–6, 8, 9, 11, or 12 and, on this record, there can be no anticipation as alleged in the Petition. See *Richardson v. Suzuki Motor Co.*, (“[t]he identical invention must be shown in as complete detail as is contained in the ... claim”).

Petitioner bore the burden in the Petition, and failed to establish that Illek anticipates claims 1–6, 8, 9, 11, or 12. See *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (“[i]n an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable”) (citing 35 U.S.C. § 312(a)(3)); see also 37 C.F.R. § 42.104(b).

Accordingly, Illek does not anticipate claims 1–6, 8, 9, 11, or 12.

2. Grounds 1B–C: Illek does not render claims 1–19 obvious

Petitioner’s obviousness analysis, at page 34 of the Petition, provides nothing but a conclusory statement without any supporting evidence:

Illek’s layers 10/13/14 are each described as being insulators, and a POSITA would understand that their application to the various faces—including sidewalls—of the semiconductor stack would serve to passivate and

protect the semiconductor stack to thereby, for instance,
prevent shorting of the junction.

The Petition does not address any “protection,” beyond “preventing shorting.” But that is only the electrical isolation aspect of the “protective insulation layer.” The “protective insulation layer” requires protection. Petitioner’s obviousness combination does not address any prevention of deterioration of the semiconductor stack.

Obviousness is a question of law based on underlying factual findings: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the art; and (4) objective considerations of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 86 S.Ct. 684, 15 L.Ed.2d 545 (1966). Both the Petition and Petitioner’s expert’s declaration have failed to conduct the Graham analysis in Grounds 1B–1C and have failed to ascertain the differences between the claims and the prior art Illek with respect to the claimed “protection insulation layer.”

As discussed above, each challenged claim recites “protective insulation layer” which is a layer that is structured to be both protective by substantially preventing the deterioration of the semiconductor stack and insulating by substantially preventing the flow of an electrical current. Illek, in contrast,

discloses two different structures for two different functions: the encapsulation

for protection against moisture and three insulating layers 10, 13, and 14 electrical insulation. As discussed above, there is no disclosure or suggestion in Illek (or Petitioner's expert opinion, *see* EX1002 at ¶ 74) for designing the three insulating layers 10, 13, and 14 for protection. In addition, as explained above, Illek teaches
5 that the encapsulation 40 is specially provided as a separate structure and with a material property (*e.g.*, molding compound BCB) to protect, yet different from the material of layers 10, 13 and 14. The Petition and Petitioner's expert failed to analyze the differences between Illek's disclosure and the claimed "protective insulation layer" in its obviousness Grounds 1B–1C, and simply made a
10 conclusory declaration of obviousness without any evidence or analysis as to how the subject matter of each challenged claim reciting the "protective insulation layer," as a whole, would have been obvious to a POSITA in light of the teachings on the different properties and functions of the encapsulation 40 and the layers 10, 13 and 14 in Illek.

15 Nonetheless, Petitioner's vague statement is insufficient to establish of obviousness. Petitioner appeared to argue that it would have been obvious that layers 10/13/14 would prevent shorting. *See* Petition at 34–35. "Protective insulation layer" requires more—it requires prevention against the deterioration of the semiconductor stack in addition to being insulating. And Petitioner's
20 combination fails to address the protective requirement in its entirety.

Petitioner's combination should not be recreated by the Board to address this deficiency. *See Shopkick Inc., v. Novitaz, Inc.*, IPR2015-00279, at 29 (PTAB May 29, 2015) (Paper 7) ("It is Petitioner's responsibility 'to explain specific evidence that supports its arguments, not the Board's responsibility to search the record and
5 piece together what may support Petitioner's arguments.'")

Because Petitioner's grounds 1B–C do not cure the deficiencies of ground 1 mentioned in the immediately preceding section, all of grounds 1A–C should be denied.

B. Grounds 2A–B Should Be Denied

1. Donofrio Does Not Teach The Protective Insulation Layer

Petitioner relied on the combination of Donofrio and Sano to render obvious claims 1–19 in Ground 2A. *See* Petition at 1. Contrary to Petitioner's contention, the combination of Donofrio and Sano not render claims 1–19 obvious.

Petitioner did not mention any protective qualities of the "protective
15 insulation layer" beyond stating that it "prevent[s] shorting of the junction." *See* Petition at 55. Petitioner's cited-to expert support (§ 160) says nothing about the protective qualities of the insulating layer, beyond repeating that it prevents shorts. *See* EX1002 at § 160; *see also* EX2001 at §§ 64–68. And Petitioner's expert's
20 the layer by the prior art, only a conclusory statement that it has less chemical

reactivity. *Id.* Chemical reactivity says nothing about a layer’s moisture protection, for instance, because the layer could be porous. EX2001 at ¶ 65. The “protective insulation layer” requires more than electrical isolation—it requires protection. Petitioner has failed to address this and has failed to establish a
5 reasonable likelihood of success that Donofrio teaches the “protective insulation layer.”

Furthermore, the claims require that the “protective insulation layer includes insulation layers having different indices of refraction from each other.” Petitioner relied on a specific embodiment of Donofrio to satisfy this limitation:

10 “Specifically, Donofrio’s insulating layer 140, which corresponds to the claimed protective insulation layer, can be made up of “multiple sublayers, such as oxide and nitride sublayers to provide, for example, a distributed Bragg reflector.” LGI1009, [0041].” *See* Petition at 85.

15 But “multiple sublayers” of “oxide and nitride” says nothing about the protective qualities of these layers. A POSITA would understand that there are many oxides and nitrides that do not protect against moisture. This was explained in detail in the preceding sections, and explained in great detail by Dr. Doolittle at ¶¶ 66, 43–45, and 54–58. A POSITA would not look at Donofrio’s disclosure of
20 oxide and nitride to mean that the insulation layer 140 is a protective insulation layer.

A POSITA would not view Donofrio as teaching any protection for its semiconductor stack. EX2001 at ¶ 67. As can be seen from the below, Donofrio's semiconductor stack (green) is completely exposed. *Id.* The semiconductor stack would be exposed to moisture, and would deteriorate. *Id.* The insulating layer 140 (yellow) provides no protection. *Id.* A POSITA would not look at Donofrio and believe that it does not teach any type of moisture protection. *Id.*

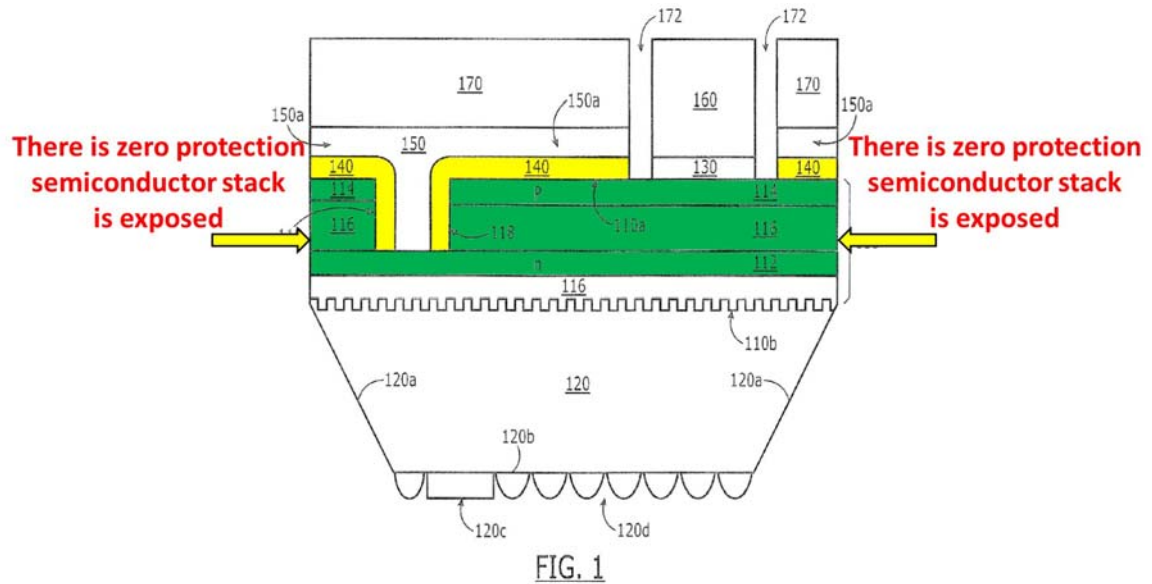


FIG. 1 of Donofrio (Annotated)

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For the sake of comparison, Fig. 12 of the '664 Patent is provided below. The protective insulation layer protects the semiconductor stack (green) by preventing deterioration due to moisture. *See* '664 Patent at 7:17–41. The

difference in how these two structures handle protecting the semiconductor stack is apparent.

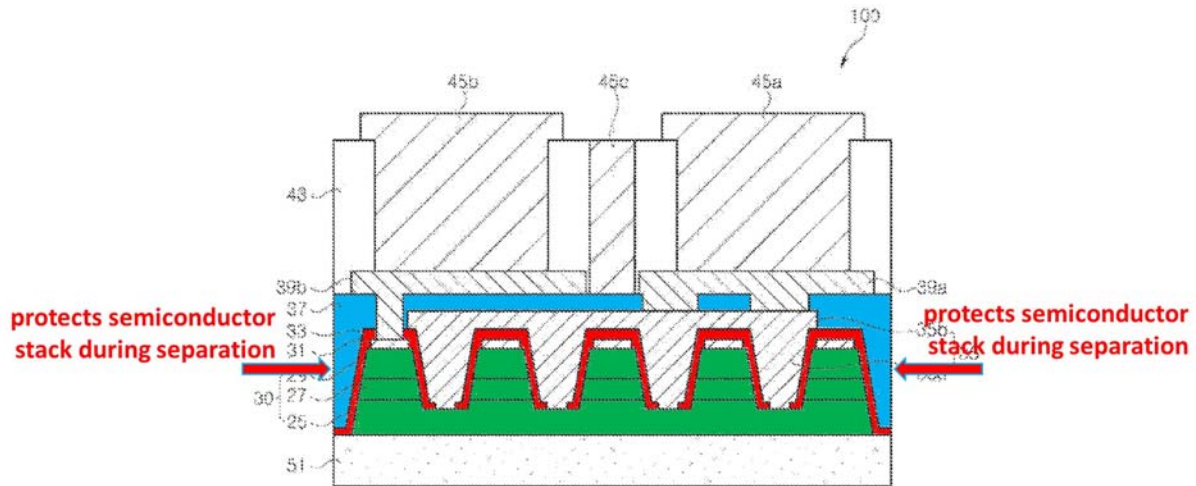


FIG. 12 of the '664 Patent (Annotated)

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Petitioner bore the burden but failed to demonstrate that Donofrio taught the “protective insulation layer” as required by claims 1–19. Petitioner did not rely on Sano to cure any of Donofrio’s deficiencies with respect to teaching the “protective insulation layer.” Ground 2A should accordingly be denied. Petitioner does not address or cure any of these deficiencies in Ground 2B. *See* Petition at 84–56.

10

Accordingly, Petitioner has failed to demonstrate that Donofrio and Sano render claims 1–19 obvious and Grounds 2A–B should be denied.

2. A POSITA Would Not Have Been Motivated To Combine Donofrio And Sano

Petitioner has failed to demonstrate that a POSITA would have been motivated to combine Donofrio and Sano. *See* EX2001 at ¶¶ 69–72.

5 As an initial matter, Petitioner’s rationale for combining Sano’s teachings is not supported by Sano or Donofrio. Petitioner argues that a POSITA would have added a slight over-etch to Donofrio and, because of that, a POSITA would have been motivated to combine Sano’s structure. *See* Petition at 59–60. Sano does not teach a slight over-etch but, instead, teaches a particular semiconductor structure.

10 EX2001 at ¶ 69. Petitioner equated the concept of a slight over-etch with the entirety of Sano. *Id.* Petitioner has pointed to no specific teaching of either Donofrio or Sano that would have motivated a POSITA to look at the other reference.

Petitioner argued that a POSITA would have been motivated to combine the

15 two because a POSITA would have been motivated to improve electrical contact. *See* Petition at 59–60. Donofrio, however, already addresses this issue, and provides improved electrical contact. EX2001 at ¶ 70. Specifically, Donofrio teaches that its n-type layer is completely exposed (EX1009 at ¶ 42) and, to improve ohmic contact, a contact layer is added (*id.* at ¶ 62). Petitioner argued that

20 Sano provides improved electrical contact, but does not explain how beyond a

slight over-etch. *See* Petition at 59–60. But the concept of a slight over-etch does not mean that a POSITA would have been motivated to combine Sano’s structure. EX2001 at ¶ 69.

Further, a POSITA would not have seen an etching like Sano’s to provide
5 any benefit to Donofrio’s teaching of a completely exposed n-type layer with an ohmic contact. EX2001 at ¶ 70. Donofrio’s layer is already exposed, and Donofrio’s ohmic contact is optimized. *Id.* Petitioner’s rationale that Sano provides a benefit is a conclusory statement without any actual support. A POSITA would not have been motivated to combine Donofrio and Sano.

10 Petitioner’s secondary rationale (*i.e.*, that it is a design choice) is equally as unsupported. Petitioner’s argument requires that the Board equate a slight over-etch with Sano’s entire teachings. Sano does not teach a slight over-etch but teaches a particular semiconductor structure. EX2001 at ¶ 69. Petitioner has not pointed to a specific teaching of Sano that is a simple design choice, but rather
15 states that over-etch is a design choice. *Id.* Petitioner’s rationale for the inclusion of Sano’s structure is unsupported. A POSITA would not have been motivated to combine Donofrio and Sano.

Nonetheless, Sano’s sidewalls are exposed as demonstrated below. A “protective insulation layer” that does not cover a sidewall, cannot plausibly be

protective. The combination of Donofrio and Sano fails to establish that the sidewalls are covered.

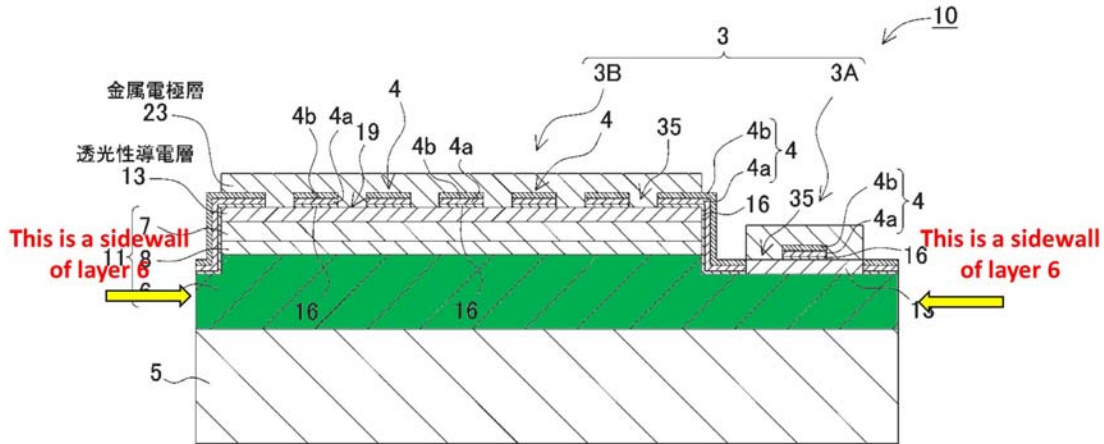


FIG. 3 of Sano (Annotated)

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Petitioner relied on the combination of Donofrio and Sano to render claims 1–19 obvious. *See* Petition at 1. The teachings in Donofrio and Sano do not support this combination. A POSITA would not have been motivated to combine the two. An obviousness analysis requires a demonstration that a POSITA “would have had some ‘apparent reason to combine the known elements in the fashion claimed.’” *See In re Whalen*, Appeal No. 2007-4423 at 16 (precedential) (citing *KSR Int’l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007)); *see also Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011) (“Obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim... Rather, obviousness requires the

15

additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention”) (citations omitted).

Petitioner is required to articulate a reason why a POSITA would combine and

5 modify prior art references, but has failed to do so. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *Metalcraft of Mayville, Inc. v. The Toro Company*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“[I]t is insufficient to simply conclude the [prior art] combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination.”); *see Belden Inc. v.*
10 *Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention”); *KSR*, 550 U.S. at 418 (“[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the
15 elements in the way the claimed new invention does”).

Petitioner bore the burden in the petition to establish that there exists a reasonable likelihood of success. *See* 37 CFR § 42.20(c) and 37 CFR § 42.108; see also 157 Cong. Rec. S1375 (daily ed. Mar. 8, 2011) (stmt. of Sen. Kyl) (demonstrating that Congress intended the “reasonable likelihood” test to

20 “requir[e] the petitioner to present a prima facie case” in the petition). Petitioner

has failed to establish that there is a motivation to combine Donofrio and Sano.

Accordingly, Grounds 2A and 2B should be denied.

3. Petitioner's Purported Combination Does Not Result In A Sidewall That Is Covered With The Protective Insulation Layer

Donofrio does not teach a sidewall—its semiconductor stack (green) is completely exposed. *See* EX1009 at Fig. 1. Acknowledging this deficiency, Petition relies on a strained reading of “sidewall” to extend to an attorney-created over-etch region in the n-type layer 112 located inside the trench to support an obviousness argument. *See* Petition at 55–61.

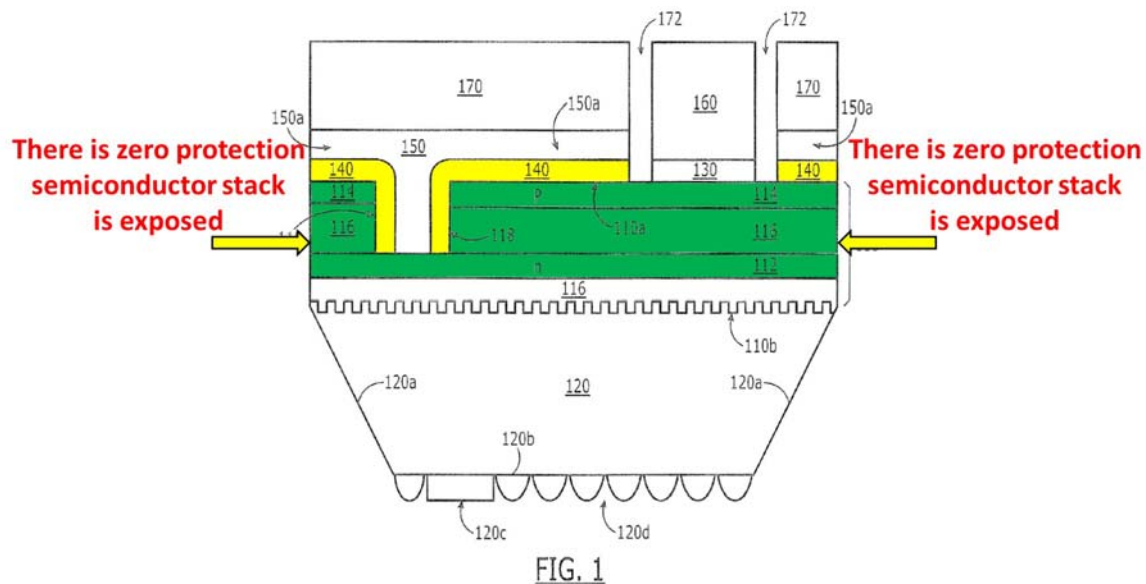


FIG. 1 of Donofrio (Annotated)

A partial over-etch into the n-type layer is not a sidewall. *See, e.g.*, EX2001 at ¶ 75. As illustrated below, Sano’s n-type layer has a sidewall at its sides. A POSITA would not have recognized a small divot, or a slight over-etch, to be a sidewall.¹⁰

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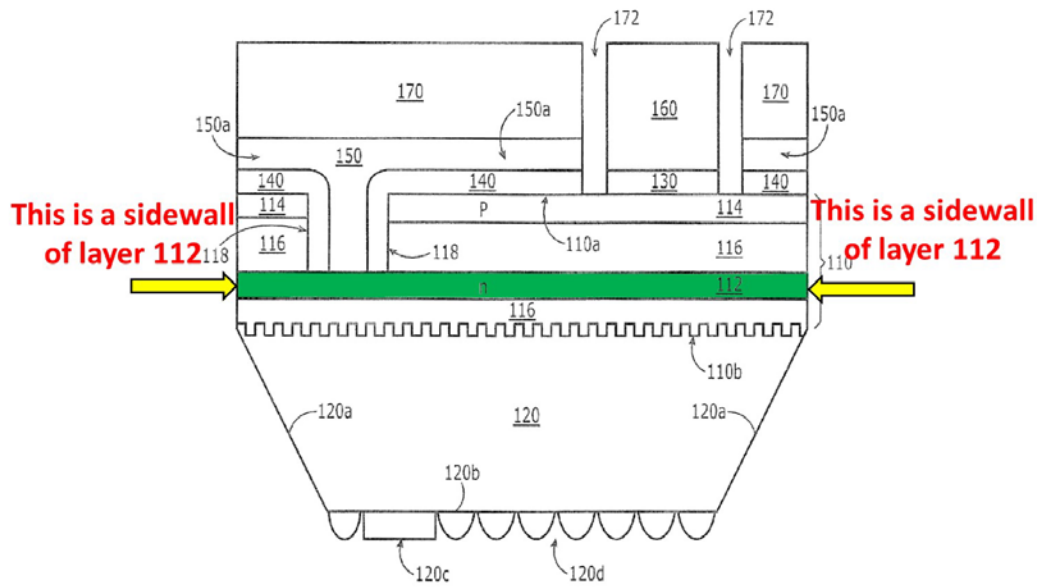


FIG. 1

FIG. 1 of Donofrio (Annotated)

¹⁰ The Board should also give little weight to Petitioner's Figure on page 57 of its Petition. Donofrio does not disclose this figure. This is a Petitioner-redraw of what Donofrio teaches to give the illusion that Donofrio teaches a significant etching into the n-layer.

Nonetheless, a “protective insulation layer” that does not cover a sidewall cannot plausibly be protective. *See, e.g.*, EX2001 at ¶¶ 73–74. As demonstrated above, Donofrio’s sidewalls are exposed, and the semiconductor stack would be subject to deterioration. Petitioner’s combination with Sano does not cure the
5 above-mentioned defect.

Petitioner has failed to establish that its identified “protective insulation layer” “cover[s] a sidewall” as required by claims 1–19. Ground 2A should be denied. Petitioner identifies similar over-etching in Ground 2B. Accordingly, Petitioner has failed to demonstrate that Donofrio and Sano render claims 1–19
10 obvious and Grounds 2A–B should be denied.

V. Petitioner’s Allegations Fail For Lack Of Evidence

The Board should afford no weight to the Declaration of Petitioner’s expert, Dr. Bretschneider, provided as EX1002. The vast majority of Dr. Bretschneider’s declaration is simply a reproduction or paraphrasing exercise of the Petition. *Cf.*
15 EX1002 at ¶¶ 55–225 (asserting grounds for invalidity), with Petition at 10–86 (repeating nearly verbatim the corresponding portions from the Declaration). The declaration substantially copies the Petition without elaboration and does not provide additional support for the Petition, in violation of 37 C.F.R. § 42.104(b)(4) & (5). *See, e.g., Wowza Media Sys., LLC v. Adobe Sys., Inc.*, IPR 2013-00054,
20 Paper 12 at 12 (PTAB Apr. 8, 2013). The declaration is no more helpful than the

Petition in determining where the challenged recitation is found in the references.

No weight should be given to Dr. Bretschneider's declaration.

VI. Conclusion

For the reasons discussed above, all challenged claims are patentable over
5 the proposed grounds based on the cited prior art in the Petition. Accordingly,
Patent Owner respectfully requests that the Board deny Petitioner's Petition for
inter partes review of the '664 Patent.

Dated: September 19, 2019

Respectfully submitted,

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CERTIFICATION OF WORD COUNT UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing *Patent Owner Preliminary Response* totals 8,415 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

This word count was made by using the built-in word count function tool in the Microsoft Word software Version 2010 used to prepare the document.

Dated: September 19, 2019

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CERTIFICATE OF SERVICE

I hereby certify that on this Nineteenth day of September, 2019, true and correct copies of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE and EXHIBIT 2001 were served via electronic mail upon the following counsel of record for Petitioner:

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