

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Universal Imaging Industries,
Petitioner,

v.

Lexmark International, Inc.,
Patent Owner.

Case IPR2019-01380
Patent 7,844,786

DECLARATION OF HARRY DIREEN, PH.D., P.E.

TABLE OF CONTENTS

I.	INTRODUCTION	3
A.	Qualifications.....	3
B.	Materials and Information Considered	5
II.	LEGAL STANDARDS	6
A.	Claim Construction Standard.....	6
B.	Standards for Determining Anticipation under 35 U.S.C §102.....	6
C.	Standards for Determining Obviousness under 35 U.S.C. §103	7
III.	THE '786 PATENT	8
IV.	LEVEL OF ORDINARY SKILL IN THE ART	12
V.	CLAIM CONSTRUCTION	13
VI.	ASSESSMENT OF THE '786 PATENT CLAIM(S) IN VIEW OF THE KNOWN PRIOR ART	13
	Overview of the Prior Art	15
A.	Applegate.....	15
B.	Hama 17	
C.	Memory Modules or Devices	19
	Grounds for Invalidity	20
VII.	CONCLUSION	21

I, Harry Direen, declare as follows:

I. INTRODUCTION

1. I have been retained by Petitioner Universal Imaging Industries (UII) as an independent expert consultant in several proceedings before the United States Patent Trial and Appeal Board (PTAB).

2. For this proceeding, I have been asked to review Adkins (U.S. Patent No. 7,844,786 - Ex. 1001) (“the ‘786 patent”), prior art to the ‘786 patent, and consider issues relating to the ‘786 patent.

3. I am being compensated at my ordinary and customary consulting rate for my work of \$280 per hour. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

A. Qualifications

4. I have over 35 years of experience as an engineer designing and developing products in the electronics and software industry, as outlined in my attached CV. I am currently working on adaptive technologies for people with spinal cord injuries. This work involves embedded computer control systems and image processing. I have worked with the US Air Force Academy in the areas of image processing, GPS designed navigation technology, and over-all control of unmanned aerial vehicles (UAVs). I work with cadets at the Academy in support of their senior year engineering projects.

5. I received my B.S. in Electrical Engineering from the University of California at Irvine and my Ph.D. in Electrical Engineering with a focus in Control Systems from the University of Colorado at Boulder.

6. I am a registered professional engineer in the state of Colorado and a senior member of the IEEE. My expertise includes control systems, digital signal processing, embedded systems design and development, XML database design, control of UAVs (Unmanned Aerial Vehicles), bio-informatics, and product reverse engineering.

7. I have a broad base of knowledge in electronic and software systems gained in my career working on various product designs for a number of companies. Throughout my career, I have designed and developed numerous embedded control systems using microprocessors and serial communication systems and protocols.

8. As one example, I developed complex adaptive control schemes using digital signal processing to control high power radio frequency (RF) generators used in semiconductor processing systems and CO2 lasers. These products used multiple microprocessors and asynchronous serial communications to communicate between the different modules.

9. While working for NeoCore I developed finite field algorithms for the company's patented ionization processing. This area is closely related to pseudo-random generators and made use of software and hardware shift-registers. I am a named inventor on two patents in this field: US Patent No: 6,934,730 Method and

System for Generating a Transform, and US Patent No: 6,493,813 Method for Forming a Hashing Code.

10. I have reverse-engineered a number of complex systems, including: media players, modems, modem compression algorithms, Coriolis mass flow meters, blood analysis meters and a variety of other products. I have successfully discovered and analyzed complex digital signal processing algorithms and pertinent operations within these products.

11. I have taught engineering at the US Air Force Academy, and taught undergraduate and graduate level classes at the University of Colorado, Colorado Springs (UCCS). I was a member of Advisory Board for the Center of Computational Biology, at the University of Colorado, Denver and was a Member of UCCS Advisory Board for developing undergraduate courses in the emerging area of computational biology. I am an inventor on three patents associated with XML database technology.

12. I understand that a copy of my CV, which further expands on my qualifications and expertise and includes articles I have published in the past ten years, will be filed with my declaration as Exhibit 1006.

B. Materials and Information Considered

13. In forming my opinions, in addition to my knowledge and experience, I have relied on those documents and information specifically recited in this report,

which I have cited with the exhibit number that I understand each has been given in this proceeding.

II. LEGAL STANDARDS

14. I am relying upon certain legal principles that counsel for UII has explained to me, which are set out below.

A. Claim Construction Standard

15. I understand that in this proceeding, the patent claims must be given a meaning “in accordance with the ordinary and customary meaning of such a claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). I understand that the best source for determining the meaning of a claim is the claims themselves, the written description (including any documents incorporated by reference into the description) and the prosecution history. I also understand that extrinsic evidence, which consists of all evidence external to the patent and prosecution history, may be considered to determine the meaning of a claim term.

B. Standards for Determining Anticipation under 35 U.S.C §102

16. I understand that a patent claim may be found unpatentable as anticipated by a prior art reference. For anticipation under Section 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.

C. Standards for Determining Obviousness under 35 U.S.C. §103

17. I understand that a patent claim may be found unpatentable as obvious if the Petitioner establishes by a preponderance of the evidence that, as of the priority date, the subject matter of the claim, considered as a whole, would have been obvious to a person having ordinary skill in the field of the technology (the “art”) to which the claimed subject matter belongs (or reasonably pertinent to the problems faced by a POSITA in the art).

18. I understand that the analysis of whether a claim is obvious depends on a number of necessary factual inquiries, for example, (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.

19. I have also been informed that the claimed invention must be considered as a whole in analyzing obviousness or non-obviousness. In determining the differences between the prior art and the claims, the question under the obviousness inquiry is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

20. Relatedly, I understand that it may be appropriate to consider whether there is evidence of a “teaching, suggestion, or motivation” to combine prior art references. I am informed that typically some kind of reason or motivation must be shown or have existed to explain why a person of ordinary skill in the art would have

thought of either combining two or more references or modifying one to achieve the patented invention. I also understand that a prior art reference may “teach away” from combining certain known elements. For example, a prior art reference teaches away from the patent’s particular combination if it leads in a different direction or discourages that combination, recommends steps that would not likely lead to the patent’s result, or otherwise indicates that a seemingly inoperative device would be produced.

21. I further understand that when a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, that may bar its patentability. Nonetheless, I also understand that a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Further, I am informed that I should be aware of the distortion that can be caused by hindsight and must be cautious of arguments reliant upon ex post reasoning. Although the suggestion to combine teachings may flow from the nature of a particular problem, defining the problem in terms of a solution can result from improper hindsight.

III. THE ‘786 PATENT

22. The ‘786 patent deals with updating a counter and a bit-field in a memory module or modules. The counter and bit-field are updated in response to a command from a processing device. The bit-field is referred to as a “punch out bit

field”. (Ex. 1001 at Abstract). While a preferred embodiment of the ‘786 is within an imaging or printing device, the ‘786 explicitly states that the teachings can be applied to any device having non-volatile memory (*Id.* at 2:35-40).

23. The non-volatile memory modules (103a, 103b, ... 103x) are separate from the processing device, 101 (*Id.* at Figure 1; 5:33-38). The processing device communicates with the memory modules over a data bus which includes an Address/Data line, 108, and a Clock line, 121. While the ‘786 specification does not mention a specific data bus standard, a POSITA will recognize the two-wire interface (Address/Data line and Clock line) as an I2C interface. The ‘786 specification states that other data bus interfaces such as a 1-wire interface may be used (*Id.* at 6:21-28). By not specifying and providing all the explicit details on the data bus interface, the ‘786 implicitly assumes that a POSITA has the knowledge, understanding, and background to choose, design and implement a functional data bus and data bus protocol between the processing unit and the memory modules that meet the rest of the patents operational requirements.

24. The ‘786 does not provide a POSITA with explicit memory devices and data sheets in order to design the non-volatile memory modules. Figure 1B shows a Secure Memory IC, 152, but the specification does not provide an explicit, off-the-shelf part with a part number and datasheet. By not providing this information, the ‘786 patent assumes a POSITA has the knowledge, understanding, and background

to choose or design a non-volatile memory that meets the rest of the system's requirements.

25. Figure 1B of the '786 does show the data bus connections going straight to the Secure Memory IC. This means the memory device has to be a smart memory device containing a serial data bus interface with internal command processing so that it can receive commands from an external processing device; process the commands; modify memory locations based upon command requirements; and send responses back to the processing device including values contained in the memory locations. The '786 specification does not provide a POSITA the details of how to design a Secure Memory IC, therefore it is expected that the Secure Memory IC is a readily available, off-the-shelf, part. Either that or the POSITA is expected to have the knowledge, understanding, and background to design a custom Secure Memory IC which meets all the requirements the '786 patent places on the device. An off-the-shelf Secure Memory IC will have a well-defined data bus and protocol with established command formats for interfacing with the device. A manufacture of the memory device must provide these explicit details so that an engineer is able to design the part into his/her system.

26. Each of the independent claims in the '786 (claims 1, 9, and 16) require the memory device to receive a command from the processing device which commands the memory to: a) change a bit in a bit field in the memory device; and b) increment a counter with in the memory device (claims 1 & 9). Assuming the

Secure Memory IC is an off-the-shelf device, these must be inherent capabilities of the off-the-shelf device. If the Secure Memory IC is not an off-the-shelf device, then the '786 assumes a POSITA has all the knowledge, understanding, and background to design a non-volatile memory device with:

- A data bus interface to an external processing unit.
- Command protocols for interfacing with a processing unit.
- Explicit command(s) for modifying a single bit in a bit field in the non-volatile memory.
- Explicit command(s) for incrementing a specific counter within the non-volatile memory.
- Possible Explicit command(s) for both modifying a single bit in a bit field in the non-volatile memory and for incrementing a specific counter within the non-volatile memory.
- Non-volatile memory.
- Some form of processing unit for carrying out the interface with the external processing unit and processing the commands.

27. Modifying a bit at a memory location and incrementing a counter at a memory location are fundamental operations that a POSITA will be intimately familiar with.

28. Claims 1 – 16 of the '786 are being challenged by UII.

IV. LEVEL OF ORDINARY SKILL IN THE ART

29. I understand that the claims of a patent are reviewed from the point of view of a hypothetical person of ordinary skill in the art (POSITA) at the time of the filing of the patent application. The “art” is the field of technology to which a patent is related.

30. I understand that a hypothetical POSITA is based on a variety of factors, including the disclosure of the subject patent, the prior art, the educational level of those working in the industry at the time, and the various approaches to address the systems and methods disclosed, which here involve microprocessors or microcontrollers, memory, serial communications, toner level sensors, and embedded software.

31. Based on my review of the patent and its file history it is my opinion that a person of ordinary skill in the art at the time of the invention would have had a bachelor’s degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems including both hardware and embedded software design. Experience and on-the-job training can substitute for formal education

32. During the time period immediately preceding the filing of the ‘786 patent, I believe that I met or exceeded the agreed definition of a POSITA. The embedded systems devices at issue here involve familiar product principles and

components that I have worked with and have been familiar with since well before the 2005 time period when the '786 patent application was filed.

V. CLAIM CONSTRUCTION

33. I understand that the parties may seek to construe certain terms during this proceeding. At present, I am not aware of any specific constructions that affect my opinions below.

VI. ASSESSMENT OF THE '786 PATENT CLAIM(S) IN VIEW OF THE KNOWN PRIOR ART

34. The independent claims 1, 9 and 16 are similar. Claim 1 states:

A method of updating memory modules, comprising:

receiving,

at one or more memory modules,

a command transmitted from a processing device,

wherein the command comprises

a) an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules and

b) a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules;

and processing the command at the one or more memory modules.

35. Independent claim 16 add the restriction that the memory module is contained in an imaging device and that the number of bits punched out are related to toner or ink levels. This claim drops the requirement for the increment counter.

36. The patent examiner provided the following reason for allowance of the '786 patent:

The primary reasons for allowance of claims 1 and 12 in the instant application is the combination with the inclusion in the claims of “a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules” (Ex. 1008, '786 file history page 12).

37. As I understand the examiner's reason for allowance, it is not the concept of updating a counter in a memory module nor the concept of updating a bit-field in a memory module, instead the allowance is for the combination of updating both a counter and “*a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules.*”

38. The '786 defines: a bit field may be “punched out,” thereby changing the bit field from an erased state to a programmed state (Ex. 1001 at 5: 6-7). In other words, the non-standard term of punching out a bit is simply changing the state of a bit from an erased state to a programmed state. A POSITA understands that non-volatile memories often have an erased state. Programming a bit, a byte, or memory location involves changing appropriate bits from the erased state to a programmed state (from a 1 to a 0 or a 0 to a 1). This is simply the characteristic of how many non-volatile memories operate and a POSITA will be familiar with this operation.

39. Combing two independent operations that give the same result as the independent operations falls into the definition of being obvious. The outcome is precisely the expected result and is therefore obvious. Changing a bit in a bit field changes an explicit bit from a 1 to a zero state or from a 0 to a 1 state. This is independent and not impacted by incrementing a counter by some value at another location in memory. Incrementing a counter at a memory location by some value is not impacted by changing a bit in a bit-field at some other memory location.

40. It is not clear from the '786 patent specification or the claims whether a single command with multiple parameters is used to cause both an changing a bit in a bit-field and causing a counter to be incremented by a given value, or two independent commands are used to effect this process. Sense the two operations are independent it really does not matter whether a single command or two commands are used, the same process is carried out either way. A POSITA fully understands this and there are no unexpected, non-obvious, results from carrying out the two operations.

41. The dependent claims are addressed in the accompanying claim chart and sections below.

Overview of the Prior Art

A. Applegate

42. The US patent 5,995,774 patent to Applegate (Applegate) titled "Method and Apparatus for Storing Data in a Non-Volatile Memory Circuit

Mounted on a Printer's Process Cartridge", published Nov. 30, 1999, addresses a non-volatile memory module contained on a printer's toner cartridge. Applegate states:

*A **toner "gas-gauge"** is created which uses "bucket levels" as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. **After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned**, thereby providing a permanent record on the process cartridge of a certain amount of toner usage* (Ex. 1004 at Abstract, emphasis added).

43. Applegate uses the term "burn" a bit rather than "punch out" a bit for the process of changing the state of a bit from an erased state to a programmed state. In the '786 patent's preferred embodiment the bit field is used to indicate the amount of toner that has been depleted (*Id.* at 5: 3-7):

... a non-volatile memory module provided with a toner cartridge may contain thirty-two bit fields, and as a particular amount of toner has been depleted (e.g., 1/32 of the total toner), a bit field may be "punched out," thereby changing the bit field from an erased state to a programmed state.

As can be seen by comparing the '786 with Applegate, the purpose and process of changing the state of a bit in a bit-field to represent the amount of toner used is the same.

44. Applegate references a specific non-volatile memory module, Dallas Semiconductor, Inc. integrated circuit, part number DS1982¹. The DS1982 uses a 1-Wire serial data communications link and protocol for communicating with a master device (Ex. 1007 at pg. 2). The datasheet states that individual bits can be changed from a logical 1 to a logical 0, and never from a logical 0 to a logical 1 (*Id.* at pg. 2). In other words, the memory bits can only be changed from the erased state, logical 1, to a programmed state, logical 0.

45. In addition to using a bit-field to represent the amount of toner consumed, Applegate teaches that other machine data may be stored in the non-volatile memory device (Ex. 1004 at 4:43-47, 5:7-14, & 13:37-40). Table 1 of Applegate indicates that a page count can be stored in the non-volatile memory. Additional counters such as: developer housing cycles, developer roll cycles, cleaner cycles are also disclosed in Table 1.

B. Hama

46. The US patent 7,269,362 to Hama (Hama), filed May 27, 2004, titled “Image Forming Apparatus, Control Method and Toner Consumption Calculating Apparatus and Method” addresses the calculation of toner consumption in a laser jet

¹ Dallas Semiconductor DS1982 1-kbit Add-Only iButton™ (<https://www.embeddeddatasystems.com/assets/images/supportFiles/manuals/DS1982-F3-DS1982-F5.pdf>)

printer (image forming apparatus) and the storage of the toner consumption information within non-volatile memory located on the toner cartridge.

47. Figure 2 of Hama shows that each toner cartridge has a memory device mounted on it: 91, 92, 93 & 94. The patent specification states that the memory devices are non-volatile memory that store information regarding the respective developers (toner cartridges). The CPU 101 updates and stores the information contained in the memories 91 – 94 (Ex. 1005 at 4:54 – 64). Hama explains that: *The memories 91 through 94 disposed to the developers 4Y, 4C, 4M and 4K and the memory 107 disposed to the engine controller 10 are preferably non-volatile memories which are capable of holding data even when the power source is off or the developers are detached from the main section (Id. at 6:15 – 20).*

48. Hama states: *The memory 91 and the like are disposed to the developer 4Y and the like of the developer unit 4. **Stored in this memory** are the initial value of the **cumulative count of the toner consumption** and the current remaining toner amount,... (Id. at 22:15 – 18, emphasis added).* Also: *The CPU 101 of the engine controller 10 calculates a toner consumption, subtracts this from the initial value and updates information regarding the current remaining toner amount. Thus **updated information regarding the remaining toner amount is stored in the RAM 107 and also in the memory of the toner cartridge 4Y or the like** (Id. at 22:15 – 18, emphasis added).*

49. Thus, Hama teaches: incrementing, in each of the one or more memory modules, at least one counter.

C. Memory Modules or Devices

50. The '786 applies to memory devices with multiple memory cells and multiple signal lines for communicating with a processing device. The memory device is assumed to have a "busy" condition that can be communicated back to the processing device. These memory devices are very common in the industry and were well known at the time of the '786 filing. An example is:

- US 5,822,251 titled "Expandable Flash-Memory Mass-Storage Using Shared Buddy Lines and Intermediate Flash-Bus Between Device Specific Buffers and Flash-Intelligent DMA Controllers", to Bruce (Bruce), published Oct. 13, 1998, discloses memory devices with multiple memory cells and multiple signal lines for communicating with a processing device. The flash memory includes a busy condition status line: *A busy signal is usually provided by each flash-memory chip to indicate when the read, write, or erase operation has completed. The busy signal allows a local processor to continue with other tasks while the flash-memory integrated circuit chip performs the flash operation* (Ex. 1003 at 1:66 – 2:3).

51. A POSITA will be fully aware of memory devices with multiple memory cells and multiple signal lines for communicating with a processor that contain status condition signals such as a busy signal. This is inherent knowledge.

Grounds for Invalidity

52. Ex. 1002-A is a claim chart comparing Applegate in combination with the various prior art references to the claims of the '786. The claim chart provides the details of the comparisons and my analysis.

53. Table 1 is a summary of my opinions. A 102 basis means that it is my opinion is that the noted art (Applegate) anticipates the noted claims of the '786 patent. A 103 basis means that it is my opinion is that the noted art (Applegate) in combination with the additional noted art (PK, and/or Hama and/or Bruce) renders the noted claims of the '786 patent obvious. PK stands for a POSITA's Knowledge.

Table 1

Ground	Claims	Basis	Prior Art
1	1 - 16	102	Applegate
2	2, 3, 14	103	Applegate & Hama
3	1 - 16	103	Applegate, PK, Hama, Bruce

It is my opinion that Applegate anticipates claims 1 – 16 of the '786. In addition, or at least, Applegate in combination Hama renders claims 2, 3, & 14 of the '786 obvious. In addition, or at least, Applegate in combination with a POSITA's knowledge, and/or Hama, and/or Bruce renders claims 1 – 16 of the '786 obvious.

VII. CONCLUSION

54. In view of the above, it is my opinion that all features of Claims 1 to 16 of the '786 patent are disclosed or obvious in view of the known prior art.

55. I declare that all statements made herein are true to the best of my knowledge. I understand that willfully false statements and the like are punishable by fine, imprisonment, or both under 18 U.S.C. § 1001.

Dated: July 23, 2019

Signed: /s/ Harry Direen
Harry Direen, Ph.D.

Addressing and command protocols for non-volatile memories utilized in recording usage counts

Abstract:	Electrical interfaces, addressing schemes, and command protocols allow for communications with memory modules in computing devices such as imaging and printing devices. Memory modules may be assigned an address through a set of discrete voltages. One, multiple, or all of the memory modules may be addressed with a single command, which may be an increment counter command, a write command, or a punch out bit field. The status of the memory modules may be determined by sampling a single signal that may be at a low, high, or intermediate voltage level.				
Inventors:	Booth, James Ronald; Willett, Bryan Scott			Assignee:	Lexmark International, Inc.
Appl. No.:	12/107278	Filed:	April 22, 2008		Granted: Nov. 30, 2010
Current US Class:	711/156; 711/103, 711/148, 711/150	Current International Class:	G06F12/00; G06F13/00; G06F13/28		
Field of Search:	711/156, 711/103, 711/148, 711/150				

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
<p>A method of updating memory modules, comprising:</p>	<p>Applegate discloses a method of updating memory modules.</p> <p>The US 5,995,774 patent to Applegate titled: “Method and Apparatus for Storing Data in a Non-Volatile Memory Circuit Mounted on a Printer’s Process Cartridge” discloses a non-volatile memory module contained on a printer’s toner cartridge. The abstract states (emphasis added):</p> <p><i>An improved electrophotographic (EP) printer is provided having a detachable process cartridge that contains a non-volatile memory device, which is an EPROM that cannot be erased after a bit is burned.</i></p> <p>...</p> <p><i>A toner “gas-gauge” is created which uses “bucket levels” as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage.</i></p>	<p>A preferred embodiment of Applegate makes use of a DS1982 non-volatile memory module. Applegate states that the DS1982 EPROM 144 also includes a one-wire function control and a memory function control at 188 (13:4-6). The Dallas Semiconductor DS1982 datasheet further clarifies that the DS1982 contains a Multidrop controller for MicroLAN which is a 1-Wire master/slave communications bus (Dallas Semiconductor DS1982 datasheet). Read and writing of the memory is accomplished over this 1-Wire master/slave communications bus.</p>

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
	<p><i>Certain important “machine data” also can be stored in the EPROM memory device on the process cartridge of the present invention.</i></p> <p>One of the embodiments noted in the ‘786 is a 1-Wire interface (6: 21-28).</p> <p>For a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference. Applegate states: <i>The details of the construction of the EPROM chip 144 can be obtained from its manufacturer, Dallas Semiconductor, Inc. located in Dallas Tex. (13:8-10).</i></p> <p>The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p> <p>Applegate points to earlier prior art and states: <i>U.S. Pat. No. 5,276,461 (owned by Tokyo Electric) which discloses a laser printer having a replaceable photosensitive cartridge and also having a nonvolatile memory mounted to a card base plate. The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media. (Applegate 2:15-21, emphasis added).</i></p>	

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
<p>receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises</p>	<p>Applegate discloses receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises</p> <p>Applegate states: <i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. And: Certain important “machine data” also can be stored in the EPROM memory device on the process cartridge of the present invention</i> (Appendix). In order to “burn” a bit or write a value in the EPROM memory a command must be sent from a master device to the memory slave device indicating that a bit in a bit field must be changed. The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p> <p>The memory module receives commands from a master processing device.</p>	
<p>a) an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules and</p>	<p>Applegate discloses an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules.</p> <p>A POSITA understands that a memory location simply</p>	<p>While a DS1982 memory module does not include an explicit increment counter command, it is clear to a POSITA from his or her training that incrementing a value at a memory location is a very basic, well understood, and trivial</p>

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
	<p>stores a value. To implement a counter, the memory value is read by a processor, an increment value is added to the memory value, and the new value is stored back into the memory location.</p> <p>Table 1 in Applegate provides a range of values that can be stored in the memory module. One of the items is a page count. Incrementing a counter at a memory location is a fundamental operation that a POSITA will be intimately familiar with.</p> <p>In addition, Applegate discloses earlier art that increments a counter in a memory module: <i>The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.</i> (Applegate 2:18-21, emphasis added).</p> <p>Applegate states: <i>Starting at a step 350 on FIG. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing</i> (20:18-22, emphasis added).</p> <p>Updating the gram count is incrementing the counter.</p>	<p>concept. A command for incrementing a counter is a basic and well understood concept and process that is obvious to a POSITA. Such a command and process has a predictable, well understood result.</p>
b) a punch out bit field command	Applegate discloses a punch out bit field command	Combing two independent operations that

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
<p>operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules;</p>	<p>operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules.</p> <p>Applegate teaches:</p> <p><i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage</i> (Abstract).</p> <p>And</p> <p><i>In the present invention, after a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage</i> (6:10-14).</p> <p>Applegate uses the term “burn” a bit rather than “punch out” a bit for the process of changing the state of a bit from an erased state to a programmed state. In the ‘786 patent’s preferred embodiment the bit field is used to indicate the amount of toner that has been depleted (5: 3-7):</p> <p><i>... a non-volatile memory module provided with a toner cartridge may contain thirty-two</i></p>	<p>give the same result as the independent operations falls into the very definition of being obvious. The outcome is precisely the expected result and is therefore obvious. Changing a bit in a bit-field changes an explicit bit from a 1 to a zero state or from a 0 to a 1 state. This is independent and not impacted by incrementing a counter by some value at another location in memory. Incrementing a counter at a memory location by some value is not impacted by changing a bit in a bit-field at some other memory location.</p> <p>It is not clear from the ‘786 patent specification or the claim whether a single command with multiple parameters is used to cause both an changing a bit in a bit-field and causing a counter to be incremented by a given value, or two independent commands are used to effect this process. Sense the two operations are independent it really does not matter whether a single command or two commands are used, the same process is carried out either way. A POSITA fully understands this and there are no unexpected, non-obvious, results from carrying out the two operations.</p>

US Patent 7,844,786 Claim 1 Limitations	vs Applegate	Obviousness Notes
	<p><i>bit fields, and as a particular amount of toner has been depleted (e.g., 1/32 of the total toner), a bit field may be “punched out,” thereby changing the bit field from an erased state to a programmed state.</i></p> <p>As can be seen by comparing the ‘786 with Applegate, the purpose and process of changing the state of a bit in a bit-field to represent the amount of toner used is the same.</p>	<p>The DS1982 datasheet states (pg. 2: <i>Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1.</i></p> <p>The DS1982 datasheet provides explicit memory function commands for writing to and changing bits in memory.</p>
<p>And processing the command at the one or more memory modules.</p>	<p>Applegate discloses and processing the command at the one or more memory modules.</p> <p>The fact that Applegate disclosed modifying memory locations implies that the commands are processed and carried out.</p> <p>Therefore, Applegate anticipates claim 1.</p> <p>In addition, or at least, Applegate in combination with a POSITA’s knowledge renders this claim obvious.</p>	

US Patent 7,844,786 Claim 2 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 1, wherein processing the command comprises incrementing, in each of the one or more memory modules, at least one counter.</p>	<p>See claim 1. Applegate discloses wherein processing the command comprises incrementing, in each of the one or more memory modules, at least one counter.</p> <p>Table 1 in Applegate provides a range of values that may be stored in the memory module, including counters for: page count, developer housing cycles, developer roll cycles, cleaner cycles, and more.</p> <p>Applegate states: <i>Starting at a step 350 on FIG. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing</i> (20:18-22, emphasis added).</p> <p>Updating the gram count is incrementing the counter.</p> <p>Applegate discloses earlier art that increments a counter in a memory module: <i>The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.</i> (Applegate 2:18-21, emphasis added).</p>	<p>If the items in Applegate Table 1 are not deemed counters, it would be obvious to a POSITA to make them counters to keep track of printer parameters that are changing over time.</p> <p>The US patent 7,269,362 to Hama (Hama), filed May 27, 2004, titled “Image Forming Apparatus, Control Method and Toner Consumption Calculating Apparatus and Method” addresses the calculation of toner consumption in a laser jet printer (image forming apparatus) and the storage of the toner consumption information within non-volatile memory located on the toner cartridge.</p> <p>Figure 2 of Hama shows that each toner cartridge has a memory device mounted on it: 91, 92, 93 & 94. The patent specification states that the memory devices are non-volatile memory that store information regarding the respective developers (toner cartridges). The CPU 101 updates and stores the information contained in the memories 91 – 94 (4:54 – 64). Hama explains that:</p>

US Patent 7,844,786 Claim 2 Limitations	vs Applegate	Obviousness Notes
	<p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p> <p>Applegate in combination with Hama renders this claim obvious.</p>	<p><i>The memories 91 through 94 disposed to the developers 4Y, 4C, 4M and 4K and the memory 107 disposed to the engine controller 10 are preferably non-volatile memories which are capable of holding data even when the power source is off or the developers are detached from the main section (6:15 – 20).</i></p> <p>Hama states: <i>The memory 91 and the like are disposed to the developer 4Y and the like of the developer unit 4. Stored in this memory are the initial value of the cumulative count of the toner consumption and the current remaining toner amount, ... (22:15 – 18, emphasis added).</i></p> <p>Also: <i>The CPU 101 of the engine controller 10 calculates a toner consumption, subtracts this from the initial value and updates information regarding the current remaining toner amount. Thus updated information regarding the remaining toner amount is stored in the RAM 107 and also in the memory of the toner cartridge 4Y or the like (22:15 – 18, emphasis added).</i></p> <p>Thus, Hama teaches: incrementing, in</p>

US Patent 7,844,786 Claim 2 Limitations	vs Applegate	Obviousness Notes
		<p>each of the one or more memory modules, at least one counter.</p> <p>Hama's teachings are closely related to Applegate's teachings therefore, a POSITA will be motivated to combine them.</p>

US Patent 7,844,786 Claim 3 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 2, wherein incrementing further comprises incrementing, in each of the one or more memory modules, the at least one counter by an increment value specified in the command.</p>	<p>See claim 2.</p> <p>Applegate states: <i>Starting at a step 350 on FIG. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing (20:18-22, emphasis added).</i></p> <p>It is inherent in Applegate's teaching that the gram counter will be updated by a value specified in a command and not simply incremented by 1.</p> <p>Therefore, Applegate anticipates this claim.</p>	<p>A POSITA understands well based upon his or her training that a counter can be incremented by 1 or by any desired incremental amount. There are no surprises or unexpected results. Updating a non-volatile memory counter after a print job is complete with the total number of pages printed produces the expected result based upon the simple math.</p> <p>Hama states: <i>The CPU 101 of the engine controller 10 calculates a toner consumption, subtracts this from the initial value and updates information regarding the current remaining toner</i></p>

US Patent 7,844,786 Claim 3 Limitations	vs Applegate	Obviousness Notes
	<p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p> <p>Applegate in combination with Hama renders this claim obvious.</p>	<p><i>amount. Thus updated information regarding the remaining toner amount is stored in the RAM 107 and also in the memory of the toner cartridge 4Y or the like (22:15 – 18, emphasis added).</i></p> <p>Clearly the Hama toner amount counter is updated by a specific value.</p>

US Patent 7,844,786 Claim 4 Limitations	vs Applegate	Obviousness Notes
The method of claim 2, wherein the command further comprises memory module addresses corresponding to each of the one or more one or memory modules.	<p>See claim 2. Applegate discloses wherein the command further comprises memory module addresses corresponding to each of the one or more one or memory modules.</p> <p>Table 1 in Applegate shows a mapping of values stored in memory by the address or byte offset from the start of a memory page. It is well understood by a POSITA that to access an item in memory, the address of the memory item is required. Unless a custom memory module is designed with custom interface commands, an address will be a required parameter in a command that accesses a memory item.</p> <p>Therefore, Applegate anticipates this claim.</p>	The DS1982 datasheet states that memory function commands include 2 address bytes (pg. 6 of the DS1982 datasheet).

US Patent 7,844,786 Claim 4 Limitations	vs Applegate	Obviousness Notes
	In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.	

US Patent 7,844,786 Claim 5 Limitations	vs Applegate	Obviousness Notes
The method of claim 1, further comprising establishing a busy status signal during the processing of the command at the one or more memory modules.	<p>See claim 1.</p> <p>Applegate discloses a non-volatile memory device in communications with a processing device. Applegate also discloses by pointing to other prior-art: <i>U.S. Pat. No. 5,276,461 (owned by Tokyo Electric) which discloses a laser printer having a replaceable photosensitive cartridge and also having a nonvolatile memory mounted to a card base plate. The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.</i> (Applegate 2:15-21, emphasis added).</p> <p>Inherent with nonvolatile memory are interface signals which interface the memory to a central processing unit or microcontroller device. It is well known to have a busy status signal as one of the signals between the memory and the central processing unit. Therefore, this is inherent to the Applegate teaching.</p>	<p>US 5,822,251 titled “Expandable Flash-Memory Mass-Storage Using Shared Buddy Lines and Intermediate Flash-Bus Between Device Specific Buffers and Flash-Intelligent DMA Controllers”, to Bruce (Bruce), published Oct. 13, 1998, discloses memory devices with multiple memory cells and multiple signal lines for communicating with a processing device. The flash memory includes a busy condition status line. Bruce Fig. 1 shows flash memory devices with “BSY” signals. Bruce states:</p> <p><i>A busy signal is usually provided by each flash-memory chip to indicate when the read, write, or erase operation has completed. The busy signal allows a local processor to continue with other tasks while the flash-memory integrated circuit chip performs the flash operation (1:66 –</i></p>

US Patent 7,844,786 Claim 5 Limitations	vs Applegate	Obviousness Notes
	<p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with Bruce renders this claim obvious.</p>	2:3).

US Patent 7,844,786 Claim 6 Limitations	vs Applegate	Obviousness Notes
The method of claim 1, wherein receiving further comprises receiving, at the one or more memory modules, the command from the processing device transmitted to the one or more memory modules via an asynchronous data channel.	<p>See claim 1. Applegate discloses wherein receiving further comprises receiving, at the one or more memory modules, the command from the processing device transmitted to the one or more memory modules via an asynchronous data channel.</p> <p>The 1-Wire data bus interface used in the preferred embodiment of Applegate (DS1982 memory module) is an asynchronous data channel. Being a 1-Wire interface there is no separate clock signal to make the interface synchronous.</p> <p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	

US Patent 7,844,786 Claim 7 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 1, wherein the punch out bit field command comprises implementing a command to change a bit associated with at least one memory module from an erased state to a programmed state.</p>	<p>Applegate discloses wherein the punch out bit field command comprises implementing a command to change a bit associated with at least one memory module from an erased state to a programmed state.</p> <p>Applegate states: <i>In the present invention, after a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. In this invention, the EPROM memory device acts as a “ write once read often ” memory device,...(6:10-16).</i></p> <p>Applegate is explicitly stating that the bit is being changed from an erased state to a programmed state.</p> <p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with a POSITA’s knowledge renders this claim obvious.</p>	<p>A preferred embodiment of Applegate makes use of a DS1982 non-volatile memory device. The DS1982 datasheet clearly states: <i>Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1</i> (pg. 2). This is very common for EPROM type non-volatile memories. In the erased state, all bits in the memory are at a logical 1 state. Programming a bit involves changing the state of the bit to a logical 0 state. This is inherent to the design of this many non-volatile memories. This claim is simply stating the obvious and standard operation of non-volatile memories. A POSITA understands this fact.</p>

US Patent 7,844,786 Claim 8 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 1, wherein the bit field comprises at least eight bits.</p>	<p>See claim 1. Applegate discloses wherein the bit field comprises at least eight bits.</p> <p>Table 1 of Applegate show a preferred memory data</p>	

US Patent 7,844,786 Claim 8 Limitations	vs Applegate	Obviousness Notes
	<p>structure layout. The memory is laid out in bytes where 1 byte represents 8-bits. Most memory is broken up into bytes or larger data words.</p> <p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
A method of updating memory modules, comprising:	<p>Applegate discloses a method of updating memory modules.</p> <p>The US 5,995,774 patent to Applegate titled: "Method and Apparatus for Storing Data in a Non-Volatile Memory Circuit Mounted on a Printer's Process Cartridge" discloses a non-volatile memory module contained on a printer's toner cartridge. The abstract states (emphasis added):</p> <p><i>An improved electrophotographic (EP) printer is provided having a detachable process cartridge that contains a non-volatile memory device, which is an EPROM that cannot be erased after a bit is burned.</i></p> <p>...</p>	<p>A preferred embodiment of Applegate makes use of a DS1982 non-volatile memory module. Applegate states that the DS1982 EPROM 144 also includes a one-wire function control and a memory function control at 188 (13:4-6). The Dallas Semiconductor DS1982 datasheet further clarifies that the DS1982 contains a Multidrop controller for MicroLAN which is a 1-Wire master/slave communications bus (Dallas Semiconductor DS1982 datasheet). Read and writing of the memory is accomplished over this 1-Wire master/slave communications bus.</p>

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	<p><i>A toner “gas-gauge” is created which uses “bucket levels” as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage.</i></p> <p><i>Certain important “machine data” also can be stored in the EPROM memory device on the process cartridge of the present invention.</i></p> <p>For a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference. Applegate states: <i>The details of the construction of the EPROM chip 144 can be obtained from its manufacturer, Dallas Semiconductor, Inc. located in Dallas Tex. (13:8-10).</i></p> <p>The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p>	
receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command is	Applegate discloses receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises	

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	<p>Applegate states: <i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. And: Certain important "machine data" also can be stored in the EPROM memory device on the process cartridge of the present invention</i> (Appendix). In order to "burn" a bit or write a value in the EPROM memory a command must be sent from a master device to the memory slave device indicating that a bit in a bit field must be changed. The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p> <p>The memory module receives commands from a master processing device.</p>	
<p>a) a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules</p> <p>and</p>	<p>Applegate discloses a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules.</p> <p>Applegate teaches:</p> <p><i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage</i> (Abstract).</p>	

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	<p>And <i>In the present invention, after a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage (6:10-14).</i></p> <p>Applegate uses the term “burn” a bit rather than “punch out” a bit for the process of changing the state of a bit from an erased state to a programmed state. In the ‘786 patent’s preferred embodiment the bit field is used to indicate the amount of toner that has been depleted (5: 3-7):</p> <p><i>... a non-volatile memory module provided with a toner cartridge may contain thirty-two bit fields, and as a particular amount of toner has been depleted (e.g., 1/32 of the total toner), a bit field may be “punched out,” thereby changing the bit field from an erased state to a programmed state.</i></p> <p>As can be seen by comparing the ‘786 with Applegate, the purpose and process of changing the state of a bit in a bit-field to represent the amount of toner used is the same.</p>	

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	<p>The DS1982 datasheet states (pg. 2: <i>Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1.</i></p> <p>The DS1982 datasheet provides explicit memory function commands for writing to and changing bits in memory.</p>	
<p>b) an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules;</p>	<p>Applegate discloses an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules.</p> <p>A POSITA understands that a memory location simply stores a value. To implement a counter, the memory value is read by a processor, an increment value is added to the memory value, and the new value is stored back into the memory location.</p> <p>Table 1 in Applegate provides a range of values that can be stored in the memory module. One of the items is a page count. Incrementing a counter at a memory location is a fundamental operation that a POSITA will be intimately familiar with.</p> <p>In addition, Applegate discloses earlier art that increments a counter in a memory module: <i>The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new</i></p>	<p>While a DS1982 memory module does not include an explicit increment counter command, it is clear to a POSITA from his or her training that incrementing a value at a memory location is a very basic, well understood, and trivial concept. A command for incrementing a counter is a basic and well understood concept and process that is obvious to a POSITA. Such a command and process has a predictable, well understood result.</p> <p>Combing two independent operations that give the same result as the independent operations falls into the very definition of being obvious. The outcome is precisely the expected result and is therefore obvious. Changing a bit in a bit-field changes an explicit bit from a 1 to a zero state or from a 0 to a 1 state. This is independent and not impacted by incrementing a counter by some value at</p>

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	<p><i>printed sheet of print media.</i> (Applegate 2:18-21, emphasis added).</p> <p>Applegate also states: <i>Starting at a step 350 on FIG. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing</i> (20:18-22, emphasis added). Updating the gram count is incrementing the counter.</p>	<p>another location in memory. Incrementing a counter at a memory location by some value is not impacted by changing a bit in a bit-field at some other memory location.</p> <p>It is not clear from the '786 patent specification or the claim whether a single command with multiple parameters is used to cause both an changing a bit in a bit-field and causing a counter to be incremented by a given value, or two independent commands are used to effect this process. Sense the two operations are independent it really does not matter whether a single command or two commands are used, the same process is carried out either way. A POSITA fully understands this and there are no unexpected, non-obvious, results from carrying out the two operations.</p>
and processing the command at the one or more memory modules.	<p>Applegate discloses and processing the command at the one or more memory modules.</p> <p>The fact that Applegate disclosed modifying memory locations implies that the commands are processed and carried out.</p> <p>Therefore, Applegate anticipates claim 1.</p>	

US Patent 7,844,786 Claim 9 Limitations	vs Applegate	Obviousness Notes
	In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.	

US Patent 7,844,786 Claim 10 Limitations	vs Applegate	Obviousness Notes
The method of claim 9, wherein the punch out bit field command comprises implementing a command to change a bit associated with at least one memory module from an erased state to a programmed state.	<p>See claim 9. Applegate discloses wherein the punch out bit field command comprises implementing a command to change a bit associated with at least one memory module from an erased state to a programmed state.</p> <p>Applegate states: <i>In the present invention, after a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. In this invention, the EPROM memory device acts as a "write once read often" memory device,...(6:10-16).</i> Applegate is explicitly stating that the bit is being changed from an erased state to a programmed state.</p> <p>Therefore, Applegate anticipates claim 1.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	<p>A preferred embodiment of Applegate makes use of a DS1982 non-volatile memory device. The DS1982 datasheet clearly states: <i>Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1</i> (pg. 2). This is very common for EPROM type non-volatile memories. In the erased state, all bits in the memory are at a logical 1 state. Programming a bit involves changing the state of the bit to a logical 0 state. This is fundamental to the design of this many non-volatile memories. This claim is simply stating the obvious and standard operation of non-volatile memories. A POSITA understands this fact.</p>

US Patent 7,844,786 Claim 10 Limitations	vs Applegate	Obviousness Notes

US Patent 7,844,786 Claim 11 Limitations	vs Applegate	Obviousness Notes
The method of claim 9, wherein the bit field comprises at least eight bits.	<p>See claim 9. Applegate discloses wherein the bit field comprises at least eight bits.</p> <p>Table 1 of Applegate show a preferred memory data structure layout. The memory is laid out in bytes where 1 byte represents 8-bits. Most memory is broken up into bytes or larger data words.</p> <p>Therefore, Applegate anticipates claim 1.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	

US Patent 7,844,786 Claim 12 Limitations	vs Applegate	Obviousness Notes
The method of claim 9, wherein receiving further comprises receiving, at the one or more memory modules, the command from the processing device transmitted to the one or more memory modules via an asynchronous data channel.	<p>See claim 9. Applegate discloses wherein receiving further comprises receiving, at the one or more memory modules, the command from the processing device transmitted to the one or more memory modules via an asynchronous data channel.</p> <p>The 1-Wire data bus interface used in the preferred embodiment of Applegate (DS1982 memory module) is an asynchronous data channel. Being a 1-Wire</p>	

US Patent 7,844,786 Claim 12 Limitations	vs Applegate	Obviousness Notes
	<p>interface there is no separate clock signal to make the interface synchronous.</p> <p>Therefore, Applegate anticipates claim 1.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	

US Patent 7,844,786 Claim 13 Limitations	vs Applegate	Obviousness Notes
The method of claim 9, wherein processing the command comprises incrementing, in each of the one or more memory modules, said counter.	<p>See claim 9. Applegate discloses wherein processing the command comprises incrementing, in each of the one or more memory modules, said counter.</p> <p>Applegate states: <i>The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.</i> (Applegate 2:18-21, emphasis added).</p> <p>Therefore, Applegate anticipates claim 1.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	It is clear and obvious to a POSITA that commanding a counter to increment will cause the counter to actually increment.

US Patent 7,844,786 Claim 14 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 9, wherein incrementing further comprises incrementing, in each of the one or more memory modules, the counter by an increment value specified in the command.</p>	<p>See claim 9.</p> <p>Applegate states: <i>Starting at a step 350 on FIG. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing</i> (20:18-22, emphasis added).</p> <p>It is inherent in Applegate's teaching that the gram counter will be updated by a value specified in a command and not simply incremented by 1.</p> <p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p> <p>Applegate in combination with Hama renders this claim obvious.</p>	<p>A POSITA understands well based upon his or her training that a counter can be incremented by 1 or by any desired incremental amount. There are no surprises or unexpected results. Updating a non-volatile memory counter after a print job is complete with the total number of pages printed produces the expected result based upon the simple math.</p> <p>Also: <i>The CPU 101 of the engine controller 10 calculates a toner consumption, subtracts this from the initial value and updates information regarding the current remaining toner amount. Thus updated information regarding the remaining toner amount is stored in the RAM 107 and also in the memory of the toner cartridge 4Y or the like</i> (22:15 – 18, emphasis added).</p> <p>Clearly the Hama toner amount counter is updated by a specific value.</p>

US Patent 7,844,786 Claim 15 Limitations	vs Applegate	Obviousness Notes
<p>The method of claim 9, further comprising establishing a busy status signal during the processing of the command at the one or more memory modules.</p>	<p>See claim 9.</p> <p>Applegate discloses a non-volatile memory device in communications with a processing device. Applegate also discloses by pointing to other prior-art: <i>U.S. Pat. No. 5,276,461 (owned by Tokyo Electric) which discloses a laser printer having a replaceable photosensitive cartridge and also having a nonvolatile memory mounted to a card base plate. The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.</i> (Applegate 2:15-21, emphasis added).</p> <p>Inherent with nonvolatile memory are interface signals which interface the memory to a central processing unit or microcontroller device. It is well known to have a busy status signal as one of the signals between the memory and the central processing unit. Therefore, this is inherent to the Applegate teaching.</p> <p>Therefore, Applegate anticipates this claim.</p> <p>In addition, or at least, Applegate in combination with Bruce renders this claim obvious.</p>	<p>US 5,822,251 titled “Expandable Flash-Memory Mass-Storage Using Shared Buddy Lines and Intermediate Flash-Bus Between Device Specific Buffers and Flash-Intelligent DMA Controllers”, to Bruce (Bruce), published Oct. 13, 1998, discloses memory devices with multiple memory cells and multiple signal lines for communicating with a processing device. The flash memory includes a busy condition status line. Bruce Fig. 1 shows flash memory devices with “BSY” signals. Bruce states:</p> <p><i>A busy signal is usually provided by each flash-memory chip to indicate when the read, write, or erase operation has completed. The busy signal allows a local processor to continue with other tasks while the flash-memory integrated circuit chip performs the flash operation (1:66 – 2:3).</i></p>

US Patent 7,844,786 Claim 16 Limitations	vs Applegate	Obviousness Notes
<p>A method of updating memory modules in an imaging device, comprising:</p>	<p>Applegate discloses a method of updating memory modules.</p> <p>The US 5,995,774 patent to Applegate titled: “Method and Apparatus for Storing Data in a Non-Volatile Memory Circuit Mounted on a Printer’s Process Cartridge” discloses a non-volatile memory module contained on a printer’s toner cartridge. The abstract states (emphasis added):</p> <p><i>An improved electrophotographic (EP) printer is provided having a detachable process cartridge that contains a non-volatile memory device, which is an EPROM that cannot be erased after a bit is burned.</i></p> <p>...</p> <p><i>A toner “gas-gauge” is created which uses “bucket levels” as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage.</i></p> <p><i>Certain important “machine data” also can be stored in the EPROM memory device on the process cartridge of the present invention.</i></p>	<p>A preferred embodiment of Applegate makes use of a DS1982 non-volatile memory module. Applegate states that the DS1982 EPROM 144 also includes a one-wire function control and a memory function control at 188 (13:4-6). The Dallas Semiconductor DS1982 datasheet further clarifies that the DS1982 contains a Multidrop controller for MicroLAN which is a 1-Wire master/slave communications bus (Dallas Semiconductor DS1982 datasheet). Read and writing of the memory is accomplished over this 1-Wire master/slave communications bus.</p>

US Patent 7,844,786 Claim 16 Limitations	vs Applegate	Obviousness Notes
	<p>For a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference. Applegate states: <i>The details of the construction of the EPROM chip 144 can be obtained from its manufacturer, Dallas Semiconductor, Inc. located in Dallas Tex. (13:8-10).</i></p> <p>The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p> <p>Applegate points to earlier prior art and states: <i>U.S. Pat. No. 5,276,461 (owned by Tokyo Electric) which discloses a laser printer having a replaceable photosensitive cartridge and also having a nonvolatile memory mounted to a card base plate. The nonvolatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media. (Applegate 2:15-21, emphasis added).</i></p>	
receiving, at one or more memory modules, a command transmitted from a processing device,	<p>Applegate discloses receiving, at one or more memory modules, a command transmitted from a processing device.</p> <p>Applegate states: <i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is</i></p>	

US Patent 7,844,786 Claim 16 Limitations	vs Applegate	Obviousness Notes
	<p><i>irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. And: Certain important “machine data” also can be stored in the EPROM memory device on the process cartridge of the present invention</i> (Appendix). In order to “burn” a bit or write a value in the EPROM memory a command must be sent from a master device to the memory slave device indicating that a bit in a bit field must be changed. The DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.</p> <p>The memory module receives commands from a master processing device.</p>	
<p>wherein the command is indicative of usage of toner or ink in a consumable item in the imaging device</p>	<p>Applegate discloses wherein the command is indicative of usage of toner or ink in a consumable item in the imaging device.</p> <p><i>A toner “gas-gauge” is created which uses “bucket levels” as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage (Applegate Abstract, emphasis added).</i></p>	

US Patent 7,844,786 Claim 16 Limitations	vs Applegate	Obviousness Notes
<p>and is operable to instruct the one or more memory modules to punch out a specified bit within the one or more memory modules indicative of said usage of toner or ink;</p>	<p>Applegate discloses and is operable to instruct the one or more memory modules to punch out a specified bit within the one or more memory modules indicative of said usage of toner or ink.</p> <p>Applegate teaches: <i>After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage</i> (Abstract).</p> <p>And <i>In the present invention, after a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage</i> (6:10-14).</p> <p>Applegate uses the term “burn” a bit rather than “punch out” a bit for the process of changing the state of a bit from an erased state to a programmed state. In the ‘786 patent’s preferred embodiment the bit field is used to indicate the amount of toner that has been depleted (5: 3-7):</p> <p><i>... a non-volatile memory module provided with</i></p>	<p>The DS1982 datasheet states (pg. 2: <i>Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1.</i></p> <p>The DS1982 datasheet provides explicit memory function commands for writing to and changing bits in memory.</p>

US Patent 7,844,786 Claim 16 Limitations	vs Applegate	Obviousness Notes
	<p><i>a toner cartridge may contain thirty-two bit fields, and as a particular amount of toner has been depleted (e.g., 1/32 of the total toner), a bit field may be "punched out," thereby changing the bit field from an erased state to a programmed state.</i></p> <p>As can be seen by comparing the '786 with Applegate, the purpose and process of changing the state of a bit in a bit-field to represent the amount of toner used is the same.</p>	
<p>and processing the command at the one or more memory modules.</p>	<p>Applegate discloses and processing the command at the one or more memory modules.</p> <p>The fact that Applegate disclosed modifying memory locations implies that the commands are processed and carried out.</p> <p>Therefore, Applegate anticipates claim 16.</p> <p>In addition, or at least, Applegate in combination with a POSITA's knowledge renders this claim obvious.</p>	