

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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UNIVERSAL IMAGING INDUSTRIES, LLC,  
Petitioner.

v.

LEXMARK INTERNATIONAL, INC.,  
Patent Owner.

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Case No. IPR2019-01378 on Patent No. 9,245,591 B2,  
Case No. IPR2019-01380 on Patent No. 7,844,786 B2  
and  
Case No. IPR2019-01381 on Patent No. 8,966,193 B2

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**DECLARATION OF JEFFREY J. FOLKINS, PH.D.  
IN SUPPORT OF PATENT OWNER PRELIMINARY RESPONSE TO  
PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NOS. 7,844,786 B2, 9,245,591 B2 AND 8,966,193 B2**

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## I. INTRODUCTION

1. My name is Jeffrey J. Folkins. I am retired from Xerox Corporation, where I worked for 34 years.

2. I have been engaged by Lexmark International, Inc. (“Lexmark” or “Patent Owner”) as a consultant in connection with Petitions for *inter partes* review (IPR) filed by Universal Imaging Industries, LLC (“UII”) of the patents and claims listed below:

Case No.	Patent No.	Claims
IPR2019-01378	9,245,591 B2	1-16
IPR2019-01380	7,844,786 B2	1-16
IPR2019-01381	8,966,193 B2	1-37

3. I will therefore refer to the patents challenged in these petitions for IPR as the “Challenged Patents” and the claims challenged in these petitions for IPR as the “Challenged Claims.” I am providing opinions regarding the IPRs for

each of the '591 Patent, the '786 Patent, and the '193 Patent. If an issue is only pertinent to one of the IPRs, I have indicated as such while providing the relevant analysis.

4. I was asked to consider whether the Challenged Claims of the Challenged Patents would have been patentable to a person of ordinary skill in the art as of the date of the invention.

5. This declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, as well as testimony from depositions that not yet been taken.

## **II. SUMMARY OF OPINIONS**

6. I have analyzed, among other documents, the Petitions for IPR of the Challenged Patents and the supporting evidence cited by UII, including the cited Direen Declarations. I have also considered the additional evidence cited herein and relied on my own experience in the field. In my analysis and in rendering my opinions, I have considered the knowledge and understanding of a person of

ordinary skill in the art at the time of the earliest priority date of the Challenged Patents.

7. It is my opinion that the Challenged Claims of the Challenged Patents have not been shown to be anticipated or obvious over the prior art or combinations of prior art relied upon by UII. For example, the references, alone or in combination, do not disclose a memory receiving a command from a processing device comprising an increment counter command, a punch out bit command, or a combination of the two, nor do the references disclose a memory module limiting the voltage on a signal line to an intermediate voltage to indicate the occurrence of a busy or error condition. In my analysis, I have focused on the independent claims of the Challenged Patents except where I have specifically noted otherwise. However, it is my opinion that UII's invalidity positions against the dependent claims of the Challenged Patents suffer from the same shortcomings as those against the independent claims. Therefore, my conclusions that the UII Petitions fail to show that the independent claims are anticipated or obvious necessarily means that the corresponding dependent claims are also not anticipated or obvious.

8. The subsequent sections of this declaration will first provide my qualifications and experience and then describe the details of my analysis and observations.

### **III. QUALIFICATIONS AND EXPERIENCE**

#### **A. Education and Experience**

9. I obtained a B.S. in Physics from Harvey Mudd College in 1976 and a Ph.D. in Physics from the University of Pennsylvania in 1981. I am an elected fellow in the American Physical Society. I have received national awards from the Society for Imaging Science and Technology (“IS&T”).

10. I worked at Xerox Corporation from 1981 to 2015, as an engineer and scientist, as a Project Manager, as a Program Manager, and as a Research Fellow (2005-2015). During this time, I developed technologies and products utilizing both electrophotographic and inkjet printing methods. I am an inventor of approximately 153 U.S. patents issued between 1984 and 2019 on inventions covering various aspects of inkjet and electrophotographic printing.

11. I worked as both a Research Fellow and a Program Manager at Xerox Corporation for about 34 years developing technologies and products for both electrophotographic and inkjet products.

12. The technologies that I developed have been incorporated in tens of Xerox product families ranging from small desktop printers to industrial high-volume production printers incorporating both electrophotographic and inkjet printing methods. Some examples of printer products that I was involved with included CiPress 500/325 Production Inkjet Continuous Feed printers, ColorQube 8570/8870 printers, ColorQube 9200 Series, and iGen3 & Docutech HLC Color Production Printers. For a more fulsome summary, I refer to my curriculum vitae, a copy of which is attached to this declaration as Appendix A..

13. My involvement in these printer projects included design and development of the architecture, concept, and technology, as well as benchmarking, assessment and prototyping of the printer systems that included electrophotographic development and toner subsystems, process controls, system architecture and color systems.

14. I have served as the technology phase Program Manager for the Xerox CiPress Production Inkjet Printer and as the Technical Program Manager of the Xerox ColorQube solid ink Inkjet printer. As the technical lead and the program manager my responsibilities also included leading a team of engineers and scientists that integrated the components and systems for the single pass color process that ultimately led to a new generation of Xerox color products, including Xerox's flagship iGen Digital Presses.

15. Some examples of printer technologies I have worked on are as follows. I developed a toner delivery system that in conjunction with a development system extended developer life almost indefinitely. This toner delivery system was featured in most subsequent Xerox products.

16. I designed and then led a team to create the first practical "scavengeless" development housing that was required to enable single pass full color electrophotography ("Image on Image"). I also led a team for the first implementation of this single pass color printing. This developer housing and this color single pass technology and system were subsequently productized as the

Xerox iGen production printer which has been the flagship product of Xerox for the past 15 years.

17. I developed two types of productized electrophotographic process controls systems. One system measured real time developability electrical currents for use in controlling toner dispensing. For this device I also designed portions of the productized electronics. The other was an electrostatic voltmeter using toner development for use with setting photoconductor charging levels and developability bias voltages.

18. An example of the skills I utilized for these tasks includes the writing of the machine control and interface software as well as the electrical design for multiple prototype single pass color printers.

19. Furthermore, I have managed and led groups of engineers with diverse skills including software and controls, electrical design, mechanical engineering, physics and materials science.

20. I have been recognized for my work in printing technologies and have received various awards and honors, including, for example, Election to Fellow in the American Physical Society in 1999; 2007 Johann Gutenberg Prize from the

Society for Imaging Science and Technology; and 2013 R&D100 Product Award from R&D Magazine “High Speed Printer Without Water” (one of the principal developers).

21. I have been a member of various professional associations related to printing technologies, including: American Physical Society (elected Fellow in 1999, life member); and Society for Imaging Science and Technology (IS&T) (former member). I am the author of multiple invited papers related to Inkjet and electrophotography.

22. A copy of my curriculum vitae is attached to this declaration as Appendix A.

**B. Compensation**

23. I am compensated by Lexmark for my work in connection with my work for this declaration. The compensation is not contingent upon my performance, the outcome of the IPRs or any other proceeding, or any issues involved in or related to the IPRs.

**C. Documents and Other Materials Relied Upon**

24. My opinions expressed in this declaration are based on documents and materials identified in this declaration, including each of the Challenged Patents, the prosecution histories of each Challenged Patent, the Petitions for IPR of each Challenged Patent, the Declarations from Dr. Harry Direen attached to each Petition for IPR (and labeled Ex. 1002 in each case) and the accompanying claim charts (Ex. 1002-A), the other exhibits cited by Petitioner in each proceeding, and the other materials that I refer to and that I cite in this declaration. I have considered these materials in their entirety, even if only portions are discussed here.

**IV. STATEMENT OF LEGAL PRINCIPLES**

**A. Claim Construction**

25. I am a scientist and engineer by training and by trade. I am not an attorney. Lexmark's counsel has advised me that in an IPR, a claim in patent is construed in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art at the time of the invention. I have further been advised that the person of ordinary skill in the art is deemed to read

the claim term not only in the context of the particular claim, but in the context of the entire patent, including the specification and the prosecution history.

**B. Anticipation**

26. Lexmark counsel has advised me that in order for a patent claim to be valid, the claimed invention must be novel. Lexmark's counsel has further advised me that if each and every element of a claim is disclosed in a single prior art reference, then the claimed invention is anticipated, and the invention is not patentable according to 35 U.S.C. § 102. In order for the invention to be anticipated, all of the elements and limitations of the claim must be shown in a single prior art reference, arranged as in the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. In order for a reference to inherently disclose a limitation, that claim limitation must necessarily be present in the reference.

**C. Obviousness**

27. Lexmark's counsel has advised me that obviousness under 35 U.S.C. § 103 is a basis for invalidity of a claim in a patent. I understand that where the

prior art does not identically disclose all of the limitations of a given patent claim, that patent claim is invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art. Obviousness can be based on prior art in the form of a single prior art reference or a combination of references that either expressly or inherently disclose all limitations of the claimed invention.

28. It is my understanding that the question of obviousness is to be determined based on:

- The scope and content of the prior art;
- The difference or differences between the subject matter of the claim and the prior art (whereby in assessing the possibility of obviousness one should consider the manner in which a patentee and/or a Court has construed the scope of a claim);
- The level of ordinary skill in the art at the time of the alleged invention of the subject matter of the claim; and

- Any relevant objective factors (the “secondary indicia”) indicating nonobviousness, including evidence of any of the following:  
  
commercial success of the products or methods covered by the patent claims; a long-felt need for the alleged invention; failed attempts by others to make the alleged invention; copying of the alleged invention by others in the field; unexpected results achieved by the alleged invention; praise of the alleged invention by the alleged infringer or others in the field; the taking of licenses under the patent by others and the nature of those licenses; expressions of surprise by experts and those skilled in the art at the subject matter of the claim; and whether the patentee proceeded contrary to accepted wisdom of the prior art.

## **V. THE CHALLENGED PATENTS**

### **A. Level of Ordinary Skill in the Art**

29. I understand that in analyzing the validity of a patent, the analysis is done from the perspective of a person having ordinary skill in the art (“POSITA”).

30. I have been informed that the following factors may affect the determination of the ordinary level of skill as it relates to the claims and description of a patent: (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) the prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of active workers in the field.

31. In my opinion a POSITA with respect to the subject matter of the '786, '193 and '591 Patents would have a bachelor's degree in electrical and/or computer engineering with one or more years of work experience in printer design, including hardware and/or embedded software design for printer applications. This description is flexible and additional education could substitute for work experience, and vice versa.

32. I understand that UII has proposed that a POSITA would have "a bachelor's degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems, including both hardware and embedded software design." In my opinion, I do not believe that the difference between the level of skill in the art that I have proposed and the level of skill

proposed by UII is determinative with respect to the outcome of the case, because UII has not shown that the claims are obvious under either definition.

33. Although my qualifications and experience exceed those of the person having ordinary skill in the art as defined above, I am familiar with the above described person having ordinary skill in the art via my work at Xerox. I have conducted my analyses and rendered my opinions in this declaration from the perspective of the person having ordinary skill in the art as of the earliest priority dates of the Challenged Patents: June 16, 2005 for the '786 Patent, and April 19, 2006 for the '193 and '591 Patents.

**B. Inventive Features of the Challenged Patents**

34. I understand that UII has filed petitions for *inter partes* review (IPR) challenging each of the '786 Patent, the '193 Patent and the '591 Patent. I understand that the '591 Patent was granted from U.S. Application No. 14/198,088 which is a continuation in part of U.S. Application No. 14/053,566, which is a continuation of U.S. Application No. 13/174,759 that became the '193 Patent. Therefore, the specification of the '591 Patent includes the same technical

disclosure, including Figs. 1-8B, as the '193 Patent, but adds additional disclosure in FIGS. 9, 10 and 11 and the related textual description.

I also understand that the '193 Patent shares the same Figs. 1-7 and the accompanying written description as the '786 Patent, while adding Figs. 8A and 8B and the related textual description.

35. To summarize, Figs. 1-7 and the accompanying textual description are common to all three Challenged Patents, while Figs. 8A and 8B and the accompanying textual description are common to the '193 Patent and the '591 Patent.

36. For portions of the specification that are common to all three patents, I will cite to the '193 Patent in my analysis. I will separately discuss the portions of the specification of the '591 Patent and '786 Patent to the extent that they are relevant to my analysis.

37. The '193 Patent describes novel methods and circuitry for imaging devices, such as printers, to communicate with memory modules. *See generally* '193 Patent, Abstract. At the time of the inventions of the '193 Patent, computing devices such as printing and imaging devices were becoming more advanced,

including an increasing number of non-volatile memory modules included within each device. '193 Patent at 1:41-43. The increasing speed and page rates of printing and imaging devices combined with the greater number of non-volatile memory modules needing to be updated created significant difficulties updating each of the non-volatile memory modules at the same time. *Id.* at 1:43-55.

Available non-volatile memory modules could experience degradation during operation, thereby necessitating error handling techniques to mitigate interruption in their operation. *Id.* at 1:56-60. There was also a cost premium associated with each additional electrical connection, particularly in removable or consumable components such as printer cartridges. *Id.* at 1:60-2:5. However, conventional communications protocols were insufficient to address all of these issues, leaving an unmet need in the art for better addressing schemes, command protocols, and interfaces. *Id.* at 2:6-11.

**1. The Patents Describe Inventions Related to  
Generating Protocols for Self-Management of  
Information by Memory Modules**

38. The inventors of the Challenged Patents met this need in the art by developing novel and creative methods and circuits for communicating with

memory modules in imaging devices or systems such as printers. For example, the '193 Patent describes and claims specific protocols for sending messages to memory modules. In one particular embodiment, the '193 Patent teaches a specific protocol 420 to send a command to "punch out" (e.g. change from an erased state to a programmed state) a specified bit within a memory module. *Id.* at 15:1-16. Fig. 4B shows the command protocol, including the command itself 422, the address of the memory module 424, the length of a list of bit-field numbers 426, and the address of specific bit fields 428:

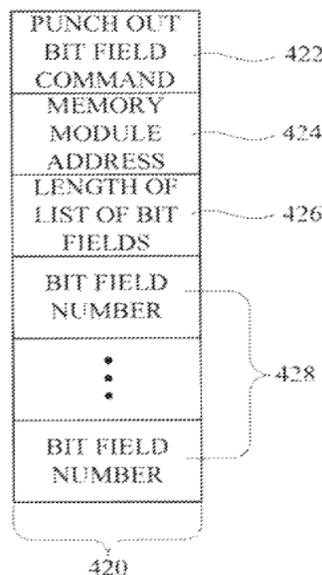
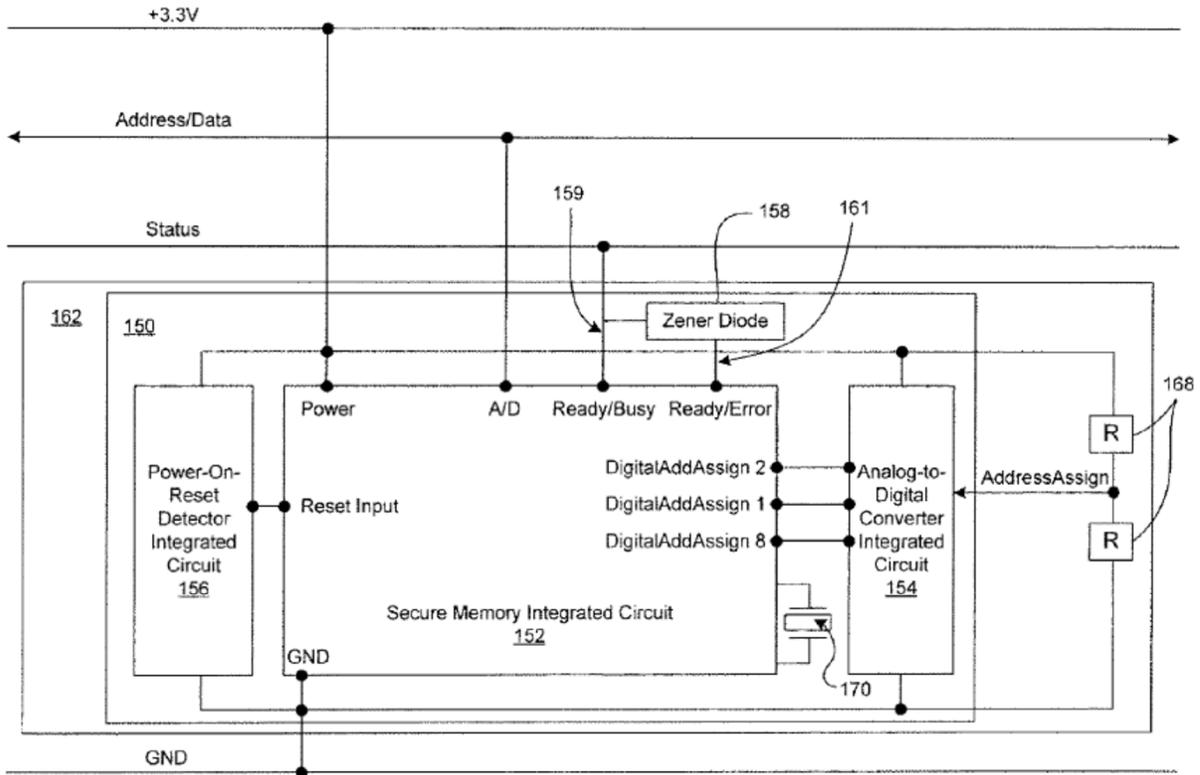


FIG. 4B

**FIG. 4B of the '193 Patent**

Embodiments claimed in the '786 Patent provide similar protocols for managing countable information (e.g., a number of pages printed) stored on memory modules in imaging devices or systems such as printers. *Id.* at 2:55-65, 4:66-5:4.

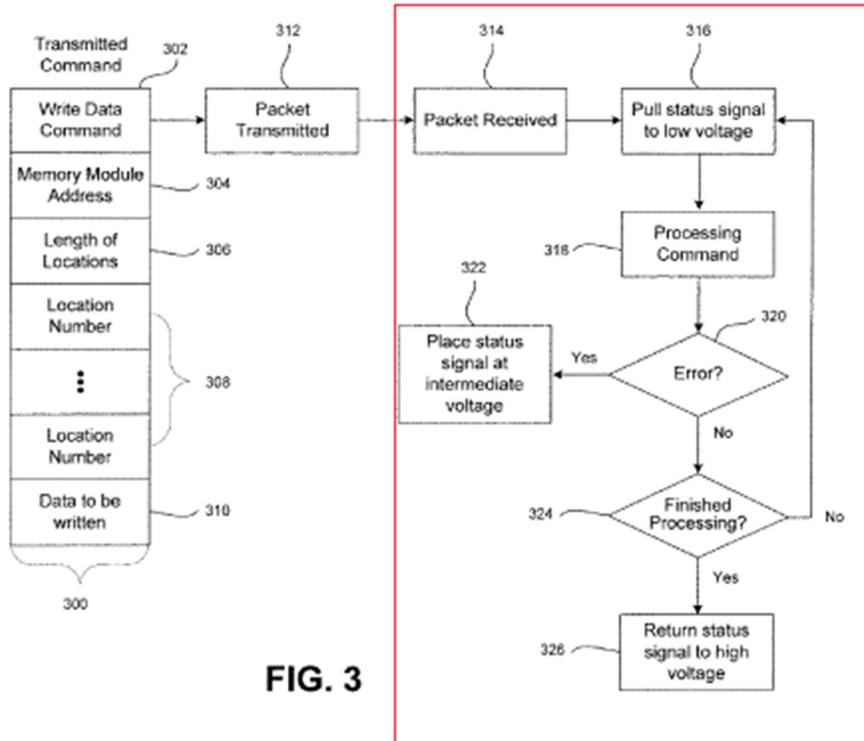
39. The protocols can be implemented on memory modules because the Challenged Patents employ intelligent memory, which differs from prior art memory that was capable of merely writing and storing specific values. For example, Figure 1B of the '193 Patent shows that the memory modules include a secure memory integrated circuit with processing capability for handling commands from the processing device:



**FIG. 1B**

**FIG. 1B of the '193 Patent**

40. Likewise, Figure 3 of the '193 Patent shows various processing steps performed by the memory module after it receives the packet at step 314:



**FIG. 3**

**FIG. 3 of '193 Patent (Annotated)**

41. As Petitioner UII’s expert Dr. Direen acknowledges, the ability to process information in this fashion makes the memory modules “smart memory.” See Ex. 1002 to IPR No. IPR2019-01380, Direen Declaration (’786 Patent) ¶25; Ex. 1002 to IPR No. IPR2019-01381, Direen Declaration (’193 Patent) ¶25. Specifically, a person of ordinary skill in the art would have understood the

memory module's "processing the command" as akin to executing program instructions.

42. I offer an example to show the difference between systems like those in the Challenged Claims employing and utilizing features of "smart" memory, and those systems that either do not employ, or may employ but do not use the abilities of, "smart" memory.

43. In the latter cases, which I will dub "normal" memory cases, a central processor reads information from the memory, processes that information in the context of additional information, and communicates back to the memory an instruction to write a specific value resulting from the processing. In one operation of such a normal memory, for example, the central processor may determine that an ongoing print operation used five of the image forming device's remaining pages for print. The central processor recognizes that a stored page remaining value must now be updated, sends a communication to the memory seeking a read of the page remaining value, and then receives a communication back indicating the last stored value was forty pages remaining. The central processor then determines that the number of remaining pages is now thirty-five. Finally, the

central processor then directs the memory to overwrite the “40 remaining pages” value with the specific value the processor calculates, i.e., “35 remaining pages.”

44. In contrast, the “smart” memory case disclosed in the Challenged Patents removes several steps by delegating part of the execution of program instructions to the memory modules. As in the normal memory case, a central processor similarly determines that an ongoing print operation uses five of the remaining number of pages. But different from the normal memory case, the central processor simply directs the memory modules to decrement the “remaining pages” value by five pages without specifying the final value for “35 remaining pages” and lets the memory modules process the instruction, to determine the proper final value and the write the proper final value into memory. Upon receipt of this instruction, the “smart” memory module processes the command by reading the currently-stored “remaining pages value” (e.g., 40 pages), modifying that value in accordance with the instruction provided by the central processor (e.g., subtracting five pages) to obtain the new value of “35 remaining pages,” and updating the “remaining pages value” to reflect its calculation of the new value (in this example, “35 remaining pages”).

45. The advantage of processing items within the memory modules, using the technology disclosed by the Challenged Patents, rather than in the central processor, is that this may result in a faster operation. Rather than query the module for a value, have the module send the value back to the central processor, do the calculation at the central processor, and then then send back the result, memory modules like those in the '193 Patent simply receive one communication and process it (i.e., modify current values relative to existing values. Additionally, there are certain operations that can only be done in the memory module. The most notable example, which is discussed in the '193 Patent's specification, is processing of security-related tasks such as determining module authenticity, encryption, etc. '193 Patent at 14:12-23. Hence processing commands within the memory module itself can provide various advantages over systems employing "normal" memory (or not actually utilizing features of the "smart" memory).

46. [not used]

**2. The Patents Further Describe Inventions Related to Transmission Protocols Between Central Processing and Memory Modules**

47. Another innovation described by the '193 Patent and other Challenged Patents allows one of several memory modules linked to a signal wire to signal the occurrence of a condition to the controlling computer system without interrupting transmission of information by the controlling computer system over the same wire. The Challenged Patents teach that this goal is accomplished by a device on the wire signaling the occurrence of a condition by limiting the voltage of the signal wire to an intermediate voltage which is greater than the low voltage representing a logical "0" and lower than the high voltage representing a logical "1." *See generally* Ex. 1001 at 9:24-57. For example, if at least one device on the combined Address Data/Error channel has an error, the device will prevent the voltage on the signal line from exceeding the intermediate value. Doing this enables the system to convey two pieces of information (whether the logical state of the line is a "1" or a "0," and whether or not at least one device has an error) by using both a single line and only three different voltages that are generated to be placed on the single line.

48. I have made a chart below, based on the description in Column 9 of the '193 Patent, to summarize how the '193 Patent teaches that these pieces of information can be conveyed simultaneously on a single line:

<b>Voltage Level Generated from Memory Module and Applied to Single Line</b>	<b>Address Data State</b>	<b>Error State</b>
High	Logical "1"	No error (i.e., no device signaling an error)
Intermediate	Logical "1"	At least one device has an error
Low	Logical "0"	Independent of whether any device has an error

49. The Clock/Busy line can likewise signal two pieces of information (the logical state of a clock signal and whether or not at least one device is busy) using the same logic based on the three voltage levels:

<b>Voltage Level Generated from Memory Module and Applied to Single Line</b>	<b>Clock State</b>	<b>Busy State</b>

High	Logical “1”	No device is busy
Intermediate	Logical “1”	At least one device is busy
Low	Logical “0”	Independent of whether any device is busy

50. In both cases, the device connected to the single line generates one of the three voltage levels and can “limit” the voltage to an intermediate value if the condition (busy or error) occurs because the voltage can only go “high” where no device has a busy or error condition.

51. In one embodiment in the Challenged Patents, the limiting of the voltage on a combined Address Data/Error channel to an intermediate voltage indicates an error at one or more memory modules (*id.* at 9:27-31), while the limiting of the voltage on a combined Clock/Busy channel to an intermediate voltage indicates that at least one memory module is busy (*id.* at 9:44-47.) In both cases the controlling computer system can continue to transmit information over the Address Data/Error and Clock/Busy channels while the voltage is limited to an intermediate value by the memory module; the intermediate voltage then

represents a logical “1” state while the low voltage continues to represent a logical “0” state. *Id.* at 9:24-31, 9:41-47.

52. The Challenged Patents disclose that the same Address Data/Error and Clock/Busy channels can be used to communicate with multiple memory modules, as shown in Fig. 1C:

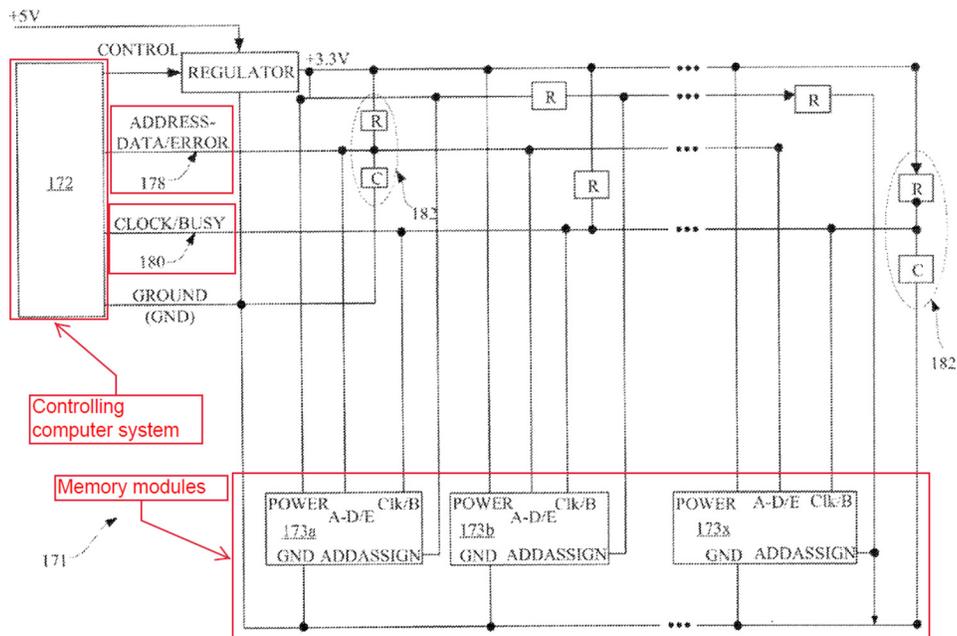


FIG. 1C

**FIG. 1C of the ‘193 Patent (Annotated)**

53. Therefore, the voltage limiting scheme and the use of three voltage levels in the Challenged Patents allow several memory modules to signal a

specified condition (busy or error) simultaneously on a single line. Because the system is concerned with whether *at least* one memory module has a busy or error condition, if multiple memory modules signal an error condition, they will not interfere with each other and the controlling computer system will receive the message (by virtue of the fact that the logical “1” value is now the intermediate voltage rather than the high voltage) that a busy or error condition has occurred. As I further explain below, this feature of signaling and communicating between the controlling computer system and the memory modules is absent from the prior art asserted by UII, particularly Blood.

54. The use of the intermediate voltage advantageously allows the controlling computer system to continue to send data and clock signals to all memory modules, while tracking if a memory module has an error or is busy, using only two lines, which reduces the number of connections needed relative to the prior art. *Id.* at 9:5-23.

55. In an alternate embodiment shown in Fig. 1A disclosed in the Challenged Patents, the busy and error conditions may also be communicated over a common “status” line. In this embodiment, the intermediate voltage enables the

single “status” line to represent the ready, error, and busy states for a plurality of memory modules. In this scenario, all of the memory modules may hold the line low while they are busy processing the command, but hold the line to an intermediate value if there is an error. ’193 Patent at 7:47-62.

### **C. Claim Construction**

56. I understand that UII has not proposed to construe any claim terms in the Challenged Patents. I further understand that at the institution stage, the Board need not construe any terms unless the construction is relevant to the Institution Decision. In my opinion, UII has not shown that any of the challenged claims are invalid as anticipated or obvious regardless of what construction is given.

### **VI. ANALYSIS OF REFERENCES CITED BY UII**

57. I have reviewed the prior art references cited by UII in its Petitions. For the purpose of my analysis, I have considered the substance of these references without determining whether those references by UII are in fact prior art. In my review of the UII’s IPR petitions and the declarations by Dr. Direen on the ‘193 and ‘591 Patents, UII and Dr. Direen repeatedly mischaracterize the inventive features of the Challenged Patents, typically by drastically oversimplifying the

inventions described and claimed. I will point out some of those in the following sections. In addition, UII's IPR petitions and the declarations by Dr. Direen overlook relevant portions of these references which show why the challenged Lexmark patents are not invalid over the cited references.

**A. Applegate (U.S. Patent No. 5,995,774)**

58. U.S. Patent No. 5,995,774 to Applegate et al (Ex. 1004 to both the '1380 and '1381 IPRs) is a 1999 patent by Lexmark, and generally describes “[a]n improved electrophotographic (EP) printer... having a detachable process that contains a non-volatile memory device, which is an EPROM that cannot be erased after a bit is burned.” *See* Ex. 1004 at Abstract. Applegate also generally describes the structure of an EPROM memory designed to be included within a printer cartridge:

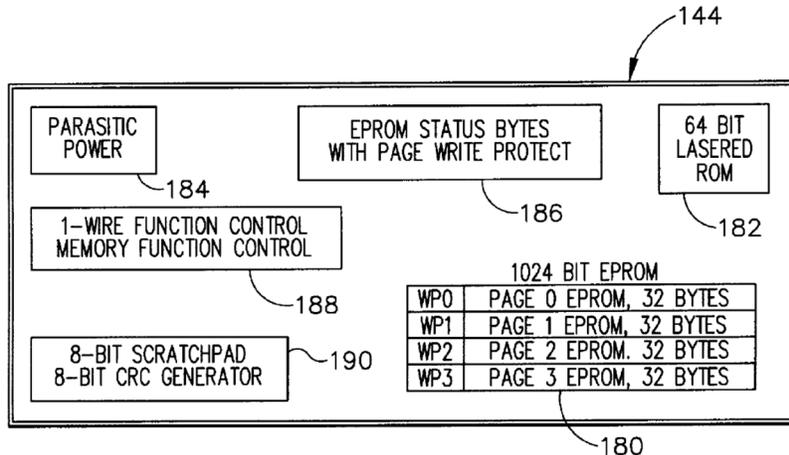


FIG. 6

**FIG. 6 of Applegate**

59. I have reviewed Applegate in its entirety in addition to reviewing the various sections cited by UII and its expert Dr. Direen. Based on my review, Applegate is silent regarding the specific communications protocols between the printer and the memory in the cartridge. Applegate is also silent regarding the specific structure of any commands sent to the memory in the cartridge. The closest disclosure cited by either UII or Dr. Direen, and indeed the only discussion at all in Applegate regarding how signals are communicated between the printer

and the toner cartridge, is a simple block diagram in Fig. 5 showing a two-wire interface 176 (highlighted in red) between the printer and the cartridge:

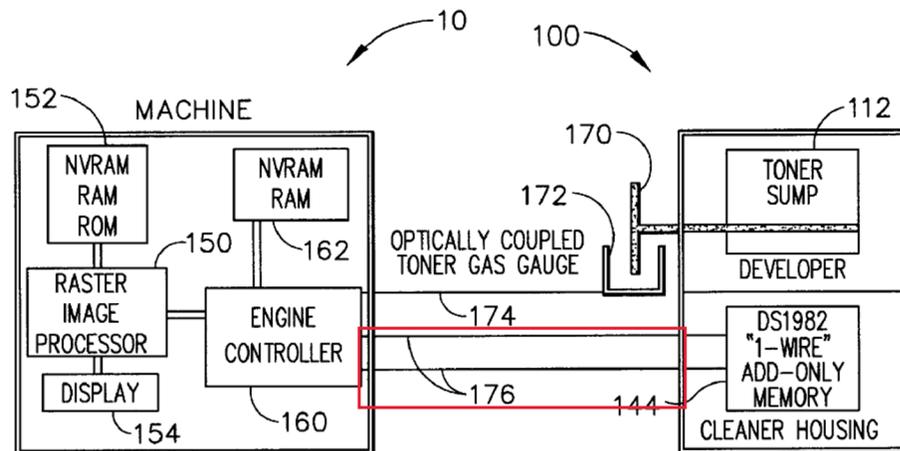


FIG. 5

**FIG. 5 of Applegate (Annotated)**

60. This diagram in Fig. 5 and the accompanying explanation of it in the text in Applegate merely describe the physical structure of the interface. In my opinion, neither this diagram in Fig. 5 nor the explanation of it in the text in Applegate says anything about the content or structure of any messages sent over the two-wire interface 176, nor would a person of ordinary skill in the art infer a

specific communication protocol or the content of the messages from the diagram.

Additionally, in my opinion, the only processing capability shown in Fig. 5 of Applegate is on the side of the printer itself (that is, the left-hand side of the image), including the Raster Image Processor 150 which connects to the display and the Engine Controller 160.

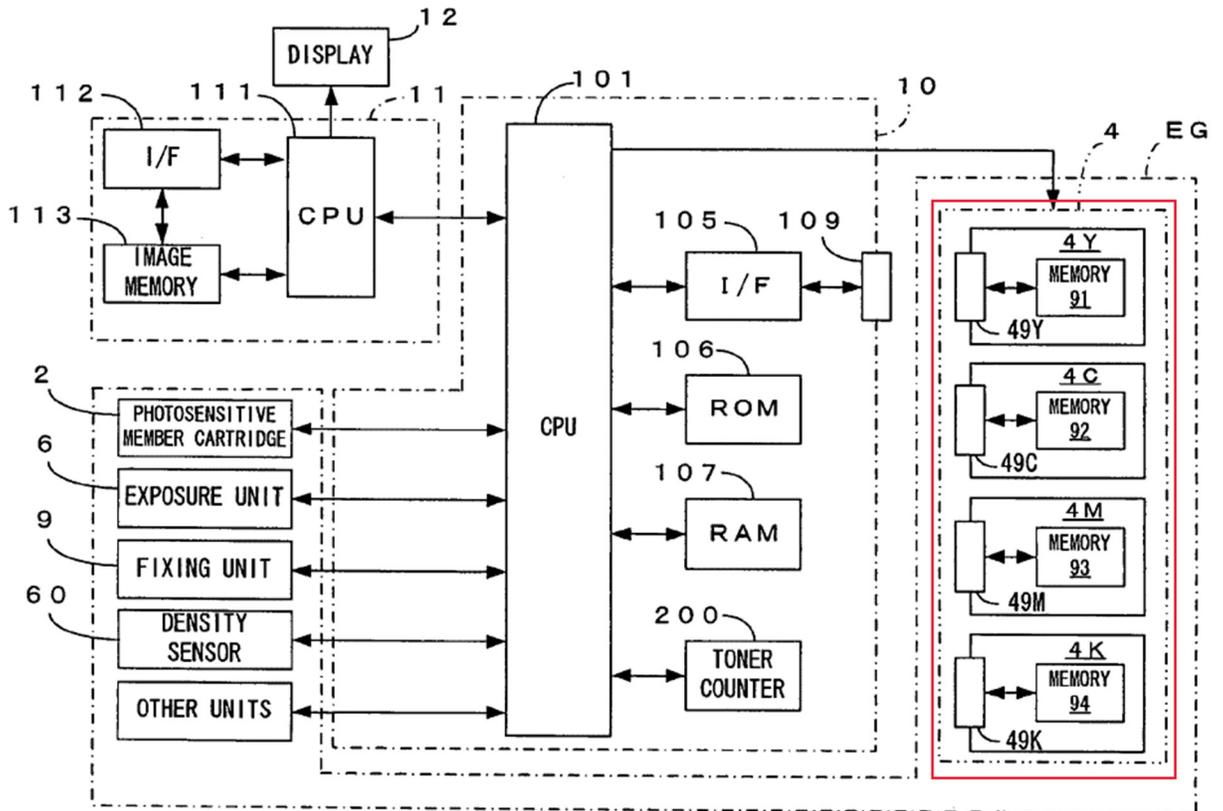
61. In addition to its lack of description of any commands, Applegate does not describe how any such commands are processed by the memory module. In my opinion, this is one of several important differences between Applegate and the Challenged Patents' smart memory module (including the associated processing capabilities) with respect to the claimed subject matter in the Challenged Claims. In the absence of processing capability on the memory module itself as in the smart memory module described by the Challenged Patents, a memory module might only have the capability to passively record values specified by an external processing device (in the case of a printer, a processor on the printer itself as opposed to a cartridge). In the absence of more specific disclosure about commands or how they are processed, a person of ordinary skill in the art would not infer that the disclosure of Applegate teaches anything other than

a basic, passive memory module with respect to the claimed subject matter in the Challenged Claims.

**B. Hama (U.S. Patent No. 7,269,362)**

62. U.S. Patent No. 7,269,362 to Hama et al (Ex. 1005 to both the '1380 and '1381 IPRs) teaches an “Image Forming Apparatus, Control Method, and Toner Consumption Calculating Apparatus and Method.” It appears to me that UII relies on Hama, at least in the Petition on the '193 Patent, to argue that Hama teaches an “increment counter command.” In my opinion, this is incorrect and contradicts with the disclosure in Hama.

63. According to Hama, a printer may connect to a series of developer units 4Y, 4C, 4M, 4K (corresponding to different ink colors), each of which has an electrical interface 49 to the main printer body, a toner reservoir, and a memory (91-94). See Fig. 2:



**FIG. 2 of Hama (Annotated)**

64. Hama teaches that the memories 91-94 store “the initial value of the cumulative count of toner consumption and the current remaining toner amount.” Hama at 22:15-20. Hama’s system relies on a combination of estimates of the amount of toner consumed measurements of toner density on a test image in order

to inform a user whether a cartridge needs to be replaced, partly because toner counts alone may be erroneous. *Id.* at 2:3-46. Figs. 15 and 16 show flow charts in which the system uses both counter information and toner test information to determine whether to update the “cumulative count” stored in the memory. In Fig. 15, the processor (in the main printer) first reads the counter information and determines whether it is below a predetermined value, and if so forms a test image and changes the count (at step S15) if the test image is less dense than a predetermined value. In Fig. 16, the steps are reversed and the processor first checks the test image, then the counter information:

FIG. 15

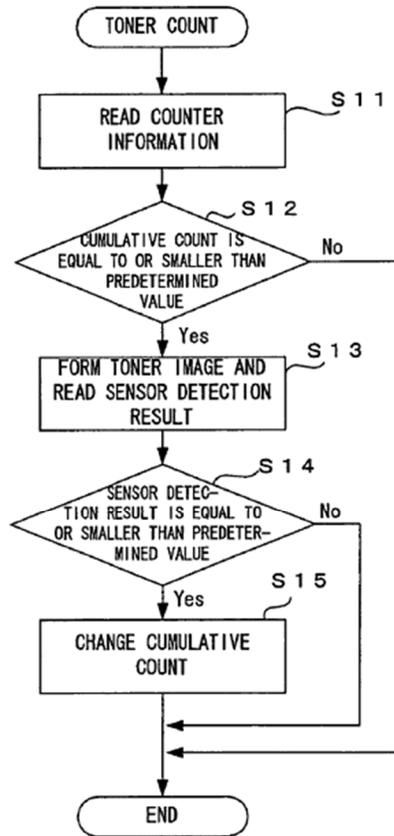
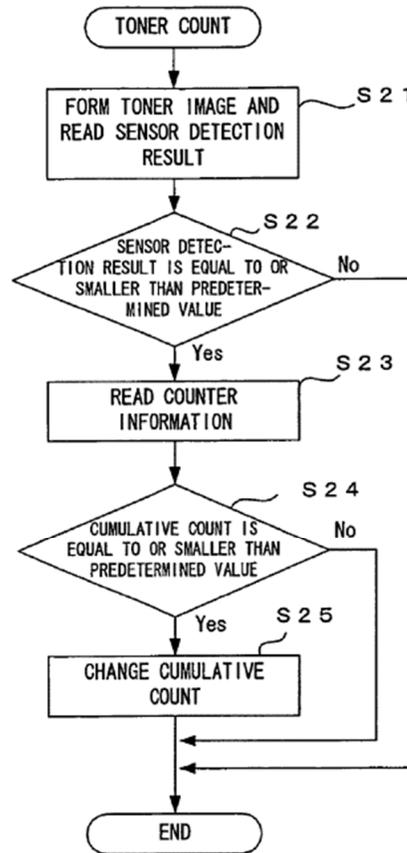


FIG. 16

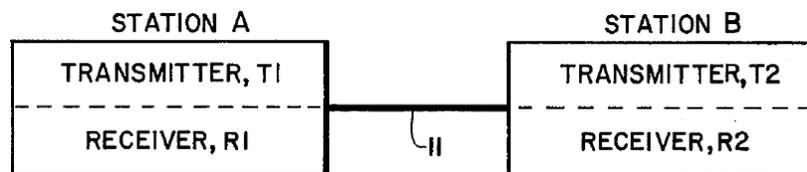


FIGS. 15 and 16 of Hama

**C. Blood (U.S. Patent No. 3, 933,867)**

65. UII and its expert Dr. Direen rely extensively on Blood (Ex. 1003 to both the '1378 and '1381 IPRs) in several of their obviousness combinations. It appears to me that the primary reason that UII and Dr. Direen cite Blood is that it teaches a signaling method between two transmitting and receiving stations which results in an "intermediate" voltage. However, as explained below, Blood teaches a signaling method very different than that what is claimed in the Challenged Claims of the Challenged Patents for which UII relies on Blood.

66. Based on my reading of Blood, Blood generally describes a method for "full duplex transmission of digital data on a single signal line." (Abstract.) Fig. 1 in Blood illustrates this by showing a signal line between two generic stations A and B which each have a transmitter and a receiver.



**FIG. 1 of Blood**

67. Blood states that both “transmitter” and “receiver” are “generic expressions to denote many diverse systems and subsystem components, such as teletypewriters, CRT display devices, memories, registers, central processing units and the like...” Blood at 2:23-29. Blood does not discuss implementation in memories in any further detail beyond this statement.

68. The absence of such teachings by Blood is significant to both the ’1378 and ’1381 Petitions and the supporting Direen Declarations because both sets of documents repeatedly refer to hypothetical situations involving memories and state that Blood teaches particular usages of a memory. For example, the Petitions rely on Blood for various claim limitations that require a memory to receive a command and, as part of the processing of that command, limit the voltage on a signal line to indicate the existence of a condition, which may be either a busy condition or an error condition. See, e.g. IPR2019-01381 (’193 Patent) at 30. In my view, such statements are unsupported by Blood’s disclosure at least because Blood does not teach any specific application of its teachings to a memory beyond generally listing “memories” as one of the potential systems that it

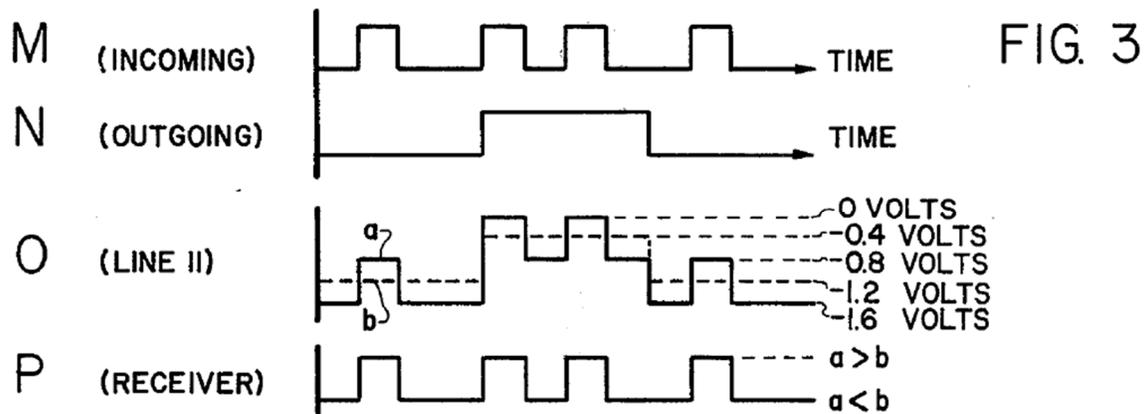
could apply to. In particular, Blood says nothing about handling error or busy conditions by any transmitter or receiver, particularly not a memory.

69. The Petitions and Direen Declarations appear to rely on Blood for teaching a signal line between two stations that may result in an “intermediate” voltage value. However, the claims of the challenged ‘193 and ‘591 Patents require much more than simply some form of an intermediate voltage, and the intermediate voltage taught by Blood is very different from what the claims require.

70. Blood teaches a duplexing method in which each station is a binary device that sets the voltage to a high level or a low level without providing any intermediate voltage between the high and low levels by each station. In other words, each station generates a binary high/low waveform on the signal line and is not taught by Blood to generate an intermediate voltage level. Blood describes a well-known technique for adding binary signals from two communicating stations together on a single transmission line connecting the two communicating stations to enable simultaneous duplex (i.e. so both devices can transmit at the same time). Blood teaches that “the net composite of the outgoing and incoming signals

appearing in the signal line is a scalar or analog addition of the two signals.”

Blood at 3:35-47. This addition of two binary signals with two voltage levels on the signal line can lead to three different signal levels on the signal line while the two communicating stations each only generate binary signals without generating an intermediate voltage level between the two binary voltage levels. For example, in Fig. 3, lines M and N show the binary signals from separate transmitters, while line O is the resulting signal on the common signal line from the addition of the two signals:

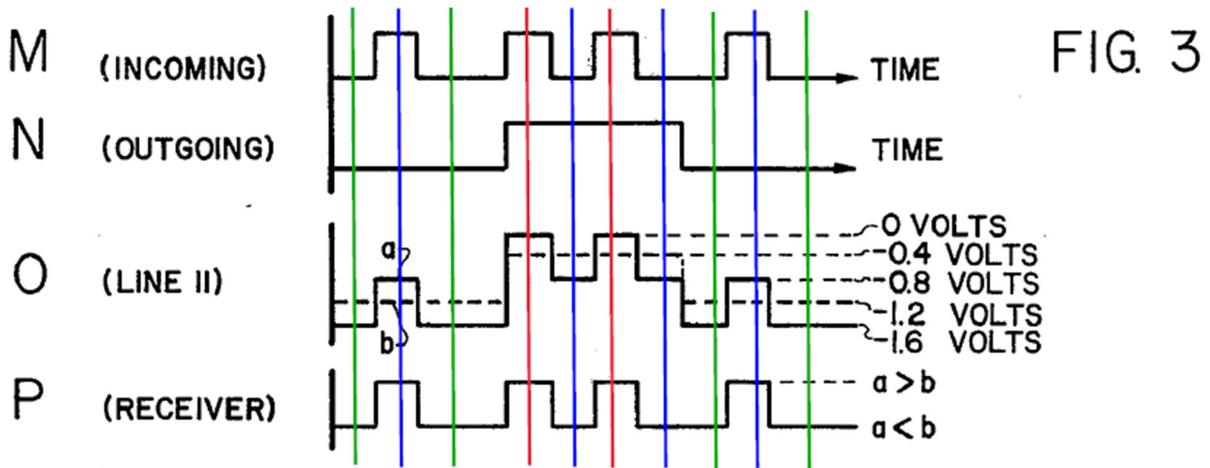


**FIG. 3 of Blood**

71. The receiver at each station in Blood uses a differential amplifier to subtract the signal transmitted by that station, so that the receiver only receives the signal from the transmitter in the other station. In Fig. 3, for example, the differential amplifier at the station transmitting signal N subtracts the value of the outgoing signal N from the composite signal O on the connecting line to form resulting signal P, which is the same as the output of the other station. Blood at 4:21-33.

72. In the figure below, I have annotated in color the result of the “scalar or analog addition” function taught by Blood with reference to Fig. 3: three different resultant voltage levels on the signal line by adding two different binary signals from the two communicating stations in a total of four different signal states. When both signals (lines M and N) are high, the resulting signal O on the connecting signal line is at the highest voltage. These time points are annotated below in red. When both signals are low, the resulting signal O on the connecting signal line is at the lowest voltage. These points are annotated below in green. When one signal is high and the other signal is low, regardless of which is which,

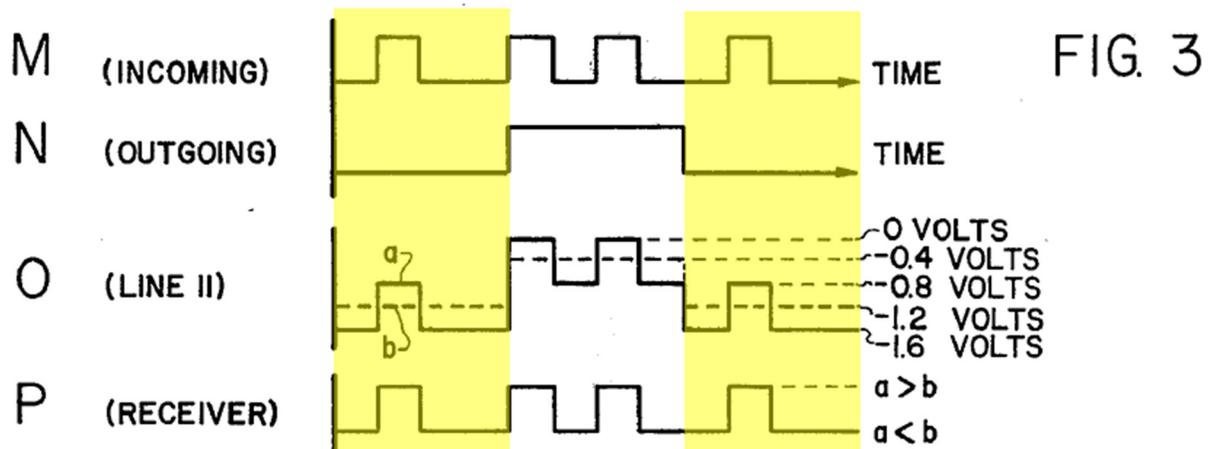
the resulting voltage is at an intermediate level, which is shown below at the time points indicated in blue for two different signal states from the two stations:



**FIG. 3 of Blood (Annotated)**

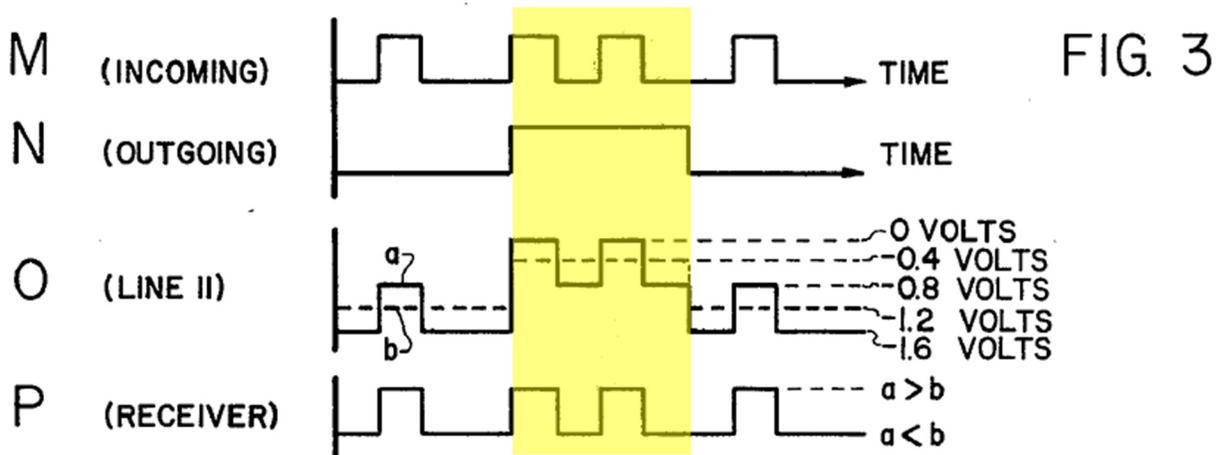
73. Because the voltages taught by Blood are only the result of the combined action of the two transmitters of the two stations connected to the signal line, there is no point at which a voltage as a result of combining two binary signals from the two transmitters that would otherwise go between “low” and “high” states because signals from one transmitter is limited by the other signal . The resulting voltages shown in Blood’s Fig. 3 on Line “O” are only the result of the combined action of the two transmitters. The reason Blood ends up with 3

voltages at 0 volt (top), -0.8 volt (middle) and -1.6 volt (bottom) on Line “O” is because two 1 bit digital signals whose values are each only 0 or 1 are added together and hence the results can only be 0, 1 or 2 (and then scaled to whatever voltage is desired). The highest voltage only occurs when both transmitters transmit high, whereas the lowest voltage only occurs when both transmitters transmit low. Neither station by itself produces a signal that causes the resulting signal on line “O” to go from “high” to “low.” Instead (for example), when the signal from station “N” is low, the resulting voltage “O” alternates between the intermediate and low voltages based on the other signal “M:”



**FIG.3 of Blood (Annotated)**

74. However, when the signal from station “N” is high, the resulting voltage alternates between the intermediate and high voltages based on the other signal “M:”



**FIG.3 of Blood (Annotated)**

75. In neither case does one station limit the resulting signal to a value that is both less than the high “one” value and greater than the low “zero” value. At all times, each station is a binary station and simply sends out a high voltage level or a low voltage level but nothing between the high and low voltage levels: there is no intermediate voltage generated by either one of the two communicating stations coupled to the signal line. The “intermediate” voltage shown in Fig. 3 of

Blood occurs whenever one signal is high and the other is low, regardless of which is which.

76. I have prepared the chart below summarizing the states of the voltage as taught by Blood, which is substantially different from the intermediate voltage limiting functions taught by the '193 Patent and the '591 Patent:

<b>Station A/ Station B</b>	<b>High</b>	<b>Low</b>
<b>High</b>	High	Intermediate
<b>Low</b>	Intermediate	Low

77. In order to show how this feature differs from the intermediate voltage limiting functions taught by the Challenged Patents, I have reproduced my charts from my discussion of the inventive features of the Challenged Patents for comparison:

Address Data/Error channel:

<b>Voltage Level Generated from Memory Module and Applied to Single Line</b>	<b>Address Data State</b>	<b>Error State</b>

<b>High</b>	Logical “1”	No error (i.e., no device signaling an error)
<b>Intermediate</b>	Logical “1”	At least one device has an error
<b>Low</b>	Logical “0”	Independent of whether any device has an error

Clock/Busy channel:

<b>Voltage Level Generated from Memory Module and Applied to Single Line</b>	<b>Clock State</b>	<b>Busy State</b>
High	Logical “1”	No device is busy
Intermediate	Logical “1”	At least one device is busy
Low	Logical “0”	Independent of whether any device is busy

78. In another aspect, different from the Challenged Patents, Blood also does not teach that more than two memory cells can communicate simultaneously on the same line. Each device in Blood simply adds its own binary voltage to the

signal line, then subtracts its own voltage from the result to identify the signal being transmitted by the other device. If more than two devices are signaling at the same time, the remaining device would not be able to interpret the signal because after subtracting out its own signal, it would still be left with a signal that is the result of the combined signals of two or more other devices. Therefore, the system of Blood would not be able to handle simultaneous communication between multiple devices without additional duplexing or multiplexing methods not described in Blood itself. However, as taught by the Challenged Patents, the use of intermediate voltages to signal busy or error conditions enables the processing device to communicate with a plurality of devices while simultaneously assessing whether at least one device is busy, at least one device has an error, or if all devices are ready.

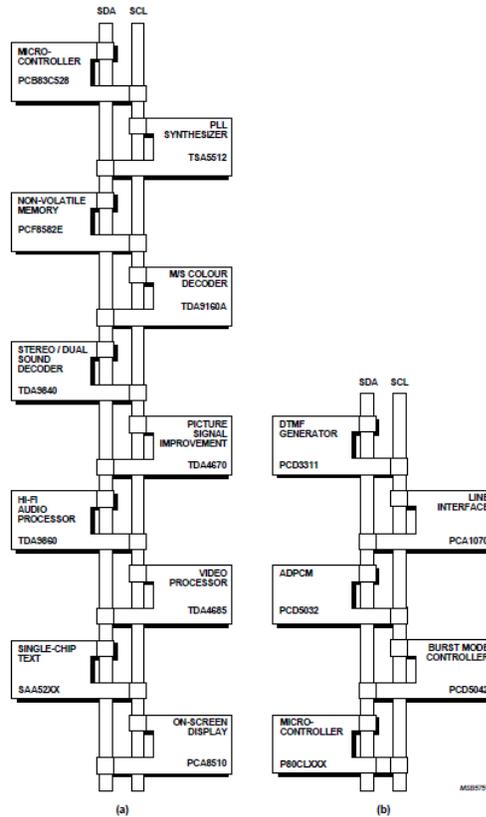
79. In light of the teachings in Blood, it is my opinion that Blood teaches that each of the two stations in its Fig. 3 produces a binary signal carrying either a high level or a low level and does not teach that either station shown in Fig. 3 “limits” the other to an intermediate voltage between the high and low levels. Blood simply teaches that the signals from the two stations are added together, and

each station simply subtracts its own signal to find the signal from the other station. This is not a “limiting” function for each of different stations in the Challenged Patents.

**D. Purported I<sup>2</sup>C Specification**

80. I understand that UII has provided a document which they claim is version 2.1 of the Phillips I<sup>2</sup>C Bus Specification (“I<sup>2</sup>C Specification”) in its Petitions. This I<sup>2</sup>C Specification also does not disclose the key inventive features of the challenged Lexmark patents.

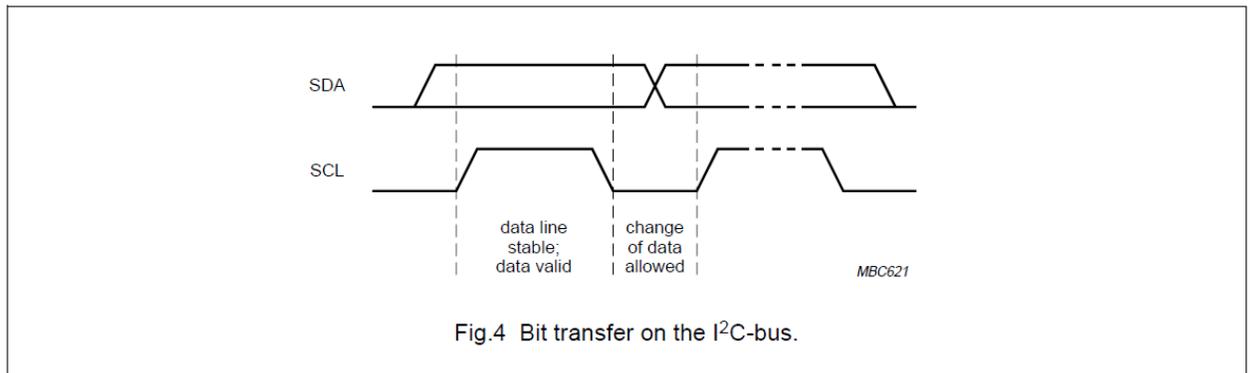
81. The I<sup>2</sup>C Specification teaches a common bus and associated protocols to link one or more master components to a plurality of slave components using two signal wires, one of which carries a clock signal (serial clock line (SCL)) and the other of which carries data (serial data line (SDA)). For example, Fig. 1 of the I<sup>2</sup>C Specification shows representative examples of applications with multiple components connected to a controller via a bus comprising the SDA and SCL lines:



**Fig. 1 of I<sup>2</sup>C Specification**

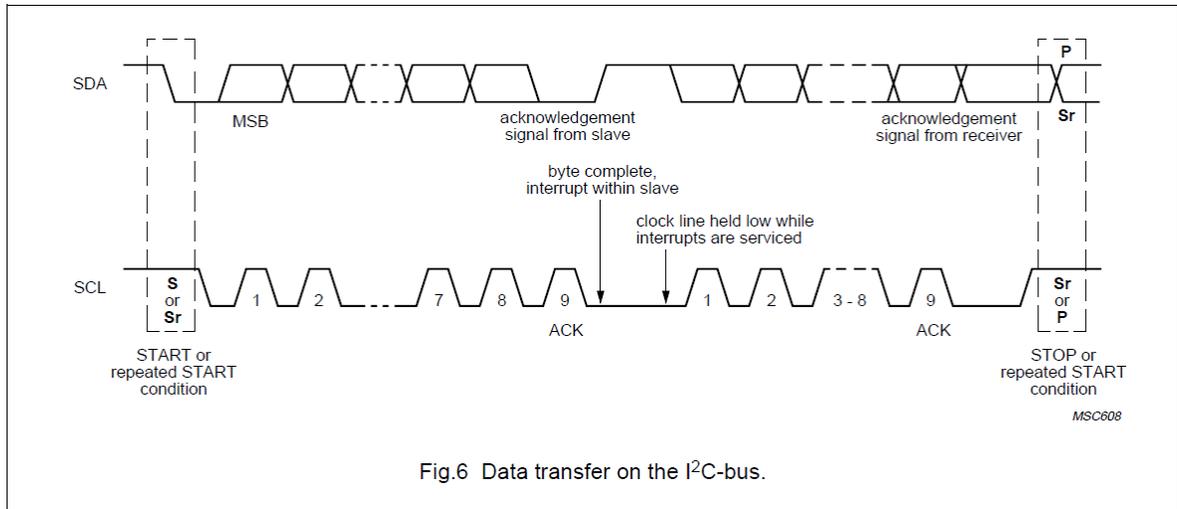
82. The purpose of the clock signal on the SCL line is to control the timing and speed of data transmission on the common bus, as well as to define certain start and stop conditions. The I<sup>2</sup>C Specification accomplishes this by defining that data on the SDA line must be stable during the “high” period of the SCL line’s clock cycle and may only change when the clock cycle is low. I<sup>2</sup>C

Specification, ¶ 6.1. Therefore, one bit of data on the SDA line may be transmitted for each high/low cycle of the clock signal on the SCL line. This is shown in Fig. 4 of the I<sup>2</sup>C Specification:



**Fig. 4 of I<sup>2</sup>C Specification**

83. A critical feature of the I<sup>2</sup>C Specification is that only one device may transmit at a time. Once a device has received a transmission, it responds with an acknowledgement, which may not begin until the original transmission is complete. I<sup>2</sup>C Specification at 10, ¶ 7.2. For example, Fig. 6 shows a sequence in which a master transmits a message and the slave acknowledges it only after the original transmission is complete:



**Fig. 6 of I<sup>2</sup>C Specification**

84. In order to ensure that only one device transmits at a time, the I<sup>2</sup>C Specification specifies detailed procedures for “arbitrating” which device may transmit in a conflict. See I<sup>2</sup>C Specification at 12, ¶ 8.2. This process involves each master checking the voltage on an SDA line so that “a master which transmits a HIGH level while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn’t correspond to its own level.” Therefore, each transmitter in the I<sup>2</sup>C Specification is a binary device that only generates a binary signal carrying either a high level or a low level and does not “limit” any output signal to an intermediate voltage between the high and low

levels. This binary nature of each of the transmitters in the I<sup>2</sup>C Specification is similar to the binary nature of the stations in Blood. For example, Fig. 9 depicts the arbitration process based on binary signal levels of masters 1 and 2 in the I<sup>2</sup>C Specification:

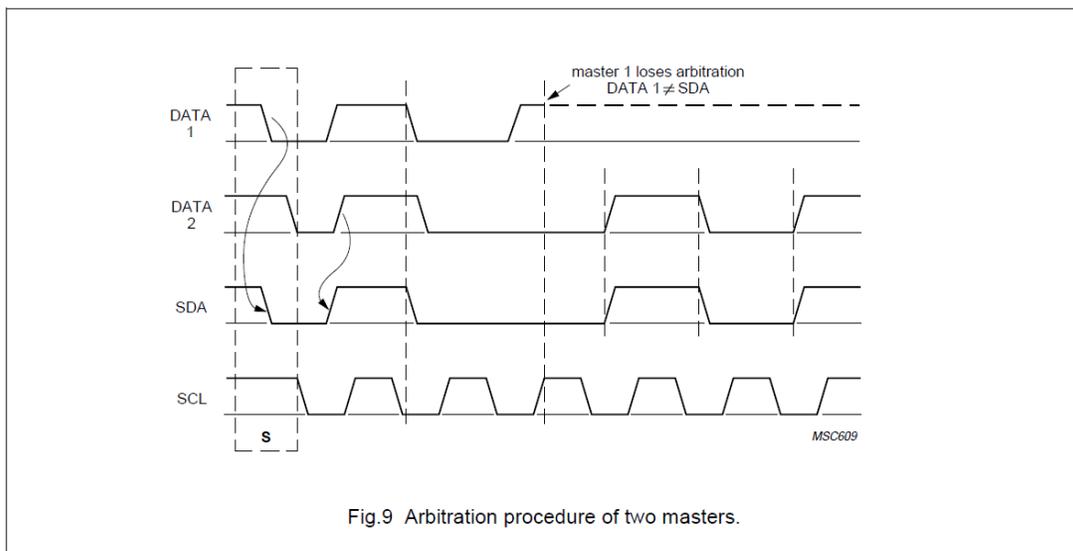


Fig.9 Arbitration procedure of two masters.

### Fig. 9 of I<sup>2</sup>C Specification

85. Nowhere does the I<sup>2</sup>C Specification teach that two devices may communicate simultaneously on either line. I note that the arbitration procedure discussed above is specifically designed to avoid such a condition.

86. The I<sup>2</sup>C Specification also does not teach any intermediate voltage in any form on either line, whether it is a device on the bus transmitting at an intermediate voltage or a device limiting the voltage to such an intermediate voltage. All of the communications over the two lines disclosed by the I<sup>2</sup>C Specification are simple binary communications; that is, the SDA and SCL lines alternate between low and high voltages. I have copied below Figs. 4-10, each of which only shows the SCL and SDA lines alternating between binary “high” and “low” voltages, without any teaching or suggestion of an intermediate voltage:

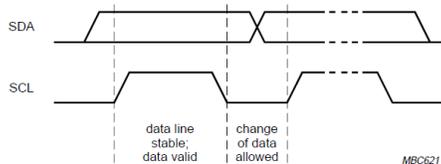


Fig.4 Bit transfer on the I<sup>2</sup>C-bus.

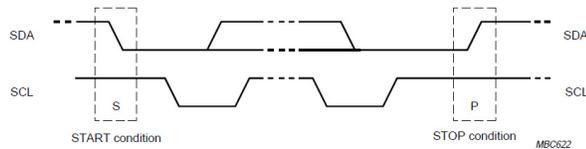


Fig.5 START and STOP conditions.

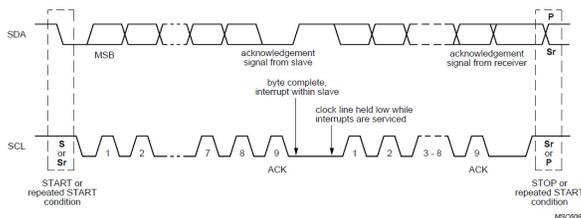


Fig.6 Data transfer on the I<sup>2</sup>C-bus.

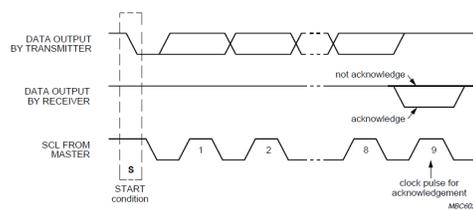


Fig.7 Acknowledge on the I<sup>2</sup>C-bus.

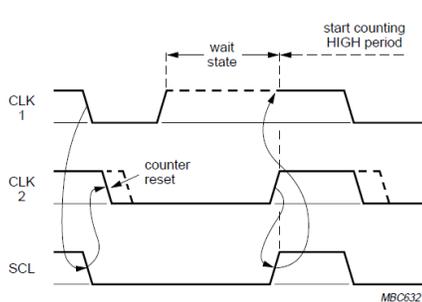


Fig.8 Clock synchronization during the arbitration procedure.

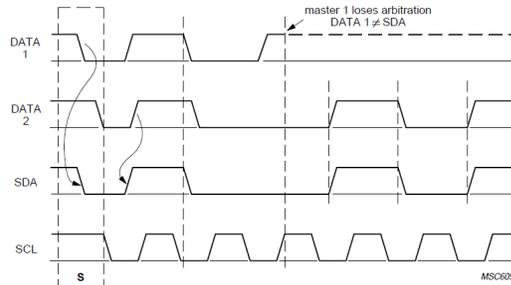


Fig.9 Arbitration procedure of two masters.

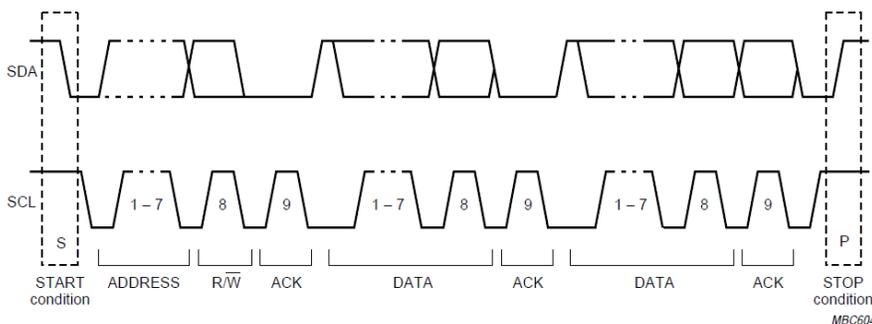


Fig.10 A complete data transfer.

87. Although the I<sup>2</sup>C Specification does not disclose any feature where a device on the line can limit voltage to an intermediate value, it does teach that a slave device can hold the SCL line to a zero value. I<sup>2</sup>C Specification at 11, ¶ 8.1. However, this feature is very different from the voltage limiting features discussed in the challenged patents and has a very different purpose and result.

88. The I<sup>2</sup>C Specification teaches that “clock signals from a master” may be “stretched by a slow-slave device holding-down the clock line.” I<sup>2</sup>C

Specification at 8. This feature is known as “clock stretching.” Because only one data bit may be transmitted per clock cycle, holding down the clock signal enables a slave device to limit the rate at which data is transmitted, which enables a slower device on the bus (e.g. what the I<sup>2</sup>C Specification refers to as a “slow-slave” device) to ensure that data is not transmitted faster than it is received.

89. Additionally, if the slave device cannot receive or transmit another complete byte of data until it has performed some other function (e.g. servicing an internal interrupt), the slave device can hold the SCL line low at the conclusion of the byte of data. I<sup>2</sup>C Specification at 10, ¶ 7.1 Again, because data bits may only be changed when the clock signal changes, this feature stops the master from transmitting additional data until the slave device releases the line. This feature is shown in Fig. 6:

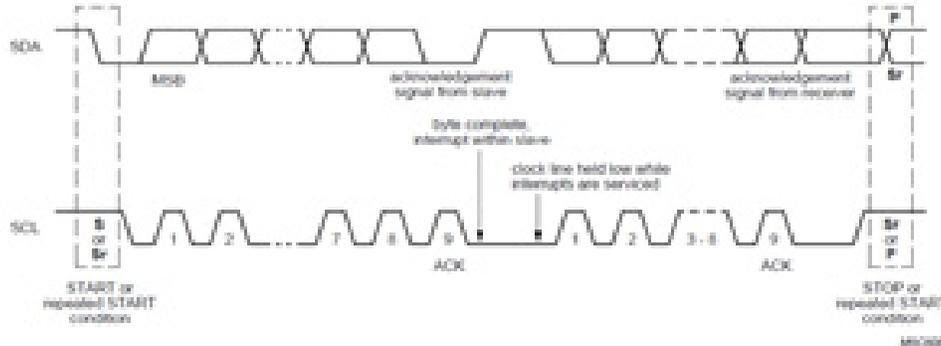


Fig.6 Data transfer on the I<sup>2</sup>C-bus.

### Fig. 6 of I<sup>2</sup>C Specification

90. In both cases (the slave device holding down the SCL line to slow the transmission rate or to service an internal interrupt), the data is held to the low value rather than an intermediate value. There is no disclosure of limiting voltage to an intermediate value in the I<sup>2</sup>C Specification. Additionally, the purpose of holding the line low in both cases is to prevent further transmission of data until the line is released. In my view, allowing a master device to continue to transmit clock signals at an intermediate voltage while the line is being held low would defeat the purpose of the clock-stretching features taught by the I<sup>2</sup>C Specification.

91. Petitioner's expert Dr. Direen states several times that the bus shown in the challenged patents, e.g. at Fig. 1 of the '193 Patent, is an I<sup>2</sup>C interface. See,

e.g. IPR2019-01381, Ex. 1002, ¶ 23. Although Dr. Direen does not fully explain the basis of this statement, it appears that his statement is based merely on the '193 Patent teaching a two-wire interface, one of which is a line which carries data including clock signals and the other of which is an interface which carries data including Address/Data information.

92. I disagree with Dr. Direen based on the I<sup>2</sup>C Specification. Merely having a two-wire interface with lines that include Clock and Address/Data information does not make an interface an I<sup>2</sup>C interface. The purpose of common standards such as the I<sup>2</sup>C Specification is to enable a fixed set of communications protocols that enable devices on the bus to communicate with each other. Altering the protocols used by a device on the bus in ways not contemplated by the specification means that other standard-compliant devices would no longer recognize communications from that device without corresponding alterations to their own communications protocols. Such alterations mean that the devices are no longer using the protocols specified by the I<sup>2</sup>C Specification. For example, because the I<sup>2</sup>C Specification is silent on intermediate voltages, an I<sup>2</sup>C Specification-compliant device would not need to recognize any voltage other than

a “high” or “low.” Likewise, communicating a busy or error condition simultaneously over the same channel as a clock or address/data line is also inconsistent and incompatible with the I<sup>2</sup>C Specification.

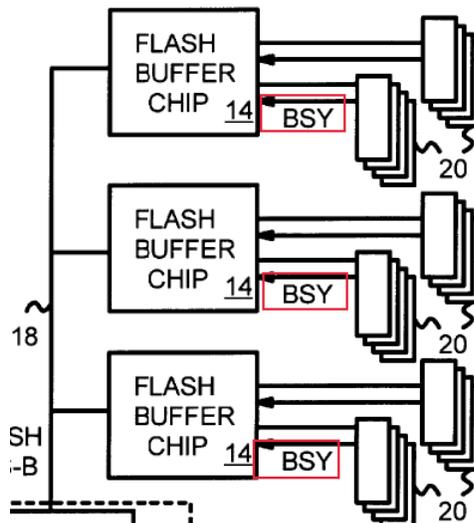
**E. Bruce (U.S. Patent No. 5,822,251)**

93. Bruce is Ex1003 in the 1380 Petition on the ‘786 Patent and Ex 1005 in the 1378 Petition on the ‘591 Patent and generally describes an expandable flash memory system. See Bruce at Abstract. In the description of the related art, Bruce refers to hard disks as the “traditional storage medium in computer systems,” but notes that “hard disks suffer from their inherent fixed size” and lack of expandability. Bruce at 1:21-44. Bruce is therefore directed to this problem of expandability of a memory chip by grouping flash memory chips in banks attached to common flash buffer chips. Bruce at Abstract, Fig. 1.

94. Petitioner UII and its expert Dr. Direen appear to rely on Bruce for the teaching of a “busy” signal from the flash memory chips. This interpretation of Bruce by UII and Dr. Direen lacks basis in the teachings by Bruce because Bruce teaches communicating “busy” status information via a *separate* line from any other signal lines: "All busy signals from flash-memory chips in a bank that is

connected to a flash buffer chip are connected to a **common bank-busy line.**"

Bruce at 3:21-25 (emphasis added). The flash buffer chip then generates a single busy output (again via a separate line from any other signal) to the flash bus. *Id.* at 3:26-31. The separate bank-busy lines are shown in Bruce's drawings such as Fig. 2 which is reproduced below.



**FIG. 2 in Bruce (Annotated)**

95. Based on my reading of Bruce, Bruce does not teach or suggest communicating a "busy" signal over the same line as any other data in any manner, particularly not by limiting the voltage of a data or clock communication line to an intermediate voltage.

96. Bruce does not talk at all about printer cartridges or any other similar type of disposable components with embedded memory. The expandability concern to which Bruce is directed is a distinct technical issue from those faced in designing small systems with embedded disposable memories. In my opinion, a person of ordinary skill in the art would recognize that the technical issues faced by Bruce, specifically expanding memory in a fixed system, are distinct from those faced in designing embedded memories for devices such as printer cartridges. There is no indication that Bruce deals with a system that is intended to be disposable; indeed, Bruce's purpose is to enable a system that can be used for a long time through expansion. Adding a separate "busy" line to a common flash buffer chip, as Bruce does, helps the system of Bruce meet the need for an expandable system, but does nothing for the problems addressed by the Challenged Patents, which teach a need to minimize the number of electrical connections used by the device. See, e.g. '193 Patent at 1:60-2:11.

## **VII. ANALYSIS OF INVALIDITY GROUNDS ASSERTED BY UII PETITION AGAINST '786 PATENT**

### **A. Summary of Grounds Asserted by UII**

97. I understand that UII has asserted in its Petition the following grounds of invalidity against the '786 Patent:

- Ground 1: Anticipation by Applegate (claims 1-4, 6-14, and 16)
- Ground 2: Obviousness over Applegate and Bruce (claims 5 and 15)

98. In my opinion, UII has not shown that the '786 Patent is invalid on any of the grounds asserted in its Petition.

### **B. Ground 1: Applegate does not anticipate any claims of the '786 Patent**

- 1. Applegate does not teach “receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises... an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules”**

99. Each of independent claims 1 and 9 of the '786 Patent contains an identical limitation requiring an “increment counter command” received at a memory module from a processing device. Claims 2-8 and 10-15 depend from

claims 1 and 9 and therefore incorporate the same limitation. In my opinion, UII has not shown where such a command is taught by Applegate.

100. The entire discussion of these claim elements in UII's Petition is on pages 10 (for claim 1) and 18 (for claim 9) of the Petition, and is identical for each claim where this limitation appears. In each case, UII cites the following portions of the specification of Applegate:

- Fig. 5
- Fig. 6
- 2:17-21
- 11:31-38
- 20:18-22

101. Other than a cursory assertion that Applegate discloses the claim limitation, I found no discussion in this section of the Petition explaining UII's view as to how this claim element is met. In the sections below, I review and analyze the teachings of each of the portions of Applegate cited by UII. In my

opinion, none of them discloses the claimed increment counter command. I will discuss each of these citations individually.

102. Fig. 5 of Applegate is reproduced below:

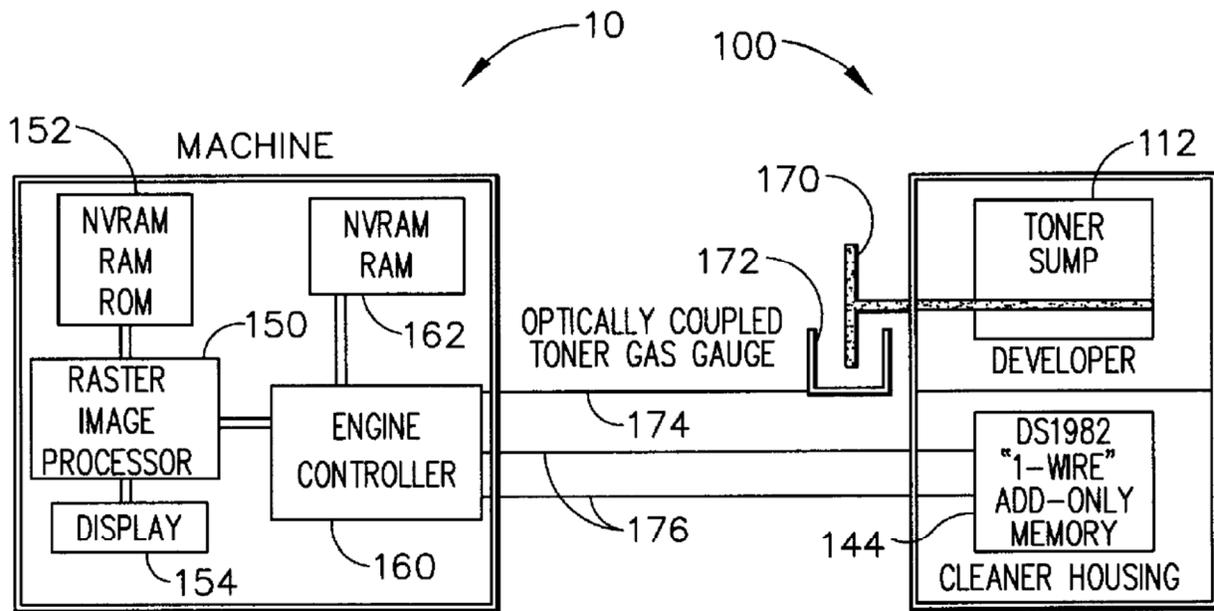


FIG. 5

FIG. 5 of Applegate

103. Fig. 5 of Applegate is simply a schematic diagram of the hardware taught by Applegate. The only thing that Fig. 5 shows with respect to

communications between the printer and the memory in the cartridge is the physical structure of the interface, such as the two wires 176 between the engine controller 160 and the add-only memory 144. Fig. 5 of Applegate does not explain any communications protocols used, nor does it discuss the structure of any communications (commands or otherwise) sent over those two wires. Therefore, in my opinion, Fig. 5 does not teach the claim limitation.

104. Fig. 6 in Applegate is reproduced below:

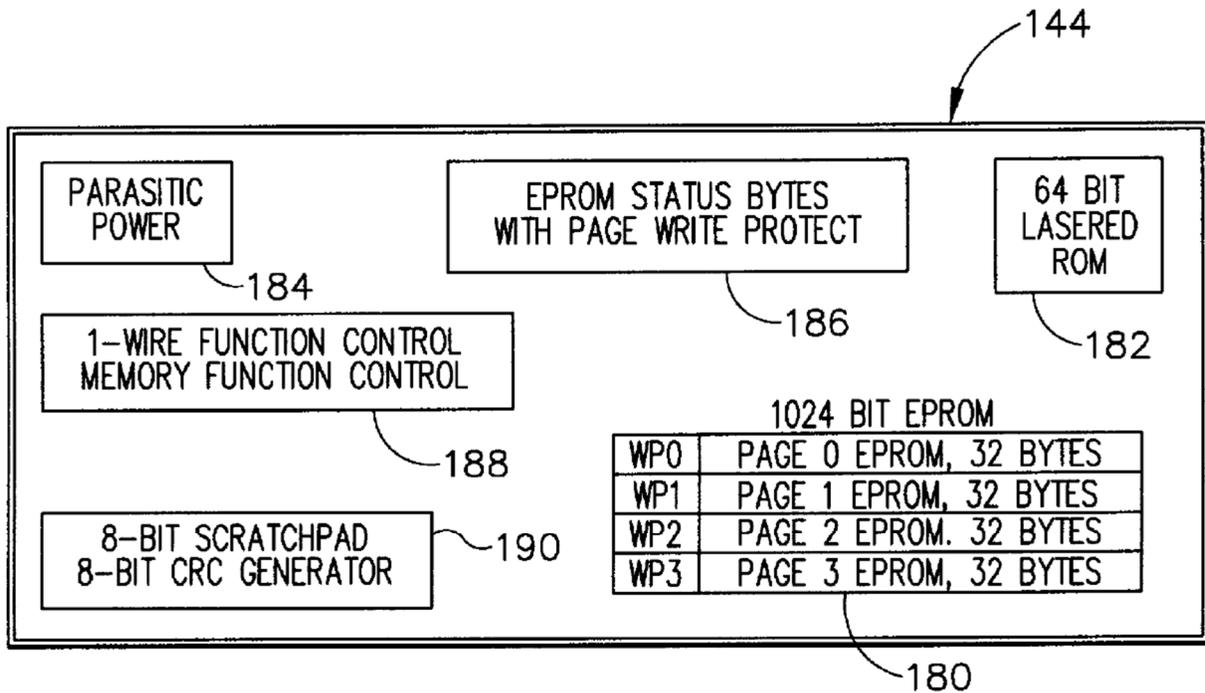


FIG. 6

Fig. 6 of Applegate

105. Fig. 6 of Applegate is an illustration of the structure of the memory. Fig. 6 does not say anything about the structure of commands that might be received by the memory. Therefore, in my opinion, Fig. 6 of Applegate does not teach the claim limitation.

106. Column 2, lines 17-21 of Applegate is located within the “Background of the Invention” section of Applegate, and discusses a prior art patent, U.S. Pat. No. 5,276,461 owned by Tokyo Electric. I note that the disclosure of this prior art patent is not incorporated by reference into the disclosure of Applegate, but rather is simply cited as the prior art before Applegate. Therefore, I understand that it is inappropriate to consider this passage from the Tokyo Electric ’461 Patent part of the invention claimed by Applegate for purposes of anticipation as the law has been explained to me by Lexmark counsel. It is a different patent covering a different invention by different inventors at a different company. Nevertheless, this passage in the Tokyo Electric ’461 patent does not teach the claim limitation even if considered with the remainder of Applegate. Column 2, lines 17-21 of Applegate read as follows:

*The non-volatile memory comprises an EEPROM  
integrated circuit, which has a new count value  
incremented every time the printer produces a new  
printed sheet of print media.*

107. This discussion of Applegate only notes that a new count value is incremented when the printer produces a new printed sheet of print media. Therefore, Column 2, lines 17-21 of Applegate is silent about *how* the count is incremented or where the increment calculation is performed, and says nothing about any command from a processing device to a memory module, much less an increment counter command as claimed. In my opinion, there is also no reason to infer that such a command exists. Therefore, in my opinion, this passage does not show the claim limitation.

108. Column 11, lines 31-38 of Applegate reads as follows:

*Engine controller 160 is also in communication with an optically coupled toner “gas gauge sensor” 172, via an electrical conductor 174. Engine controller 160 is also in communication with the EPROM 144 that is mounted to the cleaner housing sub-assembly 130 of the process cartridge 100. This interface between engine controller 160 and the EPROM 144 is preferably via a two-wire electrically conductive path 176.*

109. This passage is the written description that corresponds to Fig. 5 of Applegate, which I discussed above. Like Fig. 5 in Applegate, this passage merely describes the physical hardware characteristics of the interface between the printer and the cartridge, and says nothing about communication protocols or particular commands. Therefore, in my opinion, this passage does not teach the claim element.

110. Column 20, lines 18-22 of Applegate: The cited passage reads as follows:

*Starting at a step 350 on Fig. 8, a sheet of print media is printed for a particular print job. This step is arrived at for every print job received by printer 10. After that occurs, at a step 352 the toner gram count is updated after this sheet of print media has completed its printing.*

111. UII does not provide any analysis in the Petition explaining how this passage in Applegate purportedly meets the claim limitation. For reasons provided below based on my analyses, it does not.

112. First, the passage says nothing about a command as required by the claim limitation. UII does not explain how the passage at 20:18-22 of Applegate teaches a “command,” and I am not aware of any reason to infer a command based on this passage. The passage is a description of a figure in Applegate which describes actions taken by the printer. There is no description of a communication protocol which includes a specified command, nor does this passage say where the toner gram count being updated is located.

113. Second, the passage does not teach incrementing a counter. The claim limitation of the '786 Patent specifically requires incrementing a counter, not just updating a value of some sort. Although UII does not argue that this claim element is inherent in Applegate, the fact that the cartridge in Applegate may have a “toner gram count” does not mean that the count is necessarily updated by a command to increment the counter. There are multiple ways that a memory value like the “toner gram count” can be updated, most of which involve the processor in the printer simply writing an updated value to the memory module. For example, if the processor on the printer “knows” (either by querying the memory on the toner cartridge or by recording toner usage in its own separate memory) that the toner

gram count at the start of a printing job was 160 grams and that approximately 10 grams of toner were used during a print job, the processor can write the new value (150) to the memory module. As I explained at Paragraphs 42-44 above, sending an updated value to the memory module is different from sending an increment counter command, in which case the command instructs the memory module to increment the counter (that is, to add to a value already stored on the memory module). This particular step is not specifically disclosed in Applegate beyond the high level statement of “the toner gram count is updated” (Applegate at 20:18-26). Simply put, the disclosure in Applegate is not sufficient to identify any command that tells the memory module to increment a counter.

2. **Applegate does not teach “receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises... a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules”**

114. Each of independent claims 1, 9, and 16 of the '786 Patent contains an identical limitation requiring an “punch out bit field command” received at a memory module from a processing device. Claims 2-8 and 10-15 depend from

claims 1 and 9 and therefore incorporate the same limitation. In my opinion, UII has not shown where such a command is taught by Applegate.

115. The entire discussion of these claim elements in UII's Petition is on pages 11 (for claim 1), 18 (for claim 9), and 24-25 of the Petition, and is identical for each claim where this limitation appears. In each case, UII cites the following portions of the specification of Applegate:

- Abstract
- Fig. 5
- Fig. 6
- 6:10-14
- 11:31-38
- 14:43-54

116. Other than a cursory assertion by UII that Applegate discloses the claim limitation, I found no discussion in this section of the Petition explaining UII's view as to how this claim element is met. I reviewed each of the portions of

Applegate cited by UII, and in my opinion, none of them discloses the claimed increment counter command. I will discuss each of these citations individually.

117. Abstract of Applegate: UII cites the following passage from the Abstract:

*After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, therefore providing a permanent record on the process cartridge of a certain amount of toner usage.”*

118. This passage says nothing about commands or communication protocols between the processing device and the memory unit at all, much less the specific format of a command received by the memory unit from the processing device. This quoted sentence simply states that as the end result of a process, one of the bits of the EPROM memory device is irreversibly burned, but does not specify what causes that result.

119. Column 6, lines 10-14 of Applegate is identical to the passage quoted above in the Abstract except for the addition of the words “in the present invention.” Therefore, the same analysis applies.

120. Fig. 5 and column 11, lines 31-38 of Applegate: I previously discussed this figure and the supporting description regarding the “increment counter” limitation, and the same analysis applies. As I discussed previously, this figure and the supporting description merely describe the physical hardware characteristics of the interface between the printer and the cartridge and say nothing about communication protocols or particular commands. Therefore, in my opinion, this figure and passage do not teach the claim element.

121. Fig. 6 of Applegate: I previously discussed this figure and the supporting description regarding the “increment counter” limitation, and the same analysis applies. As I discussed previously, Fig. 6 is just an illustration of the structure of the memory. Fig. 6 does not say anything about the structure of commands that might be received by the memory, including either any increment counter command or any punch out bit command. Therefore, in my opinion, Fig. 6 of Applegate does not teach the claim limitation.

122. Column 14, lines 43-54 of Applegate: This cited passage reads as follows:

*The main portion of memory elements of EPROM 144 comprises the 1024 bits of non-volatile memory elements 180 that are initially set to a Logic 1 value, and which can be irreversibly cleared to a Logic 0 on a bit-by-bit basis. As discussed above, these 1024 bits are logically divided into four 32-bit “pages.” Each of the logical pages of this set of EPROM memory elements 180 can be physically write-protected by circuitry that falls within the function block 186 as depicted on FIG. 6. Once a page has been write-protected, none of its bits can be burned thereafter, and their values at that point are permanently set as either Logic 1 or Logic 0.*

123. This disclosure in Applegate provides a general description of the structure of the memory, which is also shown in Fig. 6. However, like Fig. 6, this

paragraph does not say anything about the structure of commands that might be received by the memory. At most, this passage describes the capability of specific pages in memory to be irreversibly burned. However, it also does not describe any command received by a memory unit from the processing device to punch out a bit. Therefore, in my opinion, this passage does not teach the claim element.

124. [not used]

125. [not used]

126. [not used].

**3. Applegate does not teach “processing the command at the one or more memory modules”**

127. Each independent claim in the '786 Patent requires “processing the command at the one or more memory modules.” Claims 2-8 and 10-15 depend from claims 1 and 9 and therefore incorporate the same limitation. In my opinion, UII’s Petition does not show that Applegate meets this limitation.

128. As I discussed previously, the '786 Patent teaches (e.g. at Fig. 1B) that the memory module receives commands from the processing device and processes those commands. In my opinion, Applegate does not teach any such

processing. The processing device in Applegate simply sends values to be stored in the memory module, without any teaching of processing commands on the side of the memory module. For example, UII relies on Fig. 9 as disclosing the claimed “processing the command at the one or more memory modules.” However, in my opinion, Fig. 9 refers to processing steps performed by the processor on the printer itself (that is, the engine controller 160 shown on the printer side on the left side of Fig. 5), and there is no processor shown on the memory module itself (see Fig. 6) capable of executing the steps shown in the flowchart. The only references to the memory module (that is, to the EPROM) in Fig. 9 are places where the processor on the printer simply writes a certain value (e.g. cycle count or bucket level) directly to the EPROM, but there is no teaching of processing these commands by the memory module.

**C. Ground 2: Claims 5 and 15 are not obvious over Applegate in view of Bruce**

129. In my opinion, claims 5 and 15 are not obvious over Applegate in view of Bruce. Claims 5 and 15 are dependent claims which depend from claims 1 and 9, respectively. I have been informed by counsel that a dependent claim

incorporates all of the limitations of the independent claim that it depends from.

The Petition (at 27-28) relies on and incorporates by reference its discussion of Applegate from Ground 1 regarding the limitations of the independent claims.

Because the Petition has failed to show that Applegate anticipates independent claims 1 and 9 for the reasons that I discussed above regarding Ground 1, it has also failed to show that the same limitations as incorporated into claims 5 and 15 are obvious.

130. UII does not argue that Bruce teaches the limitations discussed above in the independent claims which are not taught by Applegate, including an increment counter command, punch out bit command, a command comprising both of these, and processing the command at the one or more memory modules. In my opinion, there are no teachings in Bruce which fix these deficiencies.

131. It is also my opinion that a person of ordinary skill in the art would not have combined Applegate and Bruce. First, I disagree with the explanation provided by the Petition that because “both Applegate and Bruce deal with integrated circuits comprising memory cells,” a person of ordinary skill in the art “would be motivated to combine Bruce’s improved memory handling techniques

in order to improve the memory capabilities of the printer cartridges disclosed in Applegate.” Neither the Petition nor its expert Dr. Direen explains how the separate busy signal line taught by Bruce would supposedly improve the system of Applegate, and I am not aware of any based on my review of both references and my experience in the industry. Moreover, it is my opinion that neither the Petition nor Dr. Direen have explained any reason why a person of ordinary skill in the art would have been motivated to make such a combination at the time of the invention (as opposed to in hindsight), and no such reason exists.

132. I further note that Applegate and Bruce relate to different types of systems. Applegate specifically describes communication protocols for use in (for example) printers. Bruce is designed for an expandable flash memory system, and the specific architecture that Bruce teaches including a separate “busy” line is designed for that specific type of expandable flash memory system. In particular, having a separate busy line facilitates the addition of additional memory chips or banks of such chips. Based on my reading of the two different systems in Applegate and Bruce, I do not see how a person of ordinary skill in the art would be guided by the different teachings on different techniques in Applegate and

Bruce to combine Applegate and Bruce as suggested in the UII's petition. I reviewed UII's Petition and I found no analyses or explanations within the Petition as to how Applegate and Bruce would be combined.

## **VIII. ANALYSIS OF INVALIDITY GROUNDS ASSERTED BY UII PETITION AGAINST '193 PATENT**

### **A. Summary of Grounds Asserted by UII.**

133. I understand that UII has asserted in its Petitions the following grounds of invalidity against the '193 Patent:

- Ground 1: Anticipation by Applegate
  - Claims 1-8 and 10-15
- Ground 2: Obviousness over Applegate and Hama
  - Claims 5, 6, 13, and 15
- Ground 3: Obviousness over Applegate and Blood
  - Claims 5, 6, 13, and 15
- Ground 4: Obviousness over Applegate, Blood, and the I<sup>2</sup>C Specification
  - Claims 25 and 26

134. In my opinion, none of these Challenged Claims are invalid as being anticipated or obvious based on the grounds of invalidity asserted by UII.

**B. Ground 1: Applegate does not anticipate any claims of the '193 Patent**

**1. Applegate does not teach “a command... for instructing the memory module to punch out at least one bit of at least one specified bit field within the memory module”**

135. Each of independent claims 1 and 10 contains a claim limitation requiring that the memory module “receives” or performs the step of “receiving” a command which instructs the memory module to “punch out at least one bit of at least one specified bit field within the memory module.” Claims 2-9 and 11-16 depend from these claims and therefore incorporate the same limitation. UII’s very brief arguments in the 1381 Petition regarding the ’193 Patent are identical to those that it makes regarding the corresponding limitation in the 1378 Petition regarding the ’786 Patent, and cite the exact same portions of the specification of Applegate. *See* 1381 Petition at 12-13, 19-20. Therefore, my opinions discussed above as to why UII has failed to show that Applegate teaches the similar claim limitation with regard to the ’786 Patent also apply to these claim limitations in the ’193 Patent.

In my opinion, UII has failed to show that these claim limitations are taught by Applegate.

**2. Applegate does not teach “processing the command at the memory module” or “wherein the memory module... processes the at least one command”**

136. Each of independent claims 1 and 10 of the '193 Patent contains a limitation requiring that the memory module “processes the at least one command” or performs the step of “processing the command at the memory module.” Claims 2-9 and 11-16 depend from these claims and therefore incorporate the same limitation. UII’s very brief arguments in the 1381 Petition regarding the '193 Patent are identical to those that it makes regarding the corresponding limitation in the 1378 Petition regarding the '786 Patent, and cite the exact same portions of the specification of Applegate. *See* 1381 Petition at 13-15, 21. Therefore, my opinions discussed above as to why UII has failed to show that Applegate teaches the similar claim limitation with regard to the '786 Patent also apply to these claim limitations in the '193 Patent. In my opinion, UII has failed to show that these claim limitations are taught by Applegate.

**3. Applegate does not teach a command which comprises “incrementing the [non-volatile] counter by an amount specified in the [at least one] command”**

137. Claim 5 requires a second command which is “operable to instruct the memory module to increment a non-volatile counter therein,” while claim 15 requires that “the memory module processes the at least one command by incrementing the non-volatile counter by an amount specified in the at least one command.” UII’s very brief arguments in the 1381 Petition regarding the ’193 Patent are identical to those that it makes regarding the corresponding limitation in the 1378 Petition regarding the ’786 Patent, and cite the exact same portions of the specification of Applegate. *See* 1381 Petition at 13-15, 21. Therefore, my opinions discussed above as to why UII has failed to show that Applegate teaches the similar claim limitation with regard to the ’786 Patent also apply to these claim limitations in the ’193 Patent. In my opinion, UII has failed to show that these claim limitations are taught by Applegate.

**C. Ground 2: Applegate and Hama**

138. UII relies on a combination of Applegate and Hama for dependent claims 5, 6, 13, and 15, each of which requires a command to increment a counter.

In my opinion, UII has not shown that any of these claims are obvious over the combination of Applegate and Hama.

139. First, UII has not shown that these claims are obvious because it has not shown that Applegate teaches or suggests every element of the claims that these claims depend from. Claims 5 and 6 depend from claim 1, while claims 13 and 15 depend from claim 10. For these elements, UII just relies on Applegate for the elements of the independent claims. *See* 1381 Petition at 26-29. Therefore, because UII has failed to show that Applegate teaches or anticipates all of the elements of the independent claims, it has not shown that the dependent claims or obvious. UII does not argue that Hama teaches any element from these independent claims that is missing from Applegate, and in my opinion, there is no reason that a person of ordinary skill in the art would find that Hama teaches any element required by the claims that is missing from Applegate.

140. Second, UII has not shown why a person of ordinary skill in the art would have combined Applegate and Hama. UII asserts that “a skilled artisan would be motivated to combine these references as they each disclose methods for tracking toner in printer cartridges by using non-volatile memories associated with

the respective printer cartridges.” *See* 1381 Petition at 26. I disagree. In my opinion, the mere fact that references are in the same field or relate to the same type of device, by itself, would not give a person of ordinary skill in the art a reason to borrow elements from one reference to alter the other. In my opinion, there is no explanation either in the 1381 Petition or in the Direen Declaration why a person of ordinary skill in the art would import any teaching from Hama to either fix any problem with Applegate or improve the system taught by Applegate, and I am not aware of any such reason.

141. Third, Hama does not even teach the elements that UII cites it for. For example, UII cites Hama at column 22, lines 15-18 for the increment counter command. *See* 1381 Petition at 27. However, the cited passage simply says that the value of remaining toner amount is updated. Updating a value in memory does not imply a command to increment a counter. For example, the new value can simply be written to memory without any instruction to increment a counter at all. Therefore, in my opinion, UII has not shown that these elements are obvious over the combination of Applegate and Hama.

**D. Ground 3: Applegate and Blood**

142. UII's Petition for IPR of the '193 Patent under Case No. IPR2019-01381 ("the 1381 Petition") relies on a proposed combination of Applegate and Blood to challenge claims 9 and 16-37 of the '193 Patent. In my opinion, the 1381 Petition does not show that these claims are obvious at least because (1) these claims contain the same elements which are missing from Applegate in claims 1-9 and 10-15, and Blood also does not teach these elements; (2) a person of ordinary skill in the art would not have combined these references, and (3) Blood does not teach "upon encountering an error condition... limiting voltages on a first interface signal line of the memory module to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state."

**1. Blood does not remedy the deficiencies of Applegate**

143. Of the '193 Patent claims challenged based on the combination of Applegate and Blood, Claims 9 and 16 depend from claims 1 and 10, respectively, while independent claims 17 and 30 also contain limitations requiring a command to punch out a specified bit field and the memory module processing the command:

Claim	Limitation
17	<p>wherein the <b>command is indicative of usage of toner or ink</b> in a consumable item for an imaging device and instructs the memory module to punch out at least one memory cell in at least one <b>specified bit field</b> within the memory module indicative of the usage of toner or ink,</p> <p>following reception of the command, the memory module <b>processes the at least one command</b></p>
30	<p>wherein the <b>command pertains to usage of toner or ink</b> in a consumable item for an imaging device for instructing the memory module to punch out at least one bit of at least one <b>specified bit field</b> within the memory module to indicate the usage of toner or ink,</p> <p>and wherein the <b>memory module processes the command following the reception thereof</b></p>

144. The 1381 Petition relies on Applegate for these limitations, using the same arguments that it makes for Ground 1. In my opinion, because each claim challenged under the combination of Applegate and Blood contains the same limitations that UII failed to show in Applegate, UII failed to show these limitations for the combination of Applegate and Blood as well. Neither UII nor Dr. Direen argued that Blood teaches these elements, and in my opinion, Blood does not teach any of these elements. Specifically, Blood is simply a generic

duplex signaling reference and says nothing about commands to punch out a specified bit field of a memory, nor an increment counter command, nor processing commands at a memory module.

**2. A person of ordinary skill in the art would not have combined Applegate and Blood**

145. I have been informed by counsel that it is the Petitioner's burden, if relying on a combination of two or more references under § 103, to show that a person of ordinary skill in the art would have been motivated to combine the references. In my opinion, UII has failed to show why a person of ordinary skill in the art would have combined Applegate and Blood.

146. The only statement in the 1381 Petition explaining the motivation to combine is a statement at p. 29 that “[a] skilled artisan would be motivated to combine Blood’s teachings with Applegate’s in order to facility [sic] more efficient communication among the integrated circuits used in printing apparatuses.” I disagree. In my, this statement does not articulate in any way how the purported nation of Applegate and Blood would supposedly make the communication between integrated circuits used in printing apparatuses more efficient, nor does it

even articulate how the proposed combination would work. Without some explanation of how the proposed combination will work, it is difficult to understand or evaluate what benefit the combination of references would supposedly have. Nevertheless, neither the 1381 Petition nor Dr. Direen explains how the proposed combination would work or how that combination would somehow result more efficient communication, and in my opinion, there is no reason for a person of ordinary skill in the art to believe that combining these two references would improve communication. Even assuming that in hindsight these two references could be combined and would provide some benefits by being combined, in my opinion, there is no reason that a person of ordinary skill in the arts will have seen such a benefit and sought to combine them at the time of the inventions claimed in the challenged patents. In my opinion, there is nothing in Applegate, whether in the reference itself or in the nature of the problem that Applegate was trying to solve, that would have indicated to a person of ordinary skill in the art at the time of the alleged invention that they should look to Blood to improve the system of Applegate.

**3. Petitioner’s proposed combination does not teach “upon encountering an error condition... limiting voltages on a first interface signal line of the memory module to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state”**

147. Even if a person of ordinary skill in the art would have combined Applegate and Blood in the manner argued by the 1381 Petition, and in my opinion, they were not, the resulting combination still does not teach or suggest claim. Specifically, the 1381 Petition relies on Blood for additional limitations in each of dependent claims 9 and 16 and independent claims 17 and 30 contains a limitation requiring a memory module to limit the voltage on a first interface signal line to an intermediate voltage (that is, a voltage lower than a binary “1” state and higher than a binary “0” state) in response to either a busy condition or an error condition. For example, claim 9 recites “limiting voltages on a first interface signal line of the memory module to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state.” In contrast, as I explained above at Paragraph 70, the device connected to the signal line in both Applegate and Blood

is a binary device that only generates a binary signal carrying either a high level or a low level and does not “limit” any output signal to an intermediate voltage between the high and low levels. I reproduce Claims 16, 17, and 30 below which recite a similar limitation as in Claim 9:

Claim	Element
9	upon encountering an <b>error condition</b> while processing the command, <b>limiting voltages</b> on a first interface signal line of the memory module to be <b>no more than an intermediate voltage</b> greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state
16	upon encountering an <b>error condition</b> while processing the at least one command, <b>limiting voltages</b> on the first interface signal line to be <b>no more than an intermediate voltage</b> greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state for a period of time to indicate an occurrence of the error condition
17	upon encountering an <b>error condition</b> while processing the command, <b>limiting a voltage</b> on a first signal line of the plurality of signal lines to be <b>no more than an intermediate voltage</b> greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state for a period of time to indicate an occurrence of the error condition

30	<b>a voltage</b> on a first signal line of the plurality of signal lines is <b>limited</b> for a period of time by the memory module to be <b>no more than an intermediate voltage</b> greater than voltages corresponding to a binary zero value and less than voltages corresponding to a binary one value, for <b>indicating by the memory module one of a busy condition and an error condition</b>
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148. In my opinion, Blood does not teach these limitations. As I explained in my discussion of Blood, Blood does not teach limiting a voltage to an intermediate value in any way. Rather, the “intermediate” value of Blood simply results from the addition of the two signals. The claims require that one station limits the voltage to an intermediate value, but Blood teaches that each of the stations performs separate operations of addition (of its own signal to the voltage on the signal line), and subtraction (subtracting its own output from the combined voltage on the signal line), but as I explained in detail previously in this Declaration, neither station in Blood performs the “limiting” function required by the claims; that is, holding the line to less than or equal to a specified intermediate voltage.

149. The 1381 Petition also does not argue that Applegate teaches these limitations, and in my opinion, Applegate does not teach these limitations.

Specifically, there is nothing in Applegate about limiting any voltage to an intermediate value.

**4. Blood does not teach limiting voltage based on an error condition or busy condition**

150. In my opinion, both the 1381 Petition and Dr. Direen have failed to show that either Blood or the combination of Blood and Applegate teaches that the claimed limiting of a voltage to an intermediate voltage occurs upon encountering an error condition or a busy condition. It is my opinion that neither Blood nor the combination of Blood and Applegate teaches limiting voltage based on an error condition or a busy condition.

151. The 1381 Petition regarding the '193 Patent simply asserts that the intermediate voltage state taught by Blood "occurs during an error condition," but provides no explanation or evidence to support this statement, and in my opinion, there is no teaching in Blood which supports this statement. The 1381 Petition cites Figure 3 of Blood and 5:53-55, but in my opinion, neither the figure or the passage says anything about busy or error conditions. Figure 3 of Blood, which I have discussed previously, merely shows the resulting voltages from signals from two

stations being added together, and it is not about busy or error conditions, or signaling those conditions, anyway. The cited passage at 5:53-55 says in its entirety that “When both transmitters send, then the voltage level at the transmission line 11 shifts between three levels, as illustrated in Fig. 3; O.” in my opinion, this passage is also completely irrelevant to busy or error conditions.

152. In my opinion, there is nothing else in Blood, whether or not cited by the 1381 Petition or Dr. Direen, which says anything about handling conditions such as busy or error conditions, and in particular there is nothing in one which describes claimed invention of signaling such a condition by limiting the voltage on a signal line to an intermediate value between the voltages that would otherwise be a binary “zero” and “one.” Based on my review of Blood, it is simply silent about either error or busy conditions. As I discussed previously, the intermediate value in Blood occurs whenever one of the two stations is transmitting a “one” and the other is transmitting a “zero,” which has nothing to do with signaling an error or busy condition.

153. Neither the 1381 Petition nor the Direen declaration cites anything from Applegate that teaches or suggests either limiting a voltage to signal

anything, or signaling a busy or error condition in any way, much less the specific claimed teaching of limiting a voltage to an intermediate value to signal a busy or error condition. In my opinion, there is no such teaching in Applegate.

154. I also disagree with the assertions by the Petitions and Dr. Direen that the limitations would have been obvious over the general knowledge of a person of ordinary skill in the art. At most, both the Petitions and Dr. Direen assert that either busy or error conditions of memory modules were known in the art, then assert in hindsight that it would be obvious to apply the duplexing methods of Blood to communication of busy or error conditions. I disagree. In my opinion, the mere fact that a particular problem or need may have been known does not mean that a person of ordinary skill in the art would have known to solve that problem using the claimed inventions. Moreover, the configuration of an interface to communicate to a memory or multiple memories over a bus involves non-trivial engineering challenges, and in my view it is unreasonable to simply say that a person of ordinary skill in the art would have arrived at a particular configuration simply because they may have wanted to communicate busy or error conditions somehow.

**E. Ground 4: Applegate, Blood, and I<sup>2</sup>C Specification**

155. UII's 1381 Petition for IPR of the '193 Patent further relies on a combination with the I<sup>2</sup>C Specification in addition to Applegate and Blood to challenge claims 25 and 26. In my opinion, the 1381 Petition does not show that these claims were obvious at least because these claims depend indirectly from claim 17, and claim 17 is not obvious for the reasons that I discussed earlier. UII only cites the I<sup>2</sup>C Specification for the teaching of a second input signal comprising a clock signal on a second signal line. In my opinion, the I<sup>2</sup>C Specification does not provide any of the limitations of claim 17 that were missing from UII's proposed prior art combination, nor does the I<sup>2</sup>C Specification explain any additional reason why a person of ordinary skill in the art would have combined Applegate and Blood.

156. In my opinion, a person of ordinary skill in the art would not have combined the I<sup>2</sup>C Specification with Applegate and Blood, nor does the 1381 Petition or Dr. Direen explain why a person of ordinary skill in the art would have done so. The 1381 Petition on the '193 Patent simply says that "a skilled artisan would also be motivated to combine the teachings of I<sup>2</sup>C Spec [sic], as the I<sup>2</sup>C

Protocol is the standard protocol for implementing communication on an integrated circuit.” This statement does not explain any reason why a person of ordinary skill in the art would be motivated to combine the I<sup>2</sup>C Specification *with* Applegate and Blood. The fact that I<sup>2</sup>C Specification is a standard protocol does not, in my opinion, mean that a person of ordinary skill in the art would have combined its teachings with anything in Applegate, Blood, or both. Indeed, in my opinion the I<sup>2</sup>C Specification would not have been combined with Blood precisely because the duplexing methods of Blood are inconsistent with the standardized protocol of the I<sup>2</sup>C Specification. Specifically, the I<sup>2</sup>C Specification teaches a standard protocol based only on binary voltages and one device communicating at a time, so the duplexing using intermediate voltages taught by Blood would not only be inconsistent with the I<sup>2</sup>C Specification’s standardized approach, but devices on a bus designed to comply with the I<sup>2</sup>C Specification would not be able to recognize such communications. Simply put, two devices talking at the same time using three voltages rather than two would be incomprehensible to an I<sup>2</sup>C device.

**IX. ANALYSIS OF INVALIDITY GROUNDS ASSERTED  
AGAINST '591 PATENT**

**A. Grounds asserted by UII**

157. I understand that UII's Petition for IPR under Case No. IPR2019-01378 on Patent No. 9,245,591 ("the 1378 Petition") alleges that Claims 1-16 of the '591 Patent are invalid over the combination of Blood, the I<sup>2</sup>C Specification, and Bruce.

**B. Ground 1: Blood, I<sup>2</sup>C Specification, and Bruce**

158. UII's 1378 Petition relies on the combination of Blood, the I<sup>2</sup>C Specification, and Bruce for its sole invalidity challenge against claims 1-16 of the '591 Patent. In my opinion, none of these claims are obvious over the combination of Blood, Bruce, and the I<sup>2</sup>C Specification.

159. Although the exact language of the claims that UII challenges based on Blood, the I<sup>2</sup>C Specification, and Bruce varies, there are a number of common reasons that I saw why the combination of Blood, the I<sup>2</sup>C Specification, and Bruce does not render any of these claims obvious. First, a person of ordinary skill in the art would not have combined these references. Second, neither any of these

references nor the combination of them teaches limiting (or changing) an upper voltage on a signal line to an intermediate voltage which is less than the normal upper voltage corresponding to a binary “one” and greater than the normal lower voltage corresponding to a binary “zero.” Third, the proposed combination does not teach limiting or changing such a voltage to indicate an error or busy condition. Fourth, the proposed combination does not teach indicating an error or busy condition by a memory module while simultaneously continuing to receive binary clock or data signals on the same line.

**1. A person of ordinary skill in the art would not have combined Blood, the I<sup>2</sup>C Specification, and Bruce**

160. It is my opinion both that UII has failed to show that a person of ordinary skill in the art would have combined Blood, the I<sup>2</sup>C Specification, and Bruce, and that a person of ordinary skill in the art in fact would not have been motivated to combine these references because of technical incompatibilities between them.

161. I will begin with the reasons that in my opinion, UII has not given a convincing reason that a person of ordinary skill in the art would have combined

these references. UII argues, for example in the 1378 Petition at 9, that (regarding the disclosures of Blood, the I<sup>2</sup>C Specification, and Bruce) a person of ordinary skill in the arts “would have looked to combine these disclosures to improve the performance and capabilities of these memory devices.” However, in my opinion, this statement is not supported by any explanation of how the combination of these disclosures would “improve the performance and capabilities of these memory devices” for me to evaluate. Moreover, I do not see any reason why a person of ordinary skill in the art at the time of the inventions claimed in the Lexmark inventions would expect the combination of Blood, the I<sup>2</sup>C Specification, and Bruce to improve the performance of a memory device.

162. Specifically, neither the 1378 Petition nor Dr. Direen’s declaration explains any reason why there is any problem or need presented by any of these three very different references that would lead a person of ordinary skill in the art to seek to modify that reference by incorporating teachings from any of the others. In my opinion, there is no reason that a person of ordinary skill in the art would have looked to the single-line duplexing of Blood to fix any problem with or improve the standardized system described by the I<sup>2</sup>C Specification, or vice versa.

163. I understand that UII relies on Bruce because it teaches a “busy” signal, but in my opinion there is no reason why a person of ordinary skill in the art would look to either Blood or the I<sup>2</sup>C Specification to fix any issue with the busy signal taught by Bruce. Bruce is designed for an expandable flash memory system, and the specific architecture that Bruce teaches including a separate “busy” line is designed for that specific type of expandable flash memory system. In particular, having a separate busy line facilitates the addition of additional memory chips or banks of such chips. There is no reason, either explained in the 1378 Petition or in Dr. Direen’s declaration or that I am otherwise aware of in the art, why a person of ordinary skill in the art would want to replace this specific architecture in Bruce either with an I<sup>2</sup>C bus or with the duplexing methods taught by Blood. Moreover, attempting to duplex this busy signal onto a common flash bus would essentially negate the core feature of the “busy” line in Bruce’s design scheme.

164. It is further my opinion that the proposed combination would be impractical due to technical incompatibilities between the references, particularly between Blood and the I<sup>2</sup>C Specification. As I explained previously, in my opinion the I<sup>2</sup>C Specification would not have been combined with Blood precisely

because the duplexing methods of Blood are inconsistent with the standardized protocol of the I<sup>2</sup>C Specification. Specifically, the I<sup>2</sup>C Specification teaches a standard protocol based only on binary voltages and one device communicating at a time, so the duplexing using intermediate voltages taught by Blood would not only be inconsistent with the I<sup>2</sup>C Specification's standardized approach, but devices on a bus designed to comply with the I<sup>2</sup>C Specification would not be able to recognize such communications. Simply put, two devices talking at the same time using three voltages rather than two would be incomprehensible to an I<sup>2</sup>C device.

**2. The combination of Blood, I2C Specification, and Bruce does not teach “limiting” or “changing” an upper voltage to an intermediate voltage**

165. Several of the Challenged Claims include claim limitations which require the memory module to “limit” or otherwise change the upper voltage on a first signal line to an intermediate voltage. I will use claim 1 as an example of this claim limitation:

the memory module configured such that upon encountering a first condition while processing a command received by the memory module, the memory

module **limits a voltage on a first signal line of the plurality of signal lines** for a period of time to be **no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state** for a period of time for indicating an occurrence of the first condition.

166. In my opinion, the proposed combination of Blood, the I<sup>2</sup>C Specification, and Bruce does not teach such claim limitations. I understand that the 1378 Petition and Direen Declaration generally rely on Blood, particularly Figure 3 of Blood, for the intermediate voltage limiting claim limitations. In my opinion, this is incorrect. The claim limitations at issue require more than just that the transmission line somehow uses three voltage levels, one of which is between the other two. These claims require a memory module to specifically limit the upper voltage to a level that is greater than a binary zero state and lower than a binary one state. Blood simply teaches an addition of the voltages from the two transmitters on the signal line, not that a memory module “limits” the voltage of the resulting signal. In my opinion, UII has not explained in any of its Petitions which station shown in Fig. 3 of Blood, or the text of Blood at 5:53-55, limits the

other or how it limits the other station. Each station performs an addition function (adding its own signal to the combined voltage on the line) and a subtraction function (subtracting its own signal from the combined voltage to identify the voltage from the other station), but nowhere in Blood is there any teaching that either station limits the voltage to a value less than or equal to an intermediate voltage.

167. In my opinion, UII has also failed to demonstrate that claims 7 and 11 are obvious for similar reasons.

168. In my opinion, neither Bruce nor the I<sup>2</sup>C Specification fixes this deficiency in Blood, and it does not appear that either UII or Dr. Direen argues that they do. As I discussed at length previously, I<sup>2</sup>C Specification teaches a standard protocol which communicates using only two binary values, and limiting to an intermediate value would be incompatible with that standard. As for Bruce, it teaches signaling a busy condition of a memory over a separate wire, and says nothing about communicating using intermediate values.

**3. The combination of Blood, I2C Specification, and Bruce does not teach limiting voltage based on an error condition or a busy condition**

169. Even if a person of ordinary skill in the art would have combined Blood, Bruce, and the I2C Specification, which they would not have for the reasons that I explained previously, it is also my opinion that the proposed combination does not teach limiting a voltage to an intermediate voltage upon encountering an error condition or a busy condition. I will again use claim 1 as an example of this claim limitation:

the memory module configured such that **upon encountering a first condition while processing a command** received by the memory module, the memory module **limits a voltage** on a first signal line of the plurality of signal lines for a period of time to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state for a period of time **for indicating an occurrence of the first condition...**

wherein the first signal comprises a clock signal and the first condition comprises a **busy condition**.

170. Several of the challenged claims (such as Claim 2) contain similar limitations requiring that the memory device limits the voltage on a second signal line to an intermediate value to indicate an “error” condition. In my opinion, these claim limitations are not met for either a “busy” condition or an “error” condition.

171. Not only does Blood not teach “limiting” a voltage to an intermediate value for the reasons that I discussed previously, there is also no indication that the intermediate voltage taught by Blood (which is actually simply the result of two signals being added together) is ever used to indicate a busy or error condition. Nor would combining Blood, Bruce, and the I2C Specification result in such an intermediate voltage being used to indicate a busy or error condition.

172. UII asserts several times in its Petitions (e.g. in the Petition on the ’193 Patent at 31) something to the effect that “an error condition signal on the memory going low will cause the line 11 voltage to go to an intermediate voltage halfway between the high and low voltages on line 11 when the processor side of the line is in the high state.” In my opinion, neither Blood nor any of the other references cited supports this statement. Blood says nothing about error signals. UII here appears to be making a series of assumptions without justifying any of

them. UII first assumes a hypothetical scenario in which a specific combination of devices is used as the first and second stations described in Blood. In that hypothetical, UII then assumes that one of the stations is sending a clock signal (about which Blood is silent). UII assumes again that the other station needs to signal an error (or a busy condition), and on top of all of these assumptions, it piles the last assumption that a person of ordinary skill in the art would choose to have the other station signal the error (or busy condition) by limiting the voltage to an intermediate value. In my opinion, UII fails to provide any justification for *any* of this series of assumptions, much less the combination of them.

173. In my opinion, the question is not merely whether any of these references somehow teaches a busy or error condition or whether busy or error conditions in memory modules were known in the art, but whether the teachings of this particular combination would lead a person of ordinary skill in the art to utilize the particular inventive method claimed by the Challenged Patents to indicate a busy or error condition. In my opinion, UII has provided no reason or evidence why a person of ordinary skill in the art would do that in view of the prior art references. In other words, in my opinion, UII is simply assuming the inventive

insight behind the challenged patents rather than showing why the inventive features would have been obvious at the time of the invention.

174. Even if a POSITA were to combine the teachings of these three references, there is no reason that it would necessarily result in the claimed invention. Even using the duplexing method of Blood to communicate a busy condition would simply result in the signal for such a condition being added to the total voltage on the line, not limiting the voltage as claimed.

175. The I<sup>2</sup>C Specification and Bruce also teach away from using the claimed invention to signal a busy condition. The I<sup>2</sup>C Specification teaches that devices communicate one at a time, or in some cases simply hold the clock line down to block *any* further communication until that device is ready for further communication. The natural implication of the teachings of the I<sup>2</sup>C Specification is that a device needing to send a busy or error signal would send such a signal in the same manner, not by holding the line to an intermediate value that other I<sup>2</sup>C Specification compliant devices would not even recognize. As for Bruce, Bruce already teaches a method of signaling a busy status over a separate busy line, so

the teachings of Bruce would lead a person of ordinary skill in the art away from signaling such a status on a line dedicated to other signals.

**4. The combination of Blood, I2C Specification, and Bruce does not teach that the memory module simultaneously indicates the occurrence of a busy condition by limiting the voltage on the first signal line while receiving a clock signal on the same line**

176. Several asserted claims of the Challenged Patents require that a memory module must receive a clock signal and indicate the existence of a busy condition by limiting the voltage on the signal line to an intermediate voltage, while at the same time continuing to receive the clock signal. Claim 1 is an example:

Claim	Element
1	wherein the memory module is configured <b>to receive a first signal on the first signal line</b> , and during the period of time in which the memory modules limits a voltage on the first signal line of the plurality of signal lines to be no more than the intermediate voltage... the intermediate voltage on the first signal line is interpreted by the memory module as a binary one state of the first signal such that during the period of time <b>the memory module receives the first signal</b> on the first signal line while <b>at the same time</b> the memory module <b>communicates the occurrence of the first condition</b> on the first signal line to the processing device,

wherein the first signal comprises a <b>clock signal</b> and the first condition comprises a <b>busy condition</b> .
--

177. Other claims contain a similar limitation requiring that an error message is communicated on a second signal line, while the memory module continues to receive data on that second signal line. Claim 2 is an example of such a claim.

178. In my opinion, the combination of Blood, I<sup>2</sup>C Specification and Bruce does not teach such limitations, and UII has not shown that it does. For example, UII simply asserts (at 14) that “it is well-known for a device to send a busy condition in response to a signal on the clock line” based on the I<sup>2</sup>C Specification. However, in my opinion, simply adding a clock signal does not provide any reason why a memory device would simultaneously communicate a busy condition while continuing to receive clock signals. As I discussed previously, the I<sup>2</sup>C Specification teaches that only one device at a time may communicate. Sending a busy signal while simultaneously receiving clock signals over the same line is contradictory to this teaching of the I<sup>2</sup>C Specification. The proposed modification

would be fundamentally incompatible with the teachings of the I<sup>2</sup>C Specification and Blood, and UII fails to explain how it would reconcile such teachings.

179. Therefore, in my opinion, this claim element is not taught by the combination of the I<sup>2</sup>C Specification, Blood, and Bruce.

## **X. CONCLUSION**

180. For the foregoing reasons, it is my opinion that the Challenged Claims of the '786 Patent, '193 Patent, and '591 Patent are not invalid for the reasons asserted by UII.

Declaration of Jeffrey J. Folkins, Ph.D.  
Case No. IPR2019-01378 on Patent No. 9,245,591 B2  
Case No. IPR2019-01380 on Patent No. 7,844,786 B2  
Case No. IPR2019-01381 on Patent No. 8,966,193 B2  
Ex. 2001

181. I hereby declare that all the statements made in this Declaration are of my own knowledge and true; that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under the penalty of perjury that all statements made in this Declaration are true and correct to the best of my knowledge and belief.

Executed on November 5, 2019 (Date)

By Jeff J Folk (Signature)

Jeffrey J. Folkins, Ph.D.

ROCHESTER, N.Y.

# APPENDIX A

# Jeffrey J. Folkins

292 Weymouth Dr.  
Rochester, NY 14625  
jfolkins1@gmail.com  
585-739-9195

## Summary

Research Fellow and research Program Manager in the areas of inkjet and electrophotographic printing at Xerox Corporation (retired).

Received a B.S. in 1976 from Harvey Mudd College and a Ph.D. in 1981 in Solid State Physics from the University of Pennsylvania, whereupon joined Xerox Corporation's R&D division, eventually becoming a Research Fellow. Early work at Xerox centered on electrophotographic development subsystems, process controls and color systems ultimately incorporated into multiple Xerox products. Following this, led a team that integrated the components and systems for the single pass color electrophotographic process that ultimately led to a new generation of Xerox color products, including the flagship iGen Digital Presses.

Since year 2000, has led teams developing unique experimental inkjet products and product architectures. Served as the initial Technical Program Manager of the Xerox ColorQube solid ink Inkjet printer. Subsequently worked as the initial Program Manager for the Xerox CiPress Production Inkjet Printer. Additionally, led teams on various experimental inkjet related projects. Led R&D's production inkjet competitive benchmarking efforts.

Technologies developed over the years have been included in tens of Xerox products and product families with an excellent record of 153 U.S. Patents.

Elected Fellow in the American Physical Society and is the 2007 recipient of the IS&T Society's Johann Gutenberg Prize as well as the 1986 Xerox President's award.

## Education

- Ph.D., 1981, Physics (experimental solid state)  
University of Pennsylvania, Philadelphia, Pennsylvania.  
Thesis: Critical Behavior in the Dipolar-coupled Ising Random Ferromagnet  $\text{LiTb}_p\text{Y}_{1-p}\text{F}_4$
- BS, 1976, Physics, Harvey Mudd College, Claremont, California

## Employment

**Xerox Corporation**, 1981–2015, Research Fellow (retired)

### **Inkjet Product Development:** (2000 – 2015)

- CiPress 500/325 Production Inkjet Continuous Feed Printer: Technical Program Manager and then Program Manager during the technology phase. Led team and developed architecture, concept and technology for high speed solid ink (“Waterless”) inkjet production printer. Delivered technology and prototypes to product delivery team.

- ColorQube 8570/8870: Enabled higher speeds by developing a modified high efficiency print process for incorporation in with product.
- ColorQube 9200 Series: Technical Program Manager during technology phase. Developed and delivered high speed solid ink intermediate transfer inkjet technology and prototypes to product delivery team.
- Program Manager for proprietary high quality intermediate transfer production printer prototype.
- System Integration Manager for proprietary Acoustic Ink inkjet printing program.
- R&D organization's production printing competitive benchmarking and assessment lead.

### **Electrophotographic Product Development** (1981 – 2000)

- iGen3 & Docutech HLC Color Production Printer:
  - Project leader of team that made the first “Image On Image” (IOI) color printer prototype that demonstrated the base technology for the future iGen3 and the Docutech HLC production printers
  - Project leader of team that developed Hybrid Scavengeless Development (HSD) critical to iGen3 / Docutech HLC, as well as Hybrid Jumping Development used in the DC265, DT120 and the Nuvera family
  - Developed many of the IOI and HSD functions/features used in iGen3, including: Split Recharge, Burst Mode, Dual Donor HSD, HSD Cleaning Cycles, HSD Setpoints, Wire Modules, AC Charge with Erase recharging systems, HSD air manifolds, Reversal black registration sensing, Split Pretransfer, Process controls with IOI, Limp-a-long modes, Multi-cycle diagnostics, Conditional mode asymmetric ID zone printing, Cross contamination bias modes, AC at cycleout for wire history.
- Developed “Mag Brush ESV” used in: Xerox 9900; 9500 retrofits; 5048 Family; 5028 Family
- Developed "CSDC" Toner Controller used in: Xerox 1025; 1038; & 5028 Families
- Co-developed Trickle Development used in: Xerox 5028 Family; 4850/4890; DC265; 8830; iGen3, Nuvera, Docutech HLC etc.
- Design of Twin Auger Crossmixer developer housing architecture used in: Xerox 5048, 5775. DC265, etc.

### **Assorted Process and Modeling**

- Modeling Studies: Toner layer voltages, Magnetic brush conductivity & developability, Ionographic blooming, “Trickle”, Process Controls, etc.
- Developed an “Integrated Parameter Management” methodology technology delivery process for managing/integrating CP's, C.S.'s, IOC's, etc
- DFLSS Green Belt Certification 2005

## **University of Pennsylvania**

Research Assistant, 1977-1981, Teaching Assistant, 1976-1977, Advisor: John Griffin

## **Lawrence Livermore Laboratories**

Summer Employment, 1975 & 1976,  
Hydrodynamics Division, Livermore, California. Supervisor: John Shaner  
Measured shock waves in a variety of dense materials

## **Radio KWOW AM 1600**

Radio Engineer, part time 1973-1976,  
South Mills and Olive, Pomona, California. Supervisor: Jon Wickstrom  
Weekend night operation of automated programming and technical maintenance

## **Radio KSPC FM 99.7**

Chief Engineer 1973-1974  
Pomona College's non-profit radio station  
FCC First Class Radiotelephone License 1973

## **Notable Awards & Honors**

- 1999 Elected Fellow in the American Physical Society
- 2007 IS&T's Johann Gutenberg Prize (Society for Imaging Science and Technology)
- 2013 R&D100 Product Award, R&D Magazine "High Speed Printer Without Water", one of the principle developers,
- Xerox Internal Awards:
  - 1986 Xerox Presidents Award
  - 2004 Xerox Greece Olympics Award
  - 1985 Individual Contributors Recognition Award for Excellence (RBG)
  - 1995 Excellence in Science and Technology Award
  - 1985 Team Recognition Award for Excellence (RBG)
  - 1994 CR&T Special Recognition Award
  - 1995 Excellence in Support of Research Award
  - 1996 Eagle Award
  - 1998 Eagle Award

## **Professional Associations**

- **American Physical Society (elected Fellow in 1999)** (life member)
- **Society for Imaging Science and Technology (IS&T)** (formerly)

## **Invited External Presentations** (not including contributed papers/presentations)

### ***Invited paper: Waterless Inkjet High Speed Printing***

IMI 19<sup>th</sup> Annual European Ink Jet Conference, Lisbon, Portugal, November 2011

### ***Invited paper: Solid Ink Printing Technology***

Japan Society of Colour Material, 7th IT Seminar, Tokyo, Japan, December 3, 2010

**Keynote Overview: Digital Imaging Technologies: Key Challenges**

CAMP Annual Technical Meeting  
The New York State Center for Advanced Materials Processing, Clarkson University  
May 12, 2005 at Canandaigua Inn on the Lake, Canandaigua, NY

**Interactive Panel on the future of Inkjet vs EP technologies**

2007 IS&T NIP Conference

**Edmonton Canada Product Announcement:**

**Innovation Behind the Docutech 100/120 and Phaser 8400**

Edmonton, Alberta, Canada  
March 16, 2004

**Issued Patents** (151 U.S patents.)

***A Development System Having a Bounded Electrical Bias***

Jeffrey J. Folkins  
U.S. #4,466,732 8/21/84

***A Control System for Regulating the Dispensing of Marking Particles in an Electrophotographic Printing Machine***

Jeffrey J. Folkins, Alfred M. Loeb, Henry R. Till, Shahid Haque  
U.S. #4,492,179 1/8/85

***A Development System Using Electrically Field Dependent Developer Material***

Jeffrey J. Folkins  
U.S. #4,565,438 1/21/86

***An Extended Life Development System***

Jeffrey J. Folkins, Cyril G. Edmunds & Steven C. Hart  
U.S. #4,614,165 9/30/86

***An Apparatus for Sensing the Presence of Toner Particles***

Jeffrey J. Folkins  
U.S. #4,611,900 9/16/86

***A Development System***

Jeffrey J. Folkins  
U.S. #4,603,961 8/5/86

***A Control System for an Electrophotographic Printing Machine***

Jeffrey J. Folkins  
U.S. #4,643,561 2/17/87

***Preview System for an Electrophotographic Printing Machine***

Jeffrey J. Folkins  
U.S. #4,740,814 4/26/88

***A Hybrid Control System for a Copier***

Jeffrey J. Folkins  
U.S. #4,786,924 11/22/88

***A Piecewise Development System***

Jeffrey J. Folkins  
U.S. #4,851,884 7/25/89

***Self-Biased Scorotron Grid Power Supply and Electrostatic Voltmeter Operable Therefrom***

Jeffrey J. Folkins  
U.S. #4,868,907 9/19/89

***Electrophotographic Device With a Bead Pickoff Arrangement***

Jeffrey J. Folkins and Morton Silverberg

U.S. #4,868,607 9/19/89  
***Automatic Color Separation System***  
Jeffrey J. Folkins, Robert N. Goren and James D. Rees  
U.S. #4,922,298 5/1/90  
***Resistive Nib Ionographic Imaging Head***  
Jeffrey J. Folkins (Name is misspelled on patent as Eolkins)  
U.S. #4,951,071 8/21/90  
***Electrode Wire Cleaning***  
Jeffrey J. Folkins  
U.S. #4,984,019 1/8/91  
***Developing Device with Dual Donor Rollers Including Electrically Biased Electrodes for Each Donor Roller***  
Jeffrey J. Folkins, Joseph G. Schram & Eric J. Schneider  
U.S. #5,032,872 7/16/91  
***Triboelectric Charge Measurement***  
Jeffrey J. Folkins  
U.S. #5,034,775 7/23/91  
***Development Apparatus Having a Transport Roll Rotating at Least Twice the Surface Velocity of a Donor Roll***  
Jeffrey J. Folkins and Joseph Schram  
U.S. #5,063,875 11/12/91  
***Highlight Color Copier***  
Jeffrey J. Folkins  
U.S. #5,089,847 2/18/92  
***Electrode Wire Contamination Prevention and Detection***  
Jeffrey J. Folkins & Samuel W. Ing  
U.S. #5,134,442 7/28/92  
***Fiber Cleaning System for a Development System***  
Jeffrey J. Folkins & Don B. Jugle  
U.S. #5,153,642 10/6/92  
***Development System Having Tensioned electrode Wires***  
Laurence Barker, Tom Behe, Dan Bray, James Davidson, Gerald Kryk, Jeffrey J. Folkins & Joseph Schram  
U.S. #5,153,647 10/6/92  
***Electrode Wire Mounting for Scavengeless Development***  
Gerald Thomas Lioy, Jeffrey Joseph Folkins & Thomas James Behe  
U.S. #5,153,648 10/6/92  
***Machine With removable Unit Having Two Element Electrical Connection***  
Ross E. Schroll and Jeffrey J. Folkins  
U.S. #5,177,529 1/5/93  
***Development Unit Having an Asymmetrically Biased Electrode Wires***  
Jeffrey J. Folkins  
U.S. #5,206,693 4/27/93  
***Method and Apparatus for Minimizing the Voltage Difference Between a Developed Electrostatic Image Area and a Latent Electrostatic Non-Developed Image***  
Dan Bray, Tom Behe & Jeffrey J. Folkins  
U.S. 5,241,356 8/31/93  
***Donor Roll for Scavengeless Development in a Xerographic Apparatus***  
Thomas J. Behe, Jeffrey J. Folkins, Joseph G. Schram, William H. Wayman, Gerald T. Lioy and Grace T. Brewington

U.S. 5,245,392      9/14/93  
***Contaminant Control for Scavengeless Development in a Xerographic Apparatus***  
Thomas J. Behe, Daniel M. Bray, Jeffrey J. Folkins, Gerald M. Kryk, Joseph G. Schram  
and Cyril Edmunds  
U.S. 5,253,016      10/12/93  
***Method and Apparatus for Correction of Blooming Artifacts in Ionographic  
Devices***  
Tracy E. Thieret, Jeffrey J. Folkins, Richard G. Stearns & William B. McDonald III  
U.S. 5,225,856      7/6/93  
***Method and Apparatus for Monitoring and Controlling a Toner Image Formation  
Process***  
Jeffrey Joseph Folkins and Cyril G. Edmunds  
U.S. 5,307,119      5/26/94  
***Mark Detection Circuit for an Electrographic Printing Machine***  
Fred F. Hubble III, James P. Martin, & Jeffrey J. Folkins  
U.S. 5,339,150      8/16/94  
***Proper Charging of Donor Roll in Hybrid Development***  
Jeffrey Joseph Folkins, Thomas James Behe, Joseph G. Schram  
U.S. 5,341,197      8/23/94  
***Charging System for Eliminating Edgebanding in an Electrostographic Printing  
Process***  
Jeffrey Joseph Folkins, Daniel M. Bray, Alexander J. Fioravanti, Keneth W. Pietrowski,  
Gerald Thomas Lioy & Thomas James Behe  
U.S. 5,365,317      11/15/94  
***Method and Apparatus for Measuring Photoreceptor Voltage Potential Using a  
Charging Device***  
Jeffrey Joseph Folkins  
U.S. 5,359,393      10/25/94  
***Apparatus for Image Registration***  
Steven C. Hart, Fred F. Hubble III, Thomas J. Hammond, Jeffrey J. Folkins & James P.  
Partin  
U.S. 5,394,223      2/28/95  
***Proper Charging of Donor Roll in Hybrid Development***  
Jeffrey Joseph Folkins, Thomas James Behe, Joseph G. Schram  
U.S. 5,420,375      5/30/95  
***Development System for Use in a Color Printer***  
Jeffrey J. Folkins, Daniel M. Bray & Alexander J. Fioravanti  
U.S. 5,499,084      3/12/96  
***Method and Apparatus for Establishing Exposure and Developer Setpoints for  
Color Image Formation***  
Jeffrey J. Folkins  
U.S. 5,515,155      5/7/96  
***Method and Apparatus to Improve Registration in a Black First Printing Machine***  
Jeffrey J. Folkins & Daniel W. Costanza  
U.S. 5,537,190      7/16/96  
***Process Color Using Light Lens Scanning Techniques***  
Jeffrey J. Folkins  
U.S. 5,548,391      8/20/96  
***Electrode Wire Positioning for Scavengeless Development***

Thomas J. Behe, Daniel M. Bray, Jeffrey J. Folkins, Steven C. Hart, & Joseph G. Schram  
U.S. 5,572,302 11/5/96

***Corona Dual-Use for Color Image Formation***  
Jeffrey J. Folkins  
U.S. 5,574,541 11/12/96

***Dual Use charging Devices***  
Jeffrey J. Folkins  
U.S. 5,574,540 11/12/96

***Multiple Use of a Sensor in a Printing Machine***  
Jeffrey J. Folkins  
U.S. 5,574,527 11/12/96

***Five Cycle Image On Image Printing Architecture***  
Jeffrey J. Folkins  
U.S. 5,576,824 11/19/96

***Single Positive Recharge Method and Apparatus for Color Image Formation***  
Zhao-Zhi Yu, Charles H. Tabb, John O'Brien, James Beachner, Mark Gwaltney, Meng Lean, Jeffrey J. Folkins  
U.S. 5,579,100 11/26/96

***Method and Apparatus for reducing Transferred Background Toner***  
Jeffrey J. Folkins  
U.S. 5,579,089 11/26/96

***Method and Apparatus for Reducing Residual Toner Voltage***  
Kenneth W. Pietrowski, Samuel W. Ing, Roger L. Bullock, Thomas J. Fleck, Charles H. Tabb, Zhao-Zhi Yu, Jeffrey J. Folkins, Daniel M. Bray, Cyril G. Edmunds  
U.S. 5,581,330 12/3/96

***Split Recharge Method and Apparatus for Color Image Formation***  
Jeffrey J. Folkins, Kenneth Pietrowski, Roger L. Bullock, Thomas J. Fleck, Charles H. Tabb, Zhao-Zhi Yu & Mark A. Gwaltney  
U.S. 5,600,430 2/4/97

***Negative Wrap Back Up Roll Adjacent the Transfer Nip***  
Thomas James Behe, Grace T. Brewington, Jeffrey Joseph Folkins & William H. Wayman  
U.S. 5,652,648 7/29/97

***Developer Set Up Using Residual Toner Voltage Readings***  
Jeffrey J. Folkins  
U.S. 5,666,590 9/9/97

***Donor Roll for Scavengeless Development in a Xerographic Apparatus***  
Thomas J. Behe, Jeffrey J. Folkins, Joseph G. Schram, William H. Wayman, Gerald T. Lioy and Grace T. Brewington  
U.S. 5,245,392 12/23/97

***Transfer, Cleaning and Imaging Stations Spaced Within An Interdocument Zone***  
Jeffrey J. Folkins  
U.S. 5,749,034 5/5/98

***Leading Edge electrostatic Voltmeter Reading in the Image-On-Image Electrophotographic Printing Process***  
Jeffrey J. Folkins  
U.S. 5,794,098 8/11/98

***Five Cycle Color Printing Architecture With Transfer After Cleaning***

Jeffrey J. Folkins  
U.S. 5,761,579

***Erase Before D.C. Recharge In Color Electrophotographic Printing***  
Jeffrey J. Folkins  
U.S. 5,794,106      8/11/98

***Reproduction Machine Including An Acoustic Scavengeless Assist Development Apparatus***  
Christopher Snelling, Dan A. Hays, Jeffrey J. Folkins & Dale Mashtare  
U.S. 5,809,385      9/15/98

***Integrated Multi-Toner Dispensing***  
Jeffrey J. Folkins  
U.S. 5,826,150      10/20/98

***Fused Image Sensing***  
Jeffrey Joseph Folkins & Vittorio Castelli  
U.S. 5,839,016      11/17/98

***Internal Erase Before Last Development In Color Electrophotographic Printing***  
Jeffrey J. Folkins & Charlie Tabb  
U.S. 5,848,335      12/8/98

***D.C. Recharge To Reduce Cross Contamination In The Read IOI Process***  
Jeffrey J. Folkins  
U.S. 5,778,289      7/7/98

***Erase Before A.C. Recharge In Color Electrophotographic Printing***  
Charles Tabb, Jeffrey Folkins, Kenneth Pietrowski  
U.S. 5,778,288      7/7/98

***Reduced Interdocument Zone in a Printing System Having a Single Developer Power Supply***  
Jeffrey J. Folkins  
U.S. 5,862,438      1/19/99

***Asymmetrical Donor Member Voltage***  
Jeffrey J. Folkins  
U.S. 5,940,667      8/17/99

***Wide Area Beam Sensor Method and Apparatus for Image Registration Calibration in a Color Printer***  
Jeffrey J. Folkins  
U.S. 5,909,235      6/1/99

***Switched Standby Housing Bias in REaD Printers***  
Jeffrey J. Folkins  
U.S. 6,006,049      12/21/99

***Method of Printing Secure Documents***  
Jeffrey J. Folkins, Michael M. Shahin, Craig Smith, Michael A. Parisi, Lingappa K. Mestha  
U.S. 5,983,065      11/9/99

***Five Cycle Color Printing Architecture With A Camming Mechanism For Engaging And Disengaging A Transfer And Cleaning Stations***  
Jeffrey J. Folkins  
U.S. 5,999,790      12/7/99

***Wrong-Sign Toner Detection System***  
Jeffrey J. Folkins  
U.S. 6,006,048      12/21/99

***Multiple charging of a toner image for transfer***  
Jeffrey J. Folkins  
U.S. 5,999,783      12/7/99

***Hybrid Scavengeless Development Using An Apparatus And A Method For Preventing Wire Contamination***  
Jeffrey J. Folkins & William Wayman  
U.S. 6,049,686 4/11/00

***A Non-Fuser Apparatus Customer Replaceable Unit Including a Fuser Release Agent Supply Assembly***  
Jeffrey J. Folkins  
U.S. 6,058,279 5/2/00

***Image to Paper Registration Sensor Utilizing differential Transfer***  
Jeffrey J. Folkins  
U.S. 6,201,937 B1 3/13/01

***Set-up and diagnosis of Printing Device Electrophotographic Cleaning Station Using Potential Measurement***  
Jeffrey J. Folkins  
U.S. 6233413 B1 5/15/01

***Aluminized Roll Including Anodization Layer***  
Thomas, J. Behe & Jeffrey J. Folkins  
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***Row Scrambling in Ejector Arrays***  
Jeffrey J. Folkins, Richard N. Ellson, Steven Buhler, David Mantell  
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Jeffrey J. Folkins, William Wayman, Robert Grace, Rasin Moser, Larry Hogestyn  
U.S. 6,668,146 12/23/03

***Multi-Stage Pre-Transfer Substrate Heating Assembly***  
Eilleen Aviles, Barry Mandel, Martin Krucinski, Jeff Folkins, Keith Buddendeck  
U.S. 6,932,526 8/23/05

***Alternate Imaging Mode for Multipass Direct Marking***  
Jeffrey J. Folkins  
U.S. 6,985,250 1/10/06

***Printer Jet Detection Method and Apparatus***  
Jeffrey J. Folkins  
U.S. 7,021,732 4/4/06

***Systems And Methods For Print Head Defect Detection And Print Head Maintenance***  
Jeffrey J. Folkins & Donald J Drake  
U.S. 7,264,328 9/07

***Enhanced printer reliability using extra print module***  
Donald Drake & Jeffrey J. Folkins  
U.S. 7,278,699 9/07

***Systems and Methods for print head defect detection and print head maintenance***  
Jeffrey J. Folkins & Donald Drake  
U.S. 7,300,133 11/27/07

***Ink Jet Printer Having Print Head With Partial Nozzle Redundancy***  
David A. Mantell & Jeffrey J. Folkins  
U.S. 7,338,144 3/4/08

***Ink Jet Printer Having Multiple Transfixing Modes***  
Jeffrey J. Folkins  
U.S. 7,390,084 6/24/08

***Asymmetric IDZ Precession in a Multi-Pass Direct Marking System***  
Jeffrey J. Folkins

U.S. 7,426,043      9/16/08  
***System And Method For Controlling A Print Head To Compensate For Subsystem Mechanical Disturbances***  
Jeffrey J. Folkins, Daniel W. Costanza, David Mantell, Gregg A. Guarino, Martin E. Hoover, Abu Islam  
U.S. 7,467,838      12/23/08  
***Dynamic IDZ Precession in a Multi-Pass Direct Marking System***  
Jeffrey J. Folkins  
U.S. 7,532,342      05/12/09  
***Systems and Methods for Detecting Inkjet Defects***  
Eklund, Elliott, Jeffrey J. Folkins, David L. Knierim  
U.S. 7,623,254      11/24/09  
***Double Reflex Printing***  
Jeffrey J. Folkins  
U.S. 7,665,817      2/23/10  
***Apparatus For Media Preheating In An Ink Jet Printer***  
Trevor Snyder, James Williams, Jeffrey Folkins, Barry Mandel  
U.S. 7,682,014      3/23/10  
***Ink Printer Using Forward Direction Printing Process***  
Jeffrey J. Folkins, James R. Larson, Paul J. McConville, Edward B. Caruthers, David J. Gervasi, Roger Leighton, Michael J. Levy  
U.S. 7,798,633      9/21/10  
***Ink-Jet Printer Using Phase-Change Ink Printing On A Continuous Web***  
James, Larson, Jeffrey J Folkins, Roger Newell, Donald Bott, Roger Leighton, Edward Caruthers, David Gervasi, David Mantell, Vincent Williams, Michael Levy, James Casella, Jeremy Dejong, Paul McConville  
U.S. 7,828,423      11-9-10  
***Printhead Registration Correction System And Method For Use With Direct Marking Continuous Web Printers***  
Yongsoon Eun, Enrique R. Viturro, Howard Mizes, Jeffrey Folkins  
U.S. 7,857,414      12-28-10  
***System And Method For Distributing Image Values Of A Color Separation***  
David Allen Mantell, Jeffrey J. Folkins  
U.S. 8,031,372      10/4/11  
***System And Method For Compensating For Weak, Intermittent, Or Missing Inkjets In A Printhead Assembly***  
Jeffrey J. Folkins & David Allen Mantell  
U.S. 8,042,899      10/25/11  
***Asymmetric IDZ Precession in a Multi-Pass Direct Marking System***  
Jeffrey J. Folkins  
U.S. 8,054,476      11/8/11  
***System And Method For Compensating For Registration Errors Arising From Heated Rollers In A Moving Web Printing System***  
Yongsoon Eun, Jess R. Gentner, Todd Thayer, R. Enrique Viturro, Jeffrey J. Folkins  
U.S. 8,136,907      3/20/12  
***System And Method For Compensating Runout Errors In A Moving Web Printing System***  
Yongsoon Eun, Jess R. Gentner, Jeffrey J. Folkins  
U.S. 8,162,428      4/24/12  
***Staggered Head Stitch Shifts in a Continuous Feed Direct Marking Printer***  
David Allen Mantell, Jeffrey J. Folkins

U.S. 8,167,404      5/1/12  
***Reflex Printing With Temperature Feedback Control***  
R. Enrique Viturro, Yongsoon Eun, Todd Thayer, Jeffrey J. Folkins  
U.S. 8,251,504      8/28/12  
***System And Method For Compensating For Small Ink Drop Size In An Indirect Printing System***  
Jeffrey J. Folkins & David Allen Mantell  
U.S. 8,256,857      9/4/12  
***Direct marking printer having a User configurable print resolution***  
James R. Larson & Jeffrey J. Folkins  
U.S. 8,287,081      10/16/12  
***Method And System For Printhead Alignment To Compensate For Dimensional Changes In A Media Web In An Inkjet Printer***  
Howard Mizes, R. Enrique Viturro, David Mantell, Jeffrey J. Folkins  
U.S. 8,292,398      10/23/12  
***Method And System To Compensate For Process Direction Misalignment Of Printheads In A Continuous Web Inkjet Printer***  
Yongsoon Eun, Enrique Viturro, Jess R. Gentner, Jeffrey J. Folkins  
U.S. 8,313,163      11/20/12  
***System And Method For Equalizing Multiple Moving Web Velocity Measurements In A Double Reflex Printing Registration System***  
Yongsoon Eun, Jeffrey J. Folkins, Jess R. Gentner  
U.S. 8,346,503      01/01/13  
***Non-Contact Heating Of Solid Ink Prints After Ink Fixing***  
James Larson, Jeffrey J. Folkins, Paul McConville  
U.S. 8,350,879      1/8/13  
***System And Method For Rendering Image Values To Be Printed In A Single Pass By Serially Arranged Printheads***  
David Allen Mantell, Jeffrey J. Folkins, James R. Larson  
U.S. 8,384,971      2/26/13  
***Method And System For Operating A Printhead To Compensate For Failed Inkjets***  
David Mantell & Jeffrey J. Folkins  
U.S. 8,419,160      4/16/13  
***Method And System For Aligning Printheads That Eject Clear Ink In An Inkjet Printer***  
Howard, Mizes, David Mantell, Joe Sheflin, Mike Mongeon, Mike Levy, Charles Rizzolo, Jeffrey J. Folkins  
U.S. 8,506,038      8/13/13  
***Method And System For Printhead Alignment To Reduce Or Eliminate Banding Artifacts For Interlaced Printheads***  
Howard Mizes, Jeffrey Folkins, David Mantell  
U.S. 8,517,502      8/27/13  
***Method And System For Reflex Printing To Compensate For Registration Errors In A Continuous Web Inkjet Printer***  
Jeffrey J. Folkins, Yongsoon Eun, Jess R. Gentner, Todd Thayer, R. Enrique Viturro  
U.S. 8,529,007      9/10/13  
***Reflex Printing With Temperature Feedback Control***  
R. Enrique Viturro, Yongsoon Eun, Todd Thayer, Jeffrey J. Folkins  
U.S. 8,567,894      10/29/13  
***Protective Device for Inkjet Printheads***

Barry Paul. Mandel, Jeffrey J. Folkins, Joannes N. M. DeJong, Lloyd A. Williams,  
Linn C. Hoover, Ruddy Castillo  
U.S. 8,573,733 11/5/13

***Test Pattern Less Perceptible To Human Observation And Method Of Analysis Of Image Data Corresponding To The Test Pattern In An Inkjet Printer***  
Howard Mizes, Jeffrey Folkins, Chrales Rizzolo,, Michael Mongeon  
U.S. 8,585,173 11/19/13

***Direct marking printer having a User configurable print resolution***  
James R. Larson & Jeffrey J. Folkins  
U.S. 8,608,278 12/17/13

***Temperature Leveling Roller and Pressure Nip Assembly***  
James Williams, Paul McConville, Jeffrey J. Folkins  
U.S. 8,641,163 2/4/14

***Method And System For Adjusting PrintHead Voltage Parameters In An InkJet Printer***  
Christine Ann Steurrys, David A Tence, James Buehler, Yeqing (Juliet) Zhang, Jeffrey J. Folkins  
U.S. 8,662,616 3/4/14

***Method And System For Split Head Drop Size Printing***  
David Allen Mantell, Jeffrey J. Folkins  
U.S. 8,668,294 3/11/14

***Method And System for Improved Ink Jet or Printhead Replacement***  
Russell J. Powers, Jan Enderle, Jeffrey J. Folkins  
U.S. 8,672,436 3/18/14

***Optical Data Transmission System For Direct Digital Marking Systems***  
U.S. 8,681,194 3/25/14  
ID20101698 Mark R. Kendrick | Pillsbury Winthrop Shaw Pittman LLP

***Method For Identifying And Verifying Dash Structures As Candidates For Test Patterns And Replacement Patterns In An Inkjet Printer***  
Howard Mizes, Helen Shin, David Mantell, Jeffrey J. Folkins  
U.S. 8,721,026 5/13/14

***System And Method For Process Direction Registration Of Inkjets In A Printer Operating With A High Speed Image Receiving Surface***  
Helen HaeKyung Shin, Howard Mizes, Jeffrey J. Folkins, Yeqing Juliet Zhang  
U.S. 8,764,149 7/1/14

***System And Method For Imaging And Evaluating Printing Parameters In An Aqueous Inkjet Printer***  
Howard Mizes, Jeffrey Folkins, Chu-heng Liu, David Mantell, Anthony Condello, Paul McConville  
U.S. 8,777,396 7/15/14

***System And Method For Sub-Pixel Ink Drop Adjustment For Process Direction Registration***  
Helen HaeKyung Shin, David Allen Mantell, Jeffrey J. Folkins,  
Patricia Donaldson, John Gary Shaw  
U.S. 8,814,300 8/26/14

***Printhead Having Apertures For Application Of A Surface Treatment Fluid***  
Greg Alan Hildebrand, Cory Daniel Luth, Jeffrey J. Folkins, Jeffrey Scott Rigotti,  
Srinivasa Deshiikan  
U.S. 8,820,885 9/2/14

***System and method for compensating for drift in multiple printheads in an inkjet printer***  
Yeqing Zhang, Jeffrey J. Folkins, Alex Scott Brougham  
U.S. 8,851,601 10/ 7/14

***System And Method For Spatial Dependent Correction For Images Printed With Multiple Drop Parameters***

Howard Mizes, Jeffrey Folkins, David Mantell  
U.S. 8,960,839 2/24/15

***Spreader/Transfix System For Handling Tabbed Media Sheets During Duplex Printing In An Inkjet Printer***

Barry P. Mandel, Jeffrey J. Folkins, Alex Brougham  
U.S. 8,967,789 3/3/15

***Method and Apparatus for Accumulating Excess Ink in a Stationary Receptacle in Imaging Devices that Form Images on Intermediate Imaging Surfaces***

Jeffrey Folkins, David Mantell  
U.S. 9,004,631 4/14/15

***System And Method For Process Direction Registration Between Multiple Inkjets In An Inkjet Printer***

Howard Mizes, Jeffrey Folkins  
U.S. 9,010,893 4/21/15

***Sparse Test Patterns In Printed Documents For Identification Of Inkjet And Printhead Performance In A Printer***

Howard Mizes, Jeffrey J. Folkins  
U.S. 9,044,960 6/2/15

***System And Method For Imaging And Evaluating Coating On An Imaging Surface In An Aqueous Inkjet Printer***

Howard Mizes, Jeffrey Folkins, Chu-heng Liu, David Mantell  
U.S. 9,056,495 6/16/15

***System And Method For Ink Drop Acceleration With Time Varying Electrostatic Fields***

Jeffrey Folkins, Jing Zhou, Richard Germain  
U.S. 9,114,609 8/25/15

***Scratch Resistant Inks***

Srini Deshhiikan, Jeffrey Folkins, Paul McConville, Joanne Lee  
U.S. 9,228,102 1/5/16

***Sacrificial Coating and Indirect Printing Apparatus Employing Sacrificial Coating on Intermediate Transfer Member***

James Larson, Mandakini Kanungo, Jeffrey Folkins, Santokh Badesha  
U.S. 9,327,519 5/3/2016

***System For Adjusting Operation Of A Printer During Three-Dimensional Object Printing Using An Optical Sensor***

Brian Conrow, Robert Kleckner, Jeffrey Folkins, Paul Hosier, Howard Mizes  
U.S. 9,327,537 5/3/2016

***Transfix Surface Member Coating***

Anthony Condello, Santokh Badesha, Mandakini Kanungo, Chu-heng Liu, Jeffrey Folkins, David Gervasi, Palghat Ramesh, Paul McConville, Phillip Wantuck, Lifeng Chen  
U.S. 9,353,290 5/31/2016

***Ink And Media Treatment To Affect Ink Spread On Media Treated With Primer In An Inkjet Printer***

Anthony Condello, Chu-heng Liu, Jeffrey Folkins, Daniel J. McVeigh, Joseph M. Ferrara, Christopher G. Lynn, Jason Hang  
U.S. 9,403,383 8/2/2016

***System And Method For Controlling Material Drop Volume In Three Dimensional Object Printing***

Hoosier, Mizes, Jeffrey Folkins, Brian Conrow, Paul Hosier, Robert Kleckner  
U.S. 9,415,546 8/16/2016  
***Method Of Etching Using Inkjet Printing***  
James Larson, Jeffrey Folkins, Chu-heng Liu, Wayne Buchar, Mandakini Kanungo,  
Santokh Badesha  
U.S. 9,447,504 9/20/16  
***Ink And Media Treatment To Affect Ink Spread On Media In An Inkjet Printer***  
Chu-heng Liu, Anthony Condello, Jeffrey Folkins  
U.S. 9,463,649 10/11/16  
***System And Method For Reducing Condensation On Printheads In A Print Zone Within An Aqueous Inkjet Printer***  
Anthony Condello, Jeffrey Folkins, Dan McVeigh, Linn Hoover, Paul McConville  
U.S. 9,539,817 1/10/17  
***Digital Manufacturing System For Printing Three-Dimensional Objects On A Rotating Surface***  
Patricia Donaldson, Jeffrey Folkins  
U.S. 9,604,412 3/28/17  
***Solid Ink Mask Removal Process***  
Paul McConville, Jeffrey J. Folkins, James Larson, Alex Fioravanti  
U.S. 9,648,752 5/9/17  
***Digital Manufacturing System For Printing Three-Dimensional Objects On A Rotating Core***  
Patricia Donaldson, Naveen Chopra, Jeffrey Folkins  
U.S. 9,701,064 7/11/17  
***Sacrificial Coating And Indirect Printing Apparatus Employing Sacrificial Coating On Intermediate Transfer Member***  
James Larson, Jeffrey Folkins, Mandakini Kanungo, Santokh Badesha  
U.S. 9,718,964 8/1/17  
***System For Controlling Operation Of A Printer During Three-Dimensional Object Printing With Reference To A Distance From The Surface Of Object***  
Jeffrey Folkins, Patricia Donaldson  
U.S. 9,738,032 8/22/17  
***System And Method For Operating A Three-Dimensional Printer To Compensate For Radial Velocity Variations***  
Patricia Donaldson, Jeffrey Folkins  
U.S. 9,751,259 9/5/17  
***System And Method To Maintain Printheads Operational In A Continuously Printing System***  
Jeffrey Folkins, James Larson, Paul McConville  
U.S. 9,862,193 1/9/18  
***System And Method For Missing Ejector Correction In Three-Dimensional Object Printing By Waveform Adjustment***  
David Mantell, Jeffrey Folkins  
U.S. 9,914,264 3/13/18  
***System And Method For Test Pattern Formation During Three-Dimensional Object Printing***  
Howard Mizes, Brian Conrow, Patricia Donaldson, Jeffrey Folkins, Paul Hosier, Robert Kleckner  
U.S. 10,052,823 8/21/18

***System And Method For Compensating For Dissimilar Shrinkage Rates In Different Materials Used To Form A Three-Dimensional Printed Object During Additive Manufacturing***

Anthony Condello, Jeffrey Folkins

U.S. 10,335,995 7/2/19

***Method For Providing Color And Material Property Options In A Three-Dimensional Object Printer***

Jeffrey J. Folkins, Barry Mandel

U.S. 10,406,803 9/10/19

*Issued Only in Brazil*

***A Dual Mode Development System***

Jeffrey J. Folkins Issued Brazil P18302878

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***Velocity of Transverse Ultrasound in Solid CD<sub>4</sub>***

R.P. Wolf, F.A. Stahl and J.J. Folkins, J. Phys. Chem. Solids, 39, 719 (1978)

***Magnetic, Optical and Magneto-Optical Behavior of LiTbF<sub>4</sub> and KTb<sub>3</sub>F<sub>10</sub> Crystals***

J.A. Griffin, J. Folkins, M.J. Weber, R. Morgret, J.D. Litster, D. Gabbe and A. Linz, J. Appl. Phys. 49(3), 209 (1978)

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J.A. Griffin, J.J. Folkins and D. Gabbe, Phys. Rev. Lett. 45, 1887 (1980)

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**Personal**

**Born 3/10/54**

**Wife: Cynthia Cowley Folkins**

**Children: Bethany (32) & Amelia (30)**