UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

UNIVERSAL IMAGING INDUSTRIES, LLC,
Petitioner.

v.

LEXMARK INTERNATIONAL, INC.,
Patent Owner.

_____

Case IPR2019-01380
Patent 7,844,786

_____

PATENT OWNER PRELIMINARY RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,844,786

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Petitioner's Exhibits	
Exhibit	**Description**
1001	U.S. Patent No. 7,844,786 to Lexmark
1002	Declaration of Dr. Harry Direen
1003	U.S. Patent No. 5,822,251 to Bruce
1004	U.S. Patent No. 5,995,774 to Applegate
1005	U.S. Patent No. 7,269,362 to Hama
1006	Curriculum vitae of Dr. Harry Direen
1007	Dallas Semiconductor, Inc. integrated circuit, part number DS1982
1008	File History of U.S. Patent No. 7,844,786

Patent Owner's Exhibits	
Exhibit	**Description**
2001	Declaration of Jeffrey J. Folkins, Ph.D.

I. INTRODUCTION

Universal Imaging Industries, LLC. ("Petitioner") filed a Petition for *Inter Partes* Review of claims 1-16 of U.S. Patent No. 8,445,786 ("'786 Patent;" Ex. 1001) on July 22, 2019. Paper No. 1 ("Petition.") The Petition is based on two grounds. Claims 1-4, 6-14, and 16 are challenged as being an anticipated by U.S. Patent No. 5,995,774 ("Applegate;" Ex. 1004) while dependent claims 5 and 15 are challenged as rendered obvious by Applegate in view of U.S. Patent No. 5,822,251 ("Bruce;" Ex. 1003.)

Lexmark International, Inc. ("Patent Owner") is a leading developer, manufacturer, and supplier of printing and imaging products, software, solutions, and services for consumers and businesses. Lexmark and its engineers have invested heavily innovating in these fields and have obtained numerous patents covering Lexmark inventions, including the '786 Patent at issue here. Petitioner intentionally designs its microchips to copy circuits in Lexmark's products which embody technologies protected by the '786 Patent, and therefore infringes the '786 Patent. Petitioner filed this Petition after Patent Owner filed a lawsuit in order to stop Petitioner's infringement of the '786 Patent and nine other Lexmark patents.

Patent Owner requests that this Petition be denied because Petitioner has failed to establish "that there is a reasonable likelihood that [it] would prevail with

respect to at least 1 of the claims challenged in the petition" under 35 U.S.C. § 314(a), as the Petition is both substantively and procedurally flawed.

First, the Petition places its eggs in one basket and relies on Applegate as allegedly anticipating all but two claims of the '786 Patent. Applegate, another Lexmark invention filed a decade before the '786 Patent, fails to disclose key limitations of the challenged claims. The '786 Patent claims are directed to command-based methods of updating memory modules. Applegate is not. There is zero disclosure in Applegate of updating memory modules via commands, let alone commands that instruct the memory modules to increment a counter or punch out a bit field. Petitioner anchors its challenge to irrelevant "sound bites" in Applegate of irreversibly burning a bit to track toner levels as being the claimed "punch out bit field command." However, Petitioner's analysis falls far short and ignores the crux of the claims: memory modules that both receive and process commands. Simply put, Applegate has little, if any, relevance to the '786 Patent claims.

Indeed, Petitioner's expert, Dr. Direen, admits to Applegate's holes and improperly attempts to fill in the gaps using another reference - a data sheet for a Texas Instrument product called "DS1982." This approach is a non-starter. For all but two challenged claims, the Petition uses Applegate as an anticipatory reference and so must show that these claims are taught within the four corners of Applegate. DS1982 is not incorporated by reference into Applegate and is therefore off-limits.

Dr. Direen's admission that Applegate cannot and does not anticipate the challenged claims is fatal to the Petition.

Petitioner's obviousness ground challenges just two dependent claims and adds only one reference to Applegate (Bruce, not DS1982). This ground fails for myriad reasons, most significantly, that the Petition does not demonstrate how Bruce redresses Applegate's failings as to the relevant independent claims. Petitioner also offers no rational justification for combining Applegate with a random reference geared toward memory storage on computers.

In view of these defects and the Petition's complete failure to show how the prior art taught the inventions claimed by the '786 Patent, the Board should deny the Petition.

II. THE '786 PATENT

At the time of the inventions of the '786 Patent, computing devices such as printers were becoming more advanced and included an increasing number of non-volatile memory modules. (Ex. 1001, '786 Patent at 1:32-34.) The increasing speed and page rates of printing, combined with the greater number of non-volatile memory modules needing to be updated, created significant difficulties updating each of the non-volatile memory modules at the same time. (*Id.* at 1:34-46.) Conventional communications protocols were insufficient to address these issues,

leaving an unmet need in the art for better addressing schemes, command protocols, and interfaces. (*Id.* at 1:64-2:2.)

The inventors of the '786 Patent met this need by developing novel methods and circuits for communicating with and off-loading processing to memory modules located in either the printer or the toner cartridge. (*See* Ex. 2001, Declaration of Jeffrey J. Folkins, Ph.D., in Support of Patent Owner Preliminary Response ("Folkins Decl.") ¶¶37-38.)[1] Moving certain command processing from the printer's processor to the memory modules allowed storage rates to keep up with increasingly-fast printing speeds. (*Id.* ¶45.) For example, printing systems typically track information about the number of pages printed and the amount of toner remaining in a cartridge. Indeed, "page count" information is tracked in multiple forms such that a single print may require incrementing multiple memories tracking data such as (1) total number of pages printed, (2) total number of color pages printed, and (3) total number of letter pages printed, to name a few. (Ex. 1001, '786 Patent at 4:54-62; *see also, id*. at 11:64-12:10 (explaining that "the increment counter command may be utilized with a plurality of counters with different counts - for example global

[1] Ex. 2001 is filed in support of this Patent Owner Preliminary Response as well Preliminary Responses in IPR2019-01378 (on U.S. No. 9,245,591 B2) and IPR2019-01381 (on Patent No. 8,966,193 B2). These patents share parts of a common specification with the '786 Patent. In his declaration, Dr. Folkins cites to the '193 Patent for the common specification disclosure across the three patents. (*See* Ex. 2001, Folkins Decl. ¶¶34-36.)

page counts, color page counts, letter-sized page counts, and transparency page counts").) In addition to updating page counts, non-volatile memories also track information about toner usage such as the amount of toner used per print job and the amount of toner left in a cartridge. (*Id.* at 4:62-5:11.) Thus, a single print job may require updating multiple memory modules with page count and toner information. (*Id*. at 5:12-15, 11:64-5:4.)

The '786 Patent describes and claims specific protocols for sending commands regarding count increments and toner levels to the memory modules for processing. In one embodiment, the '786 Patent teaches a specific protocol to send commands to increment a counter within one or more memory modules and to "punch out" (e.g., change from an erased state to a programmed state) a specified bit in one or more memory modules to record the depletion of toner in a cartridge. (*Id.* at 12:14-48.) Figs. 4A and 4B show illustrative command protocols, for example an increment counter command 402, a punch out bit field command 422, the address of a memory module 424, the length of a list of bit-field numbers 426, and the addresses of specific bit fields 428:

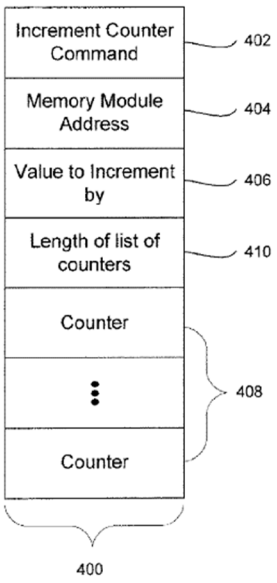

FIG. 4A

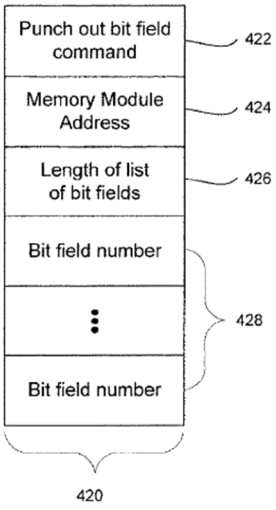

FIG. 4B

FIGs. 4A and 4B of the '786 Patent

The increment counter command enables each memory module to include a counter maintaining its own count, which makes it unnecessary for the processing device to know the present values of the counts which are being updated. (Ex. 1001 at 11:58-12:13; *see also* Ex. 2001, Folkins Decl. ¶45.) The punch out command, on the other hand, enables each memory module to change a particular bit field from an erased state to a programmed state signifying depletion of toner in the cartridge. (Ex. 1001, '689 Patent at 5:2-12, 12:33-48; *see also* Ex. 2001, Folkins Decl. ¶38.)

These protocols and commands can be implemented by the claimed memory modules because the '786 Patent employs an intelligent memory structure capable of processing commands. (Ex. 2001, Folkins Decl. ¶39.) For example, Figure 1B

(annotated) shows that the memory modules include a secure memory integrated circuit with processing capability for handling commands from the processing device.

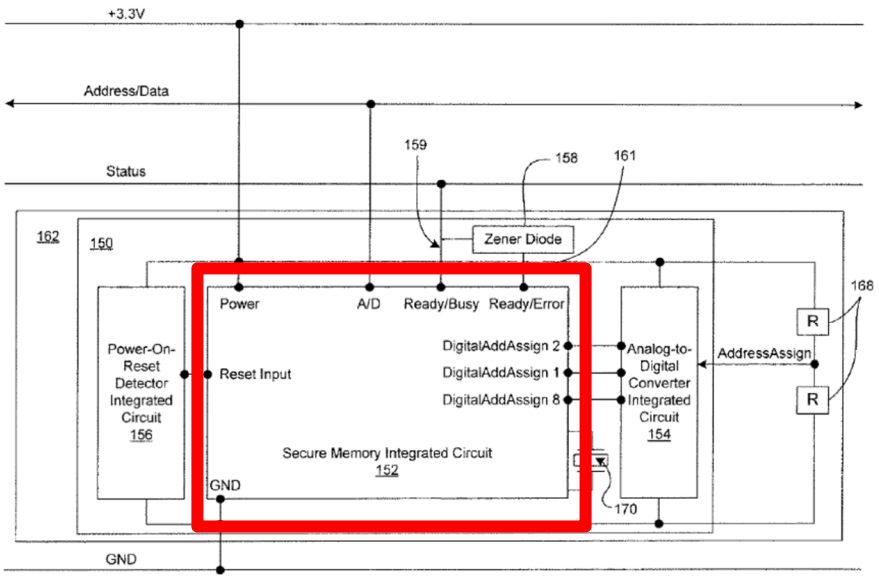

FIG. 1B

FIG. 1B of the '786 Patent (annotated)

Similarly, Fig. 3 (annotated) illustrates the processing steps performed by the intelligent memory module after it receives a packet containing the command at step 314:

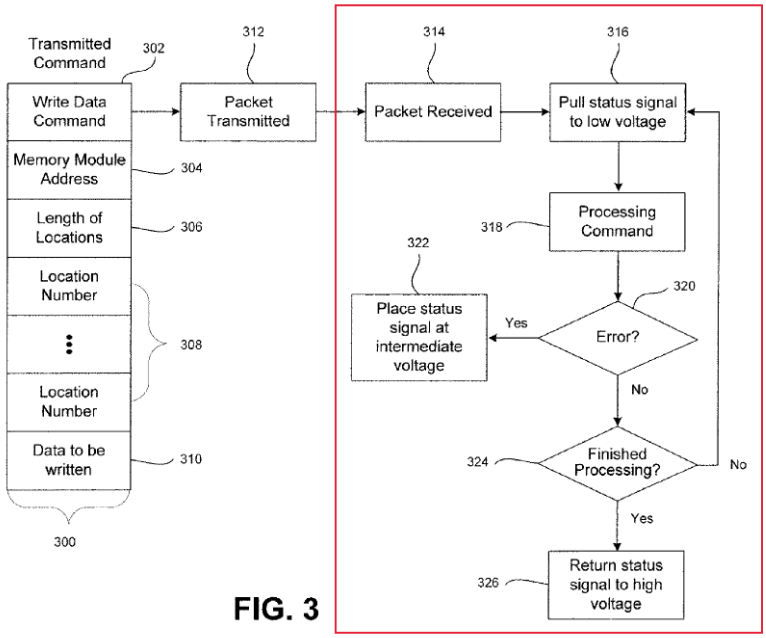

FIG. 3

FIG. 3 of the '786 Patent (annotated)

(*See also* Ex. 1001, '786 Patent at 11:47-57, Ex. 2001, Folkins Decl. ¶40.)

Both parties' experts agree that the claimed memory modules are intelligent (or "smart") memories. (*See* Ex. 2001, Folkins Decl. ¶39 ("the Challenged Patents employ intelligent memory"), *id.* ¶41, Ex. 1002, Declaration of Dr. Harry Direen ("Direen Decl.") ¶25 ("Figure 1B of the '786 does show the data bus connections going straight to the Secure Memory IC. *This means the memory device has to be a smart memory* device containing a serial data bus interface with internal command processing so that it can receive commands from an external processing device; process the commands; modify memory locations based upon command

requirements; and send responses back to the processing device including values contained in the memory locations.") (emphasis added).)

A. The Challenged Independent Claims

Independent claims 1, 9 and 16 are all directed to methods for updating memory modules and are reproduced below:

> Claim 1. A method of updating memory modules comprising,
>
> a command transmitted from a processing device,
>
> wherein the command comprises
>
> a) an increment counter command operable to instruct the one or more memory modules to increment the counter within the one or more memory modules and
>
> b) a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules; and
>
> processing the command at the one or more memory modules.
>
> Claim 9. A method of updating memory modules, comprising:
>
> receiving, at one or more memory modules, a command transmitted from the processing device, wherein the command is
>
> a) a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules and
>
> b) an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules; and

> processing the command at the one or more memory modules.
>
> Claim 16. A method of updating memory modules in an imaging device, comprising:
>
> receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command is indicative of usage of toner or ink in a consumable item in the imaging device and is operable to instruct the one or more memory modules to punch out a specified bit within the one or more memory modules indicative of said usage of toner or ink; and
>
> processing the command at the one or more memory modules.

B. Petitioner's Mischaracterization of the '786 Patent

Petitioner egregiously mischaracterizes the nature and scope of the '786 Patent in its attempt to highlight alleged similarities between the '786 Patent and its primary prior art reference — Applegate. (*See, e.g.*, Petition at 3-4.) Petitioner wrongly contends that the '786 Patent is "directed to storing the remaining level of toner or ink in a printer cartridge" and focuses its entire summary on the '786 Patent's minimal disclosure of a "punch out bit." (*See id.* at 3 (quotations omitted).) Petitioner's summary does not mention the term "memory modules," which appears at least four times in each of the independent claims, nor the terms "command" or "processing," which appear at least twice in each of these claims. Instead, Petitioner

ignores the majority of the '786 Patent's description and improperly tries to narrow the claims to "irreversibly storing information in a bit field." (Petition at 4.) Even Petitioner's own expert disagrees with Petitioner's summary of the '786 Patent. (*Compare* Petition at 3 ("The '786 Patent is generally directed to storing the remaining level of toner or ink in a printer cartridge.") *with* Ex. 1002, Direen Decl. ¶22 ("The '786 patent deals with updating a counter and a bit-field in a memory module or modules. The counter and bit-field are updated in response to a command from a processing device.").)

Contrary to the Petitioner's mischaracterizations, and as Petitioner's expert affirms, claims 1, 9 and 16 are directed to the processing of commands by memory modules to increment a counter and punch out a specific bit field. (*See* Ex. 2001, Folkins Decl. ¶57.) And a person of ordinary skill in the art would understand this concept because the claim language requires each limitation to be performed by the "one or more memory modules." (*See* Claim 1 (expressly reciting (a) "*receiving, at one or more memory modules*," (b) "an increment counter command *operable to instruct the one or more memory modules*;" (c) a punch out bit field command *operable to instruct the one or more memory modules*;" and (d) "*processing* the command *at the one or more memory modules*."); *see also* Ex. 2001, Folkins Decl. ¶¶39, 45, 99, 114, 127.)

III. PERSON OF ORDINARY SKILL IN THE ART

Petitioner proposes that a person of ordinary skill in the art (POSITA) at the time of the invention would have "a bachelor's degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems, including both hardware and embedded software design." (Petition at 5 (citing Ex. 1002, Direen Decl. ¶¶29-32).) Patent Owner does not believe that the definition of a POSITA is material to the outcome of this IPR Petition because Petitioner has not shown that the claims are anticipated or obvious to a POSITA given the level of skill proposed by Petitioner. Nevertheless, to the extent needed Patent Owner submits that a POSITA with respect to the subject matter of the '786 Patent would have a bachelor's degree in electrical and/or computer engineering with one or more years of work experience in printer design, including hardware and/or embedded software design for printer applications. (Ex. 2001, Folkins Decl. ¶31.)

IV. CLAIM CONSTRUCTION

Petitioner does not propose construction of any claim terms. (Petition at 5.) At this stage, the Board need not construe terms unless the construction is relevant to the Institution Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd. et al.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (Board "need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d

795, 803 (Fed. Cir. 1999)). In this case, the Petition fails to show a reasonable likelihood of prevailing regardless of what construction is given, so for the purposes of this Preliminary Patent Owner Response, Patent Owner does not propose any constructions.

V. SUMMARY OF ALLEGED PRIOR ART

A. Applegate

U.S. Patent No. 5,995,774 to Applegate et al. (Ex. 1004) is a Lexmark patent issuing on a 1998 application that generally describes "[a]n improved electrophotographic (EP) printer… having a detachable process cartridge that contains a non-volatile memory device, which is an EPROM that cannot be erased after a bit is burned." (*See* Ex. 1004, Applegate at Abstract; Ex. 2001, Folkins Decl. ¶58.) Applegate also details in Fig. 6 the structure of an EPROM memory designed to be included within a toner cartridge:

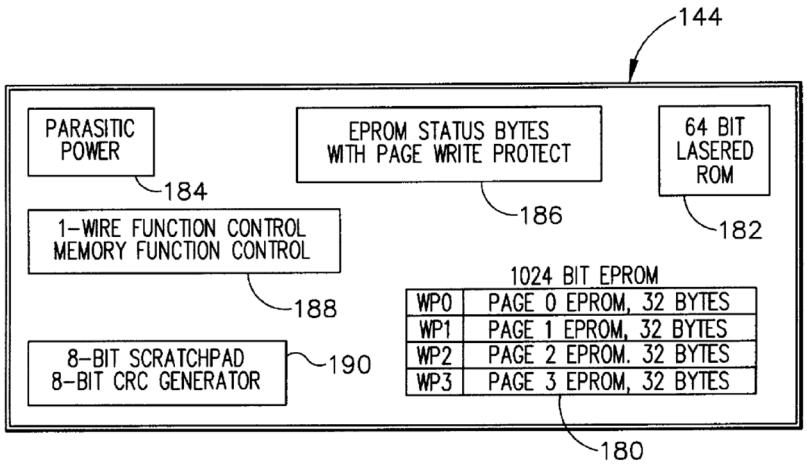

FIG. 6

FIG. 6 of Applegate

However, Applegate does not discuss communications protocols between the printer and the memory in the cartridge, nor the specific structure of any commands sent to the memory in the cartridge. (Ex. 2001, Folkins Decl. ¶59.) The only discussion in Applegate regarding how signals are communicated between the printer and the toner cartridge is a simple block diagram in Fig. 5 showing a two-wire interface 176 between the printer and the cartridge:

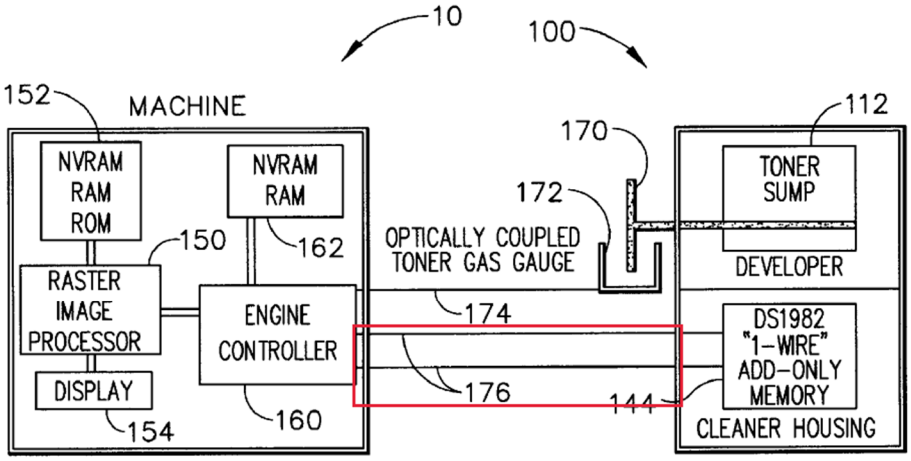

FIG. 5

FIG. 5 of Applegate (Annotated)

(*Id.* ¶59.) Neither this figure nor the explanation of it says anything about the content or structure of any messages sent over the two-wire interface 176. (*Id.* ¶60.) Nor does Applegate disclose any processing capability located within the memory. For

example, the only processors shown in Fig. 5 are located on the printer itself, such as the Raster Image Processor 150 and the Engine Controller 160. (*See id.* ¶¶60-61.)

Applegate generally discusses using a particular type of memory–a part made by Dallas Semiconductor called the "DS1982"– but does not describe how, if at all, the memory processes commands. (Ex. 1004, Applegate at 12:40-52.) Indeed, Applegate suggests that information about this part is only available by directly contacting the manufacturer. (*Id.* at 13:8-10 ("The details of the construction of the EPROM chip 144 can be obtained from its manufacturer, Dallas Semiconductor, Inc., located in Dallas Tex.").)

B. Bruce

U.S. Patent No. 5,822,251 to Bruce et al. generally describes an expandable flash memory system. (Ex. 1003, Bruce at Abstract.) According to the background of the invention section, Bruce was trying to solve the need for expandable memory in *computer* storage systems, particularly in view of the physical limitations of prior art hard disks. (*Id.* at 1:22-43; *see* Ex. 2001, Folkins Decl. ¶93.) Bruce sought to address this problem by grouping flash memory chips in banks attached to common flash buffer chips. (Ex. 1003, Bruce at Abstract, Fig. 1; Ex. 2001, Folkins Decl. ¶93.)

Therefore, Bruce is intended to solve problems associated with expanding the amount of memory in a fixed flash memory system. The '786 Patent, by contrast,

explains that the problem to be addressed includes the cost premium associated with additional electrical connections in small disposable devices such as printer cartridges. (Ex. 1001 at 1:51-63.) Bruce does not mention printers or the technical issues unique to printer cartridges or other disposable components with embedded memory. (Ex. 2001, Folkins Decl. ¶96.)

VI. LEGAL STANDARDS

A. Anticipation

"It is axiomatic that for anticipation, *each and every* claim limitation must be explicitly or inherently disclosed in the prior art." *In re NTP, Inc.*, 654 F.3d 1279, 1302 (Fed. Cir. 2011) (citations omitted). "To establish anticipation, each and every element in a claim, arranged as is recited in the claim, must be found in a single prior art reference." *ZTE Corp. v. ContentGuard Holdings, Inc.*, IPR2013-00134, Paper 12 at 24 (PTAB June 19, 2013) (citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001)); *NetMoneyIn, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008). To anticipate, "[t]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." *Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991). Thus, the Board "must analyze prior art references as a skilled artisan would." *Microsoft Corp. v. Proxyconn Inc.*, IPR2012-00026, Paper 73 at 33 (PTAB Feb. 19, 2014) (internal citations omitted).

An anticipatory reference need not "duplicate word for word what is in the claims." *Standard Havens Products, Inc. v. Gencor Industries, Inc*., 953 F.2d 1360, 1369 (Fed. Cir. 1991). However, "anticipation by inherent disclosure is appropriate only when the reference discloses prior art that must necessarily include the unstated limitation, [or the reference] cannot inherently anticipate the claims." *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1355 (Fed. Cir. 2013) (quoting *In re Omeprazole Patent Litigation*, 483 F.3d 1364, 1378 (Fed.Cir.2007)); *see also HTC Corp. v. Cellular Commc'ns Equip., LLC*, 877 F.3d 1361, 1368 (Fed. Cir. 2017) ("A party seeking to establish inherent anticipation must show that a person of ordinary skill in the art would recognize that missing descriptive matter in a prior art reference is nevertheless necessarily present"). Inherency "may not be established by probabilities or possibilities." *PersonalWeb Techs. LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (overturning PTAB Final Written Decision of obviousness where challenged limitation was not "necessarily" present in cited reference) (quoting *PAR Pharm., Inc. v. TWI Pharm., Inc*., 773 F.3d 1186, 1195 (Fed. Cir. 2014)). Conclusory assertions that a limitation is inherent, whether by counsel or by experts, are insufficient to meet a Petitioner's burden. *Roland Corp. v. inMusic Brands, Inc.*, IPR2018-00335, Paper 14 at 26 (PTAB July 2, 2018) (Decision Denying Institution); *Universal Remote Control, Inc. v. Universal Electronics, Inc.*, IPR2014-01146, Paper 12 at 4 (PTAB Feb. 19, 2015).

B. Obviousness

To establish obviousness, it is the petitioner's "burden to demonstrate… that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (quotations omitted).

As explained by the Federal Circuit:

> Obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim. . . . Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.

Unigene Labs., Inc. v. Apotex, Inc., 655 F.3d 1352, 1360 (Fed. Cir. 2011) (citations omitted). "To render a claim obvious, prior art cannot be 'vague' and must collectively, although not explicitly, guide an artisan of ordinary skill towards a particular solution. . . . [A] combination is only obvious to try if a person of ordinary skill has 'a good reason to pursue the known options.'" *Id.* at 1361 (quoting *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 418 (2007)). The party challenging a patent as obvious cannot rely on "mere conclusory statements," but must instead provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn,* 441 F.3d 977, 988 (Fed. Cir. 2006)). "It is impermissible to use the claimed invention as an

instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991)).

VII. THE PETITION SHOULD BE DENIED UNDER 35 U.S.C. § 314(a) BECAUSE IT FAILS TO SHOW A REASONABLE LIKELIHOOD THAT ANY CHALLENGED CLAIM OF THE '786 PATENT IS UNPATENTABLE

A. The Petition Fails to Show a Reasonable Likelihood of Prevailing on Ground 1's Challenge to Fourteen Claims as Anticipated by Applegate

For the reasons outlined below, Petitioner has not met its burden of proving a reasonable likelihood of success on this Ground.

1. Applegate does not disclose receiving a command which comprises "an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules"

Applegate does not disclose this limitation. Independent claims 1 and 9 require receiving "an increment counter *command operable to instruct the one or more memory modules* to increment a counter *within the one or more memory modules*" (emphasis added). Petitioner generally points to Applegate's update of a "toner gram count," but the claims are not limited to an "increment counter" alone; instead, they expressly define both "how" the counter is incremented ("*receiving . . . a command operable to instruct* . . to increment a counter") and "where" the counter is incremented (receiving . . . a command . . *to increment a counter within the one*

or more memory modules"). (*See also* Ex. 2001, Folkins Decl. ¶94.) Petitioner cannot and does not show any memory module in Applegate that does this.

For this limitation, Petitioner relies on Figure 5, its corresponding description (Ex. 1004, Applegate at 11:31-38), and Figure 6. (Petition at 10.) But nowhere in these disclosures is there any mention of a "command" that instructs the "memory modules" to increment a counter within the memory module. (Ex. 2001, Folkins Decl. ¶¶100-01; *see also id.* ¶¶102-13.) Figure 5 is nothing more than a schematic diagram of Applegate's hardware system and simply depicts communication between the engine controller and the add-only memory 144 via wires 176.

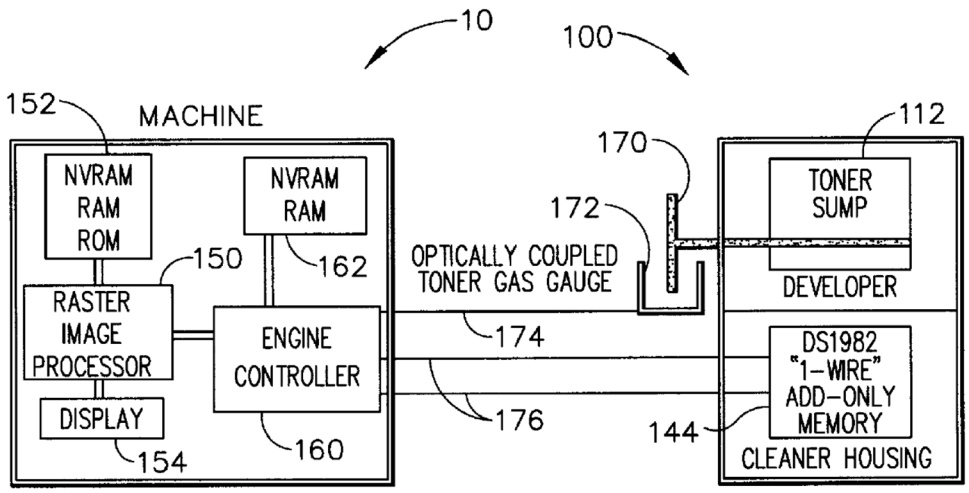

FIG. 5

FIG. 5 of Applegate

Absent from Figure 5 and its description is any disclosure of the "how" or "where" elements required by this claim limitation. (*Id.* ¶¶102, 108-09.) Specifically, there is no disclosure of the protocols used for communication between the printer and the memory, let alone any mention of a "command" sent over the two wires wherein the command instructs the memory module to increment a counter. (*See id*.) Figure 6 does not advance Petitioner's argument either as it simply depicts Applegate's memory structure but with no details about its operation or ability to execute commands. (*Id.* ¶¶104-05.)

Petitioner fares no better with its reliance on Col. 2, lines 17-21 from Applegate's "Background of the Invention."[2] (Petition at 10.) Here, Applegate discusses U.S. Patent No. 5,276,461 to Tokyo Electric, which is not incorporated by reference and thus not part of the Applegate specification. *See Advanced Display Sys., Inc. v. Kent State University*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) ("To incorporate material by reference, the host document must identify with detailed

[2] An anticipation challenge cannot rely on disparate teachings from within a patent, including a distinct prior art system. *See, e.g., Net MoneyIn, Inc.* 545 F.3d at 1371 ("[I]t is not enough that the prior art reference … includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention"); *see also In re Arkley*, 59 C.C.P.A. 804, 455 F.2d 586, 587 (1972) ("[T]he [prior art] reference must clearly and unequivocally disclose the claimed [invention] or direct those skilled in the art to the [invention] without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference.").

particularity what specific material it incorporates and clearly indicate where that material is found in the various documents.") As to the Tokyo Electric patent, Applegate simply recites:

> The non-volatile memory comprises an EEPROM integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of printed media.

(Ex. 1004, Applegate at 2:17-21.) This disclosure fails to advance the ball because it too is silent as to "how" ("command operable to instruct the one or more memory modules to increment") and "where" ("increment a counter within the one or more memory modules") the counter is incremented and says nothing about transmitting any command from the processing device to a memory module, and certainly not the increment counter command recited by the claims. (Ex. 2001, Folkins Decl. ¶¶106-07.)

Petitioner points to Applegate's toner gram count in its final attempt to satisfy this limitation. (Petition at 10 (citing Ex. 1004, Applegate at 20:18-22).) This passage describes actions taken by the printer but lacks any detail about how or where the toner gram is incremented. Even considering this brief description in Applegate, Petitioner fails to offer any explanation whatsoever as to how Applegate's "toner gram count" is incremented using a command received by and

implemented within Applegate's memory module. (Ex. 2001, Folkins Decl. ¶¶110-13.)

To the contrary, Applegate simply discloses that the "toner gram count is *updated* after [a] sheet of media has completed its printing." (Ex. 1004, Applegate at 20:21-22 (emphasis added).) Petitioner does not argue that Applegate's update is based on a command received from the printer. (Ex. 2001, Folkins Decl. ¶112.) Nor does Petitioner argue that this element is inherent. The mere fact that the toner gram count is "updated" does not mean it was updated by a command instructing the memory module to increment its counter. (*Id.* ¶113.) A processor writing an updated value to memory is not the same as a processor sending an increment counter command instructing the memory module to increment its counter by adding to a value already stored in the memory module. (*Id.*; *see also id.* ¶¶42-44.) Applegate's brief disclosure of a toner gram count is insufficient to identify any command that tells the memory module to increment a counter. (*Id.* ¶113.) Given Applegate's limited disclosure and Petitioner's lack of explanation, Applegate cannot and does not anticipate claims 1 and 9 or the claims that depend therefrom.

2. Applegate does not disclose "receiving a command… for instructing the memory module to punch out at least one bit

of at least one specified bit field within the memory module indicative of the usage of toner or ink"

Independent claims 1, 9, and 16 all require that the memory modules receive a command instructing it to "punch out" at least one bit of a "specified bit field" within the memory module:

Claim	Limitation
1	A punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules
9	A punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules
16	A command, transmitted from a processing device, wherein the command . . . is operable to instruct the one or more memory modules to punch out a specified bit within the one or more memory modules indicative of said usage of toner or ink

Petitioner fails to show any teaching in Applegate of a punch out bit field command received and processed by memory modules. (Ex. 2001, Folkins Decl. ¶¶114-16.) This lack of showing is hardly surprising because Applegate is not focused on methods for updating memory modules.

The Petition cites to Applegate as teaching that "[a]fter a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned…" (Petition at 11 (citing Ex. 1004, Applegate at Abstract).) However, Petitioner fails to show how this passage

discloses any *command,* let alone the required *command* instructing the memory module to punch out a "specified bit field." (Ex. 2001, Folkins Decl. ¶¶117-18.)

Petitioner relies on various Applegate passages found at Column 6, lines 10-14, and Column 14, lines 43-54 that merely discuss the general idea of punching out bits. These passages are completely silent regarding using a command to punch out "a specified bit field." And the Petition's citation to Column 11, lines 31-38 fares no better as it generally describes the idea that the controller is electrically linked to the EPROM, but doesn't describe a command to the EPROM, let alone describe the content of the commands. (*See id.* ¶¶118-20, 122-23.)

As explained above, Figures 5 and 6 of Applegate are general schematics of the interface between the printer and the toner cartridge (Fig. 5) and the EPROM in the cartridge (Fig. 6).

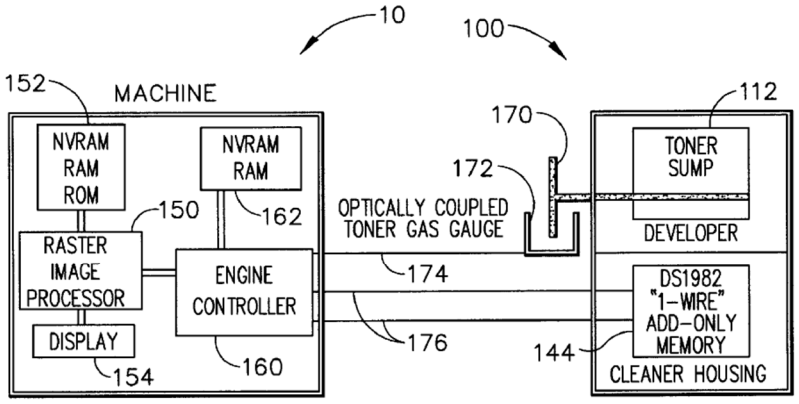

FIG. 5

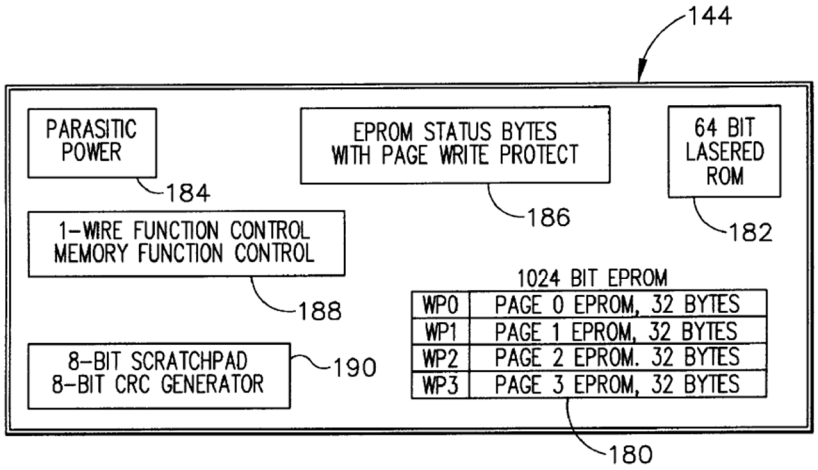

FIG. 6

FIGs. 5 and 6 of Applegate

Neither figure depicts a command nor the content of a specific command. (*See id.* ¶¶120-21.) And neither the Petition nor the Declaration of Dr. Harry Direen (Ex. 1002, "Direen Decl.") cites any specific portion of these figures or explains how they show a command.

The Petitioner's reliance on step 406 of Fig. 9 is also misplaced.

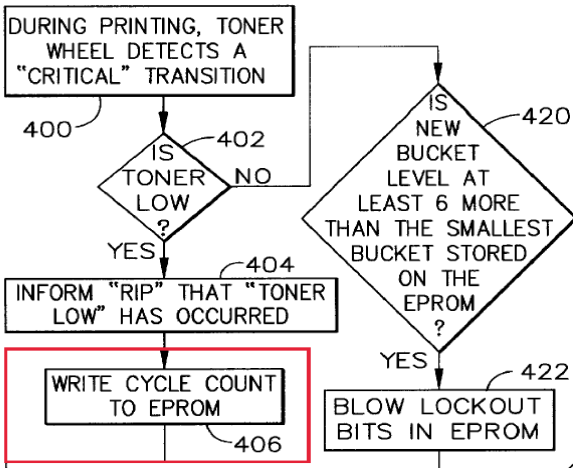

FIG. 9 of Applegate (annotated)

Step 406, labeled "write cycle count to EPROM" says nothing about a command to punch out a specified bit field. And neither the Petition nor the Direen Declaration explains why a POSITA would infer such a specific command from this notation. (*Id.* ¶128.)

Dr. Direen's declaration does nothing to bolster Applegate's lack of disclosure. Like the Petition, Dr. Direen provides no explanation as to *why* a command having the specified format—that is, a command instructing the memory to punch out a specified bit field—would necessarily be present in the system taught by Applegate. Such conclusory assertions are insufficient to show that a limitation not explicitly disclosed is inherently present. *Roland*, IPR2018-00335, Paper 14 at 26; *Universal Remote Control,* IPR2014-01146, Paper 12 at 4.

Dr. Direen also opines, without any support, that "[t]he fact that Applegate disclosed modifying memory locations implies that the commands are processed and carried out." (Ex. 1002-A at 7; s*ee also id.* at 4 ("In order to "burn" a bit or write a value in the EPROM memory a command must be sent from a master device to the memory slave device indicating that a bit in a bit field must be changed.") As explained in the declaration of Jeffrey J. Folkins, Ph.D., writing information to memory can be done in at least two ways: the information can be written based on (1) direct instruction from a central processor to write a specific value; or (2) instruction from a central processor to read a current value, modify that value by

some amount, and write whatever new value is calculated by a processor associated with the memory executing that instruction. (Ex. 2001, Folkins Decl. ¶¶42-44.) Thus, Dr. Direen's conclusory assertion does not comport with the operation of memory in practice. And putting aside its conclusory nature, this argument never appears in the Petition itself and thus should not be given any weight by the Board. *Cisco Systems, Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 at 7-10 (PTAB Aug. 29, 2014); *2Wire, Inc. v. TQ Delta, LLC,* IPR2015-00239, Paper 18 at 10 (PTAB May 29, 2015).

Because Petitioner and its expert fails to identify any evidence in Applegate, either explicitly or inherently, of a command to punch out a specified bit field in a memory, it fails to meet its burden of showing that independent claims 1, 9 and 16 are anticipated by Applegate.

3. Applegate does not disclose processing the command at the one or more memory modules

The last limitation found in all three independent claims recites "processing the command at the one or more memory modules." (*See* claims, 1, 9 and 16.) Petitioner fails to show that Applegate discloses any command for at least the reasons stated above, and certainly does not show that the (non-existent) command is processed by the memory modules.

Petitioner argues that Applegate's writing cycle counts to the EPROM and irreversible burning a bit on an EPROM memory are "commands … processed at the one or more memory modules." (Petition at 12-13.) This is wrong.

Petitioner misinterprets the claimed "memory module" to be nothing more than dumb memory limited to storing a predetermined value. The '786 Patent and claims make clear that the "memory modules" must be intelligent and thus capable of receiving commands or executing instructions. (Ex. 2001, Folkins Decl. ¶39.) Indeed, Figure 1B depicts the "memory modules" as intelligent modules including a secure memory integrated circuit with processing capability for handling commands from the processing device.

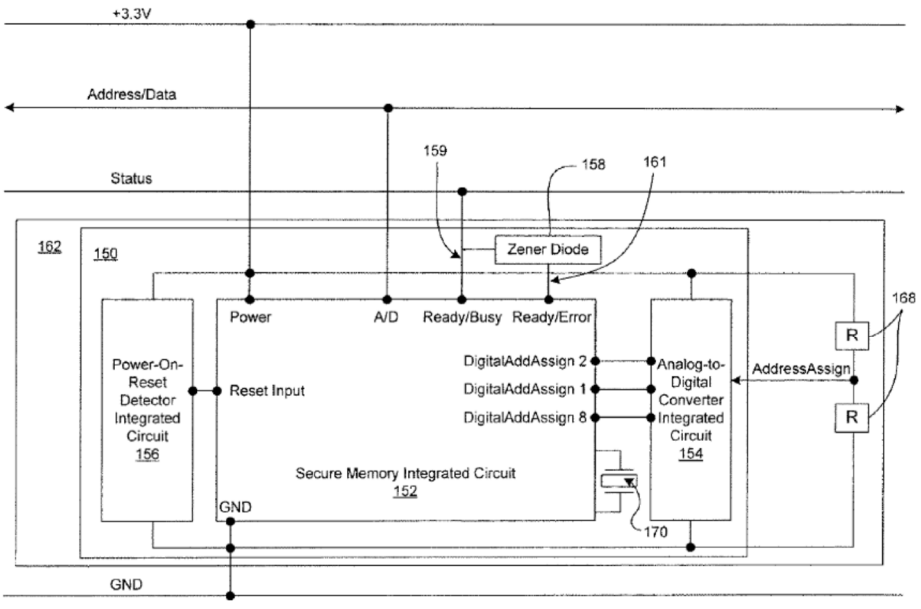

FIG. 1B

FIG. 1B of Applegate

Processing commands within the memory modules rather than at the central processor results in faster operations thus allowing page counts and the like to be quickly updated and keep up with ever-increasingly faster print speeds. (Ex. 1001, '786 Patent at 1:39-46, 1:64-5:2; Ex. 2001, Folkins Decl. ¶¶45, 128.) Indeed, Dr. Direen agrees with Patent Owner and Dr. Folkins and admits that the claimed memory modules are intelligent and capable to processing commands as shown by his testimony below:

> Figure 1B of the '786 does show the data bus connections going straight to the Secure Memory IC. This means ***the memory device has to be a smart memory device*** containing a serial data bus interface ***with internal command processing so that it can receive commands from an external device; process the commands; modify memory locations based on the command requirements;*** and send responses back to the processing device including values contained in the memory locations.

(Ex. 1002 ¶ 25 (emphasis added).)

In Applegate, the command processing steps are performed by the printer's processor (engine controller 160) and not by memory 144. Even Figure 6, which illustrates Applegate's memory, fails to depict any type of processing capability.

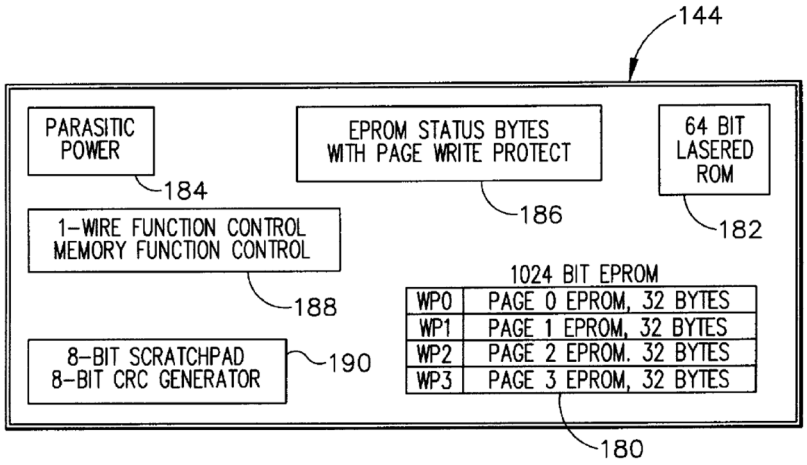

FIG. 6

FIG. 6 of Applegate

(Ex. 2001, Folkins Decl. ¶105.) The few references to the EPROM memory in Applegate simply describe writing a resulting value (e.g. cycle counts or bucket levels) to the memory based on a calculation from a central processor. (*Id.* ¶128.) Thus, both experts agree: Applegate's memory is not capable of processing commands. Applegate's memory cannot and does not meet this claim limitation.

For at least the reasons stated above, Applegate does not anticipate independent claims 1, 9 and 16. Similarly, because Applegate is deficient with respect to the independent claims, it cannot anticipate the claims depending therefrom including dependent claims 2-4, 6-8, 10-14 and 16. Accordingly, Ground 1 of the Petition must be denied.

B. The Petition Fails to Show a Reasonable Likelihood of Prevailing on Ground 2's Obviousness Challenge Based on Applegate in View of Bruce

1. Bruce does not teach any element missing from Applegate

For at least the reasons stated above and incorporated herein, Applegate does not anticipate independent claims 1 and 9 from which claims 5 and 15 depend. Bruce does not cure Applegate's deficiencies. Indeed, Petitioner does not argue that Bruce meets any of the limitations in independent claims 1 or 9. (Petition at 26-28 (entire discussion of Ground 2).) Nor does the Petition argue that the combination of Applegate and Bruce renders obvious any aspect of claims 1 or 9 that Applegate failed to disclose on its own. (*See id.*) Thus, Petitioner's combination of Applegate in view of Bruce cannot, and does not, render claims 5 and 15 obvious. (*See* Ex. 2001, Folkins Decl. ¶¶129-30.)

Petitioner separately asserts that "Ground 1 … shows how Applegate anticipates" claims 5 and 15.[3] (Petition at 27-28.) This assertion should be ignored for myriad reasons: most notably because no reference to the claimed "busy status signal" is found in any prior section of the Petition covering Applegate or Ground 1. To the extent the Board gives this assertion any weight, it should be only to deny

[3] Patent Owner understands Petitioner's claim that "Ground 1 also shows how Applegate anticipates claim 5" in the section addressing claim 15 to mean Petitioner believes Applegate anticipates claim *15*.

institution on Ground 2 for failing to state with particularity the scope of the challenged Grounds. *See* 35 U.S.C. § 312(a)(3); *see also adidas AG v. Nike, Inc.,* IPR2016-00920, Paper 6 at 6 (PTAB Oct. 20, 2016) (denying institution because, *inter alia*, an obviousness challenge "cite[d] to portions of [a primary reference] for all features of that claim, and also submit[ted] parallel citation in some cases to portions of [a secondary reference]" without "provid[ing] adequate explanation as to what features [petitioner] contends are absent from [the primary reference] that it also must rely on content of [the secondary reference] to meet the challenged claims.").[4]

2. The Petition and Dr. Direen fail to show that a POSITA would have combined Applegate and Bruce

Even if the Petitioner could show, which it cannot, that the combination of Applegate and Bruce teach each claim limitation of independent claims 1 and 9, Petitioner's obviousness ground still fails because Petitioner's alleged motivation to combine falls far short of even the basic requirements. Petitioner merely asserts that both Applegate and Bruce "disclose integrated circuits comprising memory cells" and that a POSITA "would be motivated to combine Bruce's improved memory

[4] The supposed grounds for challenging claim 5 and 15 are only further confused by Dr. Direen's Declaration, as he suggests that the claims are rendered obvious by Applegate in view of "PK" (which is "POSITA's Knowledge) and/or Bruce and/or yet another reference, Hama. (*See* Ex. 1002, Direen Decl. at 20, Table 1.)

handling techniques in order to improve the memory capabilities of the printer cartridges disclosed in Applegate." (Petition at 27.) Such conclusory assertions are inadequate to support an obviousness analysis. *KSR*, 550 U.S. at 418 (2007) (combination of prior art teachings must be based on "some articulated reasoning with some rational underpinning") (quoting *In re Kahn*, 441 F.3d 977, 998 (Fed. Cir. 2006)).

The fact that references are in a similar technical field does not explain why or how a POSITA would modify one reference according to the teachings of the other. *See Johns Manville Corp. v. Knauf Insulation, Inc.,* IPR2018-00863, Paper 8 at 19 (PTAB Oct. 2, 2018) (analogous art is "merely a threshold inquiry" and "is not sufficient to establish that a POSITA would have had reason to combine its teachings with other prior art in the manner set forth in the claim") (quoting *Secarus Techs., Inc. v. Glob. Tel*Link Corp.,* 701 F.App'x. 971, 977 (Fed. Cir. 2017) ("a broad characterization of [prior art references] as both falling within the same alleged field… without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness combination")); *see also DUO Security Inc. et al v. Strikeforce Techs., Inc.*, IPR2017-01041, Paper 7 at 21 (PTAB Oct. 16, 2017) (assertion "that the three references are in the same field and their disclosed systems share broad and general similarities" was inadequate to provide specific reason to combine). The Petition does not explain what need is unmet by

Applegate, why a POSITA would look to Bruce to solve it, or how a POSITA would modify the teachings of Applegate to incorporate the teachings of Bruce.

Moreover, Dr. Direen's declaration does nothing to bolster Petitioner's obviousness argument. Absent from Dr. Direen's declaration is any explanation as to why a POSITA would have combined Applegate and Bruce. In fact, Dr. Direen never contends that claims 5 and 15 are obvious in view of Applegate and Bruce. (*See* Ex. 1002, Direen Decl. ¶¶52-53 and Table 120.) Instead, Dr. Direen opines that claims 5 and 15 are anticipated by Applegate but also points to Bruce in his "obviousness notes" as teaching the "claimed busy status signal". (*Compare* Ex. 1002-A at 12-13, 25 *contrasted with* Ex. 1002, Direen Decl. ¶53, Table 1.) And while Patent Owner is unable to decipher the specific grounds under which dependent claims 5 and 15 are challenged, *see supra* Section VII.A.3 and n.4, what is abundantly clear is Dr. Direen fails to provide any motivation, let alone articulate any rational underpinning, for combining Applegate and Bruce (or any other reference) to construct the claimed invention.

Nor could he. A POSITA would not have been motivated to combine Applegate to attain the claimed system because neither reference discloses (let alone suggests) the claimed command to punch out a bit and increment a counter that are received and processed by the memory modules. (Ex. 2001, Folkins Decl. ¶¶131-

32.) In sum, the combination of Applegate in view of Bruce cannot and does not render obvious dependent claims 5 and 15.

VIII. DR. DIREEN IMPROPERLY RELIES ON MATERIAL OUTSIDE OF APPLEGATE FOR HIS ANTICIPATION ANALYSIS

Petitioner fails to meet its burden to show that Applegate *anticipates* any claims of the '786 Patent at least because its expert's "anticipation" analysis repeatedly relies on material beyond the disclosure of Applegate itself, including an unauthenticated purported product specification and various unsupported assertions about the common knowledge of a POSITA.

In particular, the Direen Declaration repeatedly relies on an undated document (Ex. 1007) which Dr. Direen claims is a datasheet for a memory part number referenced in the specification of the '786 Patent. (*See, e.g.* Ex. 1002, Direen Decl. ¶44; Ex. 1002-A at 2, 4-5, 7, 11, 14, 15, 19, 21, 26, and 29.) Dr. Direen repeatedly asserts that "[f]or a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference." (*See, e.g.* Ex. 1002-A at 3.) This assertion fails.

In order to incorporate other material by reference for purposes of anticipation, a document must cite such material "in a way that makes clear that the material is effectively part of the host document as if it were explicitly contained therein." *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed.

Cir. 2000). The host document must further "identify with detailed particularity what specific material it incorporates and clearly indicate where that material is found in the various documents." *Id.*

Applegate does neither of these things with respect to Petitioner's Exhibit 1007, the purported DS1982 datasheet. Applegate merely references the part number "DS1982" (*see, e.g.*, Ex. 1004, Applegate at Fig. 5, 5:31-35, 12:39-48) and suggests that "[t]he details of the construction of the EPROM chip 144 can be obtained from its manufacturer, Dallas Semiconductor, Inc., located in Dallas Tex" (*id.* at 13:8-10). Applegate contains no clear indication that any material outside of the specification relating to this part number was intended to be "effectively part of" its specification. When the authors of Applegate did incorporate material by reference, such as another Lexmark patent, U.S. Patent No. 5,634,169, they did so explicitly. (*Id.* at 5:51-57.) There is no such statement with respect to any document relating to the DS1982 chip. Nor does the passing reference to obtaining information about the DS1982 from its manufacturer identify with particularity any specific document.

Even if Applegate incorporated by reference information about DS1982, which it does not, Petitioner fails to prove that the document that it attached to its Petition as Ex. 1007 was in fact the same DS1982 reference as the DS1982 reference allegedly incorporated by Applegate. Ex. 1007 is undated, and Petitioner provides

no evidence to authenticate Ex. 1007 or even show where it came from (other than a web address listed in a footnote, see Ex. 1002, Direen Decl. ¶44 n.1), much less that it was published prior to Applegate or is somehow incorporated into Applegate's disclosure. Therefore, Petitioner has failed to authenticate DS1982 and so its reliance on Ex. 1007 is improper for any purpose, but particularly for an invalidity ground based on anticipation, where Petitioner's burden is to show that the claims are taught within the four corners of Applegate.

Nevertheless, Dr. Direen admits that Applegate itself is insufficient to show critical limitations. For example, all independent claims of the '786 Patent require a memory module to receive and process at least one command. However, Dr. Direen states that "[f]or a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference," and that "[t]he DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory." (Ex. 1002-A at 3.) Therefore, Petitioner's own expert admits that he needs to rely on an unauthenticated, undated document pulled off the Internet in order to meet critical claim limitations not taught by the reference itself. And for at least the "increment counter" claim limitation of claims 1 and 9, Dr. Direen admits that even the purported datasheet in Ex. 1007 doesn't teach the limitation, but instead simply relies on assertions, unsupported by any evidence, that a person of ordinary skill in the art would simply know to do such a command. (*See*

Ex. 1002-A at 4-5.) Such "evidence" completely fails to meet Petitioner's burden to show a reasonable likelihood of proving anticipation by Applegate itself.

IX. DR. DIREEN'S DECLARATION IS FATALLY FLAWED AND SHOULD BE AFFORDED NO WEIGHT

The Board should afford no weight to the opinions of Dr. Direen as reflected in his declaration (Ex. 1002) and the claim chart attached thereto (Ex. 1002-A). Most importantly, Dr. Direen displays a fundamental misunderstanding of the legal standard for anticipation and admits that Applegate alone does not disclose each and every element of the claims. As discussed above, while Dr. Direen opines that Applegate anticipates claims 1-16, his opinions improperly rely on teachings from the "DS1982 datasheet" to support his anticipation conclusion. (*See, e.g.* Ex. 1002-A at 2, 3-4, 7, 11, 14, 15, 16, 21, 26, 27, 29 (citing DS1982 datasheet).) As one particularly egregious example, in his claim chart supporting anticipation, Dr. Direen expressly states that "[f]or a POSITA to fully understand the Applegate teaching, the Dallas Semiconductor DS1982 datasheet will be incorporated by reference" and "[t]he DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory." (Ex. 1002-A at 3.) It is axiomatic that to establish anticipation, each and every element in a claim must be found in a single prior art reference." *ZTE Corp.*, IPR2013-00134, Paper 12 at 24 (PTAB June 19, 2013) (*citing Karsten Mfg. Corp.*, 242 F.3d at 1383); *NetMoneyIn, Inc.*, 545 F.3d at

1369). Dr. Direen's testimony advances a far different ground of invalidity (obviousness under § 103) than the Petition (anticipation under § 102), and thus implicitly admits that the challenged claims are *not* anticipated.

Dr. Direen also makes numerous arguments not contained in the Petition, in clear violation of the Board trial rules and practices. 37 C.F.R. § 42.104(b)(4) & (5). For example, Dr. Direen makes inherency arguments not advanced in the Petition. (*See, e.g.,* Ex. 1002-A at 10 (regarding Claim 3, opinion that "[i]t is inherent in Applegate's teaching that the gram counter will be updated by a value specified in a command and not simply incremented by 1").) Additionally, Dr. Direen's declaration includes two grounds that appear nowhere in the Petition.

Table 1

Ground	Claims	Basis	Prior Art
1	1 - 16	102	Applegate
2	2, 3, 14	103	Applegate & Hama
3	1 - 16	103	Applegate, PK, Hama, Bruce

As shown above in Table 1 (Ex. 1002, Direen Decl. at 20), Dr. Direen alleges a Ground 2 challenging claims 2, 3 and 14 as rendered obvious by Applegate in view of Hama. Dr. Direen also identifies a Ground 3 challenging claims 1-16 as obvious in light of Applegate, "a POSITA's knowledge," Hama, and Bruce. (*See id*.) Yet, these two grounds are not identified, let alone addressed, in the Petition.

The PTAB has repeatedly found that citing an expert declaration or claim charts to support "statements that are not otherwise supported in the Petition" amounts to an impermissible incorporation by reference. *See, e.g. Plant Science, Inc. v. The Andersons, Inc.*, IPR2014-00939, Paper 8 at 15 (PTAB Dec. 14, 2014); *Cisco Systems, Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 at 7-10 (PTAB Aug. 29, 2014) (Informative Decision of the Board). Under similar circumstances, the PTAB routinely does not "consider information presented in the Declaration but not discussed sufficiently in the Petition," and should not consider such arguments here. *2Wire, Inc. v. TQ Delta*, LLC, IPR2015-00239, Paper 18 at 10 (PTAB May 29, 2015). For at least these reasons, the Board should not afford Dr. Direen's Declaration any weight to the extent it is necessary to support Petitioner's technical arguments.

X. THE PETITION SHOULD BE DENIED IF THE BOARD FINDS ONLY A REASONABLE LIKELIHOOD OF PREVAILING ON A SUBSET OF CLAIMS

Although the Petition and supporting declaration do not show a reasonable likelihood of prevailing on *any* asserted Ground, if the Board finds that the Petition has shown a reasonable likelihood of prevailing *only* as to a small subset of the challenged claims, the Board should exercise its discretion to deny the Petition in its entirety. *See Chevron Oronite Co. LLC v. Infineum USA LP,* IPR2018-00923, Paper 9 at 11 (PTAB Nov. 7, 2018) (Informative Decision of the Board); *Deeper, UAB v.*

Vexilar, Inc., IPR2018-01310, Paper 7 at 42-43 (PTAB Jan. 24, 2019) (Informative Decision of the Board).

XI. CONCLUSION

For the reasons discussed above, Patent Owner requests that the Board deny the Petition.

Respectfully submitted,

Date: November 6, 2019

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that this brief complies with the type-volume limitations of 37 CFR §42.24. This brief contains 8,370 words as calculated by the "Word Count" feature of Microsoft Word for Office 365, the word processing program used to create it.

Date: November 6, 2019

/Anita Chou/
Anita Chou, Paralegal
Perkins Coie LLP

CERTIFICATE OF SERVICE

The undersigned hereby certifies that service on Petitioner was made as follows, in accordance with 37 CFR 42.6(e):

Date of service:	November 6, 2019
Manner of service:	1. Electronic submission through the USPTO Patent Trial and Appeal Board End-to-End System 2. Electronic mail
Document(s) served:	**PATENT OWNER PRELIMINARY RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,884,786**
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