

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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UNIVERSAL IMAGING INDUSTRIES, LLC,  
Petitioner,

v.

LEXMARK INTERNATIONAL, INC.,  
Patent Owner.

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IPR2019-01380  
Patent 7,844,786 B2

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Before JUSTIN T. ARBES, DAVID C. MCKONE, and  
GREGG I. ANDERSON, *Administrative Patent Judges*.

ANDERSON, *Administrative Patent Judge*.

DECISION

Denying Institution of *Inter Partes* Review  
35 U.S.C. § 314, 37 C.F.R. § 42.4

## I. INTRODUCTION

Universal Imaging Industries, LLC (“Petitioner”), filed a Petition requesting *inter partes* review of claims 1–16 of U.S. Patent No. 7,844,786 B2 (Ex. 1001, “the ’786 patent”).<sup>1</sup> Paper 1 (“Pet.”). Lexmark International, Inc. (“Patent Owner”), filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

We have jurisdiction under 35 U.S.C. § 314. Upon considering the record and for reasons discussed below, we deny institution of *inter partes* review.

## II. BACKGROUND

### A. *Real Party-in Interest*

Petitioner identifies Universal Imaging Industries, LLC, as the only real party-in-interest. Pet. 1. Patent Owner identifies Lexmark International, Inc., as the only real party-in-interest. Paper 4, 2.

### B. *Related Matters*

Petitioner advises us that Patent Owner has asserted the ’786 patent against Petitioner in *Lexmark International, Inc. v. Universal Imaging Industries, LLC*, case 8:18-cv-01047-EAK-AEP (M.D. Fla.) (“Related Litigation”). Pet. 1; Paper 4, 3. Patent Owner also has asserted U.S. Patent No. 8,966,193 B2 (“’193 patent”) in the Related Litigation and has filed a petition for *inter partes* review of the ’193 patent, IPR2019-01381 (“’1381 IPR”). Pet. 1; Paper 4, 3.

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<sup>1</sup> The application for the ’786 patent was filed April 22, 2008, and is a division of US 11/154,117, filed June 16, 2005, now US 7,426,613 B2. Ex. 1001, code (62). Patent Owner’s Preliminary Response does not raise any issue regarding whether any references relied on in the challenge qualify as prior art.

Patent Owner lists eight additional petitions for *inter partes* review which have been filed by Petitioner against patents assigned to Patent Owner. Paper 4, 3–4.

### *C. Technology and the '786 Patent*

The '786 patent describes memories, command protocols, and electrical interfaces for non-volatile memories utilized in recording the usage of, for example, printing cartridges for imaging and printing devices. Ex. 1001, 1:14–25. “[U]sage may be recorded based upon the number of pages printed by the device, or based upon the partial or full depletion of the print cartridges.” *Id.* at 1:26–28.

#### *1. Technology*

The non-volatile memory of computing devices has increased along with the speed needed to update or read the memory. Ex. 1001, 1:32–36. A greater number of non-volatile memory modules have to be updated in a shorter amount of time to keep up with the faster speed and page rates of printers. *Id.* at 1:36–46.

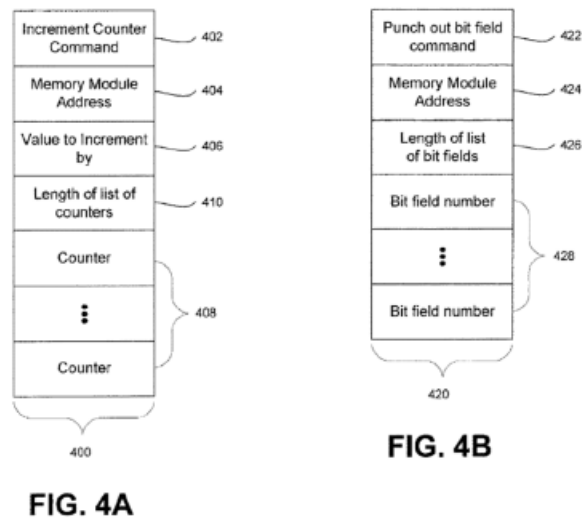
#### *2. '786 Patent (Ex. 1001)*

The '786 patent describes and claims methods for receiving, at one or more memory modules, a command transmitted from a processing device, where the command is an increment counter command operable to instruct the one or more memory modules to increment a counter within the one or more memory modules. The method also includes processing the command at the one or more memory modules.

Ex. 1001, 2:12–19. A specific command protocol sends one command to increment a counter within one or more memory modules. *Id.* at 11:60–12:13. A punch out bit field command identifies one of a plurality of memories and a location of a bit field in at least one of the memories. *Id.* at

3:25–28. A “punch out” is a change of a bit from an erased state to a programmed state, for example by changing from an initial value of “0” to a value of “1,” indicating the amount of printer toner that has been depleted.

*Id.* at 5:2–9. Figures 4A and 4B are reproduced below.



**Figures 4A and 4B are illustrative command protocols.**

Ex. 1001, 4:13–14. The first command protocol shown in Figure 4A is increment counter command 402. *Id.* at 11:61–64, 12:15–16. As shown in Figure 4B, another command is punch out bit field command 422, including the address of memory module 424 and the addresses of specific bit fields 428. *Id.* at 12:33–39.

#### *D. Illustrative Claim*

Claims 1, 9, and 16 are independent method claims. Claims 2 through 8 depend from claim 1 and claims 10 through 15 depend from claim 9. Claim 1 is illustrative and is reproduced below.

- 1[a)]<sup>2</sup> A method of updating memory modules comprising,
- [b)] receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises
- a) an increment counter command operable to instruct the one or more memory modules to increment the counter within the one or more memory modules and
- b) a punch out bit field command operable to instruct the one or more memory modules to punch out a specified bit field within the one or more memory modules; and
- [c)] processing the command at the one or more memory modules.

Ex. 1001, 15:10–21.

#### *E. Evidence*

Petitioner relies on the following evidence.

1. Applegate, US 5,995,774, issued Nov. 30, 1999 (“Applegate,” Ex. 1004).
2. Bruce, US 5,822,251, issued Oct. 13, 1998 (“Bruce,” Ex. 1003).
3. Declaration of Harry Direen, Ph.D., PE. (“Direen Declaration,” Ex. 1002).

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<sup>2</sup> Petitioner identifies three limitations of claim 1 and the other independent claims as, for example, **a)**, **b)**, and **c)**. *See* Pet. 10–11 (claim 1). For purposes of this Decision, we will refer to Petitioner’s format by bolding the inserted parentheticals, e.g., **1a)**. We refer to the first clause of Petitioner’s limitation **1b)** as the “receiving . . . a command” limitation. When referring to the a) and b) recitations actually present in claim 1 we will omit bolding and refer to them as “claim limitation a)” (“increment counter command”) or “claim limitation b)” (“punch out bit field command”).

*F. Asserted Grounds*

Petitioner asserts that claims 1–16 (Pet. 2–3) are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. <sup>3</sup> §	Reference(s)/Basis
1–4, 6–14, 16	102	Applegate
5, 15	103	Applegate, Bruce

III. ANALYSIS

*A. Claim Construction*

In an *inter partes* review requested in a petition filed on or after November 13, 2018, we apply the same claim construction standard used in district courts in a civil action under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,343 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018). In this case, the Petition was filed on July 23, 2019, and we, therefore, apply that standard here. In so doing, we construe a claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). The

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<sup>3</sup> The Leahy-Smith America Invents Act (AIA), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), amended 35 U.S.C. §§ 102 and 103, and those amendments became effective March 16, 2013. The earliest effective filing date for the ’786 patent claims is June 16, 2005, which is before the effective date of the relevant sections of the AIA. *See supra* n.1. Thus, on the present record, the grounds asserted are under the pre-AIA versions of §§ 102 and 103.

“specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess.” *Phillips*, 415 F.3d at 1316. “[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *accord Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Neither party believes any term requires construction. Pet. 5; Prelim. Resp. 12–13. We agree that no express construction is required in order to resolve the dispute. We apply the plain and ordinary meaning of the claim language as understood by a person of ordinary skill in the art.

#### *B. Legal Standard for Anticipation*

In order for a prior art reference to serve as an anticipatory reference, it must disclose every limitation of the claimed invention, either explicitly or inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

Anticipation “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a person of ordinary skill in possession of the invention.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008) (citing *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003); *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1267–69 (Fed. Cir. 1991)).

[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.

*Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Whether a patent is invalid as anticipated is a two-step inquiry. *See Power Mosfet Tech., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1406 (Fed. Cir. 2004). The first step requires construction of the claims. *Id.* The second step in the analysis requires a comparison of the properly construed claim to the prior art. *Id.*

### *C. Legal Standard for Obviousness*

A patent claim is unpatentable as obvious if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a).

“The ultimate determination of obviousness is a question of law, but that determination is based on underlying factual findings . . . . The underlying factual findings include (1) ‘the scope and content of the prior art,’ (2) ‘differences between the prior art and the claims at issue,’ (3) ‘the level of ordinary skill in the pertinent art,’ and (4) the presence of secondary considerations of nonobviousness such ‘as commercial success, long felt but unsolved needs, failure of others,’ and unexpected results. *In re Nuvasive, Inc.*, 842 F.3d 1376, 1381 (Fed. Cir. 2016) (citing, *inter alia*, *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)).

“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Furthermore, in assessing the prior art, the Board must consider whether a person of ordinary skill would have been



motivated to combine the prior art to achieve the claimed invention.

*Nuvasive*, 842 F.3d at 1381. As the Federal Circuit found, in quoting from the Supreme Court’s decision in *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–419 (2007), “‘because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known,’ ‘it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.’” *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 991–992 (Fed. Cir. 2017).

*D. Person of Ordinary Skill in the Art*

Petitioner alleges that as of the earliest priority date of the ’786 patent, “a person of ordinary skill in the art would have a bachelor’s degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems, including both hardware and embedded software design.” Pet. 5 (citing Ex. 1002 ¶¶ 29–32). Patent Owner does not believe the level of skill “is material to the outcome” but, nonetheless, argues that the experience of a person of ordinary skill would include “printer design” and “printer applications.” Prelim. Resp. 12.

No claim recites either “printer design” or “printer applications.” All the challenged claims are directed to “memory modules.” Only one of the 16 claims of the ’786 patent (claim 16) recites that the memory modules are in an “imaging device.” The word “print” appears in the Specification in the context of “imaging and printing devices” and “print cartridges.” *See, e.g.*, Ex. 1001, 4:35–40 (“imaging and printing devices”), 11:1–5 (“print cartridges”). The Specification, however, states that the invention relates to “addressing schemes, command protocols, and electrical interfaces for

non-volatile memories utilized in recording the usage of a device,” without limitation to a particular type of device. *Id.* at 1:14–17. The Specification may be used to determine the knowledge of a person of ordinary skill in the art. *In re Morsa*, 803 F.3d 1374, 1378 (Fed. Cir. 2015). We note also that the applied prior art includes printer references which reflect the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); Ex. 1004, Abs.

We are not persuaded that the experience of a skilled artisan would have been limited to printer design and applications. Accordingly, we agree with and adopt Petitioner’s proposal.

*E. Claims 1–4, 6–14, and 16 as Anticipated by Applegate*

Petitioner argues claims 1–4, 6–14, and 16 are anticipated by Applegate. Pet. 2–3, 9–26. Petitioner relies on the Direen Declaration to support some, but not all, of its arguments. Ex. 1002, App., 1–24, 26–30.

*1. Applegate (Ex. 1004)*

Applegate discloses an “improved electrophotographic (EP) printer . . . having a detachable process cartridge that contains a non-volatile memory device.” Ex. 1004, Abs. Applegate discloses, in its Background of the Invention section, that “[t]he non-volatile memory comprises an [erasable programmable read-only memory (EPROM)] integrated circuit, which has a new count value incremented every time the printer produces a new printed sheet of print media.” *Id.* at 2:17–21.

Applegate explains that

[a] toner “gas-gauge” is created which uses “bucket levels” as discrete steps to indicate how much of the measured physical toner material actually remains within the toner reservoir. After a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is

irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage.

Ex. 1004, Abs.

Applegate discloses that once toner information on usage has been stored in the EPROM memory device and a certain amount of toner has been dispensed, the stored information cannot be changed and is irreversible.

[O]ne of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage. In this invention, the EPROM memory device acts as a “write once read often” memory device, because the EPROM cannot be erased by ultraviolet light, since the window through which this normally occurs is permanently sealed closed by the manufacturer (i.e., Dallas Semiconductor, Inc. in the preferred embodiment). The burning of a bit in the EPROM memory device occurs at “critical” transitions, which include times when a new bucket level has been reached (i.e., when the amount of toner material remaining in the toner reservoir has decreased to the point where the next lower bucket level is declared to be the “current” bucket level).

Ex. 1004, 6:10–27. The EPROM, preferably a “Dallas Semiconductor, Inc. integrated circuit, part number DS1982,” is not erasable in that it is a “one-way” device that can be written to only once, but read many times, which is known as an “add-only memory.” *Id.* at 12:40–52.

Figure 5 of Applegate is reproduced below.

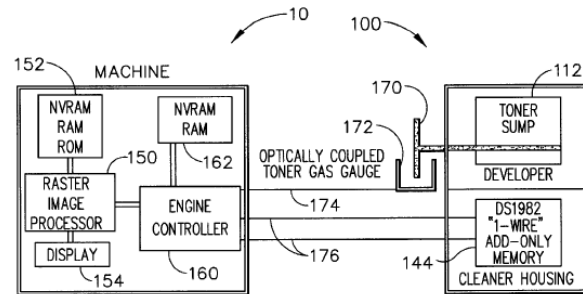


FIG. 5

**Figure 5 is a diagrammatic view of a combination of printer 10 and process cartridge 100.**

Ex. 1004, 10:63–65. As shown in Figure 5, engine controller 160 is part of print engine 36 (*see id.*, Fig. 1), and “is in communication with its own set of RAM and NVRAM.” *Id.* at 11:20–23. Still referring to Figure 5, the engine controller “is also in communication with an optically coupled toner ‘gas gauge sensor’ 172, via an electrical conductor 174.” *Id.* at 11:31–32. An interface between the engine controller and EPROM 144 “is preferably via a two-wire electrically conductive path 176.” *Id.* at 11:36–38.

## 2. Analysis of Claim 1

We analyze claim 1 as illustrative of independent claims 9 and 16.

### a. “receiving . . . a command”

Claim 1 recites, in part, “receiving, at one or more memory modules, a command transmitted from a processing device, wherein the command comprises” two particular commands. Petitioner argues “Applegate discloses receiving a command transmitted from a processing device.” Pet. 10 (citing Ex. 1002, App. 2–3; Ex. 1004, Figs. 5–6; 11:31–38). Figure 5, reproduced above, “illustrates in block diagram form some of the major components of the printer 10 and how it interfaces with the process cartridge 100.” Ex. 1004, 10:63–65. The “interface between engine controller 160

and the EPROM 144 is preferably via a two-wire electrically conductive path 176.” *Id.* at 11:36–38, Fig. 5 (element 176). The “interface” described is the citation to Applegate at page 10 of the Petition. Applegate’s Figure 6 “illustrates the major components in block diagram form of the EPROM chip 144.” *Id.* at 12:53–54.

None of the citations to Applegate disclose any type of “command.” The Petition must “specify where each element of the claim is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4). We find the Petition’s citations to Applegate do not show where or how Applegate discloses the “receiving . . . a command” limitation.

The Petition’s citation to the Direen Declaration’s claim chart for claim 1 does not remedy the deficiencies in the Petition. *See* Pet. 10 (citing Ex. 1002, App., 2–7 (claim chart for claim 1)). The Direen Declaration alleges that Applegate discloses “receiving, at one or more memory modules, a command transmitted from a processing device.” Ex. 1002, App. 4. Applegate’s Abstract is quoted, but the Direen Declaration does not show how the quoted portions of the Abstract disclose the recited “receiving . . . a command.” The Applegate Abstract citation primarily refers to how the “EPROM memory device” stores “machine data” and is “irreversibly burned” to form a permanent record of toner usage. *Id.*

The Direen Declaration also cites to Applegate’s disclosure of an integrated circuit, the DS1982 integrated circuit. *Id.* at 3. Dr. Direen testifies the DS1982 datasheet “provides the explicit commands for reading and writing the non-volatile memory.” *Id.* at 4; *see also* Ex. 1007 (DS1982 datasheet). However, Petitioner alleges anticipation based on Applegate and Petitioner does not explain why the DS1982 datasheet is part of Applegate’s disclosure. Applegate specifically states that “EPROM 144 preferably

comprises a Dallas Semiconductor, Inc. integrated circuit, part number DS1982, which is a ‘one-wire’ read only memory device.” Ex. 1004, 12:39–47. Applegate makes no reference to the DS1982 datasheet, only the part.

Dr. Direen’s claim chart regarding claim 1’s preamble contends the DS1982 datasheet “will be incorporated by reference.” Ex. 1002, App. 3. Patent Owner argues that the DS1982 datasheet is not properly incorporated by reference in Applegate. *See* Prelim. Resp. 2–3, 36. We agree.

[A]nticipation requires that the four corners of a single, prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. Material not explicitly contained in the single, prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document. Incorporation by reference provides a method for integrating material from various documents into a host document—a patent or printed publication in an anticipation determination—by citing such material in a manner that makes clear that the material is effectively part of the host document as if it were explicitly contained therein. *To incorporate material by reference, the host document must identify with detailed particularity what specific material it incorporates and clearly indicate where that material is found in the various documents.*

*Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) (citations omitted) (emphasis added). Whether a patent describes material to be incorporated by reference with sufficient particularity is assessed from the perspective of a person of ordinary skill in the art. *Id.* at 1283.

The DS1982 datasheet is not incorporated by reference at least because it was not identified; only the DS1982 part itself is disclosed. Further, as Patent Owner notes, the DS1982 datasheet is undated. Prelim. Resp. 36; *see* Ex. 1007.

As noted above, Patent Owner argues Dr. Direen testifies regarding obviousness by including the DS1982 datasheet as the basis for his conclusions, when Petitioner's asserted ground is based on anticipation. Prelim. Resp. 39–40. We agree. Indeed, the claim chart of the Direen Declaration includes an entire column devoted to “Obviousness Notes,” which acknowledges the DS1982 memory module, as opposed to the DS1982 datasheet, “does not include” the “increment counter command” recited in claim 1. Ex. 1002, App. 4. Thus, even if we were to credit Dr. Direen's testimony, that testimony does not support the anticipation challenge Petitioner actually raises in the Petition. That the Direen Declaration opines on obviousness when Petitioner's challenge is based on anticipation is also at issue in the discussion of the “increment counter command” in Section III.E.2.b below. Regardless, Petitioner does not argue obviousness.

We determine that the Direen Declaration is conclusory, does not support Petitioner's argument that Applegate discloses the “receiving . . . a command” limitation, and, as discussed below, is inconsistent with the Petition's theory of anticipation. *See infra* Section III.E.4. We give the Direen Declaration testimony little weight.

*b. “increment counter command”—claim limitation a)*

The “receiving . . . a command” limitation is analyzed in Section III.E.2.a above. It comprises two separate commands, claim limitations a) and b). The first command is claim limitation a), the “increment counter command.”

Petitioner argues Applegate discloses the “increment counter command.” Pet. 10 (citing Ex. 1004, 2:17–21). The preceding column 2 citation explains that “[t]he non-volatile memory comprises an [EPROM]

integrated circuit which has a new count value incremented every time the printer produces a new printed sheet of print media.” Petitioner also relies on Applegate’s disclosure of updating the toner gram count after each sheet is printed. *Id.* (citing Ex. 1004, 20:18–22).

Patent Owner argues Petitioner’s citations to Applegate make no mention of any “command” or an instruction to “increment a counter within the memory module.” Prelim. Resp. 20 (citing Ex. 2001<sup>4</sup> ¶¶ 100–101); *see also id.* ¶¶ 102–113. Patent Owner argues Petitioner’s mere citation to Applegate’s disclosure at column 2, beginning at line 17, set forth above, does not explain how the one or more memory modules are instructed to increment a counter or where the increment counter is located within the memory modules. *Id.* at 22 (citing Ex. 2001 ¶¶ 106–107). Patent Owner argues Applegate “says nothing about transmitting any command from the processing device to a memory module, and certainly not the increment counter command recited by the claims.” *Id.* (citing Ex. 2001 ¶¶ 106–107).

We agree with Patent Owner. Petitioner has not shown that Applegate discloses either the “receiving . . . a command” limitation, discussed in Section III.E.2.a above, or the “increment counter command.” Although Applegate’s Background of the Invention section discusses how certain consumables are counted, there is no associated command identified in the Petition or in Applegate. *See* Ex. 1004, 2:18–21 (EPROM integrated circuit “has a new count value incremented every time the printer produces a new printed sheet of print media”). The Petition must “specify where each element of the claim is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4). Petitioner has not shown where

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<sup>4</sup> Declaration of Jeffrey J. Folkins, Ph.D. (Ex. 2001).



Applegate discloses the “increment counter command.” As a result, the Petition lacks the specificity our rules require.

Petitioner does not cite to or in any other way connect the Direen Declaration to its showing on the “increment counter command.” Regardless, we have reviewed the Direen Declaration, which includes the following:

Assuming the Secure Memory IC<sup>[5]</sup> is an off-the-shelf device, these must be inherent capabilities of the off-the-shelf device. If the Secure Memory IC is not an off-the-shelf device, then the ’786 [patent] assumes a [person of ordinary skill in the art] has all the knowledge, understanding, and background to design a non-volatile memory device with:

- A data bus interface to an external processing unit.
- Command protocols for interfacing with a processing unit.
- Explicit command(s) for modifying a single bit in a bit field in the nonvolatile memory.
- Explicit command(s) for incrementing a specific counter within the nonvolatile memory.

Ex. 1002 ¶ 26. The Direen Declaration concludes that the “increment counter command,” described in the last bullet point above, was an “inherent capabilit[y]” of the Secure Memory IC, an “off-the-shelf device.” *Id.*, *see also id.* ¶ 23 (“While the ’786 specification does not mention a specific data bus standard, a POSITA will recognize the two-wire interface (Address/Data line and Clock line) as an I2C interface.”).

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<sup>5</sup> Dr. Direen’s reference is to Figure 1B of the ’786 patent which he states shows that “the data bus connections go[] straight to the Secure Memory IC.” Ex. 1002 ¶ 25; *see also id.* ¶ 24 (“Secure Memory Integrated Circuit (“IC”)” is element 152 of Figure 1B).

The paragraph 26 testimony is not a part of the claim chart provided by Dr. Direen. The Direen Declaration states that

Ex. 1002-A is a claim chart comparing Applegate in combination with the various prior art references to the claims of the '786 [patent]. *The claim chart provides the details of the comparisons and my analysis.*

Ex. 1002 ¶ 52 (emphasis added). We determine that the paragraph 26 testimony is not part of Dr. Direen's unpatentability analysis, which is set forth in the claim chart. Paragraph 26 falls under the heading "THE '786 PATENT." Ex. 1002, 8. The paragraph 26 testimony relates to the '786 patent and says nothing about Applegate. No testimony is provided that a person of ordinary skill would, with Applegate's disclosure available, "design a non-volatile memory device" with an "increment counter command." See Ex. 1002 ¶ 26. The Direen Declaration paragraph 26 is not a part of the Petition's showing regarding the "increment counter command."

Our functions do not encompass structuring a case for unpatentability. A petitioner for *inter partes* review bears the burden of demonstrating a reasonable likelihood of prevailing with respect to at least one challenged claim. 35 U.S.C. § 314(a). We are not tasked with analyzing the evidence submitted and tying it to the arguments made in the Petition that do not refer to that evidence. In this case, the uncited evidence is the Direen Declaration.

*c. "punch out bit field command"—claim limitation b)*

The second command of the "receiving . . . a command" limitation is claim limitation b), the "punch out bit field command." Petitioner argues Applegate "discloses the command comprises a punch out bit field command operable to instruct the one or more memory modules to punch

out a specified bit field within the one or more memory modules.” Pet. 11 (citing Ex. 1002 ¶ 43; Ex. 1004, Abs., 6:10–14 (“[A]fter a given amount of toner material has been dispensed through the developer unit, one of the bits of the EPROM memory device is irreversibly burned, thereby providing a permanent record on the process cartridge of a certain amount of toner usage.”)). Petitioner also provides a chart showing the alleged similarity of Applegate’s disclosure of “memory elements” clearing, irreversibly, Logic values of “1” to “0” to the ’786 patent’s “memory modules” clearing Logic values of “0” to “1.” *Id.* (citing Ex. 1004, 14:43–54; Ex. 1001, 5:2–13).

Patent Owner asserts that “Petitioner fails to show any teaching in Applegate of a punch out bit field command received and processed by memory modules.” Prelim. Resp. 24 (citing Ex. 2001 ¶¶ 114–116). Patent Owner contends, as it did in connection with the “increment counter command,” that the cited portions of Applegate do not disclose “any command, let alone the required command instructing the memory module to punch out a ‘specified bit field.’” *Id.* at 25 (citing Ex. 2001 ¶¶ 117–118) (emphases omitted).

Petitioner’s showing is insufficient to establish that the “punch out bit field command” is disclosed by Applegate. The cited paragraph 43 of the Direen Declaration compares “the ’786 [patent] with Applegate,” opining that “the purpose and process of changing the state of a bit in a bit-field to represent the amount of toner used is the same.” Ex. 1002 ¶ 43. The testimony does not address the “command” aspect of the limitation.

We note, as we did with the “increment counter command” limitation, the Direen Declaration arguably includes an opinion that the “punch out bit field command” is inherent in a “Secure Memory IC” type of device. *See* Ex. 1002 ¶ 26. The Direen Declaration asserts a person or ordinary skill

would “design a non-volatile memory device with . . . [e]xplicit command(s) for modifying a single bit in a bit field in the nonvolatile memory.” *Id.*

However, as discussed in connection with the “increment counter command,” there is no testimony that ties this conclusion about the ’786 patent to the challenge based on Applegate and, regardless, it is not cited anywhere in the Petition.

### *3. Analysis of Claims 2–4, 6–14, and 16*

Independent claims 1, 9, and 16 all recite “receiving . . . a command.” Ex. 1001, 15:11–12 (claim 1), 16:2–3 (claim 9), 16:35–36 (claim 16). All of the independent claims also have specific commands. Claims 1 and 9 each recite an “increment counter command” and a “punch out bit field command.” *Id.* at 15:13, 16 (claim 1), 16:4, 7 (claim 9). Claim 16 recites a “command . . . indicative of usage of toner or ink.” *Id.* at 16:36–37.

Claim 16 is similar to claims 1 and 9 in that the “bit field command” recited in claims 1 and 9 is described in the ’786 patent as relating to reservoirs of ink or toner cartridges. *Id.* at 4:64–5:15 (describing how bit fields are used to record the depletion of reservoirs of ink or toner cartridges).

The Petition alleges that claim 9 is identical to claim 1 but two limitations are reversed. Pet. 17. The showing for limitation 9**b**) is the same as that made for limitation 1**b**). *Compare* Pet. 10 (claim 1) *with id.* at 18 (claim 9). Petitioner’s showing for claim 16 is similar to its showings made for claims 1 and 9. *See id.* at 11 (claim 1), 19 (claim 9), 25 (all citing Ex. 1004, 14:43–54; Ex. 1001, 5:2–13 in side-by-side table). Petitioner’s arguments for claim 16 are very similar to those made regarding the “punch out bit field command” of claims 1 and 9. *See id.* at 24–25.

The Direen Declaration support for claims 9 and 16 is similar to what is presented for claim 1 and includes the same deficiencies. For example,

Dr. Direen again relies on the DS1982 datasheet in an apparent obviousness combination (rather than the anticipation challenge presented by Petitioner). Ex. 1002, App. 16 (claim 9), 27 (claim 16). Both of the cited portions of the Direen Declaration allege “[t]he DS1982 datasheet provides the explicit commands for reading and writing the non-volatile memory.” As explained in connection with claim 1, the DS1982 datasheet is not part of Applegate’s disclosure; is not incorporated by reference; and presents an obviousness challenge based on Applegate and the DS1982 datasheet when the challenge is anticipation based on Applegate. *See supra* Section III.E.2.a.

For the same reasons discussed in connection with claim 1, Petitioner has not shown a reasonable likelihood of prevailing as to claims 9 and 16 as anticipated by Applegate. Dependent claims 2–4 and 6–8 depend from claim 1. Dependent claims 10–14 depend from claim 9. As a result, Petitioner has not shown a reasonable likelihood of prevailing as to any of the dependent claims as anticipated by Applegate as well.

#### *4. Inherency and Inconsistent Theories*

The Petition does not allege any of the “receiving . . . a command,” “increment counter command,” or “punch out bit field command” limitations is inherently disclosed by Applegate. If Petitioner intends to rely on inherency, the Petition must include an argument regarding inherency. *See Denso Corp. v. Lee & Hates PLLC*, IPR2013-00027, Paper 16, 6 (PTAB June 24, 2013); *see also* 37 C.F.R. § 42.22(a)(2) (a petition “must include . . . a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent”).

The Petition alleges specific disclosures of Applegate disclose the recited commands. Pet. 10–11. Conversely, the Direen Declaration asserts that the ’786 patent describes Secure Memory IC “inherent capabilities” for

the recited command limitations. Ex. 1002 ¶ 26. The Direen Declaration also submits an obviousness theory by relying on the DS1982 datasheet. The Petition relies on anticipation. *See* Section III.E.2 above. These theories are inconsistent and, for reasons discussed above, neither is sufficient.

It is not our role to pick a theory for Petitioner regarding conflicting options presented in the Petition and the Direen Declaration, and then to apply that selected theory to the challenged independent and dependent claims. *Cf. Schumer v. Lab. Comput. Sys., Inc.*, 308 F.3d 1304, 1316 (Fed. Cir. 2002) (“It is not our task, nor is it the task of the district court, to attempt to interpret confusing or general testimony to determine whether a case of invalidity has been made out . . . .”). We will not, and cannot, piece together Petitioner’s inconsistent and contradictory arguments into a cogent and coherent explanation that supports anticipation. Rather, we must evaluate the Petition’s arguments as presented. *See Magnum*, 829 F.3d at 1380–1381 (stating that “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond,” and is not “free to adopt arguments on behalf of petitioners” (citations omitted)).

*5. Summary of Claims 1–4, 6–14, and 16 as Anticipated by Applegate*

Petitioner has not shown a reasonable likelihood that claims 1–4, 6–14, and 16 are anticipated by Applegate.

*F. Claims 5 and 15 as Obvious Over Applegate and Bruce*

Petitioner argues claims 5 and 15 would have been obvious over Applegate and Bruce. Pet. 2–3, 26–28. Petitioner relies on the Direen Declaration to support its arguments. Ex. 1002, App., 12–13, 25.

*1. Applegate (Ex. 1004)*

Applegate is described in Section III.E.1 above.

*2. Bruce (Ex. 1003)*

Bruce discloses a “flash-memory system” which is expandable. Ex. 1003, Abs. Bruce explains that “[a] busy signal is usually provided by each flash-memory chip to indicate when the read, write, or erase operation has completed. The busy signal allows a local processor to continue with other tasks while the flash-memory integrated circuit chip performs the flash operation.” *Id.* at 1:66–2:3.

*3. Analysis of Claims 5 and 15*

Claims 5 and 15 depend from claims 1 and 9, respectively. As discussed above, Petitioner has not shown a reasonable likelihood of prevailing in showing that either claim 1 or 9 is unpatentable. Bruce does not remedy any of the deficiencies noted in the Petition.

Petitioner has not shown a reasonable likelihood of prevailing in showing that claims 5 and 15 would have been obvious over Applegate and Bruce.

#### IV. CONCLUSION

Petitioner has not shown a reasonable likelihood of prevailing in showing that any of claims 1–16 are anticipated by Applegate or would have been obvious over Applegate and Bruce.

#### V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* as to the challenged claims of the ’786 patent, and no *inter partes* review is instituted.

IPR2019-01380  
Patent 7,844,786 B2

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